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AN-6094

Design Guideline for Flyback Charger Using FAN302HL/UL

1. Introduction

More than half of the external power supplies produced are used for portable electronics such as laptops, cellular phones, and MP3 players that require constant output voltage and current regulation for battery charging. For applications requiring precise Constant Current (CC) regulation, current sensing in the secondary side is always necessary, which results in sensing loss. For power supply designers faced with stringent energy-efficiency regulations, output current sensing is a design challenge.

The advanced PWM controller FAN302HL/UL can alleviate the burden of meeting international energy efficiency regulations in charger designs. The FAN302HL/UL family uses a proprietary primary-side regulation (PSR) technique where the output current is precisely estimated with only the information in the primary side of the transformer and controlled with an internal compensation circuit. This removes the output current sensing loss and eliminates all external current-control circuitry, facilitating a higher efficiency power supply design without incurring additional costs. A Green-Mode function with an extremely low operating current (200 μA) in Burst Mode maximizes the light-load efficiency, enabling conformance to worldwide Standby Mode efficiency guidelines.

This application note presents practical design considerations for flyback battery chargers employing the FAN302HL/UL. It includes instructions for designing the transformer and output filter, selecting the components, and implementing Constant Current (CC) / Constant Voltage (CV) control. The design procedure is verified through an experimental prototype converter using FAN302UL. Figure 1 shows a typical application circuit of a flyback converter using the FAN302HL/UL.

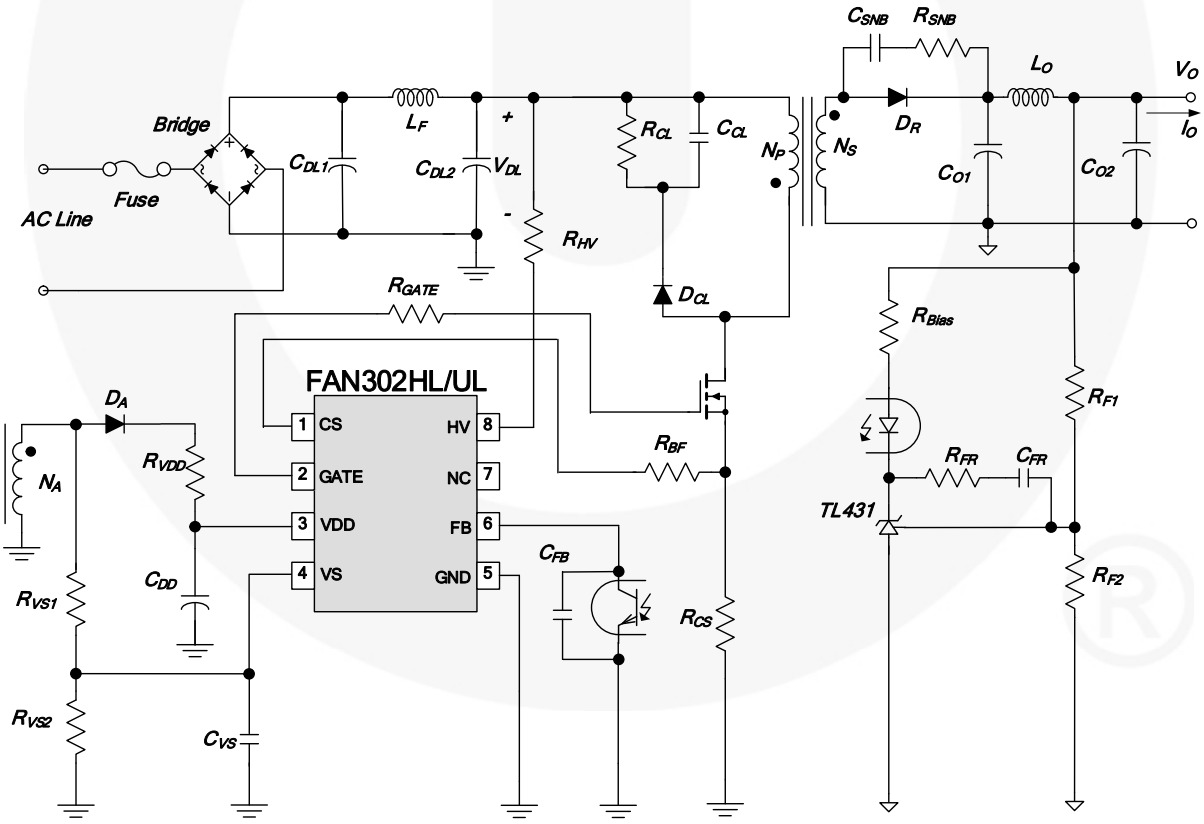


Figure 1. Typical Application Circuit

2. Operation Principle

2-1 Constant-Voltage Regulation Operation

Figure 2 shows the internal PWM control circuit of FAN302. The constant voltage (CV) regulation is implemented in the same way as the conventional isolated power supply, where the output voltage is sensed using voltage divider and compared with the internal 2.5 V reference of the shut regulator (KA431) to generate a compensation signal. The compensation signal is transferred to the primary side using an opto-coupler and applied to the PWM comparator (PWM.V) through attenuator Av to determine the duty cycle.

CC regulation is implemented internally without directly sensing the output current. The output current estimator reconstructs output current information (V_{CCR}) using the transformer primary-side current and diode current discharge time. V_{CCR} is then compared with a reference voltage (2.5 V) by an internal error amplifier and generates a $V_{EA.I}$ signal to determine the duty cycle.

$V_{EA.I}$ and $V_{EA.V}$ are compared with an internal sawtooth waveform (V_{SAW}) by PWM comparators PWM.I and PWM.V, respectively, to determine the duty cycle. As seen in Figure 2, the outputs of two comparators (PWM.I and PWM.V) are combined with the OR gate and used as a reset signal of flip-flop to determine the MOSFET turn-off instant. The lower signal, $V_{EA.V}$ and $V_{EA.I}$, determines the duty cycle, as shown in Figure 3. During CV regulation, $V_{EA.V}$ determines the duty cycle while $V_{EA.I}$ is saturated to HIGH. During CC regulation, $V_{EA.I}$ determines the duty cycle while $V_{EA.V}$ is saturated to HIGH.

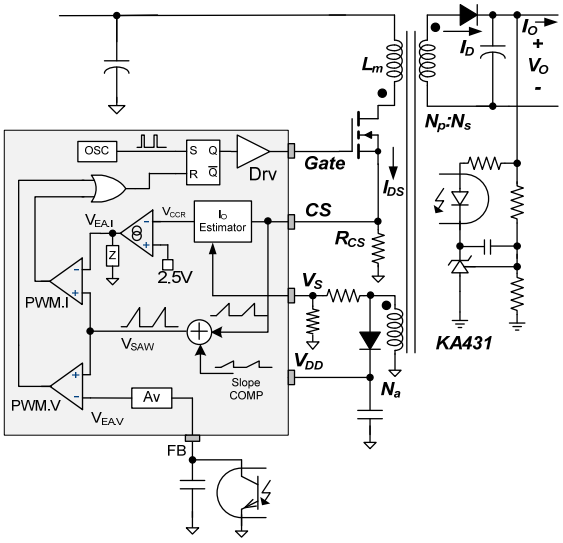


Figure 2. Internal PWM Control Circuit

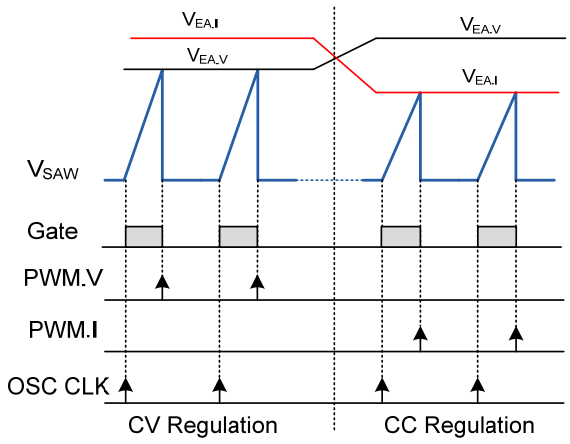


Figure 3. PWM Operation for CC and CV

Output Current Estimation

Figure 4 shows the key waveform of a flyback converter operating in Discontinuous Conduction Mode (DCM), where the secondary side diode current reaches zero before the next switching cycle begins. Since the output current estimator of FAN302 is designed for DCM operation, the power stage should be designed such that DCM is guaranteed for the entire operating range. The output current is obtained by averaging the triangular output diode current area over a switching cycle, as calculated by:

$$I_O = I_D^{AVG} = I_{PK} \frac{N_P}{N_S} \cdot \frac{t_{DIS}}{2t_S} \quad (1)$$

where I_{PK} is the peak value of the primary-side current; NP and NS are the number of turns of the transformer, primary side and secondary side, respectively; t_{DIS} is the diode current discharge time; and t_s is switching period.

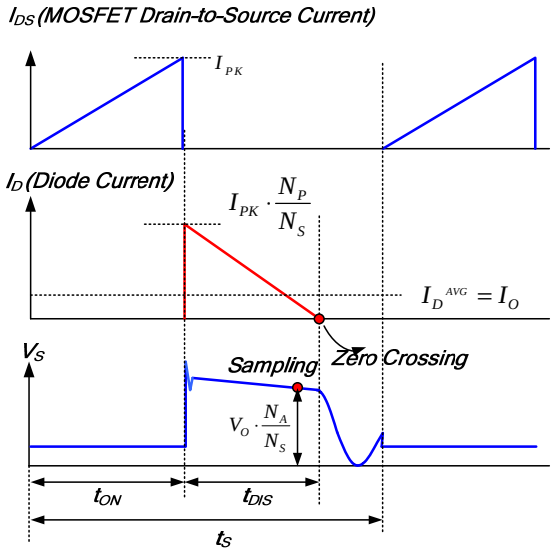


Figure 4. Key Waveforms of DCM Flyback Converter

3. Design Consideration

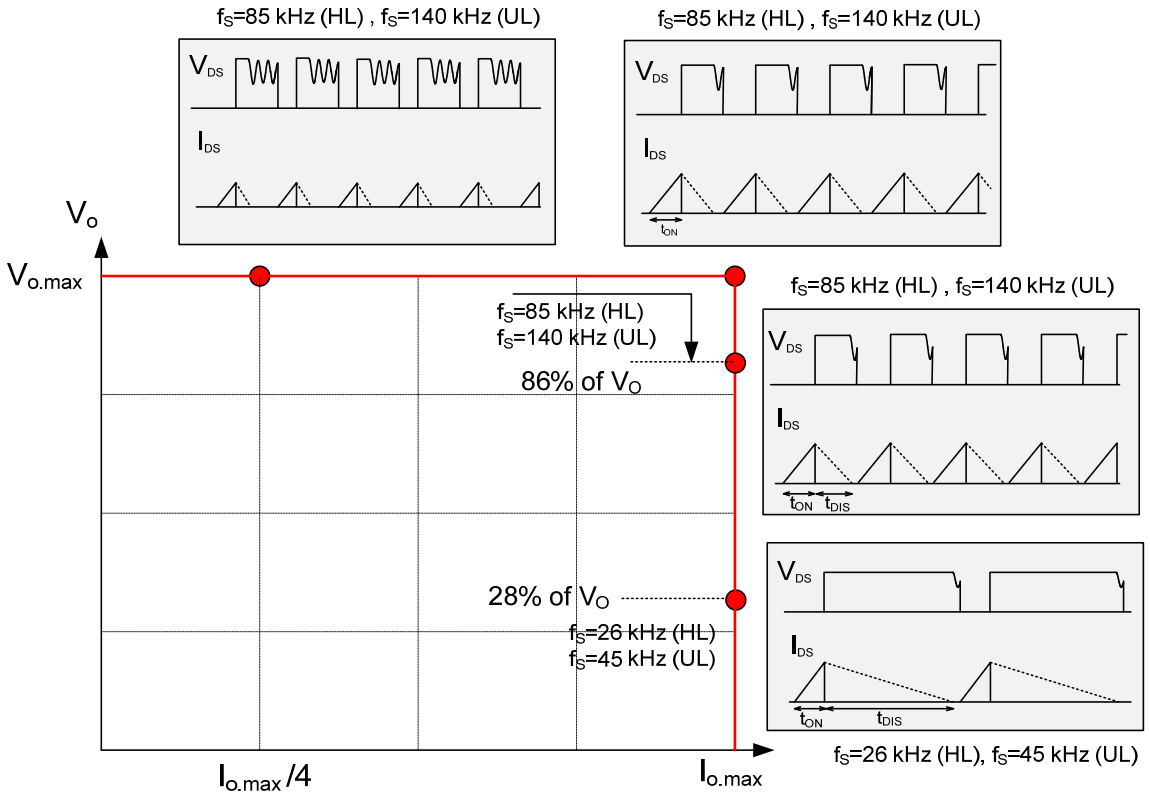


Figure 5. Operation Range of Charger with CC/CV

A battery charger power supply with CC output requires more design consideration than the conventional power supply with a fixed output voltage. In CC operation, the output voltage changes according to the charging condition of battery. The supply voltage for the PWM controller (V_{DD}), which is usually obtained from the auxiliary winding of the transformer, changes with the output voltage. Thus, the allowable V_{DD} operation range determines the output voltage variation range in CC regulation. FAN302 has a wide supply voltage (V_{DD}) operation range from 5 V up to 26.5 V, which allows stable CC regulation even with output voltage lower than a quarter of its nominal value.

Another important design consideration for CC operation is that the transformer should be designed to guarantee DCM operation over the whole operation range since the output current can be properly estimated only in DCM, as described in Section 2. As seen in Figure 5, the MOSFET conduction time (t_{ON}) decreases as output voltage decreases in CC Mode, which is proportional to the square root of the output voltage. Meanwhile, the diode current discharge time (t_{DIS}) increases as the output voltage decreases, which is inversely proportional to the output voltage. Since the increase of t_{DIS} is dominant over the decrease of t_{ON} in determining the sum of t_{ON} and t_{DIS}, the sum of t_{ON} and t_{DIS} tends to increases as output voltage decreases. When the sum of t_{ON} and t_{DIS} are same as the switching period, the converter enters CCM. FAN302 has a frequency-reduction function to prevent CCM operation by extending the switching period as the output voltage drops, as illustrated in Figure 6. The output voltage is indirectly sensed by sampling the transformer winding voltage (V_{SH}) around the end of diode current discharge time, as illustrated in Figure 4. The frequency-reduction profile is designed such that the on-time remains almost constant even when the output voltage drops in CC Mode.

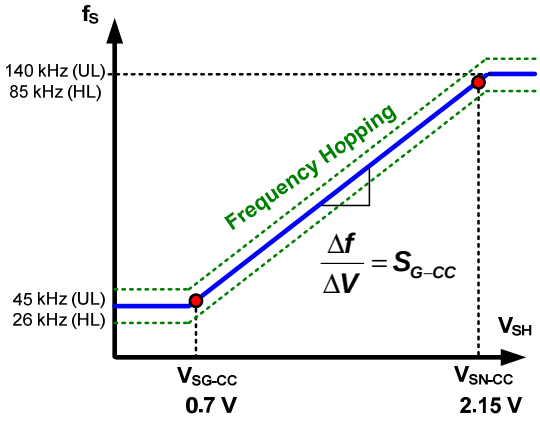


Figure 6. Frequency Reduction in CC Mode

4. Design Procedure

In this section, a design procedure is presented using the Figure 1 as a reference. An offline charger with 6 W / 5 V output has been selected as a design example. The design specifications are:

- Line Voltage Range: 90~264 V_{AC} and 60 Hz
- Nominal Output Voltage and Current: 5 V / 1.2 A
- Output Voltage Ripple: Less than 100 mV
- Minimum Output Voltage in CC Mode: 25% of Nominal Output (1.25 V)
- Maximum Switching Frequency: 140 kHz

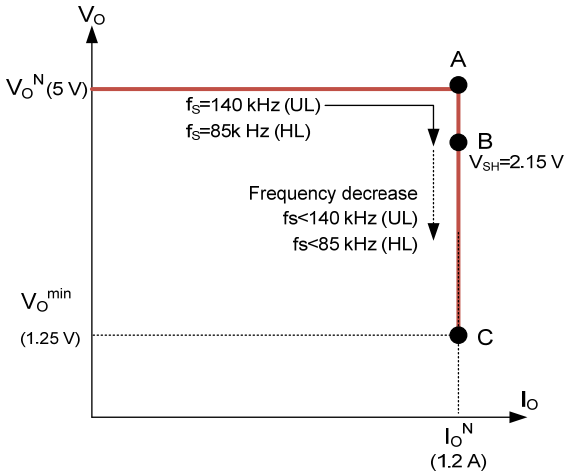


Figure 7. Output Voltage and Current Operating Area

[STEP-1] Estimate the Efficiencies

The charger application has output voltage and current that change over a wide range, as shown in Figure 7, depending on the charging status of the battery. Thus, the efficiencies and input powers of various operating conditions should be specified to optimize the power stage design. The critical operating points for design:

- **Operating Point A**, where the output voltage and current reach maximum value (nominal output voltage and current).
- **Operating Point B**, where the frequency drop is initiated to maintain DCM operation.
- **Operating Point C**, where the output has its minimum voltage in CC Mode.

Typically, low line is the worst case for the transformer design since the largest duty cycle occurs at the minimum input voltage condition. As a first step, the following parameters should be estimated for low line.

- Estimated overall efficiency for operating points A, B, and C ($E_{FF@A}$, $E_{FF@B}$, and $E_{FF@C}$): The overall power conversion efficiency should be estimated to calculate the input power and maximum DC link voltage ripple. If no reference data is available, use the typical efficiencies in Table 1.
- Estimated primary-side efficiency ($E_{FF.P}$) and secondary-side efficiency ($E_{FF.S}$) for operating point A, B, and C. Figure 8 shows the definition of primary-side and secondary-side efficiencies. The primary-side efficiency is for the power transferred from the AC line to the transformer primary side. The secondary-side efficiency is for the power transferred from the transformer primary side to the power supply output.

Since the rectifier diode forward voltage drop does not change much with its voltage rating, the conduction loss of output rectifier diode tends to be dominant for a low output voltage application. Therefore, the distribution of primary-side and secondary-side efficiencies changes with the output voltage. With a given transformer efficiency, the secondary- and primary-side efficiency, ignoring the diode switching loss, are given as:

$$E_{FF.S} \cong E_{FF.TX} \cdot \frac{V_O{}^N}{V_O{}^N + V_F} \quad (2)$$

$$E_{FF.P} = E_{FF} / E_{FF.S} \quad (3)$$

where $E_{FF.TX}$ is transformer efficiency, typically 0.95~0.98%; $V_O{}^N$ is the nominal output voltage; and V_F is the rectifier diode forward-voltage drop.

Table 1. Typical Efficiency of Flyback Converter

Output Voltage	Typical Efficiency at Minimum Line Voltage	
	Universal Input	European Input
3.3 ~ 6 V	65 ~ 70%	67 ~ 72%
6 ~ 12 V	70 ~ 77%	72 ~ 79%
12 ~ 24 V	77 ~ 82%	79 ~ 84%

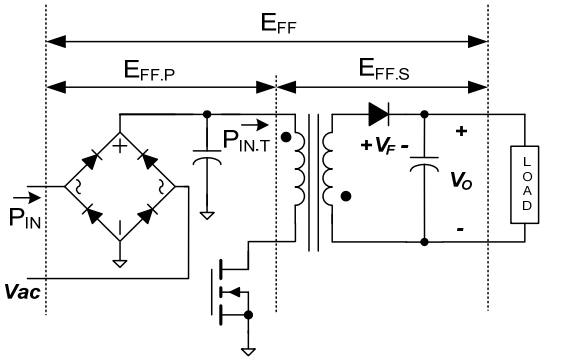


Figure 8. Primary-Side and Secondary-Side Efficiency

With the estimated overall efficiency, the input power at operating point A is given as:

$$P_{IN@A} = \frac{V_O{}^N I_O{}^N}{E_{FF@A}} \quad (4)$$

where $V_O{}^N$ and $I_O{}^N$ are the nominal output voltage and current, respectively.

The input power of transformer at operating point A is given as:

$$P_{IN.T@A} = \frac{V_O{}^N I_O{}^N}{E_{FF.S@A}} \quad (5)$$

To reduce the switching frequency as the output voltage drops in CC Mode for maintaining DCM operation, the output voltage needs to be sensed. FAN302 senses the output voltage indirectly by sampling auxiliary winding voltage just before the diode conduction finishes, as explained with Figure 4 in Section 2. Since the switching frequency starts decreasing as V_S sampling voltage drops below 2.15 V, as illustrated in Figure 6, the output voltage at operating point B can be obtained as:

$$V_{O@B} = \frac{2.15}{V_{SH@A}} \cdot (V_O{}^N + V_{F.SH}) - V_{F.SH} \quad (6)$$

where $V_{SH@A}$ is the V_S sampling voltage at operating point A, which is typically designed as 2.5 V and $V_{F.SH}$ is the rectifier diode forward voltage drop at the V_S sampling instant (85% of diode conduction time), which is typically about 0.1 V. Note that $V_{F.SH}$ is less than a third of V_F since the Vs voltage sampling occurs when the diode current is very small.

The overall efficiency at operating point B, where the frequency reduction starts, can be estimated as:

$$E_{FF@B} \cong E_{FF@A} \cdot \frac{V_{O@B}}{V_{O@B} + V_F} \cdot \frac{V_O{}^N + V_F}{V_O{}^N} \quad (7)$$

Note that the efficiency changes as the output voltage drops in CC Mode. The efficiency should be also estimated for each operating point (B and C).

The secondary-side efficiency at operating point B can be estimated as:

$$E_{FF.S@B} \cong E_{FF.S@A} \cdot \frac{V_{O@B}}{V_{O@B} + V_F} \cdot \frac{V_O{}^N + V_F}{V_O{}^N} \quad (8)$$

Then, the power supply input power and transformer input power at operating point B are given as:

$$P_{IN@B} = \frac{V_{O@B} \cdot I_O{}^N}{E_{FF@B}} \quad (9)$$

$$P_{IN.T@B} = \frac{V_{O@B} \cdot I_O{}^N}{E_{FF.S@B}} \quad (10)$$

The overall efficiency at operating point C can be approximated as:

$$E_{FF@C} \cong E_{FF} \cdot \frac{V_{O@C}}{V_{O@C} + V_F} \cdot \frac{V_O{}^N + V_F}{V_O{}^N} \quad (11)$$

where $V_{O@C}$ is the minimum output voltage for CC Mode at operating point C.

The secondary-side efficiency at operating point C can be estimated as:

$$E_{FF.S@C} \cong E_{FF.S@A} \cdot \frac{V_{O@C}}{V_{O@C} + V_F} \cdot \frac{V_O{}^N + V_F}{V_O{}^N} \quad (12)$$

Then, the power supply input power and transformer input power at operating point C are given as:

$$P_{IN@C} = \frac{V_{O@C} \cdot I_O{}^N}{E_{FF@C}} \quad (13)$$

$$P_{IN.T@C} = \frac{V_{O@C} \cdot I_O{}^N}{E_{FF.S@C}} \quad (14)$$

(Design Example)

To maximize efficiency, a low-voltage-drop Schottky diode whose forward voltage drop is 0.35 V is selected. Assuming the overall efficiency is 73% and the transformer efficiency is 97% at operating point A (nominal output voltage and current) for low line, the secondary-side efficiency is obtained as:

$$E_{FF.S@A} \cong E_{FF.TX} \cdot \frac{V_O{}^N}{V_O{}^N + V_F} = 0.907$$

Then, the input powers of the power supply and transformer at operating point A are obtained as:

$$P_{IN@A} = \frac{V_O{}^N I_O{}^N}{E_{FF@A}} = \frac{6}{0.73} = 8.22W$$

$$P_{IN.T@A} = \frac{V_O{}^N I_O{}^N}{E_{FF.S@A}} = \frac{6}{0.907} = 6.62W$$

The efficiencies at operating point B are:

$$E_{FF@B} \cong E_{FF@A} \cdot \frac{V_{O@B}}{V_{O@B} + V_F} \cdot \frac{V_O{}^N + V_F}{V_O{}^N} = 0.722$$

$$E_{FF.S@B} \cong E_{FF.S@A} \cdot \frac{V_{O@B}}{V_{O@B} + V_F} \cdot \frac{V_O{}^N + V_F}{V_O{}^N} = 0.896$$

Then, the input powers of the power supply and transformer at operating point B are obtained as:

$$P_{IN@B} = \frac{V_{O@B} I_O{}^N}{E_{FF@B}} = 7.07W$$

$$P_{IN.T@B} = \frac{V_{O@B} I_O{}^N}{E_{FF.S@B}} = 5.69W$$

The primary-side and secondary-side efficiencies at the operating point C are calculated as:

$$E_{FF@C} \cong E_{FF@A} \cdot \frac{V_{O@C}}{V_{O@C} + V_F} \cdot \frac{V_O{}^N + V_F}{V_O{}^N} = 0.610$$

$$E_{FF.S@C} \cong E_{FF.S@A} \cdot \frac{V_{O@C}}{V_{O@C} + V_F} \cdot \frac{V_O{}^N + V_F}{V_O{}^N} = 0.758$$

Then, the input powers of the power supply and transformer at operating point C are obtained as:

$$P_{IN@C} = \frac{V_{O@C} \cdot I_O{}^N}{E_{FF@C}} = 2.46W$$

$$P_{IN.T@C} = \frac{V_{O@C} \cdot I_O{}^N}{E_{FF.S@C}} = 1.98W$$

[STEP-2] Determine the DC Link Capacitor (C_{DL}) and the DC Link Voltage Range

It is typical to select the DC link capacitor as 2-3 μF per watt of input power for universal input range (90-264 V_{AC}) and 1 μF per watt of input power for European input range (195~265 V_{rms}). With the DC link capacitor chosen, the minimum DC link voltage is obtained as:

$$V_{DL@A}^{\min} = \sqrt{2 \cdot (V_{LINE}^{\min})^2 - \frac{P_{IN@A}(1-D_{ch})}{C_{DL} \cdot f_L}} \quad (15)$$

where V_{LINE}^{min} is the minimum line voltage; C_{DL} is the DC link capacitor; f_L is the line frequency; and D_{ch} is the DC link capacitor charging duty ratio defined as shown in Figure 9, which is typically about 0.2.

The maximum DC link voltage is given as:

$$V_{DL}^{\max} = \sqrt{2} \cdot V_{LINE}^{\max} \quad (16)$$

where V_{LINE}^{max} is the maximum line voltage.

The minimum DC link voltage and its ripple change with input power. The minimum input DC link voltage at operating point B is given as:

$$V_{DL@B}^{\min} = \sqrt{2 \cdot (V_{LINE}^{\min})^2 - \frac{P_{IN@B}(1-D_{ch})}{C_{DL} \cdot f_L}} \quad (17)$$

The minimum input DC link voltage at operating point C is given as:

$$V_{DL@C}^{\min} = \sqrt{2 \cdot (V_{LINE}^{\min})^2 - \frac{P_{IN@C}(1-D_{ch})}{C_{DL} \cdot f_L}} \quad (18)$$

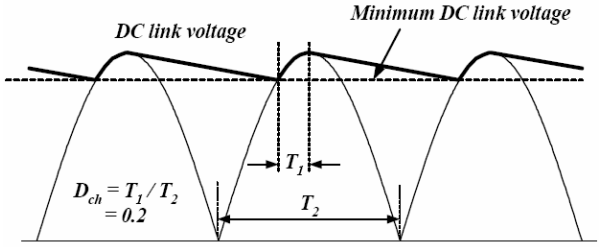


Figure 9. DC Link Voltage Waveforms

(Design Example) By choosing two 6.8 μF capacitors in parallel for the DC link capacitor, the minimum and maximum DC link voltages for each condition are obtained as:

$$V_{DL@A}^{\min} = \sqrt{2 \cdot (V_{LINE}^{\min})^2 - \frac{P_{IN@A}(1-D_{ch})}{C_{DL} \cdot f_L}}$$

$$= \sqrt{2 \cdot (90)^2 - \frac{8.22(1-0.2)}{2 \cdot 6.8 \times 10^{-6} \cdot 60}} = 90V$$

$$V_{DL}^{\max} = \sqrt{2} \cdot 264 = 373V$$

$$V_{DL@B}^{\min} = \sqrt{2 \cdot (V_{LINE}^{\min})^2 - \frac{P_{IN@B}(1-D_{ch})}{C_{DL} \cdot f_L}}$$

$$= \sqrt{2 \cdot (90)^2 - \frac{7.07(1-0.2)}{2 \cdot 6.8 \times 10^{-6} \cdot 60}} = 96V$$

$$V_{DL@C}^{\min} = \sqrt{2 \cdot (V_{LINE}^{\min})^2 - \frac{P_{IN@C}(1-D_{ch})}{C_{DL} \cdot f_L}}$$

$$= \sqrt{2 \cdot (90)^2 - \frac{2.46(1-0.2)}{2 \cdot 6.8 \times 10^{-6} \cdot 60}} = 117V$$

[STEP-3] Determine Transformer Turns Ratio

Figure 10 shows the MOSFET drain-to-source voltage waveforms. When the MOSFET is turned off, the sum of the input DC link voltage (V_{DL}) and the output voltage reflected to the primary side is imposed across the MOSFET, calculated as:

$$V_{DS}^{nom} = V_{DL}^{\max} + V_{RO} \quad (19)$$

where V_{RO} is reflected output voltage, defined as:

$$V_{RO} = \frac{N_p}{N_s}(V_O^N + V_F) \quad (20)$$

where N_P and N_S are number of turns for the primary side and secondary side, respectively.

When the MOSFET is turned on; the output voltage, together with input voltage reflected to the secondary, are imposed across the secondary-side rectifier diode calculated as:

$$V_D^{nom} = \frac{N_S}{N_P} V_{DL}^{\max} + V_O^N \quad (21)$$

As observed in Equations (19), (20), and (21); increasing the transformer turns ratio (N_P / N_S) increases voltage stress on the MOSFET while reducing voltage stress on the rectifier diode. Therefore, the N_P / N_S should be determined by the trade-off between the MOSFET and diode voltage stresses.

The transformer turns ratio between the auxiliary winding and the secondary winding (N_A / N_S) should be determined by considering the allowable IC supply voltage (V_{DD}) range. The V_{DD} voltage varies with load condition, as shown in Figure 11, where the minimum V_{DD} typically occurs at minimum load condition. Due to the voltage overshoot of the auxiliary winding voltage caused by the transformer leakage inductance; the V_{DD} at operating point C tends to be higher than the V_{DD} at minimum load condition.

The V_{DD} at minimum load condition is obtained as:

$$V_{DD}^{\min} \cong \frac{N_A}{N_S}(V_O + V_F) - V_{FA} \quad (22)$$

where V_{FA} is the diode forward-voltage drop of the auxiliary winding diode.

The transformer turns ratio should be determined such that V_{DD}^{min} is higher than the V_{DD} UVLO voltage, such as:

$$\frac{N_A}{N_S}(V_O + V_F) - V_{FA} > V_{UVLO}^{\max} + V_{MRGN} \quad (23)$$

Since the V_{DD}^{min} is related to standby power consumption, smaller N_A / N_S leads to lower standby power consumption. However, 2~3 V margin (V_{MRGN}) should be

added in to Equation (23), considering the V_{DD} ripple caused by Burst Mode operation at no-load condition.

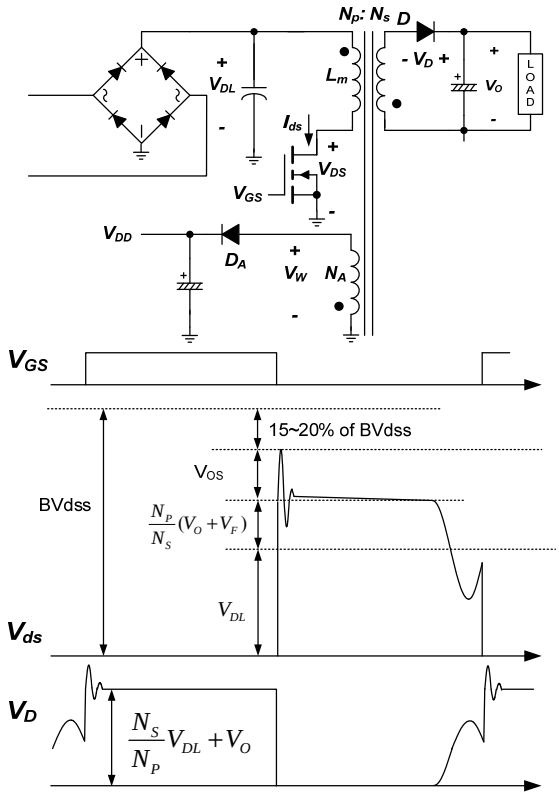


Figure 10. Voltage Stress on MOSFET and Diode

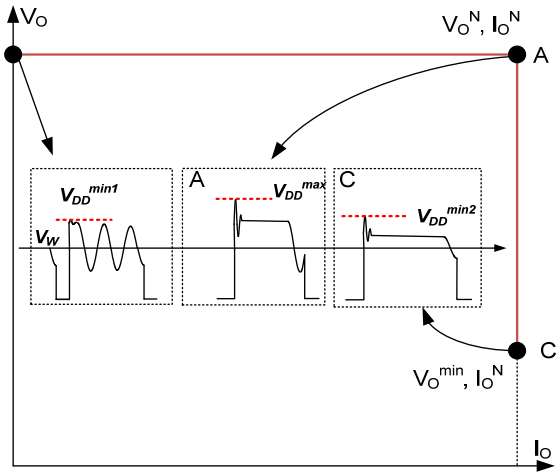


Figure 11. V_{DD} and Winding Voltage

(Design Example)

For a 700 V MOSFET to have 35% margin on V_{DS}^{nom}, the reflected output voltage should be:

$$V_{DS}^{nom} = 373 + V_{RO} < 0.65 \times 700 = 455V$$
$$\therefore V_{RO} < 82V$$

Setting V_{RO}=71 V, N_P / N_S is obtained as:

$$\frac{N_P}{N_S} = \frac{V_{RO}}{(V_o + V_F)} = \frac{71}{5.35} = 13.27$$

Then, the voltage stress of diode is obtained as:

$$V_D^{nom} = \frac{N_S}{N_P} V_{DL}^{max} + V_O = 33.13V$$

The allowable minimum V_{DD} is 5.3 V, considering the tolerances of UVLO. Considering voltage ripple on V_{DD} caused by burst operation at no-load condition, a 2 V margin is added for V_{DD} voltage calculation at no-load condition, calculated as:

$$V_{DD}^{min} = \frac{N_A}{N_S}(V_O + V_F) - V_{FA} > V_{UVLO}^{max} + V_{MRGN}$$
$$\Rightarrow \frac{N_A}{N_S}(5 + 0.35) - 0.7 > 5.3 + 2$$
$$\therefore \frac{N_A}{N_S} > 1.5$$

To minimize the power consumption of the IC by minimizing V_{DD} at no-load condition, N_A / N_S is determined as 1.6.

[STEP-4] Design the Transformer

Figure 12 shows the MOSFET conduction time (t_{ON}), diode current discharge time (t_{DIS}), and diode non-conduction time (t_{OFF}). For the transformer design, first determine how much non-conduction time (t_{OFF}) is used in DCM operation. The diode current discharge time increases as the output voltage drops in CC Mode. Even though t_{ON} decreases as output voltage drops, t_{ON} is proportional to the square root of the output voltage, while t_{DIS} is inversely proportional to the output voltage. Thus, the sum of t_{ON} and t_{DIS} tends to increase, which reduces the t_{OFF}, forcing the flyback converter with a fixed switching frequency into CCM operation as the output voltage drops.

Thus, operating point B, where the frequency reduction starts, is the worst case for determining the non-conduction time (t_{OFF}), as illustrated in Figure 12. t_{OFF} should be large enough to cover the transformer variation and frequency hopping. However, too large t_{OFF} increases RMS current of the primary side current. It is typical to set t_{OFF} as 15-20% of the switching period.

Once the t_{OFF} is determined at operating point B, the MOSFET conduction time is obtained as:

$$t_{ON@B} = \frac{1/f_S - t_{OFF@B}}{(1+\frac{N_S}{N_P}\cdot\frac{V_{DL@B}^{\min}}{V_{O@B}+V_F})} \quad (24)$$

Then, the transformer primary-side inductance can be calculated as:

$$L_m = \frac{(V_{DL@B}^{\min}\cdot t_{ON@B})^2}{2P_{IN.T@B}}\cdot f_S \quad (25)$$

Once the transformer primary-side inductance is determined, DCM operation at operating point C should be checked. To prevent CCM operation, FAN302 decreases the switching frequency as the output voltage drops, as illustrated in Figure 13. The switching frequency at the minimum output voltage is obtained as:

$$f_{S@C} = f_S - \frac{\Delta f_S}{\Delta V_{SH}}(2.15 - V_{SH@A}\cdot\frac{V_{O@C}+V_{F.SH}}{V_O^N+V_{F.SH}}) \quad (26)$$

where $\Delta f_S / \Delta V_{SH}$ is 64 kHz / V for UL version and 38 kHz / V for HL version, and $V_{F.SH}$ is the rectifier diode forward voltage drop at the V_S sampling instant (85% of diode conduction time).

Then, the MOSFET conduction time at operating point C is given as:

$$t_{ON@C} = \frac{1}{V_{DL@C}^{\min}}\sqrt{\frac{2P_{IN.T@C}L_m}{f_{S@C}}} \quad (27)$$

The non-conduction time at operating point C is given as:

$$t_{OFF@C} = \frac{1}{f_{S@C}} - t_{ON@C}(1+\frac{N_S}{N_P}\cdot\frac{V_{DL@C}^{\min}}{V_{O@C}+V_F}) \quad (28)$$

The non-conduction time should be larger than 15% of switching period, considering the transformer variation and frequency hopping.

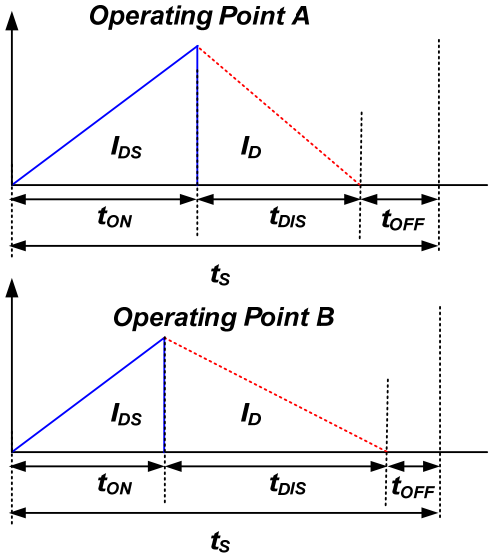


Figure 12. Variation of t_{ON}, t_D, and t_{OFF}

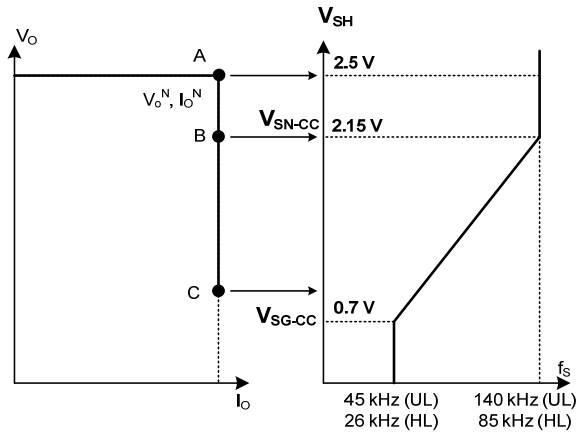


Figure 13. Frequency Reduction in CC Mode

Once the transformer primary-side inductance is obtained, the maximum peak drain current can be calculated at the nominal output condition (operating point A) as:

$$I_{DS}^{PK} = \sqrt{\frac{2P_{IN.T@A}}{L_m\cdot f_S}} \quad (29)$$

The minimum number of turns for the transformer primary side to avoid the core saturation is given by:

$$N_P^{\min} = \frac{L_m I_{DS}^{PK}}{B_{sat}A_e} \quad (30)$$

where AE is the cross-sectional area of the core in m^2 and B_{sat} is the saturation flux density in Tesla. Figure 14 shows the typical characteristics of a ferrite core from TDK (PC40). Since the saturation flux density (B_{sat}) decreases as the temperature rises, the high temperature characteristics should be considered, especially for charger application in an enclosed case. If there is no reference data, use B_{sat}=0.25~0.3T. With the turns ratio obtained in STEP-3, determine the proper integer for N_S such that the resulting N_P is larger than N_P^{min} obtained from Equation (30).

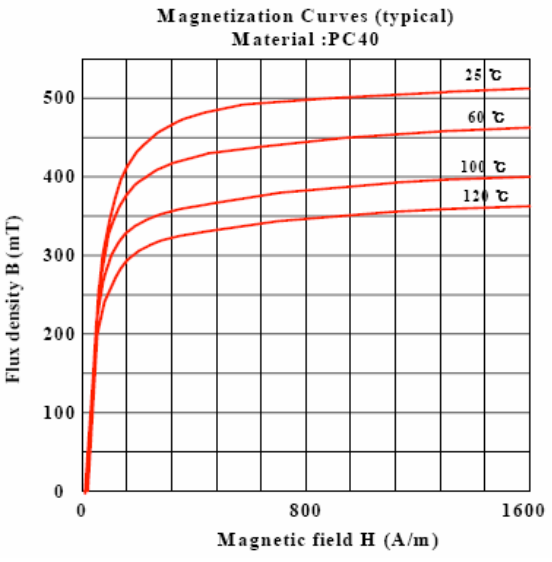


Figure 14. Typical B-H Curves of Ferrite Core (TDK/PC40)

(Design Example) By setting the non conduction time at operating point B as 1.6 μs, the MOSFET conduction time is obtained as:

$$t_{ON@B} = \frac{1/f_S - t_{OFF@B}}{(1+\frac{N_S}{N_P}\cdot\frac{V_{DL@B}^{\min}}{V_{O@B}+V_F})} = 2.15\mu s$$

The transformer primary-side inductance is calculated as:

$$L_m = \frac{(V_{DL@B}^{\min}\cdot t_{ON@B})^2}{2P_{IN.T@B}}\cdot f_S = 527\mu H$$

Assuming $V_{SH@A}$ is 2.5 V, the switching frequency at the minimum output voltage is obtained as:

$$f_{S@C} = f_S - \frac{\Delta f_S}{\Delta V_{SH}}(2.15-2.5\cdot\frac{V_{O@C}+V_{F.SH}}{V_O^{\,N}+V_{F.SH}}) = 45kHz$$

The MOSFET conduction time at minimum output voltage is obtained as:

$$t_{ON@C} = \frac{1}{V_{DL@C}^{\min}}\sqrt{\frac{2P_{IN.T@C}L_m}{f_{S@C}}} = 1.84\mu s$$

The non-conduction time at minimum output voltage:

$$t_{OFF@C} = \frac{1}{f_{S@C}} - t_{ON@C}(1+\frac{N_S}{N_P}\cdot\frac{V_{DL@C}^{\min}}{V_{O@C}+V_F}) = 10.33\mu s$$

The peak drain current at maximum load condition is given as:

$$I_{DS}^{PK} = \sqrt{\frac{2P_{IN.T@A}}{L_m\cdot f_S}} = 423mA$$

EE12.5 core is selected for the transformer. The minimum number of turns for the transformer primary side to avoid the core saturation is given by:

$$N_P^{\min} = \frac{L_m I_{DS}^{PK}}{B_{sat}A_e} = \frac{527\times10^{-6}\cdot0.423}{0.3\cdot12.88\times10^{-6}} = 63.5$$

Determine the proper integer for N_S such that the resulting N_p is larger than N_p^{min}; given as:

$$N_P = 13.27\times N_S = 13.27\times5 = 66 > N_P^{\min}$$

The auxiliary winding turns, N_A, is obtained as:

$$N_A = \frac{N_A}{N_S}\times N_S = 1.6\times5 = 8$$

[STEP-5] Set the Output Current and V_S Sensing Resistor

The nominal output current is determined by the sensing resistor value and transformer turns ratio as:

$$R_{CS} = \frac{N_P\times V_{CCR}}{2N_S I_O^{\,N}\times K} \quad (31)$$

where V_{CCR} is 2.43 V and K=12 and 10.5 V for UL and HL, respectively.

The voltage divider R_{VS1} and R_{VS2} should be determined so that V_S is about 2.5 V at 85% of diode current conduction time as:

$$\frac{R_{VS1}}{R_{VS2}} = \frac{N_A}{N_S}\frac{(V_O^{\,N}+V_{F.SH})}{V_{SH@A}} - 1 \quad (32)$$

The FAN302 indirectly senses input voltage using the VS pin current while the MOSFET is turned on, as illustrated in Figure 15. Since the VS pin voltage is clamped at 0.7 V when the MOSFET is turned on, the current flowing out of the VS pin is approximately proportional to the input voltage, calculated as:

$$I_{VS.ON} = (\frac{N_A}{N_P}V_{DL}+0.7)\frac{1}{R_{VS1}} + \frac{0.7}{R_{VS2}} \cong \frac{N_A}{N_P}\frac{V_{DL}}{R_{VS1}} \quad (33)$$

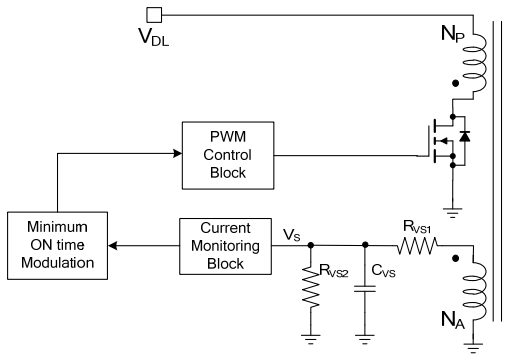


Figure 15. VS Pin Current Sensing

FAN302 modulates the minimum on-time of the MOSFET such that it reduces as input voltage increases, as shown Figure 16. This allows smaller minimum on time for high-line condition, ensuring Burst Mode operation occurs at almost the same power level regardless of line voltage variation. The V_S current needs to be higher than 150 μA.

Increasing the minimum on-time by increasing R_{VS1} and R_{VS2} allows FAN302 to enter Burst Mode at a higher power level. This reduces the standby power consumption by increasing power delivered to the output per switching. However, this also increases the output voltage ripple by increasing the time interval between switching bundles in Burst Mode. Thus, the minimum on-time should be determined by a trade-off between standby power consumption and output voltage ripple. When selecting R_{VS1} and R_{VS2}, 150 μA is the VS current level to consider seriously. If the VS current is lower than 150 μA, t_{on_min} won't be larger.

The recommendation for R_{VS1} design is to set R_{VS1} such that the minimum on time curve of Figure 16 can be fully utilized for the universal line range. It is typical to select R_{VS1} such that $I_{VS.ON}$ is around 180 μA for the minimum line voltage.

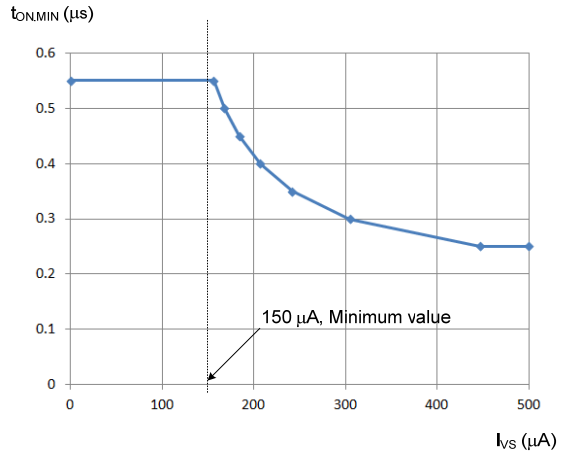


Figure 16. Minimum On-Time vs. VS Pin Current (UL)

A bypass capacitor of 22~68 pF placed closely between the VS and GND pins is recommended to bypass the switching noise. Too large a capacitor distorts V_S voltage and deteriorates the output current regulation. The RC time constant of the bypass capacitor and voltage divider resistor should be <10% of switching period, given as:

$$\tau_{RC} = (R_{VS1} // R_{VS2}) \cdot C_{VS} < \frac{1}{10 f_S} \quad (34)$$

(Design Example) The sensing resistor is obtained as:

$$R_{CS} = \frac{N_P \times V_{CCR}}{2 N_S I_O{}^N \times K} = \frac{66 \times 2.43}{2 \times 5 \times 1.2 \times 12} = 1.1\Omega$$

Note that the sensing resistor is fine-tuned to 1.2 Ω in the final schematic based on the test results of actual prototype power supply.

The voltage divider network is determined as:

$$\frac{R_{VS1}}{R_{VS2}} = (\frac{N_A}{N_S} \cdot \frac{V_O + V_{F.SH}}{2.5} - 1) = (\frac{8}{5} \cdot \frac{5 + 0.1}{2.5} - 1) = 2.26$$

To set $I_{VS.ON}$ around 180 μA for the minimum DC link, calculate the R_{VS1} as:

$$I_{VS.ON} = (\frac{N_A}{N_P} V_{DL} + 0.7) \frac{1}{R_{VS1}} + \frac{0.7}{R_{VS2}} = 180\mu A$$

$$R_{VS1} = \frac{(\frac{N_A}{N_P} \sqrt{2} \cdot 90 + 0.7) + 0.7 \times 2.26}{180\mu A} = 98k\Omega$$

By setting R_{VS1}=91 kΩ, R_{VS2} is obtained as 40 kΩ.

The bypass capacitor should be:

$$C_{VS} < \frac{1}{10 f_S (R_{VS1} // R_{VS2})} = 26\,pF$$

Thus, a 22 pF capacitor is selected for C_{VS}.

[STEP-6] Design the RCD Clamping Circuit in the Primary Side

When the MOSFET in the flyback converter is turned off, a high-voltage spike is generated across the MOSFET due to the transformer leakage inductance. This excessive voltage can lead to an avalanche breakdown and, eventually, failure of the MOSFET. Therefore, an RCD clamping circuit must limit the voltage, as shown in Figure 17. The voltage overshoot (V_{OS}) is related to the power dissipation in the clamping circuit. Setting the voltage overshoot too low can lead to severe power dissipation in the clamping circuit. For reasonable clamping circuit design, voltage overshoot (V_{OS}) is typically 1~2 times the reflected output voltage.

It is typical to have a margin of 10~20% of the breakdown voltage for maximum MOSFET voltage stress. The maximum voltage stress of the MOSFET is given as:

$$V_{DS}{}^{max} = V_{DL}{}^{max} + V_{RO} + V_{OS} \quad (35)$$

When the drain voltage of the MOSFET reaches the voltage of node X (sum of DC link voltage and clamping capacitor voltage), the clamping diode is turned on to limit the drain voltage. It is assumed that the clamping capacitor is large enough that its voltage does not change significantly during one switching cycle.

For medium-power and high-power applications where the leakage inductance energy is much larger than the energy stored in the effective output capacitance of the MOSFET, the output capacitance of the MOSFET is generally ignored when designing the clamping circuit. However, for low-power applications where the leakage inductance energy is almost the same as, or smaller than, the energy stored in the effective output capacitance of the MOSFET, the output capacitance of the MOSFET should be considered for clamping circuit design. Especially for low-power applications of less than 10 W, the transformer typically has a large number of turns, resulting in large inter-winding capacitance. This significantly contributes to the effective output capacitance of the MOSFETs, affecting the operation of the clamping circuit.

Considering the loading effect of the output capacitance of the MOSFET, the peak current of clamping circuit is given as:

$$I_{CL}{}^{PK} = \sqrt{(I_{DS}{}^{PK})^2 - \frac{C_{OSS}}{L_{LK}} V_{OS}{}^2} \quad (36)$$

where V_{OS} is the voltage overshoot of the drain voltage, as illustrated in Figure 17.

The power dissipated in the RCD network is given as:

$$P_{CLMP} = \frac{1}{2} f_S L_{LK} (I_{CL}{}^{PK})^2 \frac{V_{RO} + V_{OS}}{V_{OS}} \quad (37)$$

where $I_{CL}{}^{PK}$ is the peak clamping diode current at full load; L_{LK} is the leakage inductance.

Once the power dissipation in the snubber is obtained, the snubber resistor is calculated as:

$$R_{CL} = \frac{(V_{RO} + V_{OS})^2}{P_{CLMP}} \quad (38)$$

where R_{CL} is the clamping resistor.

The maximum ripple of the clamping capacitor voltage is obtained as:

$$\Delta V_{CL} = \frac{V_{RO} + V_{OS}}{C_{CL} R_{CL} f_s} \quad (39)$$

In general, 5~10% ripple of the selected capacitor voltage is reasonable. The clamping capacitor should be ceramic or a material that offers low ESR. Electrolytic or tantalum capacitors are unacceptable.

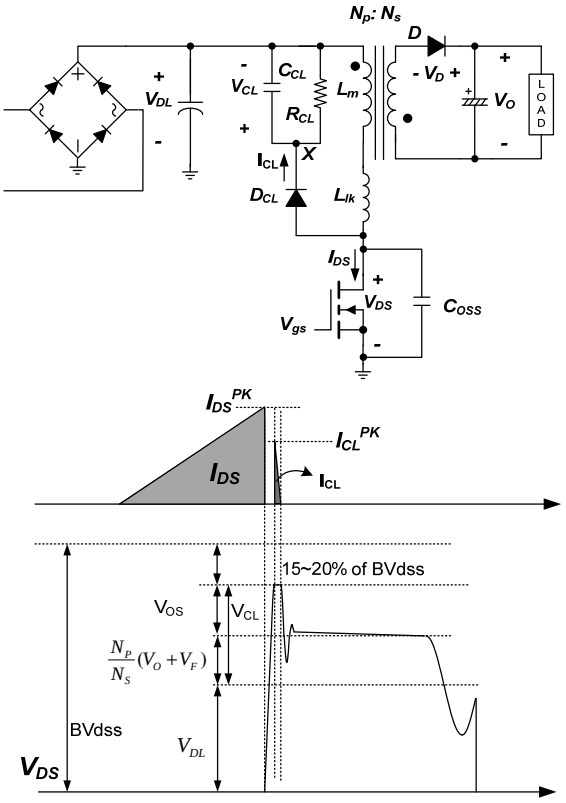


Figure 17. RCD Clamping Circuit and Waveforms

The leakage inductance measured with an LCR meter tends to be larger than the actual effective leakage inductance. Moreover, the effective output capacitance of the MOSFET is difficult to measure. The best way to obtain these parameters correctly is to use the drain voltage waveform as illustrated in Figure 18. Since L_m can be measured with an LCR meter, C_{OSS} and L_{LK} can be calculated from the measured resonant period.

In the clamping design in this section, the lossy discharge of the inductor and stray capacitance is not considered. In the actual converter, the loss in the clamping network is less than the designed value due to this effect.

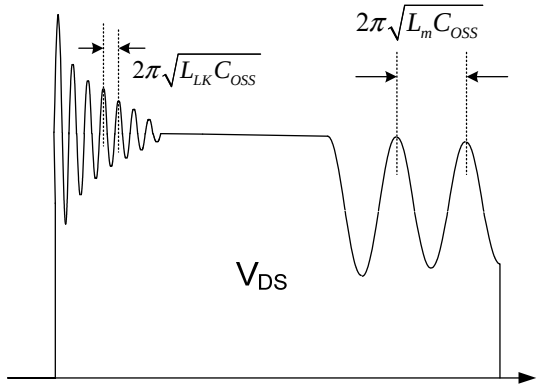


Figure 18. Drain Voltage Waveform

(Design Example) Assuming that 700 V MOSFET is used, the voltage overshoot to limit the maximum drain voltage below 600 V is:

$$V_{OS} < 600V - V_{DL}^{\max} - V_{RO} = 156$$

The leakage inductance and the effective output capacitance of MOSFET are calculated from the resonance waveform as 18 μH and 55 pF, respectively.

The peak current of clamping diode is obtained as:

$$I_{CL}^{PK} = \sqrt{(I_{DS}^{PK})^2 - \frac{C_{OSS}}{L_{LK}} V_{OS}^2} = 325mA$$

The power dissipation in the clamping circuit is obtained as:

$$P_{CLMP} = \frac{1}{2} f_S L_{LK} (I_{CL}^{PK})^2 \frac{V_{RO} + V_{OS}}{V_{OS}} = 0.194W$$

Then the clamping circuit resistor is calculated as:

$$R_{CL} = \frac{(V_{RO} + V_{OS})^2}{P_{CLMP}} = 263k\Omega$$

The actual drain voltage can be lower than the design due to the loss of stray resistance of inductor and capacitor. The resistor value can be adjusted after the power supply is actually built.

To allow less than 15 V ripple on the clamping capacitor voltage, the clamping capacitor should be:

$$C_{CL} > \frac{V_{RO} + V_{OS}}{C_{CL} \Delta V_{CL} f_s} = 410\,pF$$

A 470 pF capacitor is selected.

[STEP-7] Calculate the Voltage and Current of the Switching Devices

Primary-Side MOSFET: The voltage stress of the MOSFET was discussed when determining the transformer turns ratio in STEP-6. The maximum voltage stress of the MOSFET is given in Equations (35).

The rms current through the MOSFET is given as:

$$I_{DS}^{rms} = I_{DS}^{PK} \sqrt{\frac{t_{ON@A} f_s}{3}} \quad (40)$$

where t_{ON} is MOSFET conduction time minimum input voltage and maximum load condition, given as:

$$t_{ON} = \frac{1}{V_{DL}^{\min}} \sqrt{\frac{2P_{IN.T@A}L_m}{f_S}} \quad (41)$$

Secondary-Side Diode: The nominal reverse voltage of the diode is given in Equation (21).

The rms current of the rectifier diode is obtained as:

$$I_D^{rms} = I_{DS}^{PK} \cdot \frac{N_P}{N_S} \sqrt{\frac{t_{DIS@A} \cdot f_S}{3}} \quad (42)$$

(Design Example) The maximum voltage across the MOSFET is calculated as:

$$V_{ds}^{\max} = V_{DL}^{\max} + V_{RO} + V_{OS} = 373 + 71 + 155 = 599V$$

The rms current though the MOSFET is:

$$I_{DS}^{rms} = I_{DS}^{PK} \sqrt{\frac{t_{ON} f_s}{3}} = 0.14A$$

The diode voltage and current are obtained as:

$$V_D = V_O + \frac{N_S}{N_P} V_{DL}^{\max} = 5 + \frac{5}{66} \cdot 373 = 33.1V$$

$$I_D^{rms} = I_{DS}^{PK} \cdot \frac{N_P}{N_S} \sqrt{\frac{t_{DIS@A} \cdot f_S}{3}} = 2.14A$$

[STEP-8] Determine the Output Filter Stage

The peak-to-peak ripple of capacitor current is given as:

$$\Delta I_C = \frac{N_P}{N_S} I_{DS}^{PK} \quad (43)$$

The voltage ripple on the output is given by:

$$\Delta V_O = \frac{t_{DIS@A}}{2C_O} \cdot \frac{(\Delta I_C - I_O^N)^2}{\Delta I_C} + \Delta I_C \cdot R_C \quad (44)$$

Sometimes it is impossible to meet the ripple specification with a single-output capacitor due to the high ESR of the electrolytic or tantalum capacitors. Additional LC filter stages (post filter) can be used. When using post filters, do not place the corner frequency too low. Too low corner frequency may make the system unstable or limit the control bandwidth. It is typical to set the corner frequency of the post filter at around 1/10~1/5 of the switching frequency.

(Design Example) Assuming a 330 µF tantalum capacitor with 100 mΩ ESR for the output capacitor, the voltage ripple on the output is:

$$\Delta I_C = \frac{N_P}{N_S} I_{DS}^{PK} = 5.59A$$

$$\Delta V_O = \frac{t_{DIS@A}}{2C_O} \cdot \frac{(\Delta I_C - I_O^N)^2}{\Delta I_C} + \Delta I_C \cdot R_C = 0.592V$$

Since the output voltage ripple exceeds the specification of 100 mV, a post LC filter should be used. Two 330 µF capacitors and one 1.8 µH inductor are selected for the post LC filter. Then, the cutoff frequency of the LC filter is 9.2 kHz.

[STEP-9] Complete the RC Snubber Design for the Diode

When the primary-side MOSFET is turned on, severe voltage oscillation occurs across the secondary-side diode, as shown in Figure 19. This is caused by the oscillation between the diode parasitic capacitance (C_D) and transformer secondary-side leakage inductance (L_{LKS}). To reduce the oscillation, an RC snubber is typically used, as shown in Figure 19. To effectively introduce damping to the resonant circuit, the parameters of the RC snubber should be:

$$R_{SNB} = \sqrt{\frac{L_{LKS}}{C_D}} \quad (45)$$

$$C_{SNB} = 2 \sim 3 \; times \; of \; C_D \quad (46)$$

The secondary-side leakage inductance and the diode parasitic capacitance are difficult to measure with an LCR meter. The best way is to use a test capacitor across the diode. First, measure the natural resonance period (t_R) without connecting anything to the diode. Then, add a test capacitor across the diode (C_{TST}) such that the test resonance period (t_{RT}) becomes about twice its original value and measure the test resonance period. With the measured t_R, t_{RT}, and C_{TST}; the resonance parameters can be calculated as:

$$C_D = C_{TST} / [(\frac{t_{RT}}{t_R})^2 - 1] \quad (47)$$

$$L_{LKS} = (\frac{t_R}{2\pi})^2 \frac{1}{C_D} \quad (48)$$

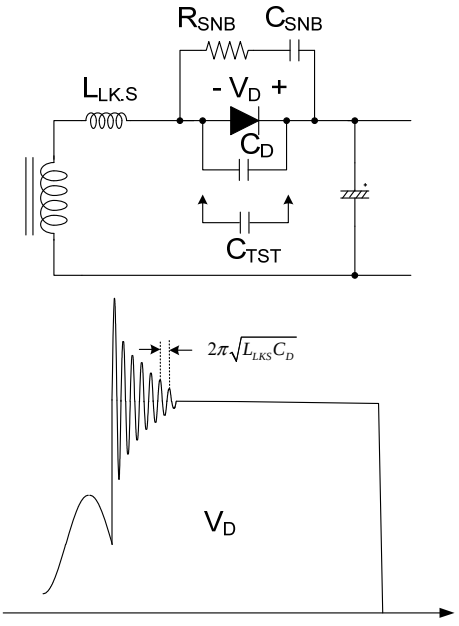


Figure 19. Diode Voltage Waveform

(Design Example) The original resonance period is measured as t_R=25 ns.

Using a 1 nF test capacitor, the resonance period is measure as t_{RT}=25 ns.

Then, the resonant parameters are obtained as:

$$C_D = C_{TST} / [(\frac{t_{RT}}{t_R})^2 - 1] = 395\,pF$$

$$L_{LKS} = (\frac{t_R}{2\pi})^2 \frac{1}{C_D} = 40nH$$

The snubber circuit parameters are calculated as:

$$R_{SNB} = \sqrt{\frac{L_{LKS}}{C_D}} = 10\Omega \quad , \quad C_{SNB} = 2.5C_D = 1nF$$

[STEP-10] Design the Feedback Loop

Since the FAN302 operates a flyback converter in DCM with a peak-current mode control, the control to output transfer function of the power stage is given as:

$$\frac{\hat{v}_o}{\hat{v}_{FB}} = G_V \cdot \frac{1 + s/\omega_Z}{1 + s/\omega_P} \tag{49}$$

where $\omega_p = \frac{2}{R_L C_{OUT}}$; $\omega_Z = \frac{1}{R_{ES} C_{OUT}}$; C_{OUT} is effective output capacitance; and R_{ES} is the effective series resistance of the output capacitor.

The gain G_V of Equation (49) is defined as:

$$G_V = \frac{1}{3} \cdot \frac{m}{m + m_a} \cdot \frac{{V_O}^N}{R_{CS} I_{DS}} \tag{50}$$

where 1/3 is the attenuation factor of feedback voltage; I_{DS} is the peak drain current at given operating condition; m_a is the slope of slope compensation signal; and m is the slope of current sensing signal, given as:

$$m = \frac{V_{DL} \cdot R_{CS}}{L_m} \tag{51}$$

Note that the effect of slope compensation is weaker at high line, which increases the gain of control-to-output transfer function. Thus, the high line is the worst case for feedback loop design.

Since the control to output transfer function is first order, the feedback control loop can be implemented with a one-pole and one-zero compensation circuit, as shown in Figure 20. The transfer function of the compensation network is given as:

$$\frac{\hat{v}_{EA}}{\hat{v}_o} = \frac{\omega_I}{s} \cdot \frac{(s/\omega_{CZ1} + 1)}{(s/\omega_{CP1} + 1)} \tag{52}$$

where $\omega_I = \frac{R_{FB}}{R_{F1} R_{bias} C_{FR}}$; $\omega_{CZ1} = \frac{1}{(R_{FR} + R_{F1}) C_{FR}}$;

and $\omega_{CP1} = \frac{1}{R_{FB} C_{FB}}$.

Note that the opto-coupler introduces a mid-frequency pole due to the collector-emitter junction capacitance. Since the collector-base junction in a photo-transistor is used as a light detector; its area is relatively large, which introduces a large effective collector-emitter junction capacitance. The typical collector-emitter junction capacitance is about 3-10 nF for the opto-coupler FOD817A, which brings a pole at around 1 kHz with a bias resistor of 42 kΩ, as shown in Figure 20. This pole can occur around the desired crossover frequency, making the system unstable. Therefore, this additional pole should be considered when designing the compensation network.

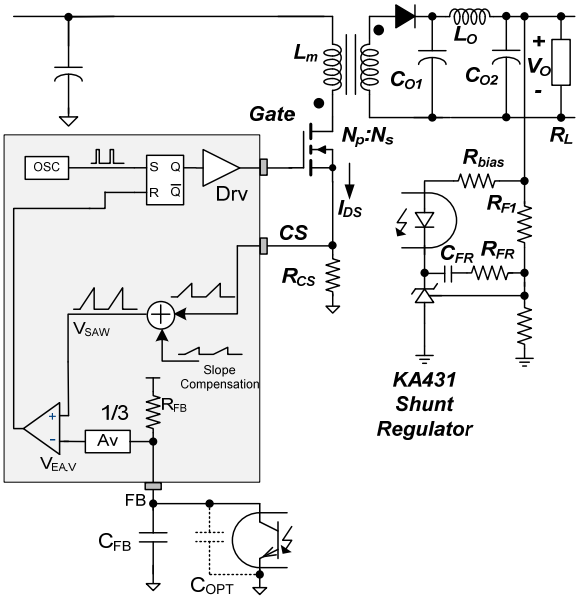


Figure 20. Feedback Loop Circuit

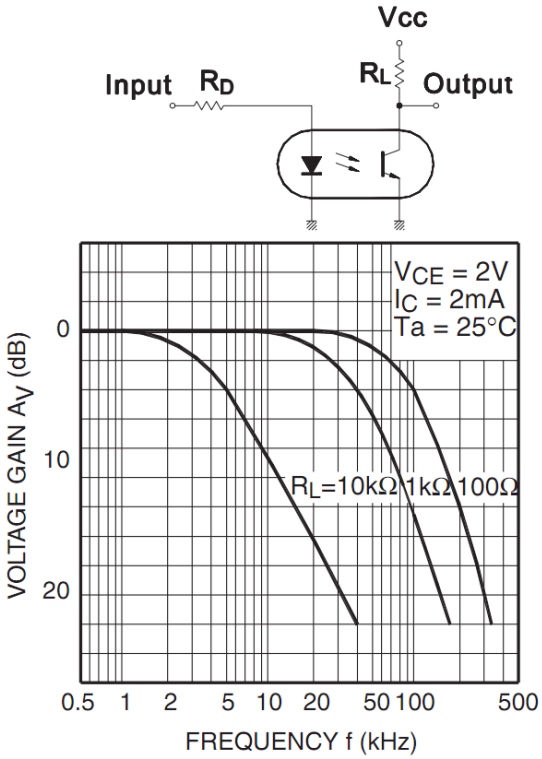


Figure 21. Frequency Response of Opto-Coupler

(Design Example) In STEP-8, the post LC filter is designed with two 330 µF capacitors and a 1.8 µH inductor. Since the resonance frequency of the post LC filter is 9.2 kHz, the bandwidth of the feedback loop should be less than 1/3 of the cut-off frequency to minimize the phase drop caused by the post LC filter. Thus, the target bandwidth of the feedback loop is determined as around 3 kHz.

To simplify analysis, the inductor of the post filter is ignored, since the bandwidth is below the cutoff frequency of post LC filter. The effective output capacitance and its effective series resistance are given as:

$$C_{OUT} = 330\mu F \times 2 = 660\,\mu F$$

$$R_{ES} = 100m\Omega / 2 = 50m\Omega$$

The slope of current sensing signal for high line is obtained as:

$$m = \frac{V_{DL} \cdot R_{CS}}{L_m} = \frac{373V \cdot 1.2}{530\mu H} = 0.845V / \mu s$$

The slope of internal slope compensation is obtained as:

$$m_a = \frac{0.3V}{1/f_S \times D_{\max}} = \frac{0.3V}{7.14\mu s \times 0.64} = 0.066V / \mu s$$

Then, the gain G_V for high line and maximum load condition is obtained as:

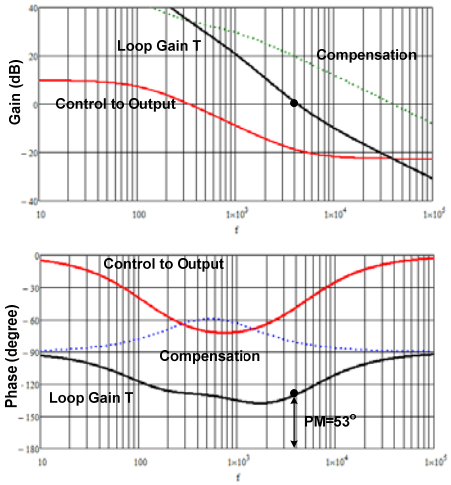
$$G_V = \frac{1}{3} \cdot \frac{m}{m + m_a} \cdot \frac{{V_O}^N}{R_{CS} {I_{DS}}^{PK}} = 3$$

The system pole and zero are obtained as:

$$\omega_p = \frac{2}{R_L C_{OUT}} = 727\,rad/s$$

$$\omega_Z = \frac{1}{R_{ES} C_{OUT}} = 30,300\,rad/s$$

With R_F=0 Ω, C_{FR}=10 nF, R_{bias}=1 kΩ, R_{F1}=50 kΩ, C_{FB}=4nF (including output capacitance of opto-transistor), and R_{FB}=42 kΩ; 3 kHz bandwidth with 53° phase margin is obtained. For C_{FB}, output capacitance of an opto-transistor is assumed to be 3 nF and a 1 nF external capacitor is used.



[STEP-11] Choose Startup Resistor for HV Pin

Figure 22 shows the high-voltage (HV) startup circuit for FAN302 applications. Internally, the JFET is used to implement the high-voltage current source, whose characteristics are shown in Figure 23. Technically, the HV pin can be directly connected to the DC link (V_{DL}). However, to improve reliability and surge immunity, it is typical to use a ~100 kΩ resistor between the HV pin and the DC link. The actual HV current with a given DC link voltage and startup resistor is determined by the intersection point of V-I characteristics line and load line, as shown in Figure 23.

During startup, the internal startup circuit is enabled and the DC link supplies the current, I_{HV}, to charge the hold-up capacitor, C_{DD}, through R_{HV}. When the V_{DD} voltage reaches V_{DD-ON}, the internal HV startup circuit is disabled and the IC starts PWM switching. Once the HV startup circuit is disabled, the energy stored in C_{DD} should supply the IC operating current until the transformer auxiliary winding voltage reaches the nominal value. Therefore, C_{DD} should be properly designed to prevent V_{DD} from dropping to V_{DD-OFF} before the auxiliary winding builds up enough voltage to supply V_{DD}.

The startup time with a given C_{DD} capacitor is given as:

$$t_{start} = \frac{C_{DD} V_{DD.ON}}{(I_{HV} - I_{DD-ST})} \quad (53)$$

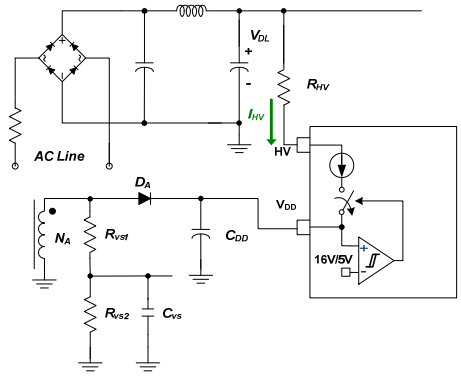


Figure 22. HV Startup Circuit

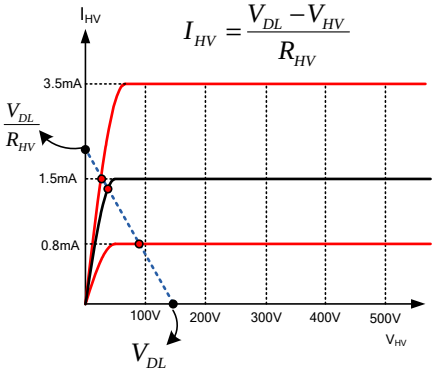


Figure 23. V-I Characteristics of HV Pin

(Design Example) With 100 kΩ HV resistor and 33 µF V_{DD} capacitor, the maximum startup time is:

$$t_{start} = \frac{C_{DD} V_{DD.ON}}{(I_{HV} - I_{DD-ST})} = \frac{33\mu \cdot 16V}{0.8mA - 0.4mA} = 1.32\,s$$

[STEP-12] Protection Setting

Output OVP:

In STEP-5, the voltage divider for VS is determined such that VS sampling voltage is about 2.5 V in normal operation. The voltage divider also determines the output over-voltage protection (OVP) level. The OVP is triggered when VS sampling voltage is above 2.8 V. The OVP trip point is given as:

$$V_O^{OVP} = 2.8\frac{N_S}{N_A}\frac{R_{VS1}+R_{VS2}}{R_{VS2}} - V_{F.SH} \quad (54)$$

Pulse-by-Pulse Current Limit:

Since FAN302 employs current-mode control, the MOSFET drain current is regulated properly by the error amplifier output in normal operation. During the load transient or abnormal condition such as output short, the error amplifier can be saturated HIGH and the drain current is regulated by the pulse-by-pulse current limit, which forces the MOSFET gate to be turned off when the current-sensing voltage reaches 0.7 V. The flux density of the transformer during the pulse-by-pulse current-limit mode should be checked to make sure that the flux density is below 0.4~0.42T to prevent severe core saturation.

$$B_{MAX}^{OCP} = \frac{L_m V_{STH}/R_{CS}}{N_P A_e} \quad (55)$$

(Design Example) With 91 kΩ and 40 kΩ for R_{VS1} and R_{VS2} from STEP-5, the OVP trip point is obtained as:

$$V_O^{OVP} = 2.8\frac{N_S}{N_A}\frac{R_{VS1}+R_{VS2}}{R_{VS2}} - V_{F.SH} = 5.63V$$

The flux density during pulse-by-pulse current limit is given as:

$$B_{MAX}^{OCP} = \frac{L_m V_{STH}/R_{CS}}{N_P A_e} = 0.36T$$

5. PCB Layout Guidelines

Printed Circuit Board (PCB) layout and design are very important for switching power supplies where the voltage and current change with high dv/dt and di/dt. Good PCB layout minimizes excessive EMI and prevents the power supply from being disrupted during surge / ESD tests. The following guidelines are recommended for layout designs.

- To improve EMI performance and reduce line frequency ripple, the output of the bridge rectifier should be connected to capacitors C_{DL2} and C_{DL1} first, then to the transformer and MOSFET.
- The primary-side high-frequency current loop is **C_{DL2} – Transformer – MOSFET – R_{CS} – C_{DL2}**. The area enclosed by this current loop should be as small as possible. The trace for the control signal (FB, CS, and GATE) should not go across this primary high-frequency current loop to avoid interference.
- Place R_{HV} for protection from the inrush spike on the HV pin (100 kΩ is recommended).
- **R_{CS}** should be connected to the ground of C_{DL2} directly. Keep the trace short and wide (Trace 4→1) and place it close to the CS pin to reduce switching noise. High-voltage traces related to the drain of the MOSFET and the RCD snubber should be away from control circuits to prevent unnecessary interference. If a heat sink is used for the MOSFET, connect this heat sink to ground.
- As indicated by 2, the area enclosed by the **transformer auxiliary winding, D_{DD} and C_{DD}**, should be small.
- Place **C_{DD}**, **C_S**, **R_{S2}**, **C_{FB}**, and **R_{BF}** close to the controller for good decoupling and low switching noise.
- As indicated by 3, the ground of the control circuits should be connected at a single point first, then to other circuitry.
- Connect ground in 3→2→4→1 sequence. This helps avoid common impedance interference for the sense signal.
- Regarding the ESD discharge path, use the shortcut pad between the AC line and the DC output (recommended). Another method is to discharge the ESD energy to the AC line through the primary-side main ground 1. Because ESD energy is delivered from the secondary side to the primary side through the transformer stray capacitor or the Y capacitor, the controller circuit should not be placed on the discharge path. 5 shows where the point-discharge route can be placed to effectively bypass the static electricity energy.
- For the surge path, select a fusible resistor of wire-wound type to reduce inrush current and surge energy. Use π input filter (two bulk capacitor and one inductance) to share the surge energy.

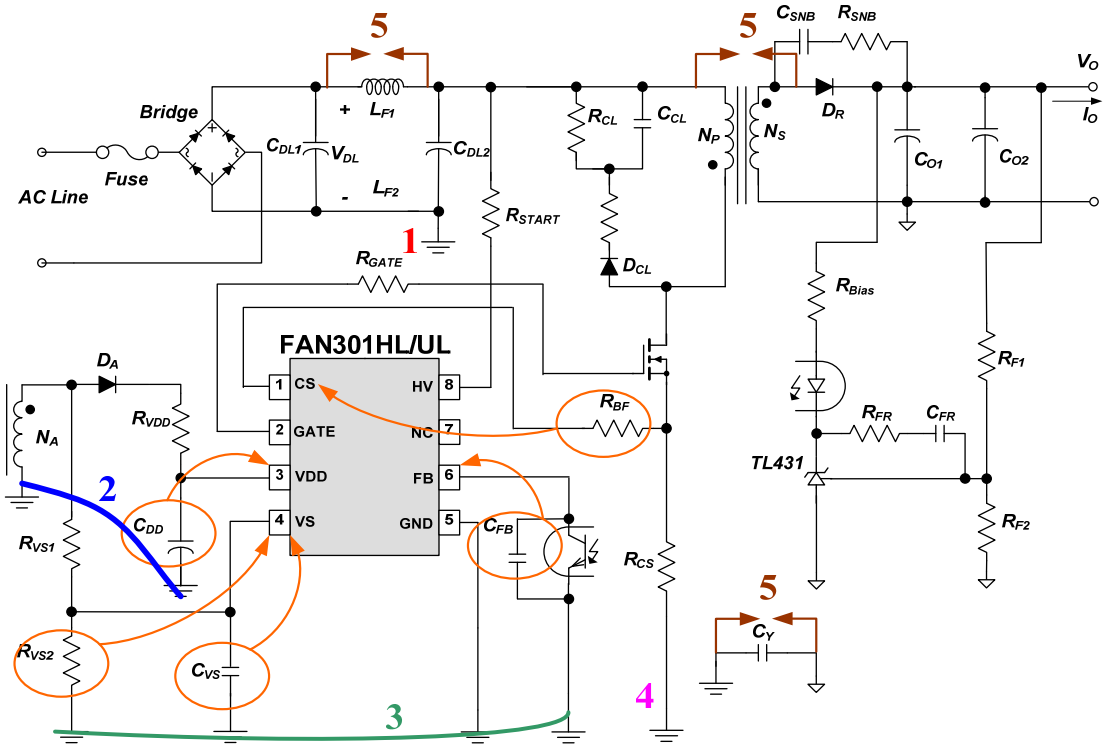


Figure 24. Recommended Layout

6. Final Schematic of Design Example

Figure 25 shows the final schematic of the 6 W charger design example. EI12.5 core is used for the transformer. Figure 26 shows the transformer winding structure. Figure 27 and Figure 28 show the PCB pattern.

Design Notes

- The leakage inductance is measured as 52 µH with an LCR meter. Calculation with the measured resonance period yields 18 µH of effective leakage inductance
- Clamping circuit resistor R10 is adjusted to 390 kΩ based on test results from the actual power supply.
- Note that the sensing resistor is fine tuned to 1.2 Ω based on test result of actual prototype power supply.

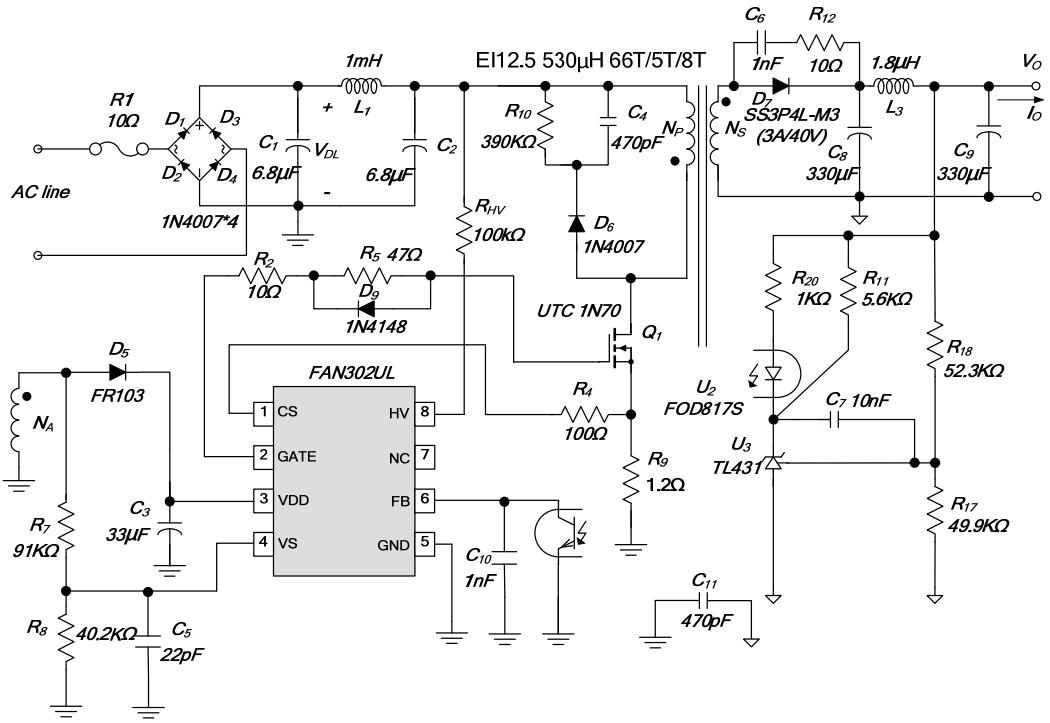


Figure 25. Final Schematic of the FAN302UL 6W Design Example

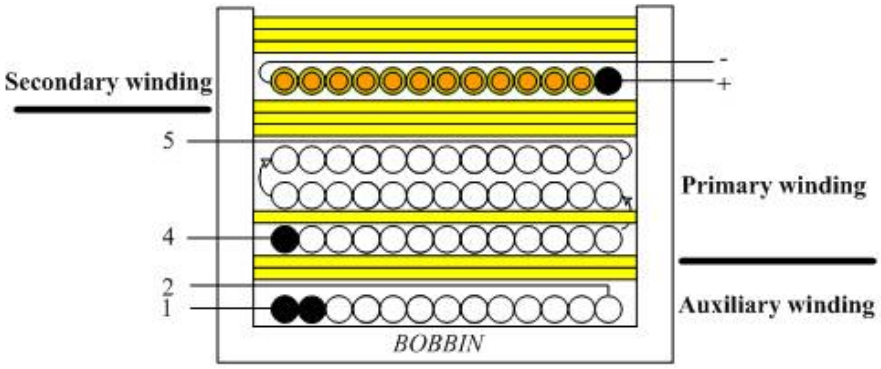


Figure 26. Transformer Winding Structure

- Core: EI12.5, Bobbin: EI12.5.
- W1 is space winding in one layer.
- W2 consists of three layers with a different number of turns. The number of turns for each layer is specified below.
- W3 consists of two layers with triple-insulated wire. The leads of positive and negative; fly lines are 3.5 cm and 2.5 cm, respectively.

NO	Terminal		Wire	Turns	Insulation
	Start Pin	End Pin			Turns
W1	1	2	2UEW 0.15*2	8	2
W2	4	5	2UEW 0.12*1	22	0
				22	1
				22	3
W3	Fly+	Fly-	TEX-E 0.4*1	5	3

	Pin	Specifications	Remark
Primary-Side Inductance	4 – 5	530 µH ±7%	100 kHz, 1 V
Primary-Side Effective Leakage Inductance	4 – 5	52 µH ±5%	Short one of the secondary windings

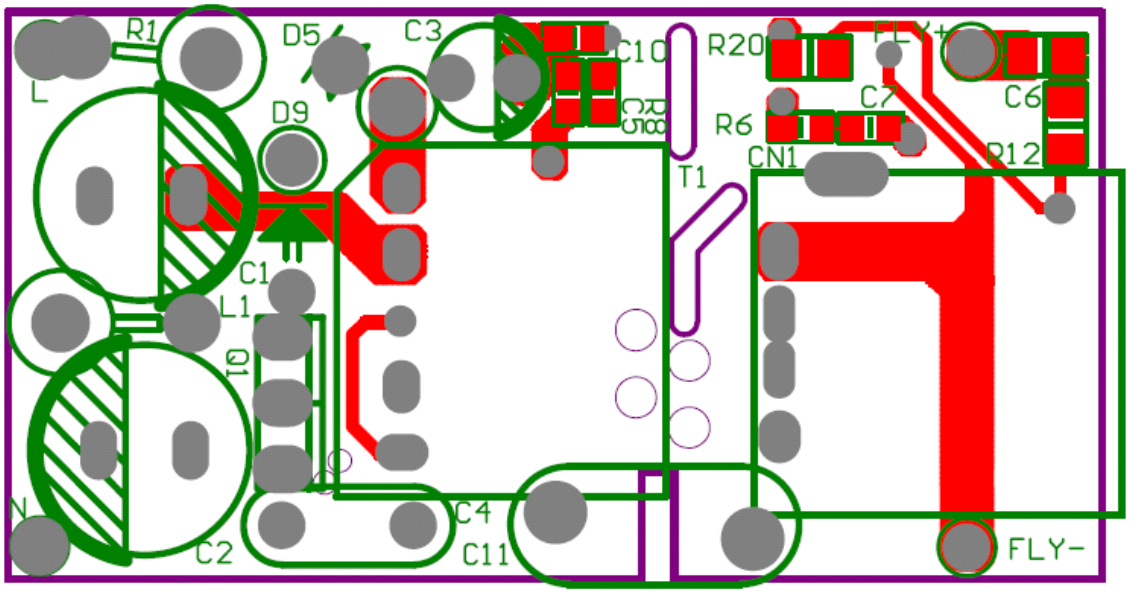


Figure 27. Front Side of PCB

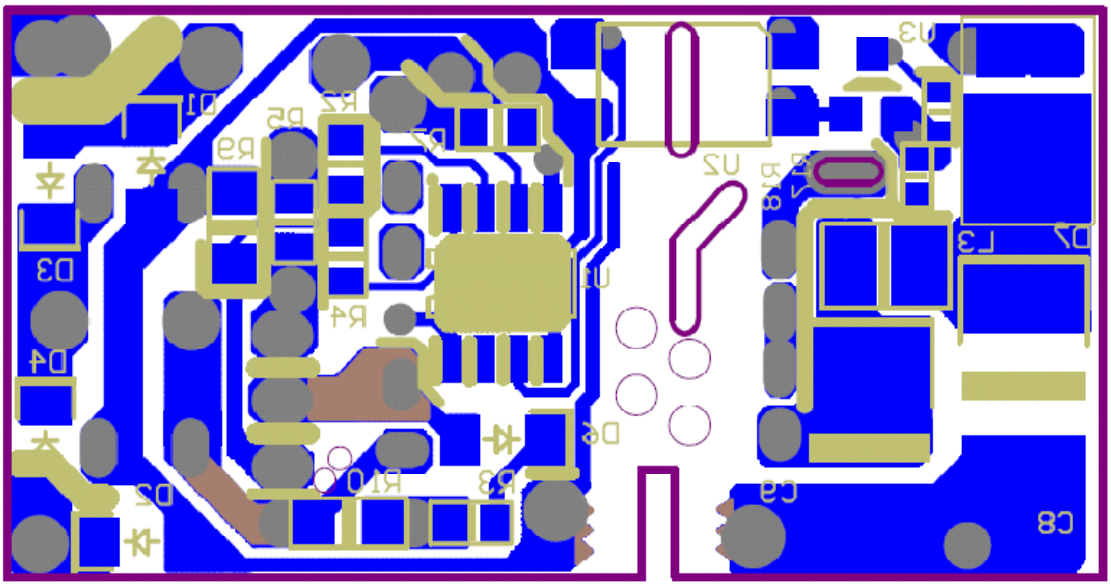


Figure 28. Back Side of PCB

7. Test Results of Design Example

To show the validity of the design procedure presented in this application note, the converter of the design example was built and tested. All the circuit components are used as designed in the design example.

Figure 29 shows the measured efficiency for different load conditions. The average efficiencies at 115 V_{AC} and 230 V_{AC} condition are 74.96% and 72.05%, respectively. Figure 30 shows the measured no-load power consumption at different line voltages. Even in the 264 V_{AC} AC line, the no-load standby power consumption is less than 10 mW, meeting the five-star level of new power consumption regulation for charger. Table 2 shows the loss breakdown for the standby power consumption for 90 V_{AC} and 264 V_{AC}.

Figure 31 shows the measured output voltage and output current curve. The output current is regulated between 1 A and 1.2 A for output voltage from 5 V down to 1 V.

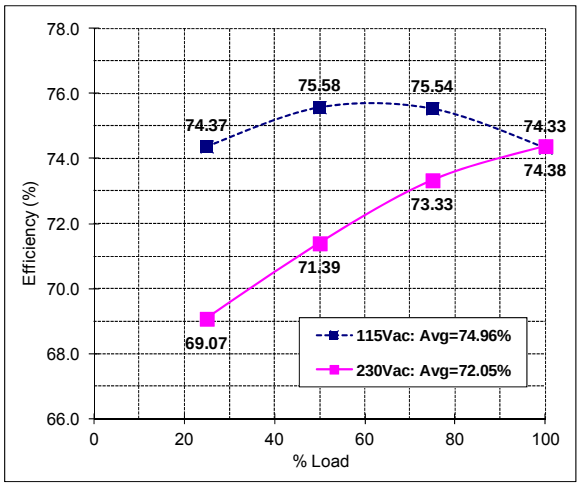


Figure 29. Measured Efficiency

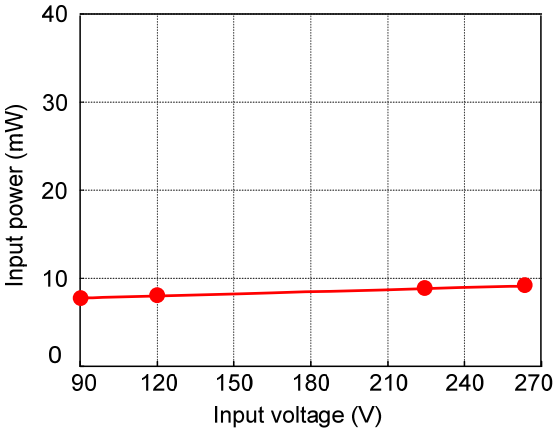


Figure 30. Standby Power Consumption

Table 2. Loss Breakdown for Standby Power Consumption

	90V_{AC}	264V_{AC}
RCD Clamping Circuit	2.19 mW	1.19 mW
MOSFET Loss	0.52 mW	1.61 mW
Output Voltage Divider Resistor (R_{VS1} and R_{VS2})	0.26 mW	0.26 mW
IC Consumption	1.52 mW	1.56 mW
Secondary-Side Feedback Circuit	3.61 mW	3.61 mW
Output Diode	1.8 mW	1.8 mW
Total (Estimated)	9.9 mW	10.3 mW
Total (Measured)	8.1 mW	9 mW

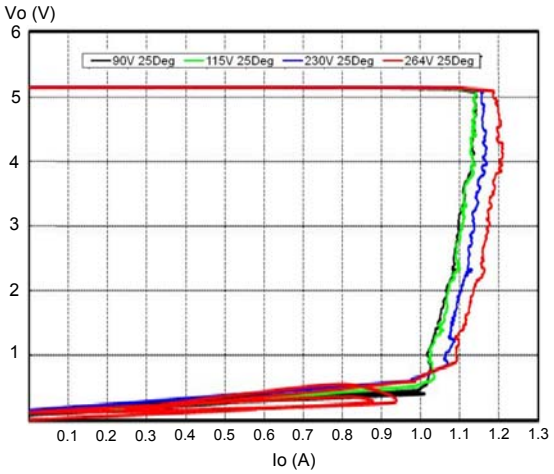


Figure 31. Output Voltage and Current Regulation

8. Related Resources

AN-4137 — Design guideline for Offline Flyback Converters Using Fairchild Power Switch (FPS™)

FAN302HL/UL — mWSaver™ PWM Controller for Lower Standby Power Battery-Charger Applications

FOD814 — Series, FOD817 Series 4-Pin High Operating Temperature Phototransistor Opto-Couplers

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