James Webb Space Telescope Mid Infra-Red Instrument Cryocooler Electronics

D. Harvey[1], T. Flowers[1], N. Liu[1], K. Moore[1], D. Tran[1], P. Valenzuela[1], B. Franklin[2], D. Michaels[2]

[1]Northrop Grumman Aerospace Systems, Redondo Beach, CA, USA
[2]Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA, USA

ABSTRACT

The latest generation of long life, space pulse-tube cryocoolers require electronics capable of controlling self-induced vibration down to a fraction of a newton and coldhead temperature with high accuracy down to a few Kelvin. Other functions include engineering diagnostics, heater and valve control, telemetry and safety protection of the cryocooler subsystem against extreme environments and operational anomalies. The electronics are designed to survive the thermal, vibration, shock and radiation environment of launch and orbit, while providing a design life in excess of 10 years on-orbit. A number of our current generation high reliability radiation-hardened electronics units are deployed on-orbit on space flight payloads. This paper describes the features and performance of our latest flight electronics designed for the Pulse Tube and Joule-Thomson cryocoolers that providing 6K cooling for the James Webb Space Telescope (JWST) Mid Infra-Red Instrument (MIRI). The electronics are capable of highly accurate temperature measurement and control over the temperature range from 4 K to 15 K. Self-induced vibration is controlled to low levels on all harmonics up to the 16th. A unique active power filter controls peak-to-peak reflected ripple current on the primary power bus to a very low level. This paper provides a design overview and ground-test data for the MIRI JouleThomson and Pulse Tube flight Cryocooler Control Electronics (CCE) units.

INTRODUCTION

Northrop Grumman has been producing space cryocoolers and cryocooler control electronics for over 20 years, beginning with the AIRS Pulse Tube cryocooler system. The requirements for the electronics includes low mass, high efficiency, radiation hardness, high reliability, high temperature control accuracy and stability, the ability to control and minimize the vibration exported from the compressor, provide cryocooler safety protection and extensive on-orbit diagnostics. All of these objectives were met with the original space cryocooler electronics; however advances in electronic technology, along with experience gained manufacturing, testing, integrating and operating several space cryocooler systems (some on-orbit for fifteen years) provided an evolutionary path to a smaller, lower mass electronics package with improved performance and reliability; that design was presented in 2003.[1] Since that time, the design has been scaled up 2x in power, the precision PRT thermometry has been

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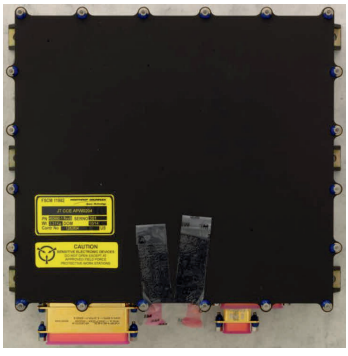

Figure 1. Flight JT Cryocooler Control Electronics.

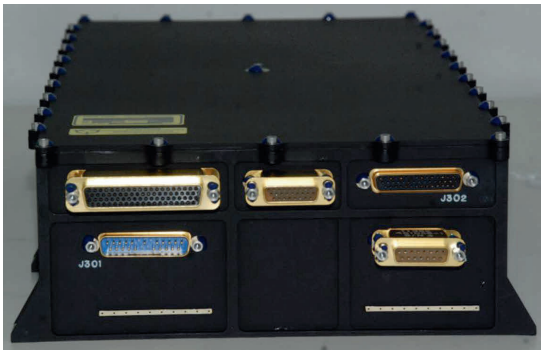

Figure 2. Flight PT Cryocooler Control Electronics.

replaced with precision Cernox[2] thermometry, heater and valve drive and control have been added, and a 1553B interface has been added.

In 2006, the Jet Propulsion Laboratory, as part of the JWST MIRI Cryocooler program, funded the development of two Cryocooler Control Electronics (CCE) units based on the second-generation Advanced Cryocooler Electronics (ACE). One CCE was designed to drive the Joule-Thomson (JT) recirculating compressor; the other was designed to drive the Pulse Tube (PT) compressor. Both CCEs were required to provide precision thermometry down to 4K and communicate with the ISIM (Integrated Science Instrument Module) Controller via a 1553 interface. The JT CCE retains the same power capability as the previous ACE CCE: 180 W. The PT CCE was required to provide up to 360 W output power to drive the PT compressor. Additionally, the PT CCE was required to control and drive five heaters and three latching valves. All other features and capabilities of the ACE (low mass per watt, high reliability, radiation hardness, extensive in-flight diagnostics and advanced vibration control) were retained. Photos of the completed JT and PT CCE units are shown in Figure 1 and Figure 2.

DESIGN DESCRIPTION

The JT and PT CCEs have similar architecture and use the same control board and flight software. The PT CCE's power section is scaled up 2x compared to the JT CCE. Both designs were based on the successful ACE (Advanced Cryocooler Electronics). Top-level design requirements are presented in Table 1. When the ACE was originally designed, we had modular scaling in mind since the HCC (High Capacity Cryocooler) was currently under development with low-temperature detector applications such as MIRI on the horizon. The MIRI PT cryocooler requires up to 325 W drive to meet MIRI cooling requirements, so it was a natural step to double the ACE power capability to 360W. Block diagrams of the JT and PT CCEs are shown in Figure 3 and Figure 4, respectively.

Each CCE is physically divided into two subassemblies: the power subassembly in the bottom contains the high-power DC-DC converters, switching power amplifiers and EMI filters; the control subassembly in the top contains the analog and digital data acquisition, signal processing, control circuitry, housekeeping converter(s), capacitor bank, and in the case of the PT CCE, the heater and valve drivers.

Similar to the ACE, the MIRI CCE's are a microcontroller-based system with all of the control loops implemented in software. 128 KB SRAM provides temporary code and data storage, while 8 KB PROM and 64 KB EEPROM provide non-volatile code and default parameter storage. All code is executed from radiation hardened SRAM. Boot and upload code are stored in PROM, with the balance of the software functions and user constants stored in EEPROM. The contents of the EEPROM can be uploaded on-orbit, providing a capability for

Table 1. Top-Level Design Requirements

Parameter	JT	PT	Comments
Bus Input Voltage	22 to 43VDC	22 to 43VDC	
Output Power	180W	360W	2 channels 10Ω/channel
Reflected Bus Ripple	<200mAp-p	<450mAp-p	at full power
Temperature Measurement Range	4K to 350K	4K to 350K	In 2 ranges
Temperature Control Range	5K to 250K	5K to 250K	
Temperature Measurement Accuracy	< ±10mK	< ±10mK	5K to 15K
	< ±1K	< ±1K	15K to 325K
Temperature Measurement Stability	< ±5mK	< ±5mK	Over 90 min interval
Vibration Control	<200mN	<200mN	On-axis, Adaptive control of each harmonic up to 16th
Cooler Drive Frequency Range	28Hz to 95Hz	28Hz to 95Hz	<0.1Hz increments
Command and Telemetry Interface	1553B	1553B	
Clock Sync Input	Yes	Yes	
Cooler Drive Sync Input	Yes	Yes	
Cooler Drive Sync Output	Yes	Yes	
Heater Drive Power	No	Up to 9W/ch	7 channels
Valve Drive	No	≥1Amp 100ms to 1s	6 channels, current-drive
User-Configurable On-Orbit	Yes	Yes	
Turn-Key Operation	Yes	Yes	
Firmware Uploadable On-Orbit	Yes	Yes	
Non-Volatile Storage	Yes	Yes	
Operating Temperature Range	-35C to +60C	-35C to +60C	Qual/Protoflight range, at full-power
Non-Operating TempRange	-35C to +70C	-35C to +70C	Qual/Protoflight range
Launch Vibration	14grms	14grms	
Total Dose Radiation Hardness	50 krad	50 krad	Can be spot-shielded for higher total dose
Size	7.85 × 9.20 × 3.00 inches	18.0 × 9.20 × 3.60 inches	Including mounting feet and filter-pin connectors
Mass	4.0 kg	9.5 kg	Including filter-pin connectors

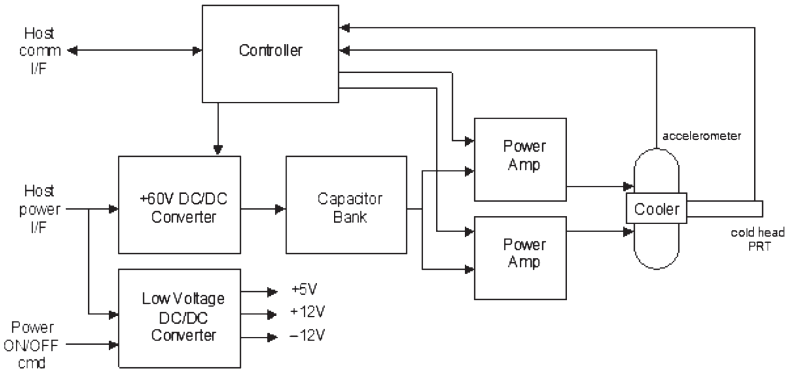

Figure 3. JT Cryocooler Control Electronics Block Diagram

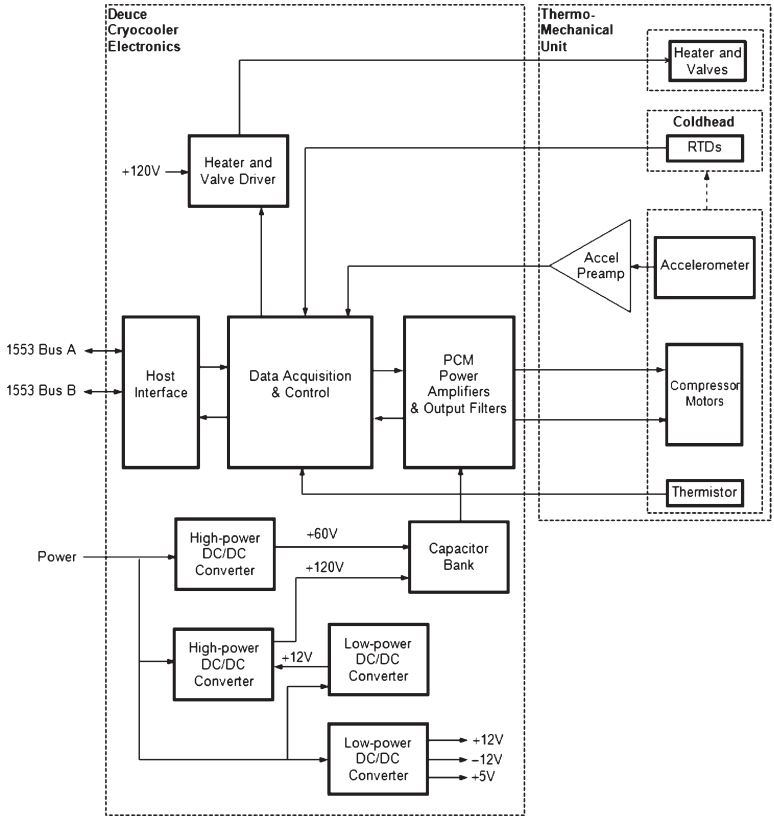

Figure 4. PT Cryocooler Control Electronics Block Diagram

operating parameter changes and software upgrades. The EEPROM also contains command macros, providing a user-configurable "turnkey" operation. A radiation-tolerant, Single Event Upset resistant FPGA provides various digital functions including address/data demultiplexing, address decoding, bus arbitration, DMA (Direct Memory Access), interrupt control, UART (Universal Asynchronous Receiver/Transmitter) serial communications, 1553B serial communications, heater control, valve control, analog data acquisition control, waveform look-up, digital-to-analog conversion, clock generation, synchronization and a watchdog timer. Synchronization between hardware and software activities is provided by a single interrupt that occurs once per cooler cycle (approx 30 Hz for PT, 90 Hz for JT). The data acquisition and waveform generation functions are synchronized to the cooler cycle interrupt. The software maintains a four second timer which is used to pace the software main loop. This four second timer is synchronized to the 1553 periodic broadcast message. Command decoding, telemetry transmission, mode changes, vibration control, temperature control and cooler safety functions are executed sequentially in the four second main-loop.

The precision temperature measurement function monitors up to seven Cernox RTDs (Resistance Thermometer Devices) mounted on the various cold heads in the MIRI cryocooler subsystem for the purpose of reporting and controlling cold head temperatures. The RTDs are measured using a 4-wire (Kelvin) connection, pulsed excitation and synchronized to the compressor drive waveform. Background subtraction removes DC errors, compressor drive pickup and thermocouple effects from the entire signal chain: RTD to A/D output. On-orbit end-to-end calibration enables absolute accuracy to within ±10mK. The on-orbit calibration is accomplished by sampling a precision resistor connected to the eighth Cernox channel. Separate Cernox RTD calibration and curve-fit coefficients for each channel are stored in EEPROM.

Vibration control is realized by sensing on-axis vibration with two redundant pairs of piezoelectric accelerometers mounted on the compressor assembly, two mounted on the JT compressor and two mounted on the PT compressor. Low-noise charge amplifiers are located on the compressor assembly to process the accelerometer signal and drive the cables to the JT and PT CCE's. The vibration signal is sampled synchronously and fed to a proprietary vibration control algorithm which continually adjusts the harmonic content of the compressor drive waveforms. The vibration control function is autonomous and adaptive, adjusting to variations in the compressors and structure dynamics.

Communication is provided over a (dual-redundant) 1553B interface. RS-422 synchronization clock inputs are provided for a 1 MHz reference clock and a cooler synchronization clock. An RS-422 synchronization clock output at the cooler drive frequency is also provided. The synchronization clocks are optional, and the CCEs functions normally in the absence of synchronization clocks. Fault management is enhanced by a RS-422 bi-level input (SAFE/HOLD) that provides the user a method of commanding the CCEs to Standby mode without using the 1553 communication channels. A RS-422 bi-level output (FAULT) provides the user a method of detecting cooler system safety exceptions without using the 1553 communication channels. A single-ended, bi-level POWER ON/OFF command enables the CCE's power converters. A passive caging relay monitor allows the user to observe the caging relay status without powering the CCEs.

A comprehensive diagnostic database is available for cryocooler system health monitoring and on-orbit debugging. Telemetry data includes cooler system mode, state and safety status, coldhead, compressor, heater and electronics temperatures, secondary power supply voltages, compressor voltage and current waveforms, vibration measurement parameters and vibration control parameters. In addition all areas of RAM can be read and written by the user for diagnostic and troubleshooting purposes.

A VCXO (voltage controlled crystal oscillator) generates a 16 MHz clock from which all internal clocks are derived. The 16 MHz clock is divided by 16 and phase-locked to the (optional) 1 MHz external reference clock.

The JT power subassembly contains a 200 W DC-DC converter, two switching power amplifiers, and EMI filters. The JT's DC-DC converter provides +60VDC to the capacitor bank and switching power amplifiers. The PT power subassembly contains two 200 W DC-DC converters, two switching power amplifiers, and EMI filters. The PT's DC-DC converters have their +60 VDC outputs wired in series to provide +120 VDC to the capacitor bank, switching power amplifiers and valve drive. The heater drives are powered off of the +60 VDC rail. The 60 V DC-DC converters are custom-designed modules that implement an active ripple control function. Each 60 V DC-DC converter is conservatively rated at 200 W output over the full range of bus voltages and operating temperatures. A smaller housekeeping converter provides +5 VDC and ±12 VDC to the control and power amplifier boards. An additional floating +12 VDC powers the secondary circuits in the upper 60 V DC-DC converter in the PT CCE. The 60 V DC-DC converters and the main housekeeping converter are synchronized to the CCE's 16 MHz master clock. The 60 V DC-DC converters are disabled when the CCEs are in Standby mode to conserve power. A single-ended, primary-referenced, bi-level command is provided to enable the main housekeeping converter, which in turn enables the 60 V DC-DC converters and auxiliary low-voltage converter. When all converters are disabled, the power consumption is less than 1W per CCE.

The power amplifiers are realized as H-bridge PCM switching amplifiers. Each JT channel is capable of delivering up to ±40 V peak, ±6 A peak or 90 W average. Each PT channel is capable of delivering up to ±72 V peak, ±9 A peak or 180 W average. Passive L-C filters smooth the power amplifier outputs and control EMI. Each amplifier channel contains a high-speed short-circuit current detector to protect the power amplifiers in the event of a shorted cable or load. The power amplifier design takes advantage of its inherent linearity by operating open-loop. The open-loop configuration ensures unconditional stability when driving the complex, non-linear load presented by the cryocooler compressors. Latching relays located on

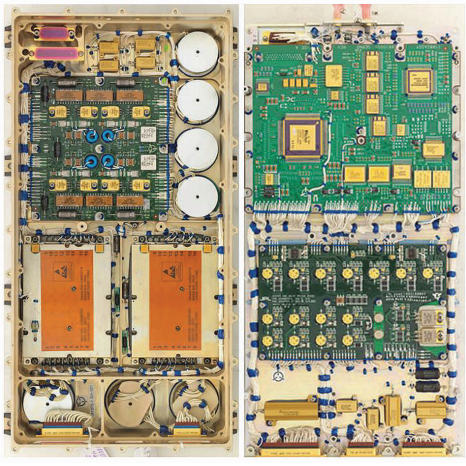

Figure 5. PT CCE subassemblies.

the power amplifier board cage (restrain) the cryocooler compressor pistons during launch by shorting the motor windings. These caging relays are dual-redundant and are controlled by user commands. In addition to 1553 telemetry indicating the caging relay status, a passive, bi-level output is provided on the communications connector to indicate caging relay status. This permits the user to monitor the caging relay status while the CCEs are powered off. The JT and PT power subassemblies are capable of delivering at least 180 W or 360 W, respectively, on a continuous basis to the cryocoolers.

The MIRI Cryocooler Subsystem contains a pair of latching cryogenic valves and six heaters. A heater and valve drive board has been designed and built at JPL and integrated into the PT CCE. Valves are all powered from the CCE's internal +120 VDC bus; heaters are powered from the +60 V bus. Because the valve winding DC resistance varies significantly over the range of operating temperatures, constant-current valve drive was selected. Series-redundant switches are incorporated into the valve and heater drivers to enhance reliability. The valves contain redundant coils which are driven by either the primary or secondary PT CCE. The CCE software can vary the valve drive pulse width under user command to accommodate faults such as shorted valve windings. Six heater drivers are provided for bang-bang control of valve heaters, decontamination heaters, and a He mass-flow sensor heater on the JT loop. Ballast resistors sized for each heater control the peak heater power. Average heater power is controlled by software bang-bang controllers. A solid-state circuit-breaker function is provided for each heater driver to protect against shorted heaters or cables.

Constructed similar to the ACE, the JT and PT CCE's are housed in an aluminum chassis machined from a single piece. Figure 5 shows the PT CCE internal configuration with the power subassembly on the left, and control subassembly on the right. Figure 6 shows the JT CCE internal configuration. 3-D solid modeling tools were used to design and layout the CCEs. Using these tools,

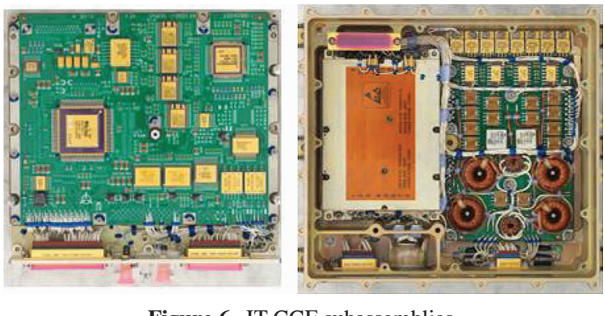

Figure 6. JT CCE subassemblies.

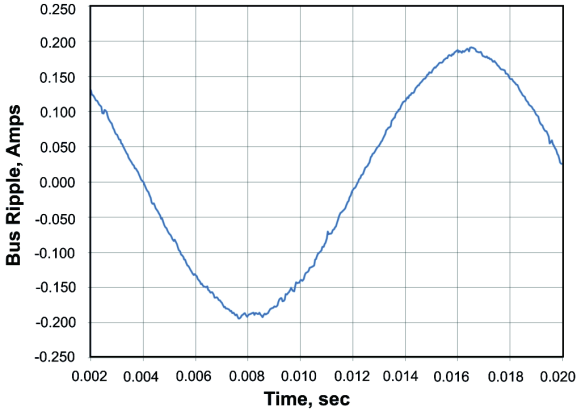

Figure 7. Flight PT bus current ripple

we were able to efficiently nest the various components, identify clearance and manufacturing issues early in the design process, accurately estimate mass, and perform thermal and structural analyses. The result was a CCE design that was easy to build and fit together perfectly on the first pass. All high power devices are mounted to the floor of the chassis, providing an excellent thermal path to the heat rejection surface. An internal shield plate forms an RF barrier inside the unit, separating the power and control subassemblies. The control subassembly is built up on the shield plate and then dropped into the unit. D-connectors located inside the unit connect the two subassemblies. An input filter cavity contains feedthrough filters, a common-mode choke, and the input power input connector. An output filter cavity contains feedthrough filters, two common-mode chokes, and the compressor drive connector. The shield plate closes off these RF-tight cavities.

D-connectors and two triaxial connectors provide interfaces to the user and the cryocooler: DC input power, communications, valve and heater drive, cryocooler compressor drive, and cryocooler instrumentation.

PERFORMANCE DATA

The flight CCEs were acceptance tested with resistive loads prior to integration with the MIRI cryocooler compressor assembly. Figure 7 shows the active ripple suppression at work: the PT CCE input ripple current is <400 mA p-p while producing full power (360 W) at 30.5 Hz with a 28 V bus. Figure 8 plots ripple current as a function of output power. Without ripple suppression, the input

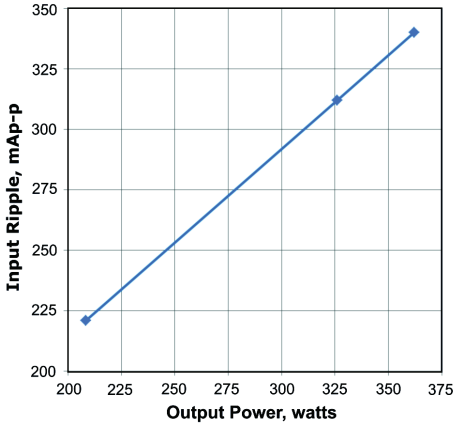

Figure 8. Flight PT bus current ripple vs output power.

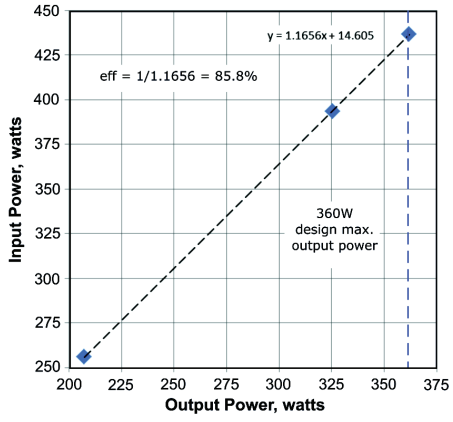

Figure 9. Flight PT CCE input power vs. output power.

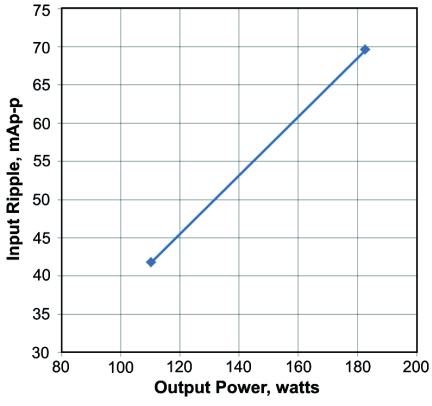

Figure 10. Flight JT CCE ripple current vs. output power.

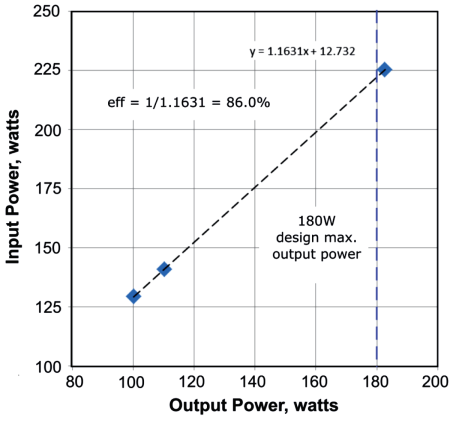

Figure 11. Flight JT CCE input power vs. output power.

current ripple would exceed 42 amps p-p. The PT CCE's active ripple suppression provides over 40 dB ripple attenuation at full power.

Figure 9 plots the PT CCE input power as a function of output power over a range of output power from 205 W to 365 W. The efficiency is flat at 85.8%. As shown in Figure 10, the JT CCE ripple current is <70 mA p-p while producing full power (180W) at 90Hz with a 28V bus. This is equivalent to 50 dB of attenuation.

Figure 11 plots the JT CCE input power as a function of output power over a range of output power from 100 W to 183 W. The efficiency is flat at 86.0%.

CONCLUSION

The MIRI Cryocooler Control Electronics meet all of their performance requirements for cooling the JWST MIRI detector to 6 K.

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2. Cernox is a registered trademark of Lake Shore Cryotronics, Inc.