UVM-Based RTL Verification – ARM SSG

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Senior Verification Engineer
ARM Holdings– Cambridge - UK

Summary

- **Short Bio**
- **ARM Holdings**
- **RTL Verification**
- **UVM Methodology**
- **Verification Flow and Tools**
- **Cambridge, England**

Short Bio

- **Education**
  - Bachelor's Degree in Computer Science at PUCRS, Campus II (Uruguaiana-RS, Brazil) – 2000
  - M.Sc. in Computer Science at PUCRS (Porto Alegre-RS, Brazil) – 2002
  - Ph.D. in Computer Science at UFRGS (Porto Alegre-RS, Brazil) – 2007
    - Sandwich doctorate at Technische Universität Darmstadt (Germany) – 2005

Short Bio

- **Work Experience**
  - Freelancer (Telecom) – GAPH PUCRS / PARKS S.A. (2000 - 2002)
  - Freelancer (Telecom) – Datum TI / Digitel S.A. (01/2003 – 04/2003)
  - Freelancer (RFID) – GSE PUCRS (2006 - 2007)
  - Assistant Teacher, Unisinos University, São Leopoldo-RS, Brazil (2007-2009)
  - IC Verification Engineer, CEITEC, Porto Alegre, Brazil (2007 - 2015)
  - Senior Verification Engineer, ARM, Cambridge, UK (2015 - current)

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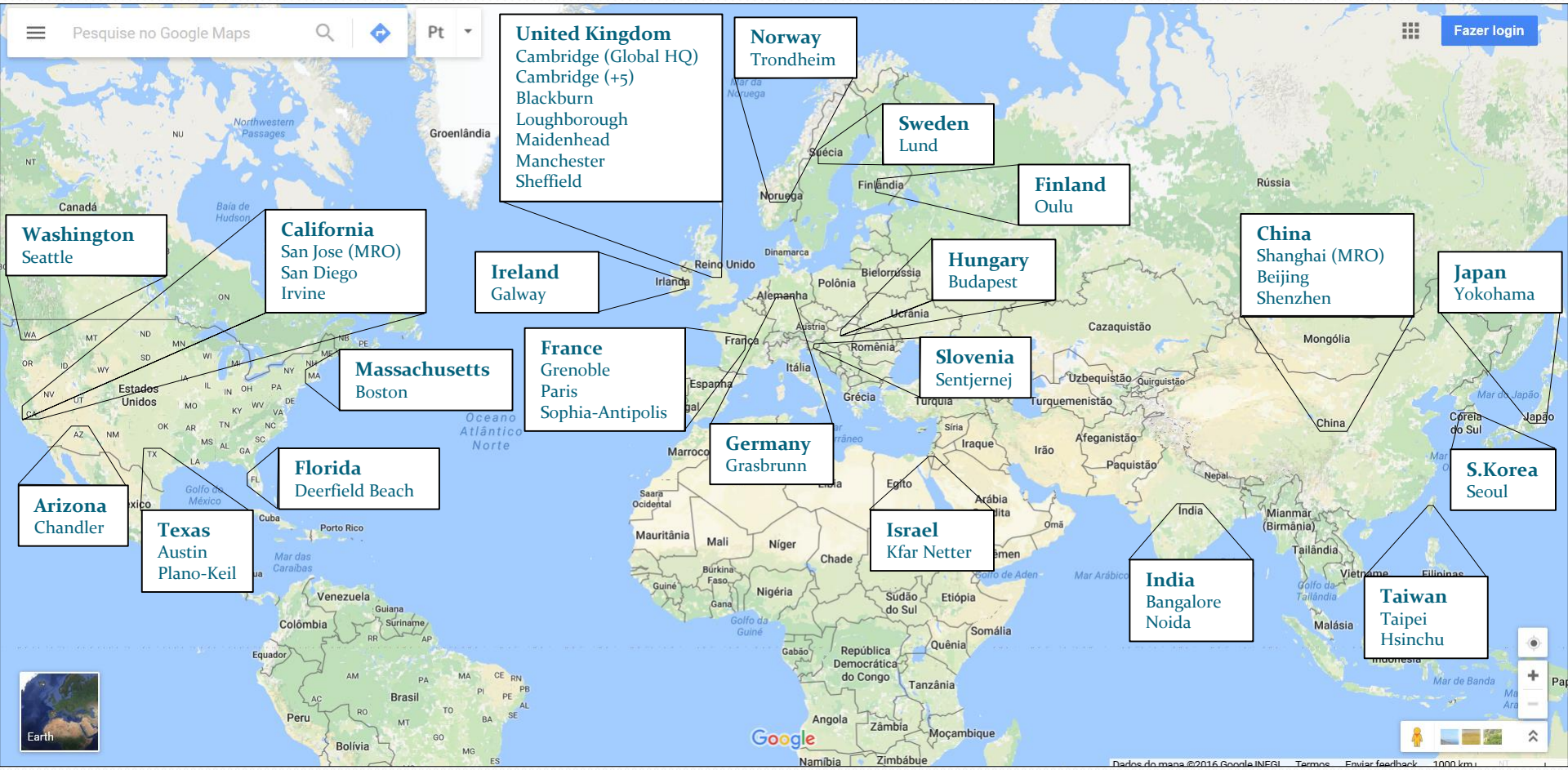
ARM Holdings

- The world's leading semiconductor IP company founded in 1990 (26 years)
- Acorn RISC Machine (1983) -> Advanced RISC Machines (1990)
- ARM technologies reach 80% of the global population
- More than 4,200 people from 61 nationalities
- Nearly four billion ARM technology-based chips shipped every quarter

ARM Holdings

- More than 86 billion ARM-based chips shipped to date (14.9bn 2015 and 12.1bn in 2014)
- 95% of smartphone market; 85% of mobile devices (smartphones, tablets, laptops)
- 1,379 licenses sold to more than 450 partners
- Joined SoftBank Group Corp in 2016 (at a price of £24 billion)

ARM Offices


United Kingdom
Cambridge (Global HQ)
Cambridge (+5)
Blackburn
Loughborough
Maidenhead
Manchester
Sheffield
Norway
Trondheim
Sweden
Lund
Finland
Oulu
Washington
Seattle
California
San Jose (MRO)
San Diego
Irvine
Ireland
Galway
Hungary
Budapest
China
Shanghai (MRO)
Beijing
Shenzhen
Japan
Yokohama
Massachusetts
Boston
France
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Sophia-Antipolis
Slovenia
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Germany
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Florida
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Arizona
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Texas
Austin
Plano-Keil
Israel
Kfar Netter
India
Bangalore
Noida
S.Korea
Seoul
Taiwan
Taipei
Hsinchu

ARM Engineering Groups

- Architecture and Technology
- CPU
- Development Solutions
- Business Lines
- Internet of Things (IoT)
- Media Processing
- Partner Enablement
- Physical IP Design
- Project Management
- Research
- Systems and Software
- Technical Operations
- Wireless Business Unit

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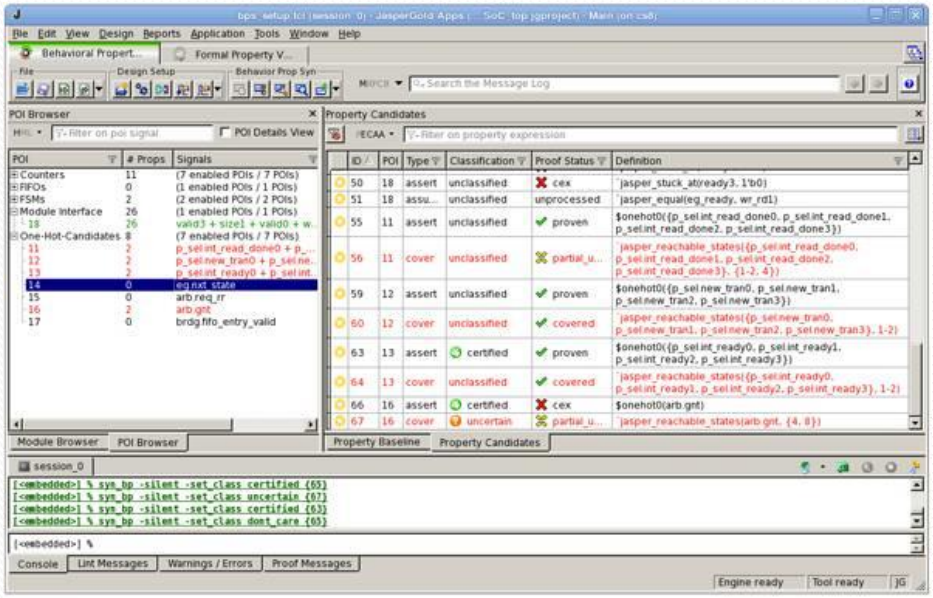
RTL Functional Verification

- Ensures that the design is logically correct
- Functionality is fully implemented and working as expected (matches the specification)
- Types of Functional Verification:
  - Formal Verification
  - Simulation-Based Verification

Formal Verification

- No input vectors
- Assertion-based
- Assumptions
- Statistic models
- Suitable for blocks, not for systems

Jasper Gold

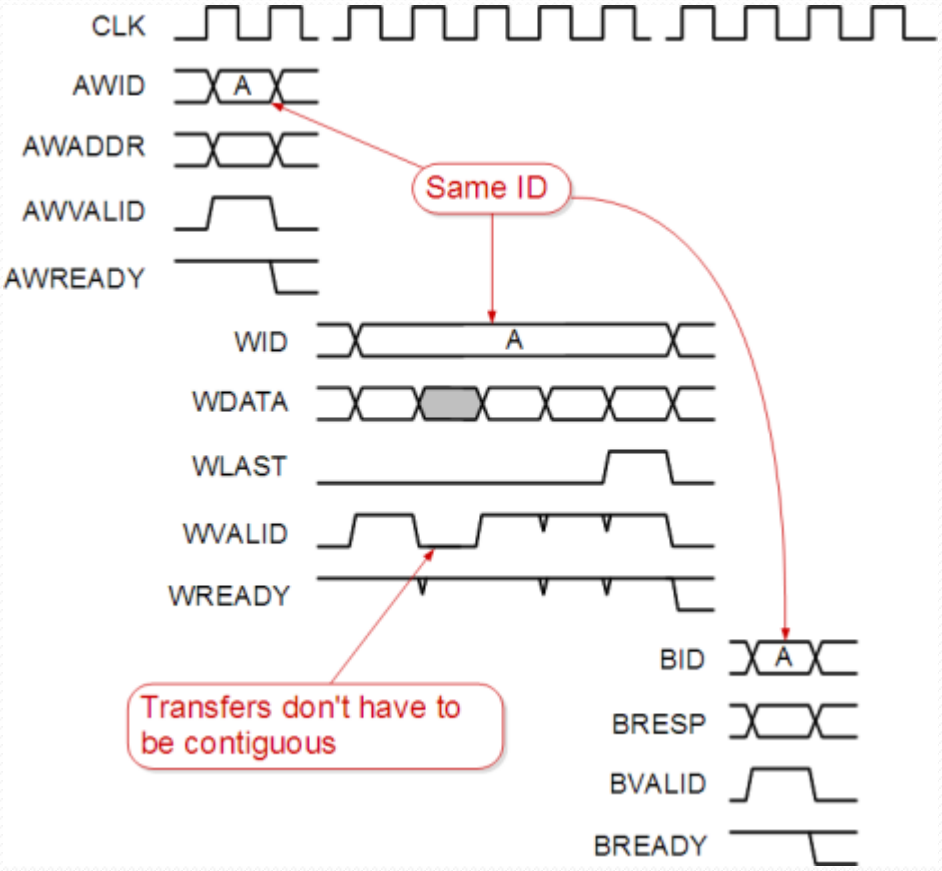


- Very useful when developing Protocol Checkers

```
assume in_1 != in_2
...
assert out_1 > out_2
...
```

Protocol Checker

- Ex: Amba 4
  - More than 50 signals
  - Set of rules for data transfer
- Protocol Checker
  - SV Module
  - Auxiliary logic
  - Assertions



Simulation-Based Verification

- Input vectors
- Output checkers
- Direct tests
  - Easy to cover some specific conditions
- Random tests
  - Random constraints
  - Functional coverage to ensure specific conditions are covered
- UVM – Universal Verification Methodology

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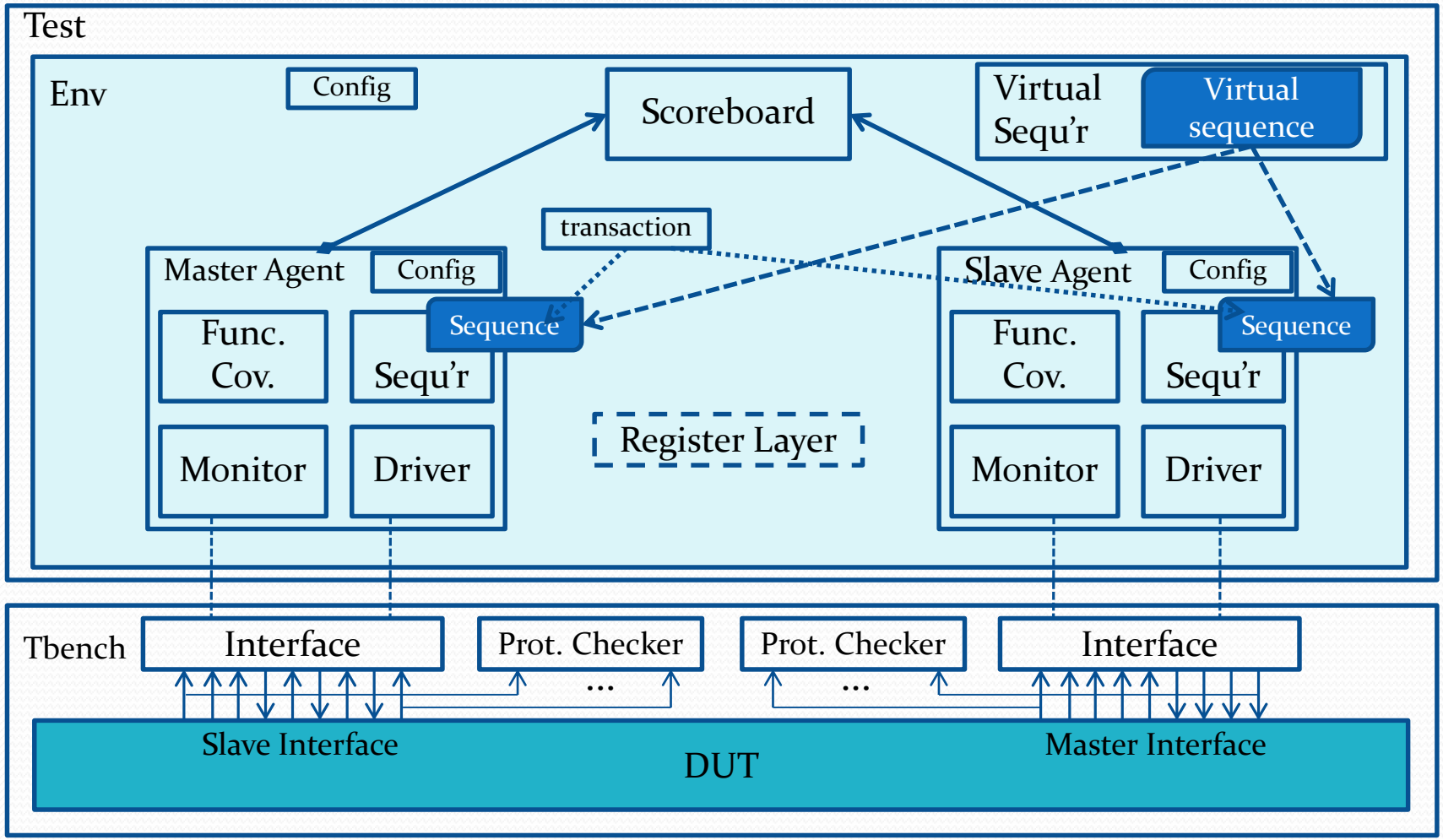
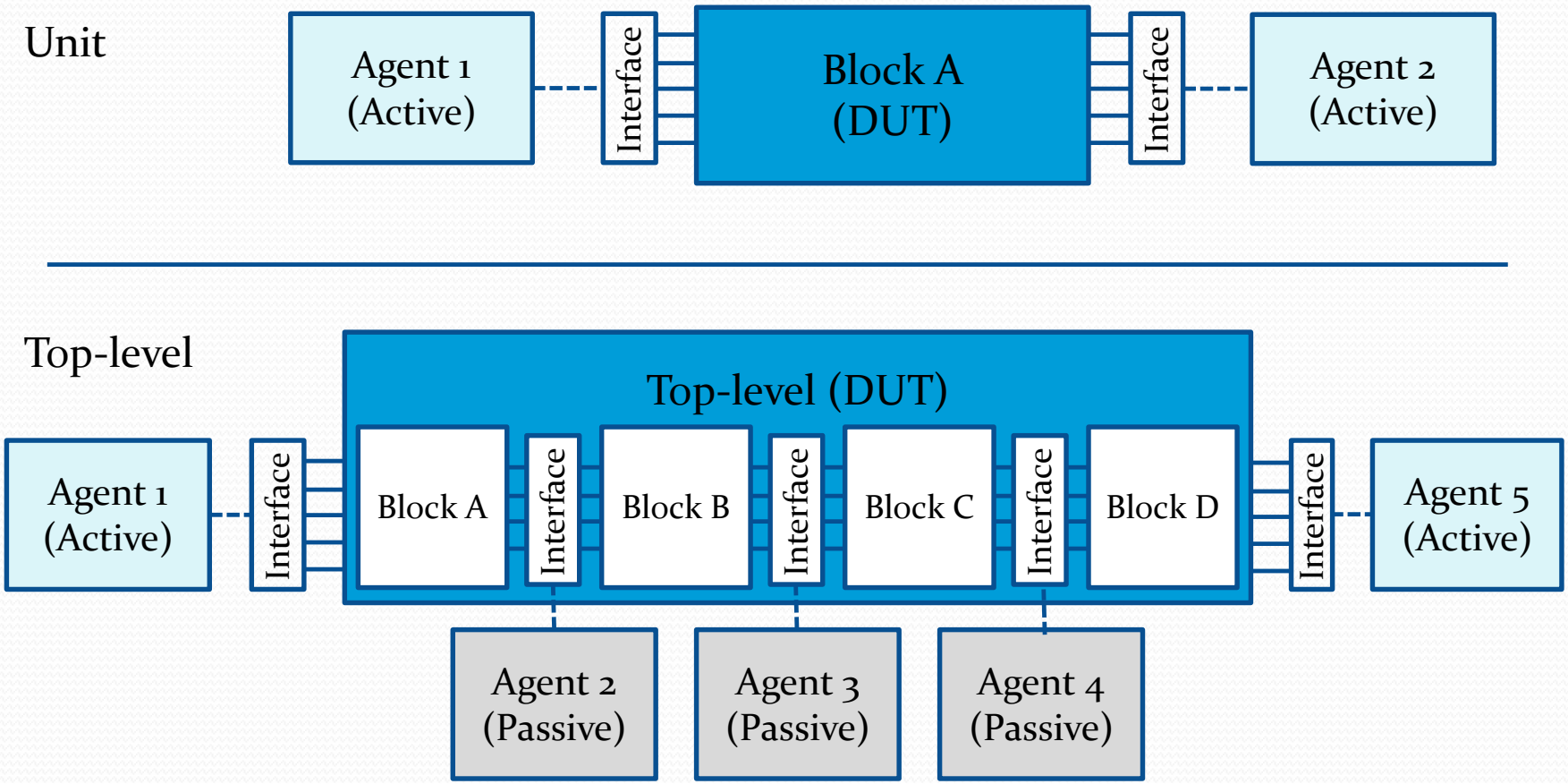
UVM – Universal Verification Methodology

- Standardized methodology derived mainly from the OVM (Open Verification Methodology) aiming the reuse of components
- Brings automation to the SystemVerilog: sequences and data automation features (packing, copy, compare) etc.
- Support from multiple vendors: Aldec, Cadence, Mentor, and Synopsys
- Standard hierarchy, structures, configurations, connections makes easier the understanding and the reuse of components

Simulation-Based Verification Using UVM

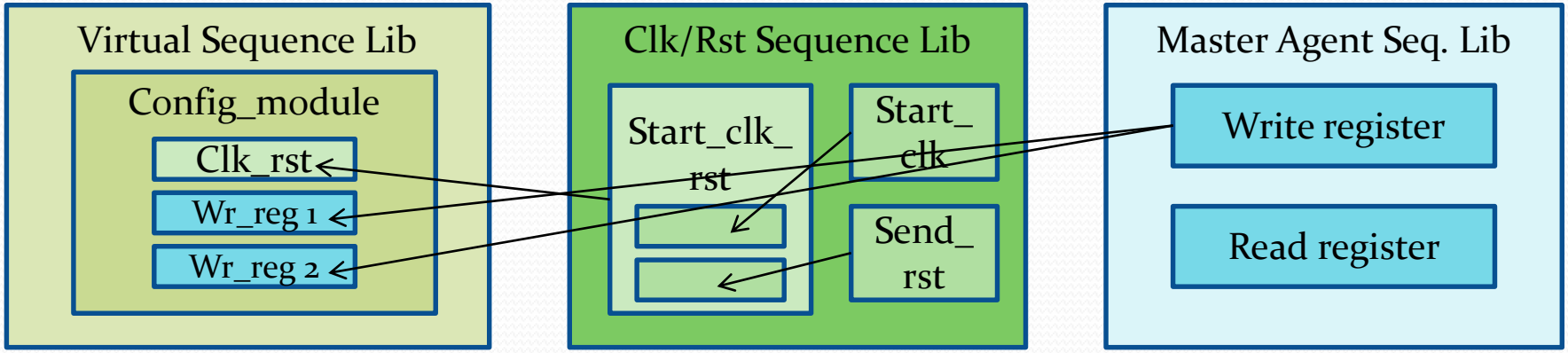


Simulation-Based Verification



For functional coverage and to feed scoreboards

UVM Sequences



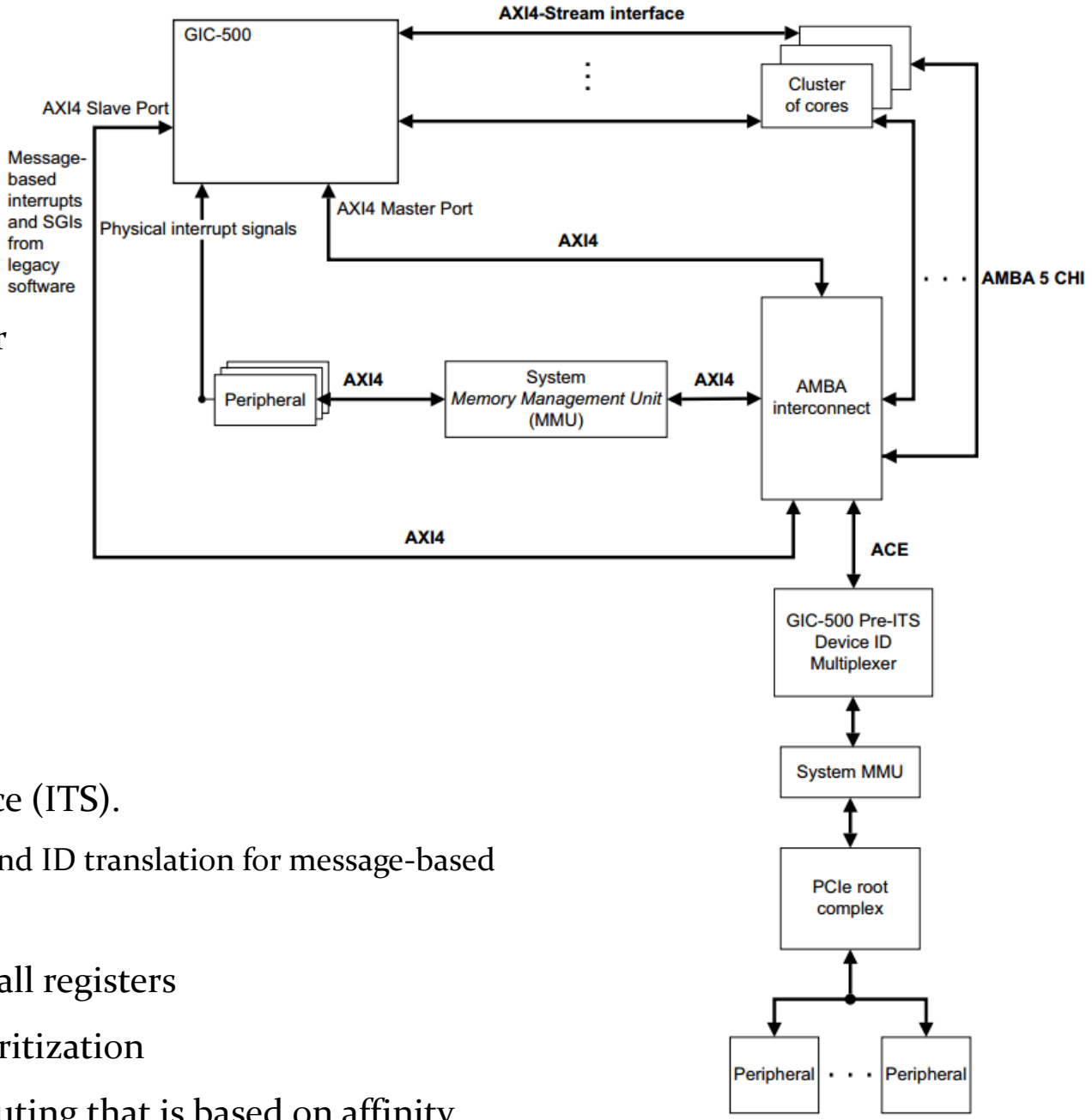
Test 1

```
...
virtual_seqr.start (config_module)
...
master_sequr.start(write_reg)
...
err_inject_seqr.start(inject _err)
```

Test 2

```
...
slave_seq.start(reactive_sequence)
...
virtual_seqr.start (config_module)
...
master_seqr.start(read_reg)
```

Ex:GIC500



- Configurable int. Controller
- Compatibility: ARMv8 (ex: Cortex-A53, Cortex-A57)
- Up to 128 cores
- Up to 32 affinity-level 1 clusters
- Up to 8 cores per cluster
- Interrupt Translation Service (ITS).
  - provides device isolation and ID translation for message-based interrupts
- Memory-mapped access to all registers
- Interrupt masking and prioritization
- Programmable interrupt routing that is based on affinity

GIC 500 Interrupt Types

- **Locality-Specific Peripheral Interrupts (LPIs)**
  - Message-based interrupt
  - Generated by a peripheral writing to a memory-mapped register
  - Target only one core at a given time
- **Shared Peripheral Interrupts (SPIs)**
  - Used for peripherals that are not tightly coupled to a specific core
  - Configurable: 32 to 960
  - Generated by wires of writes to AXI4 slave port
- **Private Peripheral Interrupts (PPIs)**
  - Independent for each core and can be programmed to support either edge-triggered or level-sensitive interrupts
  - Used for peripherals that are tightly coupled to a particular core
- **Software Generated Interrupts (SGIs)**
  - Inter-processor interrupts, that is, interrupts generated from one core and sent to other cores
  - Generated through register write

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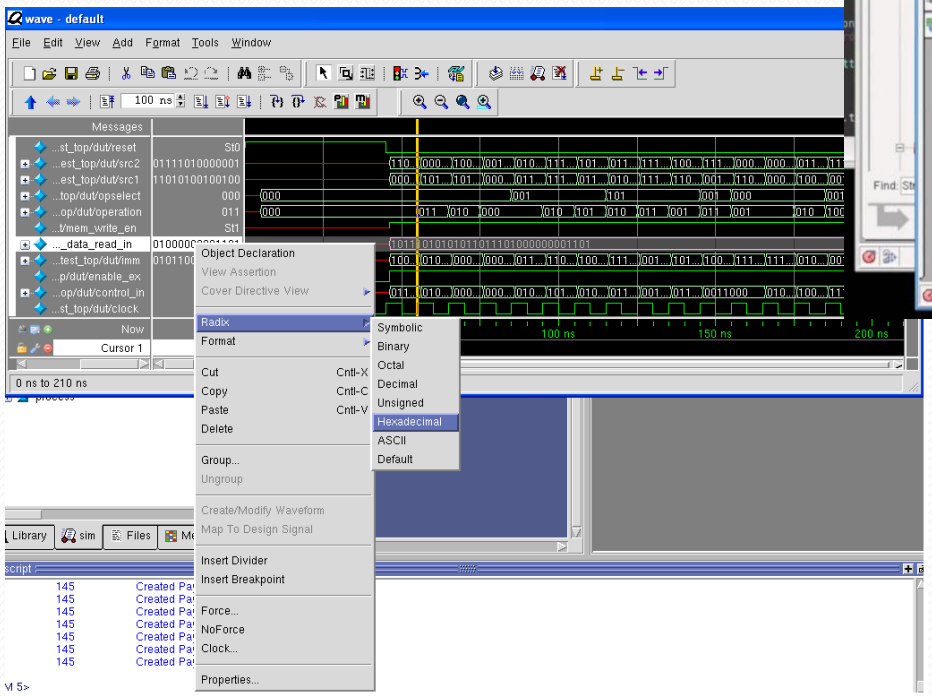
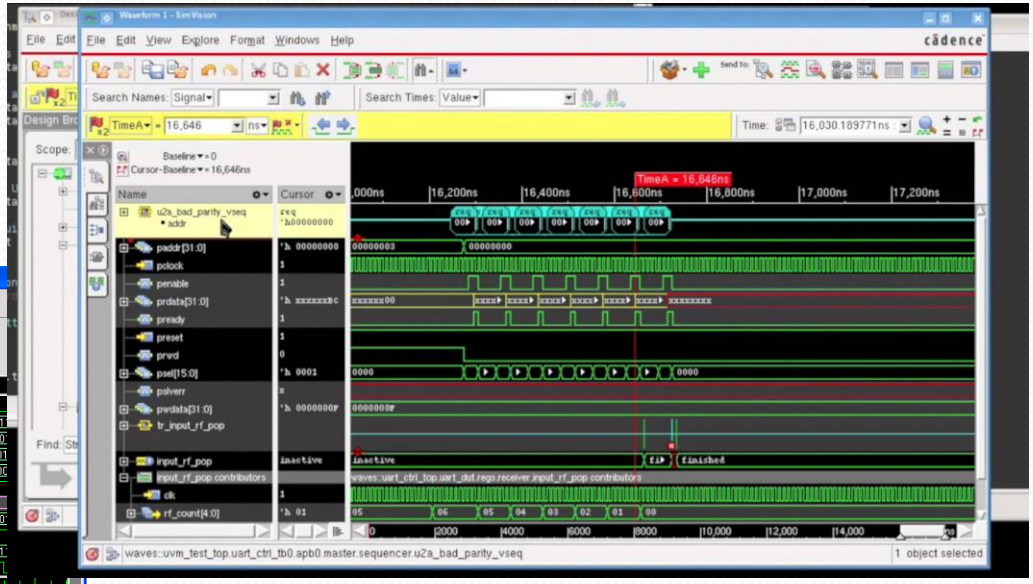
Simulation Tools

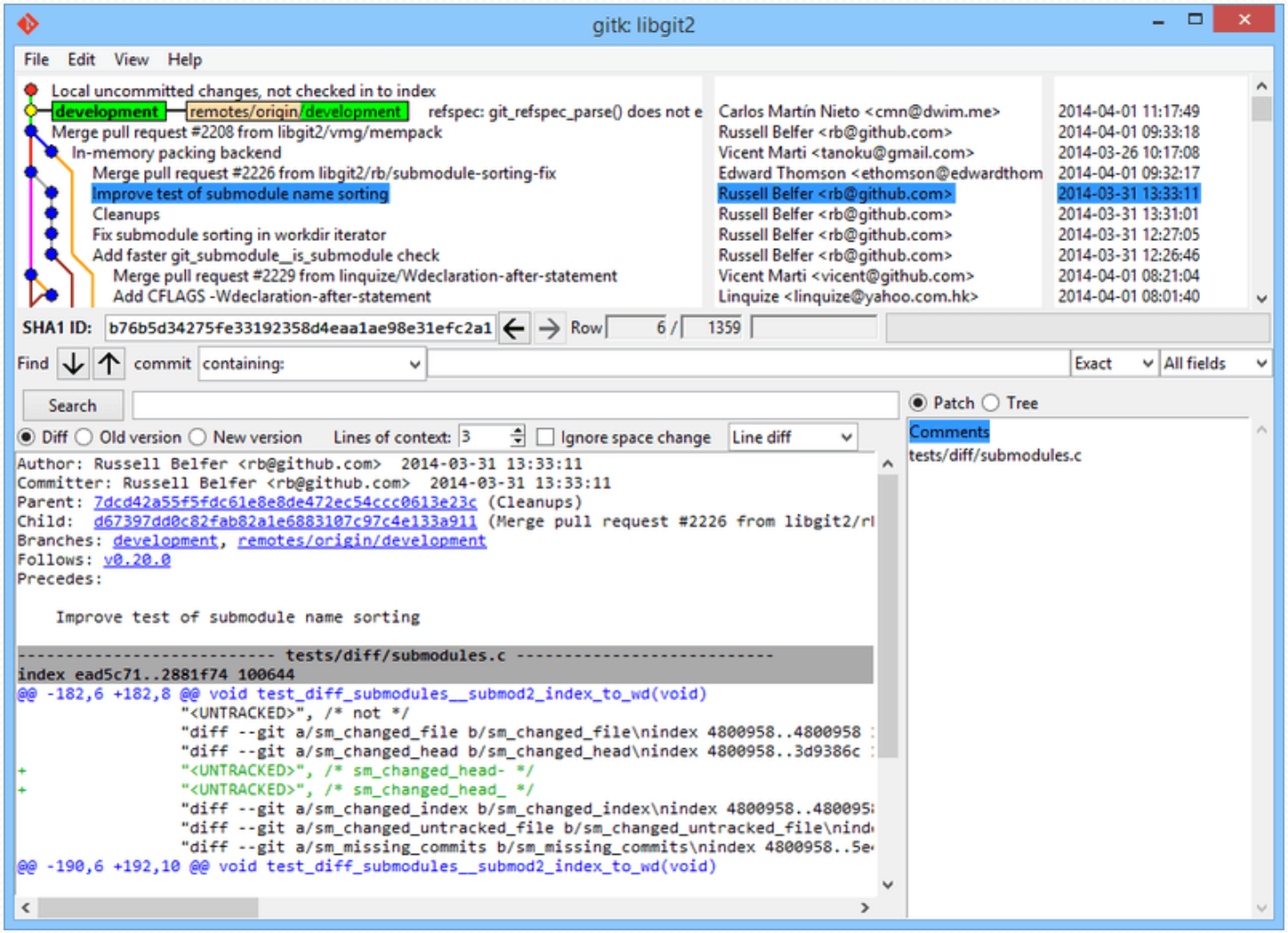
Mentor Modelsim/Questasim (MTI)



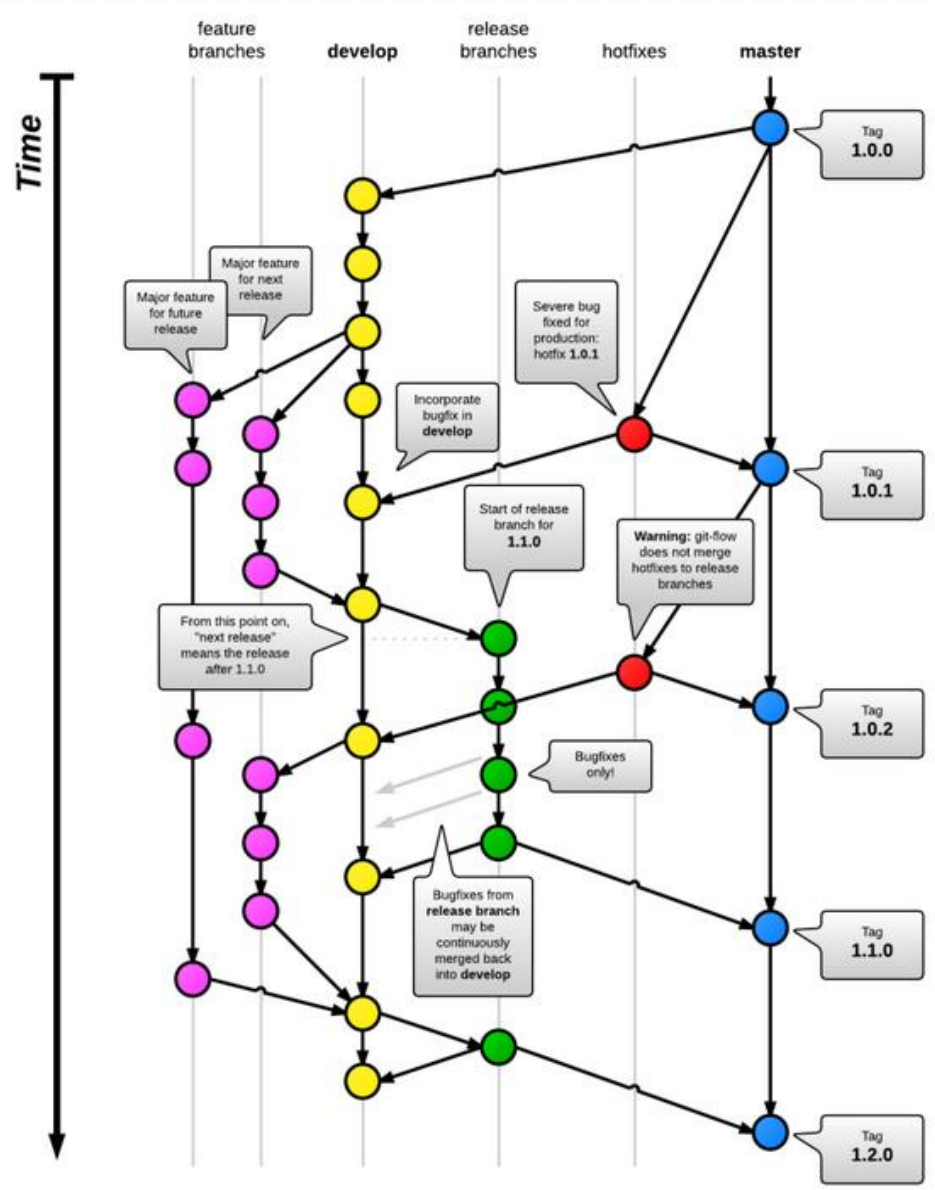


Cadence NCSim

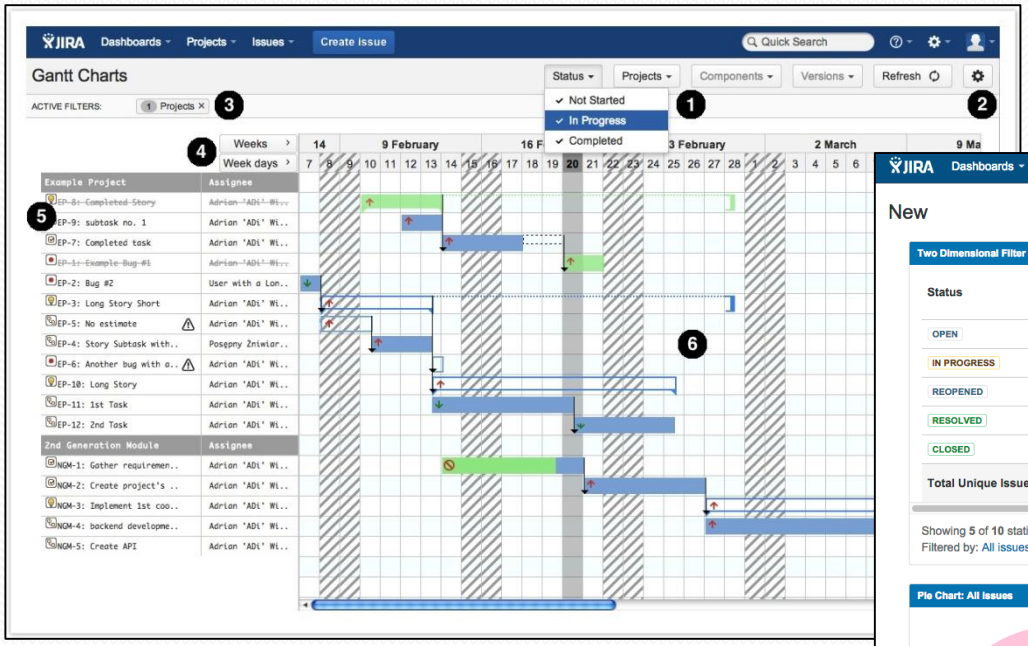
GIT - Version Control System



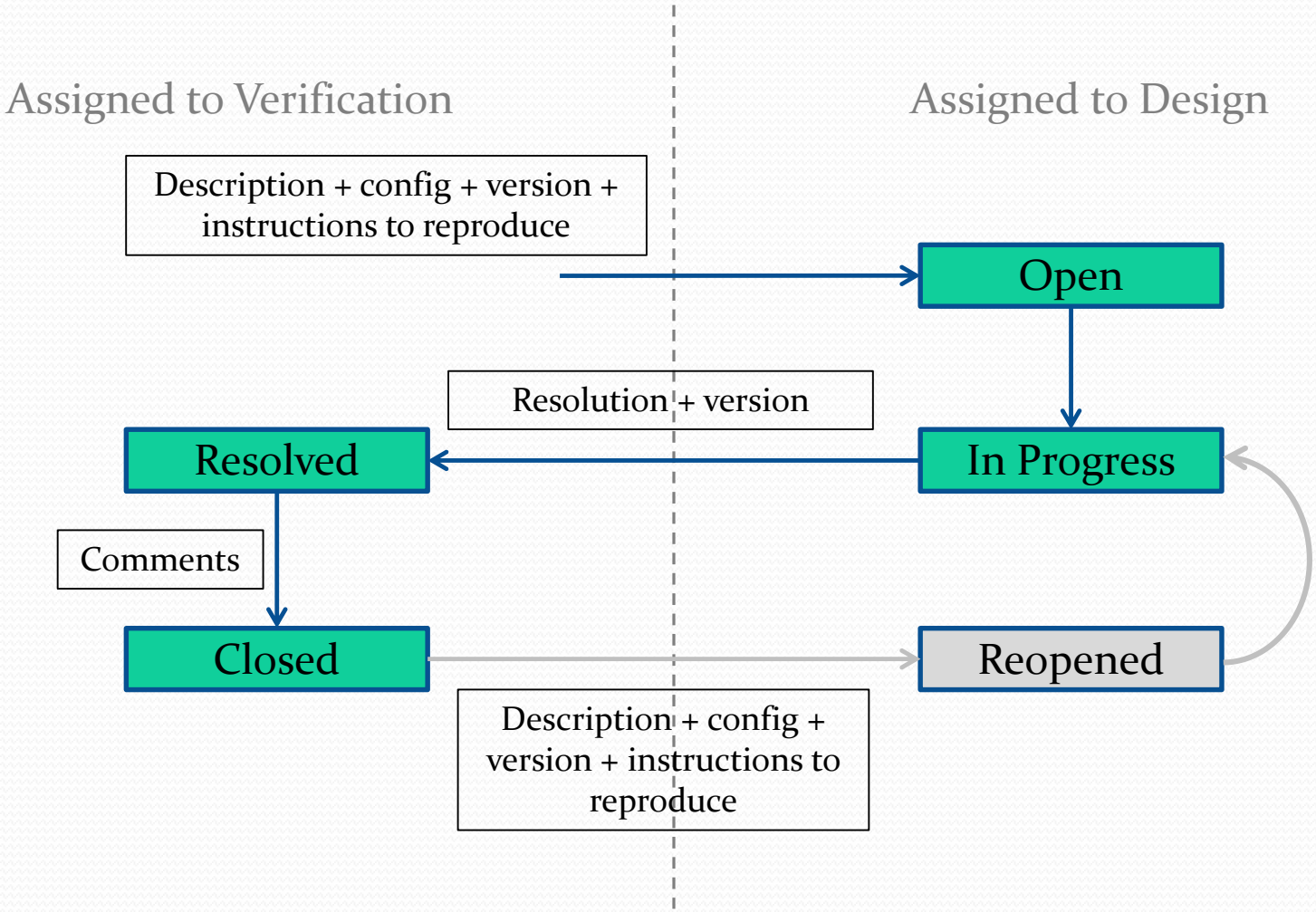
GIT Flow


feature branches
develop
release branches
hotfixes
master
Time
Tag 1.0.0
Major feature for next release
Major feature for future release
Severe bug fixed for production: hotfix 1.0.1
Incorporate bugfix in develop
Tag 1.0.1
Start of release branch for 1.1.0
Warning: git-flow does not merge hotfixes to release branches
From this point on, "next release" means the release after 1.1.0
Tag 1.0.2
Bugfixes only!
Bugfixes from release branch may be continuously merged back into develop
Tag 1.1.0
Tag 1.2.0

JIRA – Issue and Project Tracking

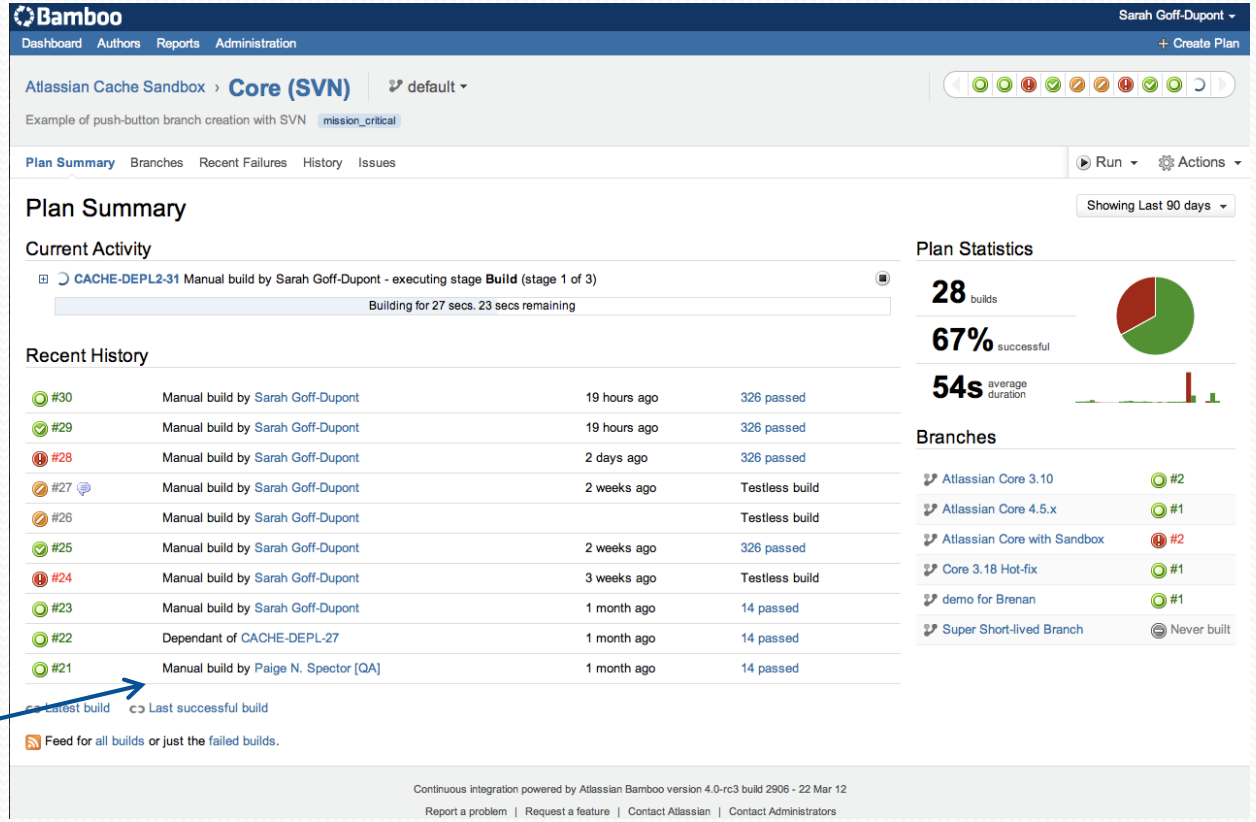


Typical Bug Workflow



Bamboo

- Continuous Integration Server
  - Automated builds and tests
  - Regression reports



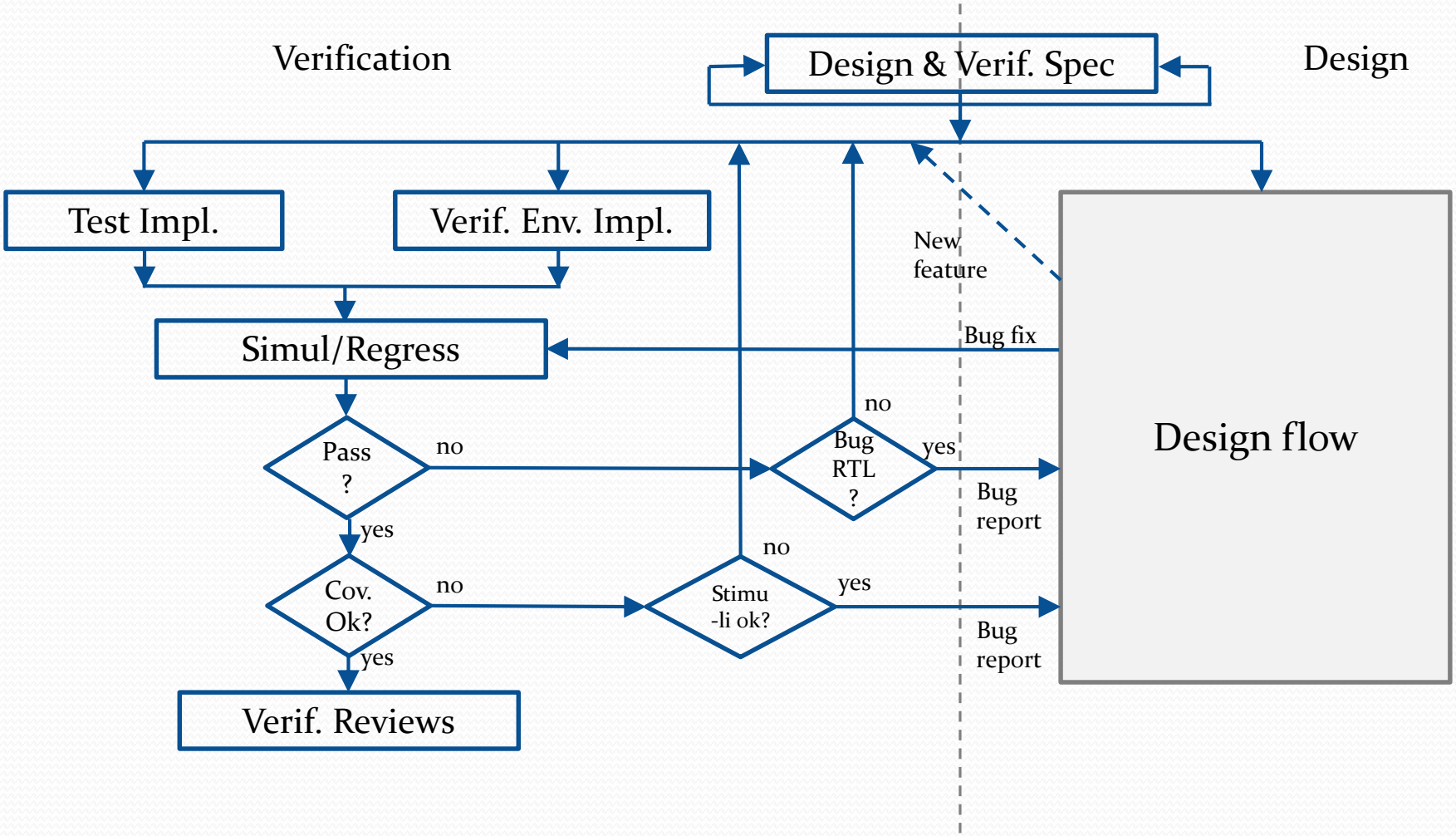
Verification Metrics

- Measures the quality of verification
- Necessary to define the end of verification process
- Code coverage
  - Statements, branches, toggle, FSMs
- Functional coverage
  - % of functionality verified (sequences, cross, states combined to inputs/outputs)
- Pass rate
  - % Success/Fail
- Different (increasing) requirements per milestone

Design Milestones

- Alpha and Beta milestones are internal quality milestones.
- LAC (Limited Access) represents the milestone after which lead partners get access to the IP
- EAC (Early Access) represents the point after which the IP is ready to be fabricated for obtaining engineering samples and testing
- REL (Release): the IP has gone through rigorous testing and is ready for mass production.

RTL Verification Flow



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ARM HQ - Cambridge

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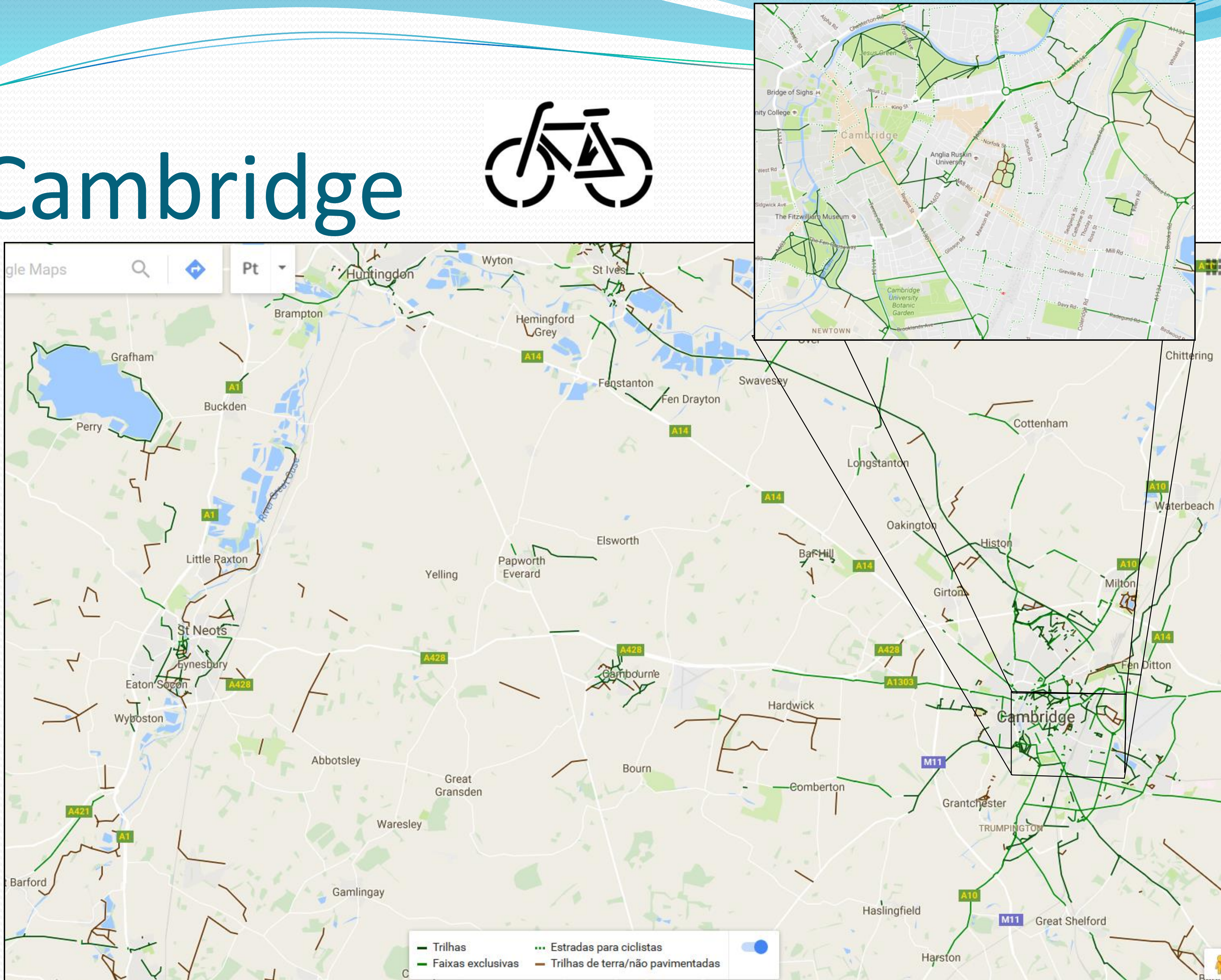
Cambridge

ARM HQ

Cambridge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Pt
Huntingdon
Wyton
St Ives
Brampton
Hemingford Grey
Grafham
Buckden
Perry
Fenstanton
Fen Drayton
Swavesey
Over
Chittering
Cottenham
Longstanton
Waterbeach
Oakington
Histon
Elsworth
Bar Hill
Little Paxton
Papworth Everard
Yelling
Girton
Milton
St Neots
Eynesbury
Eaton Socon
Cambourne
Fen Ditton
Wyboston
Hardwick
Cambridge
Abbotsley
Great Gransden
Bourn
Comberton
Grantchester
TRUMPINGTON
Waresley
Barford
Gamlingay
Haslingfield
Great Shelford
Harston
Moggerhanger
Hatley
River Great Ouse
A1
A14
A10
A428
A1303
A421
M11
Trilhas
Faixas exclusivas
Estradas para ciclistas
Trilhas de terra/não pavimentadas
Bridge of Sighs
Jesus Green
Cambridge
Anglia Ruskin University
The Fitzwilliam Museum
Cambridge University Botanic Garden
NEWTOWN
Mill Rd
Greville Rd
Davy Rd
West Rd
Sidgwick Ave
King St
Norfolk St

Cambridge

The Tab's Map of Cam...

The Tab aims to review all of Cambridge's Pubs, letting you know important things such as how much a pint costs, what the

6,550 views

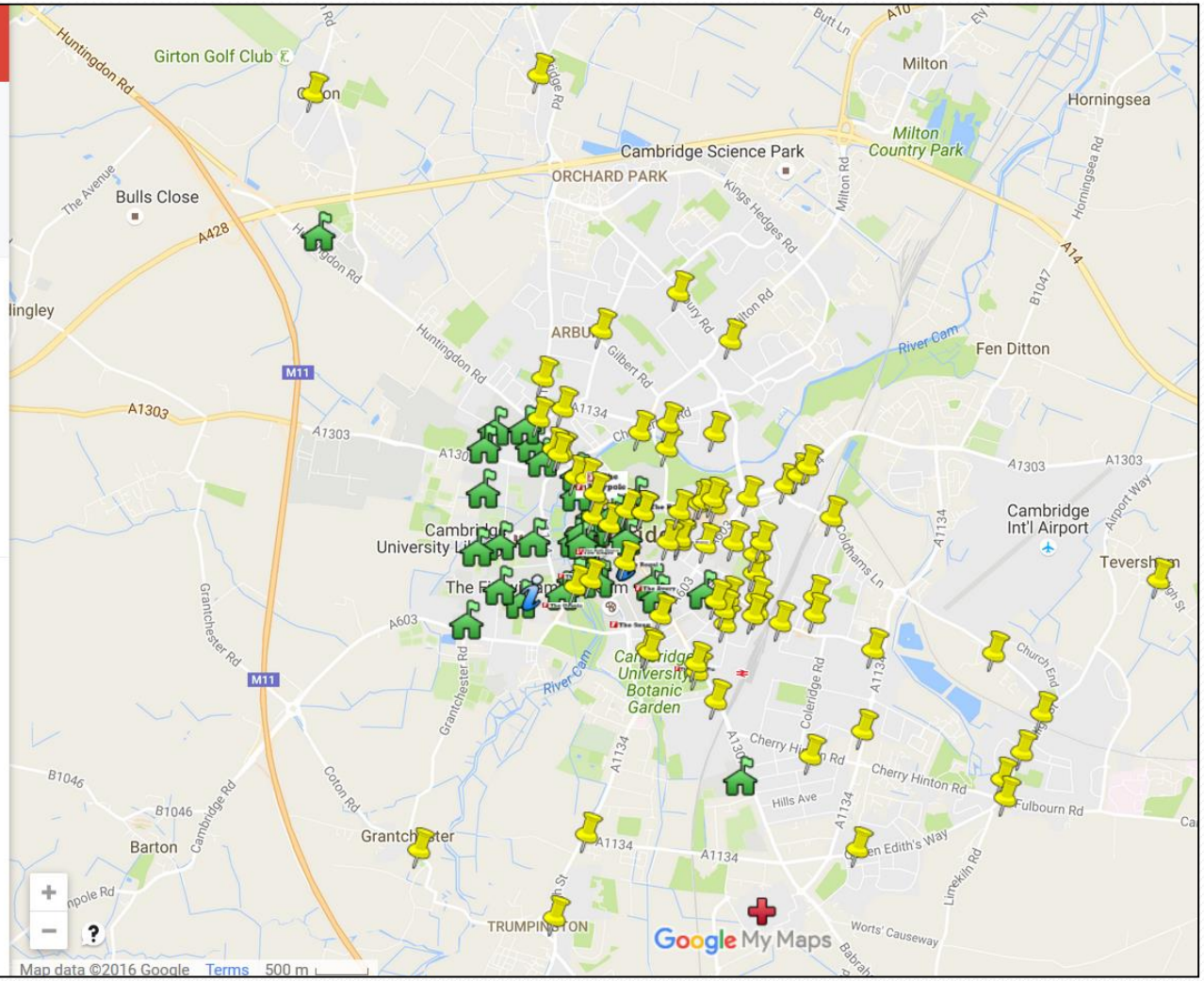
SHARE

Untitled layer

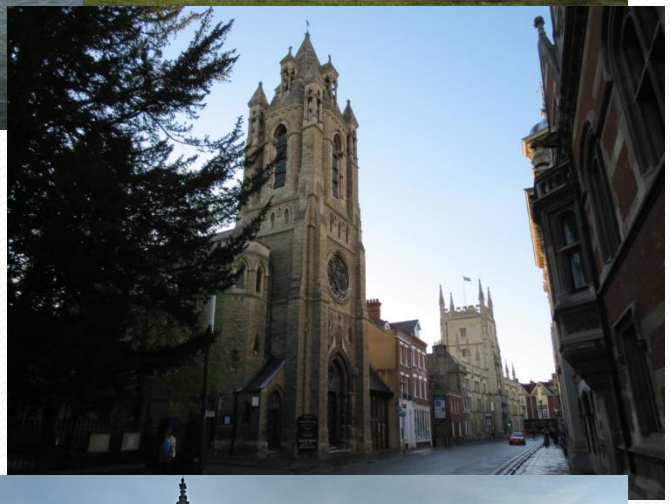
- The Rad
- The Salisbury Arms
- Cambridge Blue
- Alexandra Arms

... 117 more

Made with Google My Maps



Cambridge



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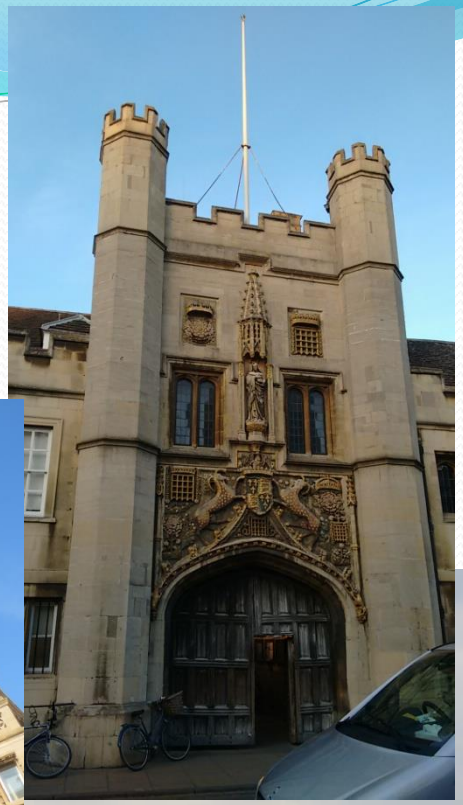

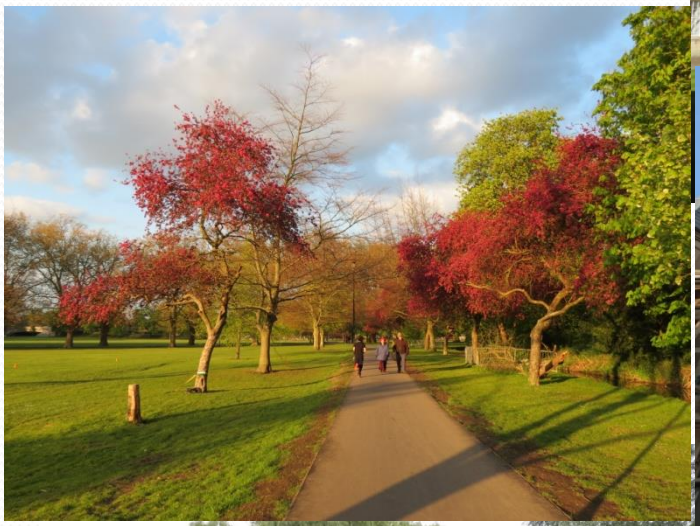


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Thank you! Questions?