

UVM-Based RTL Verification – ARM SSG

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ARM Holdings– Cambridge - UK

ARM[®]

Summary

- **Short Bio**
- **ARM Holdings**
- **RTL Verification**
- **UVM Methodology**
- **Verification Flow and Tools**
- **Cambridge, England**

Short Bio

- **Education**

- Bachelor's Degree in Computer Science at PUCRS, Campus II (Uruguaiana-RS, Brazil) – 2000
- M.Sc. in Computer Science at PUCRS (Porto Alegre-RS, Brazil) – 2002
- Ph.D. in Computer Science at UFRGS (Porto Alegre-RS, Brazil) – 2007
 - Sandwich doctorate at Technische Universität Darmstadt (Germany) – 2005

Short Bio

- **Work Experience**

- Freelancer (Telecom) – GAPH PUCRS / PARKS S.A. (2000 - 2002)
- Freelancer (Telecom) – Datum TI / Digital S.A. (01/2003 – 04/2003)
- Freelancer (RFID) – GSE PUCRS (2006 - 2007)
- Assistant Teacher, Unisinos University, São Leopoldo-RS, Brazil (2007-2009)
- IC Verification Engineer, CEITEC, Porto Alegre, Brazil (2007 - 2015)
- Senior Verification Engineer, ARM, Cambridge, UK (2015 - current)

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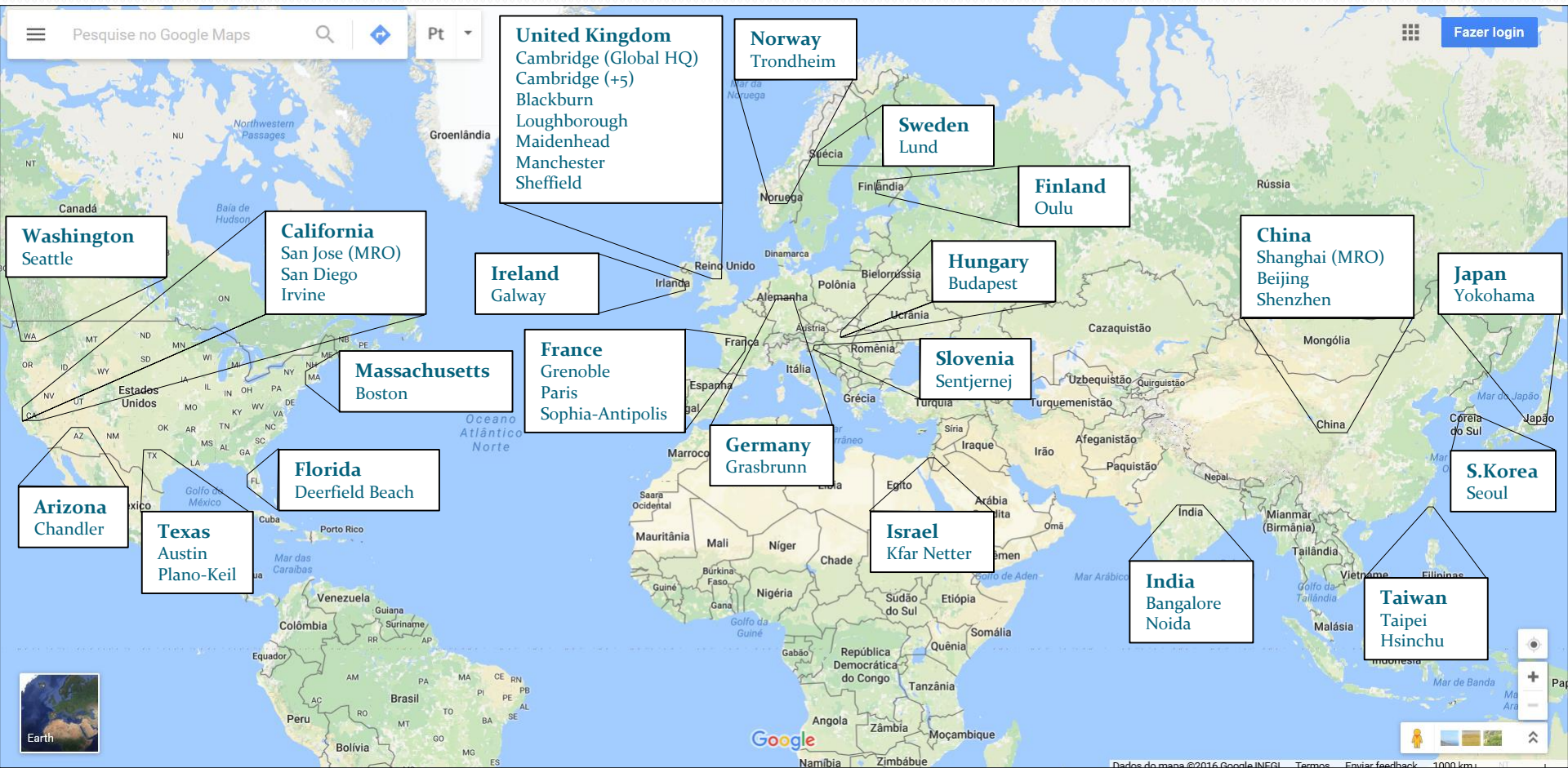
ARM Holdings

- The world's leading semiconductor IP company founded in 1990 (26 years)
- Acorn RISC Machine (1983) -> Advanced RISC Machines (1990)
- ARM technologies reach 80% of the global population
- More than 4,200 people from 61 nationalities
- Nearly four billion ARM technology-based chips shipped every quarter

ARM Holdings

- More than 86 billion ARM-based chips shipped to date (14.9bn 2015 and 12.1bn in 2014)
- 95% of smartphone market; 85% of mobile devices (smartphones, tablets, laptops)
- 1,379 licenses sold to more than 450 partners
- Joined SoftBank Group Corp in 2016 (at a price of £24 billion)

ARM Offices



ARM Engineering Groups

Architecture and Technology

CPU

Development Solutions

Business Lines

Internet of Things (IoT)

Media Processing

Partner Enablement

Physical IP Design

Project Management

Research

Systems and Software

Technical Operations

Wireless Business Unit

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RTL Functional Verification

- Ensures that the design is logically correct
- Functionality is fully implemented and working as expected (matches the specification)
- Types of Functional Verification:
 - Formal Verification
 - Simulation-Based Verification

Formal Verification

Jasper Gold

- No input vectors
- Assertion-based
- Assumptions
- Statistic models
- Suitable for blocks, not for systems



- Very useful when developing Protocol Checkers

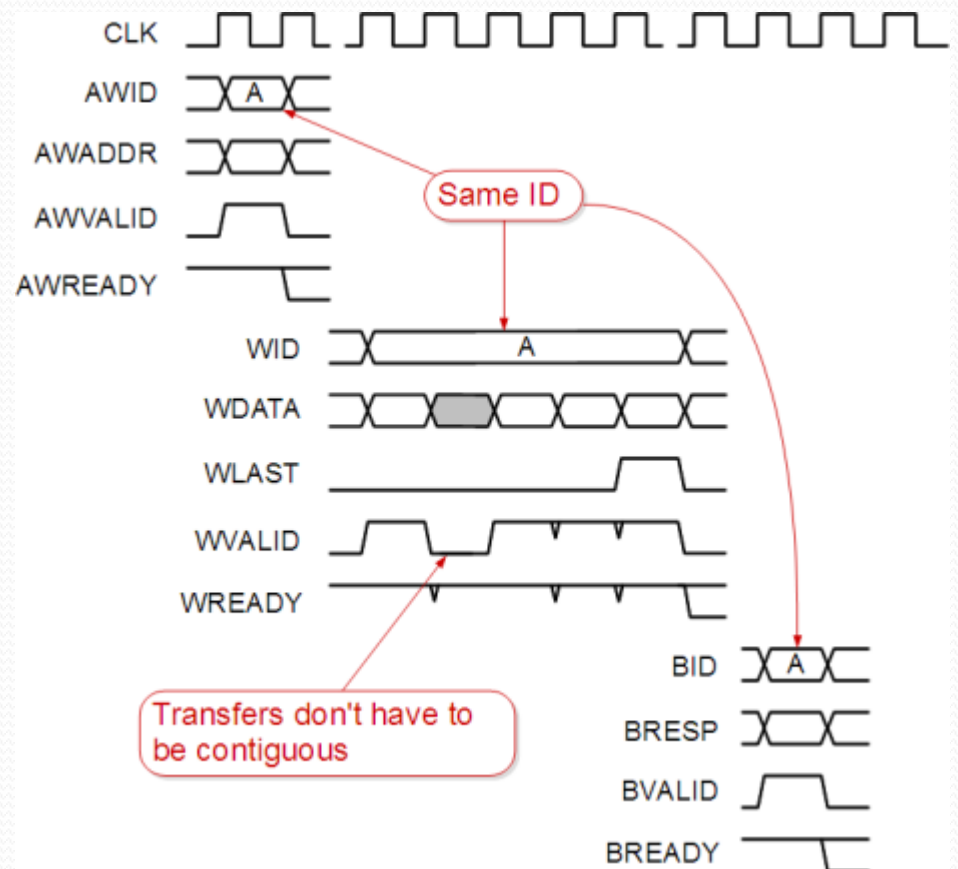
ID	POI	Type	Classification	Proof Status	Definition
50	18	assert	unclassified	cx	jasper_stuck_atready3.1'b0
51	18	assu...	unclassified	unprocessed	jasper_equal(eg_ready, wr_rdl)
55	11	assert	unclassified	✓ proven	\$onehot0((p_selint_read_done0, p_selint_read_done1, p_selint_read_done2, p_selint_read_done3))
56	11	cover	unclassified	✗ partial_u...	jasper_reachable_states((p_selint_read_done0, p_selint_read_done1, p_selint_read_done2, p_selint_read_done3), {1-2, 4})
59	12	assert	unclassified	✓ proven	\$onehot0((p_selnew_tran0, p_selnew_tran1, p_selnew_tran2, p_selnew_tran3))
60	12	cover	unclassified	✓ covered	jasper_reachable_states((p_selnew_tran0, p_selnew_tran1, p_selnew_tran2, p_selnew_tran3), 1-2)
63	13	assert	certified	✓ proven	\$onehot0((p_selint_ready0, p_selint_ready1, p_selint_ready2, p_selint_ready3))
64	13	cover	unclassified	✓ covered	jasper_reachable_states((p_selint_ready0, p_selint_ready1, p_selint_ready2, p_selint_ready3), 1-2)
66	16	assert	certified	cx	\$onehot0(arb_gnt)
67	16	cover	uncertain	✗ partial_u...	jasper_reachable_states(arb_gnt, {4, 8})

```
[<embedded>] % syn_bp -silent -set_class certified (65)
[<embedded>] % syn_bp -silent -set_class uncertain (67)
[<embedded>] % syn_bp -silent -set_class certified (63)
[<embedded>] % syn_bp -silent -set_class dont_care (63)
[<embedded>] %
```

assume in_1 != in_2
...
assert out_1 > out_2
...

Protocol Checker

- Ex: Amba 4
 - More than 50 signals
 - Set of rules for data transfer
- Protocol Checker
 - SV Module
 - Auxiliary logic
 - Assertions



Simulation-Based Verification

- Input vectors
- Output checkers
- Direct tests
 - Easy to cover some specific conditions
- Random tests
 - Random constraints
 - Functional coverage to ensure specific conditions are covered
- UVM – Universal Verification Methodology

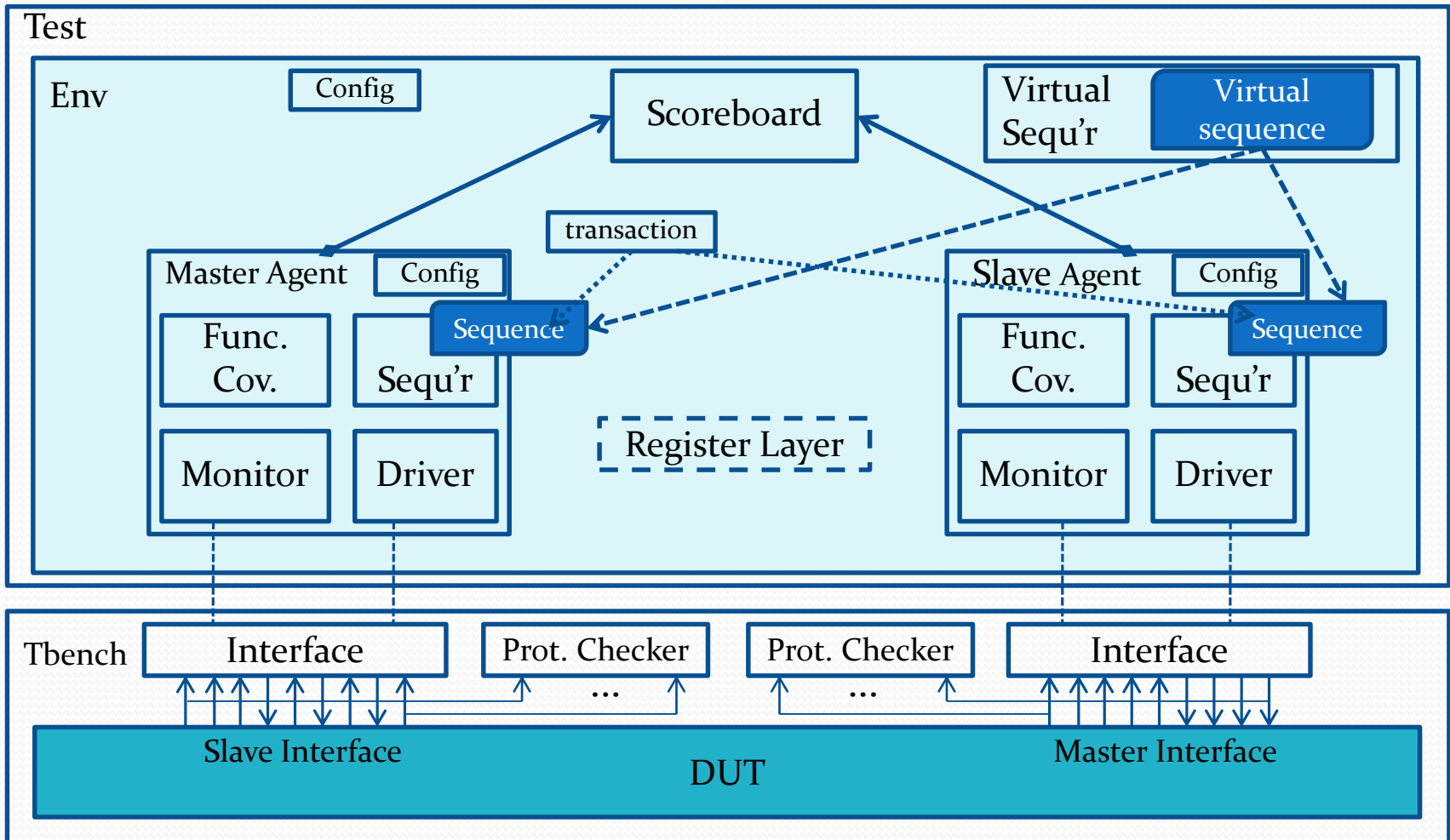
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UVM – Universal Verification Methodology

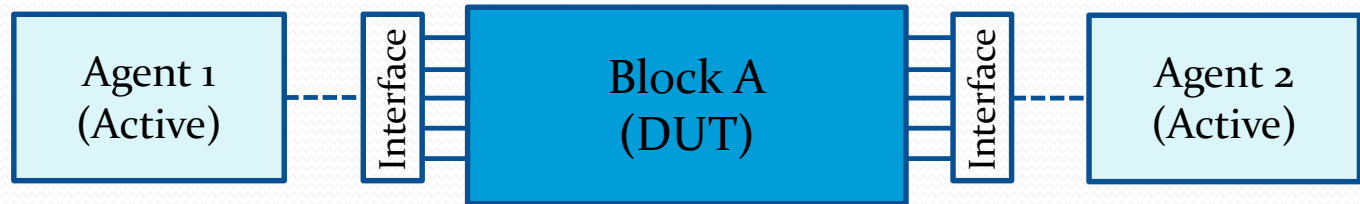
- Standardized methodology derived mainly from the OVM (Open Verification Methodology) aiming the reuse of components
- Brings automation to the SystemVerilog: sequences and data automation features (packing, copy, compare) etc.
- Support from multiple vendors: Aldec, Cadence, Mentor, and Synopsys
- Standard hierarchy, structures, configurations, connections makes easier the understanding and the reuse of components

Simulation-Based Verification Using UVM

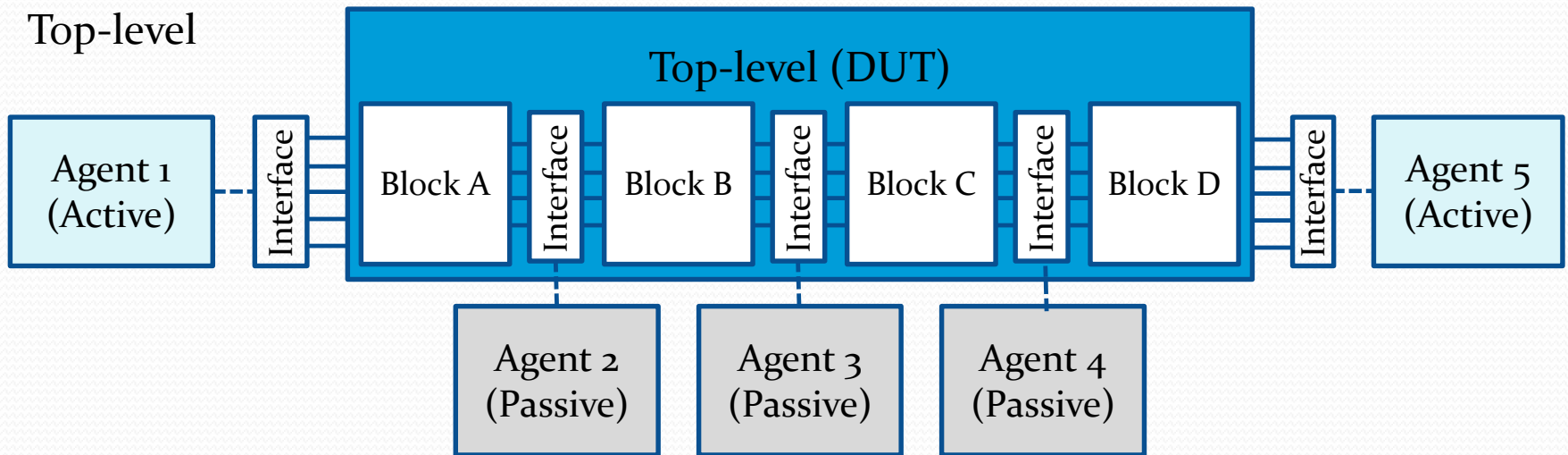


Simulation-Based Verification

Unit

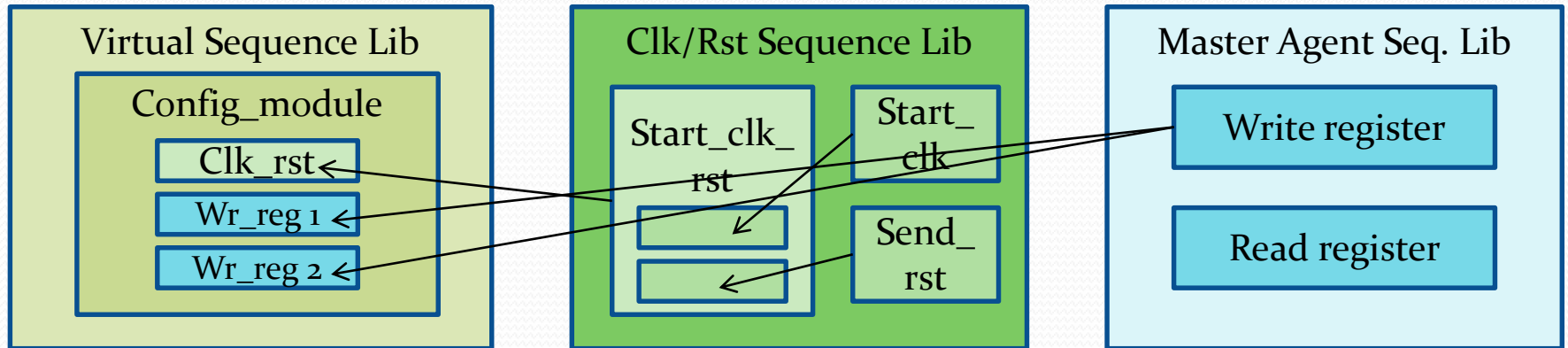


Top-level



For functional coverage and to feed scoreboards

UVM Sequences



Test 1

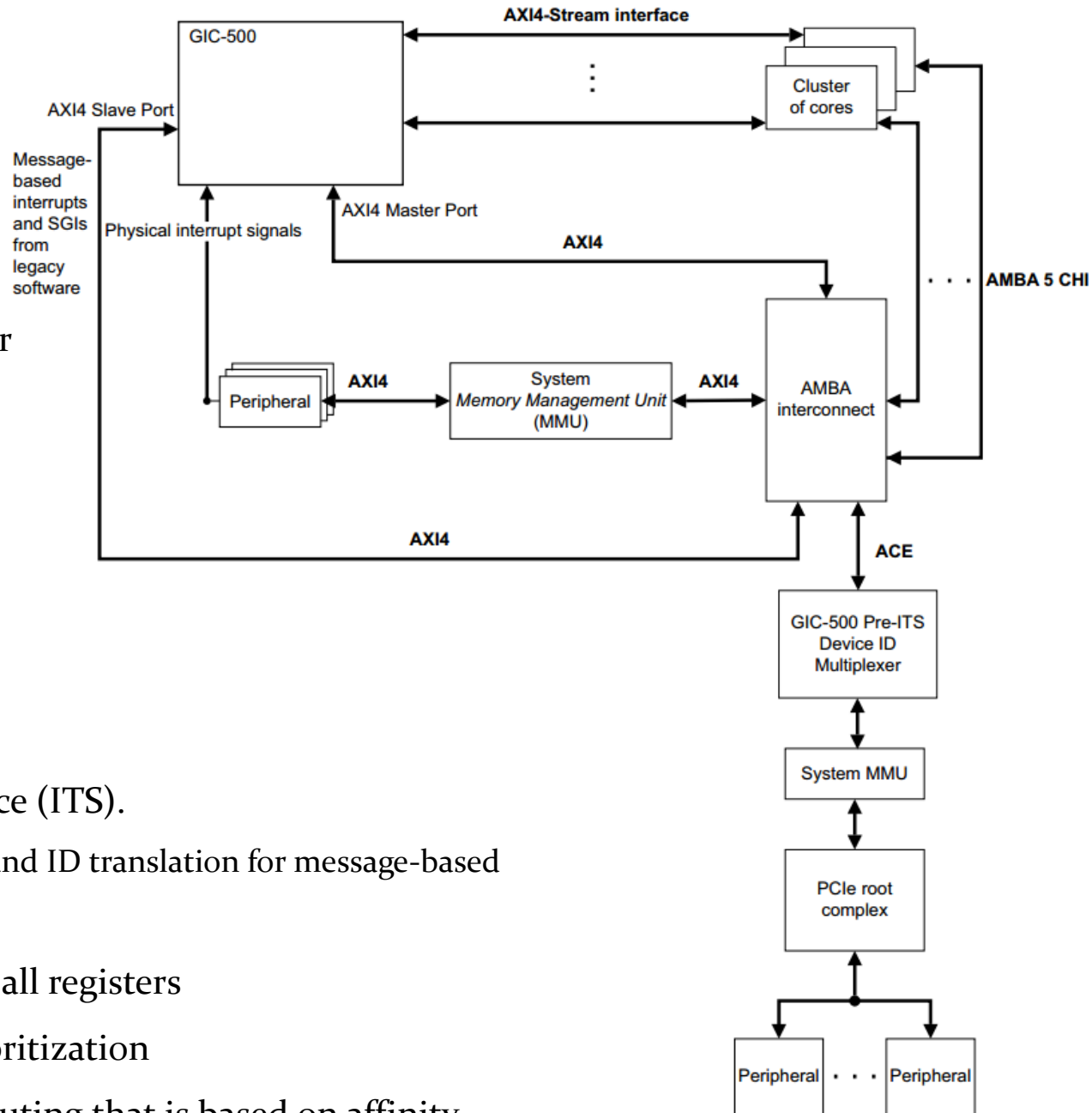
```
...  
virtual_seqr.start (config_module)  
...  
master_seqr.start(write_reg)  
...  
err_inject_seqr.start(inject_err)
```

Test 2

```
...  
slave_seq.start(reactive_sequence)  
...  
virtual_seqr.start (config_module)  
...  
master_seqr.start(read_reg)
```

Ex:GIC500

- Configurable int. Controller
- Compatibility: ARMv8 (ex: Cortex-A53, Cortex-A57)
- Up to 128 cores
- Up to 32 affinity-level 1 clusters
- Up to 8 cores per cluster
- Interrupt Translation Service (ITS).
 - provides device isolation and ID translation for message-based interrupts
- Memory-mapped access to all registers
- Interrupt masking and prioritization
- Programmable interrupt routing that is based on affinity



GIC 500 Interrupt Types

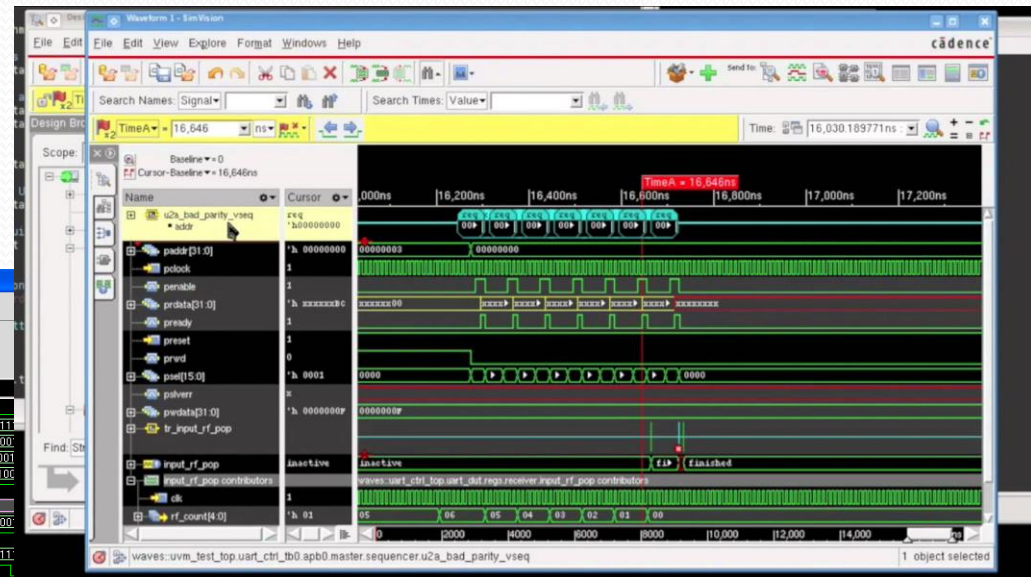
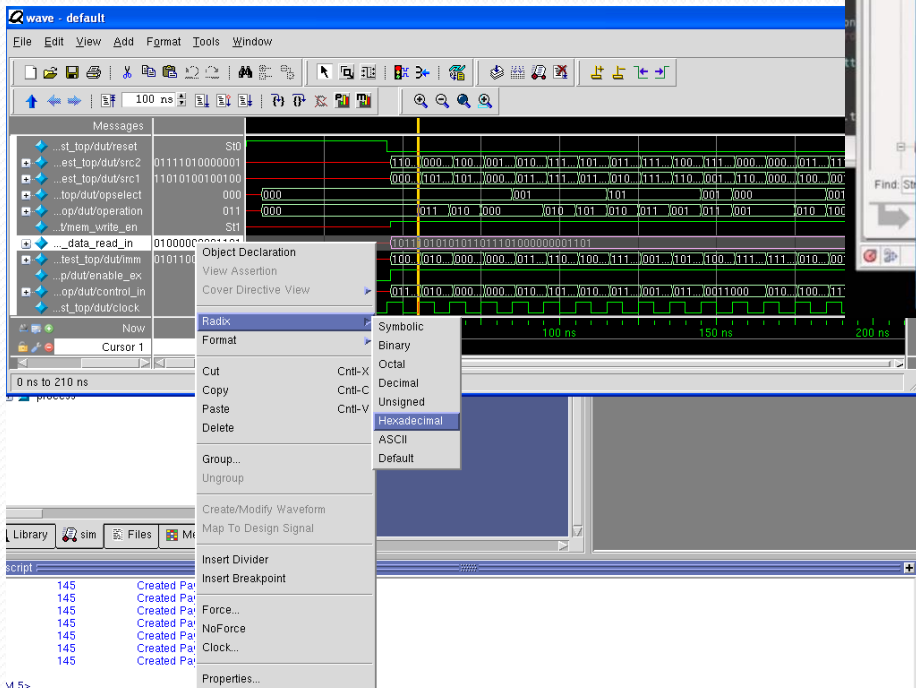
- **Locality-Specific Peripheral Interrupts (LPIs)**
 - Message-based interrupt
 - Generated by a peripheral writing to a memory-mapped register
 - Target only one core at a given time
- **Shared Peripheral Interrupts (SPIs)**
 - Used for peripherals that are not tightly coupled to a specific core
 - Configurable: 32 to 960
 - Generated by wires of writes to AXI4 slave port
- **Private Peripheral Interrupts (PPIs)**
 - Independent for each core and can be programmed to support either edge-triggered or level-sensitive interrupts
 - Used for peripherals that are tightly coupled to a particular core
- **Software Generated Interrupts (SGIs)**
 - Inter-processor interrupts, that is, interrupts generated from one core and sent to other cores
 - Generated through register write

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Simulation Tools

Mentor Modelsim/Questasim (MTI)



Cadence NCSim

GIT - Version Control System

The screenshot displays the Git GUI interface for a repository named 'libgit2'. The top-left pane shows a commit graph with the current commit highlighted in green. The top-right pane lists recent commits with their authors and timestamps. The middle section shows the SHA1 ID and search options. The bottom-left pane displays commit metadata, including the author, committer, parent, and child commit hashes. The bottom-right pane shows a diff view of the file 'tests/diff/submodules.c'.

Local uncommitted changes, not checked in to index
development remotes/origin/development refspec: git_refspec_parse() does not e
Merge pull request #2208 from libgit2/vmg/mempack
In-memory packing backend
Merge pull request #2226 from libgit2/rb/submodule-sorting-fix
Improve test of submodule name sorting
Cleanups
Fix submodule sorting in workdir iterator
Add faster git_submodule_is_submodule check
Merge pull request #2229 from linquize/Wdeclaration-after-statement
Add CFLAGS -Wdeclaration-after-statement

SHA1 ID: b76b5d34275fe33192358d4eaa1ae98e31efc2a1 Row 6 / 1359

Find commit containing: Exact All fields

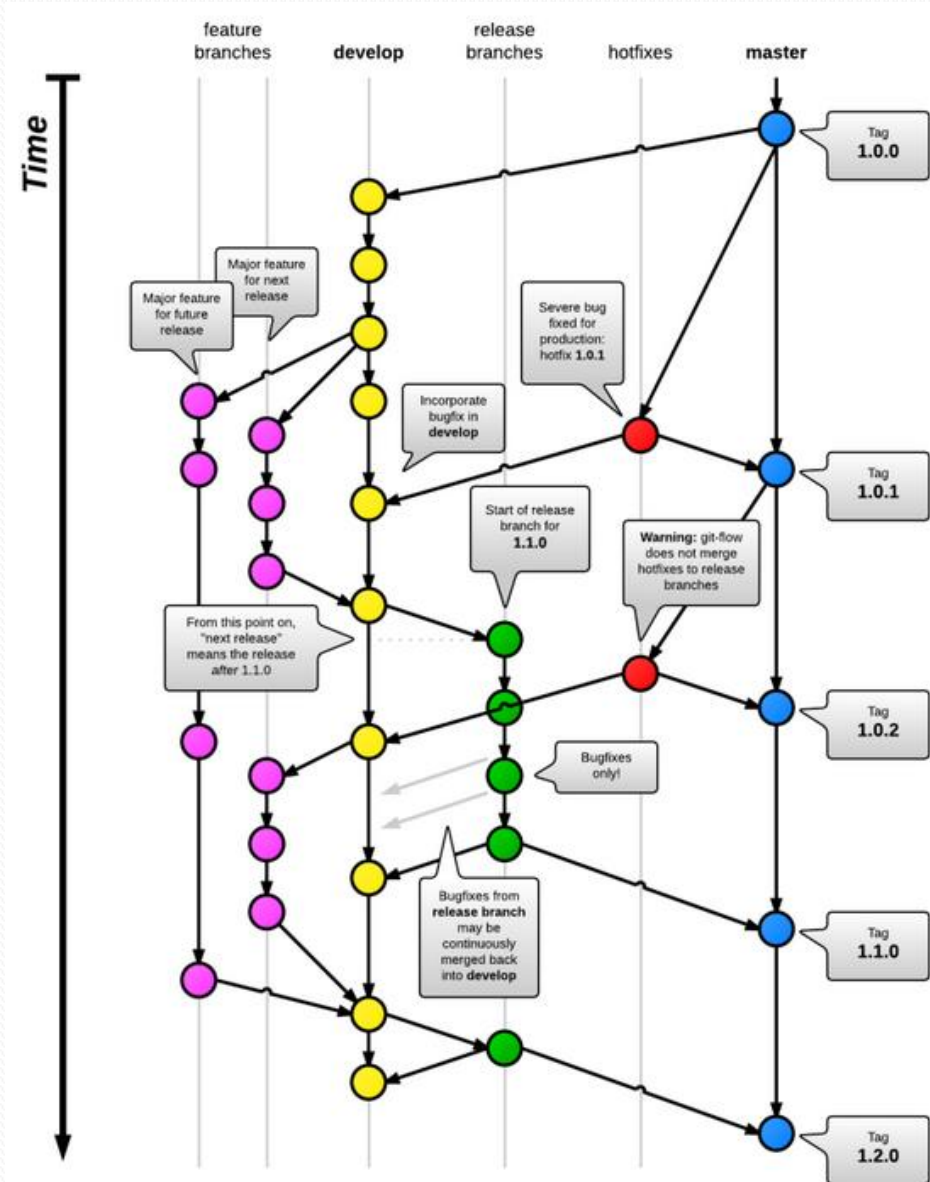
Diff Old version New version Lines of context: 3 Ignore space change Line diff

Author: Russell Belfer <rb@github.com> 2014-03-31 13:33:11
Committer: Russell Belfer <rb@github.com> 2014-03-31 13:33:11
Parent: 7dcd42a55f5fdc61e8e8de472ec54ccc0613e23c (Cleanups)
Child: d67397dd0c82fab82a1e6883107c97c4e133a911 (Merge pull request #2226 from libgit2/rb)
Branches: development, remotes/origin/development
Follows: v0.20.0
Precedes:

Improve test of submodule name sorting

```
index ead5c71..2881f74 100644
@@ -182,6 +182,8 @@ void test_diff_submodules__submod2_index_to_wd(void)
    "<UNTRACKED>", /* not */
    "diff --git a/sm_changed_file b/sm_changed_file\nindex 4800958..4800958 :
    "diff --git a/sm_changed_head b/sm_changed_head\nindex 4800958..3d9386c :
+    "<UNTRACKED>", /* sm_changed_head- */
+    "<UNTRACKED>", /* sm_changed_head_ */
    "diff --git a/sm_changed_index b/sm_changed_index\nindex 4800958..480095:
    "diff --git a/sm_changed_untracked_file b/sm_changed_untracked_file\nind:
    "diff --git a/sm_missing_commits b/sm_missing_commits\nindex 4800958..5e:
@@ -190,6 +192,10 @@ void test_diff_submodules__submod2_index_to_wd(void)
```


GIT Flow



JIRA – Issue and Project Tracking

JIRA Gantt Charts

ACTIVE FILTERS: 1 Projects x 3

Status: Not Started (1), In Progress (2), Completed (3)

Weeks: 14, 9 February, 16 F, 3 February, 2 March, 9 Ma

Week days: 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 1, 2, 3, 4, 5, 6

Example Project	Assignee
EP-8- Completed-Story	Adrian 'Adl' Wi...
EP-9- subtask no. 1	Adrian 'Adl' Wi...
EP-7- Completed task	Adrian 'Adl' Wi...
EP-1- Example-Bug-#6	Adrian 'Adl' Wi...
EP-2- Bug #2	User with a Lon...
EP-3- Long Story Short	Adrian 'Adl' Wi...
EP-5- No estimate	Adrian 'Adl' Wi...
EP-4- Story Subtask with...	Pospopy Zrivar...
EP-6- Another bug with a...	Adrian 'Adl' Wi...
EP-10- Long Story	Adrian 'Adl' Wi...
EP-11- 1st Task	Adrian 'Adl' Wi...
EP-12- 2nd Task	Adrian 'Adl' Wi...
2nd Generation Module	Assignees
NM-1: Gather requiremen...	Adrian 'Adl' Wi...
NM-2: Create project's ...	Adrian 'Adl' Wi...
NM-3: Implement 1st coo...	Adrian 'Adl' Wi...
NM-4: backend developme...	Adrian 'Adl' Wi...
NM-5: Create API	Adrian 'Adl' Wi...

JIRA Dashboard

New

Two Dimensional Filter Statistics by Assignee

Status	Admin Istrator	Atvmlyyh Uottoson	Dzoqrifs Ubbbigyih
OPEN	7	4	3
IN PROGRESS	16	14	10
REOPENED	9	11	10
RESOLVED	34	22	19
CLOSED	20	19	18
Total Unique Issues:	111	110	91

Showing 5 of 10 statistics. Show more
Filtered by: All issues

Created vs Resolved Chart: cinerea

Issues in the last 365 days (grouped weekly) View in Issue Navigator

- Created issues (112)
- Resolved issues (107)

Pie Chart: All Issues

Assignee	Total Issues
Kqkgufg Phygusqc	113
Admin Istrator	111

Issue Statistics: All Issues (Priority)

Priority	Count	Percentage
Blocker	2	9%
Critical	6	26%
Major	5	22%
Minor	4	17%
Trivial	6	26%
Total	23	

Filter Results: All Issues

T	Key	P	Summary
3	TMBI-121	↑	Messiest gratuity's convalescents aloft Arway's
7	TMBI-120	↑	Passageway's prefab's clunk begone brainchild's vireo commentator's plover
5	TMBI-119	↓	Ptomaine hences attentions blacked diocese grimed brazier's hippopotami
6	TMBI-118	↑	TMBI-116 / Pineapple Frobisher's buzzers raisins clothing
6	TMBI-117	↓	TMBI-116 / Majesties Carissa Sammy mooting lonesomes bourgeois

1-5 of 600 1 2 3 4 5 6 7 8 9 ▶

Assigned to Me

T	Key	P	Summary
6	GGIS-9	↑	GGIS-7 / Satined snot greyhound's demolish Savonarola's naphthalene's premium's Humberto's earache's
8	LICS-41	↑	Handball's cued ruggedly bacchanalians resonance occasions resonators uncompromising
2	CNEA-90	↑	Redolence silencers fortifications payload's demolitions Chicagoan comports Kristine Gregory dockyard
2	GGIS-4	↓	Hypnotism incinerating jasper's zip's equipage's Glass Lester's trollops enchanting coxswains

Typical Bug Workflow

Assigned to Verification

Description + config + version +
instructions to reproduce

Resolved

Comments

Closed

Assigned to Design

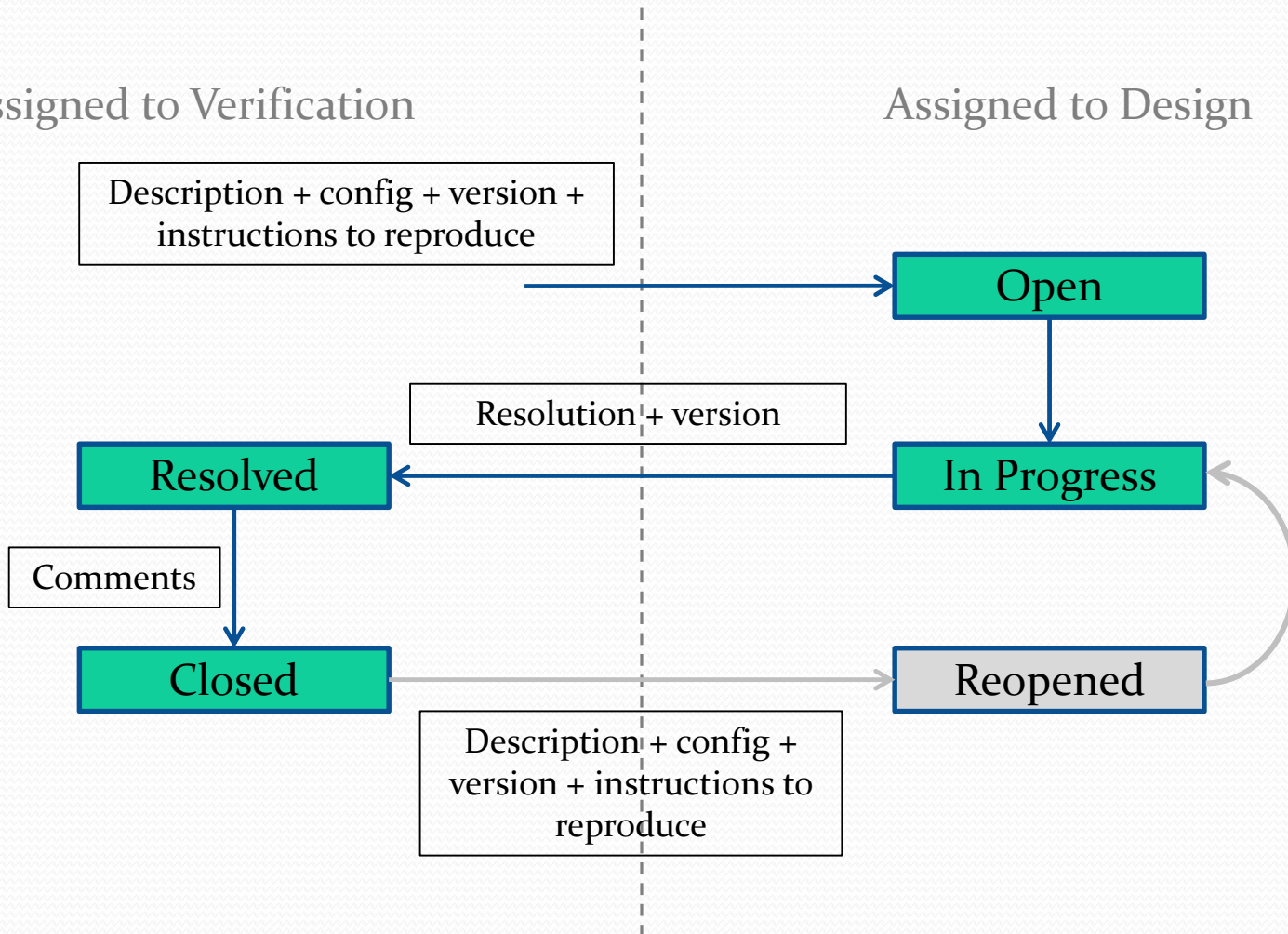
Open

In Progress

Reopened

Resolution + version

Description + config +
version + instructions to
reproduce



Bamboo

- Continuous Integration Server
 - Automated builds and tests
 - Regression reports

The screenshot displays the Bamboo web interface for a plan named 'Atlassian Cache Sandbox' (Core (SVN)). The current activity shows a manual build by Sarah Goff-Dupont, which is currently building for 27 seconds. The recent history table lists several builds, with the most recent (#30) being a manual build by Sarah Goff-Dupont that passed 326 tests 19 hours ago. The plan statistics indicate 28 builds, 67% successful, and an average duration of 54s. The branches section shows several branches, including 'Atlassian Core 3.10' and 'Atlassian Core 4.5.x'. A blue arrow points from the 'Changes by Steven Desalas' box at the bottom left to the '#21' build entry in the recent history table.

Build #	Build Name	Author	Time	Status
#30	Manual build by Sarah Goff-Dupont	Sarah Goff-Dupont	19 hours ago	326 passed
#29	Manual build by Sarah Goff-Dupont	Sarah Goff-Dupont	19 hours ago	326 passed
#28	Manual build by Sarah Goff-Dupont	Sarah Goff-Dupont	2 days ago	326 passed
#27	Manual build by Sarah Goff-Dupont	Sarah Goff-Dupont	2 weeks ago	Testless build
#26	Manual build by Sarah Goff-Dupont	Sarah Goff-Dupont	2 weeks ago	Testless build
#25	Manual build by Sarah Goff-Dupont	Sarah Goff-Dupont	2 weeks ago	326 passed
#24	Manual build by Sarah Goff-Dupont	Sarah Goff-Dupont	3 weeks ago	Testless build
#23	Manual build by Sarah Goff-Dupont	Sarah Goff-Dupont	1 month ago	14 passed
#22	Dependant of CACHE-DEPL-27	Sarah Goff-Dupont	1 month ago	14 passed
#21	Manual build by Paige N. Spector [QA]	Paige N. Spector [QA]	1 month ago	14 passed

✓ #53	Changes by Steven Desalas	5 days ago
✓ #52	Changes by Steven Desalas	5 days ago

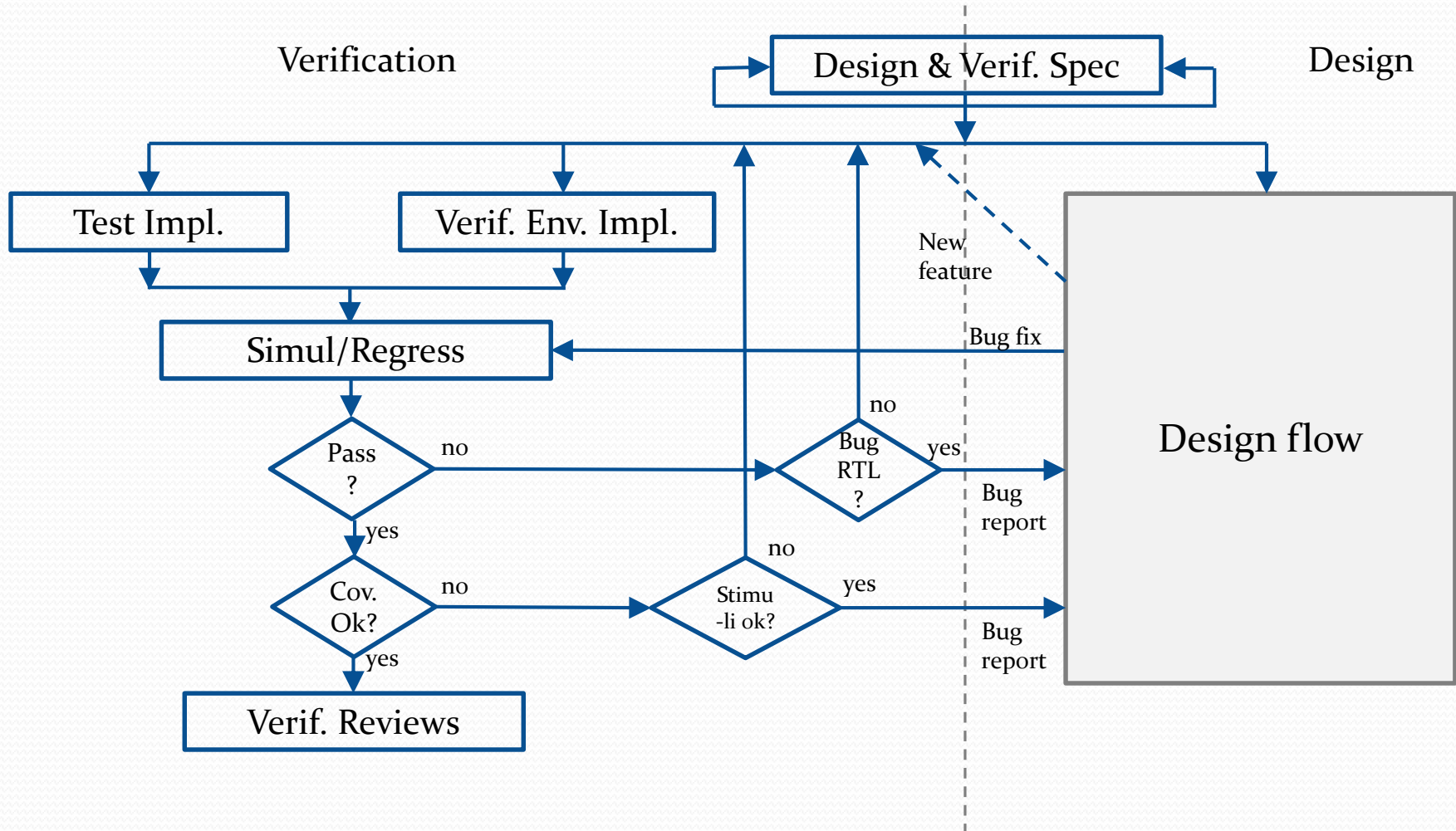
Verification Metrics

- Measures the quality of verification
- Necessary to define the end of verification process
- Code coverage
 - Statements, branches, toggle, FSMs
- Functional coverage
 - % of functionality verified (sequences, cross, states combined to inputs/outputs)
- Pass rate
 - % Success/Fail
- Different (increasing) requirements per milestone

Design Milestones

- Alpha and Beta milestones are internal quality milestones.
- LAC (Limited Access) represents the milestone after which lead partners get access to the IP
- EAC (Early Access) represents the point after which the IP is ready to be fabricated for obtaining engineering samples and testing
- REL (Release): the IP has gone through rigorous testing and is ready for mass production.

RTL Verification Flow



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ARM HQ - Cambridge



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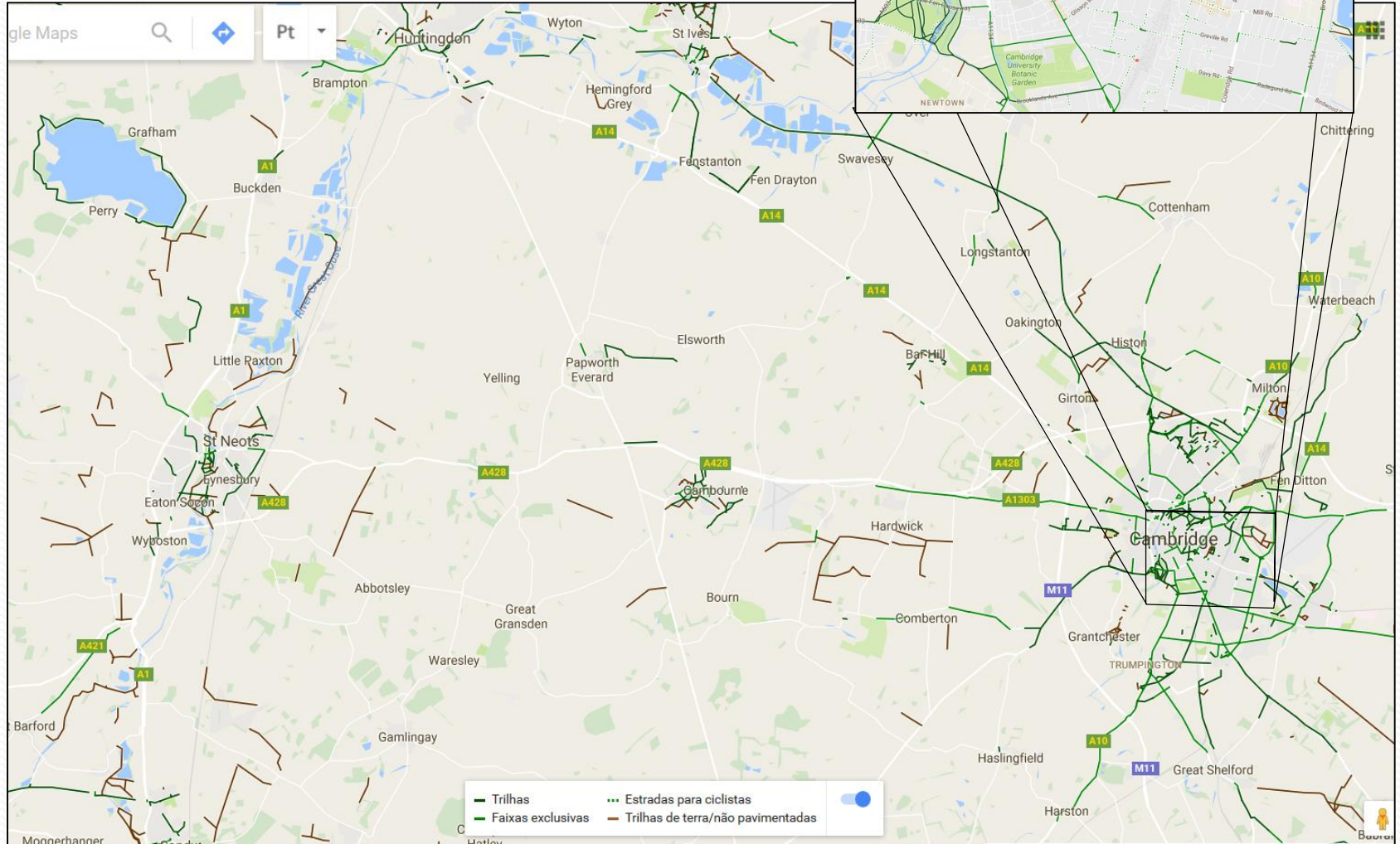
Cambridge



ARM HQ



Cambridge



Cambridge



The Tab's Map of Cam... 🔍 ☰

▼ The Tab aims to review all of Cambridge's Pubs, letting you know important things such as how much a pint costs, what the 6,550 views
[SHARE](#)

☑ **Untitled layer**

- ▼ **The Rad**
- 📌 The Salisbury Arms
- 📌 Cambridge Blue
- 📌 Alexandra Arms
- ... 117 more

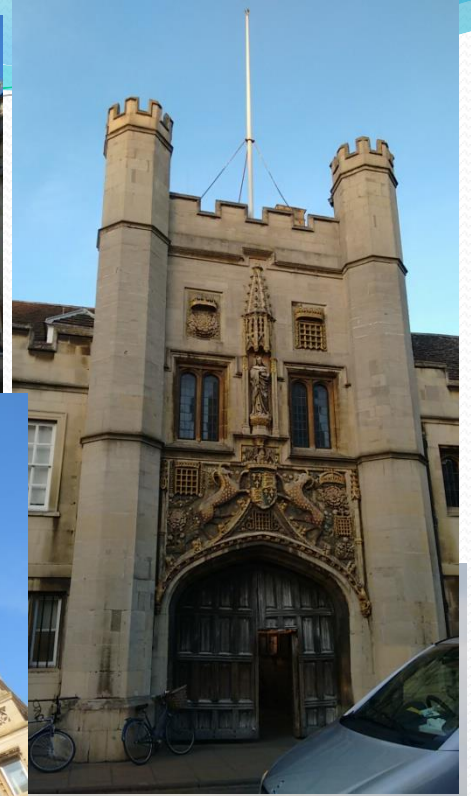
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Cambridge



Cambridge



More information

- Contact:
 - Jose.Santanna-Palma@arm.com
- Links
 - <http://www.arm.com/>
 - <https://developer.arm.com/products/system-ip/system-controllers/interrupt-controllers>

Thank you! Questions?