Comparative Analysis of Analog Controllers for DC-DC Buck Converter

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***Abstract*—This paper comprehensively describes analog controller design for DC-DC buck converter using the analogous classic controlling techniques. Different kinds of PID (proportional-integral-derivative) controllers, along with lead-lag, are examined and their simulations are analyzed using Simulink/MATLAB. The analysis is manifested in time as well as frequency domain and the converter dynamics are evaluated in state-space form as well as in transfer function form. Also, the effect of each controller design technique on system performance is simulated and discussed. The performance of all the types of PID controller is validated using the MATLAB/Simulink environment.**

***Index Terms*—PID controller, lead-lag controller, DC-DC buck converter, MATLAB/Simulink**

I. Introduction

Although thousands of methods and different algorithms have been generated related to high performance of the control systems, but the field is still challenging. A high performance control system design is significant. In the area of DC-DC power switching converter controlling techniques, PWM is considered as most reliable one as according to the linear models [1], [2], with PWM controller, the converter power stage remains effective up to one half level of the switching frequency. Controlling techniques using PWM are encouraged in many applications [3]. Another advantage offered by PWM is that it can be applied in both (voltage and current) modes; while current mode is preferable over the voltage mode because it offers dynamic simplification and also the inherent limitation. But, eventually, it depends on the control designer.

The proposed scheme designs an optimal control for the buck converter which is linearized. No hardware is in the scope of the paper. Rather, it covers system design optimization and its simulation. CAD tool [4] is used for the controller synthesis as it lets the designer to estimate the controller roughly prior to the actual design.

The PID is considered as the most substantial controller of the modern era. PID controllers like lead-lag, 1-DOF, 2-DOF and classical PIDs etc. are collated and investigated for low power and high frequency DC-DC buck converters. Statistics show that PID controllers are being used in more than 95% of the closed-loop industrial processing [5], [6]. All the controllers in the form of PID are assessed and compared performance-wise.

The paper is formulated in the following way: Section II of this paper models the buck converter system. Section III formulates the design for a lead-lag buck converter and compares its performance with other forms of PID controlling designs. Simulated results are simulated in section IV through MATLAB/Simulink environment and section V draws the conclusion.

II. Dynamic Model of the Buck Converter

Fig. 1 shows the switching of DC-DC buck converter and the feedback control circuit model. The power stage of the buck converter includes the parasitic resistances making the converter more realistic.

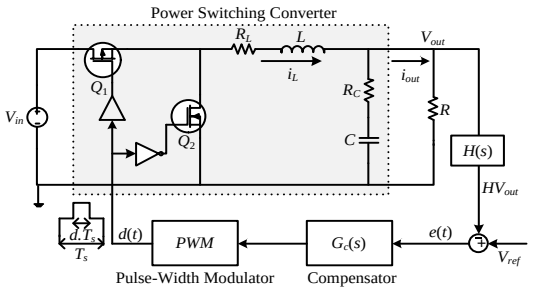

Figure 1. Buck converter power stage with feedback control loop.

The component values and the other parameters employed in this paper are tabulated in Table I.

TABLE I. Parametric Values for the Buck Converter

Symbol	Parameter	Value
L	Output Filter Inductor	4.7 µH
R_L	Series Resistance of Inductor	22 mΩ
C	Output Filter Capacitor	33 µF
R_C	Series Resistance of Capacitor	30 mΩ
R	Load Resistance	1 Ω
V_{in}	Input Voltage	5.0 V
V_{ref}	Reference Voltage	2.0 V
V_{out}	Output Voltage	2.0 V
f_s	Switching Frequency	500 kHz
T_s	Sampling Period	2 µs
PM	Phase Margin	> 50 °

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State-space representation of the proposed buck converter may be shown as below, taking all parasitic resistances into account as discussed in [7], [8];

$$\begin{aligned} \dot{\mathbf{x}} &= \mathbf{A}\mathbf{x} + \mathbf{B}u \\ y &= \mathbf{C}\mathbf{x} + \mathbf{D}u \end{aligned} \tag{1}$$

In the above equation control input is represented as u (the duty cycle), $\boldsymbol{x}$ represents the state vector, and y (the output voltage) is the measurement. The state vector $\mathbf{x}=[\mathbf{i_L} \quad \mathbf{v_C}]^{\mathrm{T}}$ represents the two state variables, namely the current flowing through the inductor (i_L) and the voltage across the capacitor (v_C).

$$\mathbf{A} = \begin{bmatrix} \frac{(R_C R + R_L R + R_L R_C)(-C)}{R_C + R} & -\frac{CR}{R + R_C} \\ \frac{LR}{R_C + R} & -\frac{L}{R_C + R} \end{bmatrix} \frac{1}{LC}$$

$$\mathbf{B} = \begin{bmatrix} V_{in}/L \\ 0 \end{bmatrix}; \quad \mathbf{C} = \begin{bmatrix} \frac{R_C R}{R_C + R} & \frac{R}{R_C + R} \end{bmatrix}; \quad \mathbf{D} = [0];$$

The state-space average technique as discussed gives a linearized control-to-output transfer function which is shown as below:

$$\left.\frac{\hat{v}_0(s)}{\hat{d}(s)}\right|_{\substack{\hat{v}_{in}(s)=0 \\ \hat{i}_{out}(s)=0}} = \left[\frac{as+1}{bs^2+cs+1}\right] V_{in} \tag{2}$$

where

$$a = CR_C$$

$$b = CL\left(\frac{R_C + R}{R_L + R}\right)$$

$$c = \left(C(R \parallel R_L) + R_C C + \frac{L}{R_L + R}\right)$$

Using the parameters given in Table I, obtaining the values of a, b and c and the transfer function in (2);

$$a = 9.9\times10^{-7}$$

$$b = 1.5637\times10^{-10}$$

$$c = 6.2962\times10^{-6}$$

$$G_p(s) = \left[\frac{4.95\times10^{-6}s + 5}{1.563\times10^{-10}s^2 + 6.299\times10^{-6}s + 1}\right] \tag{3}$$

Fig. 2 shows the Bode plot for the proposed system indicating a very small level of phase margin. This low phase margin of 24.9° at 1.95×10^5 rad/s is not enough to ensure better static and dynamic response. At low frequencies the gain should be high enough so that the steady-state error is minimized. Also, the gain crossover frequency should be high enough to meet an order of the magnitude which is below the switching frequency so that power supply responds to the transients as quickly as possible. To meet these two requirements, a compensator having a phase margin range of 45 to 60 degrees must be designed so that the required transient response is achieved [9].

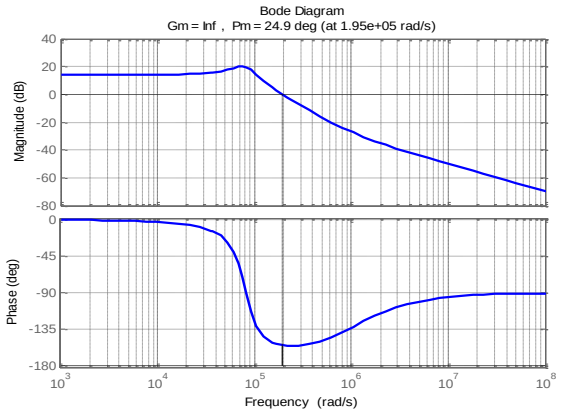

Figure 2. Bode plot of the uncompensated buck (plant) converter.

III. Control Design

Different controlling techniques, analog and classical, will be designed and compared in this section. Following requirements are needed to be satisfied by the controller for low-power and high-frequency SMPSs:

- Due to input DC voltage and sudden changes in the load current, disturbances in the output voltage occur. So, the controller must provide excellent line and load regulations so that the steady-state equilibrium is quickly obtained. Utilizing an output capacitor for the filtering purpose, power level optimization is achieved. This optimization is allowed only when there is a quick transient response. Also, due to high gain crossover frequency (high loop bandwidth), the controller responds faster to the input voltage and load current disturbances.
- The controller must give fewer ripples in the steady- state voltage (output). With respect to a constant reference point over a wide range of load variations, reduction in voltage deviation (steady-state) is needed. For this, the output voltage regulation should be tight. The constant reference value depends on the application of the targeted system. Its value can vary from few mili-volts (microprocessors) to several hundred volts (LCD monitors).
- The controller must ensure bounded output for the bounded input, i.e., closed-loop stability.
- The controller should provide adequate system robustness. To allow for the dynamic variations and modeling errors, system gains and phase margins should be sufficient.

Keeping in view the above characteristics that should be fulfilled by a compensator, various forms of the PID are being designed in the section. While designing the controllers, loop bandwidth is kept high.

A. Lead-Lag Controller

For the closed loops systems, lead-lag compensators are considered useful to shape the frequency response while the phase-lead compensators increase phase margins preventing the crossover frequency (0-dB) to

change drastically; hence improving the transient response. To decrease the high frequency gain which improves noise rejection (or augmented gain margin), phase-lag compensators are used. They also increase the low frequency gains to improve the disturbance rejection. Modification of phase and gain parameters for the open-loop frequency responses is done usually by cascading the lead compensators with the lag compensators [10]. These compensators (lead and lag) are quite similar to PID controllers in a way that the lead component of the controller behaves like a PD of PID and the lag acts as a PI controlling component.

The zero in the lag compensator is plotted almost one decade below the crossover point of the gain frequency as both zeros and poles , in lead and lag compensator, depend on 0-dB crossover point of the gain frequency. To fulfill the desired requirements for the steady-state error, the compensator gain is adjusted accordingly. Through poles/zeros adjustments and simulations on MATLAB/Simulink, for the system which is described in equation (3), we propose a lead-lag compensator as follows:

$$G_c(s) = \underbrace{33.4}_{K_c} \cdot \underbrace{\frac{\left(\frac{s}{3.1416\times10^{4}}+1\right)}{\left(\frac{s}{1.1810\times10^{3}}+1\right)}}_{Lag} \cdot \underbrace{\frac{\left(\frac{s}{1.2375\times10^{5}}+1\right)}{\left(\frac{s}{7.9754\times10^{5}}+1\right)}}_{Lead} \quad (4)$$

Fig. 3 shows the Bode for the proposed lead-lag compensator which is a controller having two poles and two zeros. The diagram clearly depicts an improvement in the bandwidth of the system as well as its phase margin which is 68 ° at 3.51×10^{5} rad/s gain crossover frequency. The phase margin has improved a lot resulting in improving the transient response. The compensator provides a boost in phase around the vicinity where there is dip in phase curve of the uncompensated buck converter.

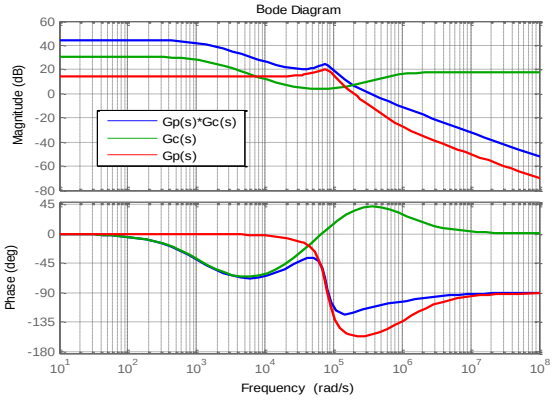

Figure 3. Bode plot of $G_p(s)$, $G_c(s)$ and $G_p(s)$*$G_c(s)$ in case of lead-lag compensator.

B. Conventional PID Controller

Following transfer function describes a PID controller which is designed to reach the desired phase margin, settling time and the maximum overshoot:

$$G_c(t) = K_i \int e(t)dt + K_d \frac{de(t)}{dt} + K_p e(t) \quad (5)$$

Or

$$G_c(s) = K_d s + \frac{K_i}{s} + K_p \quad (6)$$

where the derivative gain with K_d, proportional gain is represented by K_p and integral gain with K_i. The proposed controller has one pole and two zeros configuration. The main purpose of the design is to improve the phase margin which, in return, improves the transient response. The transfer function for the controller is given in (7) which are obtained after several iterations done on MATLAB using the SISO Designing Tool.

$$G_c(s) = 2.3775\times10^{-4} s + \frac{9.4637\times10^{5}}{s} + 30 \quad (7)$$

The Bode plot of the PID compensator shown in Fig. 4 depicts an improvement in phase margin. The improved phase margin ensures adequate set-point tracking and improved transient response.

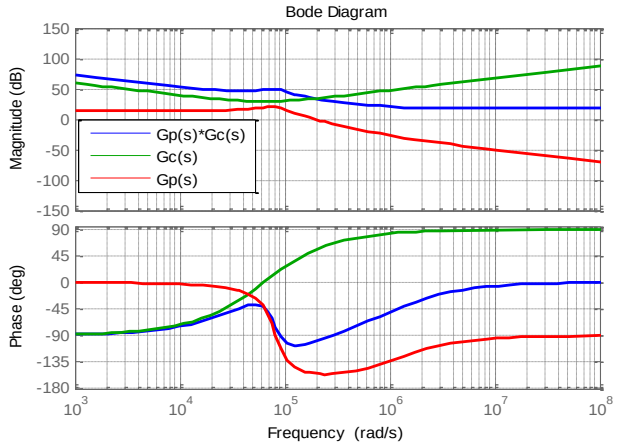

Figure 4. Bode plot of $G_p(s)$, $G_c(s)$ and $G_p(s)$*$G_c(s)$ in case of conventional PID controller.

C. Parallel PID Controller (1-DOF)

In 1-DOF (one-degree-of-freedom) parallel PID controllers, control actions (proportional, integral, and derivative) are weighted according to the gain parameters (*P*, *I* and *D*) independently and their sum is the output of the controller. Transfer function for a continuous-time and parallel controller (PID) is:

$$G_c(s) = \left[I\left(\frac{1}{s}\right) + P + D\left(\frac{Ns}{s+N}\right) \right] \quad (8)$$

where N is the filter coefficient which determines location of the pole in the derivative mode. Using SISO Designing Tool or the Simulink toolbox for the Control Design, the controller can be tuned to get the desired response. These tools first linearize the plant but there is no need of linearization in our case as it is already linearized. This algorithm chooses a bandwidth to achieve a balance between performance and robustness which is based on the open-loop frequency response. Hence, an initial controller is designed. Using the Tuner Interface for PID controller, when one of the factors (response time, phase margin or the bandwidth) the

proposed algorithm calculates the new gains. We compute the following gains:

$$I = 1.78\times10^{4}, P = 0.895, D = 9.22\times10^{-6}, N = 3.7313\times10^{5}$$

D. Parallel PID Controller (2-DOF)

For a control system, number of independently adjustable transfer functions (closed-loop) [11] is defined as its degree of freedom.

The real concerns related to a feedback controller are rejection disturbances and the fast, well-damped, response with a step change in its set-point. Aim of 2-DOF (two-degrees-of-freedom) formulation is to try to meet these objectives by providing an additional flexibility. Fig. 5 shows the block diagram of this 2-DOF controller.

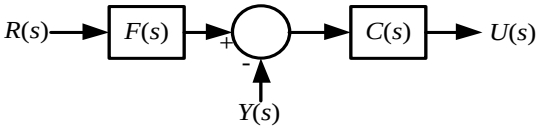

Figure 5. Block diagram of 2-DOF PID controller with set-point filter.

In the model given in Fig. 5, reference signal is represented by $R(s)$ whereas $Y(s)$ is the feedback from the output and $F(s)$ is a pre-filter acting on $R(s)$ and $C(s)$ is the 1-DOF controller.

The transfer functions $F(s)$ and $C(s)$ for the parallel 2-DOF PID controller are given as:

$$F(s) = \frac{(bPN + I)s + IN + (bP + cDN)s^2}{(PN + I)s + IN + (P + DN)s^2} \quad (9)$$

$$C(s) = \frac{(P + DN)s^2 + (PN + I)s + IN}{s(s + N)} \quad (10)$$

In Fig. 5, a filter is inserted in the controller's set-point path so it is called a set point filter type PID controller. The basic operational parameters P, I and D and the set-point weight values, called 2-DOF values/parameters, are b and c. These parameters are called proportional (b) and derivative (c) set-point weight values. In the control action, when we set b = 0, it eliminates its proportional action on $R(s)$. Elimination of the proportional function helps in reducing the maximum overshoot when there is a step change in the set-point weight values. And if we set c = 0, the derivative action is eliminated on the reference signal ($R(s)$) but it remains active on measured system response. Hence, without an extra transient response, we get a controller which achieves an effective disturbance rejection and also the set-point tracking is smooth. So, to reduce 2-DOF to 1-DOF, we set b = 0 and c = 0.

As an alternative Fig. 6 shows the block diagram of a 2-DOF PID controller where feed-forward acting on $R(s)$ is $Q(s)$, and may be given as:

$$Q(s) = \frac{(b-1)PN + (P(b-1) + DN(c-1))s}{(s + N)} \quad (11)$$

The realization shown in (11) is called as feed-forward type as, from $Y(s)$, a feed-forward path is added to $U(s)$ and to the controller.

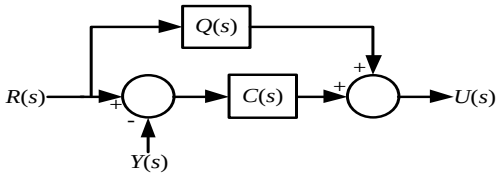

Figure 6. Block diagram for 2-DOF feed-forward PID controller.

IV. Results

Simulating the results through MATLAB/Simulink fixing 2 ms simulation time for a fixed load, Figs. 7 through 10 show the performance of various controller devices. The underdamped response for output voltage offered by the lead-lag compensated DC–DC buck converter can be observed in Fig. 7 which acquires 5% settling time in 80 μs and 18% overshoot. Comparing with other PID controllers, the proposed controller offers less overshoot but has almost the settling time. The output voltage response offered by 1-DOF and 2-DOF PID controllers is also shown in Fig. 7 to facilitate the comparison of all controllers.

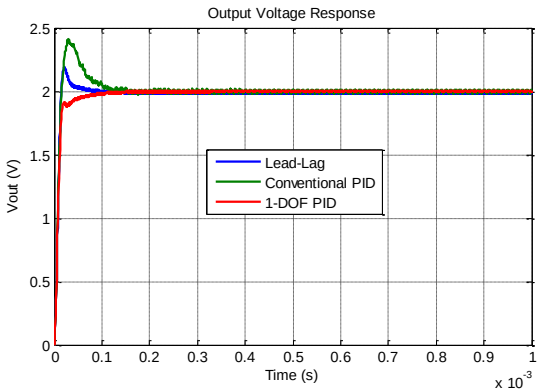

Figure 7. Output voltage response using three controllers (fixed load).

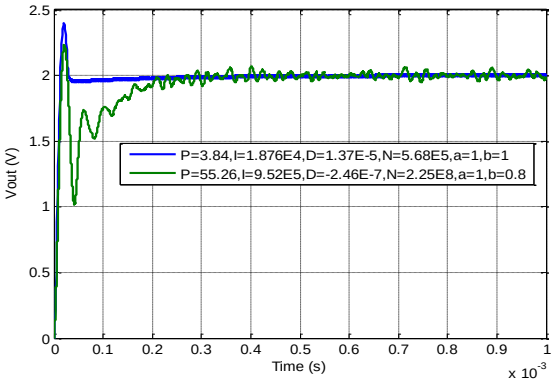

Figure 8. Output voltage response for differents parameters of a 2-DOF PID.

Observing Fig. 8 which shows the output voltage response of 2-DOF PID controller, it can be examined that how derivative and proportional weight values affect the system performance while keeping these values (b and c) in the range of 0 and 1. The controller designer has to compromise between the two factors i.e. maximum overshoot and the settling time as improvement in one

factor will cause deterioration in other. For instance, if we set the set-point values (b, c) to be (1, 0.8), one can notice the increase in maximum overshoot/undershoot. One the other hand, if we compare with the other combinations, the settling time decreases. There is another way of minimizing the maximum overshoot, i.e. increasing the gain value of the compensator but this method has a disadvantage of system oscillations due to reduction in phase margin. The set-point values should be selected carefully to ensure better performance.

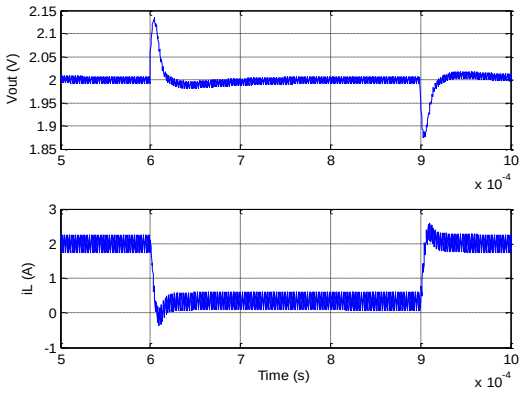

Figure 9. Load regulation for 1-DOF PID.

Coming to Fig. 9, with an addition of a step load transient to the converter (closed-loop), when there is a load change of 0.3 A to 2 A, a satisfactory time response is achieved i.e. 5 μs. Fig. 10 shows line regulation within a satisfactory range while keeping the values for input voltage varying from 4 V to 6 V. Other PID controllers also show better load and line regulation just like shown by 1-DOF PID controller. All the controllers are also found showing adequate set-point tracking. In summary, the switching converters can be controlled through PID controllers for better performance.

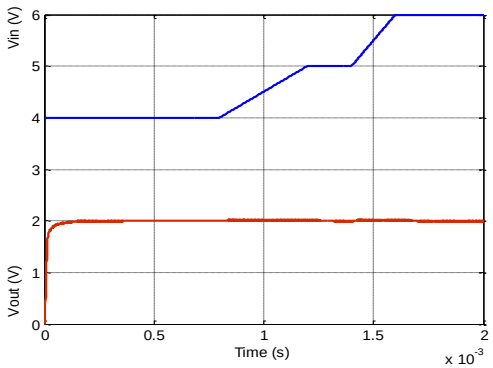

Figure 10. Line regulation for 1-DOF PID.

V. Conclusion

Different types of DC-DC buck converter controllers are designed; their operations are simulated using MATLAB and Simulink with the prototype buck converter having a DC-DC function; results taken and compared. The simulations validate the design concluding that improvement in one of the specifications (maximum overshoot and settling time) cause a fall in the other. For this particular design, less overshoot is seen in lead-lag compensator as compared to the conventional PID controller. Dynamic performance has been investigated through 1-DOF PID controller. These controllers are optimized with the help of MATLAB tool named as SISO Design Tool.

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