ISSN (Online) : 2319 - 8753
ISSN (Print) : 2347 - 6710

International Journal of Innovative Research in Science, Engineering and Technology

Volume 3, Special Issue 3, March 2014

2014 International Conference on Innovations in Engineering and Technology (ICIET'14)
On 21st & 22nd March Organized by

K.L.N. College of Engineering, Madurai, Tamil Nadu, India

Deep Submicron 50nm CMOS Logic Design With FINFET

P.C.Rajashree[#1], Ancy Thomas[#2], Rose Jaria[#3], Jane Precilla[#3], Alfred Kirubaraj[#4]

Department Of ECE, Karunya University, Coimbatore , Tamil Nadu, India.

Abstract— As the deep submicron technology is introduced, it fulfills the need of increase in speed and efficiency by using transistors of smaller size with faster switching rates. The shrink in the size of MOSFETs substantially increases the channel leakage also increasing the power dissipation. The thin body MOSFET is the backbone of FinFET. MOSFET faces problems like short channel effect, power dissipation and current leakage. FinFET is a double gate MOSFET that has two gates to control the channel and offers distinct advantages for scaling to very short gate lengths. The two gates together strongly influence the channel potential, combating the drain impact, and leading to the better ability to shut off the channel current reducing Drain Induced Barrier Lowering (DIBL). The short channel effect (SCE) can be suppressed and the power dissipation can be reduced by decreasing the fin width (T_{fin}). This paper deals with the comparison of FinFETs (NAND) in 70nm and 50nm technology in different logic styles IG (Independent gate), SG (Short gate) & IG/LP (Hybrid) modes, also it's been compared in terms of parameters like power dissipation (µW) and delay (ps). It is observed that the power dissipation (µW) in 50nm technology for SG mode, NAND gate is reduced by 49.15%, when compared to 70nm technology. When compared to 70nm NAND, the 50nm NAND, SG mode dissipates 34.04%, IG mode dissipates 29.55% and IG/LP mode dissipates 18.33% of power. It is also observed that SG mode has least delay because both gates are tied together to have high current drive. When compared to an 70nm NAND, the 50nm NAND, SG mode has 35.18%, IG mode has 61.76% and IG/LP mode has 55.52% of delay.

Keywords—FinFET, Drain Induced Barrier Lowering, Short Channel Effect, Short Gate Mode, Independent Gate Mode, Hybrid Mode

I. Introduction

As the technologies have advanced, the size of the conventional bulk metal-oxide-semiconductor field effect transistor (MOSFET) shrinks over the years. However, primary requirements such as speed, power dissipation and efficiency are still sought after. The scaling of the MOSFET from 10µm to 22nm over the last 40 years faces major concerns that have to be dealt with. The key limitation is the short channel effect (SCE) which is caused as the length of the channel is reduced leading to the lowering of the drain potential as drain source voltage increases allowing the flow of electrons . This is called Drain Induced Barrier Lowering (DIBL). The gate oxide thickness (T_{ox}) must also scale with the channel length to maintain gate control, proper threshold voltage (V_{th}) and performance. The thinning of the gate dielectric results in gate leakage, degrading the circuit performance and power [1]. The main contributor to the MOSFET leakage is sub-threshold leakage. When the gate to source voltage is below the threshold voltage, the current between the source and the drain of a MOSFET must be ideally zero, but the off-state current (I_{off}) continues to flow. This leads to the increase in power dissipation.

In order to combat these issues, the control of gate over the channel was improved by incorporating multi-gate devices or multiple gate field-effect transistors (MuGFET). The double gate metal oxide semiconductor field effect transistor (DGMOSFET), produces better control of short channel effects, lower leakage currents and enhances scaling efficiency in CMOS [2]. Among these, the fin-type field-effect transistors (FinFETs) are the most promising device structure to address these issues and most compatible with that of conventional CMOS. Thus making the fabrication processes easier [3].

TABLE I

COMPARISON OF MOSFET AND FINFET

MOSFET	*FinFET*
The main obstacle is that the control of current leakage is difficult.	The presence of multiple fins helps reduce leakage currents.
It is difficult to obtain higher on currents in bulk MOSFET.	It is easier to obtain higher on currents using multiple fins.
Power Dissipation is more.	Power Dissipation is less.
It is a planar device as the current flows parallel to wafer and the channel is placed on wafer plane.	It is a quasi-planar device -as the current flows parallel to wafer and the channel is perpendicular to wafer plane.
Only one gate is present to control the channel.	Two gates are present to control the channel hence reducing short channel effect. This is available in Short Gate (SG) and Independent Gate (IG) mode.
I_{off} -the drain current when V_{gs}=0, V_{ds}=V_{dd} (Ideally 0) increases as it goes further away from the gate.	Due to double gate, the gate capacitance is doubled, hence limiting I_{off} (Ideally 0).

The paper is structured as follows. In Section II deals with FinFET technology and the various modes of operation. Section III discusses the 50nm NAND logic gate using FinFETs. Section IV presents the results and discussion on comparison of 70nm and 50nm technology. Finally Section V presents the conclusion.

II. FINFET TECHNOLOGY

FinFET is a non-planar device having 'fin' like shaped body where the gate is wrapped around and over the fin which acts as a transistor channel. It is also termed as quasi-planar device as the current flows parallel to wafer plane and the channel is perpendicular to wafer plane [3].

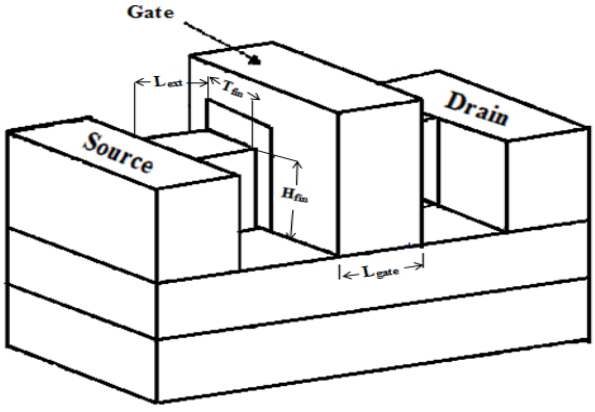


Figure 1: Structure of FinFET

Basically, FinFET was designed to be constructed on silicon-on-insulator (SOI) wafers. But the recent research has made it possible for FinFETs to work on bulk silicon wafers and improve the performance of certain parameters.

Effective channel length $L_{eff} = L_{gate} + 2\times L_{ext}$ (1)

Effective channel width $W = T_{fin} + 2\times H_{fin}$ (2)

Where H_{fin} and T_{fin} the fin height and thickness respectively, L_{gate} is length of the gate, L_{ext} is extended source or drain region as explained in Figure 1. Fin width (T_{fin}) plays a major role for controlling the short channel effect effectively. Therefore $T_{fin} \sim L_{gate}/2$ is followed [5].

In a FinFET structure, an ultra-thin Si fin forms a conducting channel wherein the electrons flow from source to drain. This conducting channel is wrapped by gate where the input voltages are supplied. Hence controlling the flow of electrons even in off state preventing the leakage of current. Sometimes there is an increase in the amount of charge carriers and the rate at which it flows, resulting in the breakdown of the conducting channel formed by single fin. This blocks the flow of electrons from source to drain which ceases the current flow.

The number of fins is increased in multi-gate field-effect transistors (MuGFET) which are constructed parallel to each other improving short channel effect. As the number of fins increases, the amount of charge carriers flowing from higher potential to lower potential also increases. Therefore, the rate at which the carriers flow is faster increasing the switching speed. The main advantage of multiple fins is better gate control over the conducting channel. Due to this, there is a reduction in current leakage. This attains high on-state drive current.

FinFETs have various logic design styles. This paper deals with two input NAND logic gate using FinFETs in SG, IG and IG/LP modes.

A. Short Gate (SG) Mode:

In the short gate mode, the front gate and the back gate is shorted together which provides better drive strength. If one of the input voltages is unstable then either the front gate or the back gate will be able to control over the operation even when the other one is affected. This mode improves efficiency and can achieve low leakage.

B. Independent Gate (IG) Mode:

The pull up transistors is merged in independent gate mode. The front gate and the back gate are given two independent input voltages respectively. The number of transistors used is reduced thereby, increasing the flexibility in circuit design. The delay is more when compared to ordinary CMOS.

C. Hybrid (LP/IG) Mode:

The hybrid mode is the combination of IG and LP (Low Power) modes. The back gates of the pull down transistors of this mode are given reverse bias voltage (V_{low}) which results in raised switching speed.

III. 50nm NAND LOGIC GATE USING FINFETS

International Technology Roadmap for Semiconductors presents the future technologies and challenges faced

(ITRS) which is tabulated in Table II. Where HP: High Performance technology, LSTP: Low Standby Power technology for portable applications, EOT: Equivalent Oxide Thickness [7]. According to Moore's law, the number of transistors fabricated on a chip increases twice a year which reduces the cost of fabrication process significantly. This devices the path to new technology nodes.

TABLE I.

EXCERPT OF 2003 ITRS TECHNOLOGY SCALING FROM 90nm TO 22nm.

Year of Production	2004	2007	2010	2013	2016
Technology node (nm)	90	65	45	32	22
HP Physical Lg (nm)	37	25	18	13	9
EOT (nm)(HP/LSTP)	1.2/2.1	0.9/1.6	0.7/1.3	0.6/1.1	0.5/1.0
V_{DD} (HP/LSTP)	1.2/1.2	1.1/1.1	1.1/1.0	1.0/0.9	0.9/0.8
I_{on}/W,HP (mA/mm)	1100	1510	1900	2050	2400
I_{off}/W,HP (mA/mm)	0.05	0.07	0.1	0.3	0.5
I_{on}/W,LSTP(mA/mm)	440	510	760	880	860
I_{off}/W,LSTP(mA/mm)	$1e^{-5}$	$1e^{-5}$	$6e^{-5}$	$8e^{-5}$	$1e^{-4}$

The layout design of 50nm technology two input NAND logic gate using various FinFETs logic styles has been featured in this section. The reduction in the area consumed by the 50nm FinFETs is advantageous in many ways. In short, the miniaturization improves cost, speed, power consumption. Figure 3.1 to Figure 3.3 shows the circuit design of two input NAND logic gates and the truth table is shown in Table III.

TABLE II

TRUTH TABLE OF NAND

INPUT 1	INPUT 2	OUT
0	0	1
0	1	1
1	0	1
1	1	0

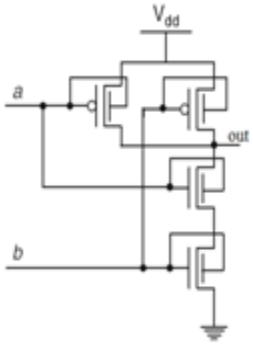


Figure 3.1: SG-Mode NAND

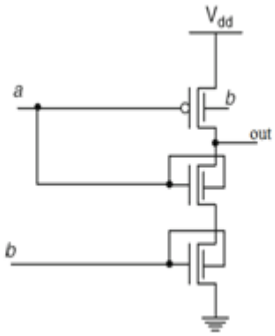


Figure 3.2: IG-Mode NAND

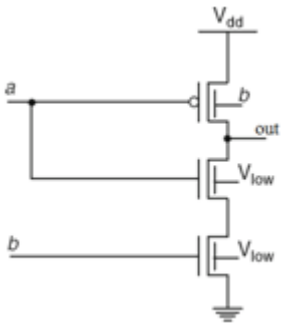


Figure 3.3: IG/LP-Mode NAND

IV. RESULTS AND DISCUSSION (70nm AND 50 nm)

The two input NAND logic gate using FinFET has been designed in various modes using Microwind 3 Tool by selecting 50nm foundry. The layout has been designed following the Lambda design rules as shown in Figure 4.1. to Figure 4.9. The layout has been designed with constant gate length (L_{gate}) as 50nm and fin width (T_{fin}) as 25nm. Along with various modes, the NAND logic gate has been designed varying the number of fins in the layout design. Power dissipation and delay for 70nm technology and 50nm technology has been hereby discussed.

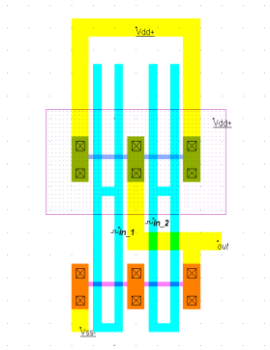


Figure 4.1: SG Layout (1 Fin)

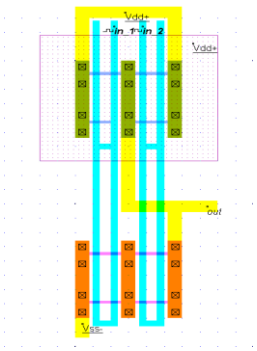


Figure 4.2: SG Layout (2 Fins)

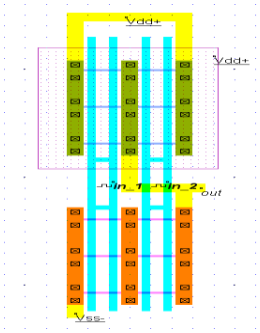


Figure 4.3: SG Layout (3 Fins)

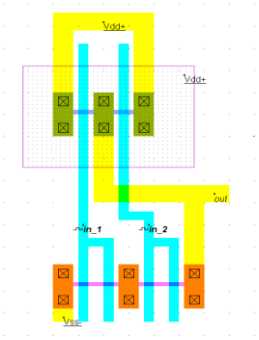


Figure 4.4: IG Layout (1 Fin)

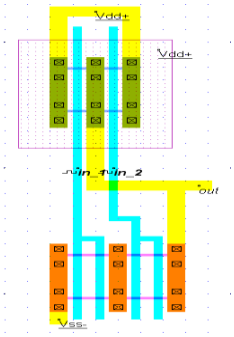


Figure 4.5: IG Layout (2 Fins)

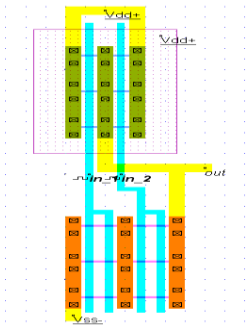


Figure 4.6: IG Layout (3 Fins)

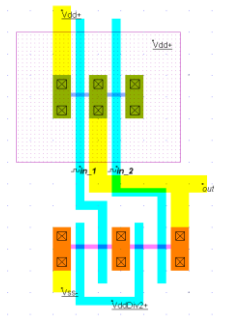


Figure 4.7: IG/LP Layout(1 Fin)

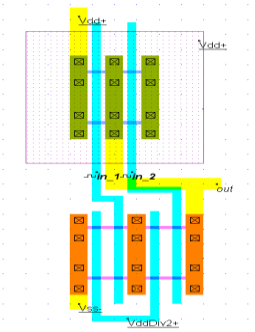


Figure 4.8: IG/LP Layout (2 Fins)

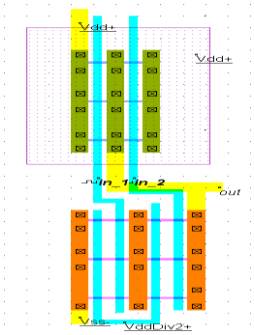


Figure 4.9: IG/LP Layout (3 Fins)

The power dissipation in various modes of 70nm technology and 50nm technology has been tabulated in Table IV. to Table VI. by varying the supply input voltage from 0.35V to 2.5V. It is inferred from the table that the power dissipation in 70nm technology is 29.36% which is higher than the others with multiple fins of 50nm technology i.e. 25.98% and these values have been graphically represented. The delay calculated as per Table VII. to Table IX. shows that the NAND-SGmode has the minimum delay by 35.18% in 50nm technology.

TABLE III

POWER DISSIPATION FOR SG MODE

SUPPLY VOLTAGE VDD (V)	**POWER DISSIPATION (µW)**			
	70nm NAND	***50nm 1Fin***	***50nm 2 Fin***	***50nm 3 Fin***
0.35	0.356	0.044	0.046	0.067
0.5	1.394	0.059	0.063	0.091
0.7	0.921	0.418	0.463	0.692
1.2	10.288	0.858	1.042	1.745
1.8	38.246	1.381	1.712	2.964
2.5	57.857	1.957	2.451	4.305

TABLE IV

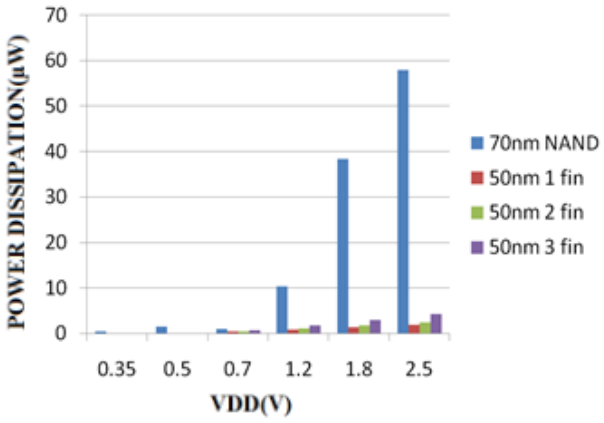
POWER DISSIPATION FOR IG MODE

SUPPLY VOLTAGE VDD (V)	**POWER DISSIPATION (µW)**			
	70nm NAND	***50nm 1 Fin***	***50nm 2 Fin***	***50nm 3 Fin***
0.35	0.869	0.025	0.092	0.130
0.5	0.65	0.035	0.125	0.174
0.7	1.889	0.271	0.907	1.277
1.2	22.706	3.021	6.053	9.075
1.8	36.511	3.022	6.054	9.074
2.5	38.156	3.022	6.054	9.078

TABLE V

POWER DISSIPATION FOR IG/LP MODE

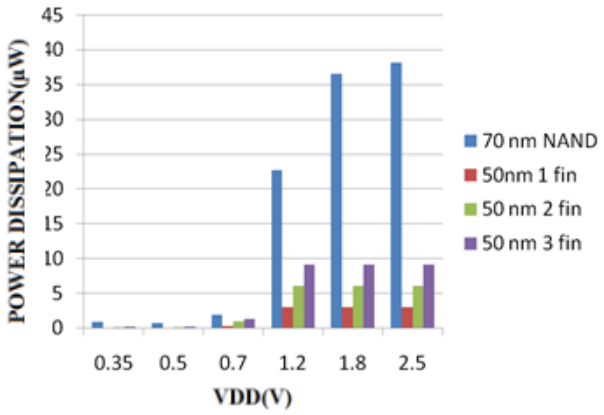
SUPPLY VOLTAGE VDD (V)	POWER DISSIPATION (µW)			
	70nm NAND	*50nm 1 Fin*	*50nm 2 Fin*	*50nm 3 Fin*
0.35	0.851	0.024	0.044	0.065
0.5	0.447	0.033	0.06	0.087
0.7	1.897	0.245	0.457	0.664
1.2	21.227	0.315	0.628	0.941
1.8	34.332	0.314	0.629	0.943
2.5	35.376	0.315	0.63	0.941



GRAPH I. Power Dissipation for SG mode

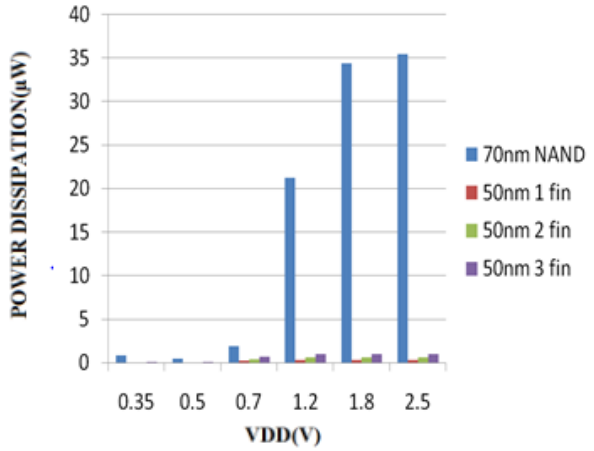
TABLE I. Delay for SG Mode

DELAY (ps)	*70nm NAND*	*50nm 1 Fin*	*50nm 2 Fin*	*50nm 3 Fin*
Fall Time	13.5	173	154	146
Rise Time	5.75	10	9	9



GRAPH II. Power Dissipation for IG Mode

DELAY (ps)	*70nm NAND*	*50nm 1 Fin*	*50nm 2 Fin*	*50nm 3 Fin*
Fall Time	11.750	20	15	15
Rise Time	9.0	10	13	10



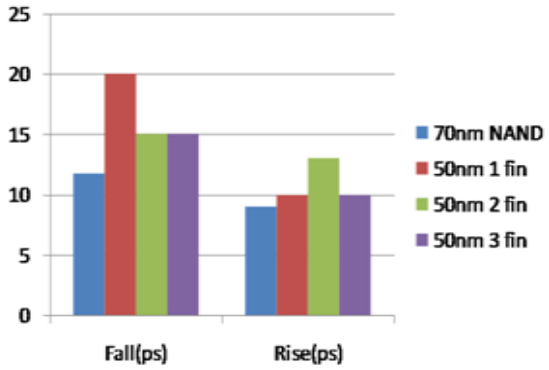
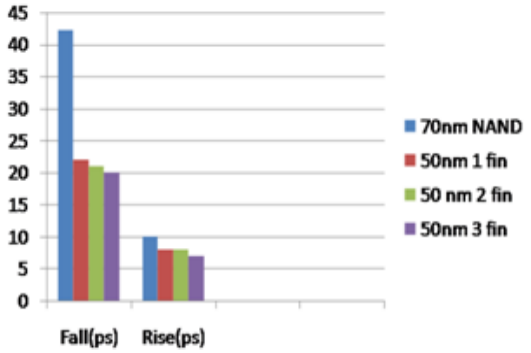


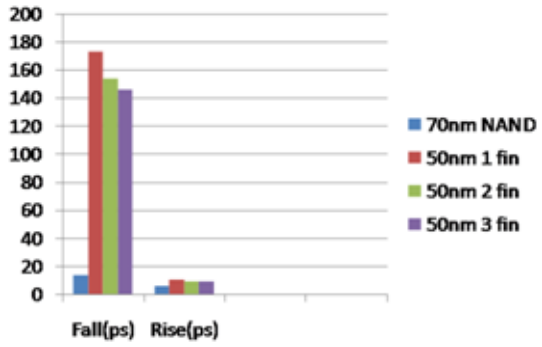
TABLE II Delay for IG Mode

DELAY (ps)	*70nm NAND*	*50nm 1 Fin*	*50nm 2 Fin*	*50nm 3 Fin*
Fall Time	42.25	22	21	20
Rise Time	10	8	8	7

GRAPH III.Power Dissipation for IG/LP Mode



GRAPH V. Delay for IG Mode



GRAPH VI. Delay for IG/LP Mode

V. Conclusion

The two input NAND logic gate is designed in SG mode, IG mode and IG/LP mode. The SG-FinFET provides better drive strength reducing delay whereas in IG-FinFET, the number of transistors needed is reduced and IG/LP-FinFET offers faster switching speed. However in 50nm has better control over short channel effects by device geometry as compared to 70nm technology. When parameters like power dissipation and delay are compared, it is observed that the power dissipation (µW) in 50nm technology for SG mode NAND gate is reduced by 49.15%, when compared to 70nm technology. Also, the 50nm NAND SG mode has 35.18%, IG mode has 61.76% and IG/LP mode has 55.52% of delay.

References

[1] Manorama, PavanShrivastava, SaurabhKhandelwal andShyamAkashe, "Threshold Voltage Control through Multiple Supply for Low Power IG-FinFET Circuit," *International Journal of Computer Applications* (0975 – 8887) Volume 78 – No.8, September 2013 April 1955.

[2] MahenderVeshala, RamchanderJatooth and Kota Rajesh Reddy, "Reduction of Short-Channel Effects in FinFET," *International Journal of Engineering and Innovative Technology (IJEIT)* Volume 2, Issue 9, March 2013.

[3] Prateek Mishra, AnishMuttreja and Niraj K. Jha, *"FinFET Circuit Design,"* Department of Electrical Engineering, Princeton University, NJ, USA.

[4] V.Raj Kumar and A. Alfred kirubaraj, "Submicron 70nm CMOS Logic Design With FINFETs," *International Journal of Engineering Science and Technology* Vol. 2(9), 2010, 4751-4758.

[5] K. G. Anil, K. Henson, S. Biesemans and N. Collaert, *"Layout Density Analysis of FinFETs,"* InterUniversity Microelectronics Center, 75 Kapeldreef, 3000 Leuven, Belgium.

[6] Michael C. Wang, "Independent-Gate FinFETs Circuit Design Methodology," *International Journal of Computer Science (IAENG)*, 37:1,IJCS_37_1_06, July 2006.

[7] International technology road map for semiconductors (ITRS) 2003.

[8] Jung Hwan Choi, AdityaBansal, MesutMeterelliyoz, Jayathi Murthy and Kaushik Roy, *"Leakage Power Dependent Temperature Estimation to predict Thermal Runaway in FinFETCircuits,"* Electrical and Computer Engineering;Mechanical Engineering, Purdue University.

[9] AnishMuttreja, NiketAgarwal and Niraj K. Jha, *" CMOS Logic Design with Independent-gate FinFETs,"* Dept.of Electrical Engineering,Princeton University, Princeton, NJ 08544, Nov.2007.

[10] JieGu, John Keane, Sachin Sapatnekarand and Chris Kim, "Width Quantization Aware FinFET Circuit Design," University of Minnesota, Minneapolis.

[11] F. M. Bufler, Yoshinori Asahi, Hisao Yoshimura, ChristophZechner, A. Schenk, and Wolfgang Fichtner, *"Monte Carlo Simulation and Measurement of Nanoscale n-MOSFETs," IEEE Trans. Electron Devices*, VOL. 50, NO. 2, February2003.

[12] Kaushik Roy, SaibalMukhopadhyay, and Hamid Mahmoodi-Meimand, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-SubmicrometerCMOS Circuits," *Proceedings of the IEEE*, VOL. 91, NO. 2 February 2003.

[13] VenkatnarayanHariharan, "Compact model development for nanoscalefinfets," Department of Electrical Engineering, IIT Bombay, 2008.

S. Jim Hawkinson, "Analysis and Performance Comparison of CMOS and FinFET for VLSI Applications," *International Journal of Emerging Technology and Advanced Engineering*,Volume 3, Issue 2, February 2013.