

COMPAL CONFIDENTIAL

MODEL NAME : *PAL50/52*

PCB NO : *LA-6591P (DA80000JV10)*
LA-6593P HF (DA80000MB10)

BOM P/N : *43192831L01*

GPIO MAP:{Macallan} GPIO Map 10102010.xlsx

E3 MACALLAN 14" UMA/ATG

rPGA Sandy Bridge +
FCBGA PCH Cougar Point-M

2011-1-6

REV : 1.0(A00)

@ : Nopop Component

CONN@ : ME controll and stuff by default

MB Type	BOM P/N			
TPM EN/ TCM DIS	43192831L01	1@	3@	7@
TPM DIS/ TCM EN	43192831L02	2@	4@	7@
TPM DIS/ TCM DIS	43192831L04	2@	3@	7@
ATG TPM EN/ TCM DIS	43192831L11	1@	3@	7@
ATG TPM DIS/ TCM EN	43192831L12	2@	4@	7@
ATG TPM DIS/ TCM DIS	43192831L13	2@	3@	7@
TPM EN/ TCM DIS HF	4319BP31L01	1@	3@	8@

7@ MB PCB1	
Part Number	Description
DA80000JV10	PCB OFD LA-6591P REV0 M/B UMA

8@ MB PCB2	
Part Number	Description
DA80000MB10	PCB OFD LA-6593P REV0 M/B UMA HF

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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

PCH	USB PORT#	DESTINATION
	0	JUSB2 (Right side 1)
	1	JUSB3 (Right side 2)
	2	JESA1 (Right Side ESATA)
	3	JUSB1 (Ext Left Side)
	4	WLAN
	5	WWAN
	6	JMINI3(Flash)
	7	USH->BIO
	8	DOCKING
	9	DOCKING
	10	Express card
	11	Bluetooth
12	Camera	
13	LCD Touch	

USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	E3 Module Bay (USB3)
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

UMA DP/HDMI Port	Connetion
Port B	MB HDMI Conn
Port C	Dock DP port 2
Port D	Dock DP port 1

Layer No.	Name	Engineer proposal (Unit : mil)			
		Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil	
		SolderMask	0.6	0.50	
		Add Plating	1.3	1.40	
1	Top	Copper foil	0.5oz	0.70	
		Prepreg	1080LRC	2.80	1.17
2	GND	Copper foil	0.5oz	0.70	
		Core	3mil H/1	3.00	3.00
3	Sig1	Copper foil	1.0oz	1.30	
		Prepreg	7628HRC*2	17.06	15.10
4	Sig2	Copper foil	1.0oz	1.30	
		Core	3mil 1/1	3.00	3.00
5	VCC	Copper foil	1.0oz	1.30	
		Prepreg	7628HRC*2	17.06	15.76
6	Sig3	Copper foil	1.0oz	1.30	
		Core	3mil H/1	3.00	3.00
7	GND	Copper foil	0.5oz	0.70	
		Prepreg	1080LRC	2.80	1.17
8	Bottom	Copper foil	0.5oz	0.70	
		Add Plating	1.3	1.40	
		SolderMask	0.6	0.50	
Overall Thickness (1.45 mm ± 10%)					57.00

need to update Power Status and PM Table

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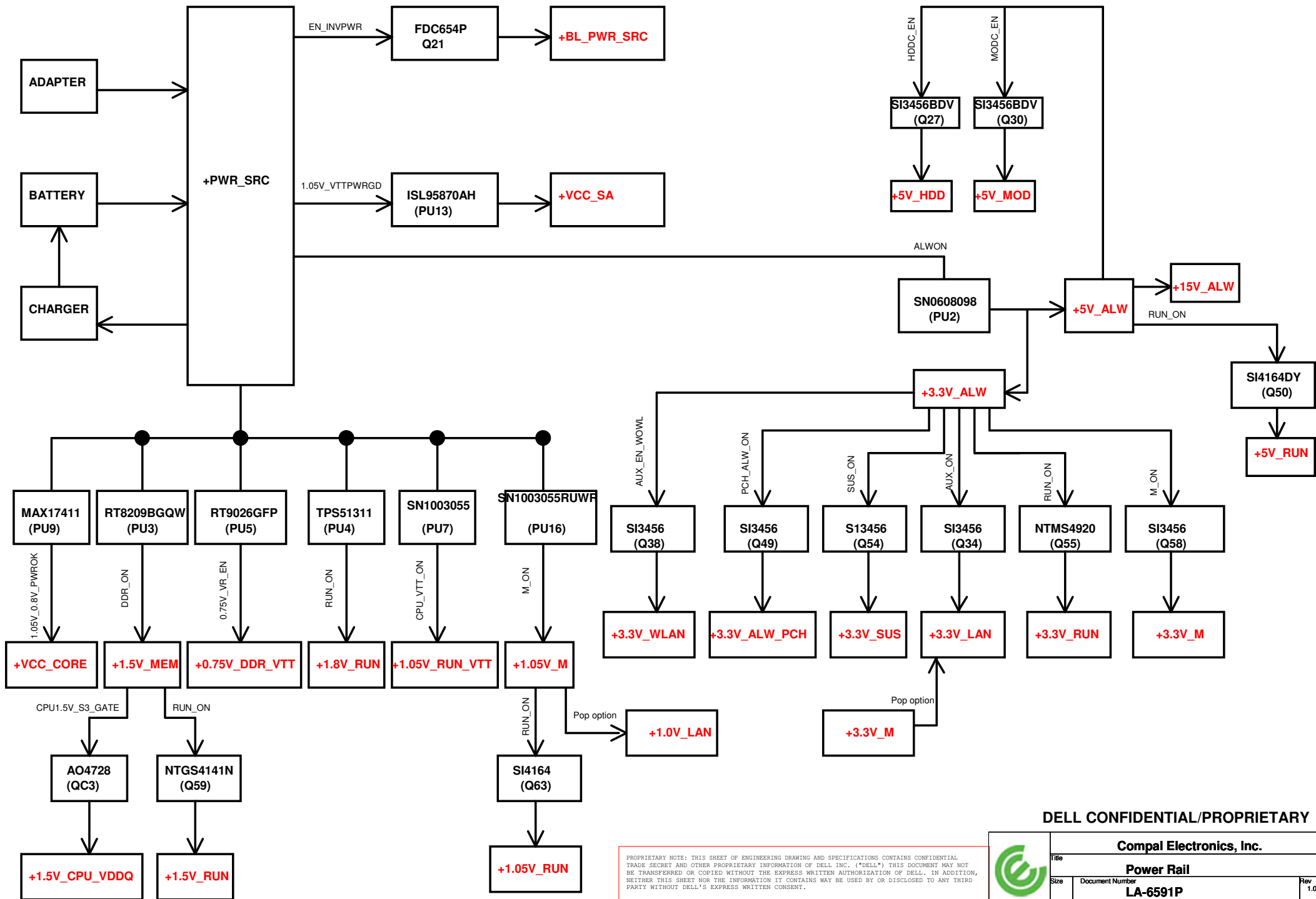
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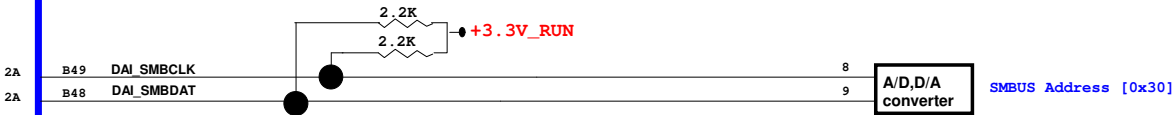
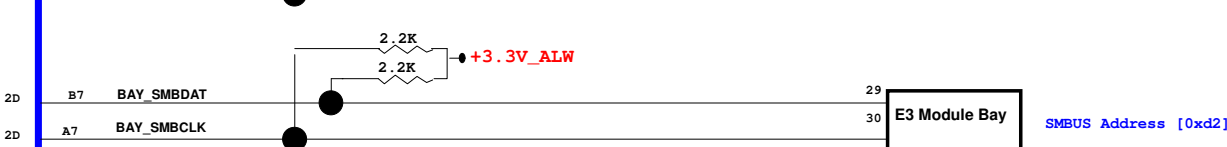
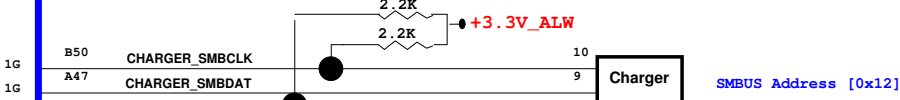
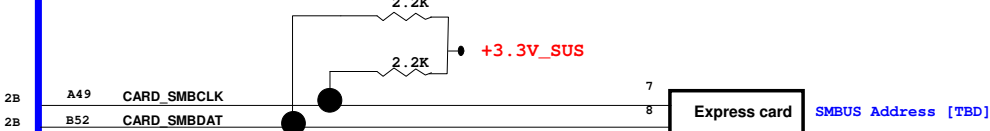
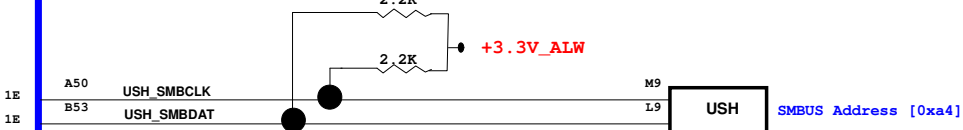
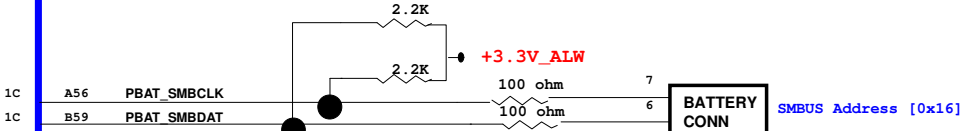
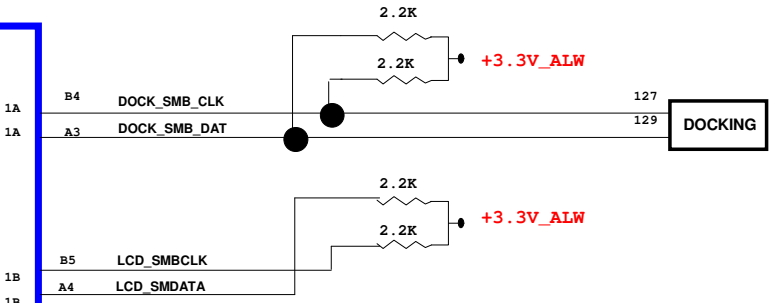
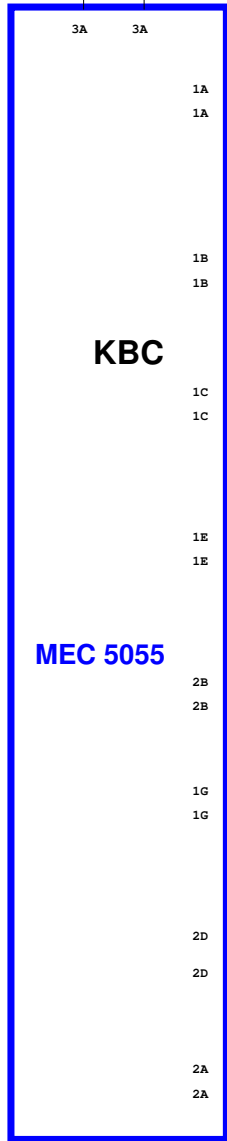
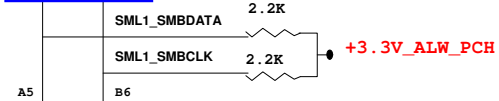
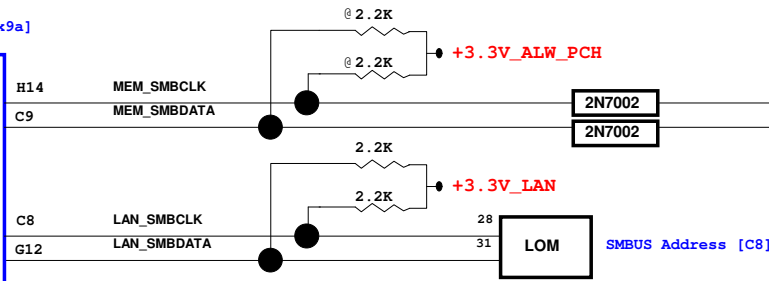
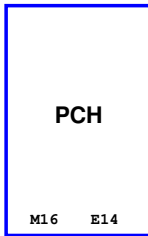
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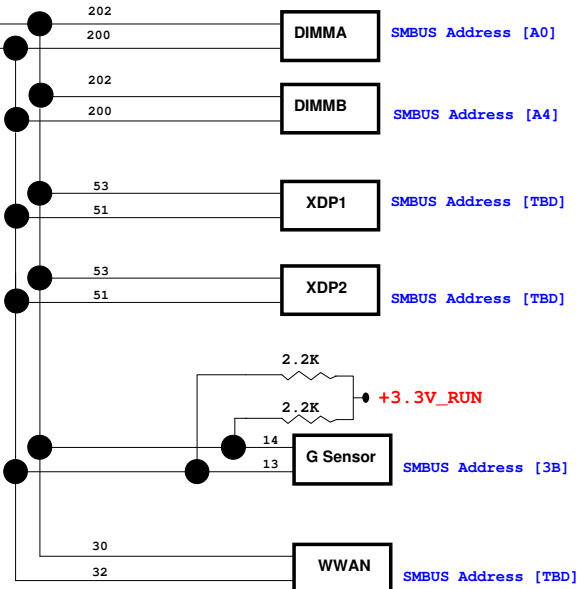


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SMBUS Address [0x9a]

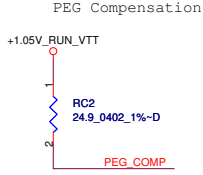
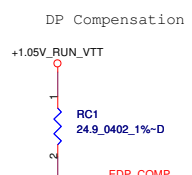
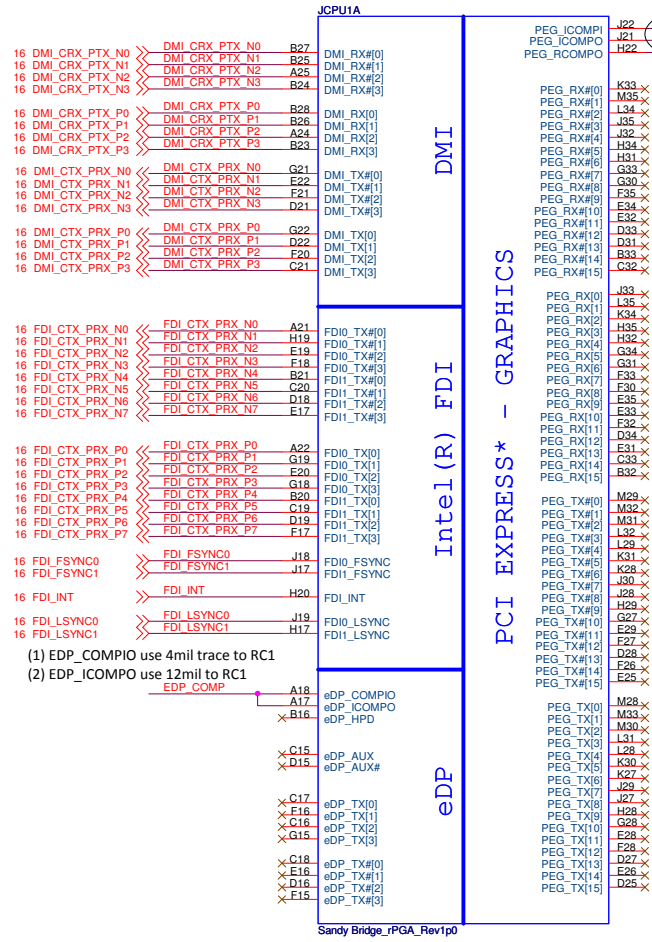


SMBUS Address
APR_EC: 0x48
SPR_EC: 0x70
MSLICE_EC: 0x72
USB: 0x59
AUDIO: 0x34
SLICE_BATTERY: 0x17
SLICE_CHARGER: 0x13



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SMBUS TOPOLOGY			
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(1) PEG_RCOMP (H22) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC2.
 (2) PEG_ICOMPO use 12mil connect to RC2



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

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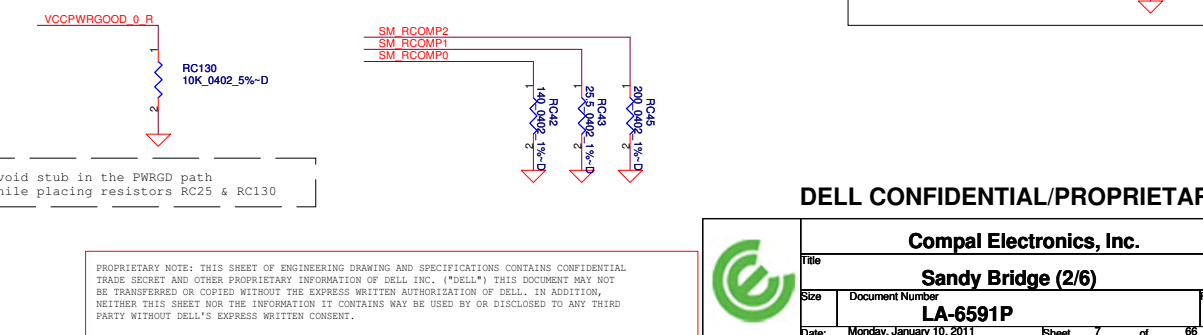
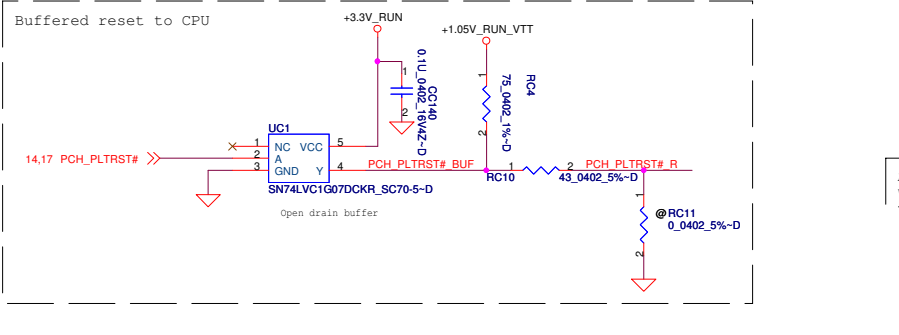
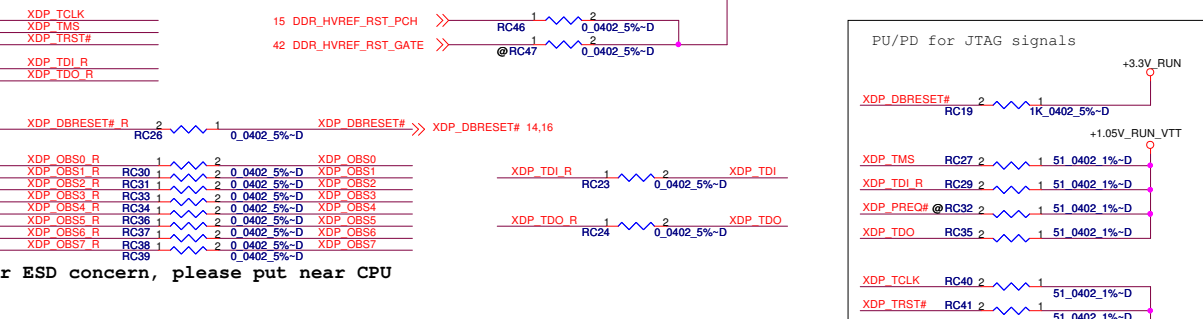
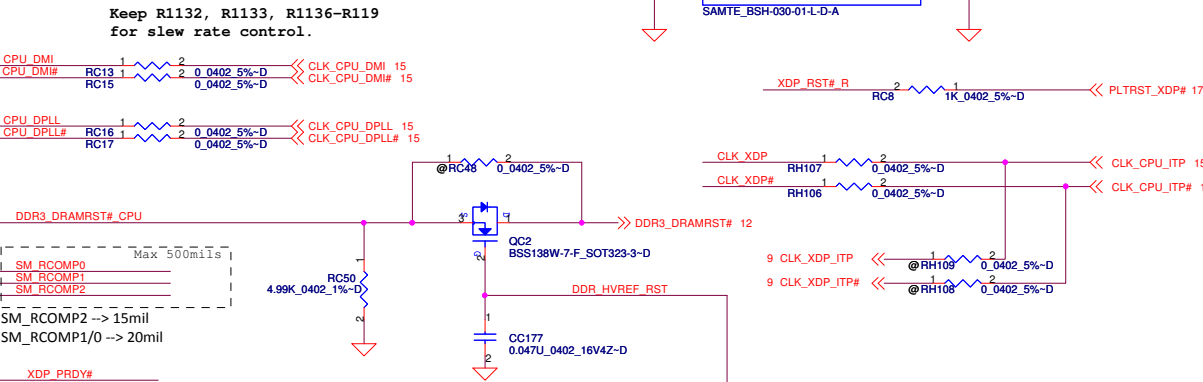
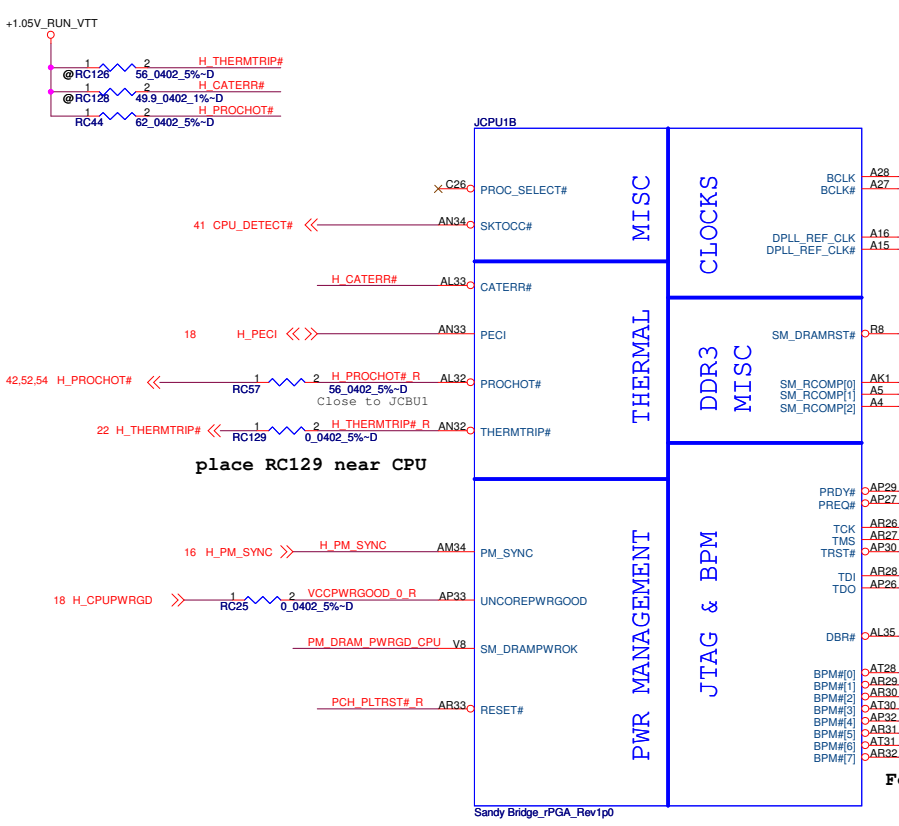
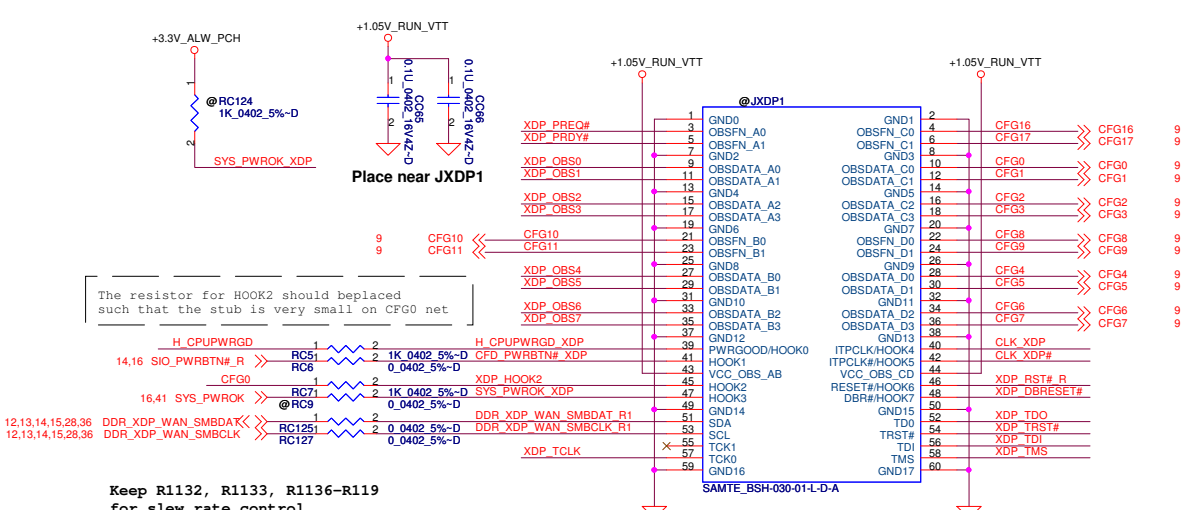
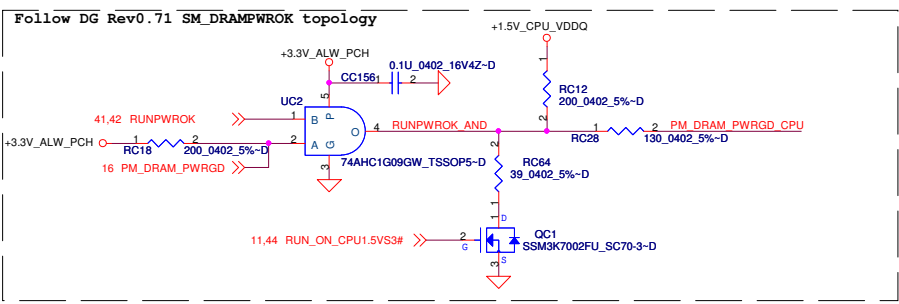
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Sandy Bridge (1/6)

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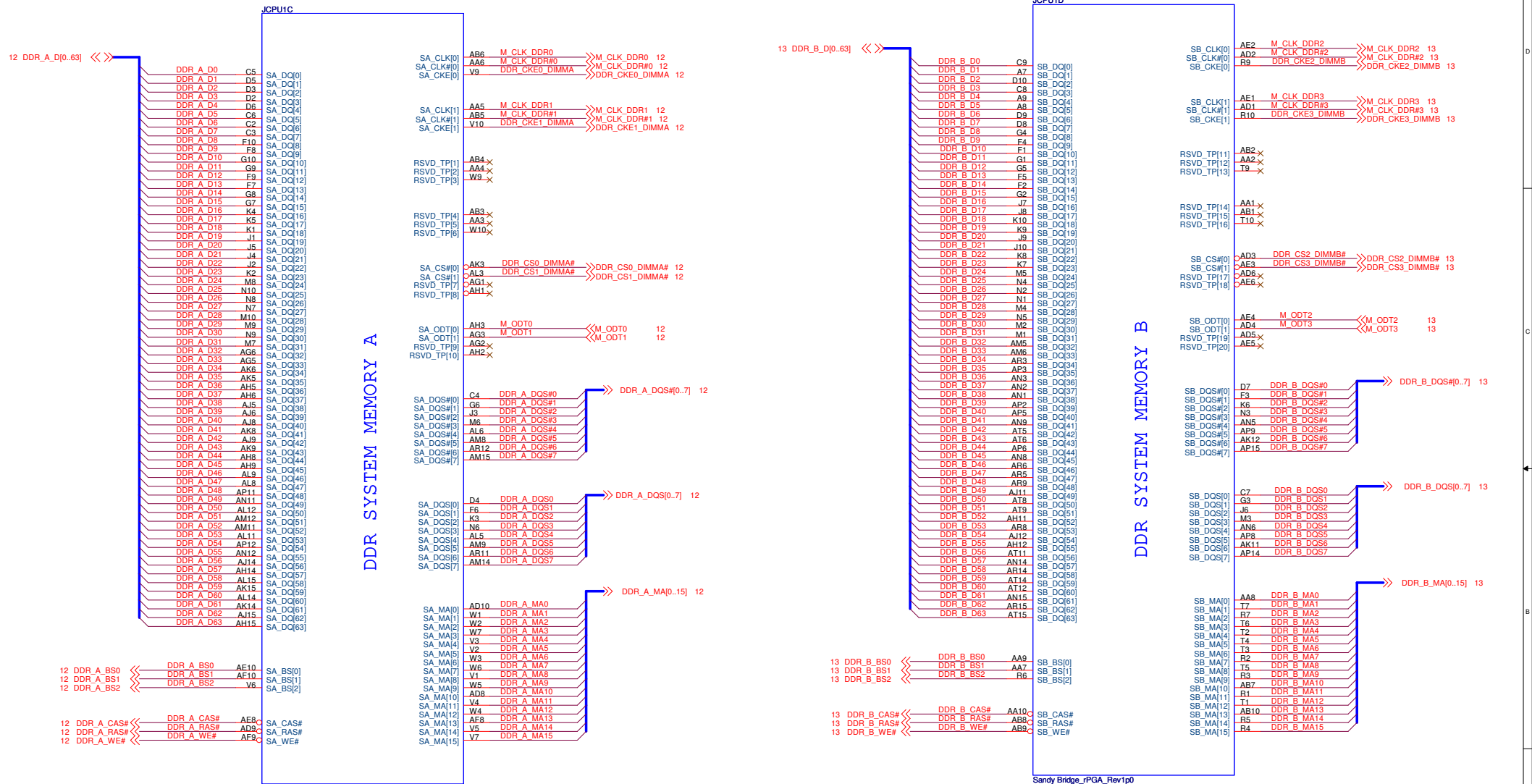


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Sandy Bridge_rPGA_Rev1p0

Sandy Bridge_rPGA_Rev1p0

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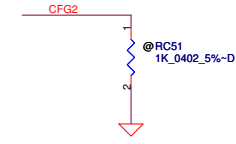
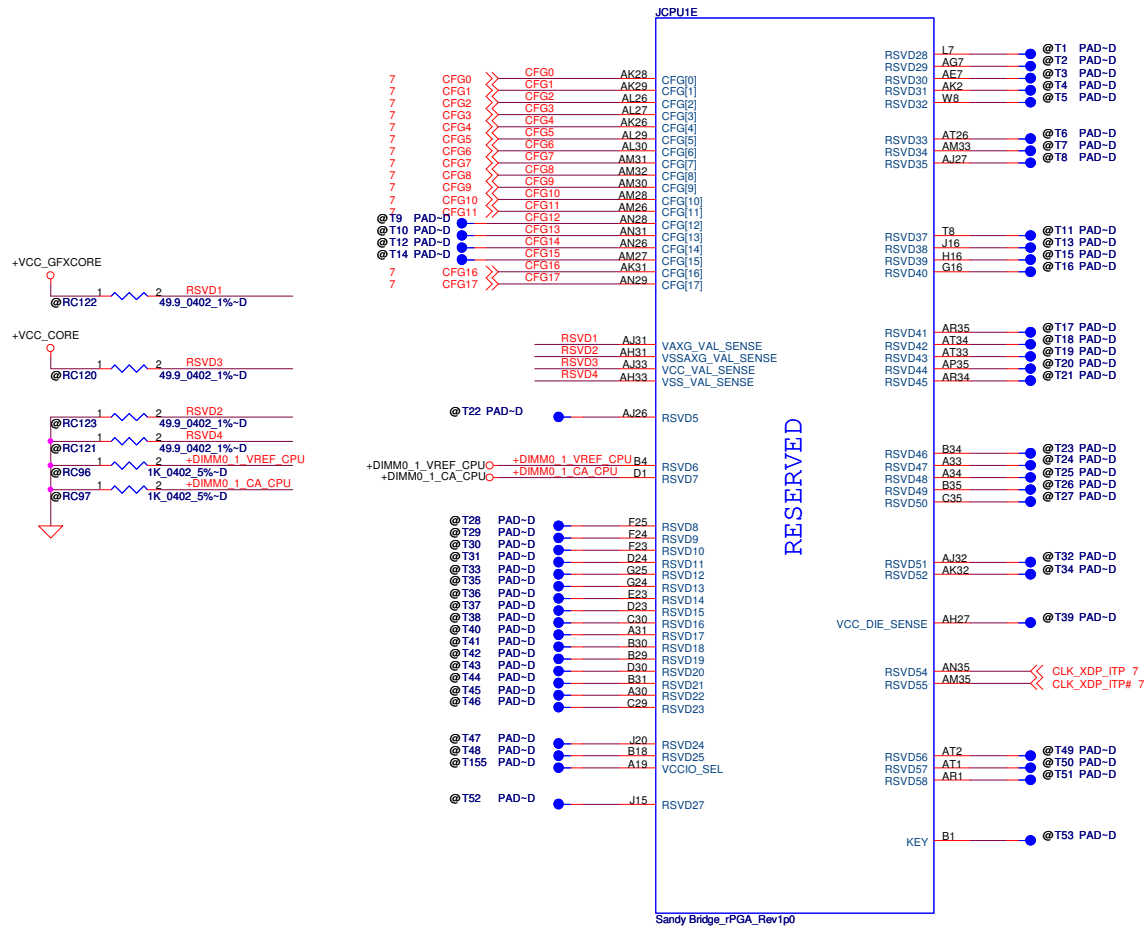
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Sandy Bridge (3/6)

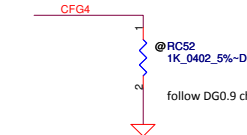
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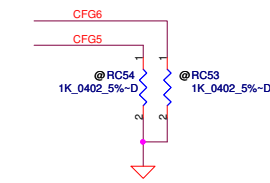
CFG Straps for Processor



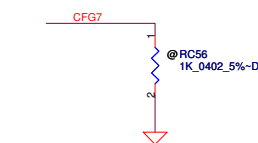
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

RESERVED

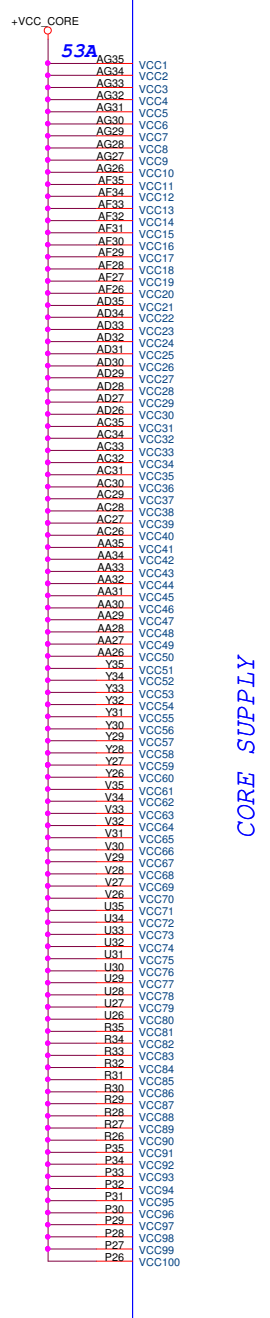
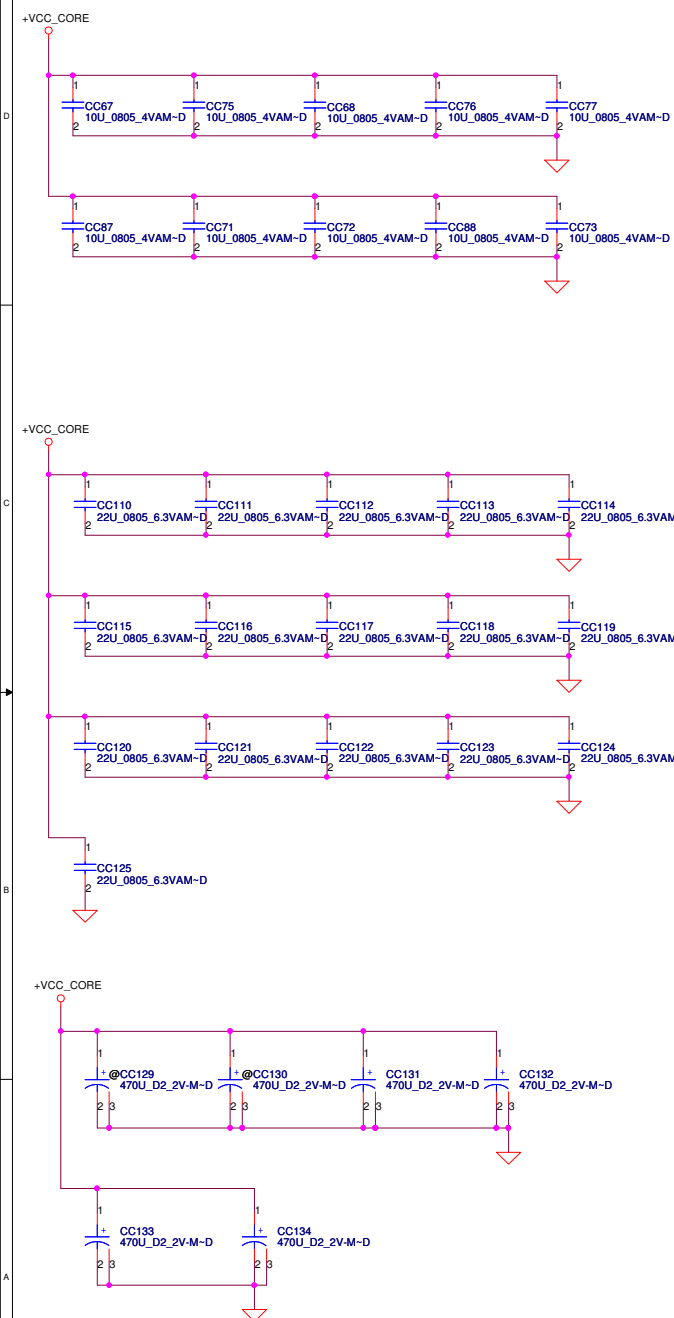
Sandy Bridge_rPGA_Rev1p0

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POWER

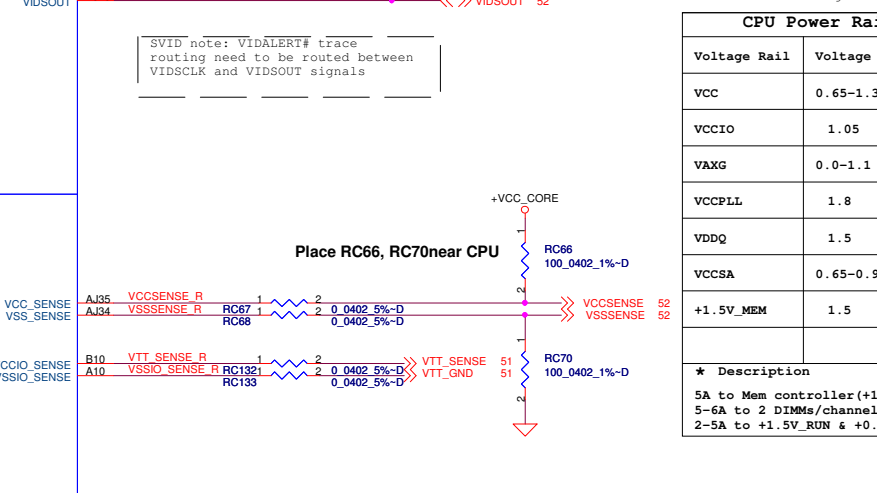
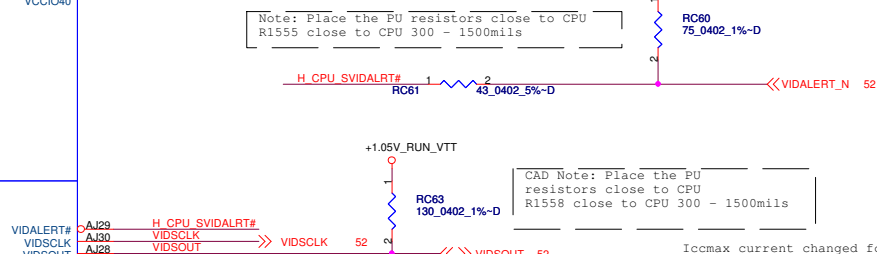
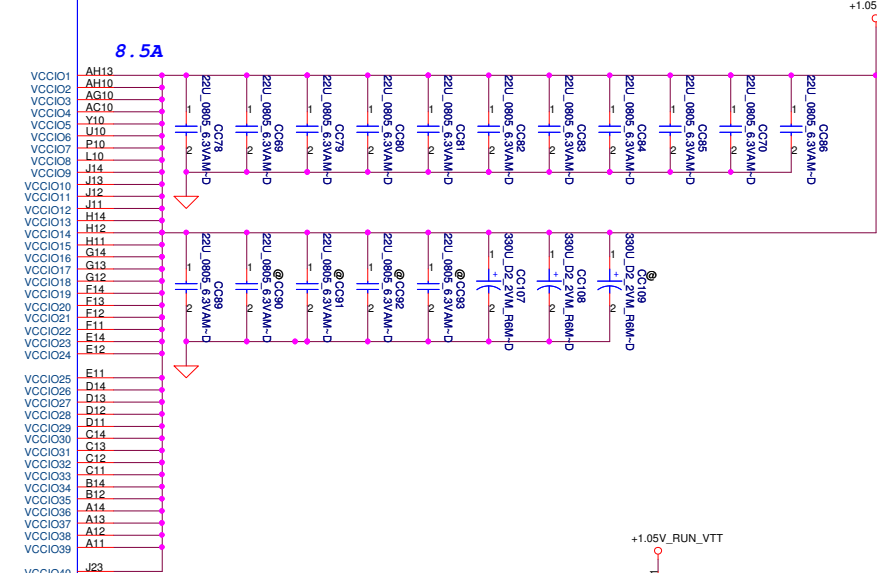


CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES



Note: Place the PU resistors close to CPU R1555 close to CPU 300 - 1500mils

CAD Note: Place the PU resistors close to CPU R1558 close to CPU 300 - 1500mils

SVID note: VIDALERT# trace routing need to be routed between VIDSCLK and VIDSOUT signals

Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05	8.5
VAXG	0.0-1.1	26
VCCPLL	1.8	3
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 *

* Description
 5A to Mem controller(+1.5V_CPU_VDDQ)
 5-6A to 2 DIMMs/channel
 2-5A to +1.5V_RUN & +0.75V_DDR_VTT

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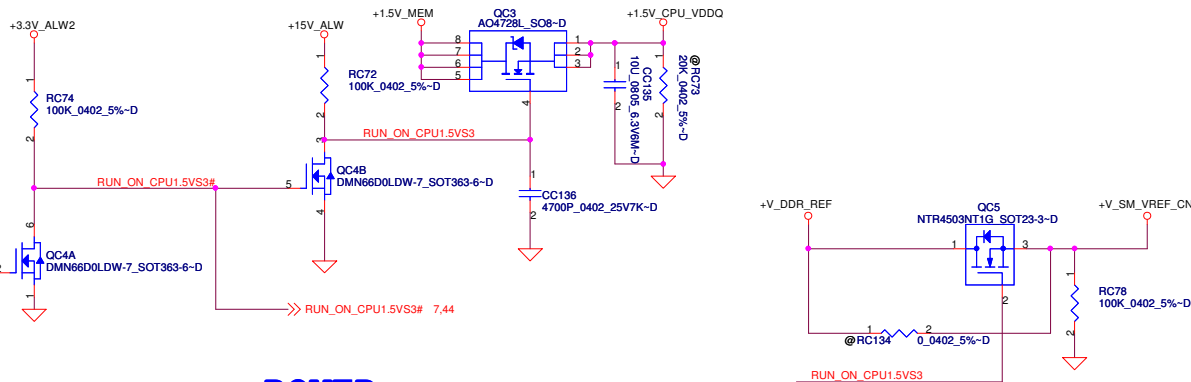
Sandy Bridge (5/6)

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+1.5V_CPU_VDDQ Source

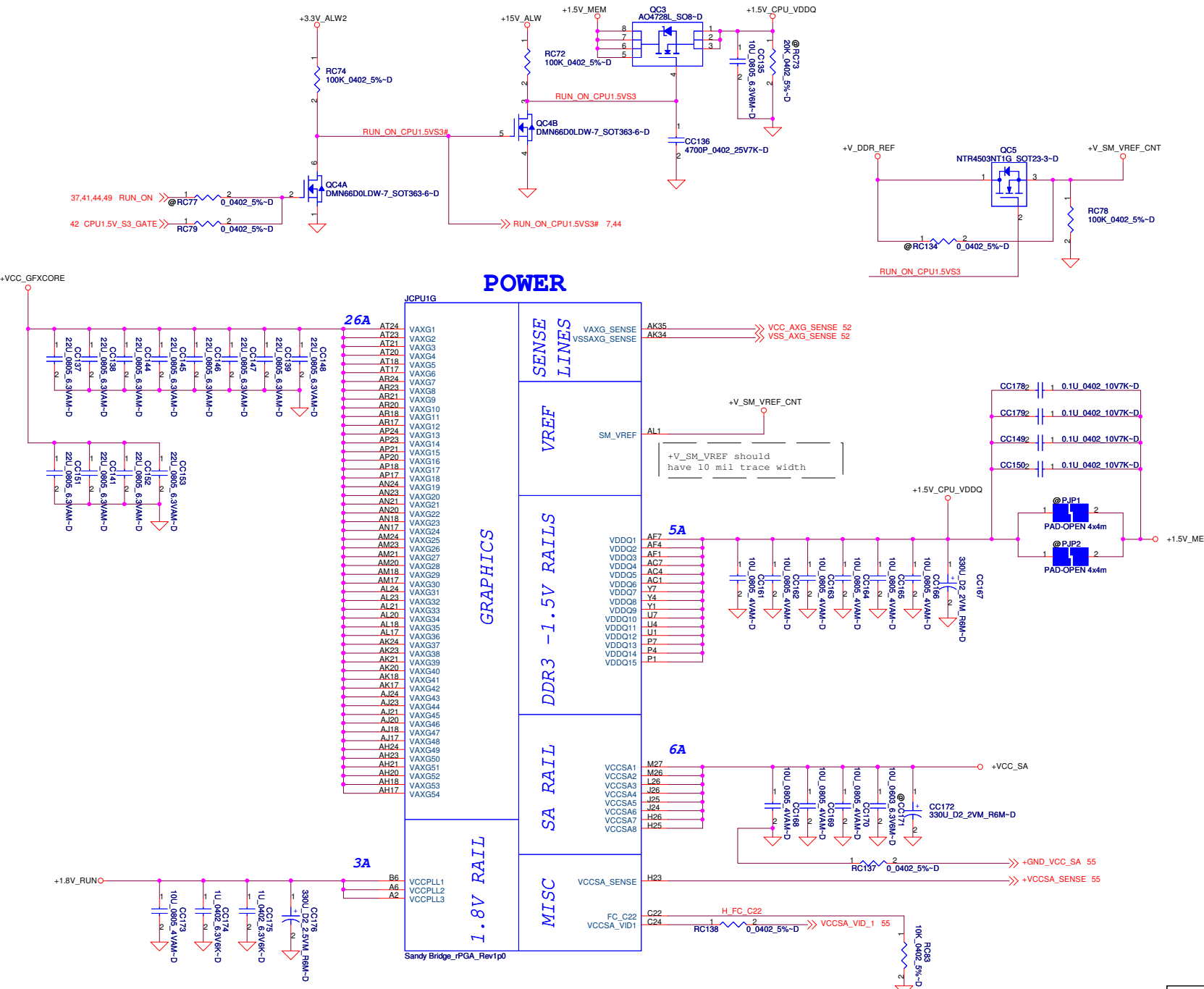


JCPU1H		
AT35	VSS1	VSS81
AT32	VSS2	AJ19
VSS3	VSS3	VSS83
AT29	VSS4	AJ16
AT27	VSS5	VSS84
AT25	VSS6	AJ13
AT22	VSS7	AJ10
AT19	VSS8	VSS86
AT16	VSS9	AJ7
AT13	VSS10	VSS87
AT10	VSS11	AJ4
AT7	VSS12	VSS88
AT4	VSS13	AJ3
VSS14	VSS14	AJ2
AR25	VSS15	VSS89
AR22	VSS16	AH35
AR19	VSS17	VSS92
AR16	VSS18	AH34
AR13	VSS19	VSS93
AR10	VSS20	AH32
AR7	VSS21	VSS94
AR4	VSS22	AH29
AR2	VSS23	VSS95
AP34	VSS24	AH28
AP31	VSS25	VSS97
AP28	VSS26	AH25
AP25	VSS27	VSS98
AP22	VSS28	AH22
AP19	VSS29	VSS99
AP16	VSS30	AH19
AP13	VSS31	VSS100
AP10	VSS32	AH16
AP7	VSS33	VSS102
AP4	VSS34	VSS103
AN30	VSS35	AH4
AN27	VSS36	VSS104
AN25	VSS37	AG9
AN22	VSS38	VSS105
AN19	VSS39	AG8
AN16	VSS40	VSS106
AN13	VSS41	AF6
AN10	VSS42	VSS107
AN7	VSS43	VSS108
AN4	VSS44	AF5
AM29	VSS45	VSS109
AM25	VSS46	AF3
AM22	VSS47	AH25
AM19	VSS48	VSS110
AM16	VSS49	AH22
AM13	VSS50	VSS111
AM10	VSS51	AH19
AM7	VSS52	VSS112
AM4	VSS53	AE34
AM2	VSS54	VSS113
AM1	VSS55	AE33
AL34	VSS56	VSS114
AL31	VSS57	AE31
AL28	VSS58	VSS115
AL25	VSS59	AE30
AL22	VSS60	VSS116
AL19	VSS61	AE29
AL16	VSS62	VSS117
AL13	VSS63	AE28
AL10	VSS64	VSS118
AL7	VSS65	AE27
AL4	VSS66	AE26
AL2	VSS67	VSS119
AK7	VSS68	AE9
AK3	VSS69	AD7
AK2	VSS70	AC9
AK1	VSS71	VSS120
AK19	VSS72	AC8
AK17	VSS73	VSS121
AK15	VSS74	AC7
AK13	VSS75	VSS122
AK11	VSS76	AC6
AK9	VSS77	VSS123
AK7	VSS78	AC5
AK5	VSS79	VSS124
AK3	VSS80	AC4
AJ25	VSS81	VSS125
		AC3
		VSS126
		AC2
		VSS127
		AC1
		VSS128
		AB35
		VSS129
		AB34
		VSS130
		AB33
		VSS131
		AB32
		VSS132
		AB31
		VSS133
		AB30
		VSS134
		AB29
		VSS135
		AB28
		VSS136
		AB27
		VSS137
		AB26
		VSS138
		Y9
		VSS139
		Y8
		VSS140
		Y7
		VSS141
		Y6
		VSS142
		Y5
		VSS143
		Y3
		VSS144
		Y2
		VSS145
		W35
		VSS146
		W34
		VSS147
		W33
		VSS148
		W32
		VSS149
		W31
		VSS150
		W30
		VSS151
		W29
		VSS152
		W28
		VSS153
		W27
		VSS154
		W26
		VSS155
		U9
		VSS156
		U8
		VSS157
		U7
		VSS158
		U6
		VSS159
		U5
		VSS160
		U3
		VSS161
		U2

POWER

GRAPHICS

1.8V RAIL

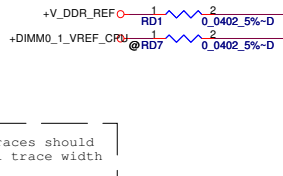


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Sandy Bridge (6/6)
LA-6591P
 Date: Monday, January 10, 2011 Sheet 11 of 66

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Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

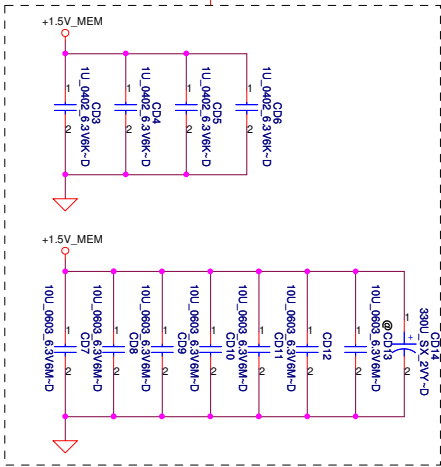


All VREF traces should
have 10 mil trace width

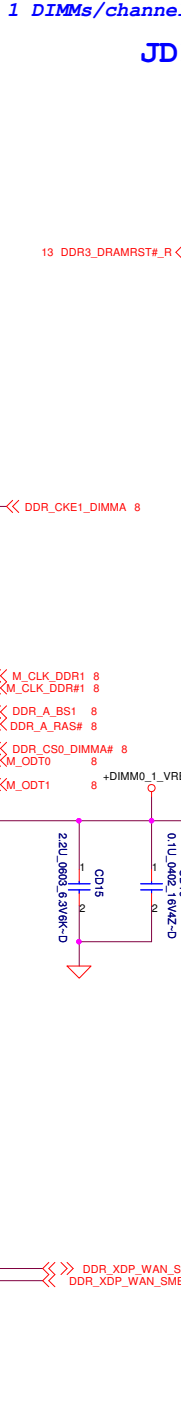
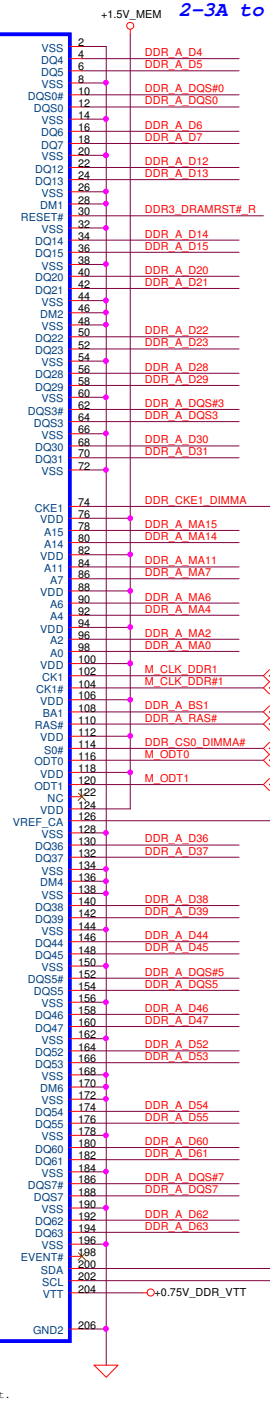
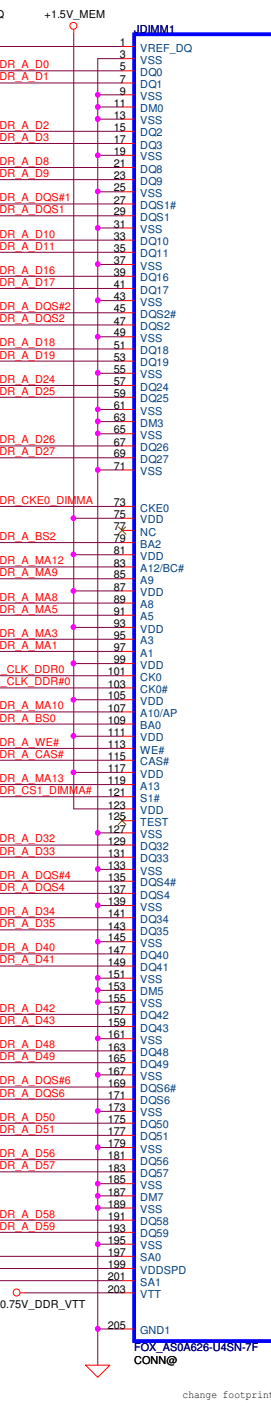
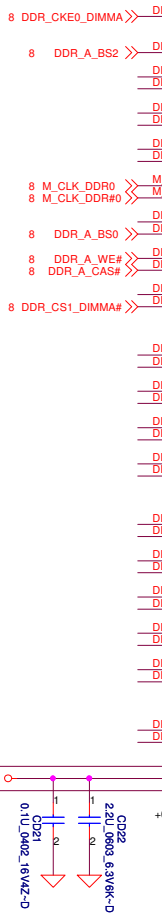
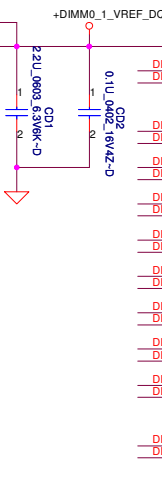
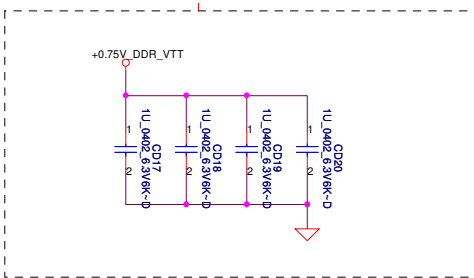
Populate RD1 for Intel DDR3
VREFDQ multiple methods M1

- 8 DDR_A_DQS#0[0.7] <<>
- 8 DDR_A_D[0.63] <<>
- 8 DDR_A_DQS#0[0.7] <<>
- 8 DDR_A_MA[0.15] <<>

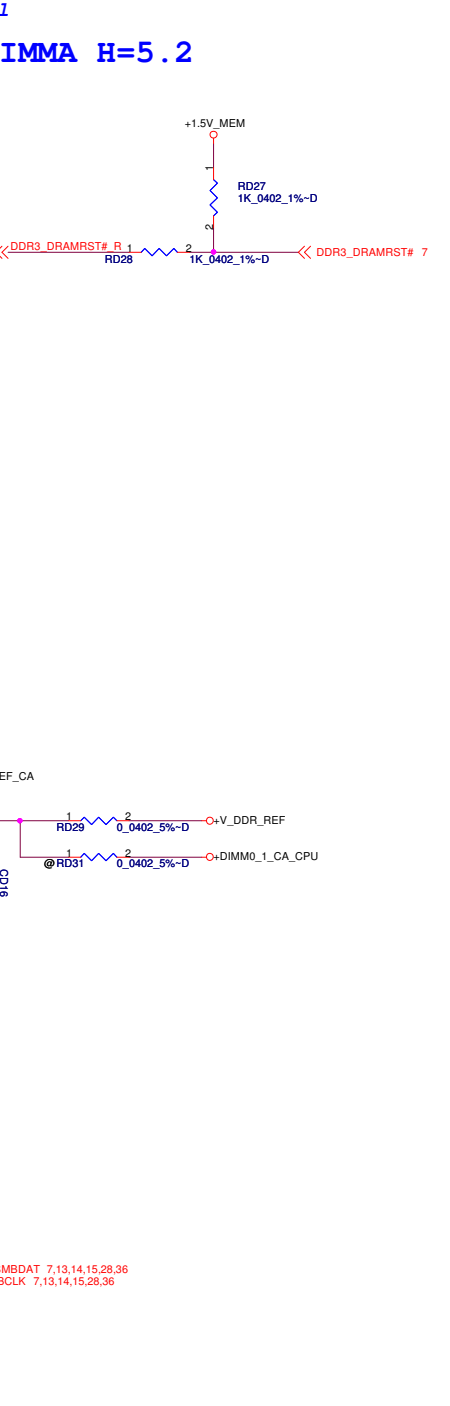
Layout Note:
Place near JDIMMA



Layout Note:
Place near JDIMMA.203,204



JDIMMA H=5.2



change footprint.

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DDRIII-SODIMM SLOT1	
LA-6591P	
Date: Monday, January 10, 2011	Sheet 12 of 66

Rev 1.0

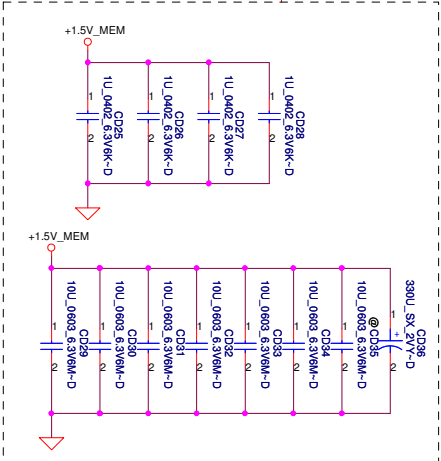
All VREF traces should have 10 mil trace width



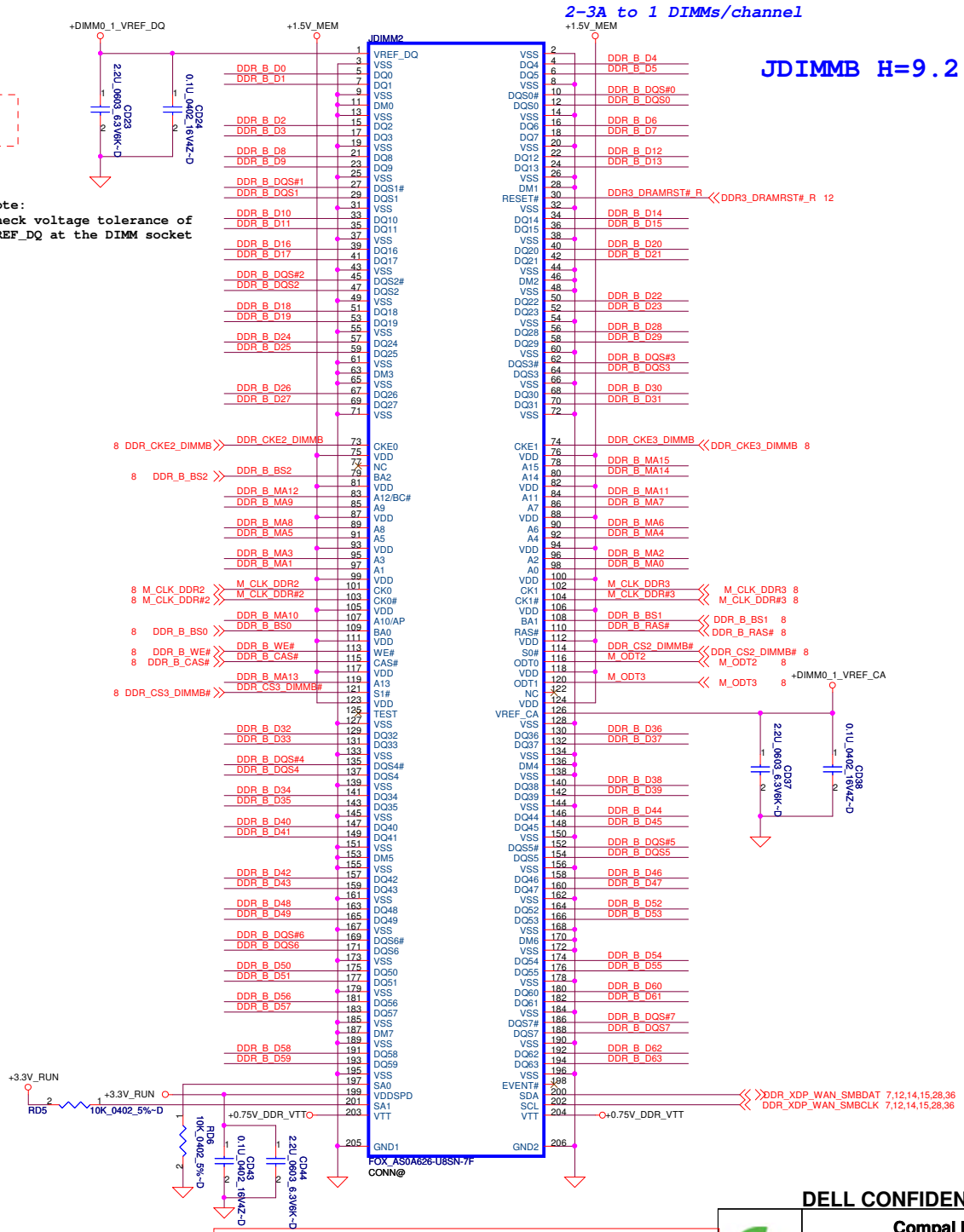
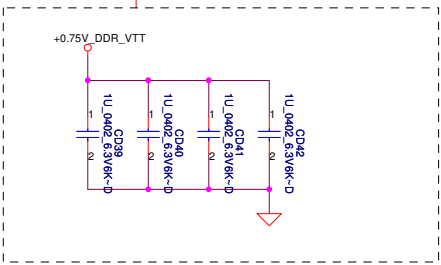
Populate RD4 for Intel DDR3 VREFDQ multiple methods M1

Note: Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note: Place near JDIMMB



Layout Note: Place near JDIMMB.203,204



JDIMMB H=9.2

2-3A to 1 DIMMs/channel

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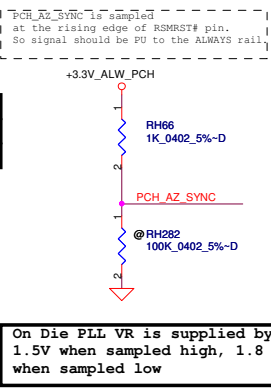


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File	DDRIII-SODIMM SLOT2		
Size	Document Number	Rev	
	LA-6591P	1.0	
Date:	Monday, January 10, 2011	Sheet	13 of 66

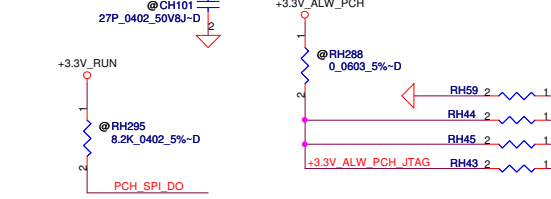
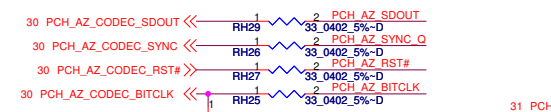
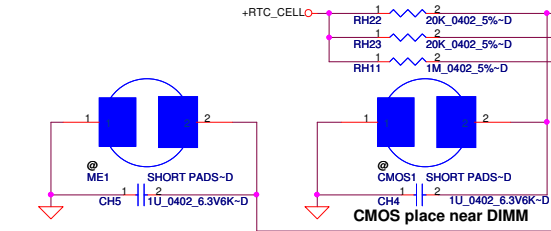
CMOS CLR1		CMOS setting	
Shunt	Clear CMOS		
Open	Keep CMOS		

ME CLR1		TPM setting	
Shunt	Clear ME RTC Registers		
Open	Keep ME RTC Registers		

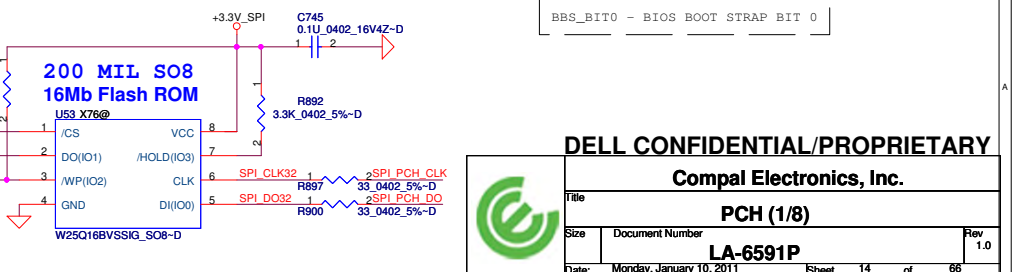
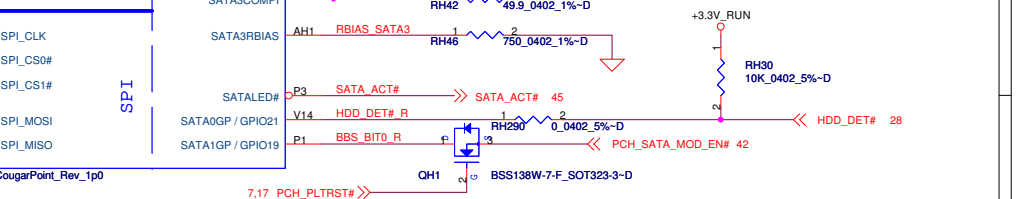
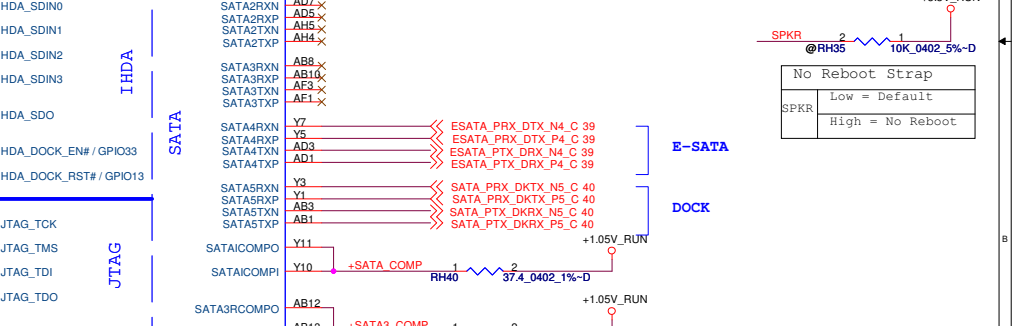
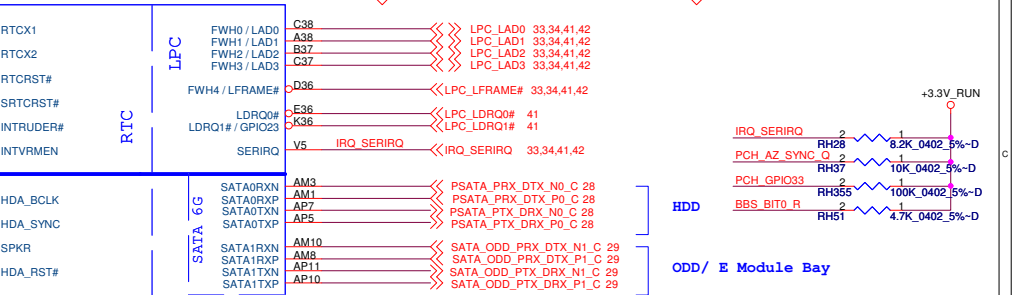
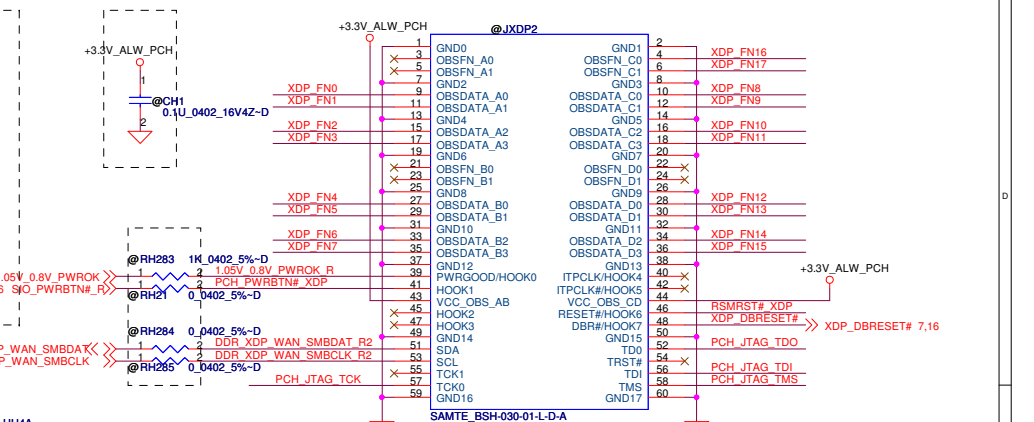
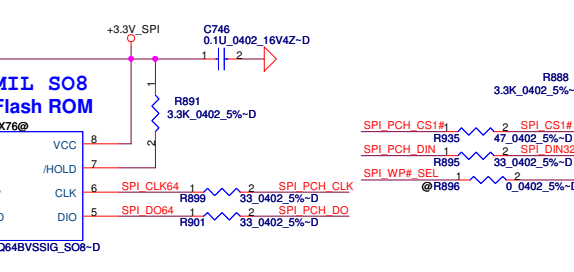
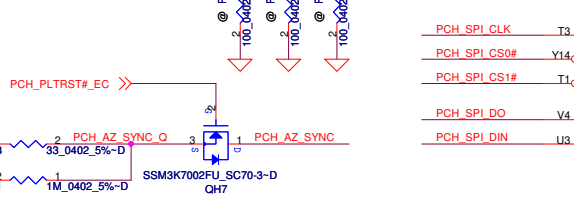
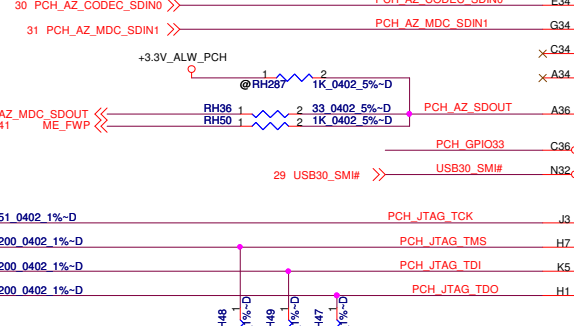
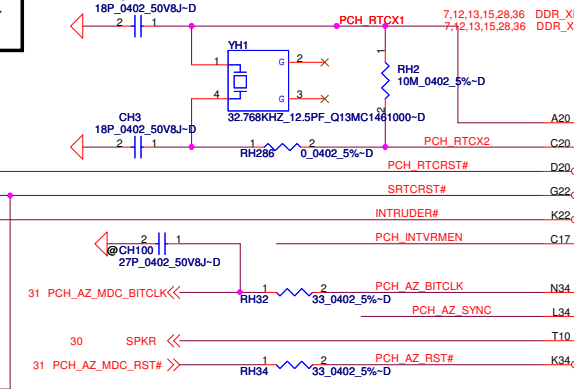
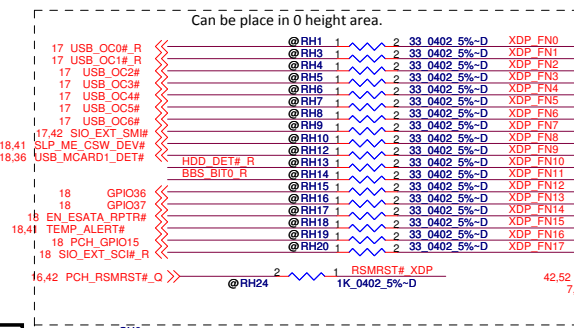
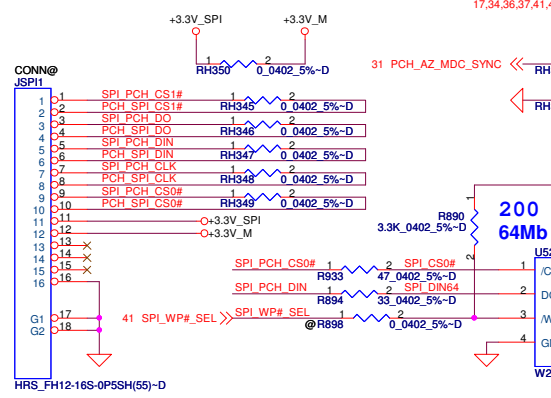


On Die PLL VR is supplied by 1.5V when sampled high, 1.8V when sampled low

INTVRMEN- Integrated SUS	
1.1V VRM Enable	
High	- Enable Internal VRs
Low	- Enable External VRs



High: Enable Intel Anti-Theft Technology
Left floating: Disable Intel Anti-Theft Technology



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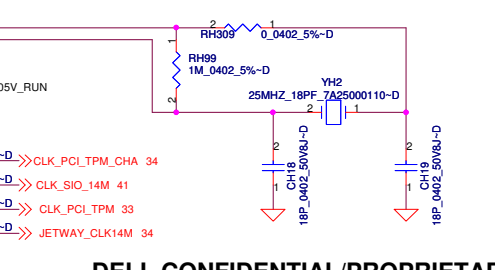
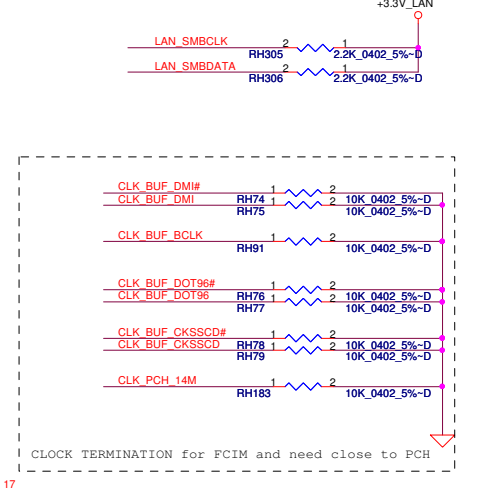
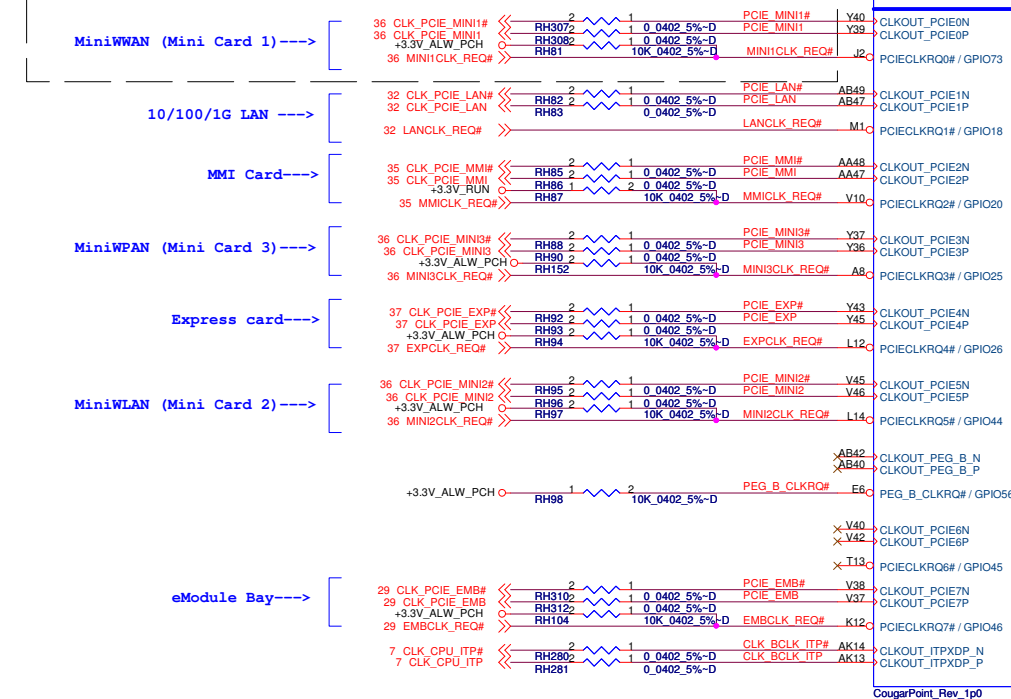
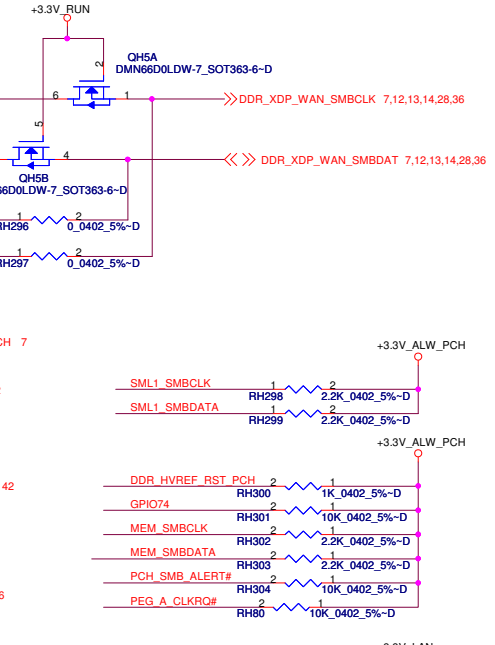
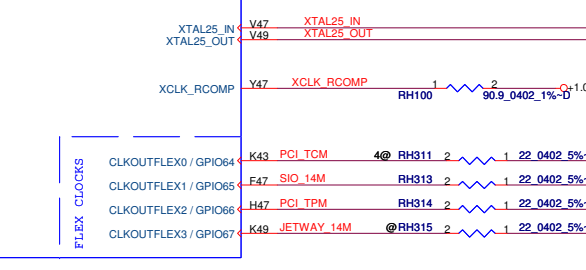
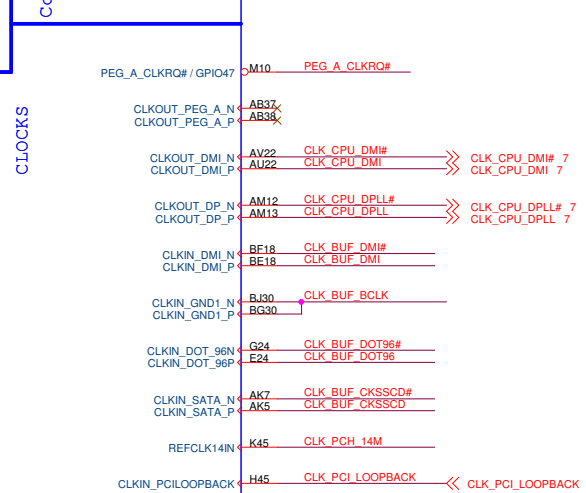
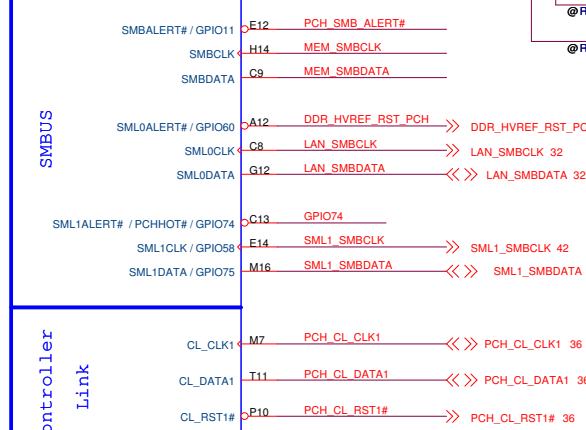
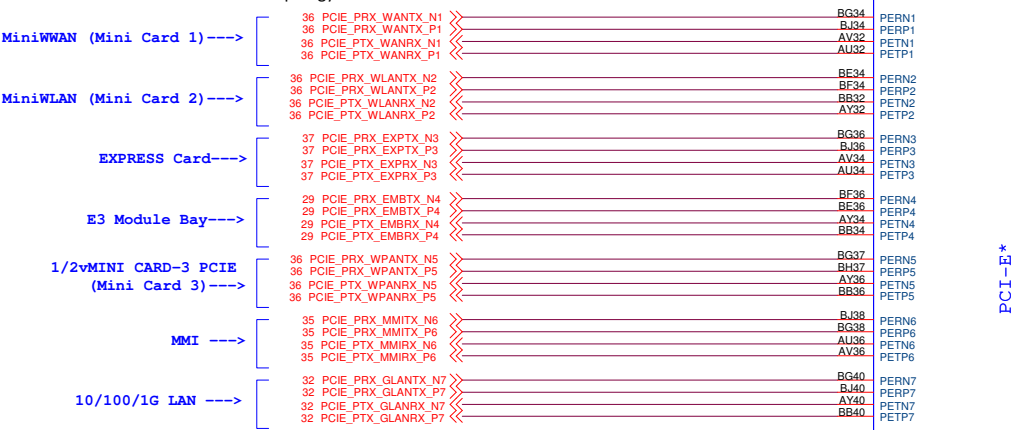
PCH (1/8)

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Follow DG0.9 Device down & Express/Mini card topology



PCIE REQ power rail:
suspend: 0 3 4 5 6 7
core: 1 2

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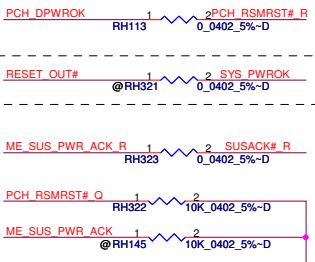
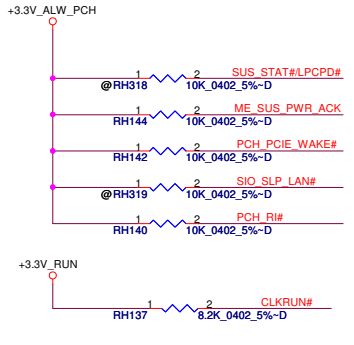
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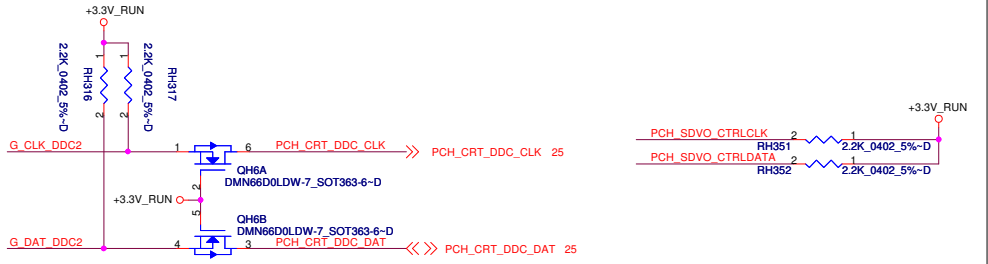
Title: PCH (2/8)

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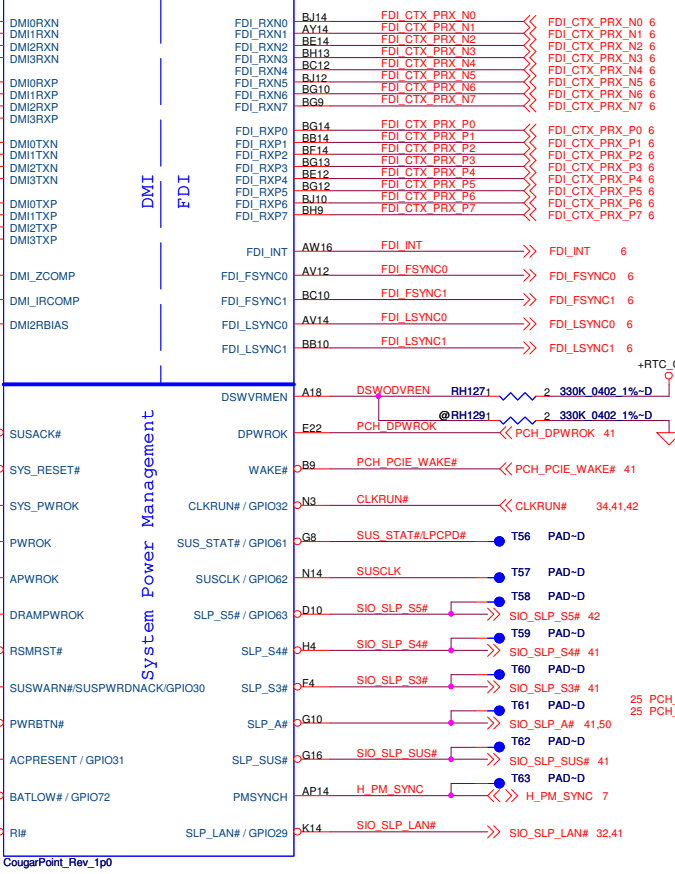


DSW0DVRN - On Die DSW VR Enable
 Enabled (DEFAULT)
 HIGH: R221 STUFFED,
 R222 UNSTUFFED
 Disabled
 LOW: R221 STUFFED,
 R222 UNSTUFFED



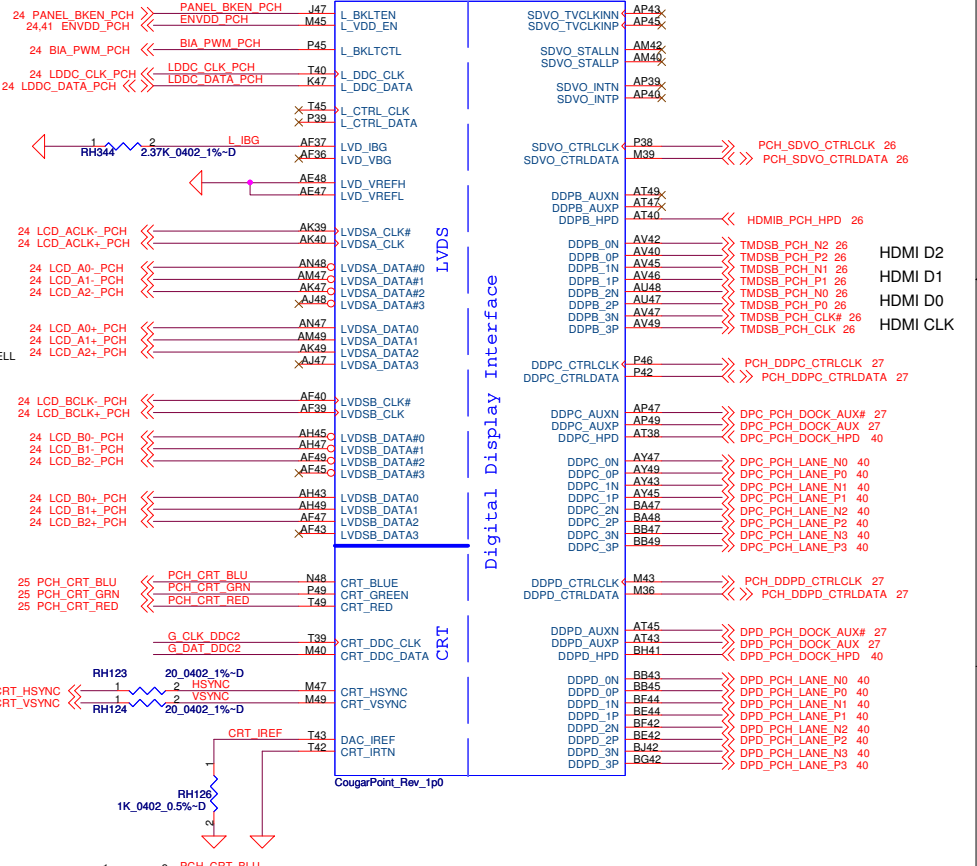
L_DDC_DATA - LVDS Detected	
1	LVDS is detected
0	LVDS is not detected

UH4C



CougarPoint_Rev_1p0

UH4D



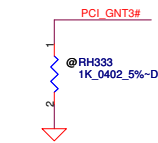
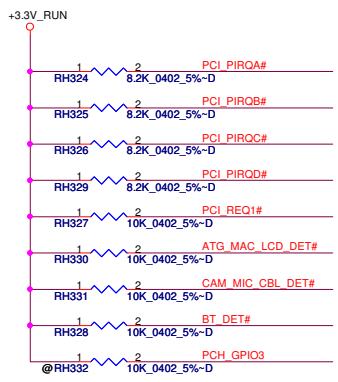
Intel request DDPB can not support eDP

Digital Display Interface

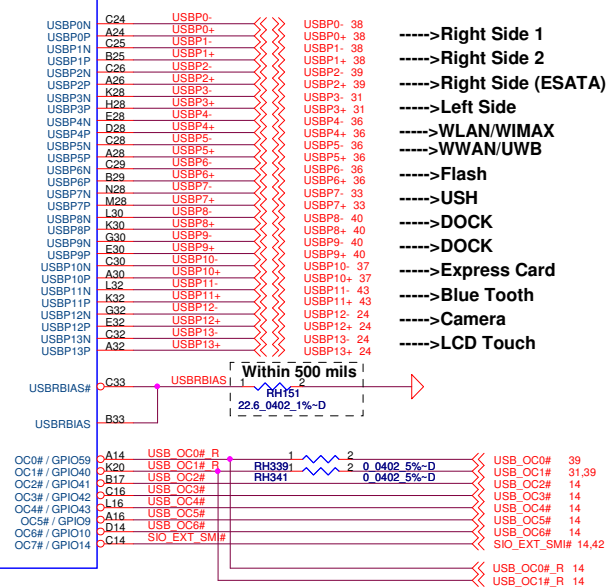
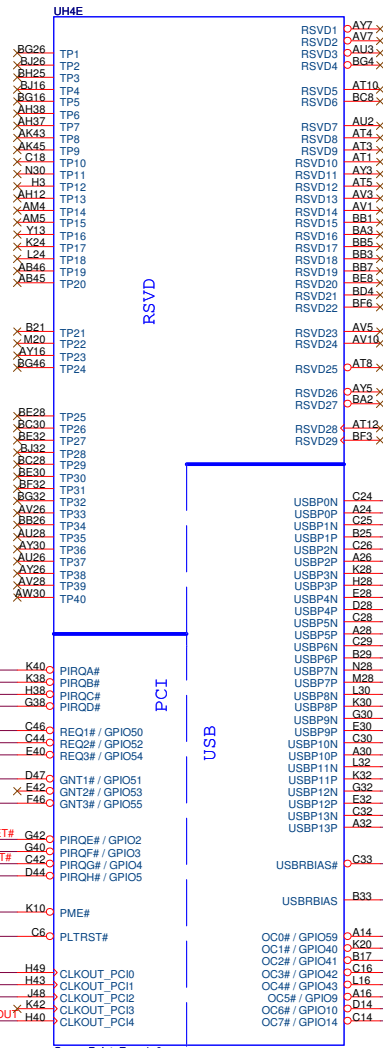
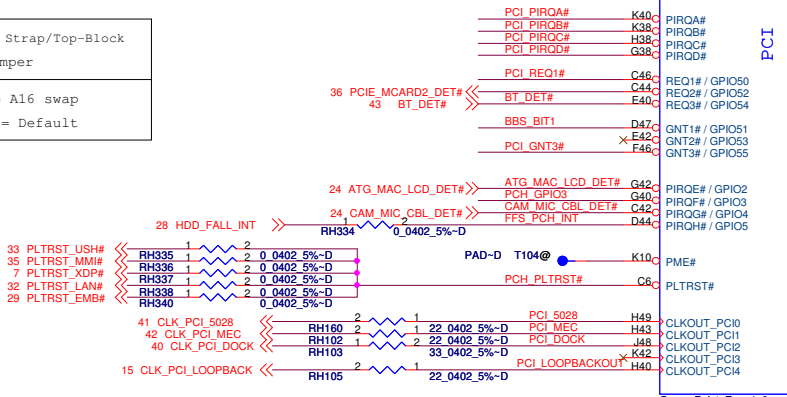


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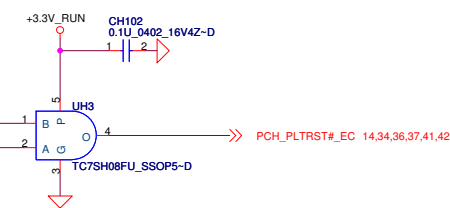
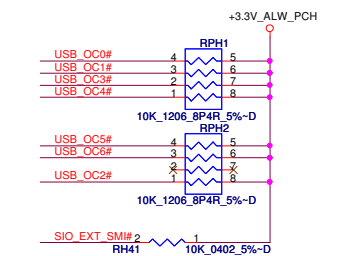
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PCH (3/8)		
Title	Document Number	Rev
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Date	Monday, January 10, 2011	Sheet 16 of 66



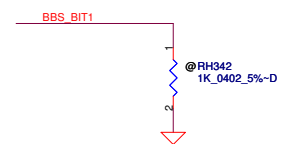
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default



- >Right Side 1
- >Right Side 2
- >Right Side (ESATA)
- >Left Side
- >WLAN/WIMAX
- >WWAN/UWB
- >Flash
- >USH
- >DOCK
- >DOCK
- >Express Card
- >Blue Tooth
- >Camera
- >LCD Touch



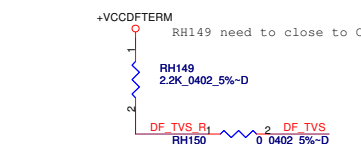
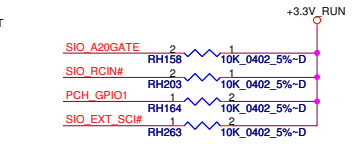
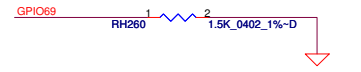
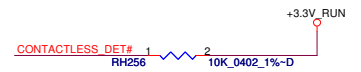
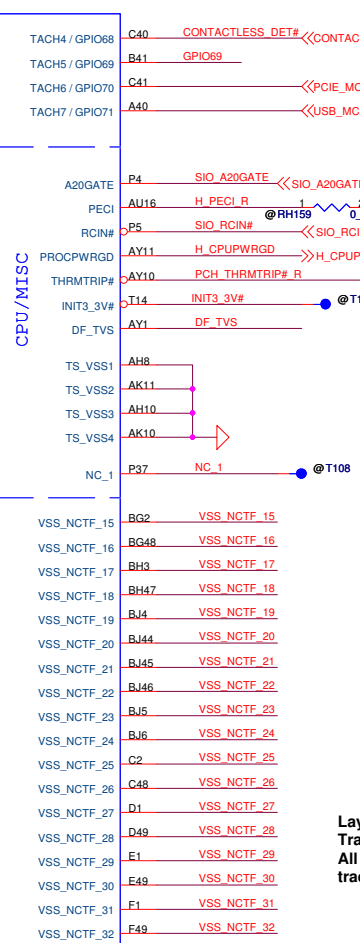
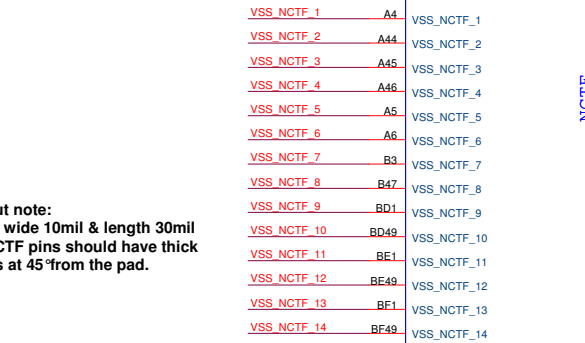
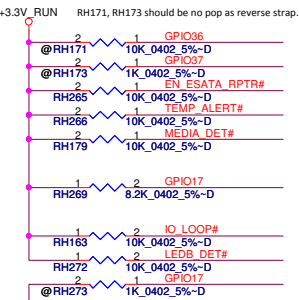
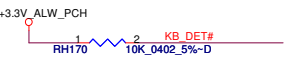
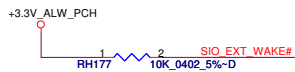
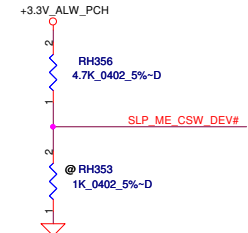
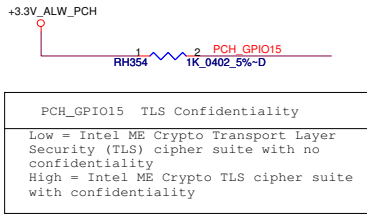
BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



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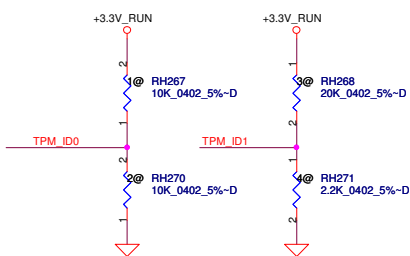
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Title: PCH (4/8)		
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DMI & FDI Termination Voltage	
DF_TVS	Set to Vss when LOW Set to Vcc when HIGH

Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.

Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
USH2.0	1	1

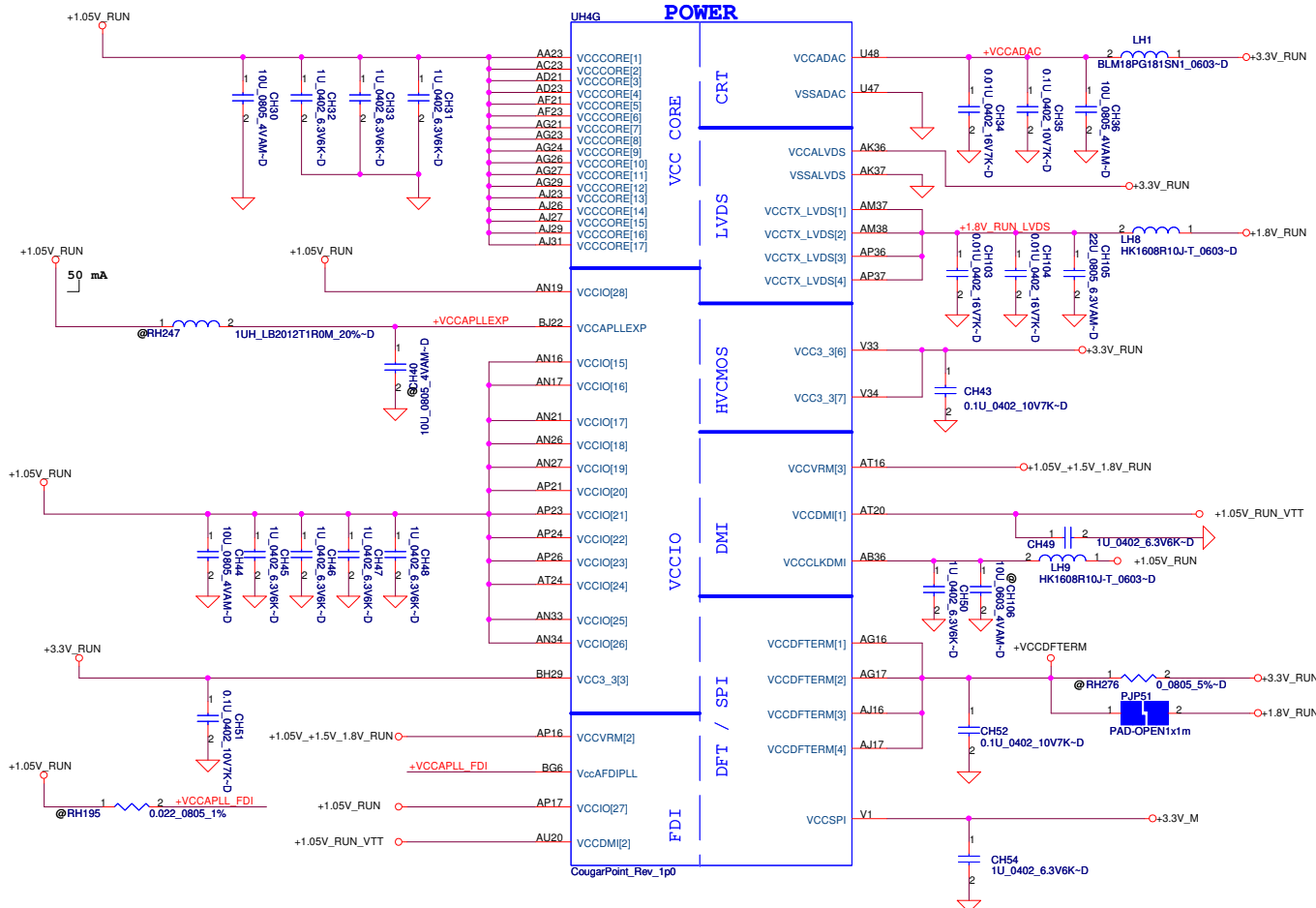
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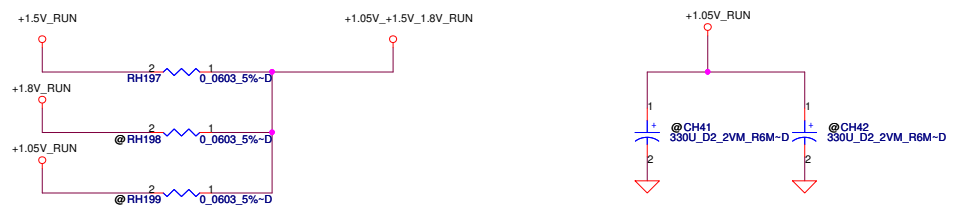
Title: **PCH (5/8)**

Size: **LA-6591P**

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PCH Power Rail Table		
Voltage Rail	Voltage	80 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.020
VccDSW3_3	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.119
VccSusHDA	3.3	0.01
VccVRM	1.8 / 1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06



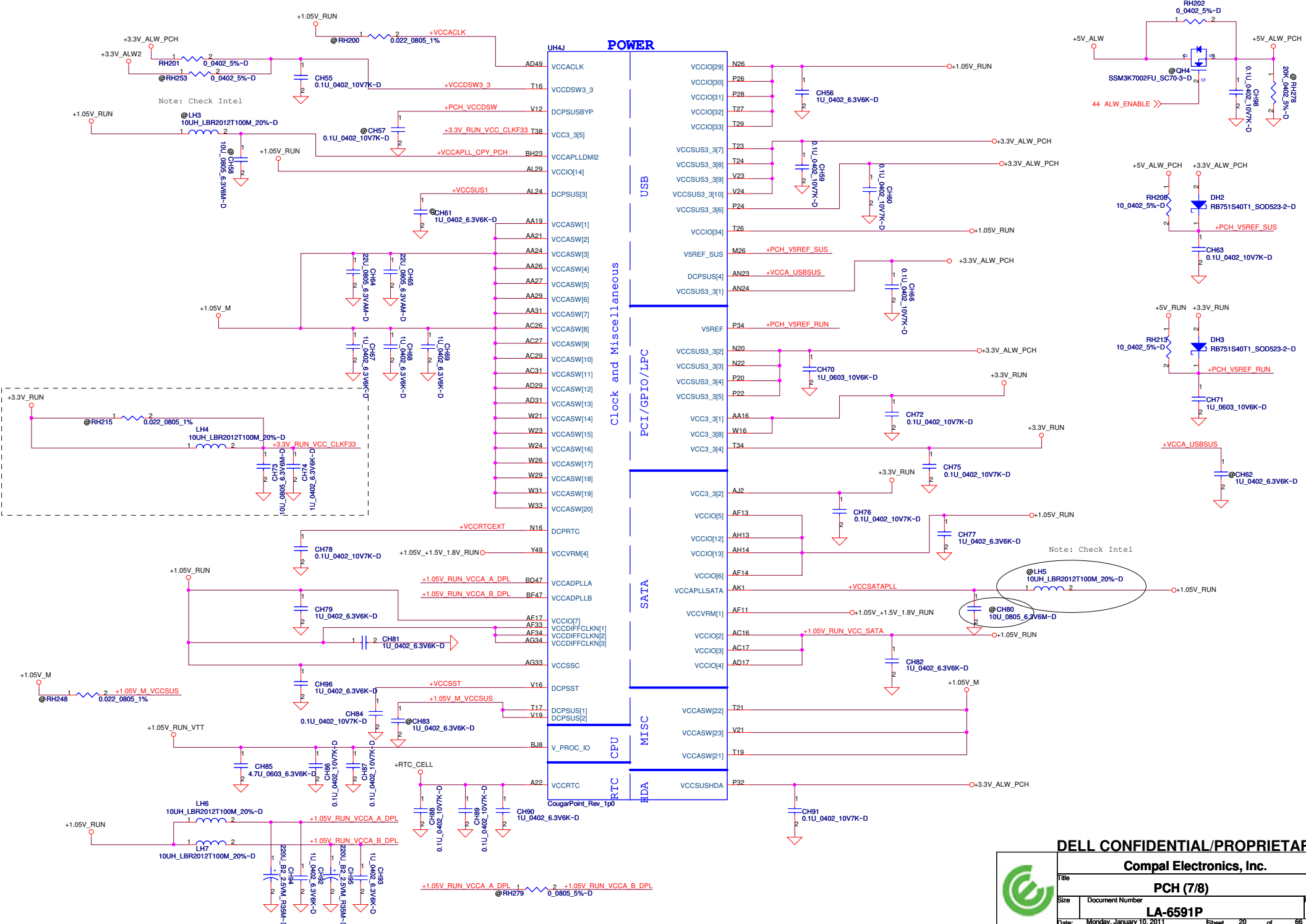
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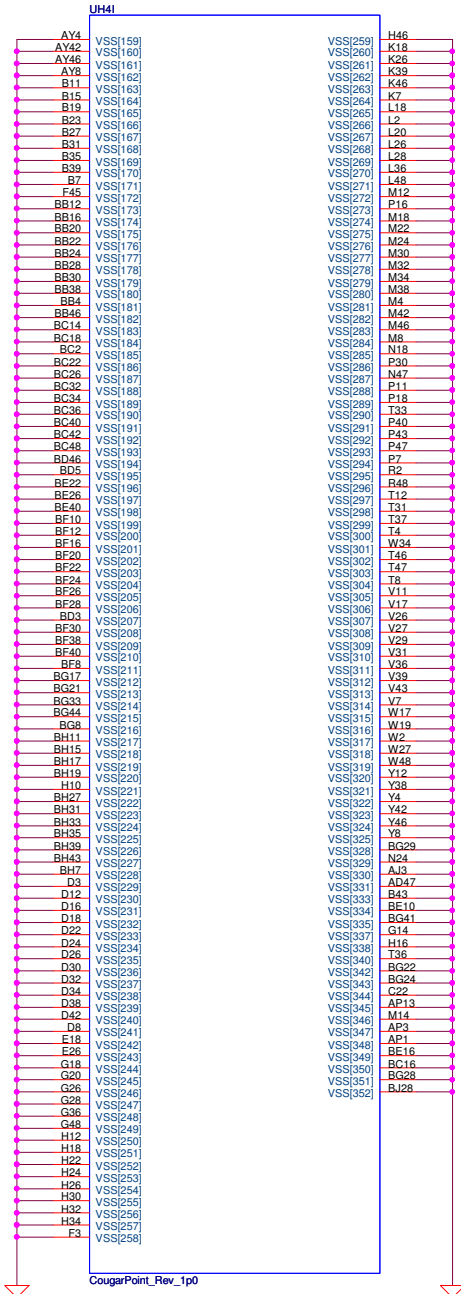
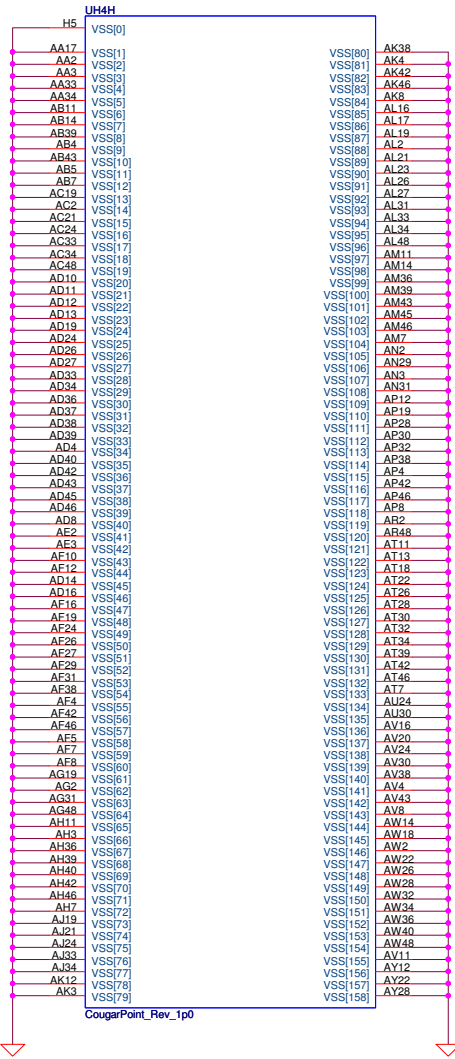
Compal Electronics, Inc.

Title PCH (6/8)		
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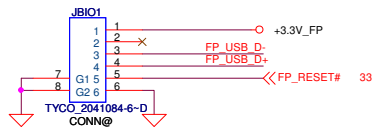
Compal Electronics, Inc.



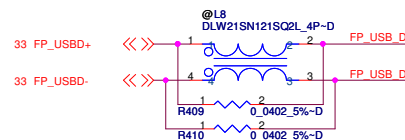
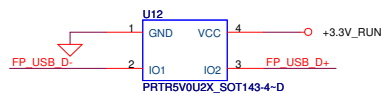
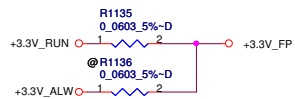
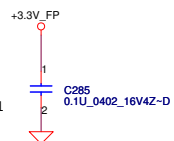
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Fingerprint CONN.



C285 Place close to JBIO1.1



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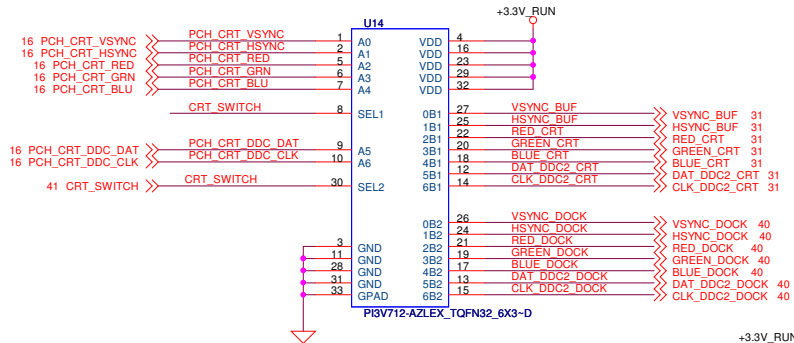


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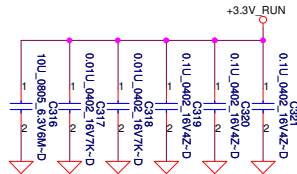
Compal Electronics, Inc.

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VGA SW for MB/DOCK

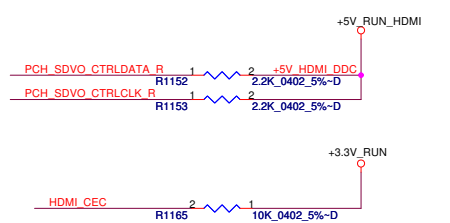
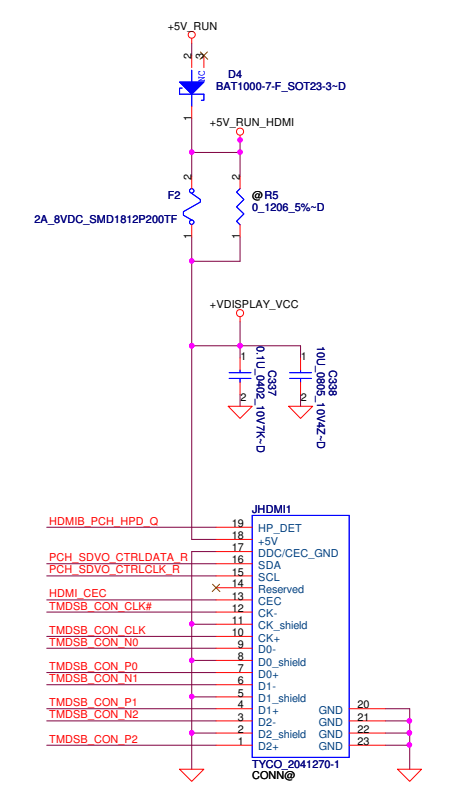
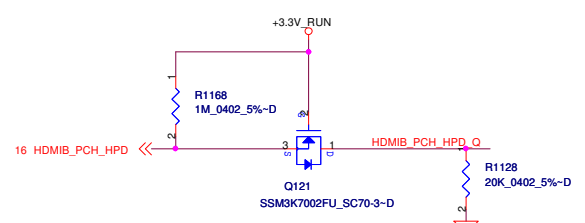
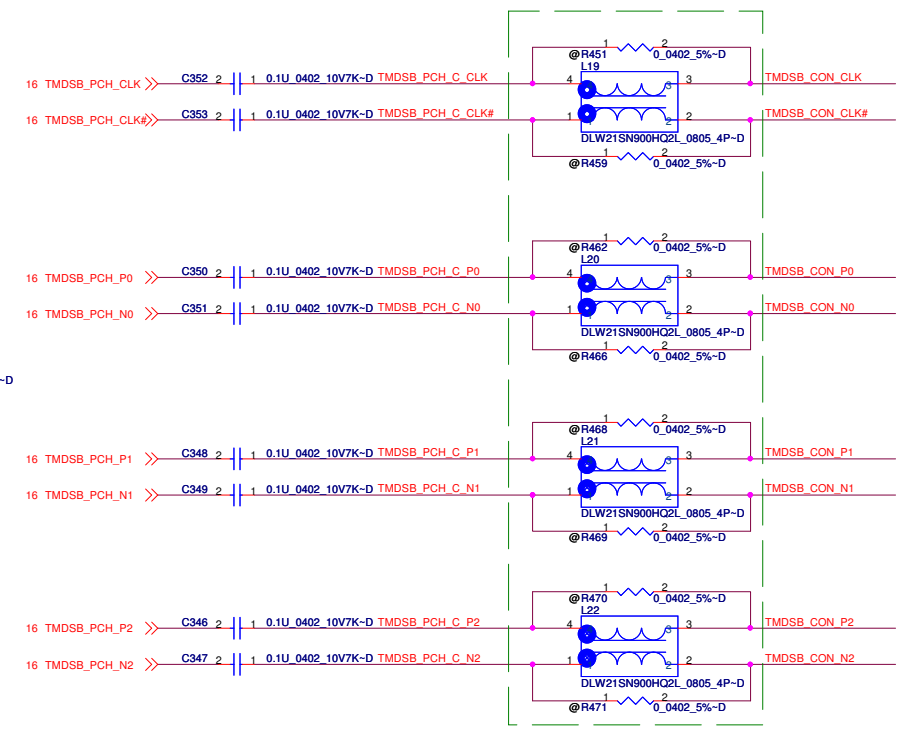
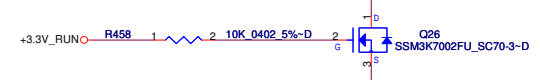
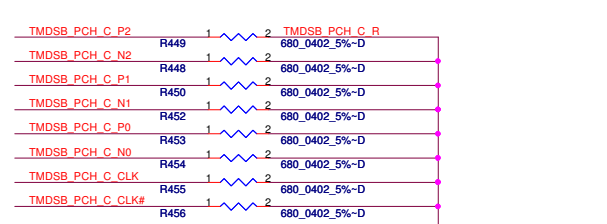


SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR



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	CRT/Video switch		
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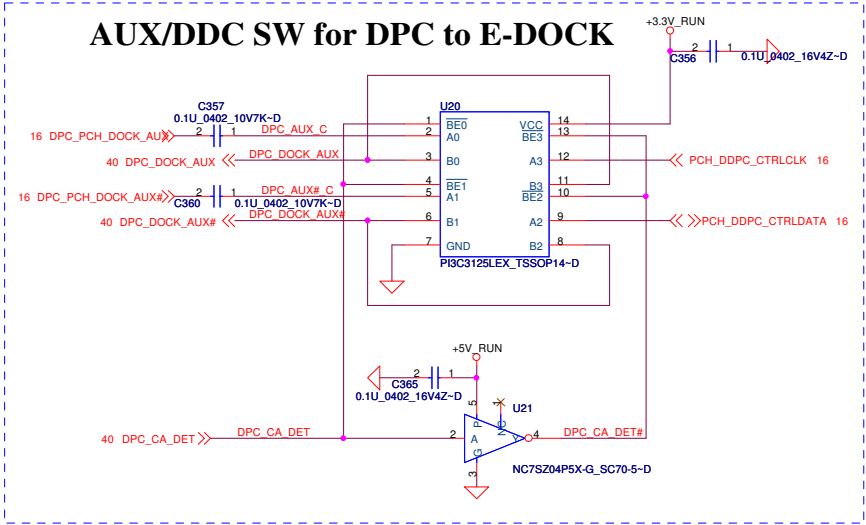
HDMI port

LA-6591P

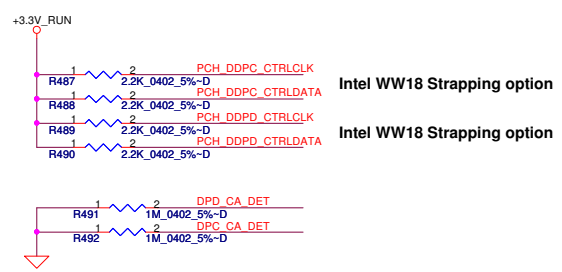
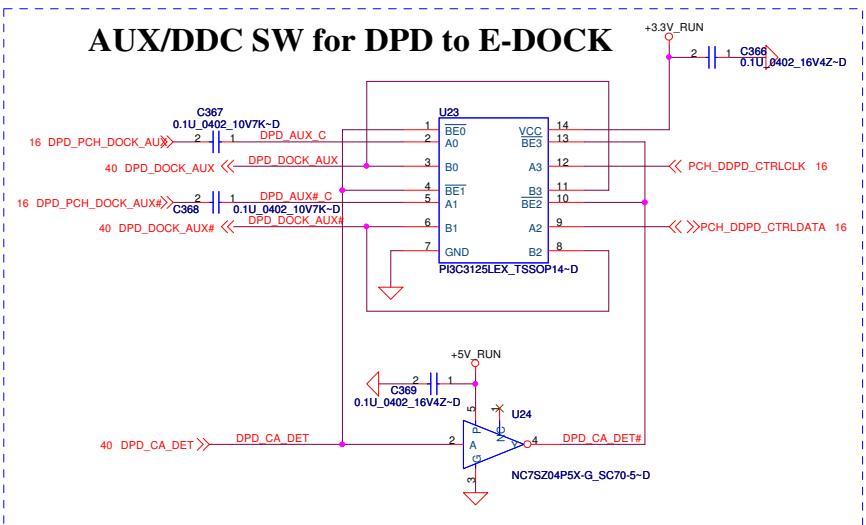
Size: Document Number
Date: Monday, January 10, 2011

Rev: 1.0
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AUX/DDC SW for DPC to E-DOCK



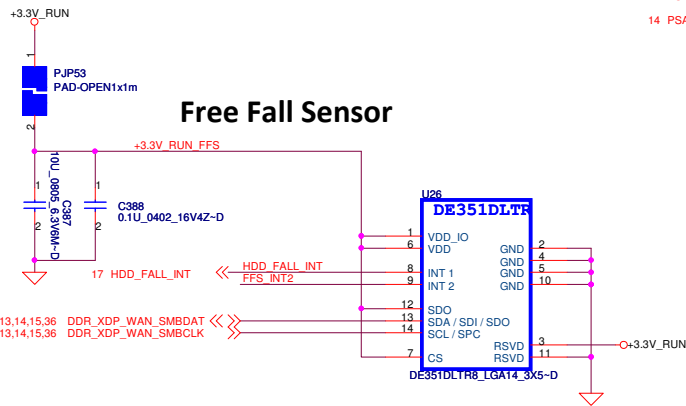
AUX/DDC SW for DPD to E-DOCK



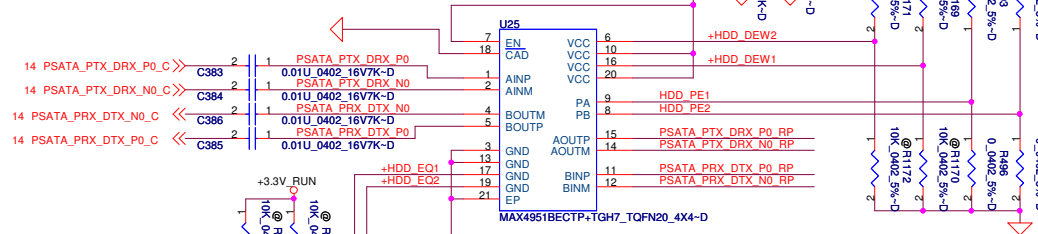
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Title DP122/DP512			
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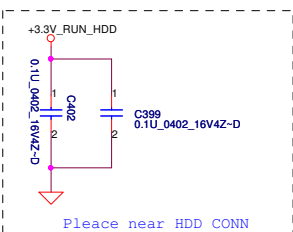
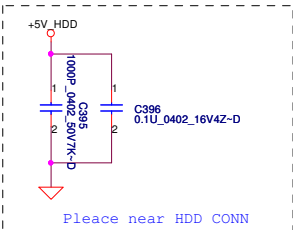
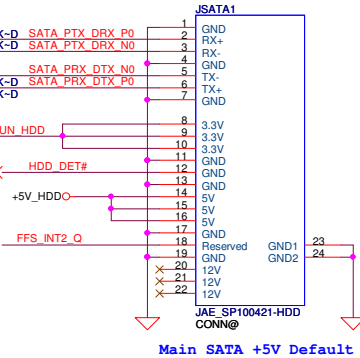


HDD Repeater

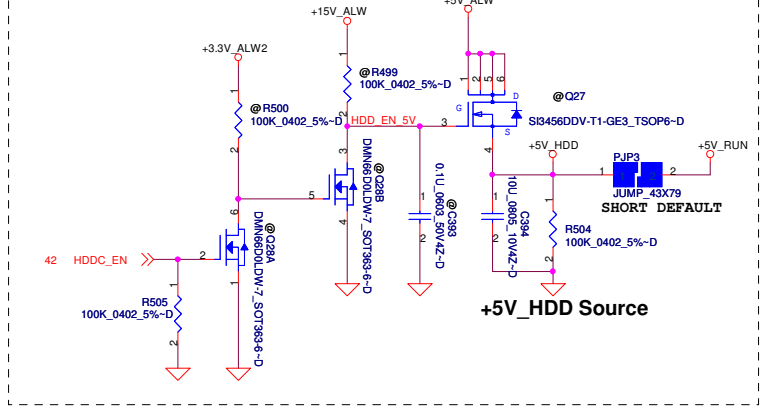


Note: +HDD_DEW1, +HDD_DEW2, +HDD_EQ1, +HDD_EQ2 need to route 10 mils and R1169, R1171, R1174, R1176 need to change to 10k and no stuff R1174, R1176 to support TI SN75LVCP601

For HDD Temp.



HDD PWR

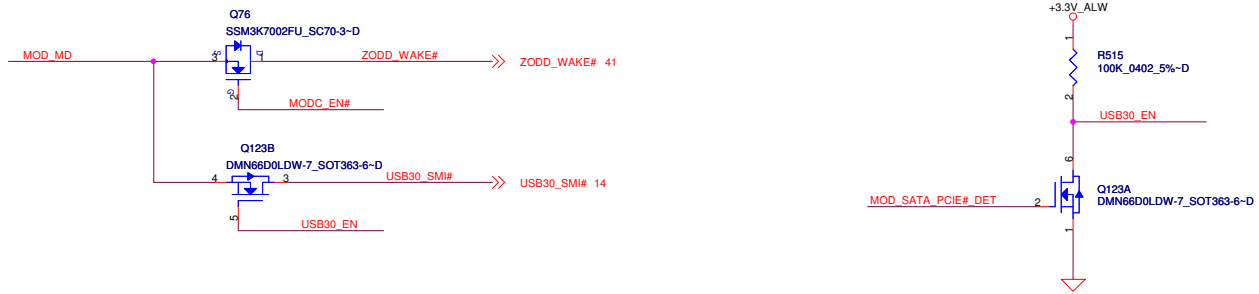
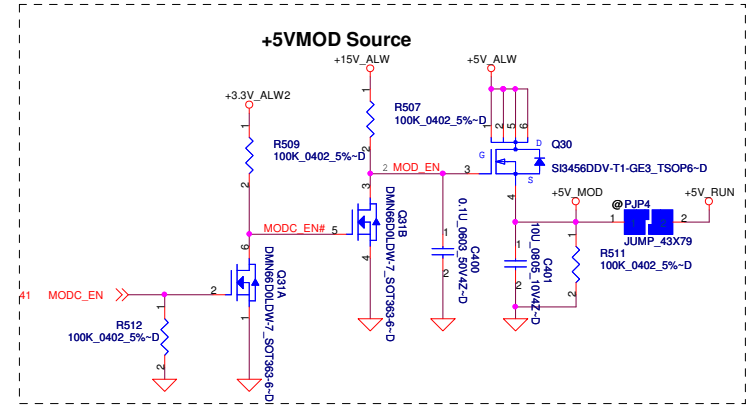
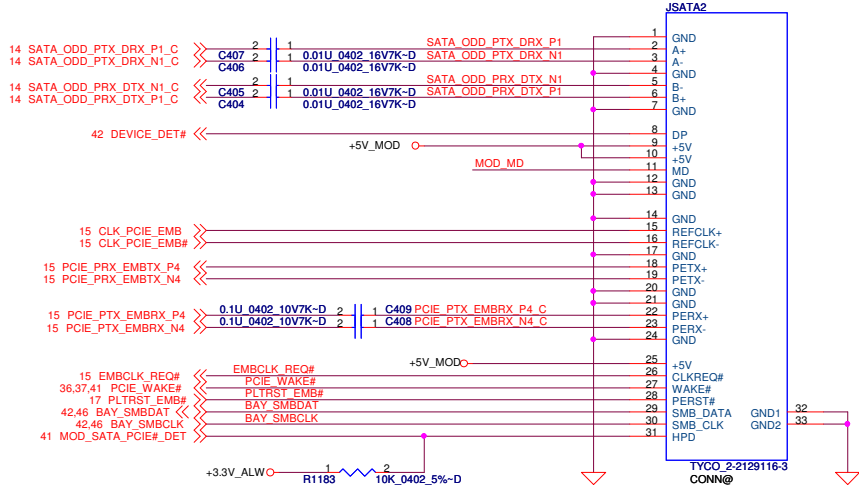
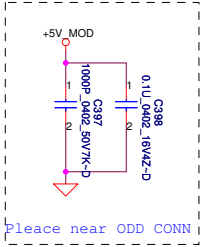
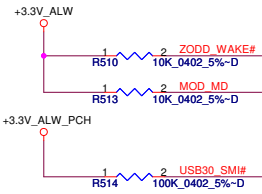


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HDD CONNECTOR		
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For ODD

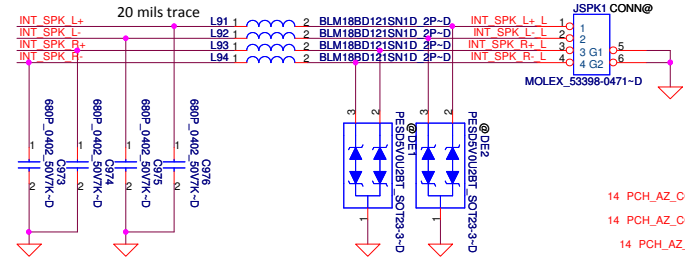


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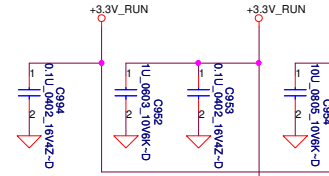
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 Title: **ODD CONNECTOR**
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 Rev 1.0

Internal Speakers Header

Speaker Connector

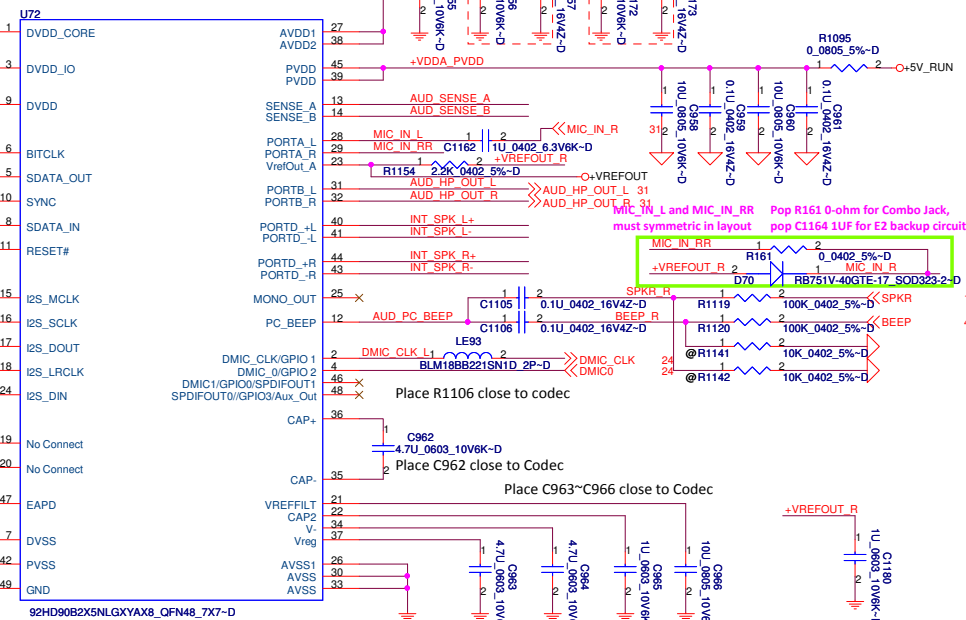


DVDD_IO should match with HDA Bus level



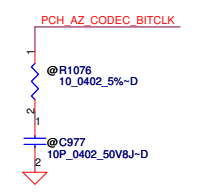
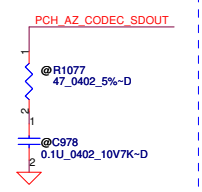
Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

Place C951~C961 close to Codec

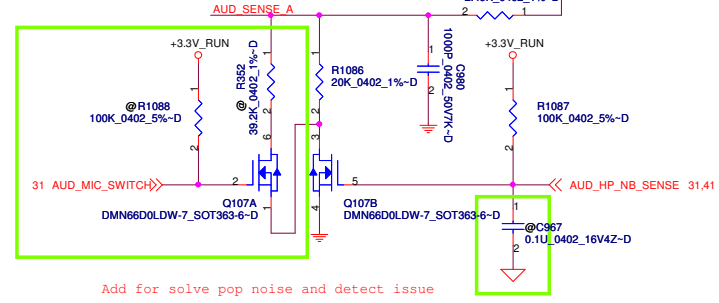


Close to U16 pin5

Close to U16 pin6

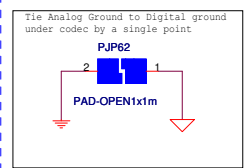
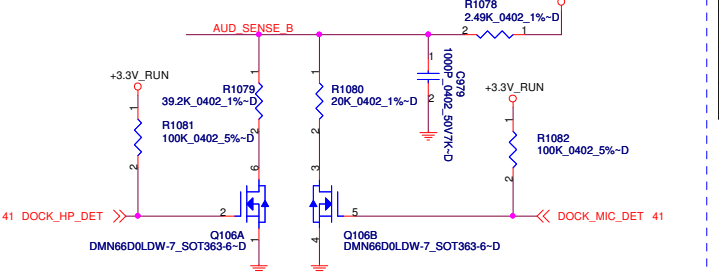


Place closely to Pin 13.



Add for solve pop noise and detect issue

Place closely to Pin 14



PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Dock Audio
PORT D	Internal SPK

Resistor	SENSE_A	SENSE_B
39.2K	PORT A (HP0)	PORT E
20K	PORT B (HP1)	PORT F
2.49K	Pull-up to AVDD	

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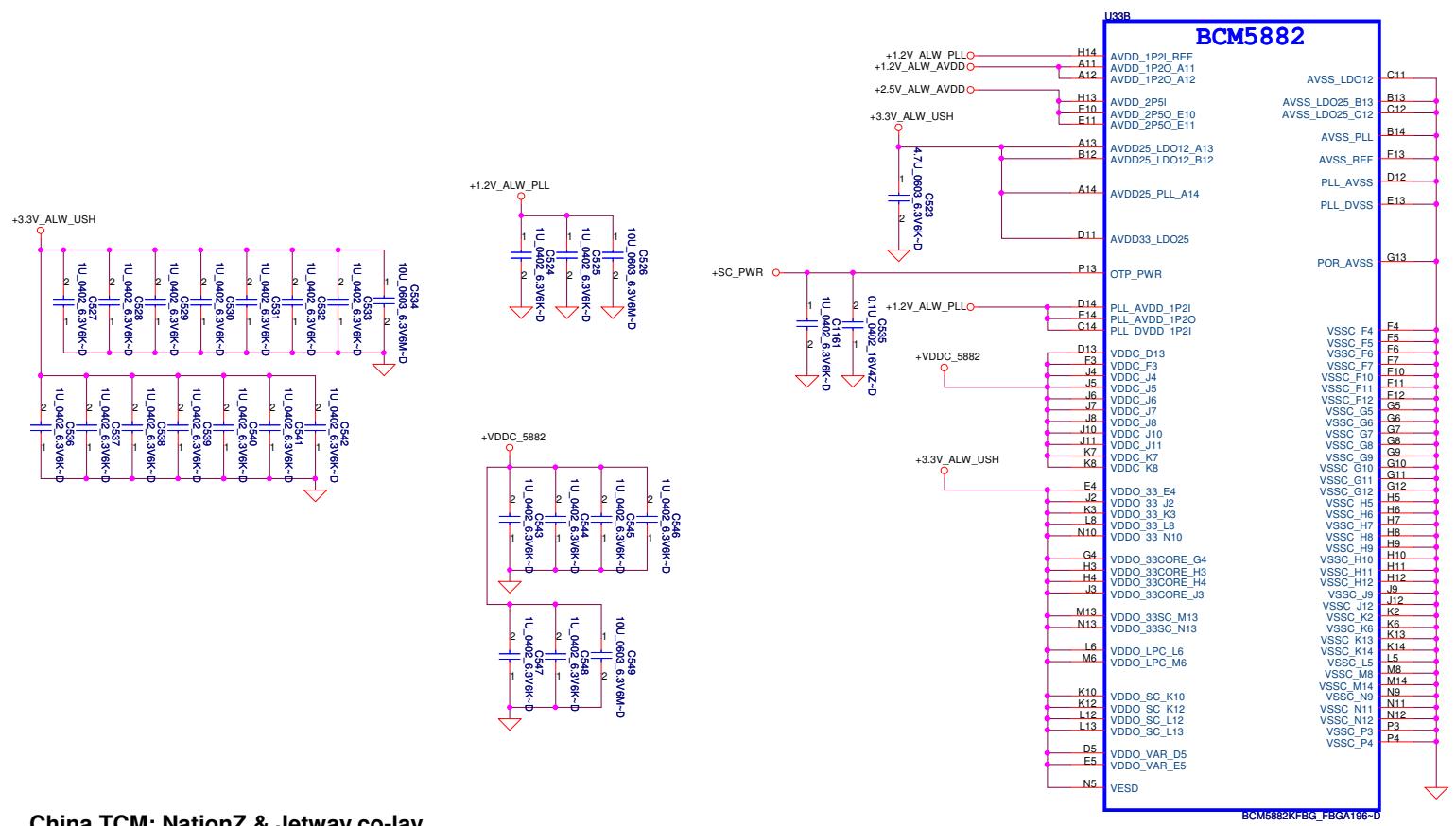
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Azalia (HD) Codec

LA-6591P

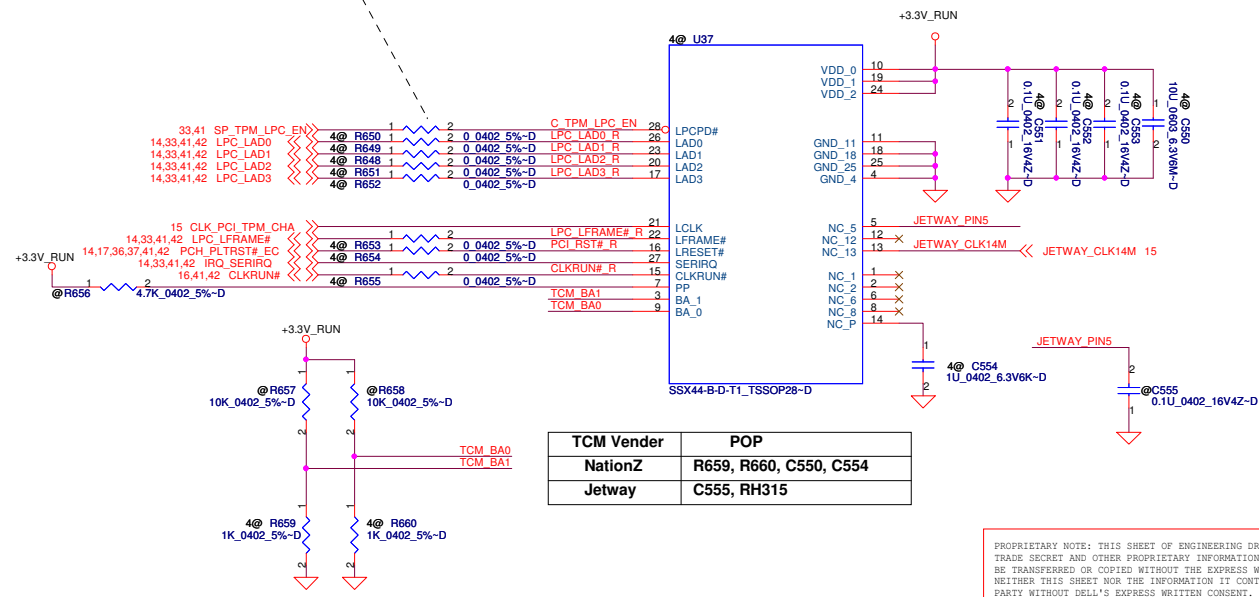
Monday, January 10, 2011

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LOW:Power Down Mode
High:Working Mode

China TCM: NationZ & Jetway co-lay



TCM Vender	POP
NationZ	R659, R660, C550, C554
Jetway	C555, RH315

USH BCM5882 and China TCM Z8H172T Option				
PART/PIN	Ref Des	TCM Enable	TPM Enable	ALL TPM/TCM Disable
TCM circuit	All 4@	POP	@	@
USH_LPCEN	PU R583 PD R615	@ POP	POP @	@ @
SIO 5028 ->SP_TPM_LPC_EN	PU R772	@	@	@
PCH GPIO39 ->TPM_ID1	PU RH268 PD RH271	@ POP	POP @	POP @
PCH GPIO38 ->TPM_ID0	PU RH267 PD RH270	@ POP	POP @	POP POP

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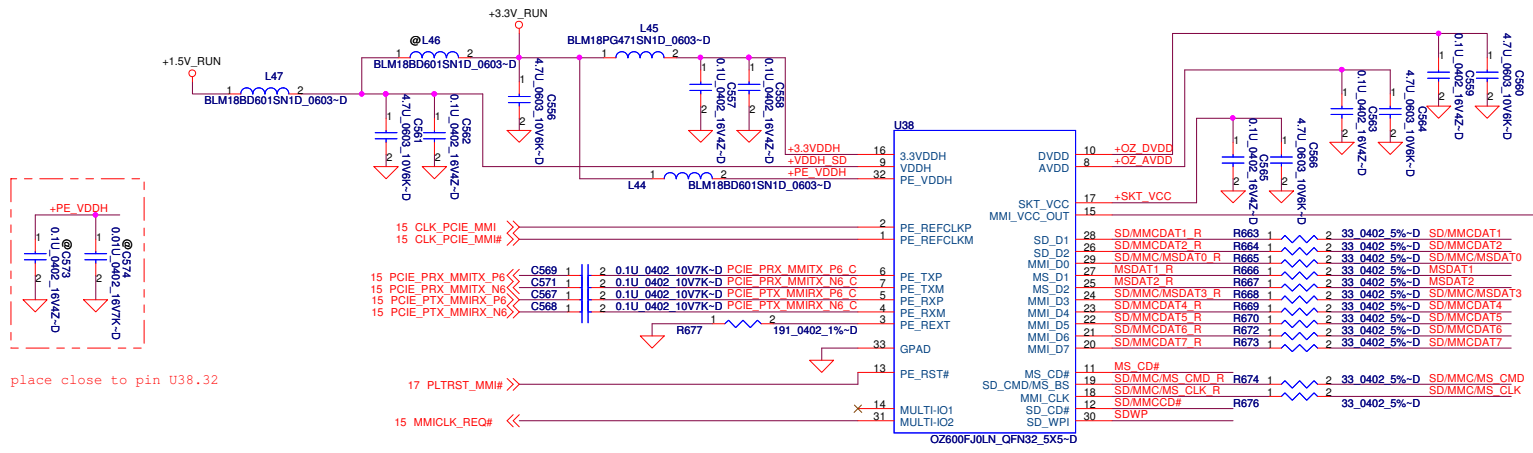
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USH BCM5882 (2/2)

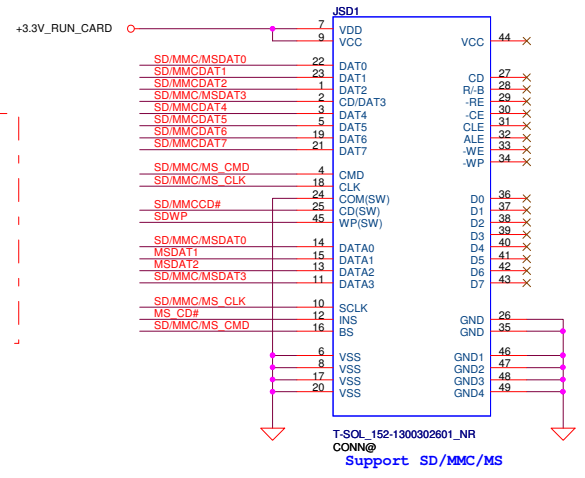
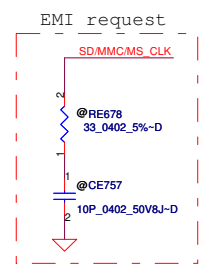
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place close to pin U38.32

Note: The trace need to route as daisy-chain and the trace of SD signals need to route as short as possible



T-SOL_152-1300302601_NR
CONN@
Support SD/MMC/MS

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Card Reader OZ600FJ0

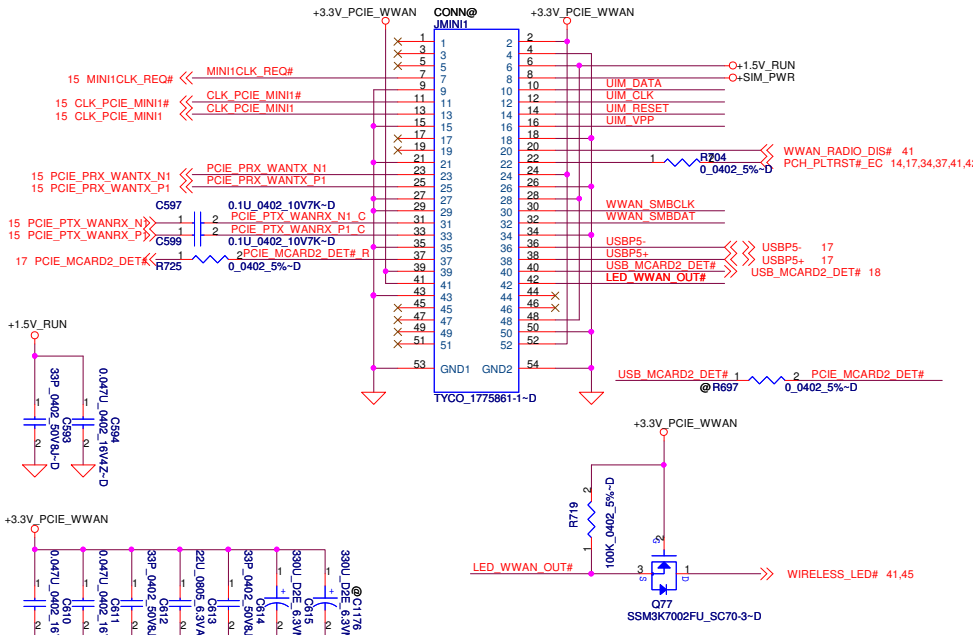
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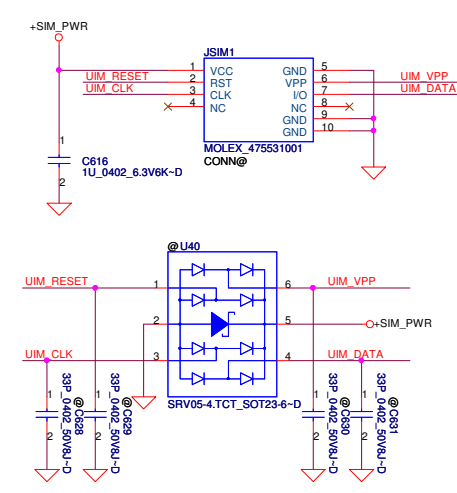
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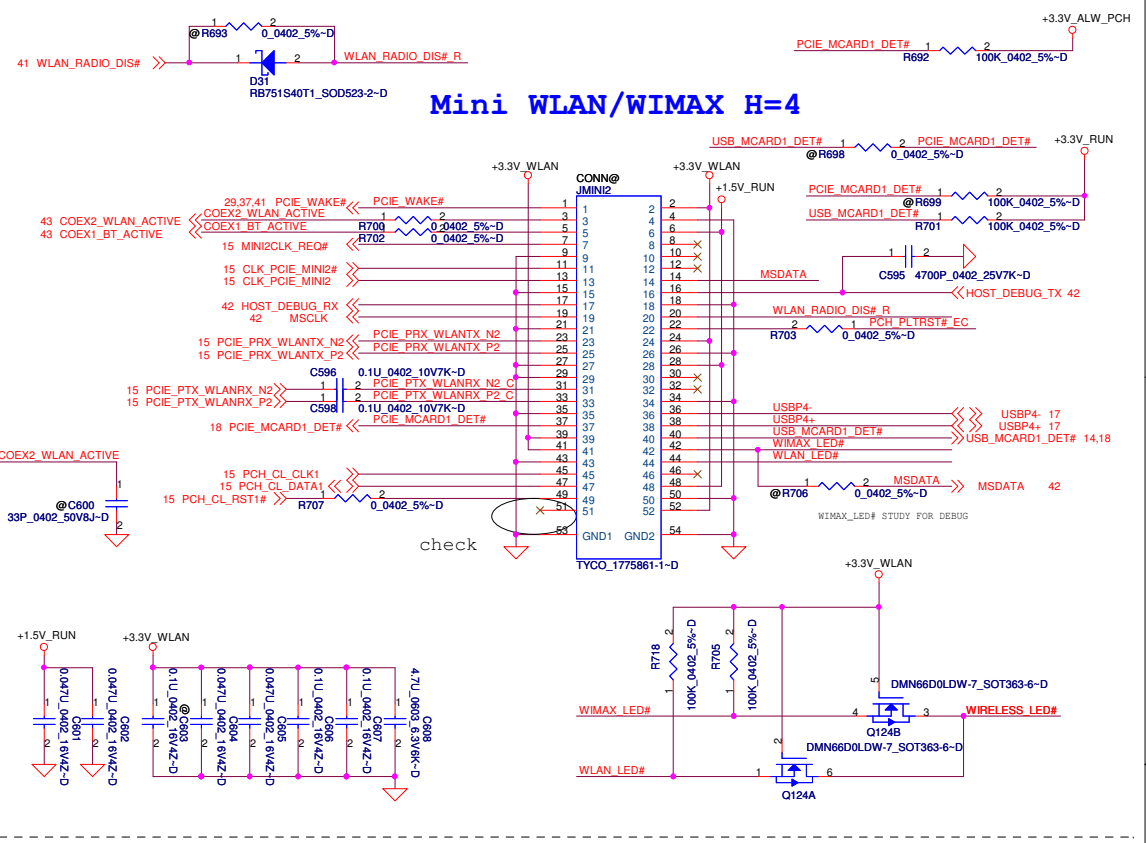
Mini WWAN/GPS/LTE/UWB H=5.2



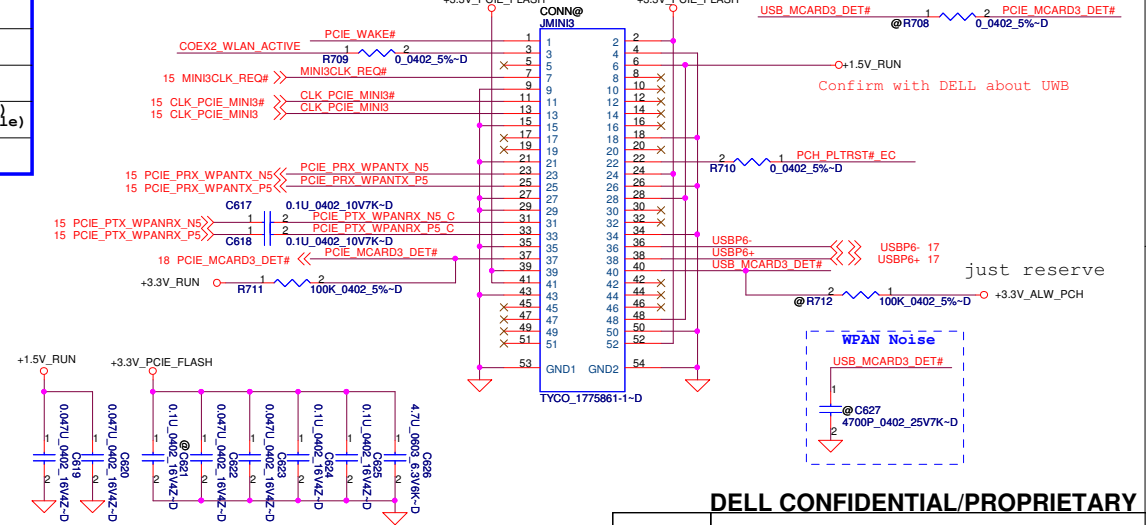
SIM Card Push-Push



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+~9%	1000	750	
+3.3Vaux	+~9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+~5%	500	375	NA



1/2 Minicard Flash Card H=4



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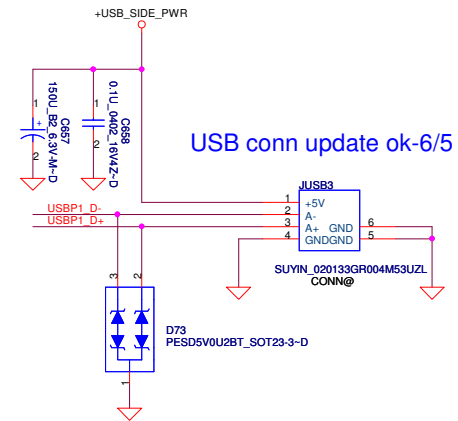
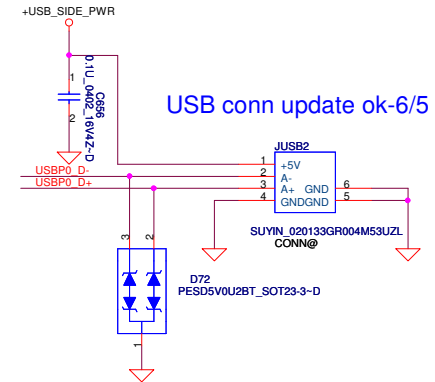
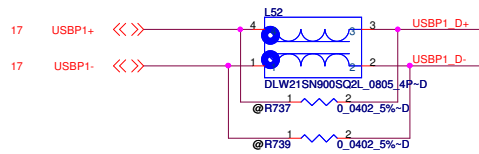
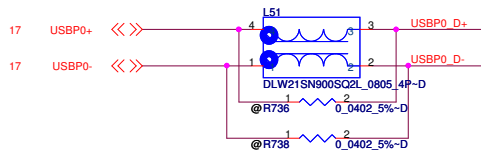
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Mini Card

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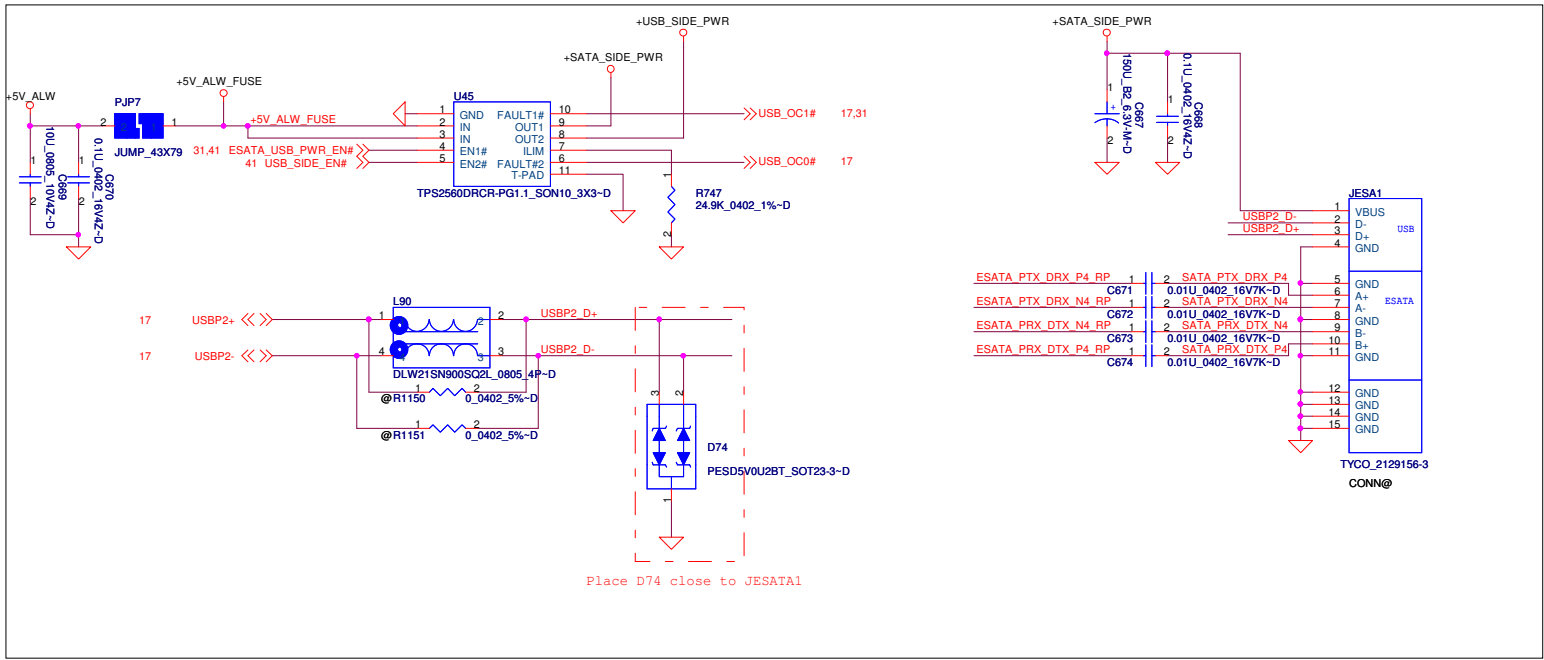
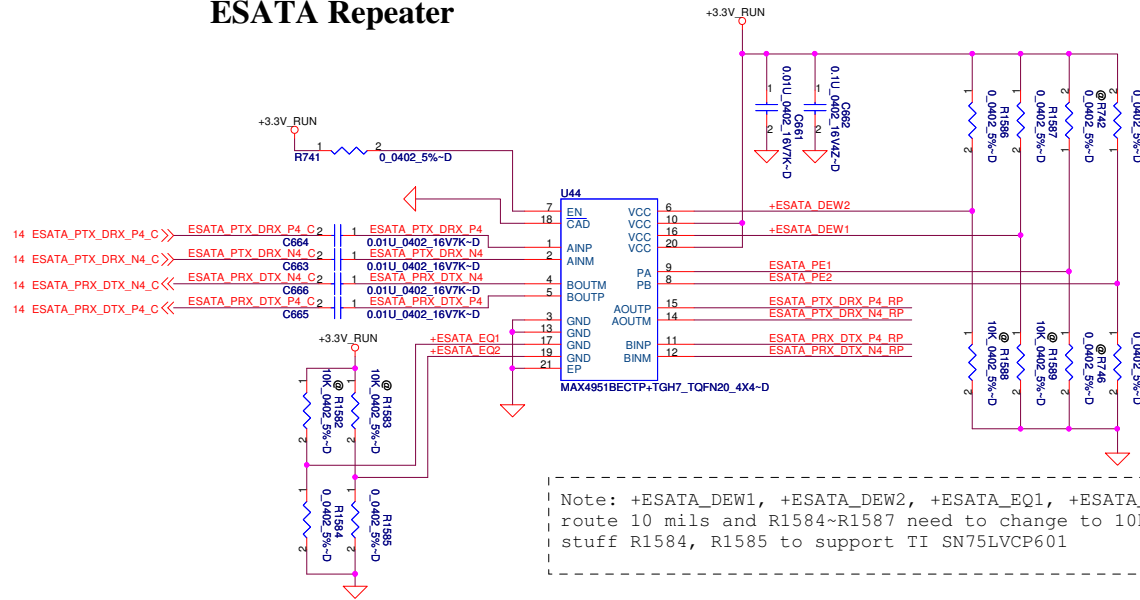


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ESATA Repeater



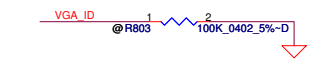
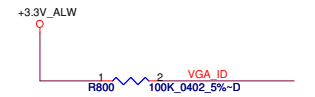
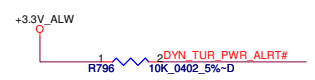
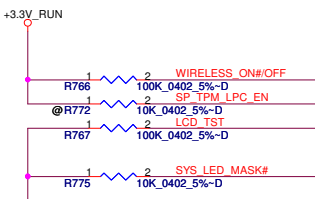
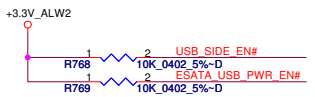
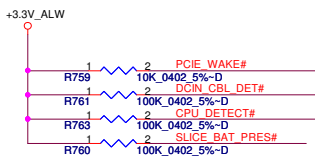
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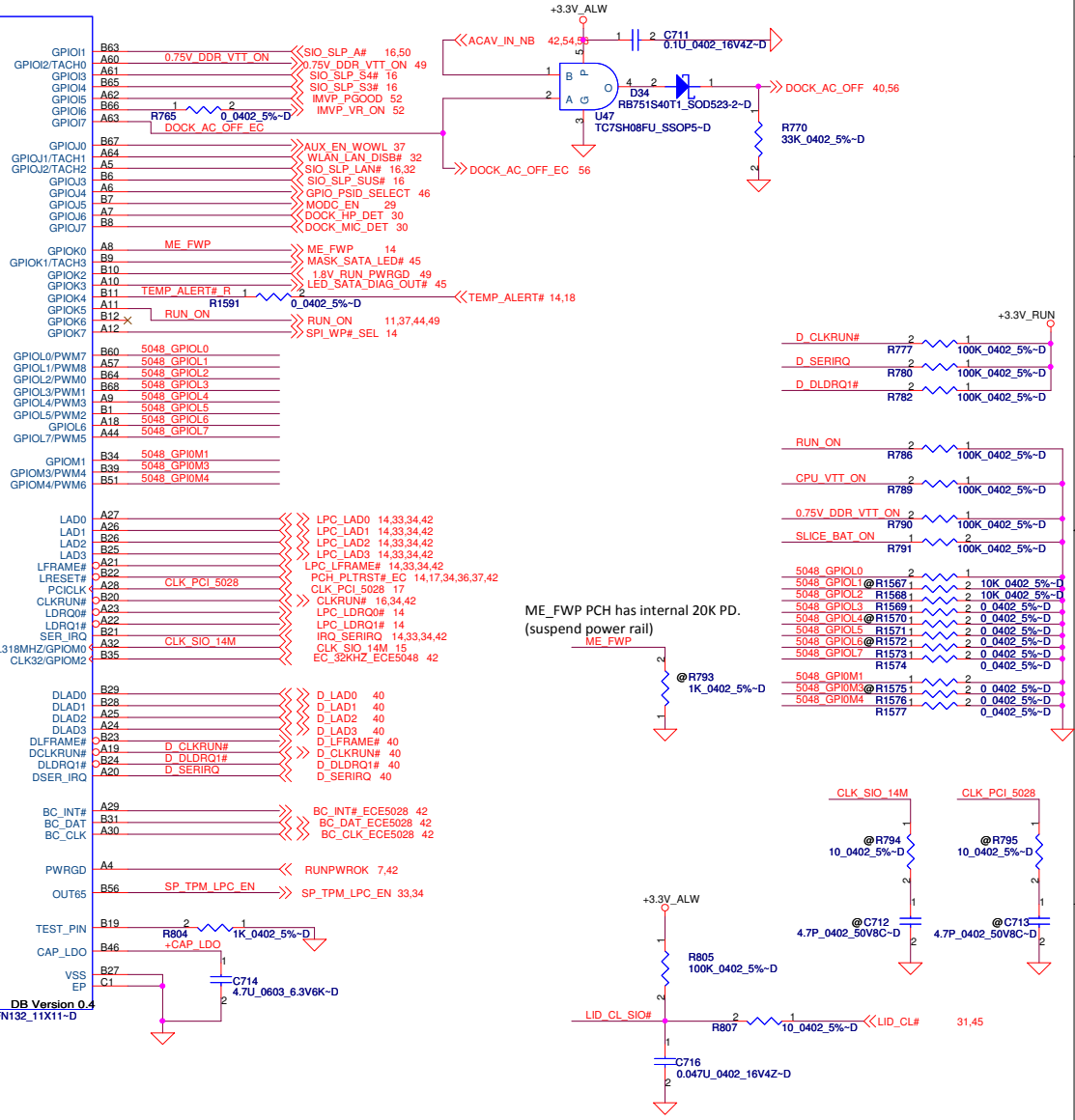
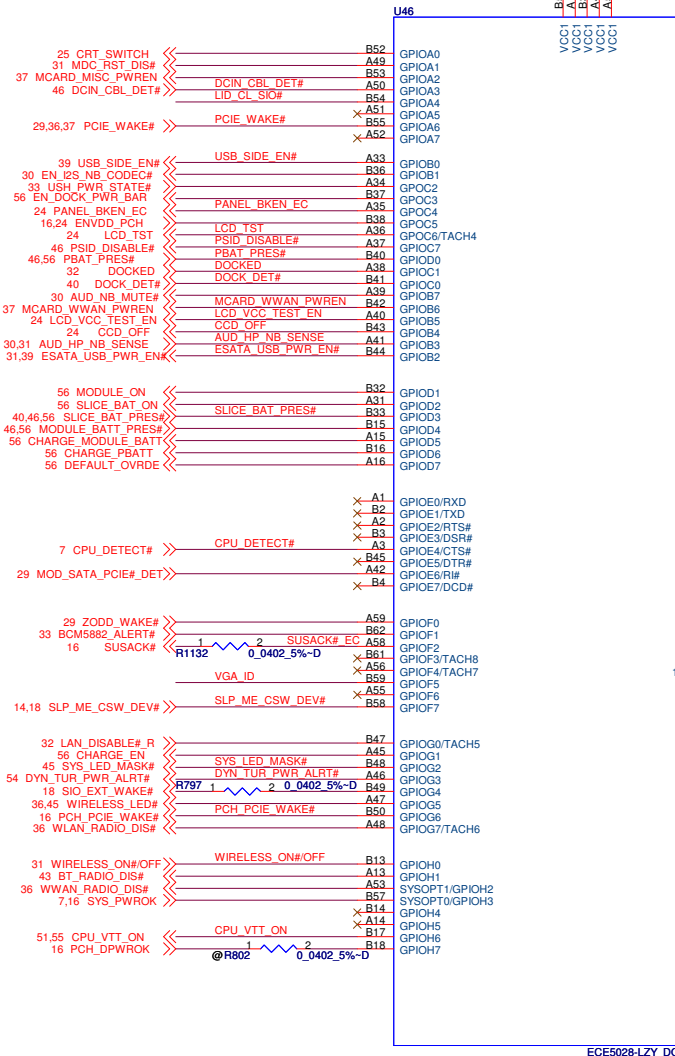


Title		USB/ESATA/IO/MDC	
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	VGA_ID
Discrete	0
UMA	1



DB Version 0.4
ECE5028-LZY_DQFN132_11X11-D

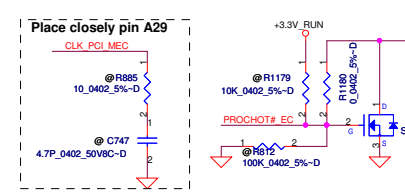
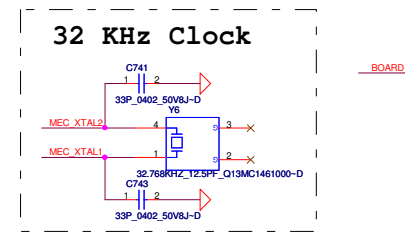
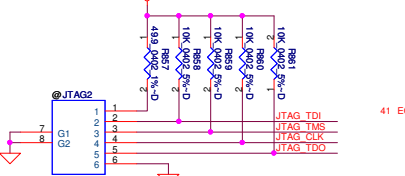
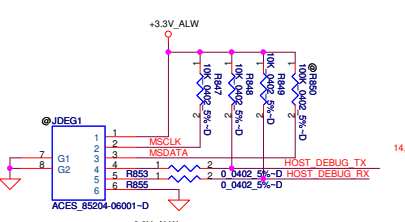
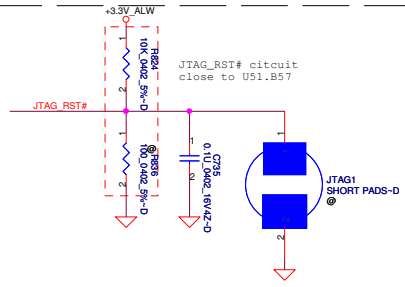
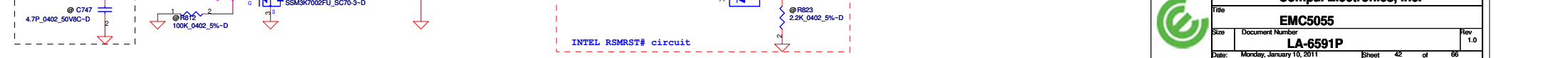
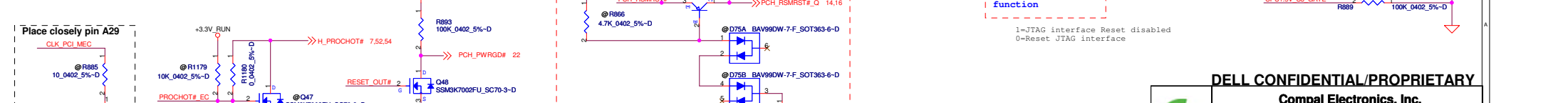
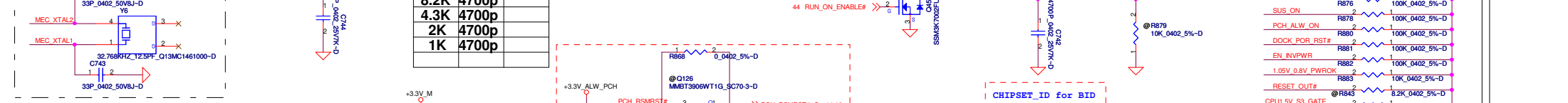
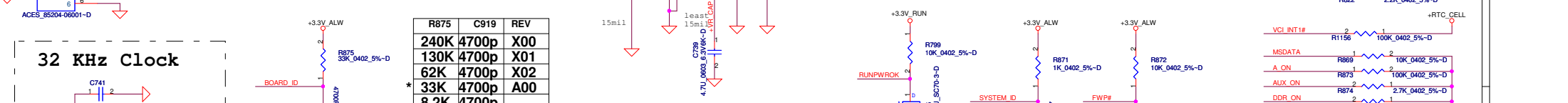
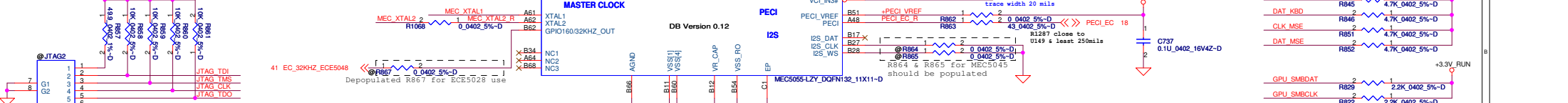
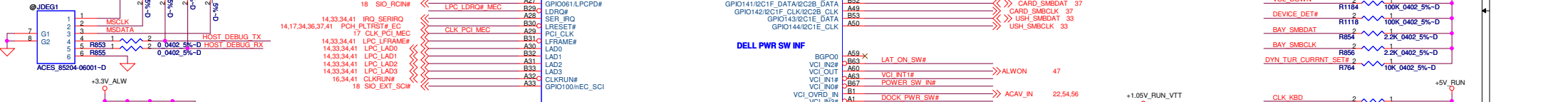
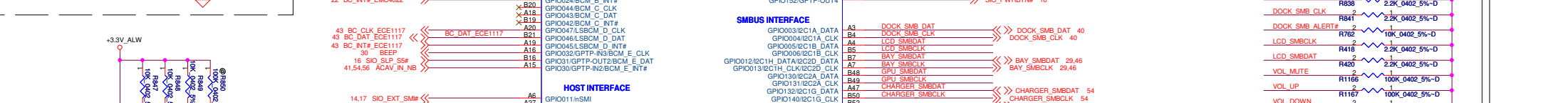
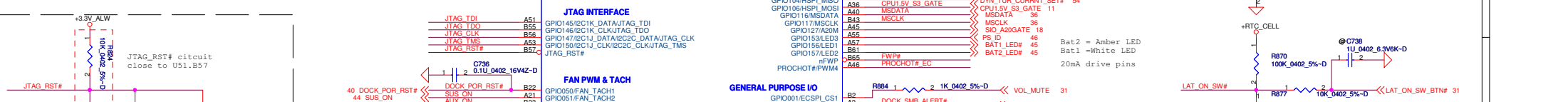
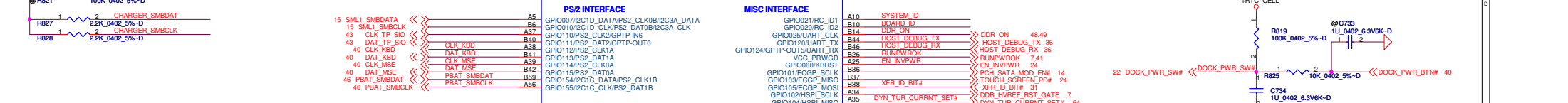
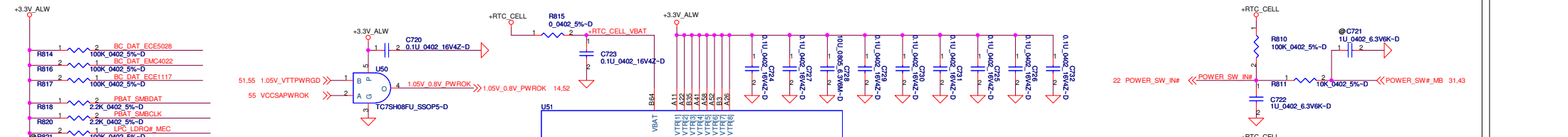
ME_FWP PCH has internal 20K PD.
(suspend power rail)

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Title ECE5028		
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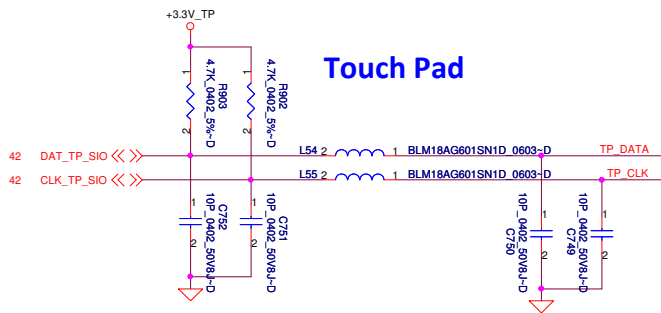
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R875	C919	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	A00
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

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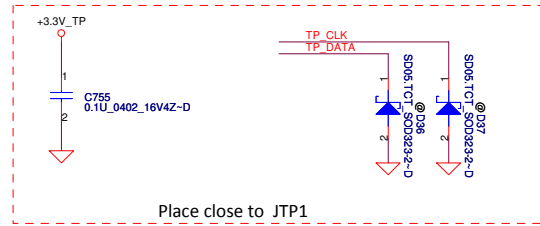
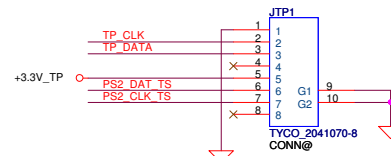
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Size	Document Number	LA-6591P	
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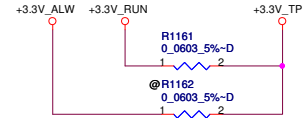
Touch Pad

Pin reverse for PT

Touch Pad Conn. Pitch=0.5mm

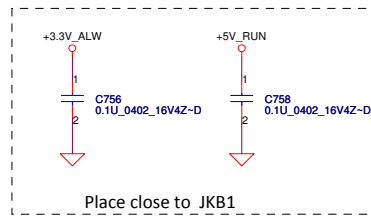
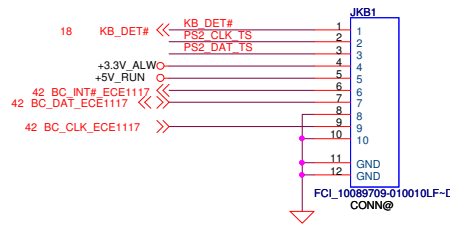


Place close to JTP1



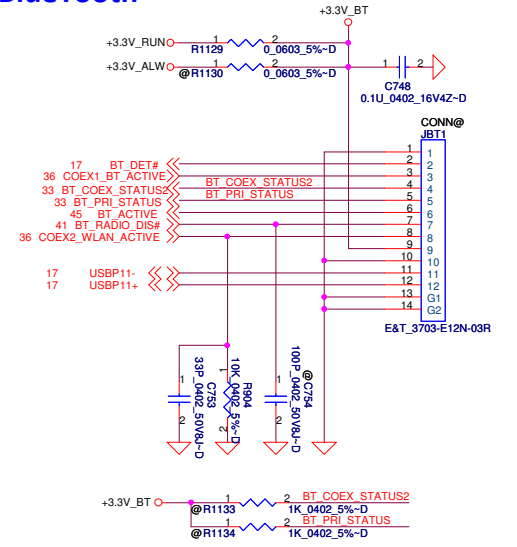
Change KB connector to same as JSC1

KB Conn. Pitch=1.0mm

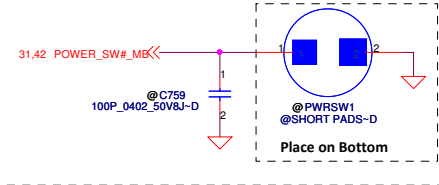


Place close to JKB1

BlueTooth



Power Switch for debug



Place on Bottom

@LVDS cable

Part Number	Description
DC020003Y0L	H-CONN SET 2XJ MB-LCD 14 WXGA+(-1ch)

@RTC BATT

Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@Speak

Part Number	Description
PK230003Q0L	SPK PACK 2XJ 2.0W 4 OHM FG

@LED Board FFC

Part Number	Description
NBX0000RFP0L	FFC 6P H P1 PAD=0.7 87.4MM MB-LCD/B OFD

@MEDIA Board FFC

Part Number	Description
NBX0000RS0L	FFC 12P G P.5 PAD.3 75MM MB-VOLUME/B OFD

@LVDS cable

Part Number	Description
DC02C00180L	H-CONN SET OFD MB-LCD CAM LED 2CHANNEL

@UMA DC IN wire cable

Part Number	Description
DC30100B00	CONN SET OFD DCJACK-MB MDM0-DC300004-DF

@Battery bridge cable

Part Number	Description
DC020014210	H-CONN SET OFD H/B-BATTERY 9PIN

@MDC wire set cable

Part Number	Description
DC30100RL0L	CONN SET OFD MDC-RJ11

@TP FFC

Part Number	Description
NBX0000RR0L	FFC 8P F P.5 PAD=0.3 136MM MB-TP/B OFD

@KB FFC

Part Number	Description
SP070007V0L	S SOCKET TYCO 1770551-1 10P H5.9 SMART

@BT wire cable

Part Number	Description
DC020014Y0L	H-CONN SET OFD MB-BT

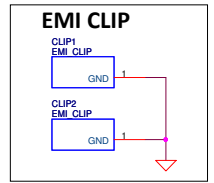
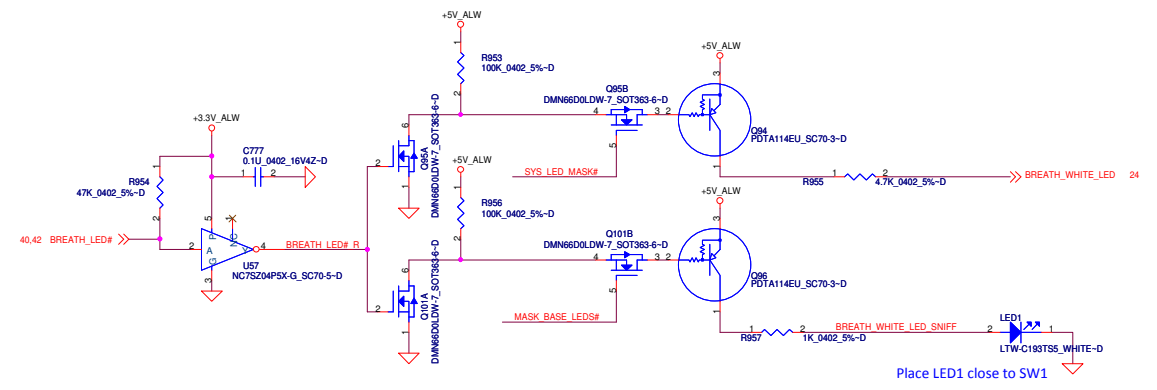
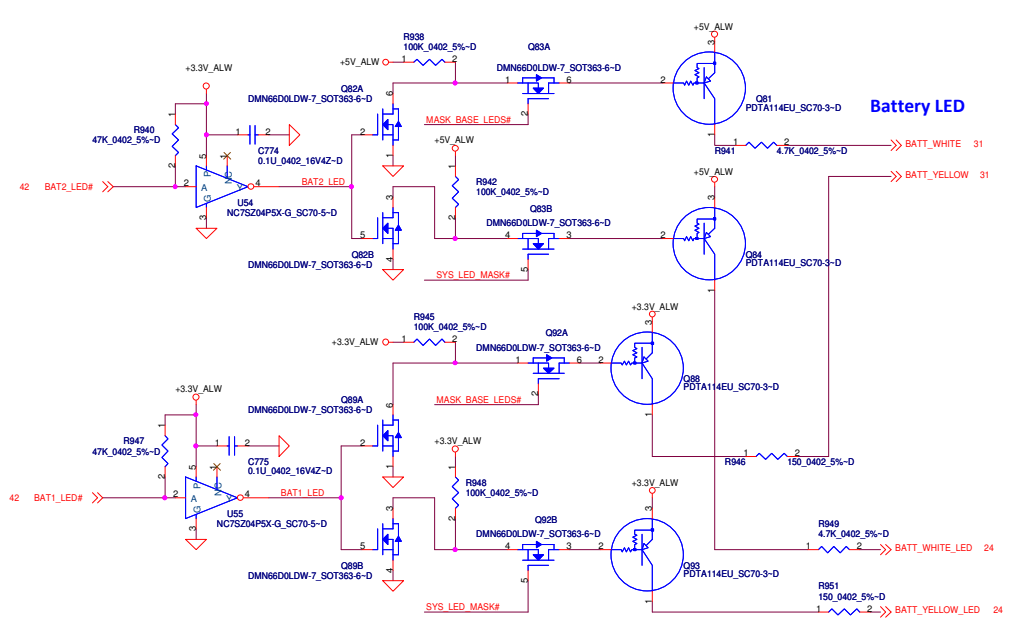
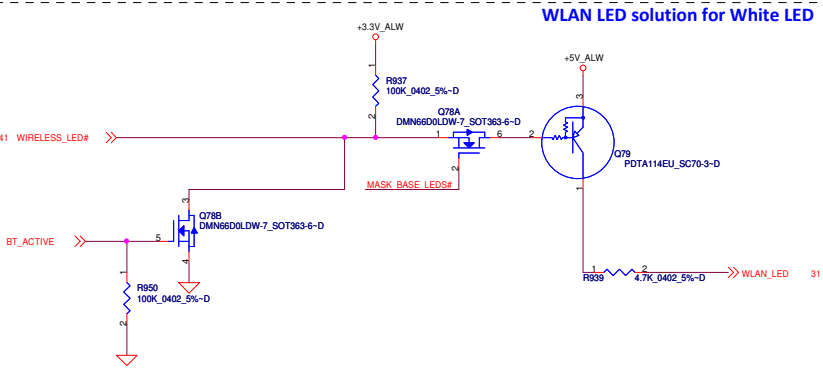
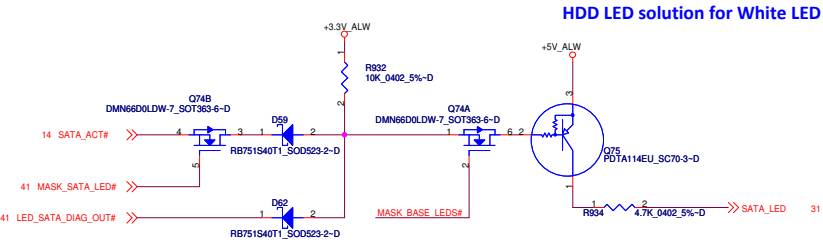
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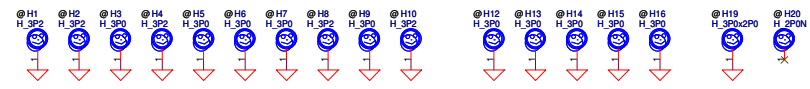
Title			
Touch Pad/Int KB/BT			
LA-6591P			
Size	Document Number	Rev	1.0
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LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

- ### Fiducial Mark
- FD1
 - FIDUCIAL MARK-D
 - FD2
 - FIDUCIAL MARK-D
 - FD3
 - FIDUCIAL MARK-D
 - FD4
 - FIDUCIAL MARK-D



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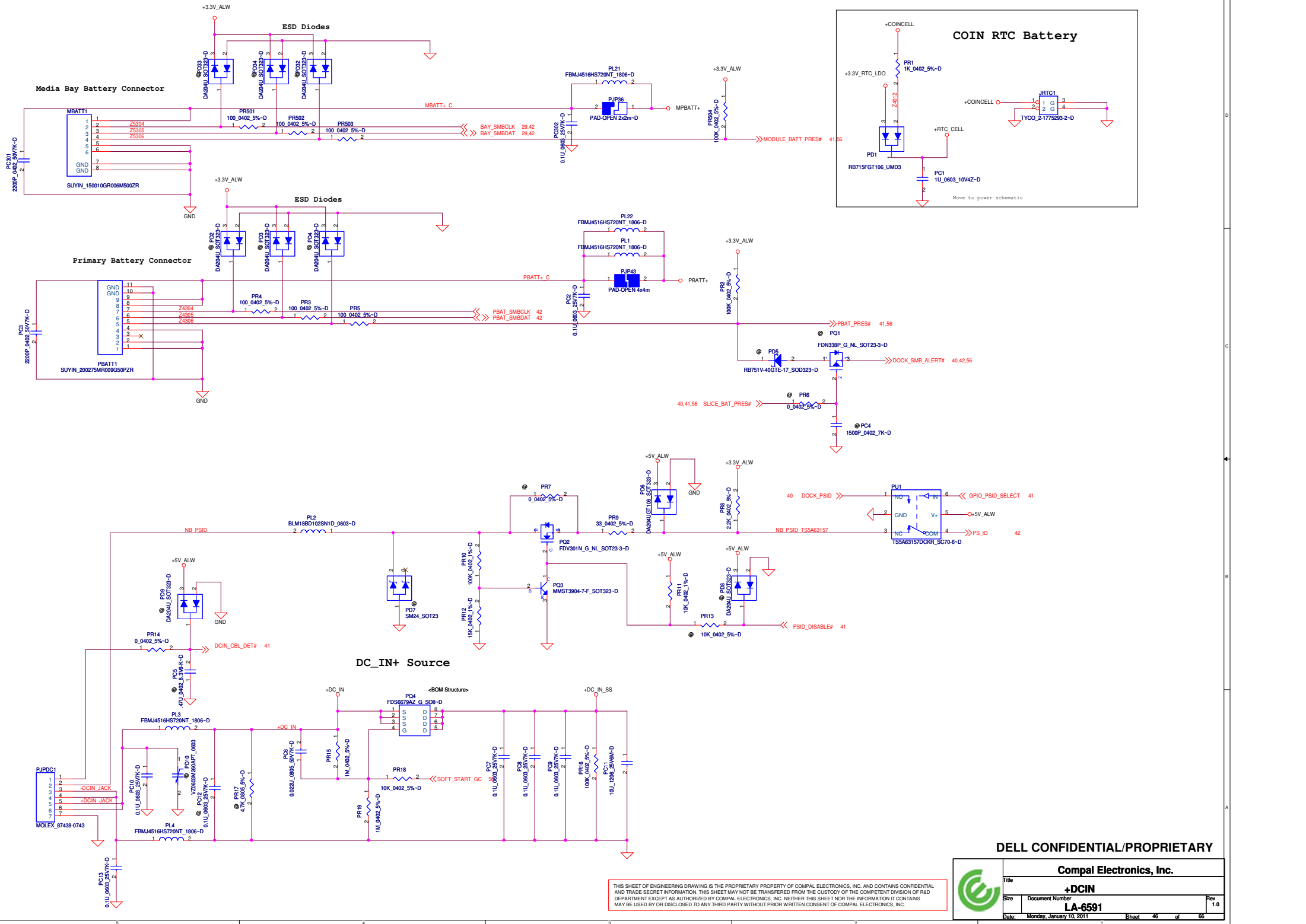
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PAD and Standoff

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		Compal Electronics, Inc.	
		+DCIN	
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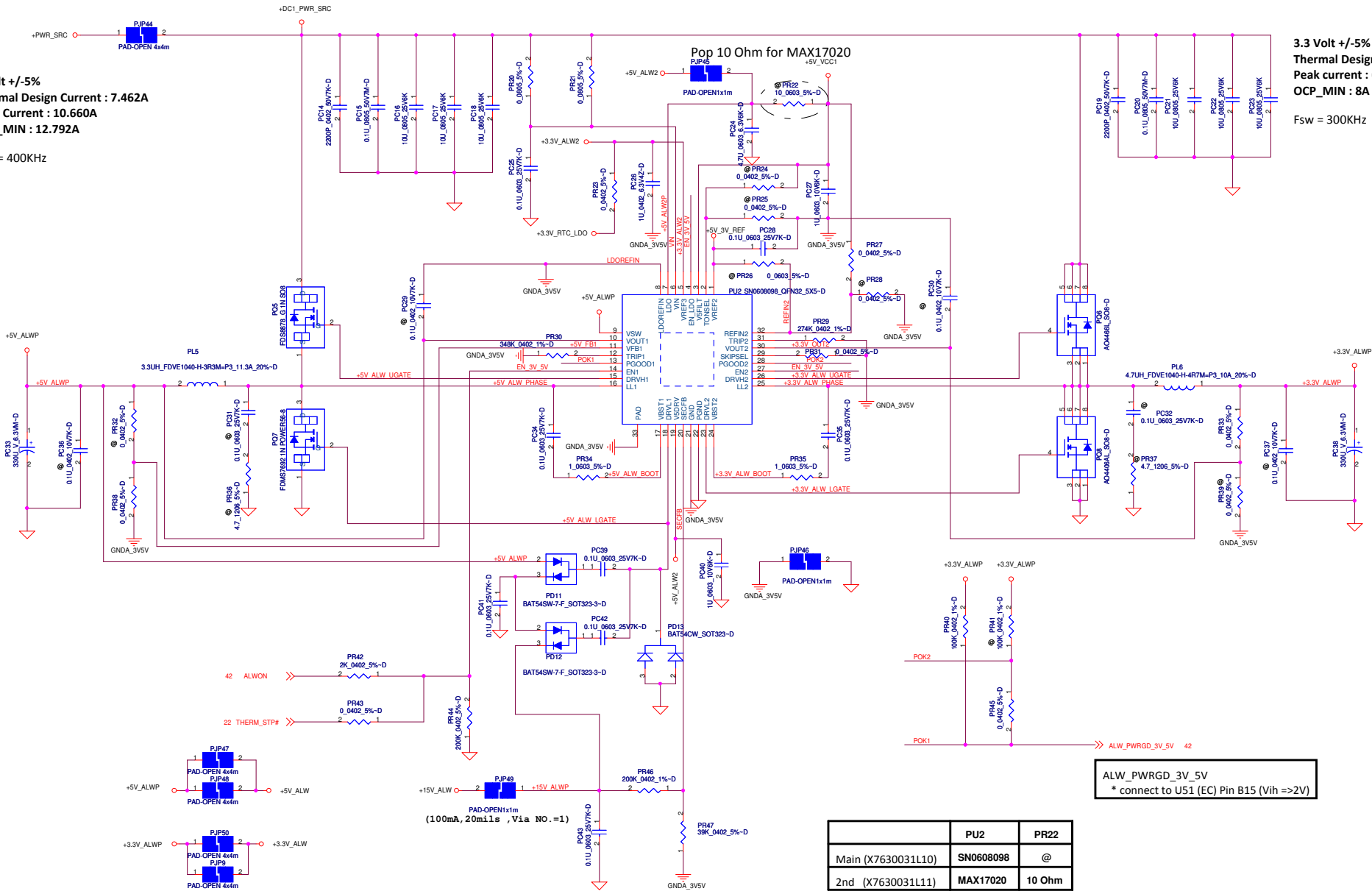
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+3.3V_ALWP / +5V_ALWP / +5V_ALW2 / +15V_ALWP / +3.3V_RTC_LDO

5 Volt +/-5%
 Thermal Design Current : 7.462A
 Peak Current : 10.660A
 OCP_MIN : 12.792A

Fsw = 400KHz

3.3 Volt +/-5%
 Thermal Design Current : 4.707A
 Peak current : 6.725A
 OCP_MIN : 8A
 Fsw = 300KHz



	PU2	PR22
Main (X7630031L10)	SN0608098	@
2nd (X7630031L11)	MAX17020	10 Ohm

ALW_PWRGD_3V_5V
 * connect to U51 (EC) Pin B15 (Vih => 2V)

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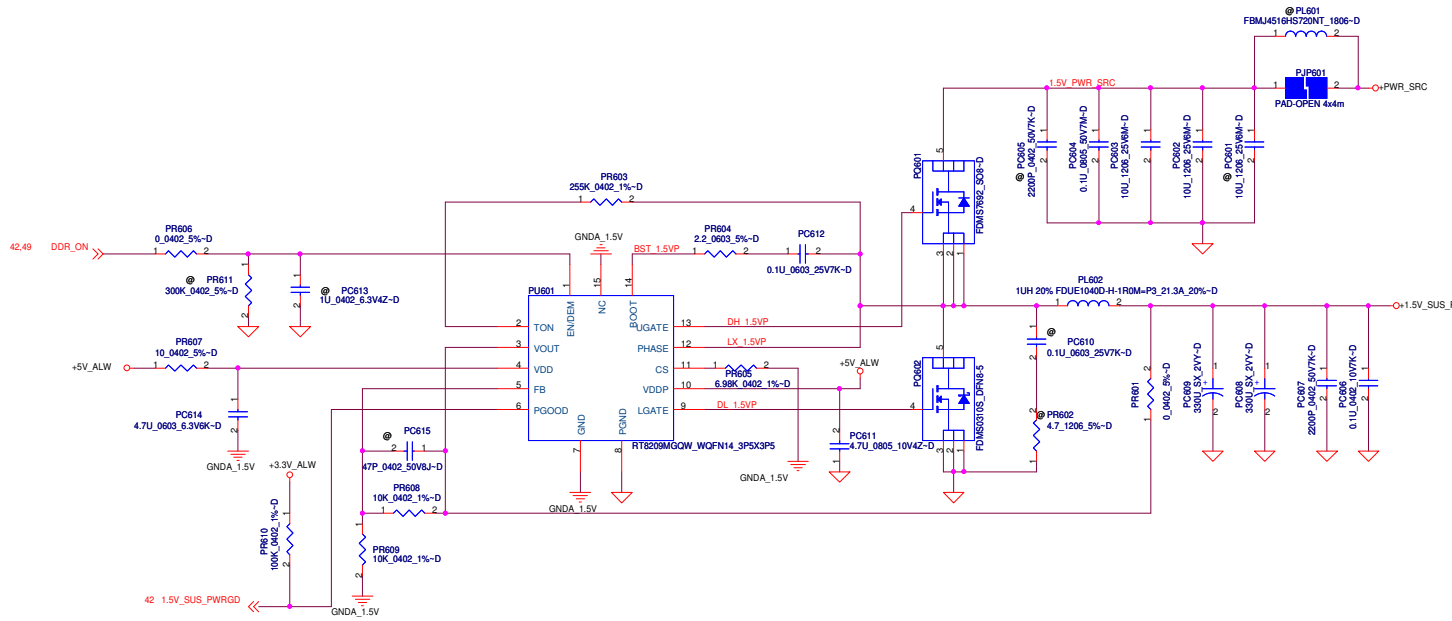
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Size: Document Number **LA-6591** Rev **1.0**

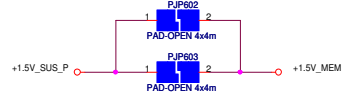
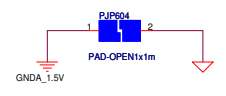
Date: Monday, January 10, 2011 Sheet 47 of 66

+1.5V_SUS_P

1.5 Volt +/-5%
 Thermal Design Current: 9.649A
 Peak current: 13.785A
 OCP_MIN:15.164A



1.5V_SUS_PWRGD
 * connect to U51 (EC) Pin B9 (Vih => 2V)



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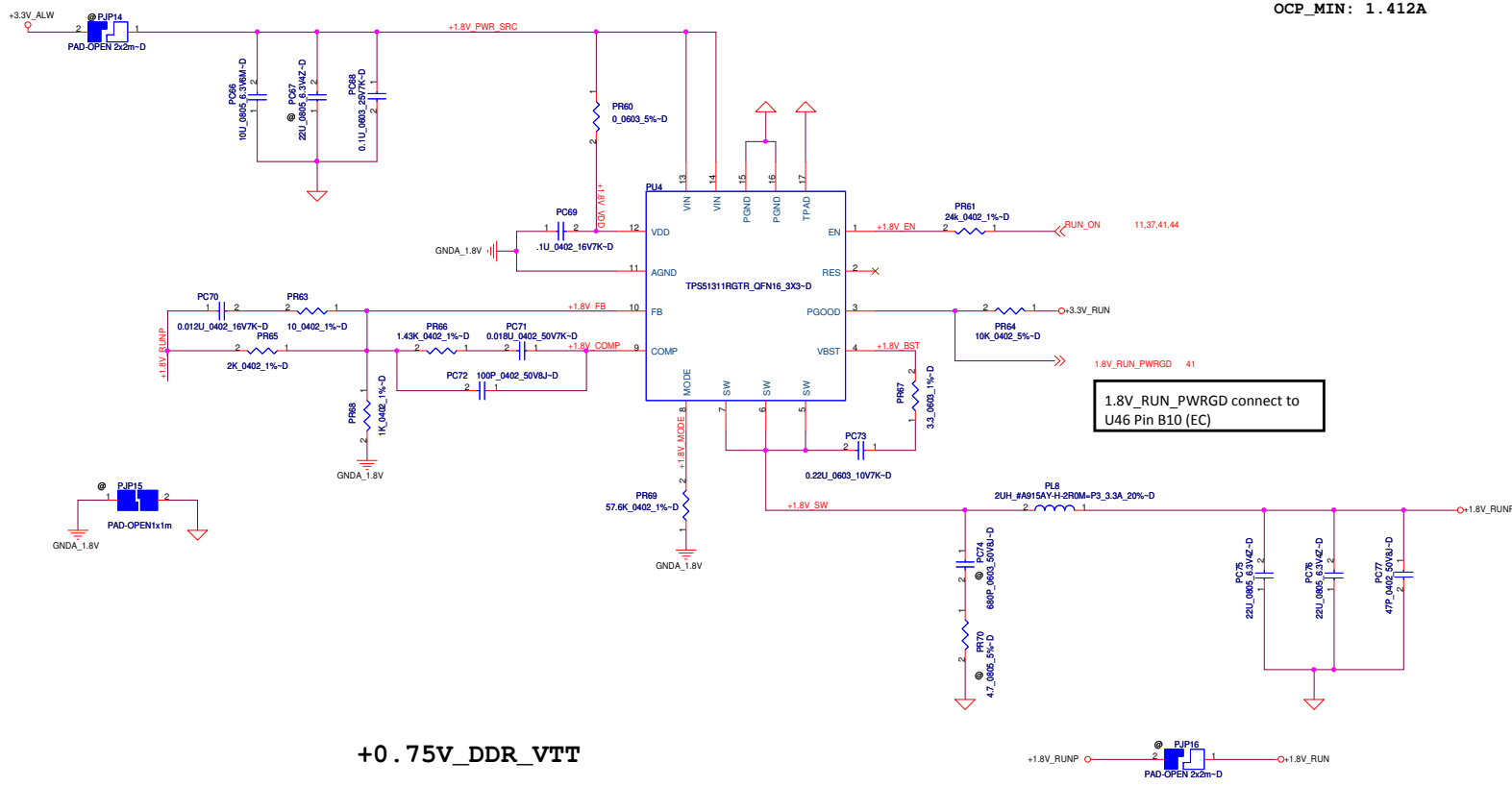
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		+1.5V MEM	
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+1.8V_RUNP

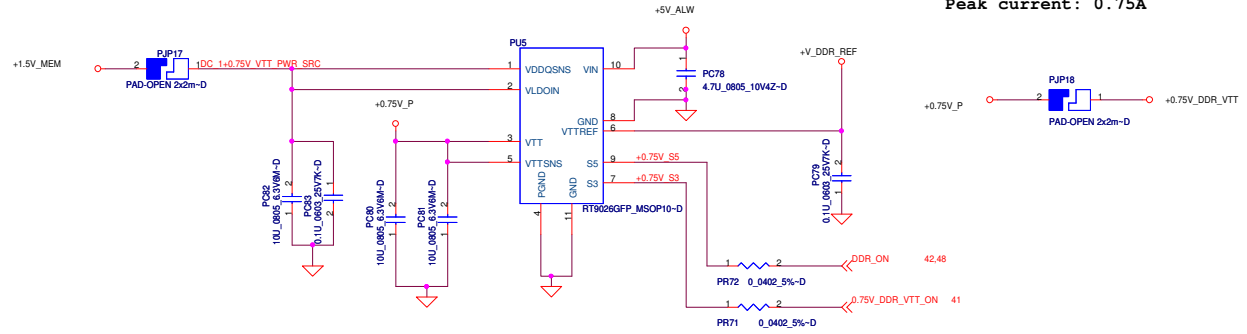
1.8 Volt +/-5%
 Thermal Design Current: 0.824A
 Peak current: 1.177 A
 OCP_MIN: 1.412A



+0.75V_DDR_VTT

DDR3 Termination

0.75Volt +/-5%
 Thermal Design Current: 0.525A
 Peak current: 0.75A

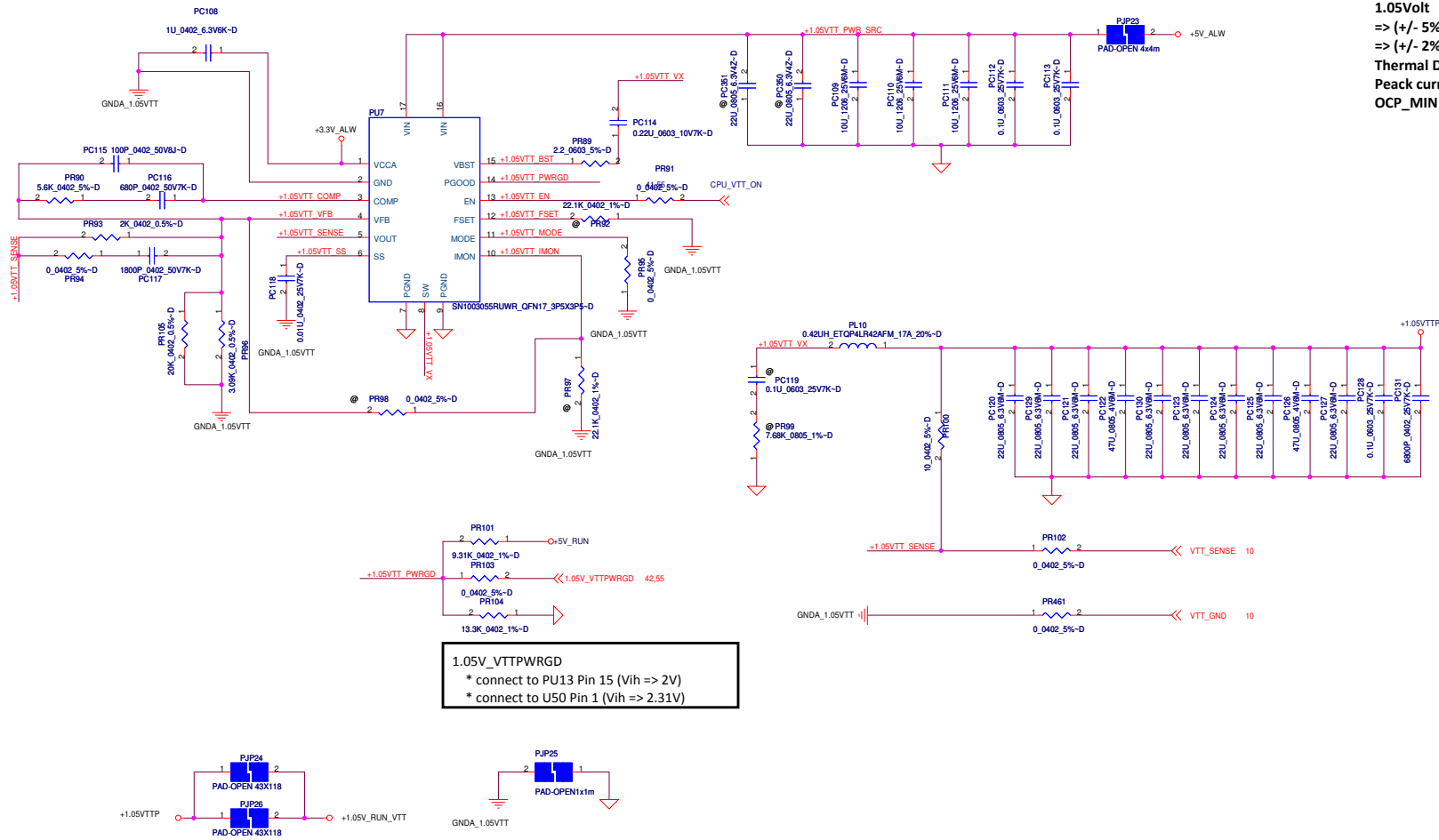


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		Compal Electronics, Inc.	
		+0.75V DDR VT/+1.8V RUN	
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+1.05VTT



1.05V_VTTPWRGD
 * connect to PU13 Pin 15 (Vih => 2V)
 * connect to U50 Pin 1 (Vih => 2.31V)

1.05Volt
 => (+/- 5% AC + DC + Ripple)
 => (+/- 2% DC + Ripple)
Thermal Design Current : 5.980A
Peak current : 8.970A
OCP_MIN : 10.764A

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Title		ISL95870A +1.05V RUN VTT	
Size	Document Number	Rev	
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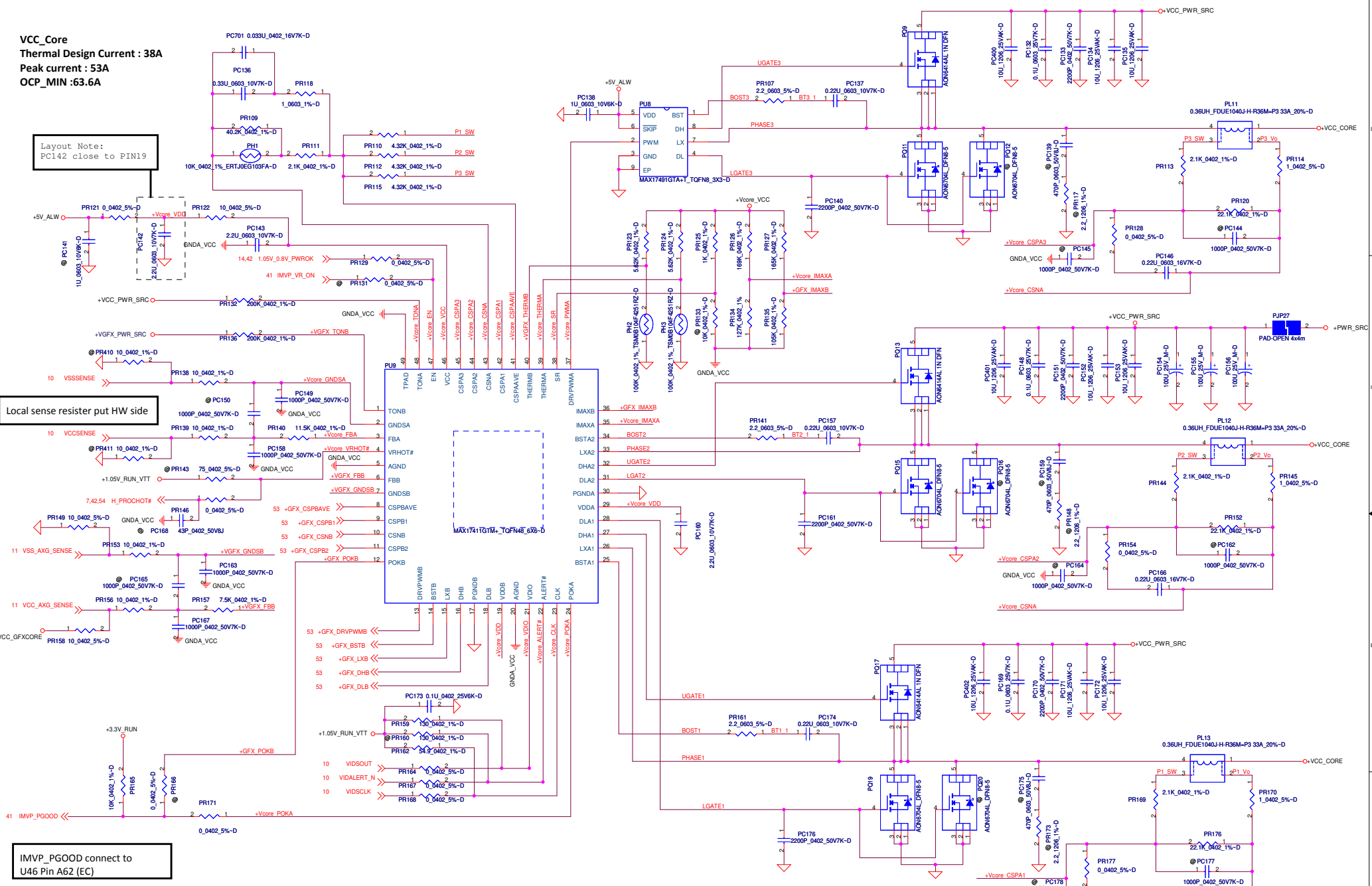
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VCC_Core
 Thermal Design Current : 38A
 Peak current : 53A
 OCP_MIN :63.6A

Layout Note:
 PC142 close to PIN19

Local sense resistor put HW side

IMVP_PG0OD connect to
 U46 Pin A62 (EC)



Vcore/VAXG H/S Mosfet	PQ9, PQ13, PQ17, PQ24, PQ26
Main (X7630031L06)	AON6414AL
2nd	SIR472
3rd (X7630031L07)	MDU2657RH

Vcore/VAXG L/S Mosfet	PQ11, PQ15, PQ19, PQ25, PQ26
Main (X7630031L06)	AON6704L
2nd	SIR164DP
3rd (X7630031L07)	MDU2653RH

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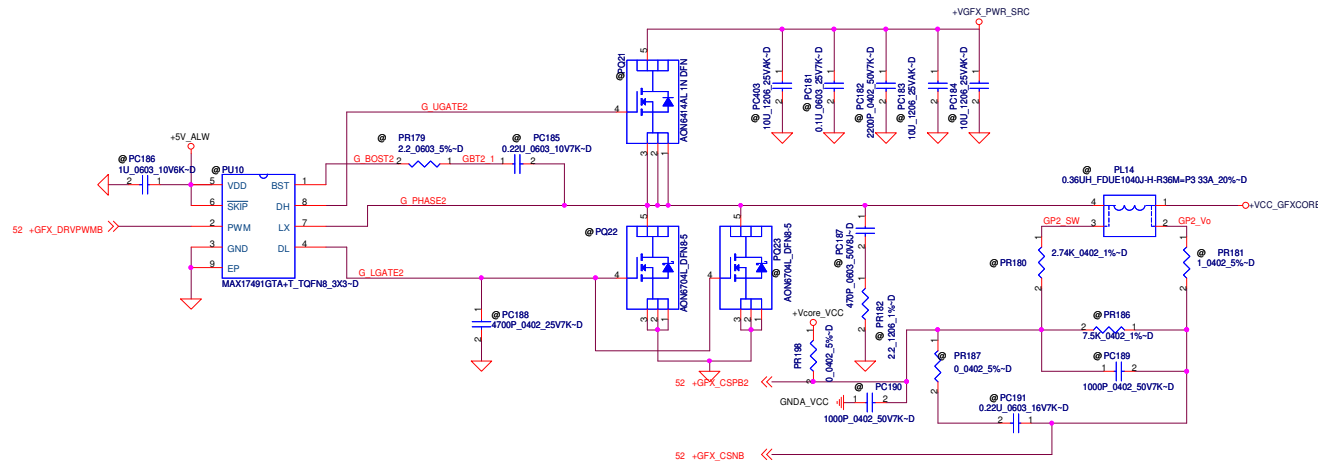
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Vcore

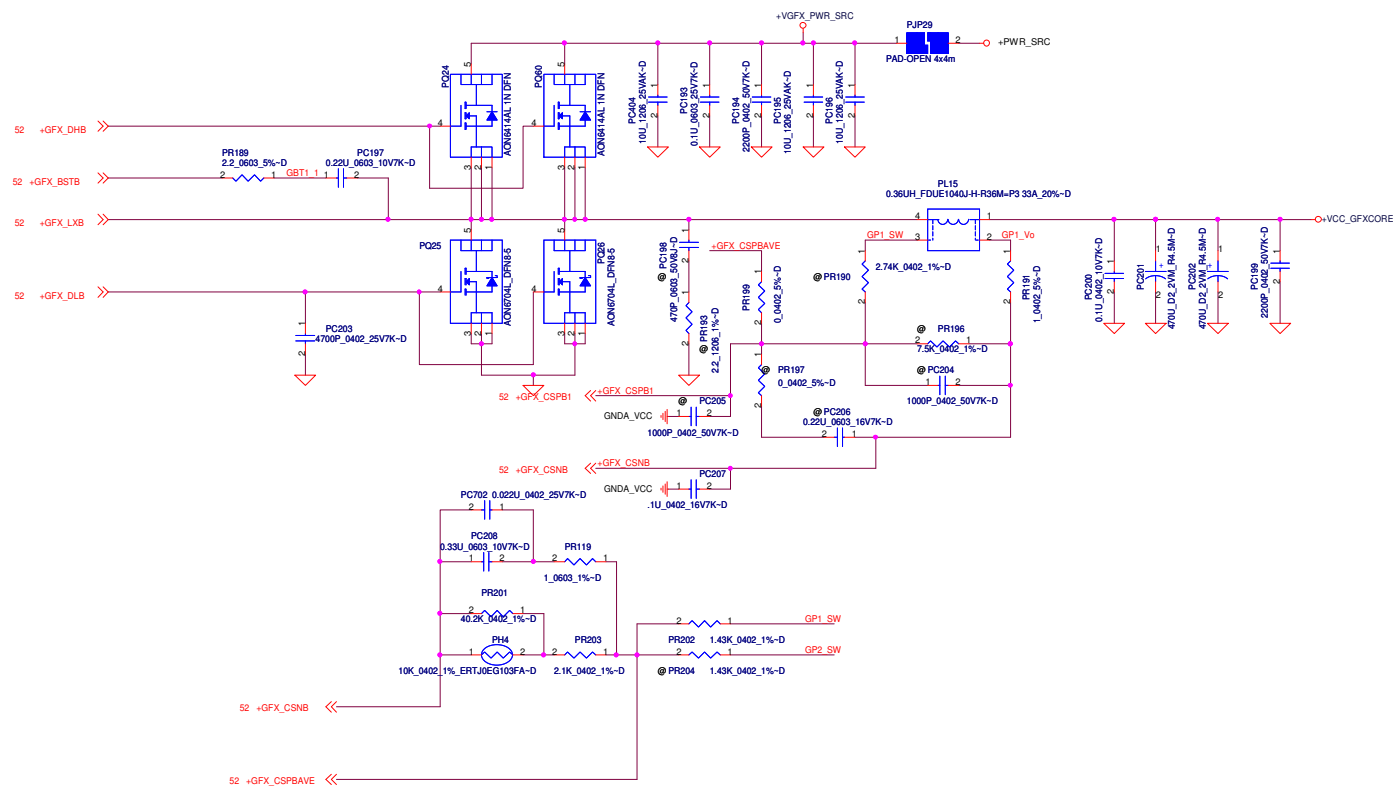
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VCC_AXG
 Thermal Design Current : 21.5A
 Peak current : 33A
 OCP_MIN :39.6A



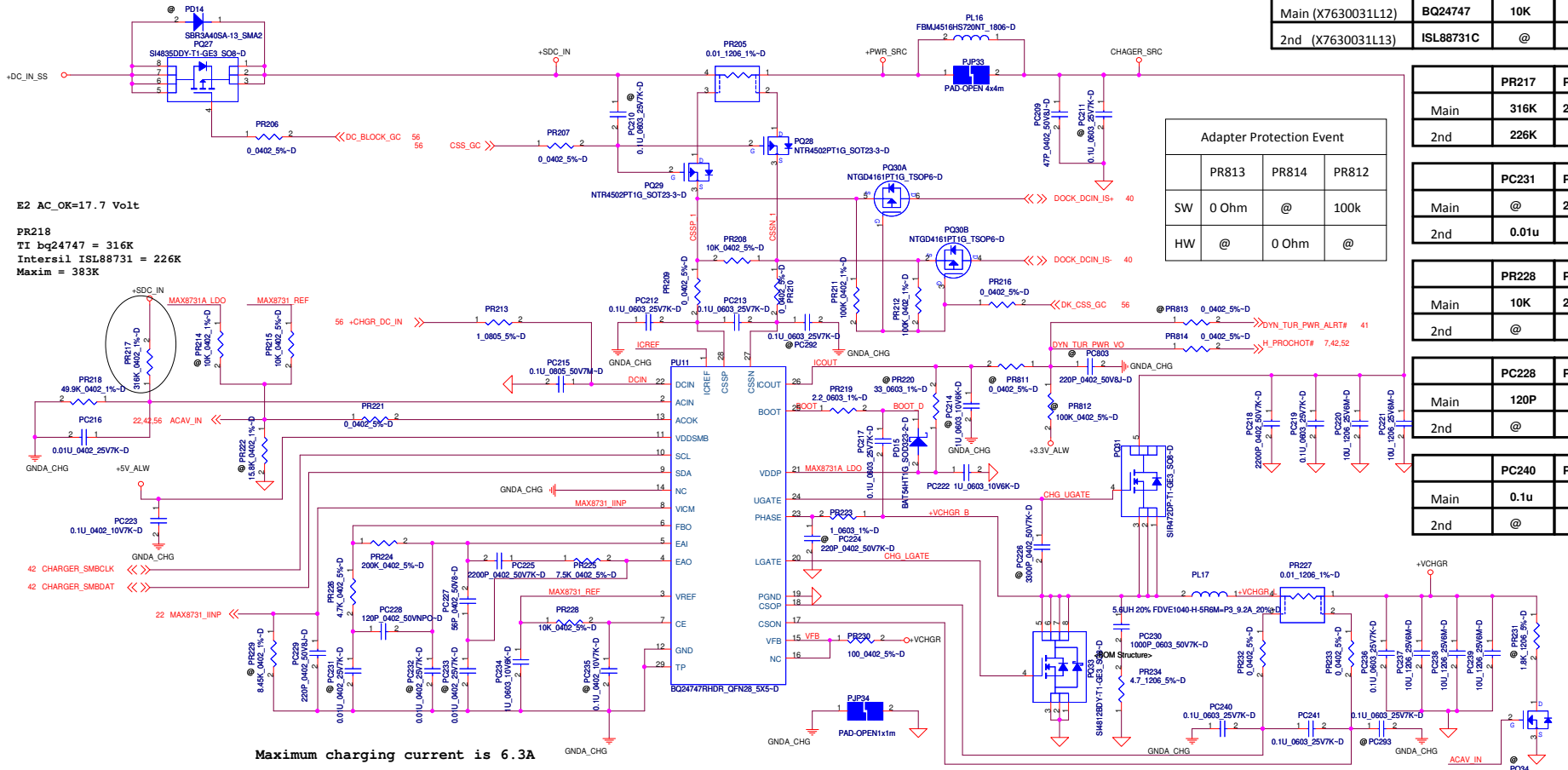
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Title		Vcore	
Size	Document Number	Rev	1.0
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Adapter Protection Event

	PR813	PR814	PR812
SW	0 Ohm	@	100k
HW	@	0 Ohm	@

	PU11	PR215	PR214	PR222
Main (X7630031L12)	BQ24747	10K	@	@
2nd (X7630031L13)	ISL88731C	@	10K	15.8K

	PR217	PC229	PR226
Main	316K	220P	4.7K
2nd	226K	@	2.2K

	PC231	PR224	PR225
Main	@	200K	7.5K
2nd	0.01u	@	@

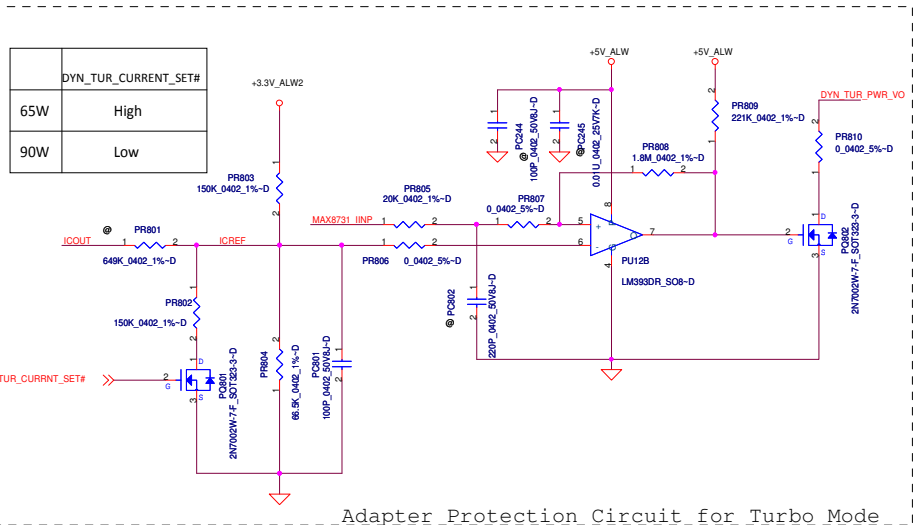
	PR228	PC225	PC227
Main	10K	2200P	56P
2nd	@	@	@

	PC228	PC234	PC233
Main	120P	1u	@
2nd	@	@	0.01u

	PC240	PC241	PR232
Main	0.1u	0.1u	0 ohm
2nd	@	@	0.22u 10 ohm

E2 AC_OK=17.7 Volt
 PR218
 TI bq24747 = 316K
 Intersil ISL88731 = 226K
 Maxim = 383K

Maximum charging current is 6.3A



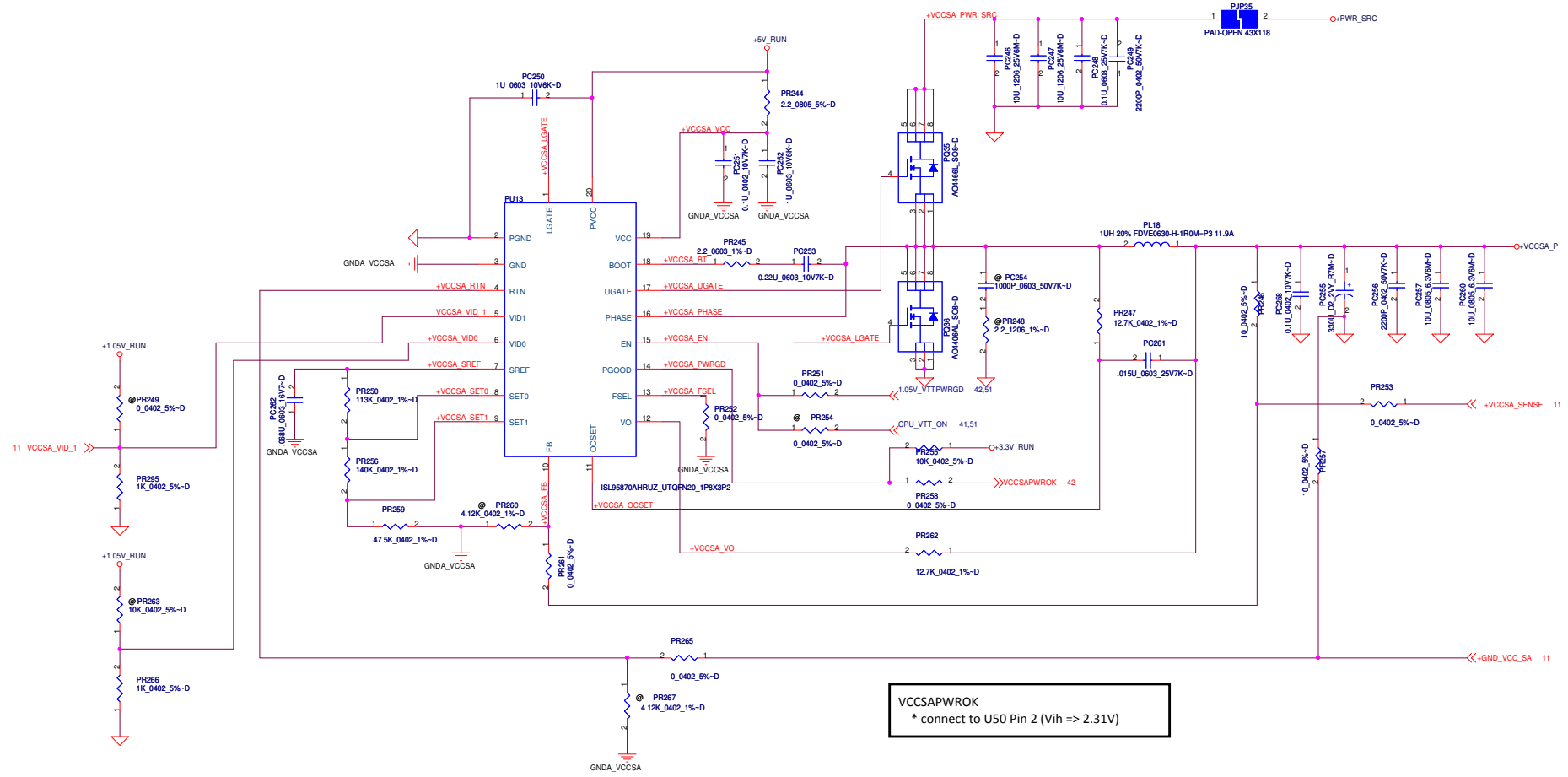
	PR223	PR220	PC214	PC292	PR209	PR210	PC213
Main	1 ohm	@	@	@	0 ohm	0 ohm	0.1u
2nd	0 ohm	4.7 ohm	1u	0.1u	10 ohm	10 ohm	0.047u

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VCCSA
 Thermal Design Current : 4.2A
 Peak current : 6A
 OCP_MIN : 7.2A



VCCSA_PWRROK
 * connect to U50 Pin 2 (Vih => 2.31V)

VCCSA_VID_1	0.9V	0.8V
	0	1

output voltage adjustable network

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ISL95870A 0.8V VCC_SA

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1	55	VCCSA	6/30	Intersil	VCCSA spike issue	Delete PR264 Delete VCCSA_VID_0 net Connect VCCSA_VID_1 net to PIN5 Depop PR249, PR267 and PR260 Change PR261 and PR260 to 0 Ohm (SD02800008L) from 24.9k (SD03424918L) Change PR259 to 47.5k (SD03447528L) from 274k (SD03427438L) Change PR256 to 140k (SD03414038L) from 0 Ohm (SD02800008L) Change PR250 to 113k () from 34k (SD03434028L) Add pull down PR295 10k(SD02810028L)	X01
2	55	VCCSA	6/30	Intel	Change VCCSA VID pull down resistor value	Change PR295 and PR266 to 1k (SD02810018L) from 10k (SD02810028L)	X01
3	47	3V/5V	7/15	Compal	3V/5V Bulk cap interfere with ME	Change PC33 and PC38 to 330U/25m/H1.9(SGA00001A8L) from 330U/25m/H2.8 (SGA1933131L)	X01
4	48	+1.5V_SUS	7/15	Compal	Vendor will not support this part	Change PC609 and PC608 to 330U/9m/2V (SGA20331E0L) from 330U/9m/2.5V (SGA19331D1L)	X01
5	46	DCIN	7/15	Compal	PL1 current rating is not enough for 9cell (3.0Ah 1C) discharge current	Change PL1 to FBMJ4516HS720NT(SM010009C8L) from FBMA-L18-453215-900LMA90T (SM01002078L) Add PL22 FBMJ4516HS720NT(SM010009C8L)	X01
6	47	3V/5V	7/16	Compal	+3.3V phase node over Mosfet Vds rating	Change PQ6 AO4466L (SB00000CG8L) from SI4128DY (SB00000IR0L) Change PQ8 AO4712L (SB00000AJ1L) from SI4134DY(SB00000KB0L)	X01
7	47	3V/5V	7/16	Compal	PC24 down size to 0603 from 0805	Change PC24 to 4.7u/6.3V/0603 (SE107475K8L) from 4.7u/6.3V/0805 (SE093475K8L)	X01
8	47	3V/5V	7/16	Compal	10u/1206/X5R/25V will COS	Change PC16,PC17,PC18,PC21,PC22 and PC23 to 10u/0805/X5R (SE00000QR00) from 10u/1206/X5R (SE142106M8L)	X01
9	55	VCCSA	7/16	Compal	VCCSA output voltage is not constant so change some net name	Change +0.8V_VCC net name to +VCCSA_P Change 0.8V_VCCPWROK net name to VCCSAPWROK Change +0.8V_VCC_SA net name to +VCC_SA	X01
10	48	1.5V_SUS	7/16	Richtek	Reserve Pull down resister on EN pin for power consumption issue	Add PR611 0402 resister pad on EN pin	X01
11	54	Charger	7/18	Compal	PQ27 body diode can handle surge current when adapter plug in so depop PD14	Depop PD14 SBR3A40SA (SC100003J00)	X01
12	56	Selector	7/18	Compal	Leakage issue on PD16	Change PD16 to ES2AA (SC100005A0L) from SBR3A40SA (SC100003J00)	X01
13	52,53	AXG_Core	7/20	MAXIM	Depop one phase for AXG_core	Change PR202 to 1.43k (SD03414318L) from 5.49k (SD03454918L) Change PR203 to 2.1k (SD03421018L) from 2.49k (SD03424918L) Change PC208 to 0.33u/10V/X7R (SE080334K8L) from 0.22u/16V/X7R (SE026224K8L) Change PR201 to 40.2k (SD03440228L) from 10K (SD03410028L) Depop PR204,PR190,PR196,PC206,PR197,PL14,PR181,PR186,PR190,PC191,PR187,PQ21,PQ22,PC184,PC183,PC182,PC181,PC403,PC185,PR179,PC188,PU10,PC186 Pop PR198 and PR199 0 Ohm (SD02800008L) Change PR157 to 8.66k (SD03486618L) from 13.3K (SD03413328L) Pop PQ60 AON6414L (SB00000NW00) Pop PQ26 AON6704 (SB00000I90L) Change PL15 to 0.36u (SH00000HQ0L) from 0.56u (SH00000I20L)	X01
14	54	Axg_core Vcore	7/20	MAXIM	Reserve 0402 cap pad for transient fine tune	Add PC701 and PC702 0402 cap pad	X01


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15	54	Charger	7/20	Compal	Reserve adapter protection circuit for turbo mode	Change PU11 pin1 net name to ICREF from GNDA_CHG Change PU11 pin26 net name to ICOUT from VCC Reserve PR801,PR802,PR803,PR804,PR805,PR806,PR807,PR808,PR809,PR810,PR811,PR812 Reserve PC801,PC802,PC803	X01
16	55	VCCSA	7/20	Compal	VCCSA phase node over Mosfet Vds rating	Change PQ35 A04466L (SB00000CG8L) from SI4128DY (SB00000IR0L) Change PQ36 A04712L (SB00000AJ1L) from SI4172DY (SB00000HN0L)	X01
17	52	Vcore VAXG_core	7/24	MAXIM	Fine tune OCP setting for Pass 2 IC	Change PR127 to 165K (SD03416530L) from 100K (SD03410038L) Change PR135 to 105K (SD03410538L) from 150K (SD03415038L) Change PR126 to 169K (SD03416938L) from 127K (SD034127380) Change PR134 to 127K (SD034127380) from 100K (SD03410038L)	X01
18	52,53	Vcore VAXG_core	7/24	MAXIM	Phase node switching waveform abnormal issue for Pass 2 IC	Change PR118 to 1 Ohm (SD014100B8L) from 2 Ohm (SD013200B8L) Change PR119 to 1 Ohm (SD014100B8L) from 2 Ohm (SD013200B8L)	X01
19	54	Charger	7/28	TI	Pop adapter protection component for turbo mode with TI solution	Pop PR803 100k (SD03410038L) Pop PR804 46.4k (SD000009R8L) Pop PR802 110k (SD03411038L) Pop PR801 1.87M (SD00000WN0L) Pop PQ801 RHU002N06 (SB50206008L) Pop PR812 100K (SD02810038L) Pop PC801 100P (SE071101J8L)	X01
20	52,53	Vcore VAXG_core	7/28	Compal	Fine tune load line and transient for Vcore and VAXG_core	Change PR140 to 12k (SD03412020L) from 12.4k (SD00000AJ8L) Change PR157 to 8.25k (SD03482518L) from 8.66K (SD03486618L) Pop PC701 and PC702 0.033uF (SE076333K8L)	X01
21	56	Selector	9/2	Compal	Change parts to HF parts	Change PQ51 FDN338P_G (SB90338001L) from FDN338P (SB90338008L) Change PD18, PD19, PD21, PD22, PD23, PD24, PD25, PD26, PD27, PD28, PD29, PD30 and PD31 RB751V-40GTE-17 (SCS00004L0L) from RB751V (SC1B751V08L) Change PQ37, PQ40, PQ41, PQ45 and PQ46 FDS6679AZ_G (SB000009D1L) from FDS6679AZ (SB000009D8L)	X02
22	46	+DCIN	9/2	Compal	Change parts to HF parts	Change PD6 DA204UGT106 (SC60000170L) from DA204UT106 (SC1A204U00L) Change PQ1 FDN338P_G (SB90338001L) from FDN338P (SB90338008L) Change PQ4 FDS6679AZ_G (SB000009D1L) from FDS6679AZ (SB000009D8L) Change PD1 RB715FGT106 (SCSB715F010) from RB715F (SCSB715F08L) Change PQ2 FDV301N_G (SB503010020) from FDV301N (SB50301008L)	X02
23	47	+5V/3.3 /+15VALW	9/2	Compal	Change parts to HF parts	Change PQ5 FDS8878_G (SB00000BV1L) from FDS8878 (SB00000BV8L)	X02
24	54	Charger	9/2	Compal	Change parts to HF parts	Change PQ33 SI4812BDY-T1-GE3 (SB00000DI1L) from SI4812BDY-T1-E3 (SB00000DI0L) Change PL17 FDVE1040-H-5R6M=P3 (SH00000CH1L) from FDVE1040-5R6M=P3 (SH00000CH0L) Change PQ27 SI4835DDY-T1-GE3 (SB00000FF1L) from SI4835DDY-T1-E3 (SB00000FF0L)	X02
25	48	+1.5V_SUS	9/2	Compal	Change parts to HF parts	Change PL602 FDUE1040D-H-1R0M=P3 (SH000009U1L) from FDUE1040D-1R0M=P3 (SH000009U0L)	X02
26	47	+5V/3.3 /+15VALW	9/2	TI	Fine tune OCP setting for +5V/+3.3V	Change PR29 to 274K (SD03427438L) from 220K (SD03422038L) Change PR30 to 348K (SD00000WW8L) from 243K (SD03424338L)	X02
27	56	Selector	9/13	Compal	Change parts to HF parts	Change PQ39 and PQ44 SI4835DDY-T1-GE3 (SB00000FF1L) from SI4835DDY-T1-E3 (SB00000FF0L)	X02
28	54	charger	9/13	Compal	Fine tune adapter protection circuit for 2nd source and reserve H_PROCHOT#	Delete PQ802 and PR807 MAX8731_IINP signal connect change to inverting input from Non-inverting input ICREF signal connect change to Non-inverting input from inverting input Pop PR811 and PR813 0 Ohm (SD02800008L) Depop PR814	X02

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29	50	+1.05VM	9/14	TI	Fine tune OCP setting	Change PR83 to 10k (SD03410028L) from 57.6k (SD03457628L)	X02
30	46	DCIN	9/16	Compal	6 ~ 7mA leakage current in slice	Change PR2 and PR504 to 100K (SD02810038L) from 10K (SD03410028L)	X02
31	50	+1.05VM	10/14	Compal	22u/1206/6.3V COS issue	Change PC98 ~ PC105 to 22u/0805 (SE00000110L) from 22u/1206 (SE077226M8L)	X03
32	51	+1.05VTT	10/14	Compal	22u/1206/6.3V COS issue	Change PC123 ~ PC125, PC121, PC127, PC120, PC129 and PC130 to 22u/0805 (SE00000110L) from 22u/1206 (SE077226M8L) Change PC122 and PC126 to 47u/0805 (SE00000G60L) from 22u/1206 (SE077226M8L)	X03
33	55	VCCSA	10/14	Compal	Fine tune VCCSA OCP setting for 2nd and 3rd source choke	Change PR247 and PR262 to 12.7k (SD03412728L) from 11.5k (SD03411528L)	X03
34	52,53	Vcore VAXG_core	10/25	Compal	Fine tune Vcore and VAXG_core load line and transient for pass3 sample	Change PR140 to 11.5k (SD03411528L) from 12k (SD03412020L) Change PR157 to 7.68k (SD00000238L) from 8.25k (SD03482518L) Change PC702 to 0.022u (SE075223K8L) from 0.033uF (SE076333K8L) Pop PC207 0.1U (SE076104K8L)	X03
35	56	Selector	10/27	Compal	Fine tune main and media battery switching to slice battery transient time	Change PC270 and PC265 to 0.22uF (SE000005Z8L) from 1uF (SE00000698L)	X03
36	56	Charger	11/01	Compal	Change adapter protection circuit trip point. (Adapter rated current + 0.75A)	Change PR802 to 95.3k (SD03495328L) from 73.2K (SD00000B18L) Change PR801 to 649K (SD03464938L) from 1.87M (SD00000WN0L)	X03
37	56	Charger	11/01	Compal	Change adapter protection event to HW from SW	Pop PR814 0 Ohm (SD02800008L) Depop PR813 0 Ohm (SD02800008L) Depop PR812 100k Ohm (SD02810038L)	X03
38	56	Charger	12/21	Compal	H_PROCHOT# can not pull high issue with external circuit at DC mode	Change PR803.1 net nam to +3.3V_ALW2 from MAX8731_REF Change PQ801.3, PR804.1 and PC801.2 net nam to PGND from GAND_CHG	A00
39	56	Charger	12/21	Compal	H_PROCHOT# pull low level can not meet Intel SPEC with TI solution at AC mode	Depop PR801 (SD03464938L) Change PR802 to 150k (SD03415038L) from 95.3k (SD03495328L) Change PR803 to 150k (SD03415038L) from 100k (SD03410038L) Change PR804 to 68.1k (SD03468128L) from 46.4K (SD000009R8L) Pop PR806, PR807, PR810 0 Ohm (SD02800008L) Pop PQ802 RHU002N06 (SB50206008L) Pop PR809 221K (SD00000HX8L) Pop PR808 1.8M (SD00000K180) Pop PR805 20K (SD03420028L) Depop PR811 (SD02800008L)	A00
40	53	VAXG_core	12/21	Compal	Fine tune GFX load line for 2nd source choke	Change PR157 to 7.5k (SD03475018L) from 7.68k (SD00000238L)	A00
41	56	Charger	12/30	TI	H_PROCHOT# spike voltage issue when AC to DC transient	Pop PR208 10k (SD02810028L)	A00
42	56	Charger	01/07	COMPAL	Adapter protection trip point for 2nd source	Change PR804 to 66.5k (SD03466528L) from 68.1k (SD03468128L)	A00
43	56	Charger	01/07	COMPAL	Change parts for HF	Change PQ801 and PQ802 to 2N7002W (SB57002040L) from RHU002N06 (SB50206008L)	A00

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1	7	HW	6/15/2010	COMPAL	Boot issue	Change QC1 control from SUS_ON to RUN_ON_CPU1.5VS3#	X01
2	11	HW	6/15/2010	COMPAL	Modify net name	Change +0.8V_VCC_SA to +VCC_SA	X01
3		HW	6/15/2010	COMPAL	Follow PPM recommendation to change material	Change capacitors from 10uF_0805_10V Y5V to 10uF_0805_6.3V_X5R: C305,C316,C387,C462,C705,C728,C760,C764,C765,C768,C769,C772,CC135,CH58,CH73,CH80 Change capacitors from 10uF_0805_6.3V to 10uF_0603_6.3V: C475,C638,C641,C643 Change resistors to 0402 size: RC134, RH201,RH253,RH208,RH213 Delete RH192 and add PJP51	X01
4	14	HW	6/15/2010	COMPAL	De-pop PCH XDP	De-pop RH1, RH3~RH10, RH12~RH21, RH24, RH283~RH285, CH1	X01
5	14	HW	6/15/2010	COMPAL	Change HDA_SYNC topology	Add QH7 and RH37	X01
6	17, 29, 42	HW	6/15/2010	COMPAL	Change ODD connector from 13 pin to 31 pin	Change ODD connector to 31 pin, add @R1189,RH340 and remove C1168, C1169,C1170,U87,U88,U89, and connect ODD_DET# to U51.B36	X01
7	18	HW	6/17/2010	COMPAL	Remove touch screen PAID pull down circuit	Remove RH241	X01
8	18	HW	6/17/2010	COMPAL	Follow Intel Design Guide Rev1.0	Change RH149 to 1k and RH150 to 4.7k	X01
9	22	HW	6/17/2010	COMPAL	Change EMC4002 to EMC4022	Change U9 to EMC4022, remove R866,R404,C279	X01
10	26	HW	6/17/2010	COMPAL	For Safety request	Add no stuff D4 and co-lay with F2, change F2 to 2A_8V	X01
11	28, 39	HW	6/17/2010	COMPAL	Change SATA repeater to MAX4951BE	Change U25, U44 to MAX4591BE and change R1169,R1171,R1174,R1176 to 0 ohm and stuff R1174,R1176	X01
12	30	HW	6/17/2010	COMPAL	Change Codec to ZB version and speaker connector	Change JSPK1 to TYCO_1734595-6 and change U72 to ZB version and stuff C962	X01
13	33	HW	6/17/2010	COMPAL	Add Jumper for power consumption measurement	Add PJP52,PJP55	X01
14	33	HW	6/17/2010	COMPAL	Change SI2301BDS to C version	Change Q36 to SI2301CDS	X01
15	33	HW	6/17/2010	BRCOM	Change RFID capacitors for more popular	Change C502,C505 from 1uF to 0.1uF	X01
16	35	HW	6/17/2010	COMPAL	Link R677 to CIS and modify JSD1 connection	Link R677 to CIS to have the correct part number and swap SD/MMCCD# from JSD1 pin16 to pin17, SDWP from JSD1 pin17 to pin 18	X01
17	37	HW	6/17/2010	COMPAL	Change express card power SW to TPS2231MRGPR-2	Change U41 to TPS2231MRGPR-2 and remove C636,C639	X01
18	41	HW	6/17/2010	COMPAL	Add pull down on SLICE_BAT_ON	Add R791	X01
19	11, 14, 42	HW	6/18/2010	COMPAL	EOL concern	Change CC176 to SGA00005H0L, change YH1,Y6 to SJ132P7KW1L	X01
20	43	HW	6/18/2010	COMPAL	Change connector	Change JKB1 to same as JSC1	X01

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21	43	HW	6/18/2010	COMPAL	Change TP pin definition	Reverse TP pin definition for PT	X01
22	14	HW	6/18/2010	COMPAL	Add RTC PAID function	Add RTC_DET# and RH355 on PCH GPIO33	X01
23	41, 42	HW	6/18/2010	COMPAL	Add series resistor and pull up resistors on MIC_MUTE#, VOL_MUTE, VOL_UP, VOL_DOWN	Add R773, R806, R884, R886, R887, R1166, R1167, R1184	X01
24	24, 45	HW	6/18/2010	COMPAL	Correct net name for LED signal	Modify signal name BREATHE_BLUE_LED to BREATHE_WHITE_LED and BREATHE_BLUE_LED_SNIFF to BREATHE_WHITE_LED_SNIFF	X01
25	41	HW	6/18/2010	COMPAL	Correct net name	Modify R1132.2 from SUSACK#_R to SUSACK#_EC	X01
26	32	HW	6/21/2010	INTEL	Remove useless resistors	Remove R556, R558, R559, R560 and short the pin1 and pin2 together	X01
27	14	HW	6/22/2010	COMPAL	Modify BOM Structure	Correct RH45 BOM structure	X01
28	24, 28, 29, 32, 37, 44	HW	6/22/2010	COMPAL	Change part for Halogen free	Change Q18, Q27, Q30, Q34, Q38, Q40, Q42, Q49, Q54, Q58 to HF part	X01
31	44	HW	6/23/2010	COMPAL	Solution +1.5V_RUN voltage drop issue	Change Q59 from SI3456BDV to NTGS4141NT1G	X01
32	41	HW	6/23/2010	COMPAL	Remove double pull high resistor	Remove R1177	X01
33	29	HW	6/23/2010	COMPAL	Remove useless resistor	Remove R1125, R1126	X01
34	44	HW	6/25/2010	COMPAL	NTMS4107NR2G EOL	Change Q55 to NTMS4920NR2G	X01
35	10	HW	6/25/2010	COMPAL	CC129~CC134 D2T LESR5M EOL	Change CC129~CC134 to SGA00004X0L	X01
36	24	HW	6/25/2010	COMPAL	Change LVDS connector to 40 pin	Change JLVDS1 to 40 pin	X01
37	31	HW	6/25/2010	COMPAL	Change I/O connector to TYCO	Change JIO1 vendor from Lotes to TYCO	X01
38	24	HW	6/25/2010	COMPAL	PT panel change touch screen pin definition	Change JTS1 pin definition for new TS pin define	X01
39	14, 29, 36, 42	HW	7/1/2010	COMPAL	Modify Module Bay circuit	1.Remove R1181, R1182, R1189. 2.Change BAY_SMBUS, DEVICE_DET# pull up power rail from +3.3V_RUN to +3.3V_ALW. 3.Change net name ODD_DET# to PCH_SATA_MOD_EN#. 4.Add Q123, Q76, R513, R514, R515 for USB_SMI# circuit. 5.De-pop C627, R712	X01
40	7	HW	7/1/2010	COMPAL	For support XDP device	De-pop RC9	X01
41	15, 18, 41, 42	HW	7/1/2010	COMPAL	Base on GPIO map to modify	1. Move SLP_ME_CSW_DEV# from GPIO45 to GPIO28, add M_CARD_PCIE_SATA# on 5028 GPIOE3. 2. Remove RH238. 3. Change SLICE_BAT_PRES# pull up power rail from +3.3V_ALW2 to +3.3V_ALW. 4. Add R889	X01
42	24	HW	7/1/2010	COMPAL	PWM function	Remove R1139, R1140 and add D68, D69	X01
43	11	HW	7/1/2010	COMPAL	VCCSA VID circuit	Change VCCSA_VID_0 to VCCSA_VID_1 and pop RC138	X01

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44	36, 45	HW	7/2/2010	COMPAL	Modify LED circuit	Remove R1578,R1579,R1580,D42,D60,D61, add Q77,Q124,R705,R718,R719	X01
45	22	HW	7/2/2010	COMPAL	Modify thermal diode for thermal request	Remove C268,C269,use DP1/DN1 for CPU,DP3/DN3 for DIMM,DN5/DP5 for WWAM	X01
46	15, 32	HW	7/5/2010	COMPAL	EOL concern	Change Y3 and YH2 from 1Y725000CE1A to 7A25000110	X01
47	11, 24, 27, 45	HW	7/7/2010	COMPAL	Change part for Halogen free part	Change QC5 to NTR4501NT1G, U21,U24,U54,U55,U57 change to NC7SZ04P5X-G, Q21 change to FDC654P-G	X01
48	29	HW	7/7/2010	COMPAL	USB30 SMI circuit	Stuff R513 due to this pin is OD type on USB30 module	X01
49	29	HW	7/8/2010	COMPAL	Link CIS symbol	Link JSATA2 CIS symbol	X01
50	35	HW	7/9/2010	O2-Mirco	Add discharge circuit for +3.3V_RUN_CARD	Add R826 on +3.3V_RUN_CARD	X01
51	15, 29, 32, 35, 36, 37	HW	7/9/2010	COMPAL	Move PCIE TX AC coupling capacitors close to PCH	Move C408,C409,C460,C461,C567,C568,C596,C597,C598,C599,C617,C618,C647,C648 to page 15 to close to PCH	X01
52	14	HW	7/12/2010	COMPAL	To solve SPI EA	Add R933,R935 on SPI chip select signals	X01
53	24	HW	7/12/2010	COMPAL	Link CIS symbol	Link JLVD51	X01
54	28	HW	7/12/2010	COMPAL	Meet EA result	Stuff R493,R494	X01
55	24, 30, 35, 38, 39	EMI	7/12/2010	COMPAL	EMI request to solve EMI issue	Add R678,C757,L92,L93, and stuff L51,L52,L90, de-pop R736~R739,R1150,R1151, and remove R1106	X01
56	31, 41, 45	HW	7/13/2010	Dell	Remove Mic mute function and LED	Remove R773,R806, R1108,R1161, Q105 and delete MIC_MUTE# signal	X01
57	28	HW	7/13/2010	COMPAL	Follow EA result	De-pop R493,R494 and pop R495,R496	X01
58	29	HW	7/13/2010	COMPAL	Modify zero ODD circuit	Change ZODD_WAKE#,MODC_EN#,MOD_SATA_PCIE#_DET,USB30_EN connection	X01
59	33	HW	7/14/2010	COMPAL	Change power rail for smart card	Change R632,R635 pull up power rail from +3.3V_ALW to +3.3V_ALW_SC	X01
60	22	HW	7/14/2010	COMPAL	Reserve capacitor for WWAN thermal diode	Add @C277	X01
61	14, 17, 18	HW	7/14/2010	COMPAL	To solve back drive issue	Move SIO_EXT_SMI# from PCH GPIO1 to GPIO14, remove RH254, and change RH164 pull up power rail from +3.3V_RUN to +3.3V_ALW_PCH	X01
62	45	HW	7/14/2010	COMPAL	Remove CLIP	Remove CLIP3~CLIP8	X01
63	38, 39	HW	7/15/2010	COMPAL	Remove one TPS2560 for cost saving	Remove U43,C659,C660,R740,PJP6, and share with power source of U45	X01
64	31, 41, 45	HW	7/15/2010	COMPAL	Remove speaker LED	Remove Q119,Q102,R1109,R1059	X01
65	17, 18	HW	7/15/2010	COMPAL	Add pull up for PCH GPIO1	Add RH41 and change reference RH164 to RH41	X01
66	24, 30, 35	HW	7/16/2010	COMPAL	Change part reference for EMI request	Change L92 to LE92,L93 to LE93,R678 to RE678,CE757 to CE757	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
67	20, 44	HW	7/16/2010	COMPAL	For cost saving	Add PJP57, RH202, no stuff QH4, Q49, RH278, R908	X01
68	22	HW	7/16/2010	COMPAL	Modify current sense connection	Move MAX8731_IINP from U9.25 to U9.31	X01
69	41, 42	HW	7/16/2010	DELL	Follow GPIO 0713	Add DYN_TURB_PWR_ALRT#, DYN_TUR_CURRNT_SET#, and change R796 pull up power rail from +3.3V_RUN to +3.3V_ALW	X01
70	35	HW	7/16/2010	COMPAL	Follow vendor request	De-pop RE678, CE757	X01
71	28, 45	HW	7/19/2010	COMPAL	Part leverage select	Change D16, D59, D62 to SC100000S0L	X01
72	14	HW	7/19/2010	COMPAL	Follow Intel XDP design	Change RH43, RH44, RH45 to 200 ohm	X01
73	38, 39	HW	7/20/2010	DELL	Change power rail for layout limitation	Change U90, U91 power rail to +USB_SIDE_PWR, U92 power rail to +SATA_SIDE_PWR	X01
74	31	HW	7/20/2010	COMPAL	Change USB3 (on IO/B) enable signal	Change USB3 enable signal from USB_SIDE_EN# to ESATA_USB_PWR_EN#	X01
75	23	HW	7/20/2010	SMSC	Follow SMSC review result	Add R403	X01
76	31	HW	7/20/2010	COMPAL	Change JIO1 for correct connector list	Change JIO1 to TYCO_2041300-2	X01
77	26	HW	7/20/2010	Safety	Follow safety request	De-pop F2, pop D4 and add R5	X01
78	17, 30, 40	HW	7/20/2010	EMI	Follow EMI request	Add RE1098, RE1100, RE1101, RE1102, CE573, CE574, change RH103, R756 to 33 ohm, C704 to 12pF	X01
79	14	HW	7/20/2010	COMPAL	Change SPI chip select damping R	Change R933, R935 to 47 ohm	X01
80	24, 39	HW	7/20/2010	COMPAL	Change material for small size	Change C300, C669 from 1206 16V to 0805 10V	X01
81	24	HW	7/20/2010	COMPAL	Change U86 power rail for touch screen	Change U86.4 power rail from +3.3V_RUN to +5V_RUN	X01
82	38, 39	HW	7/20/2010	COMPAL	Remove useless capacitors	Remove C1151~C1154	X01
83	41	HW	7/20/2010	COMPAL	Follow GPIO map	Change R796 to 10k ohm	X01
84	44	HW	7/20/2010	COMPAL	Change PJP57 footprint	Change PJP57 footprint to 4x4m	X01
85	31	HW	7/21/2010	COMPAL	Modify HP & Mic circuit	Change JIO1 pin connection	X01
86	36	HW	7/21/2010	COMPAL	Add 0 ohm R on PCIE_MCARD2_DET#	Add R725	X01
87	40	HW	7/21/2010	COMPAL	Follow EA request	Change C704 to 6.8pF	X01
88	35	HW	7/21/2010	COMPAL	Change JSD1 to support Memory Stick	Change R666, R667, change JSD1	X01
89	31, 42	HW	7/22/2010	COMPAL	GPIO MAP update.	add R1590	X01
90	39	HW	7/22/2010	COMPAL	Follow Vender request.	add R1582~R1585	X01
91	39	HW	7/23/2010	COMPAL	To compatible with SN75LVCP601	Add R1586~R1589	X01
92	41	HW	7/23/2010	COMPAL	Add 0 ohm R on TEMP_ALERT# for backup	Add R1591	X01

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93	24, 42	HW	7/24/2010	COMPAL	Follow GPIO map to add touch screen power down control circuit	Add TOUCH_SCREEN_PD#, Q125,Q32,R430,R431,C304,C306, and change JTCH1 pin 1,pin2 from +5V_RUN to +5V_TSP	X01
94	24	HW	7/26/2010	COMPAL	Reserve a 0 ohm resistor for +5V_TSP	Add R1592	X01
95	45	HW	7/26/2010	COMPAL	Add pull down 100k on BT_ACTIVE	Add R950	X01
96	15	HW	7/26/2010	COMPAL	Add BOM structure for TCM	Use 4@ for RH311	X01
97	37	HW	8/23/2010	COMPAL	Add connection for express card SW	Add connection of pin4,pin5,pin13 and pin 14	X01
98	18	HW	8/23/2010	Intel	Follow Intel design guide Rev1.2	Change RH149 to 2.2k and RH150 to 0 ohm	X01
99	10	HW	8/23/2010	COMPAL	For better return path	De-pop CC129,CC130 and pop CC133,CC134	X01
100	14, 18, 30	HW	8/23/2010	DELL	Remove PAID function of RTC and speaker	Change speaker connector to 4 pin and remove RTC_DET# and SPEAKER_DET#	X01
101	17	HW	8/26/2010	Intel	Follow Intel check list rev1.2	Add @RH332	X01
102	14, 18	HW	8/26/2010	Intel	Follow Intel request	Add RH51 and RH356	X01
103	33	HW	8/27/2010	BRCOM	Follow BRCOM request	Change L39,L40 to rated current is 400ma	X01
104	26	HW	8/27/2010	Intel	Follow Intel design guide rev1.2	Remove R1164,D65, change R1128 to 20k,	X01
105	45	HW	8/27/2010	COMPAL	Follow ME request	Add H21	X01
106	16	HW	8/27/2010	COMPAL	Reserve pull down R for ME_SUS_PWR_ACK	Add @RH145	X01
107	36	HW	9/2/2010	COMPAL	De-pop ESD diode	De-pop U40	X01
108	11	HW	9/2/2010	COMPAL	Change QC5 VGS to 20V part	Change QC5 to SB00000HK0L	X01
109	26	HW	9/3/2010	COMPAL	Follow safety request	Pop F2 and de-pop R5	X01
110	24	HW	9/8/2010	COMPAL	Change RB751V to HF part	Change D63,D64,D68,D69 to SCS00004L0L	X01
111	30, 31	HW	9/9/2010	IDT	To solve pop noise and detect issue	Add U6, Q33, Q46, D70, D71, R425, R33, R38, R424, R161, R352, R1088, C967, C307, C308	X01
112	35	HW	9/10/2010	O2	To solve RF noise issue	Add @C573,@C574, L45	X01
113	30, 38, 39	HW	9/14/2010	COMPAL	For EMI request	Change C973~C976 to 680pF and pop, add L91~L94, D72~D74, remove U90~U92	X01
114	35	HW	9/14/2010	O2	Modify circuit	Remove R661,R662, add L46,L47, change L45 to SM01000GG0L	X01
115	17, 24, 32, 41, 43	HW	10/11/2010	DELL	Follow GPIO Map	Remove R771, add U15,C478, change LVDS_CBL_DET# to ATG_MAC_LCD_DET#, TP_DET# to WLAN_LAN_DISB#	X02
116	24	HW	10/11/2010	DELL	Solve PWM leakage issue	Change R1137 to 10k	X02

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117	14	HW	10/11/2010	COMPAL	DG1.5 update	Add RH31	X02
118	45	HW	10/11/2010	COMPAL	LED brightness test result	Change R957 to 1k, R955,R941,R949,R939,R934 to 4.7k	X02
119	32	HW	10/11/2010	COMPAL	Solve LAN package lost problem	Change L30~L37 to 12nH	X02
120	9	HW	10/11/2010	COMPAL	DG1.5 update	Depop RC96,RC97	X02
121	30	HW	10/11/2010	COMPAL	Change codec to YA version	Change PN from SA00003ZZ1L to SA00003ZZ2L	X02
122	31	HW	10/11/2010	DELL	Remove Latitude On button	Depop SW2	X02
123	32	HW	10/11/2010	COMPAL	Change LAN to C0 stepping	Change PN from SA00003SI1L to SA00003SI2L	X02
124	28	HW	10/14/2010	DELL	Support SSD	Add PJP64,C399,C402	X02
125	38,39	HW	10/15/2010	COMPAL	For layout routing	Swap D72~D74 pin 2 and pin 3 for better USB routing	X02
126	31	HW	10/18/2010	IDT	Change GND reference	Change Mic detect circuit DGND to AGND	X02
127	37,38,39	HW	10/18/2010	COMPAL	Link CIS	Link CIS for L49,L51,L52,L90	X02
128	30	HW	10/18/2010	COMPAL	Change Mic detect to external detect	Remove R161 and add C1164	X02
129	14,18	HW	10/19/2010	COMPAL	Follow Intel debug port DG	Connect PCH_GPIO15 to PCH XDP	X02
130	42	HW	10/19/2010	COMPAL	Change borad ID to X02	Change R875 to 62k	X02
131	30,31	HW	10/21/2010	COMPAL	Modify Mic detect circuit	1. Add PJP65, 2. Change C307,C308 to 0402 size 3. Change C308 connection, 4. Change Mic detect power from +5V_ALW to +5V_RUN, 5. De-pop Q33,Q46,R424, 6. Move C1180 to +VREFOUT_R	X02
132	18	HW	10/21/2010	COMPAL	Follow check list	Change RH177 to 10k	X02
133	9	HW	10/25/2010	COMPAL	Follow Intel DG	De-pop RC120~RC123	X02
134	14~21	HW	10/28/2010	COMPAL	Change PCH stepping	Change UH4 to B2 stepping	X02
135	15	HW	11/5/2010	COMPAL	To fix ME issue	De-pop RH296,RH297, pop QH5,RH302,RH303	X02
136	25	HW	11/9/2010	COMPAL	To fix VGA SW EOS issue	Change C317,C318 to 0.01uF	X02
137	37	HW	11/16/2010	COMPAL	To fix soldering issue	Change express card connector JEXP1 to TAISOL 5-421005002000-9	X02
138	28	HW	11/17/2010	Intel	Follow CRB design	Change R501,R502 to 10k	X02
139	12,13	HW	11/18/2010	COMPAL	Follow part reference design rule	Change JDIMMA1 & JDIMMB1 to JDIMM1 & JDIMM2	X02
140	28,44	HW	11/19/2010	COMPAL	For cost saving	De-pop R499,R500,C393,Q28,R905,R907,C762,Q51	X02
141	31	HW	11/22/2010	COMPAL	Follow part reference design rule	Change JMEDIA1 to JMDIA1	X02

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142	18	HW	12/17/2010	COMPAL	Audio MIC detect selection	Add @RH273	A00
143	42	HW	12/17/2010	COMPAL	Follow INTEL DGl.5 RSMRST# timing cicuit	Just add RSMRST# circuit for backup. but de-pop	A00
144	34	HW	12/17/2011	COMPAL	Follow NXP design guide	Add @C575	A00
145	14	HW	12/17/2011	COMPAL	For cost saving	De-pop RH47, RH48, RH49, RH288	A00
146	42	HW	12/20/2011	COMPAL	Change Board ID	Change R875 to 33k	A00
147	42	HW	12/21/2011	COMPAL	To solve backdrive issue	Pop Q45	A00
148	33, 34	HW	12/24/2011	COMPAL	Change USH chip to CID7	Change U33 to SA00003A01L	A00
149	34	HW	1/6/2011	COMPAL	update TPM/TCM pop option table	Correct pop option table	A00

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