Lab 1: Schematic and Layout of a NAND gate

This document contains instructions on how to:

- Make a layout for your NAND gate.
- Run a DRC and LVS
- Extract your circuit with capacitive parasitics.
- How to simulate using your extracted NAND gate.

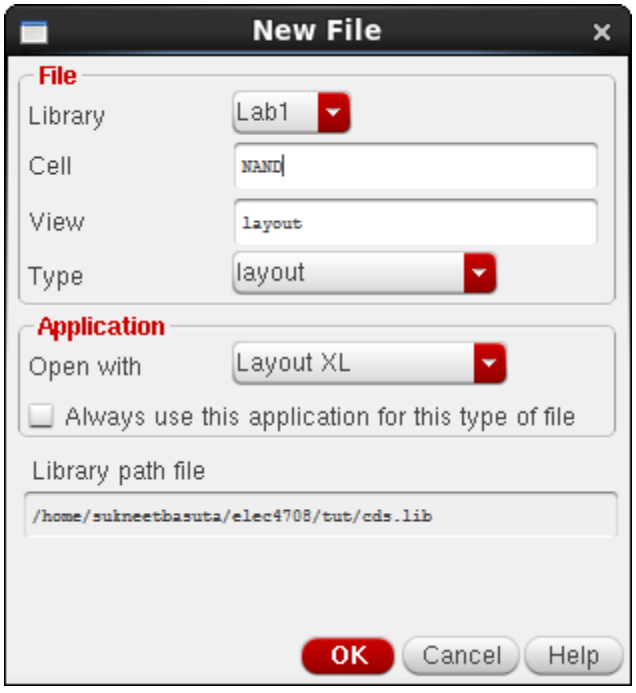
Note: Go through the whole document before you start. You will save time in the long run

Before starting make sure to change the widths of your NAND gate to those in Step 1 in Part A and to make sure the bulk connections of the NMOS transistors are connected to GND.

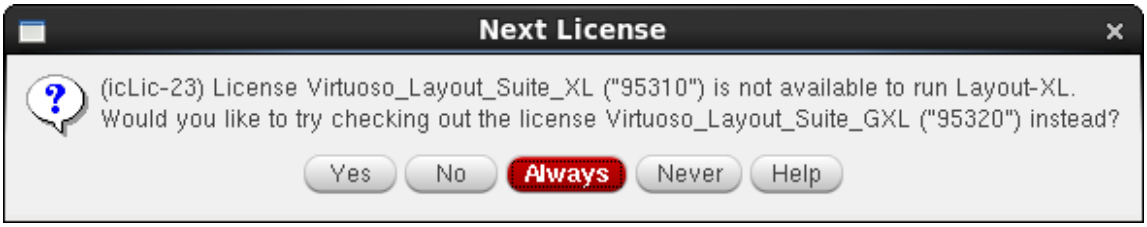
Part B: Procedure

Create Layout view

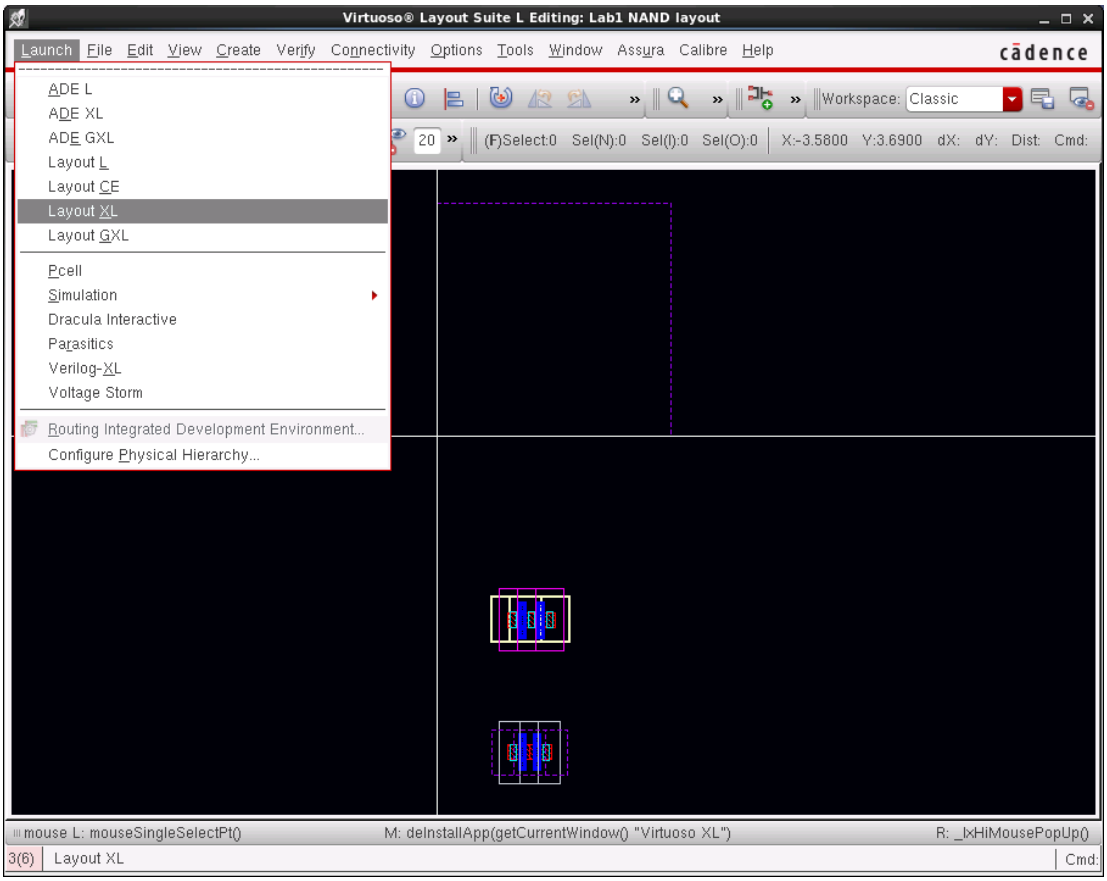
1. Make sure that Lab1 and the NAND cell view are highlighted in the "Library Manager" and from the "File" drop down menu select "New->Cell View"
2. In the "Create New File" window that pops up, change the "Type" to layout. Make sure that:
    a. "Library Name" is the name of your Lab1 Library
    b. "Cell Name" is the name of your NAND cell
    c. Change the Open With Application to "Layout XL"



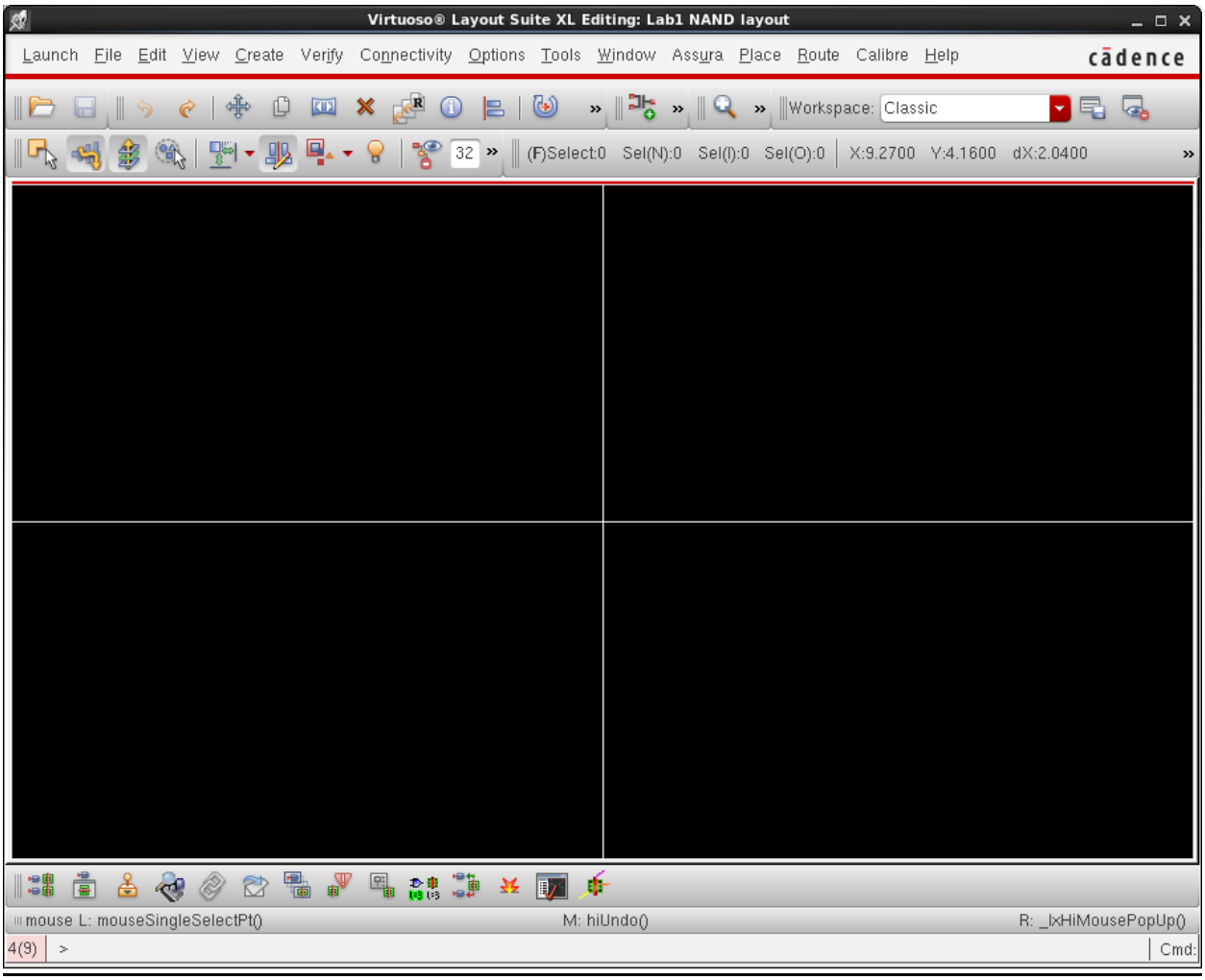
3. Close the “About what’s New Window”.
4. If you get a licensing issue, select “always”



5. If you ever reopen the layout view from the library manager, you will most likely open it in Layout L (the window title will be Virtuoso Layout Suite L and you will be missing the bottom toolbar). To open Layout XL, select **Launch -> Layout XL**



Virtuoso Layout Editor



Virtuoso Layout Editor is the layout editor of the Cadence design tools. Commonly used functions can be accessed through a button bar on the top of the editor.
Browse through the various menus to familiarize yourself with menus, items, and shortcuts. In preparation for drawing our design, the grid of Virtuoso needs to be set to match the spacing required for the target technology. Execute the following commands to set the grid appropriately:

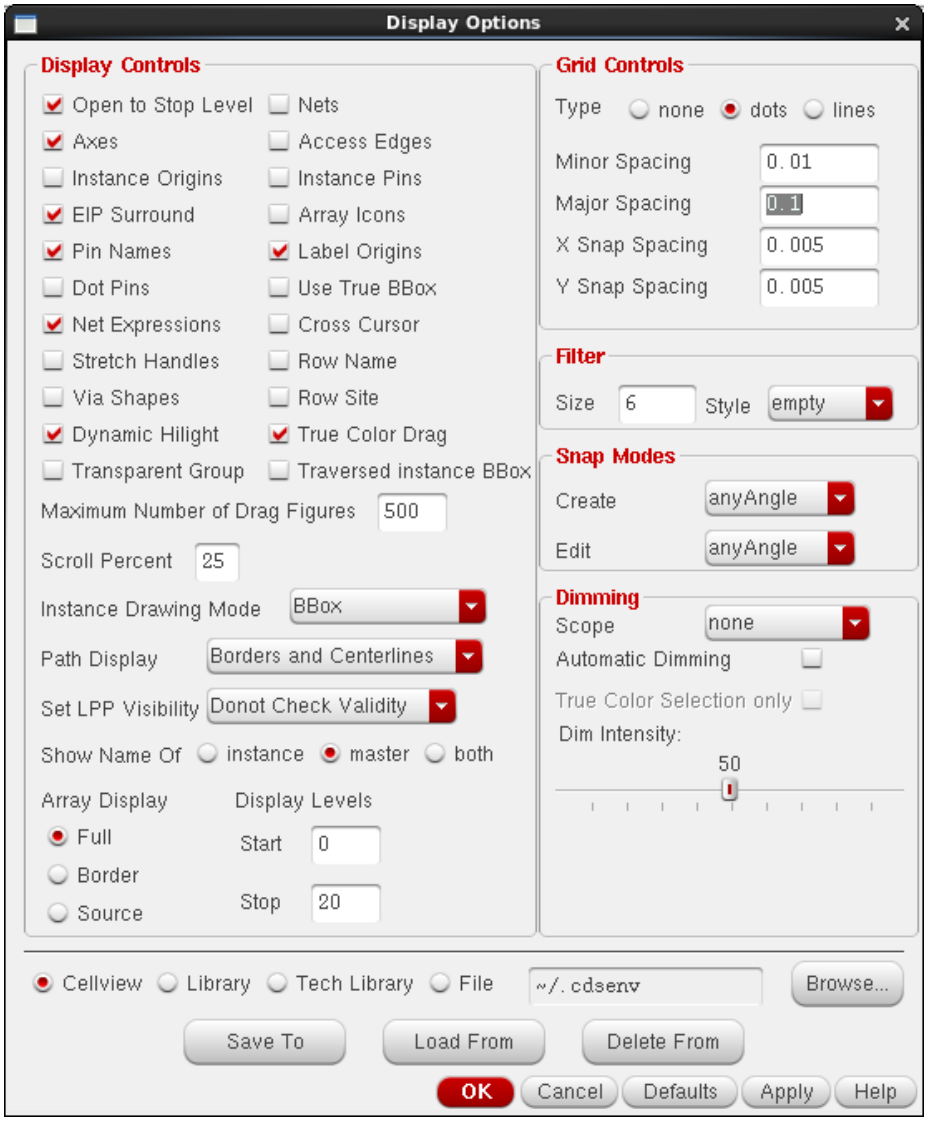
a. Select **Options -> Display i**n the Virtuoso window. The Display Options window appears.
b. Set the following fields in the Display Options window:
    I. Minor Spacing: 0.01,
    II. Major Spacing: 0.1,
    III. X Snap Spacing: 0.005,
    IV. Y Snap Spacing: 0.005,
    V. Display Levels:
        1. Start: 0, and
        2. Stop: 20, and

VI. Check Pin Names under Display Controls

VII. Make sure Snap Modes are set to “anyAngle”

VIII. Click “Save To” in the Display Options window.

c. Click OK in the Display Options window to close it;



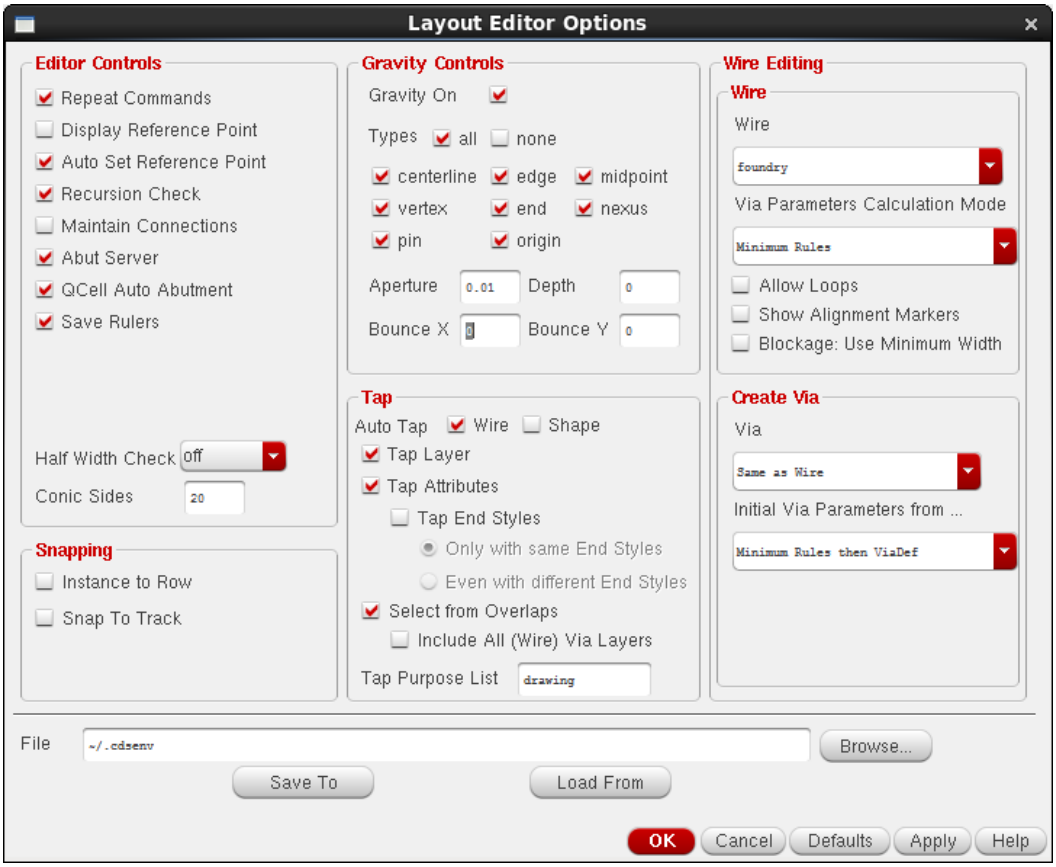
d. Select **Options -> Editor** in the Virtuoso window. The Layout Editor Options window is displayed;

e. Set the following fields in the Layout Editor Options window:

i. Turn Gravity On,

ii. Aperture: 0.01,

iii. Click “Save To” in the Layout Editor Options window. The aperture setting controls how close you have to be to snap to an object.

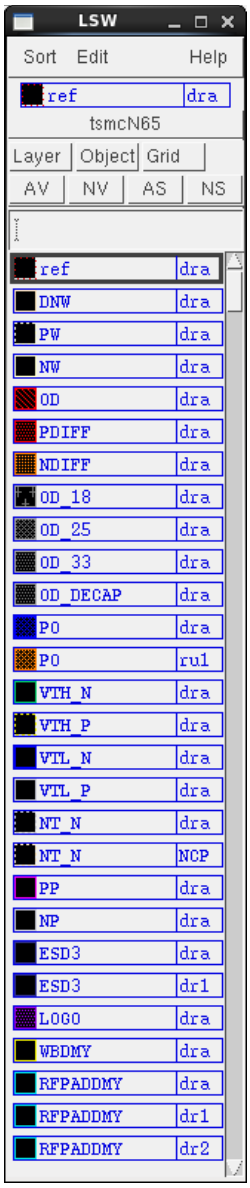


There are a few commands that will be useful to you while you are drawing the design: zoom, ruler and clear rulers. Listed below are the commands to execute them:

a. Zoom: select **View -> Zoom -> To Grid** to get closer to the working dimensions;
b. Ruler: select **Tools->Create Ruler** Click and drag the mouse across the drawing area of the Virtuoso window. It displays a ruler. To finish the ruler, you need to click the end point as well. Note that rulers are created only horizontal or vertical; and
c. Remove Rulers: To remove the rulers, select **Tools -> Clear All Rulers** from the Virtuoso window.

   To delete a single ruler, select the delete button in the top toolbar (or select **Edit -> Delete**) and select the ruler you wish to delete.

When you opened the Layout Editor, you may have also noticed the LSW window open.
The Layer Select Window (LSW) shows all the available layers that you can use in creating your layout. When manually creating shapes, you will need to select layers from this window. You can also select layers to hide and/or show. This may be useful when trying to fix issues.

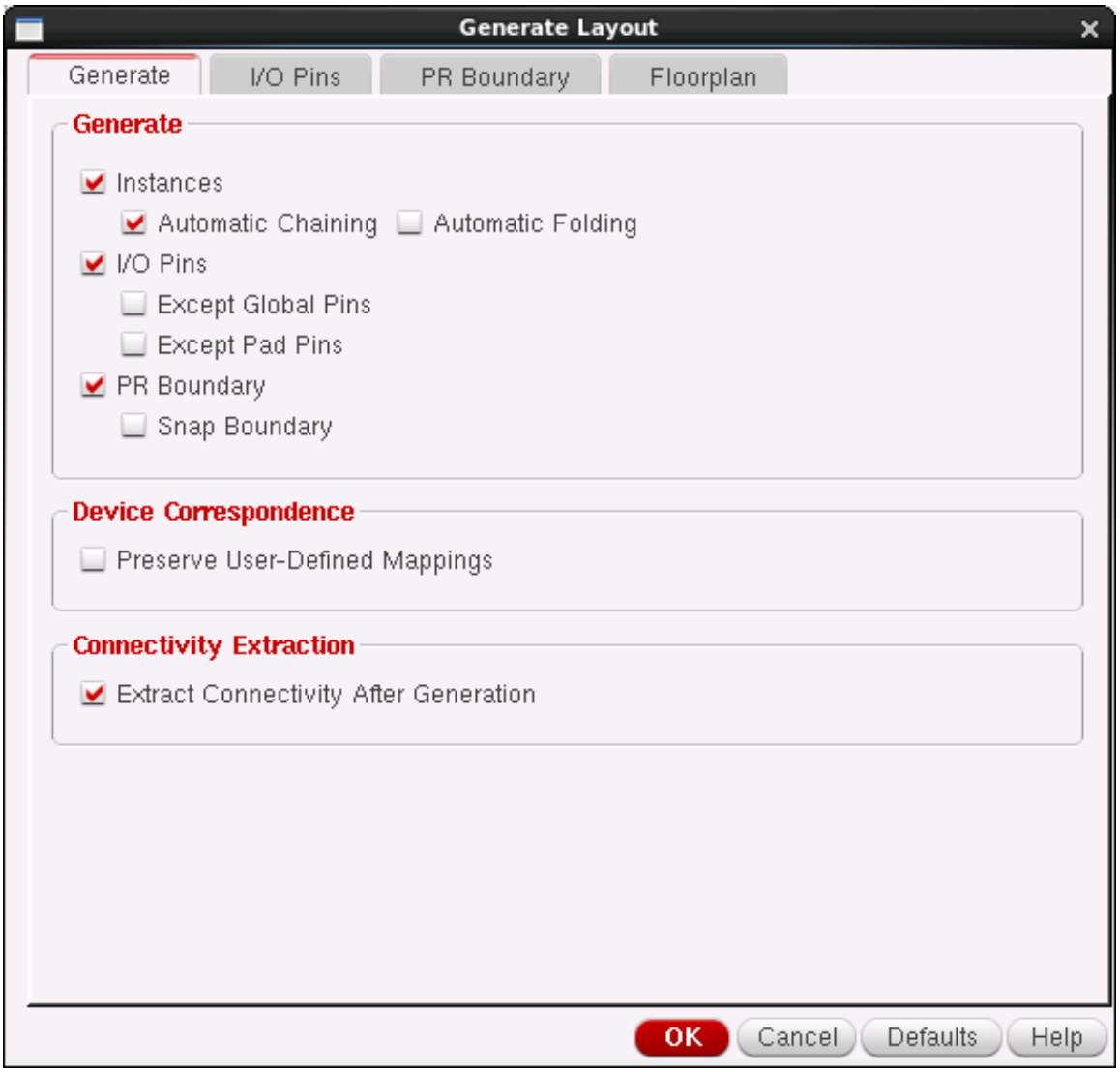


You are now you are ready to create your layout.

Adding components to the layout

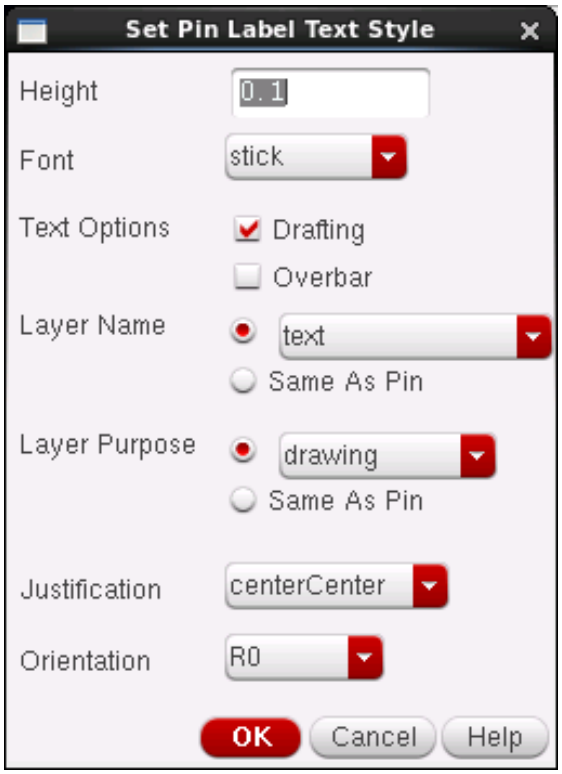
If you wish, you can manually draw each layer of each component. However, this would be time consuming and would probably drive you crazy. Technology kits often provide pre-made scalable components (usually called pCells) to match your design requirements (i.e. to match your schematic). You could individually add each component to your layout by adding an layout instance of each cell (click on  or select Create -> Instance (shortcut key ‘i’) and add each device like you did in the schematic, but select the layout view), but a better way is to have Cadence generate the layout components based on the schematic. This will add each corresponding device to the layout and automatically set the device properties (i.e. transistor widths and lengths).

6. To generate the layout, select **Connectivity -> Generate -> All from Source** (or select the Generate All From Source button  in the bottom toolbar)
7. The Generate Layout window will popup. Select “Automatic Chaining” to automatically join instances where possible.

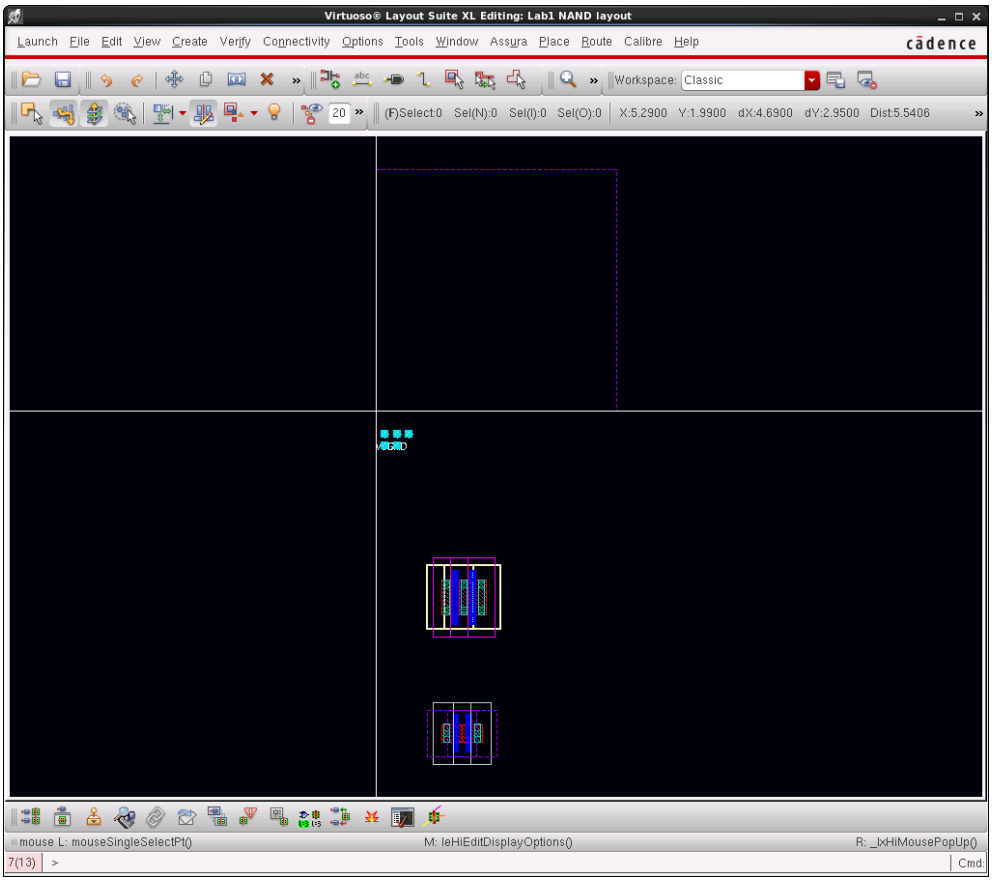


8. Select the I/O Pins tab and change the default layout for all Pins to M1 – pn (Metal 1 - pin). Why we do this will become apparent later.

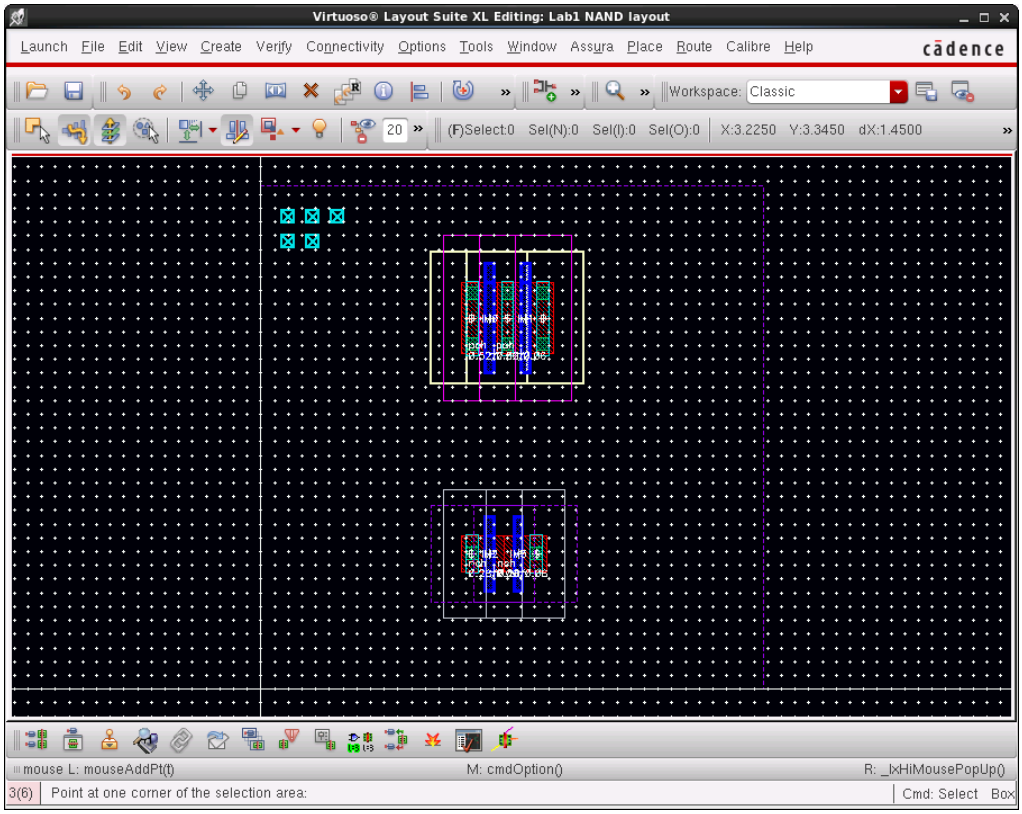
9. Check “Create label As” under Pin label and Hit the Options Button to change the text Height to 0.1. (You can also change the layer name to M1, and Layer Purpose to Pin to skip a step later, but I like to do this at the end, in case I have to change the Pin layer)



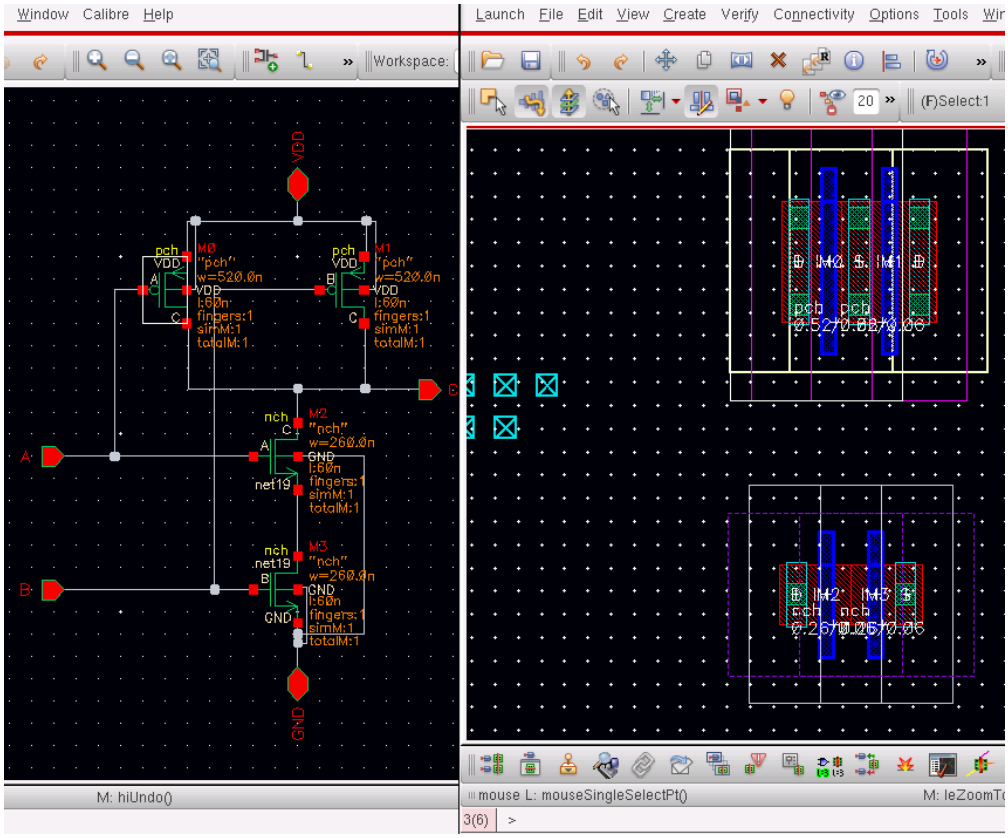
10. Hit Ok to have Cadence automatically place the devices in the layout. You should have something similar to the image below. The devices and pins are shown outside a bounding box. This bounding box is an estimate of the optimum size of the final layout. It is not necessary to have this bounding box in your layout, but it is good practice to do your layout within this box and helps keep your layout from being large. Additionally, putting devices in this boundary allows you to have Cadence automatically route the wires for you. This can be done be selecting Route -> Automatic Routing… and hitting run in the popup window. However, without constraints and rules, the routing is rarely optimal. Thus, in this case, we shall manually route the wires.



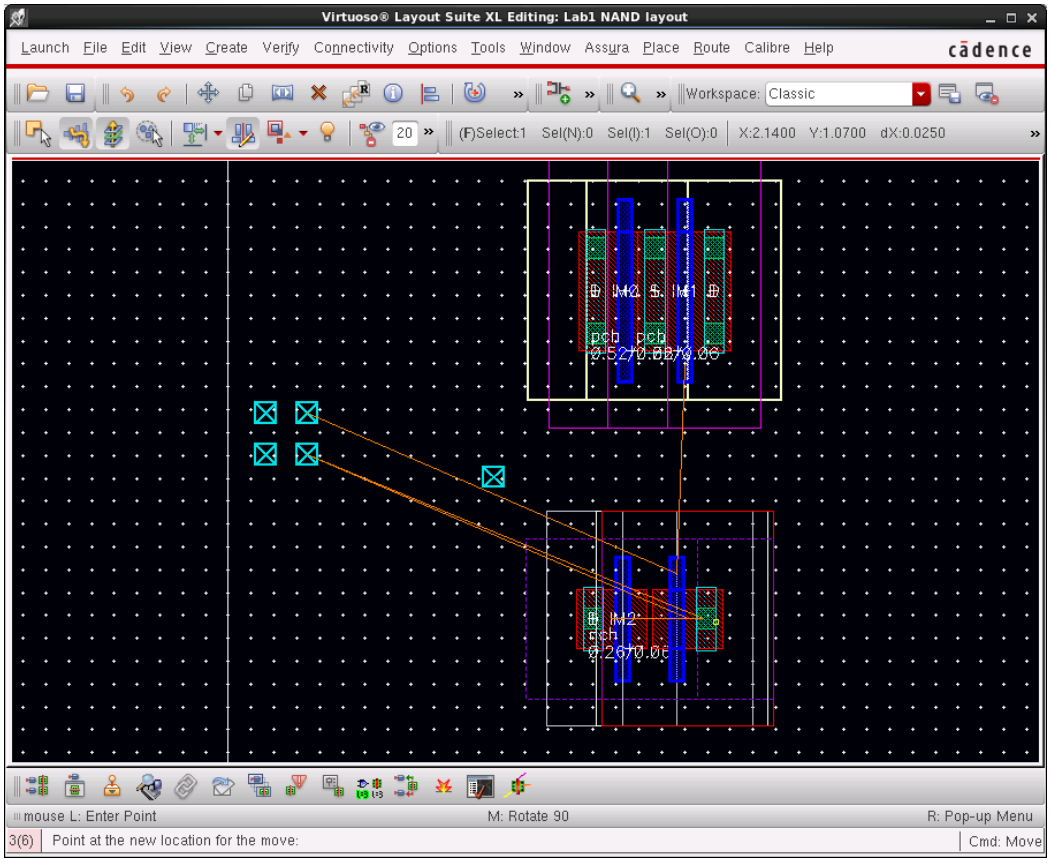
11. Place your components and pins within the bounding box.



12. Before we move on, there are some useful features in Layout XL that will make your life easier when doing layouts.
    a. Selecting a device in the layout view will highlight the device in the schematic view. This makes it easy to discern each device from each other.



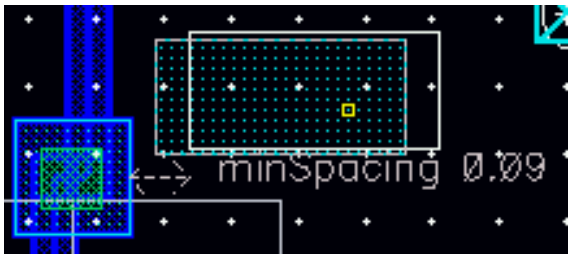
    b. Moving a device or pin will show lines that indicate its net connections.



c. Later on in the Lab you will run a Design Rule Checker to verify your layout doesn't violate any design rules. However, if you don't already know the rules, running verification after you have already made your layout can be a time wasting process because you will most likely have to make changes to satisfy the rules. Thankfully, there is a tool that can inform you of some the design rules while creating the layout, DRD.

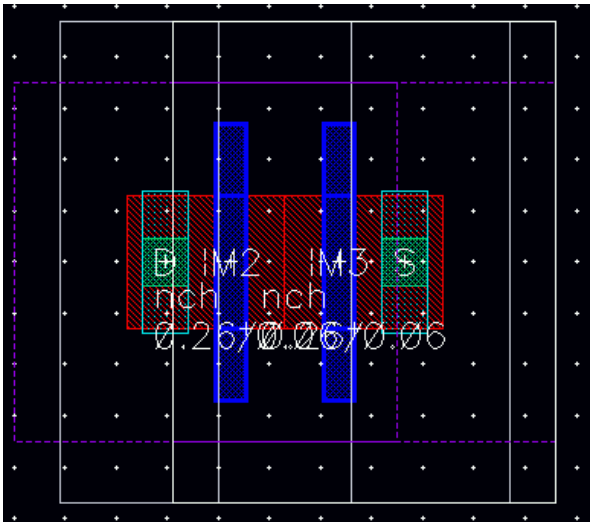
To Enable DRD, select Options DRD Edit. The DRD Options window will popup. There are 3 modes: Off, Notify, and Enforce. Notify will inform you if you are violating any design rules. Enforce will prevent you from placing anything that violates a design rule. You can also enable DRD by clicking the DRD dropdown in the top toolbar ( -- Off,  --Notify,  -- enforce). I recommend DRD Notify as it prevents you from doing anything wrong, and DRD Enforce will drive you crazy since it does not take into account existing layers of the same type.

DRD Notify: (you can still violate the rule)

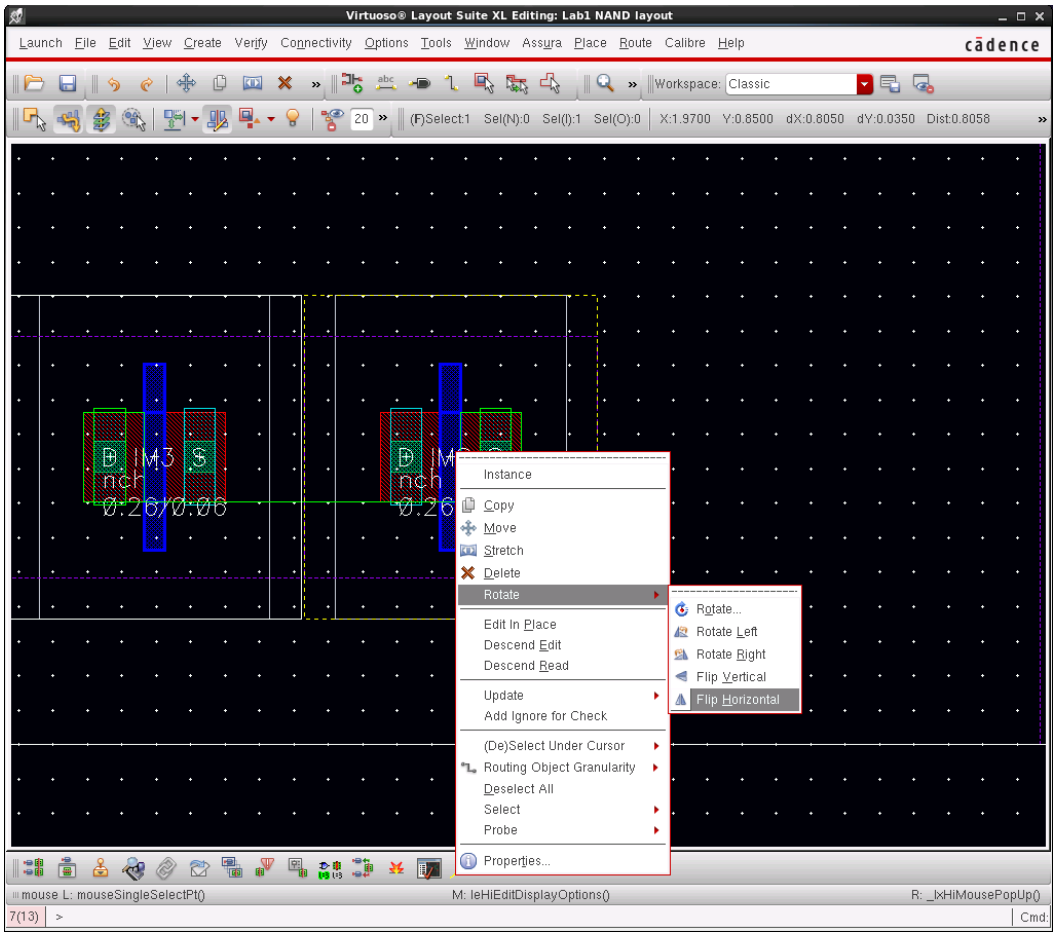


DRD Enforce: (you cannot violate the rule)

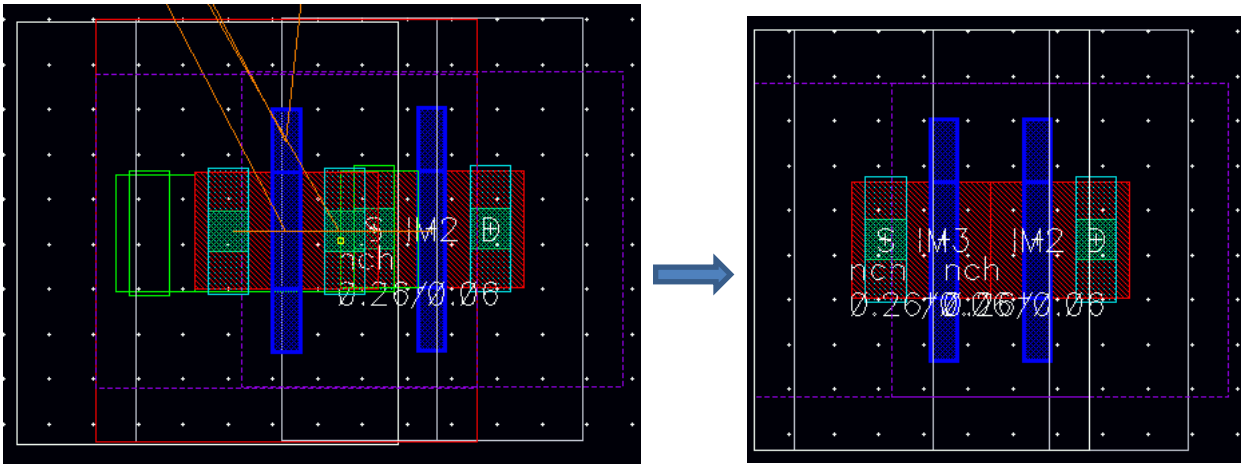
d. We had cadence automatically chain the transistors for us, but what if the chaining order is not what we want (i.e. in the diagram below, the Drain and Source of the NMOS transistors are chained, but we want to flip it around so that the drain of the NMOS closest to the output is close to the output)



To break the chain, drag the transistors apart. Move one device to the other side, Right click the device, and select **Rotate -> Flip Horizontal.** Do this to both devices.

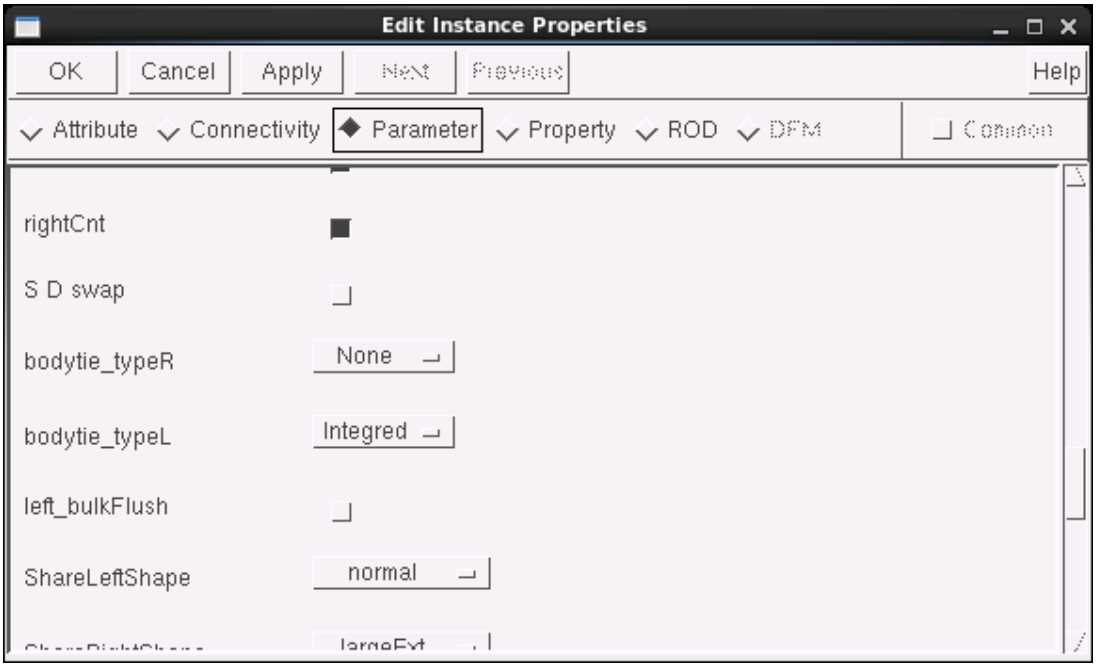


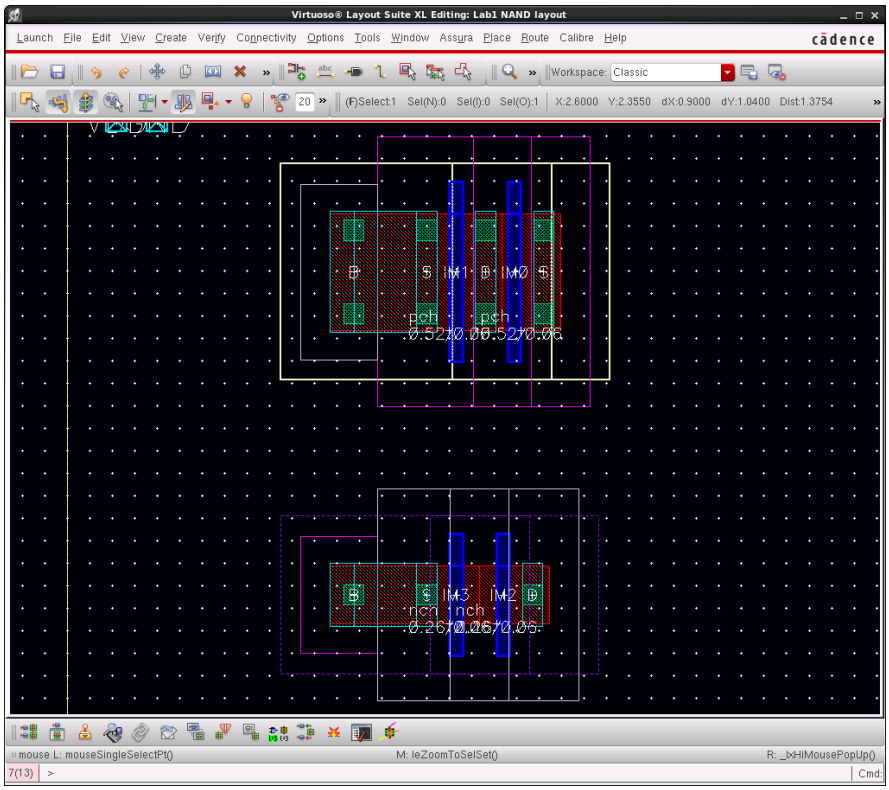
Once they have both been rotated, drag the devices on top of each other and they should chain together.



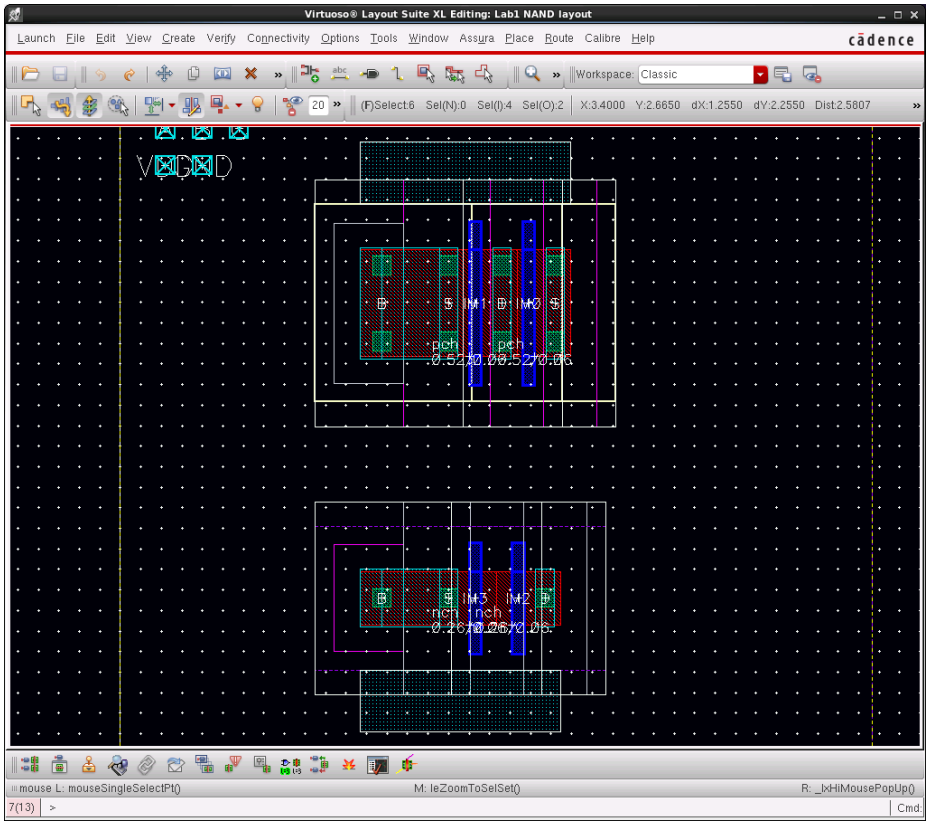
However, now the gates of the NMOS and PMOS transistors are misaligned. To fix this, change the order of the chaining of the PMOS transistors. Simply drag one transistor to the other side.

13. Before we start routing the wires, lets add a bulk connection (you only really need 1 for the pair of PMOS transistors and 1 for the pair of NMOS transitors). To do this, go into the properties for the device (right click device and select properties, or select Edit -> Properties).
14. Select the Parameter tab. In the parameter section you can change the width and length of the transistor, change the number of fingers, or add a substrate contact. To add a substrate contact, scroll down until you see bodytie_typeR and bodytie_typeL. bodytie_typeR will add a substrate contact next to the Drain, and bodytie_typeL will add a substrate contact next to the Source. In the drop down menu next to these parameters, you will see None, Integred, and Detached. Integred will attach the contact to the Source/Drain, and Detached will keep it separate. Since we want it attached to the Source, set bodytie_typeL to Integred.

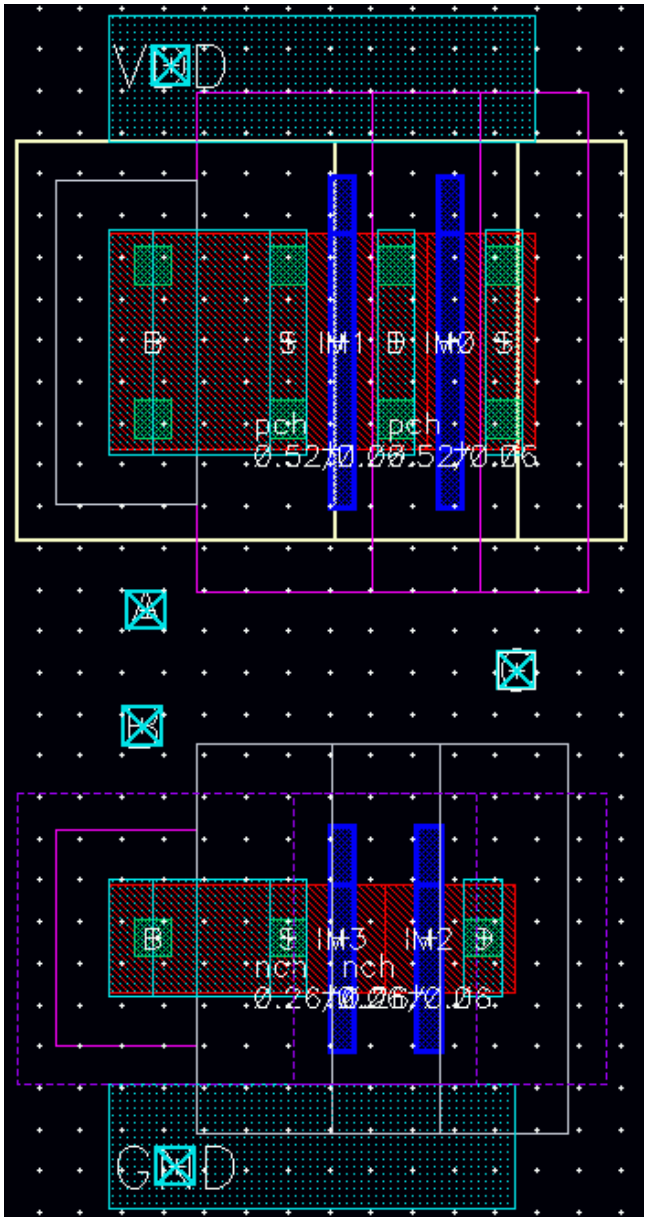




15. Let's place the power rails (VDD and GND). To do this, select the M1 – dra (Metal 1 – drawing) layer in LSW and select **Create -> Shape -> Rectangle** (Shortcut Key **'r'**). Now draw a rectangle above the PMOS transistors and below the NMOS transistors.



16. Place your pins in the location where you want them. You can do this step later, but it will make routing easier if you have an idea where they will be.



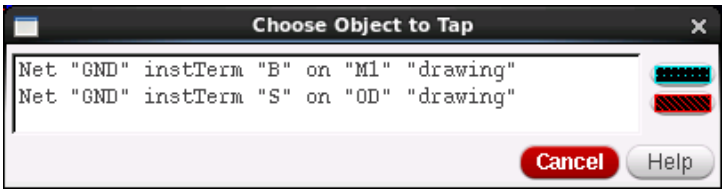
Wire Routing

17. Now do the routing. There are several ways you can route the wires (in order of automation): You can create the wires with shapes (like you did for the power rails), Use wires/paths, Use Point to Point routing (Create->Point To Point – Ctrl+Shift+P), Guided Routing (Create->Guided Routing – Ctrl + Shift+G), and Automatic Routing (Route -> Automatic Routing…). You can use any combination of these to achieve your goal.

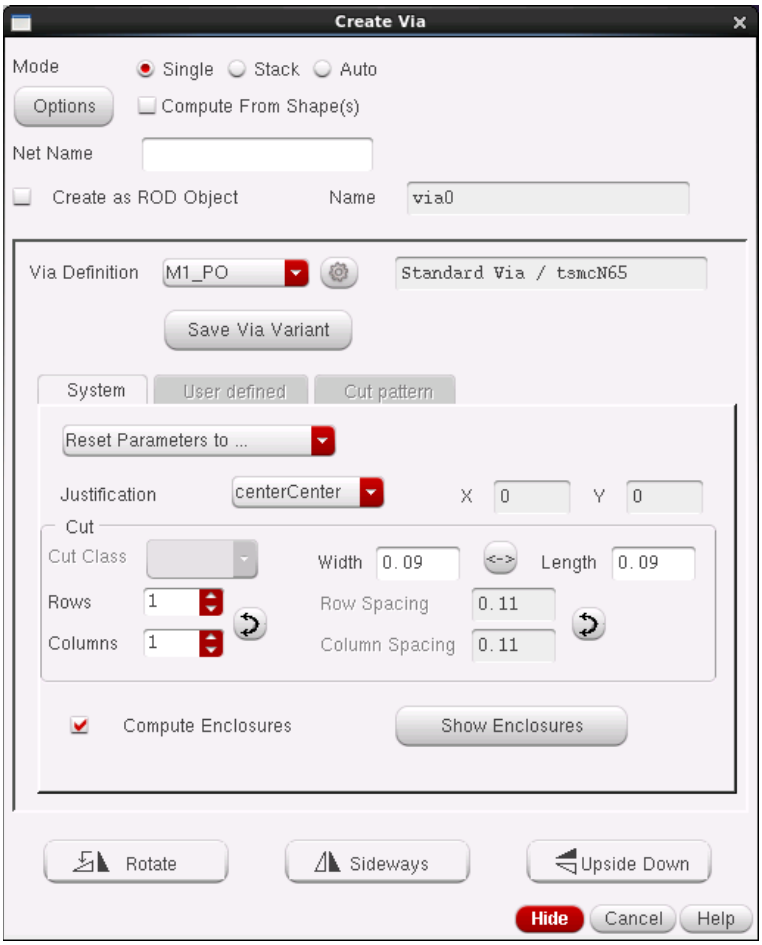
    Using shapes can be time consuming and annoying, but maybe the only way to get a layout you want. Wires will automatically select a single layer for the wire, create bends as you need them, and will try to enforce design rules (if you have DRD set to enforce). Paths are similar to wires,

but will enforce DRD (if DRD is set to enforce) and only creates minimum sized wires. Point to Point routing will automatically join 2 selected points using however many layers and vias it needs. Guided Routing is basically automatic routing with manual intervention (you can control where there wires go). Automatic routing will automatically connect all the nets in the prBoundary together. The latter 3 cases rarely optimally route wires and can result in odd layouts. Thus, I recommend using wires. If you want to use some form of automatic routing, Point to Point routing will most likely be the best choice.

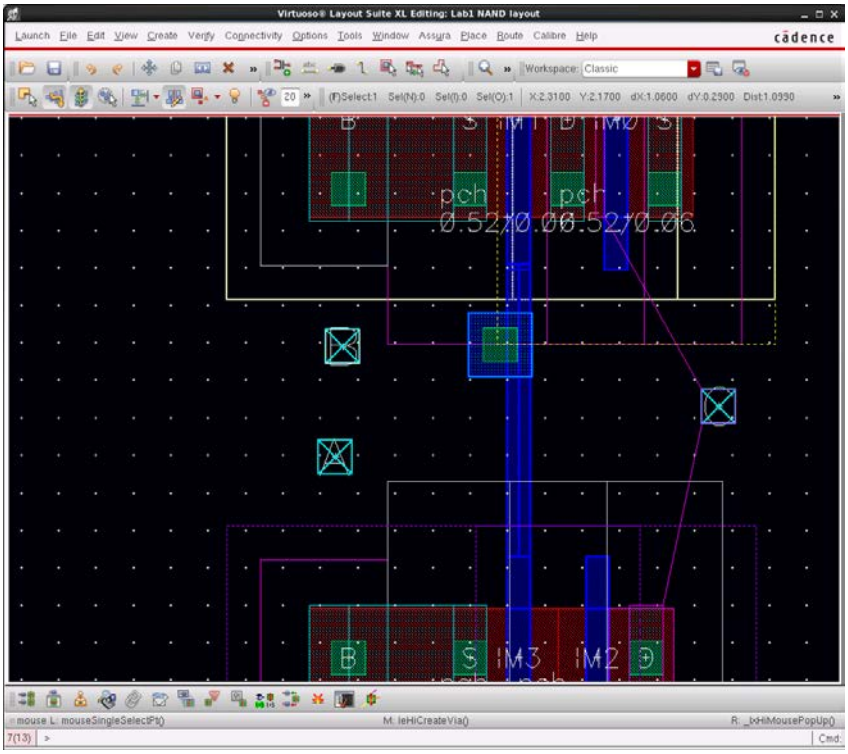
18. Select **Create->Wire**, or click the Create Wire  button in the top toolbar (Shortcut key Ctrl+Shift+W). **OR** select **Create-> Multipart Path**, to create a path. Select the metal contact of the Drain or Source, or the Poly-silicon of the gate, and draw a wire to wherever you desire. Note that it is okay for layers of the same type to overlap.
19. If a window pops up asking you to select an Object to tap, you most likely want the M1 layer.



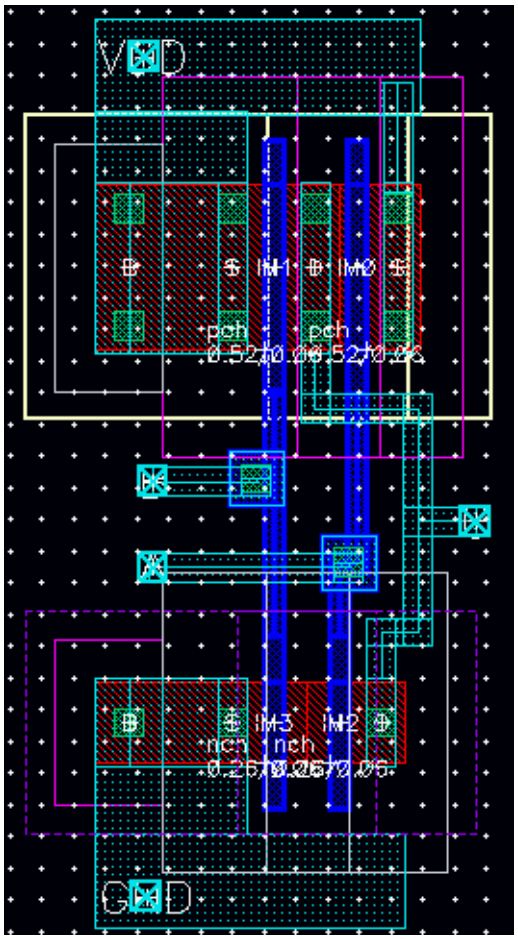
20. The downside to using the wire is that you cannot just connect 2 different layers together. First you must add a via to connect the layers. To create a via, select **Create->Via**, or select the Create Via  button (Shortcut key ‘o’).
21. The Create Via window will popup. To select the Via type, select the Via Definition drop down menu and select the 2 layers you want to join. For example, if you wanted to join Metal1 (M1) to Polysilicon (PO), you would select M1_PO. If you wanted to join Metal3 (M3) to Polysilicon (PO), you’d have to make a via from M3 to M2, then M2 to M1, and then, finally, M1 to PO.



22. Add the Via to your layout

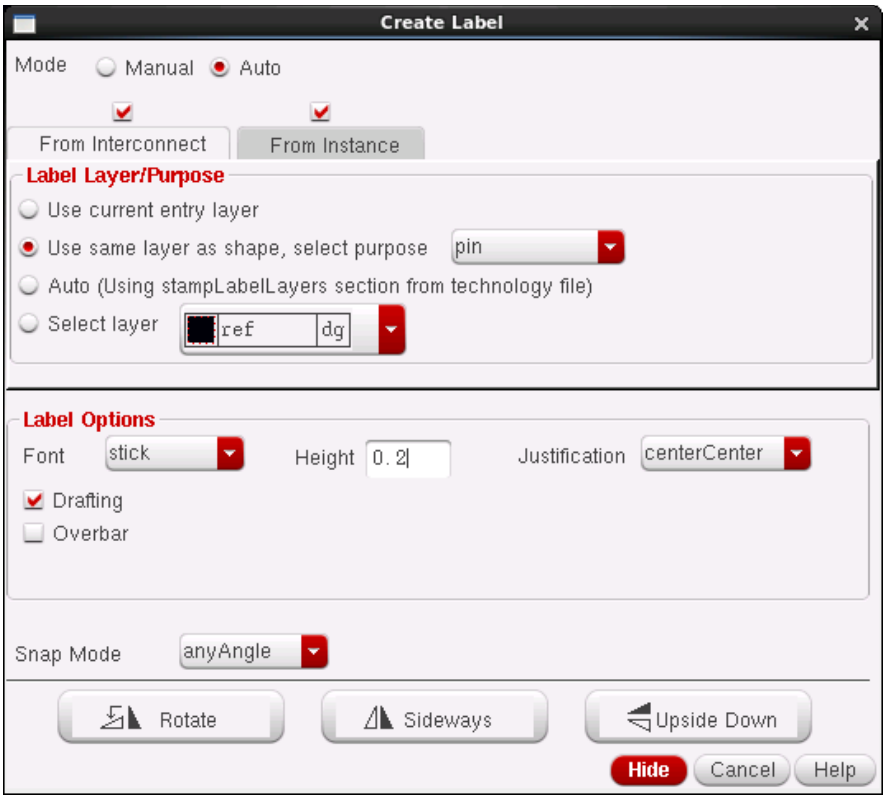


23. Wire up the rest of your layout. Using Point to Point (**Create -> Point to Point** – Ctrl+Shift+P), or manually creating shapes may help you wire up your design. (Don't be concerned if your layout is not exactly the same)

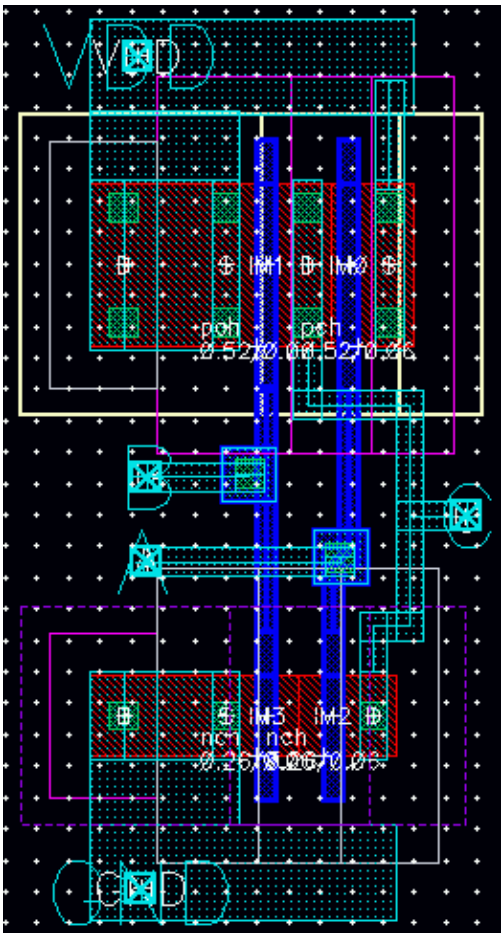


24. You can check for any incomplete nets by selecting **Connectivity->Nets->Show/Hide Selected Incomplete Nets**.
25. Before we move on, we need to label each pin for a later step (LVS and extraction). Select Create->label (or hit the Create Label 

Button on the top toolbar, or use shortcut key 'l').
26. The Create Label window will popup. Change the Mode to Auto, select "Use same layer as shape", set the purpose to pin, and change the Label Height to 0.2 (or smaller).



27. Select all the pins in your layout to give them a label.



Important Hints, Tips and Rules

- It's usually a good idea to make standard cell layouts so you can easily connect different layouts together to build circuits. Cells are normally connected side by side (not top to bottom).
    - The cells should be 3.6 microns, the width can vary (you can use the ruler to measure the dimensions of objects or map out an area to put an object down. The short cut is r in the Layout editor window)
    - The positive rail is on top (left to right), negative rail (or ground is on the bottom)
    - Make sure the rails stick out on either side so you don't violate any design rules when you connect cells together
    - Input pins are on the left and output pins on the right. Use metal 1 on the pins so you can connect from cell to cell in metal 1.
    - Don't place the I/O pins at the edge of your cell. You want them to be a little recessed so that they don't interfere with any other cells
    - Also, make your power rails extend a bit past the edge of your circuit (horizontally) so that your cells don't over lap.
    - Do all interconnect (internal cell connections) in metal 1, and if you need to crossover or are too close to a metal trace you can switch to metal 2 or metal 3.
    - Put all PMOS transistors on top and NMOS on the bottom

    - Make the pmos nwell as wide as the power rail so that you have one large nwell when you connect multiple cells together.

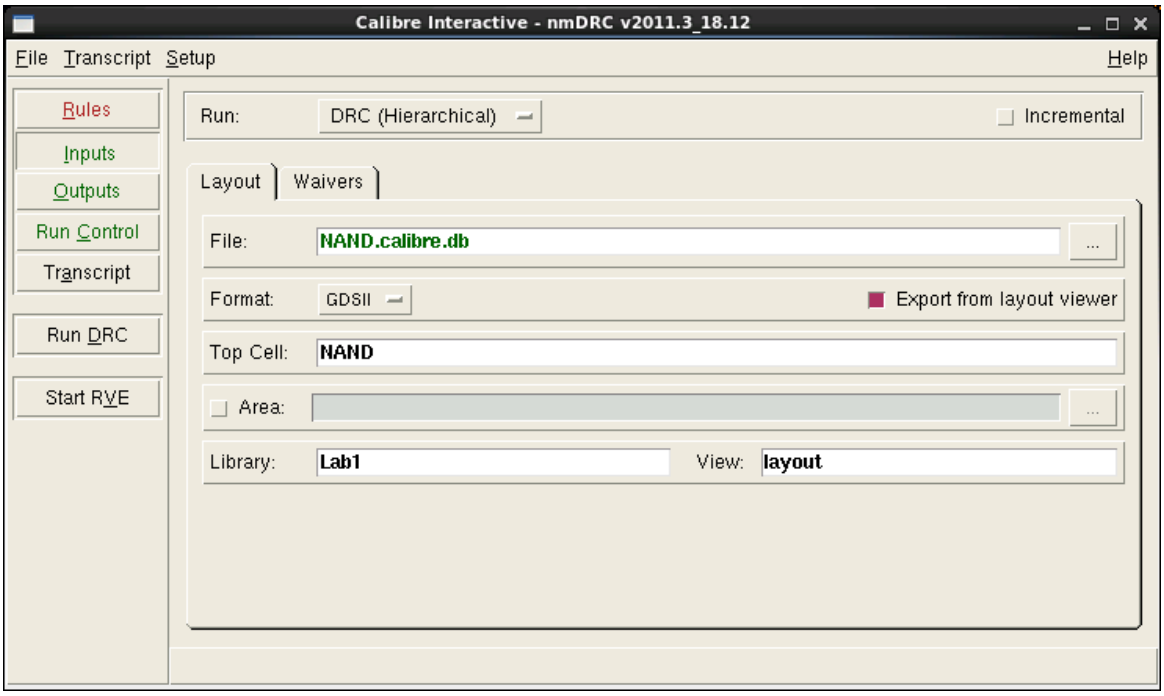
- Try not to run metal lines that are close together in parallel, you get lots of crosstalk if you do.
- Any long traces should be done in metal 1 if you can (the poly is highly resistive).
- Vias and contacts are highly resistive. You can't usually go wrong with putting down as many as you can.
    - Remember, size is important. Too big or too small is bad.
- Don't forget to ground all your substrate contacts for NMOS transistors and use the rail if the transistor is a PMOS.
- Some info on traces:
    - Wide metal lines have less resistance but more capacitance
    - Thin metal lines have lots of inductance and may not be able to handle the necessary current.
    - The design rules will have information that will help you choose the metal widths (they are in the following directory: /CMC/kits/cmosp18/doc/).
    - As a general rule:
        - Power and ground lines can be thick, metal interconnect is generally thin
    - Don't make 90-degree turns, use 45 degrees. A 90-degree turn puts a lot of electrical stress on the corner (not as important at slow speeds but can be very important in the GHz range).
- There are a lot of design rules about spacing between various layers, as well as sizes of things like contacts and how wide a metal line can be (without slotting), so run DRC often (see the next section).

At this point you should have all the tools necessary to create the NAND layout. The next step is to run a DRC.

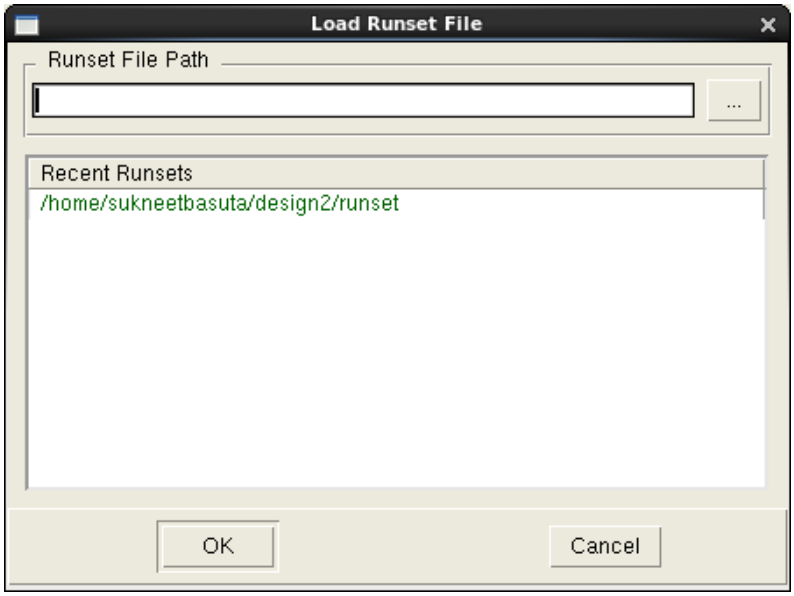
DRC

A design rule check (DRC) makes sure that your design complies with the fabrication guidelines (spacing, sizing, required layers, etc). In other words it makes sure that the fabrication facility can build what you have designed. It also does some simple checks to insure you haven't made any basic errors. Note: passing the DRC doesn't mean your design works.

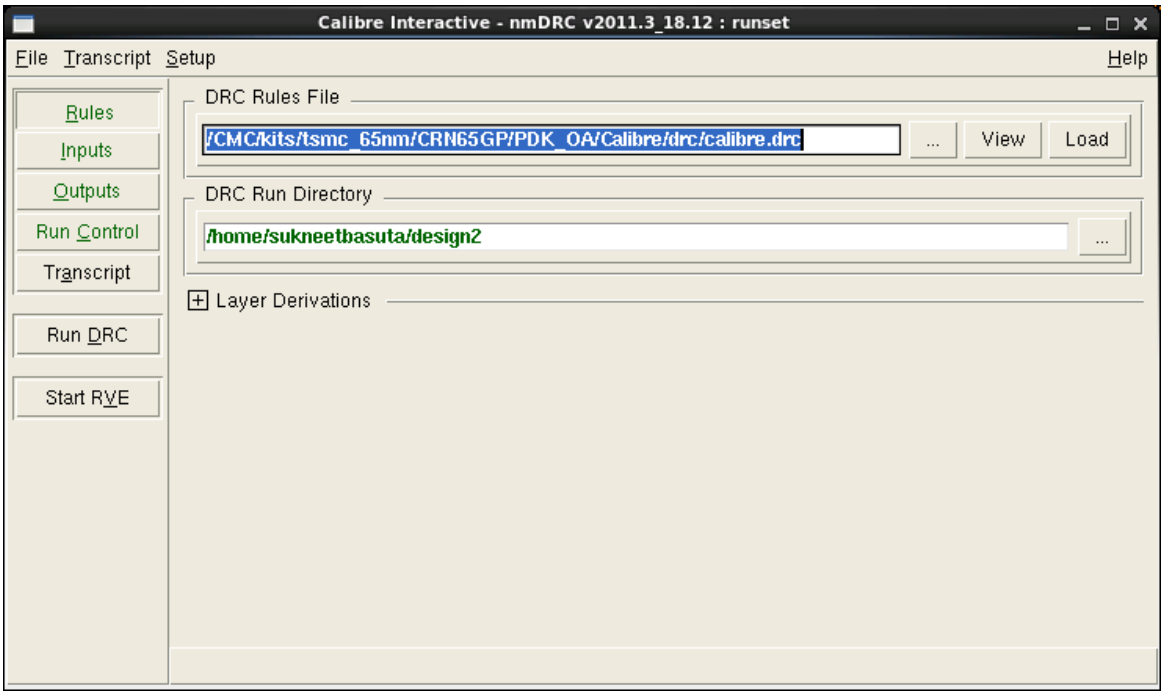
28. On menu bar, select **Calibre -> Run DRC**
29. The Calibre Interactive – nmDRC window will popup.



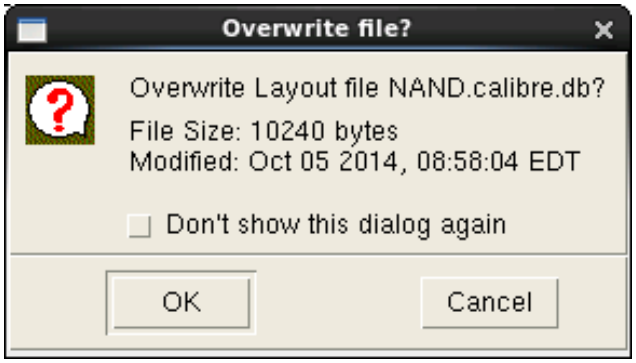
30. If a window pops up asking for a runset, hit cancel.



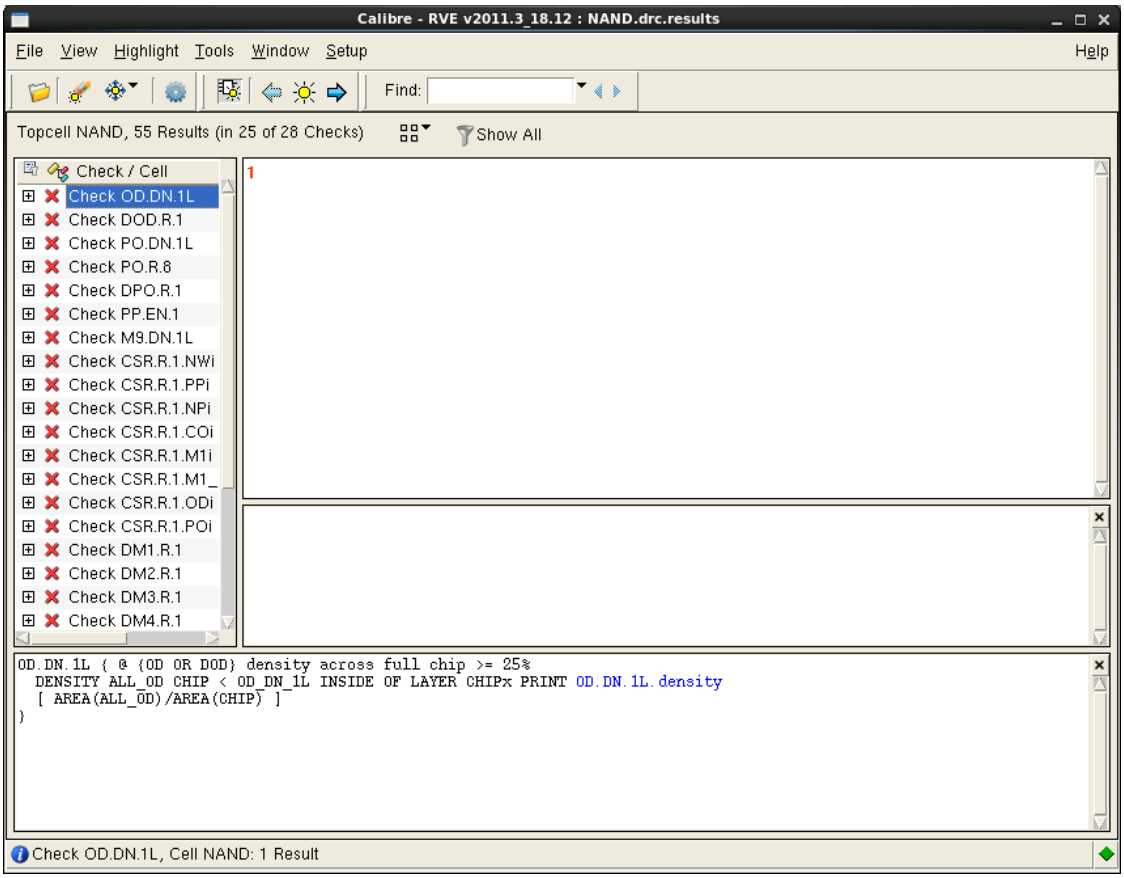
31. Select the Rules Tab on the left and set the DRC Rules File location to /CMC/kits/tsmc_65nm/CRN65GP/PDK_OA/Calibre/drc/calibre.drc



32. Now hit the Run DRC tab on the left.
33. If you have previously run DRC, you may get the following error. Select “Don’t show this Dialog again” and hit Ok.

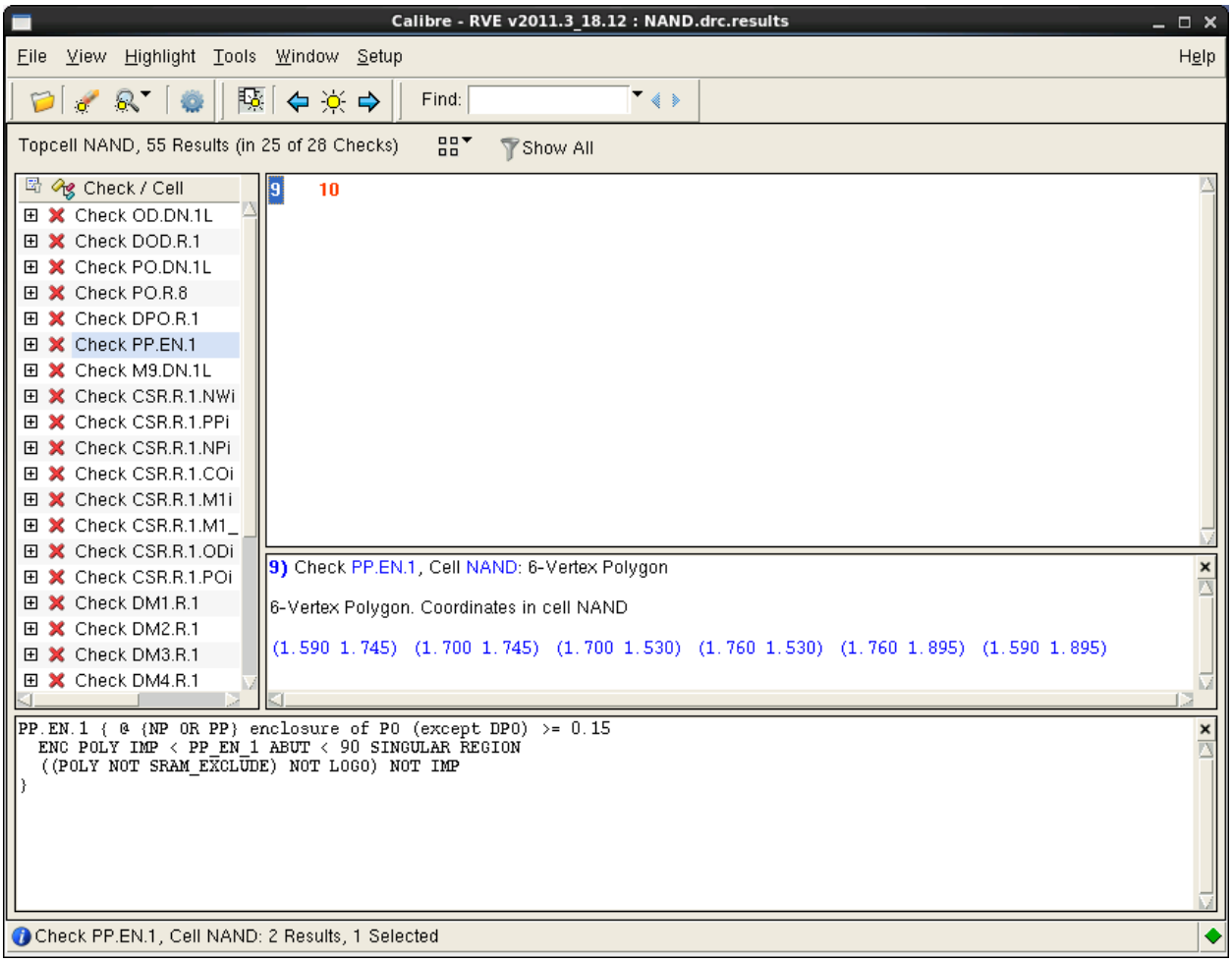


34. When the DRC is done, the Calibre RVE will popup, as well as a DRC Summery Report. In your lab report, include the end of the DRC support (everything after “--- RULECHECK RESULTS STATISTICS (BY CELL)”) from your **FINAL** DRC run.

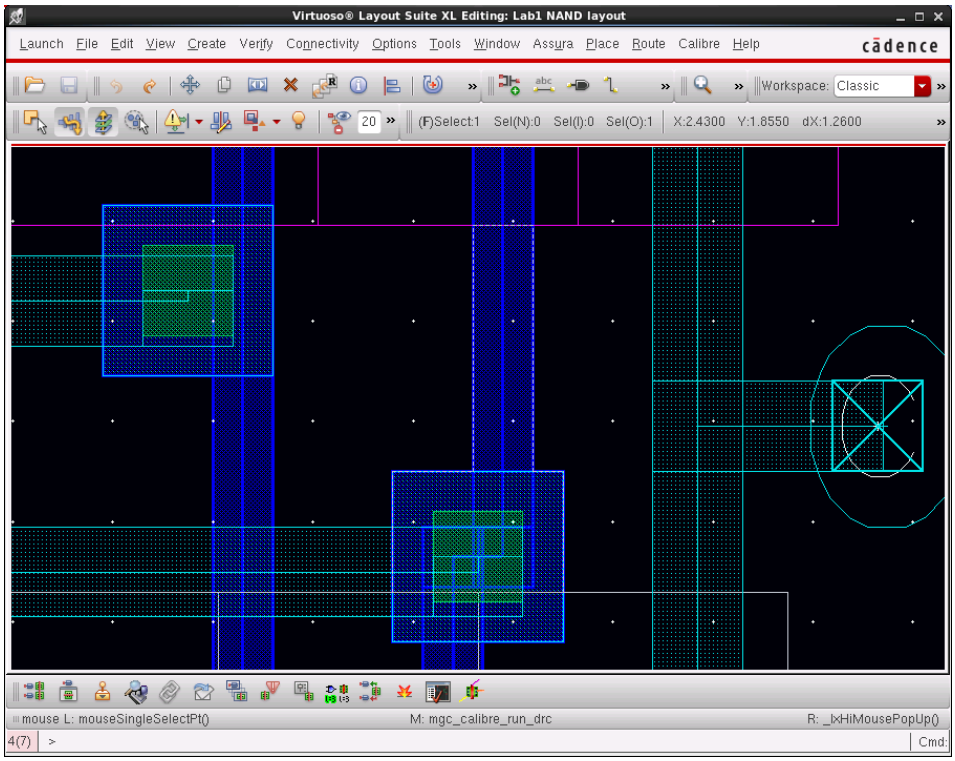


35. Since we are not making an entire chip, there are many errors that can be ignored. Ignore the following:
    - density errors (*.DN.* , i.e. OD.DN.1L)
    - Dummy layers (D*.*.* , i.e DOD.R.1)
    - Floating Gate Error (PO.R.8)
    - Layer is not allowed inside the empty area of chip corner (CRS.*.* , i.e. CSR.R.1.NWi)
    - Whole chip errors (ESD.EARN.1)

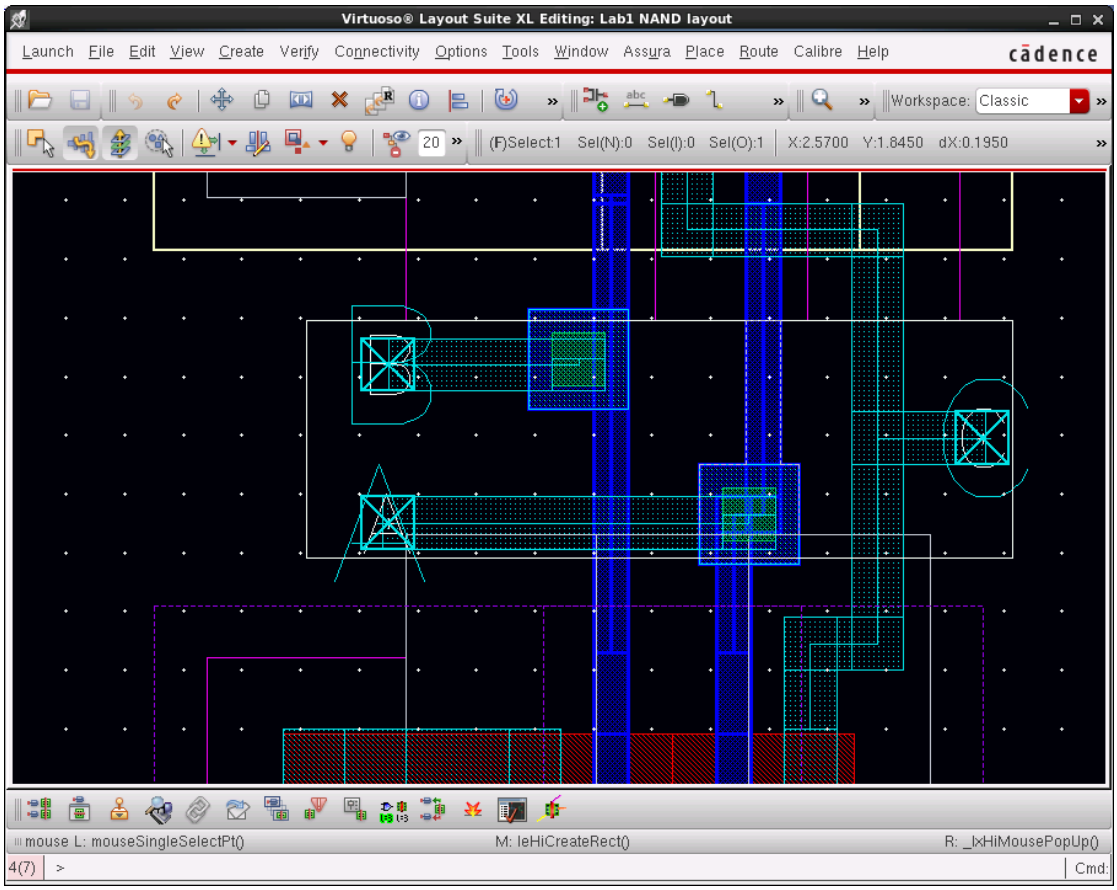
    Everything else is most likely an error. The descriptions can be cryptic sometimes, but usually with a little thought you can find the problem. Ask a TA if you are unsure.
36. For an example on how to solve a DRC error, lets looks at a common problem – PP.EN.1



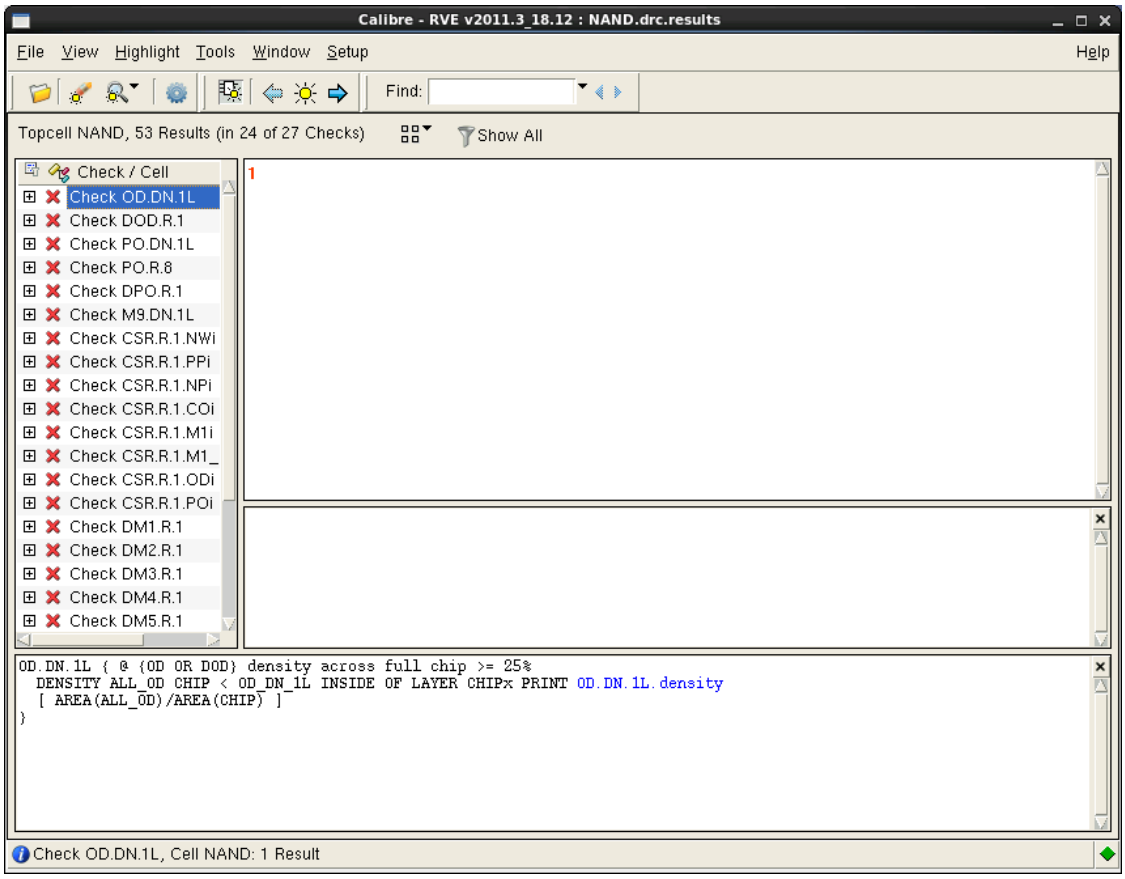
37. Double Clicking the error number (9 in the above image) will pan to the problem. (If you Select **Highlight -> Zoom to Highlights**, it will instead zoom the problem). In the image below, we can see the problem highlighted by white dashed lines. Alternatively, we can use the coordinated in the error explanation to find the error. In this case, the error is not very apparent, but the issue is that we need a n-substrate (PP) or p-substrate (NP) underneath the polysilicion (PO).



38. To fix this issue, draw a NP box under the PO layers (we are using NP since this is an N-Well process). Be careful not to overlap the PP and NP layers.



39. No when we rerun the DRC, we see the error is gone.

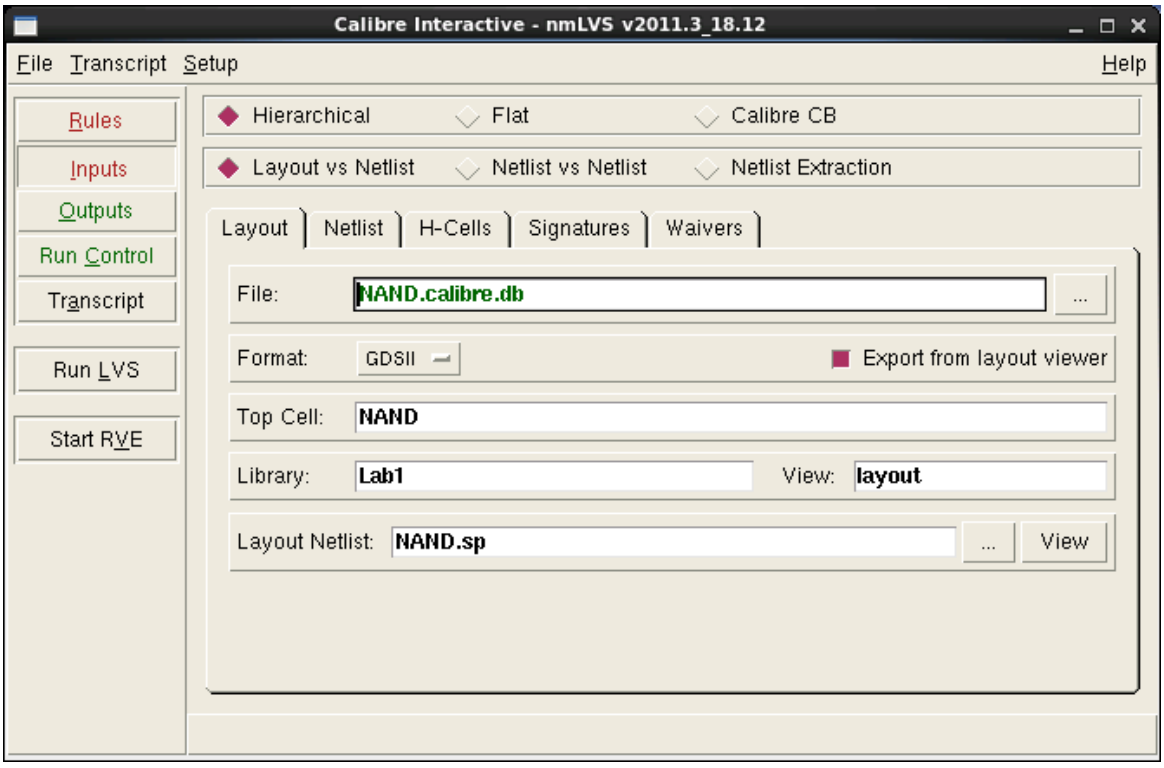


40. Not that we have fixed all the issues, we can Run LVS

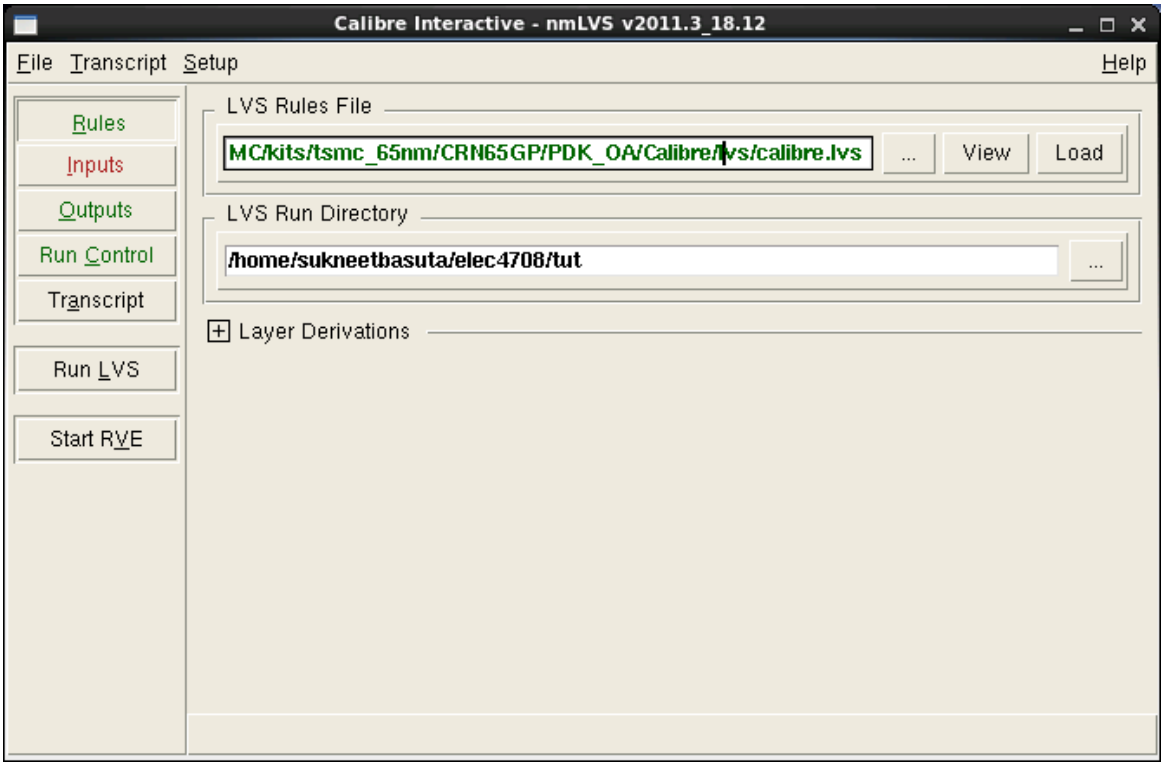
Layout-Vs-Schematic (LVS)

You can now run a LVS your circuit. The LVS compares your schematic to your layout and makes sure that you haven't made any inadvertent changes/errors.

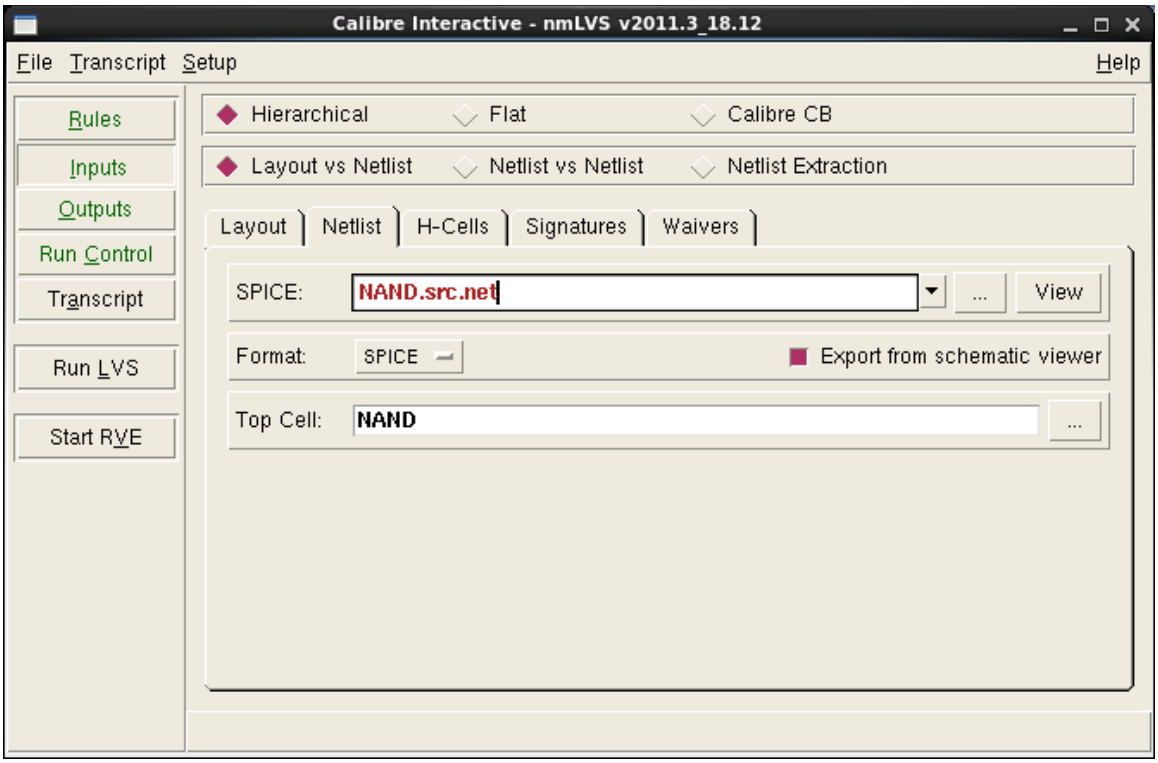
41. To open LVS, Select **Calibre -> Run LVS**
42. The Calibre Interactive – nmLVS window will popup.
43. If it asks for a runet, hit cancel.



44. Select the Rules Tab on the left and enter the following path for the Rules file /CMC/kits/tsmc_65nm/CRN65GP/PDK_OA/Calibre/lvs/calibre.lvs

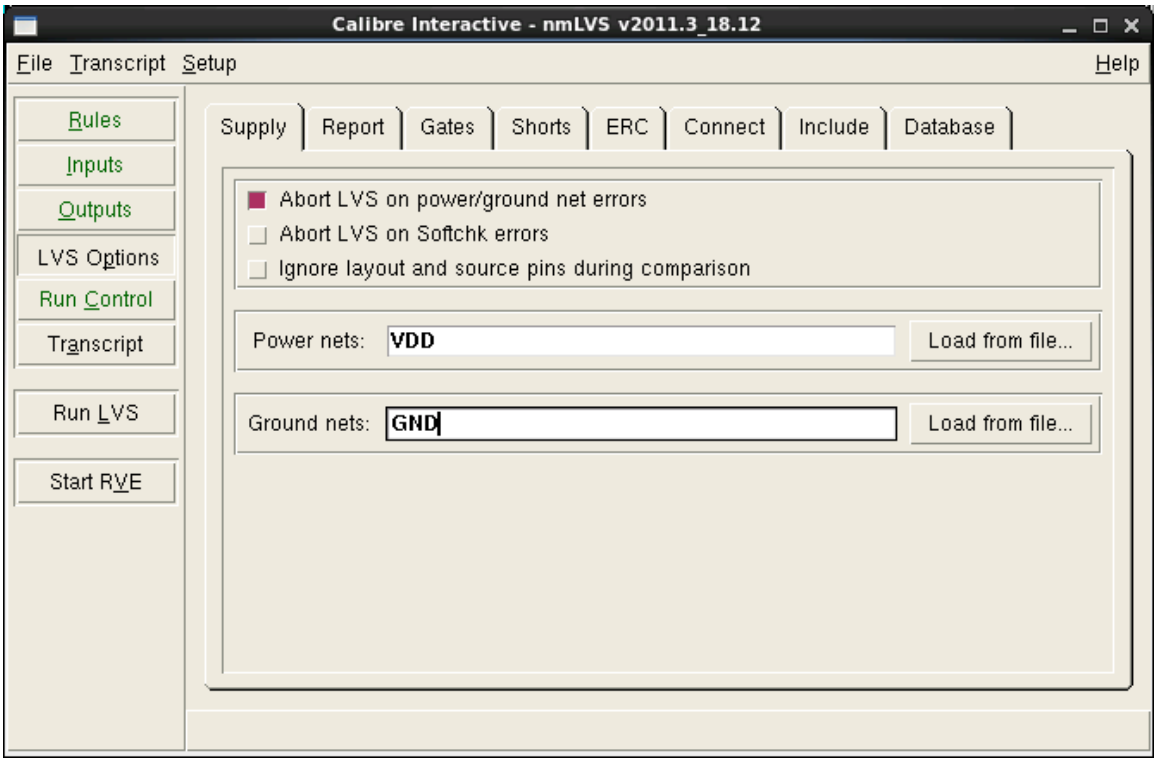


45. Select the Inputs button on the left. Then Select the Netlist tab in the middle. Check the “Export from schematic viewer” option



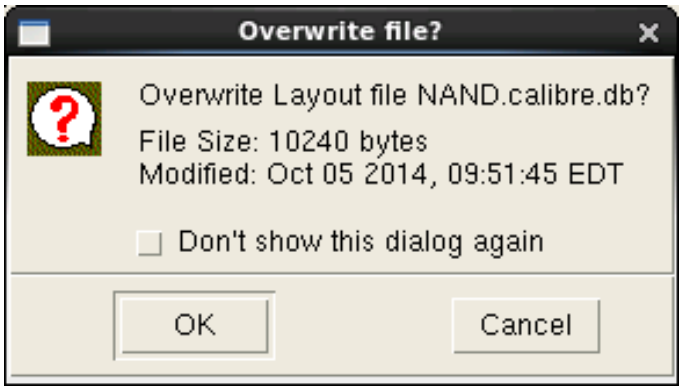
46. Select **Setup->LVS Options** in the menubar.

    Hit the LVS Options button that just appeared on the left. In the Supply Tab, enter the Pin name you used for VDD in Power nets, and the Pin name you used for GND in Ground nets. This tells Calibre the supply and ground nets.

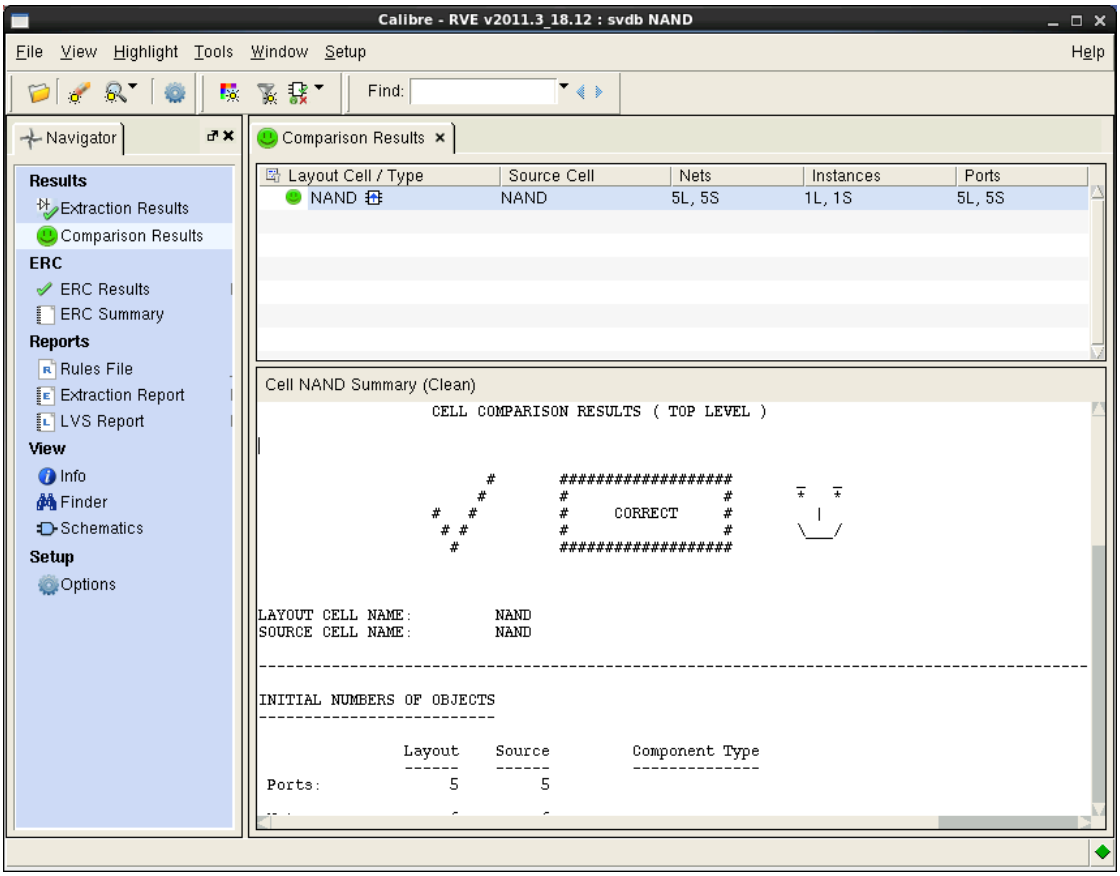


47. Now that LVS is setup. Hit Run LVS on the left.

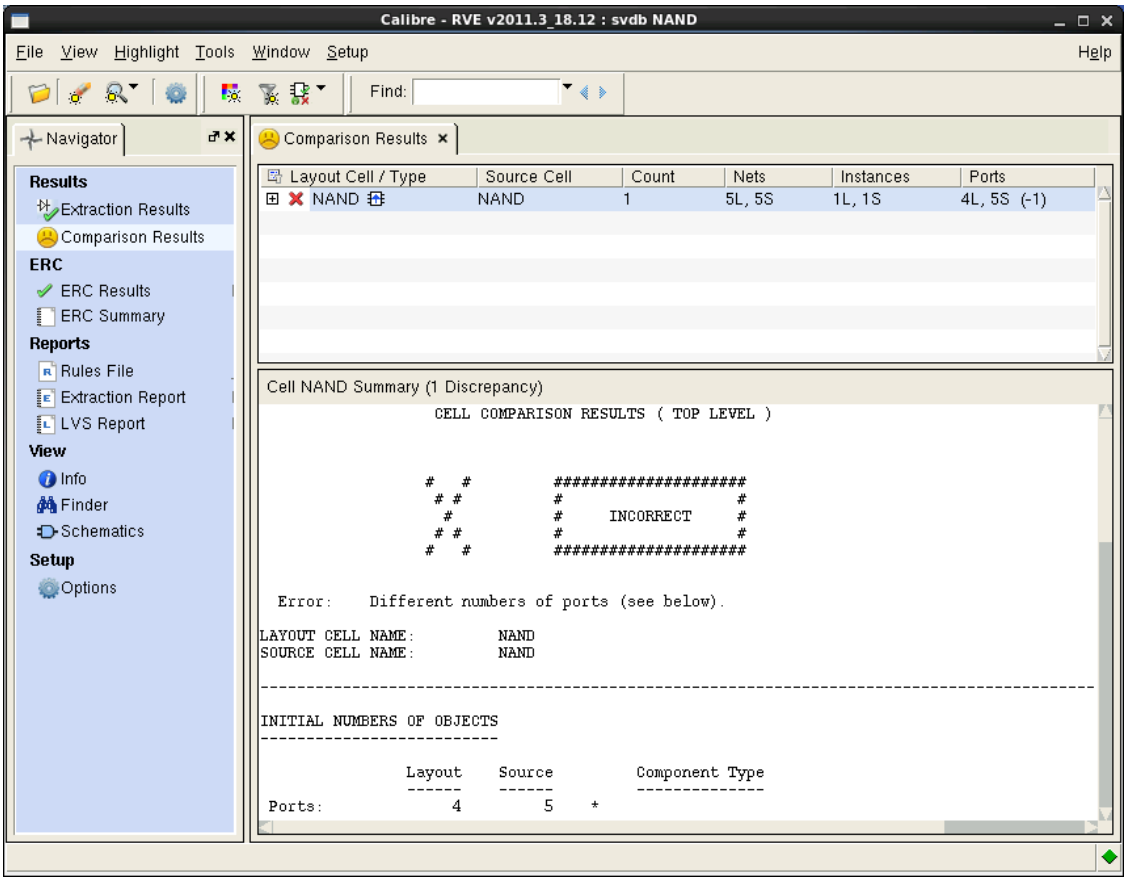
48. If you get the following error, Check “Don’t Show this dialog again”, and hit OK.



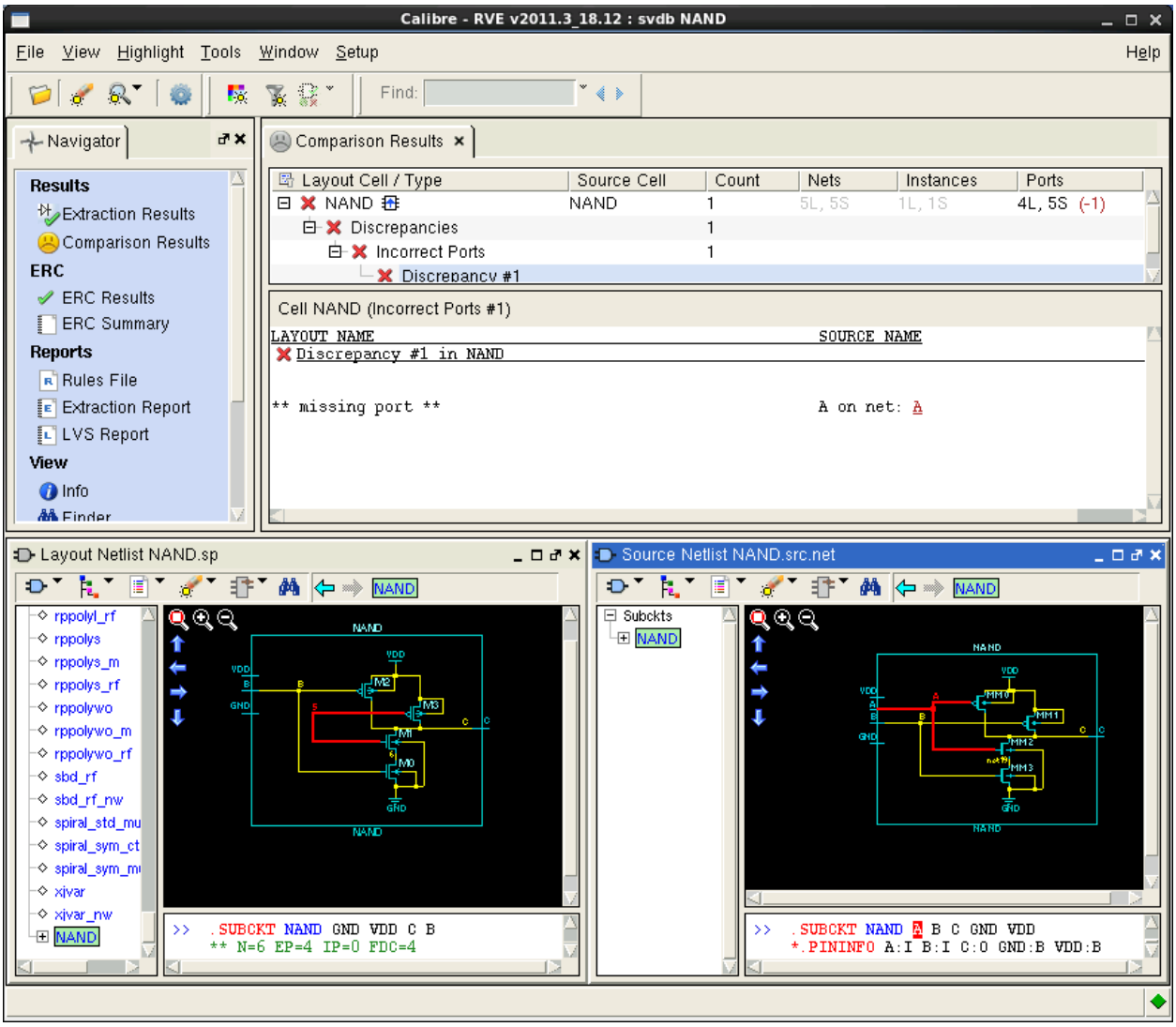
49. When the LVS run is complete, the Calibre – RVE window will appear, as well as a LVS Report file. If everything is fine, you will see a Check Mark and a Happy Face like in the window below. Include the Cell NAND Summary in your Lab report.



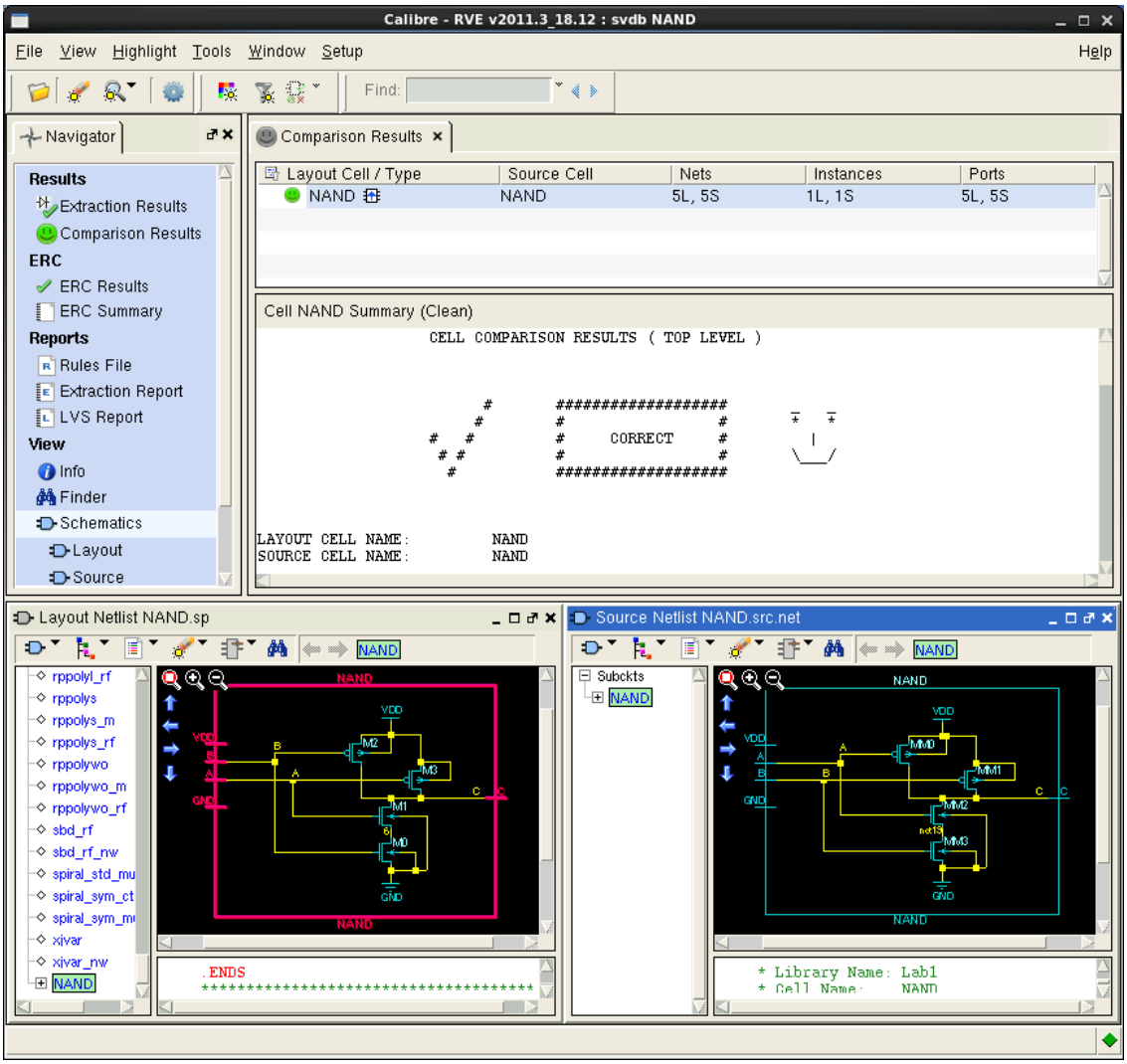
50. If the LVS failed, you will see a window like



51. We can see the problem by clicking the + next to error. When you click on the expanded error, an explanation of the error will appear where the summary was. Clicking on any Red links in this area (i.e. A in the image below) will show you the schematic the LVS run got from the layout on the left and the schematic you designed the right.
    In the image below it is clear that the pin for input A is missing.



52. You can verify your layout is good on a good run, by clicking “schematic” in the left navigator.

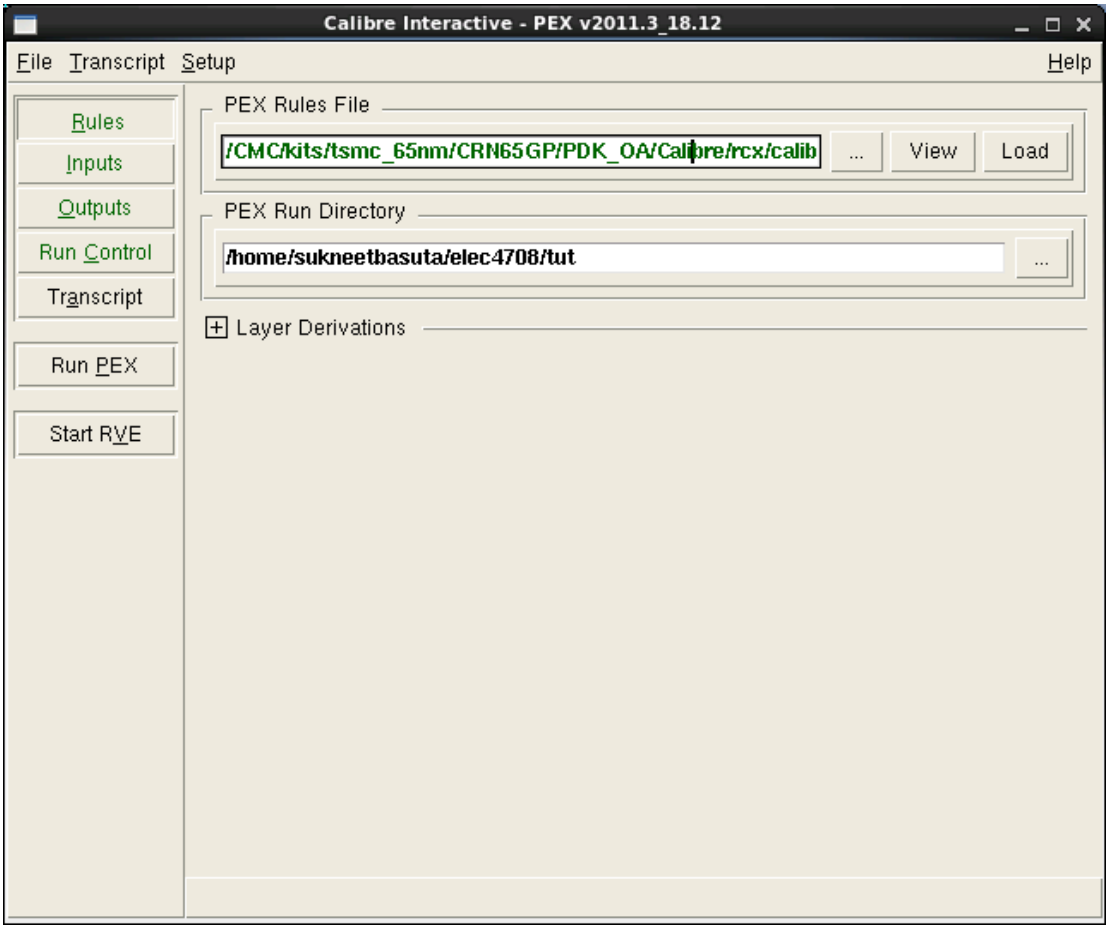


Parasitic Extraction (PEX)

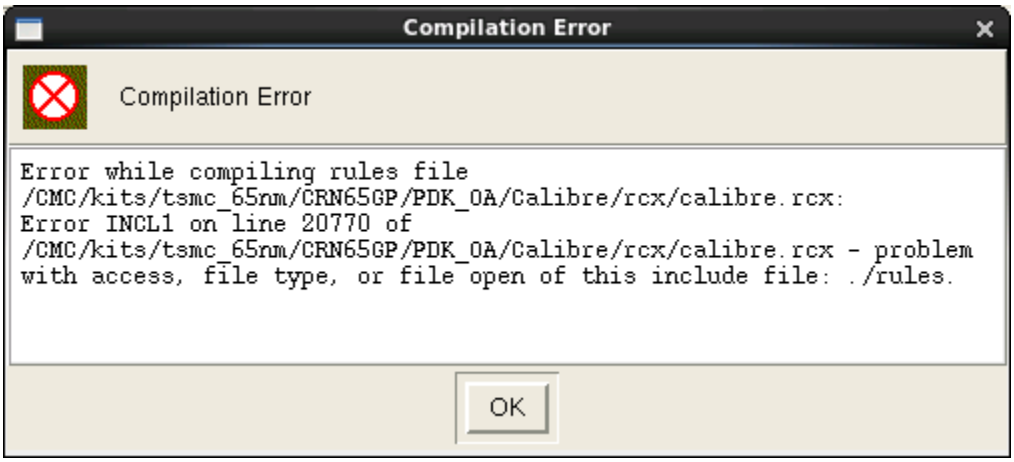
The extracted view is a version of your layout that can be used in simulation, probed for connectivity and compared to your schematic using an LVS tool. You can also add parasitic capacitance and resistance to the extracted view. Parasitics are the undesired (can often be used as part of the design) resistance, capacitance and inductance of your circuit. A good designer takes the parasitics into account when designing the circuit.

53. Before running PEX we need to copy a file to directory we created in Part A. (i.e. ~/Desktop/elec4708/lab1)
    In a terminal run (Change the last path to the directory you created):
    `cp /CMC/kits/tsmc_65nm/CRN65GP/PDK_OA/Calibre/rcx/rules ~/Desktop/elec4708/lab1`
    Or change directories into the folder (cd elec4708, etc) and run:
    `cp /CMC/kits/tsmc_65nm/CRN65GP/PDK_OA/Calibre/rcx/rules .`
54. Select **Calibre->Run PEX**
55. If it asks for a runset, hit cancel.

56. Select the Rules button on the left, and enter the following path for the rules file /CMC/kits/tsmc_65nm/CRN65GP/PDK_OA/Calibre/rcx/calibre.rcx

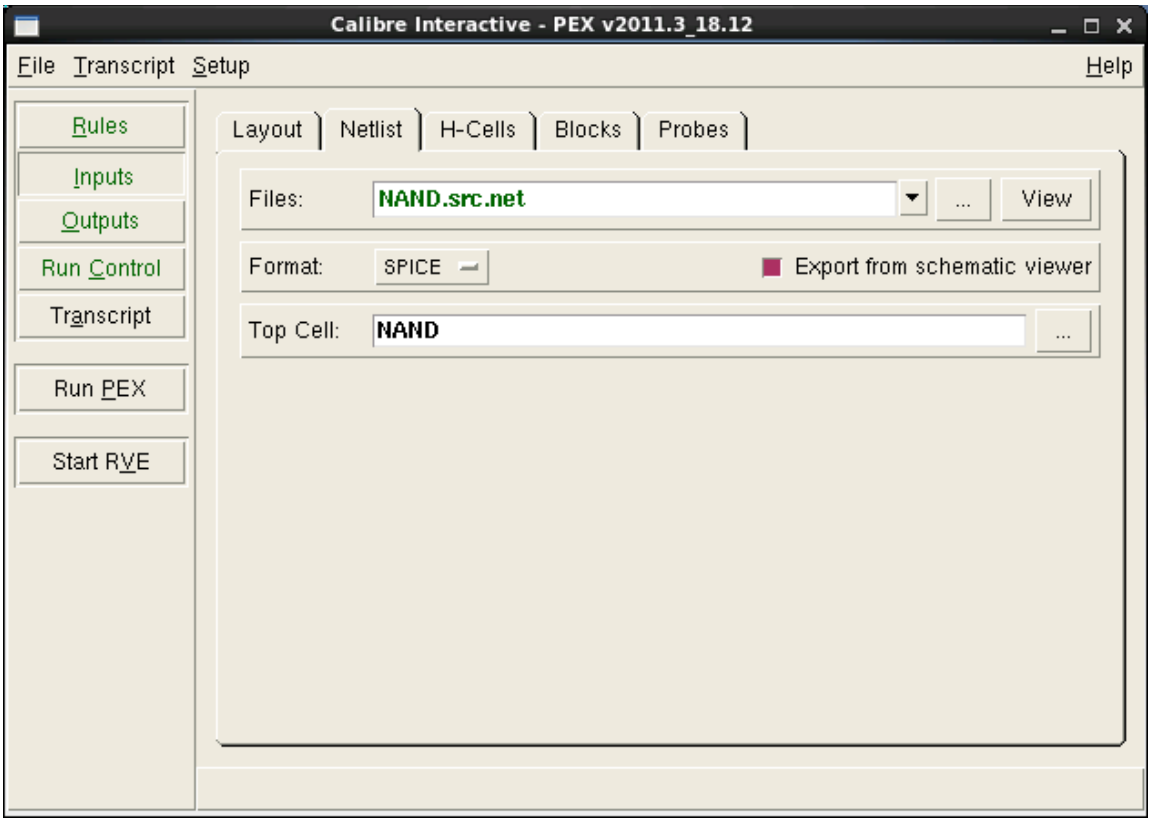


If you get the following error:

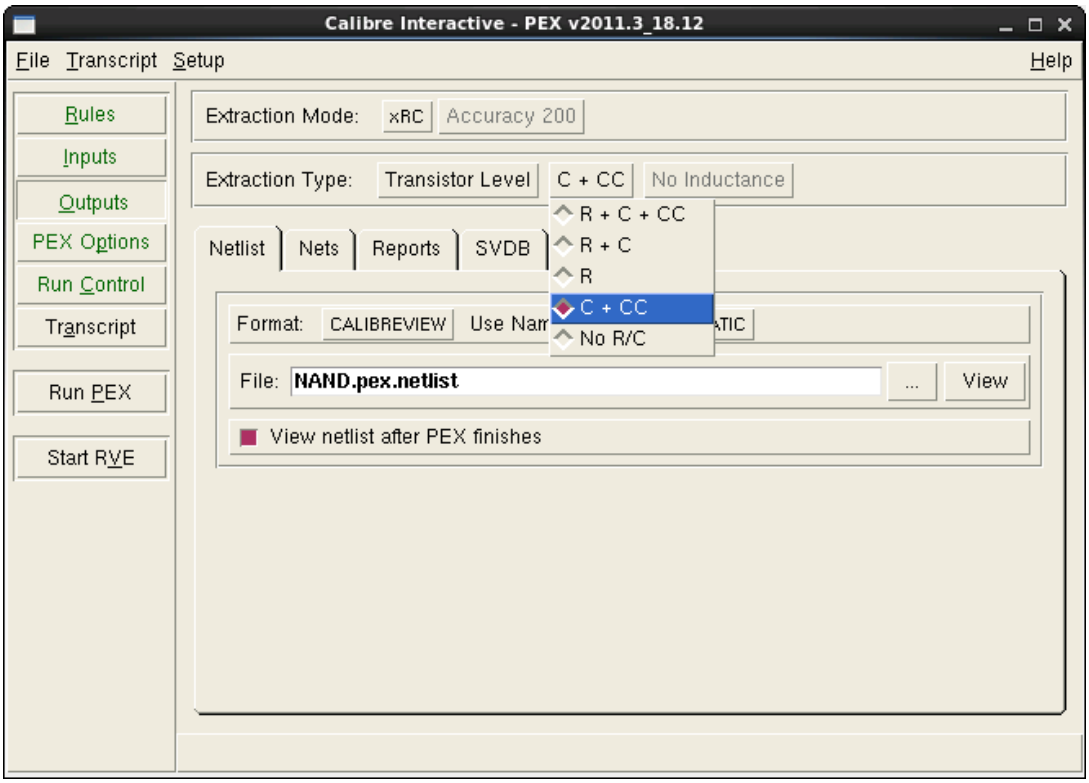


Redo Step 51, you most likely didn't copy the file to the correct path.

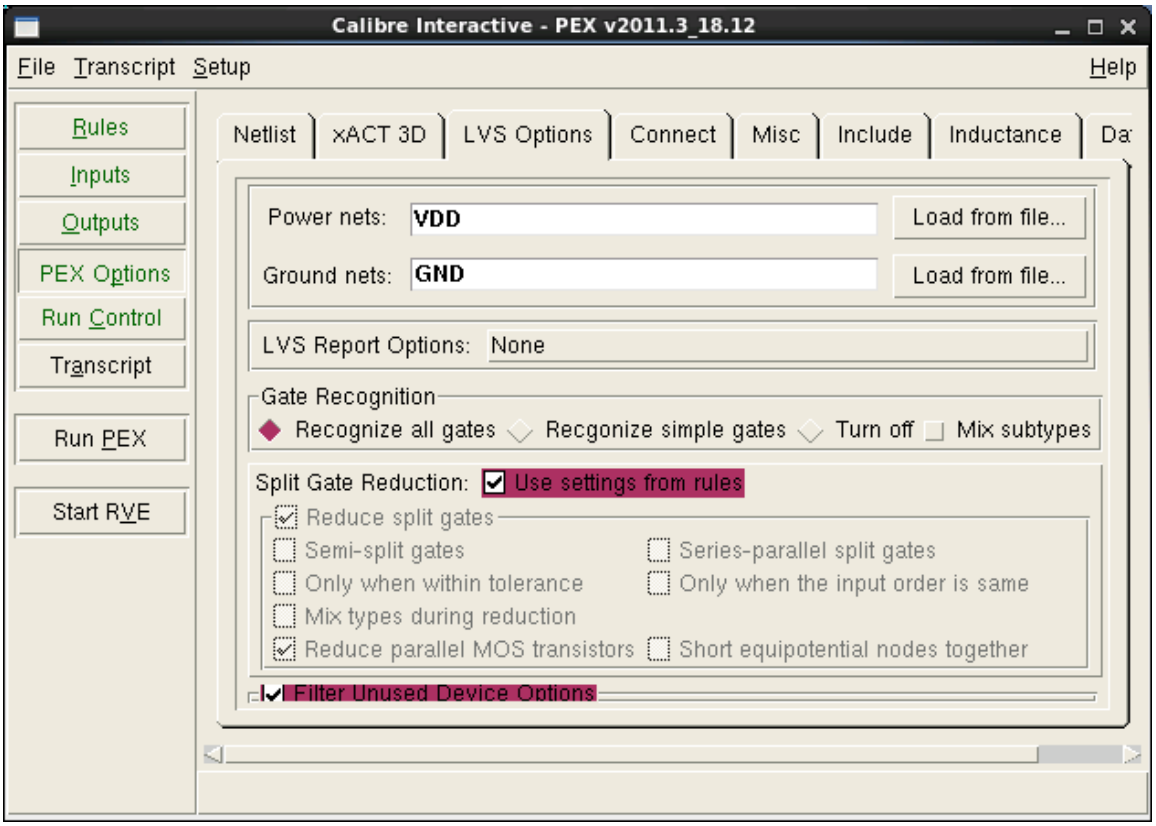
57. Select the Inputs button on the left, select the Netlist tab, and check "Export from schematic viewer"



58. Since, we only want parasitic capacitances, click on the Outputs button on the left, and change the extraction type to C+CC. Also change the Netlist Format to CALIBREVIEW.

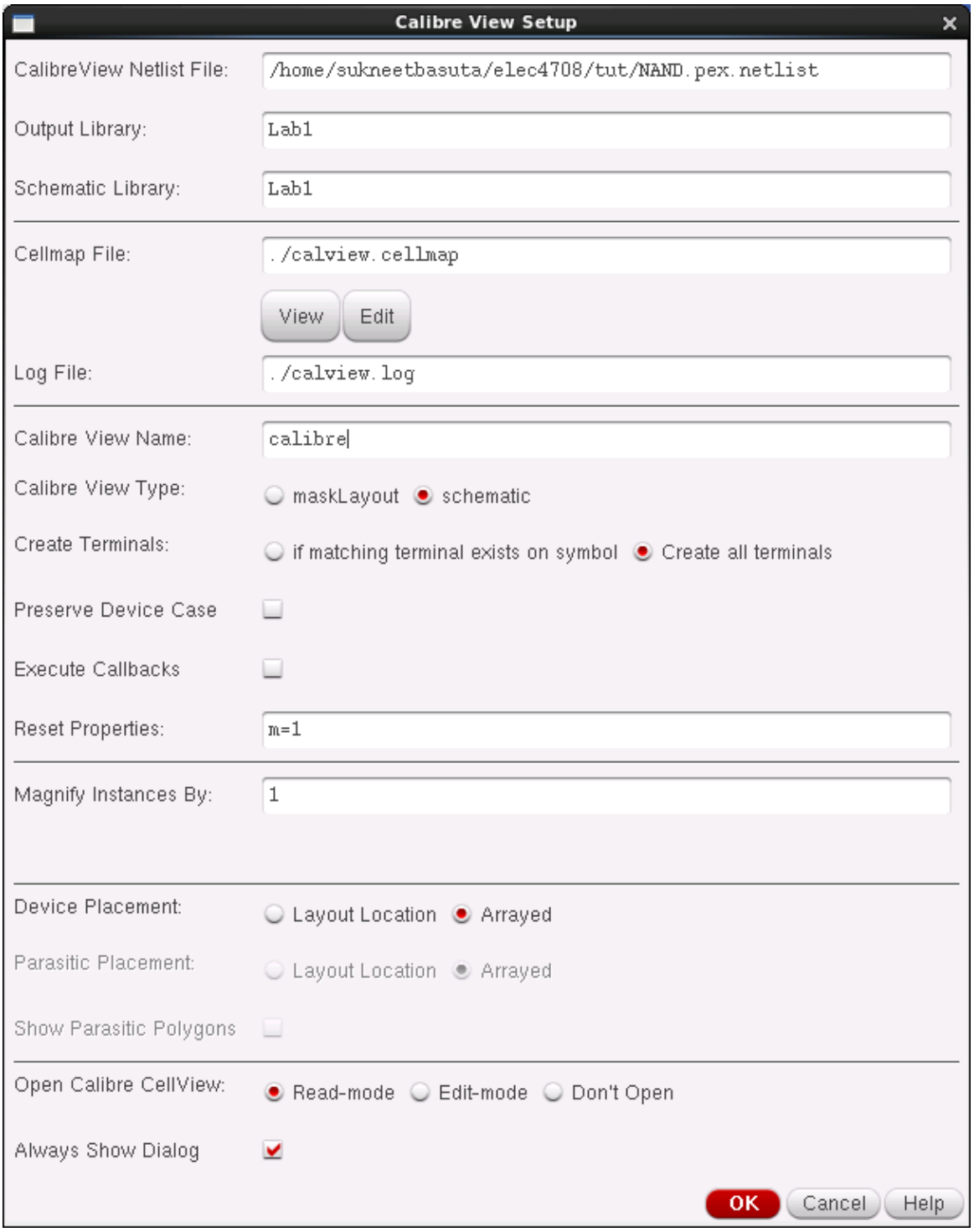


59. Select Setup -> PEX Options. The PEX Options button should appear on the left. Click it. Select the LVS Options tab, and set the Power nets (VDD) and Ground nets (GND). These should be the same as the ones you set in the LVS step.

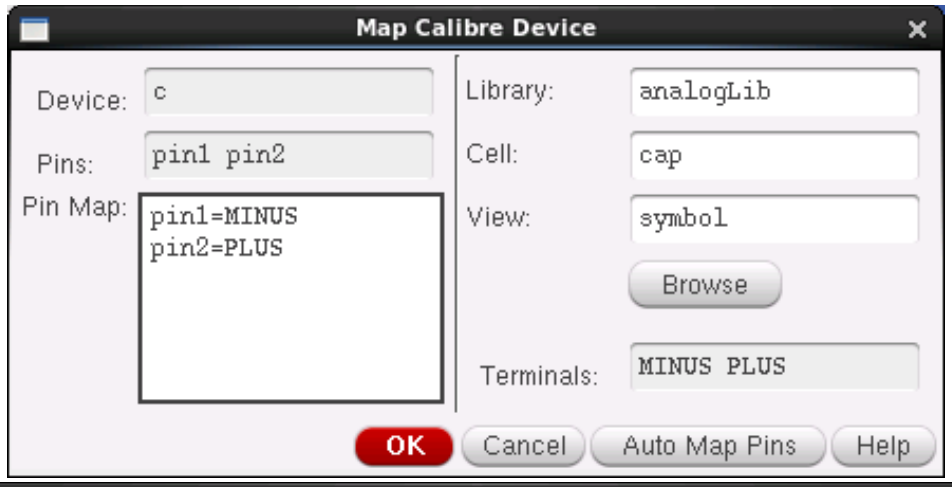


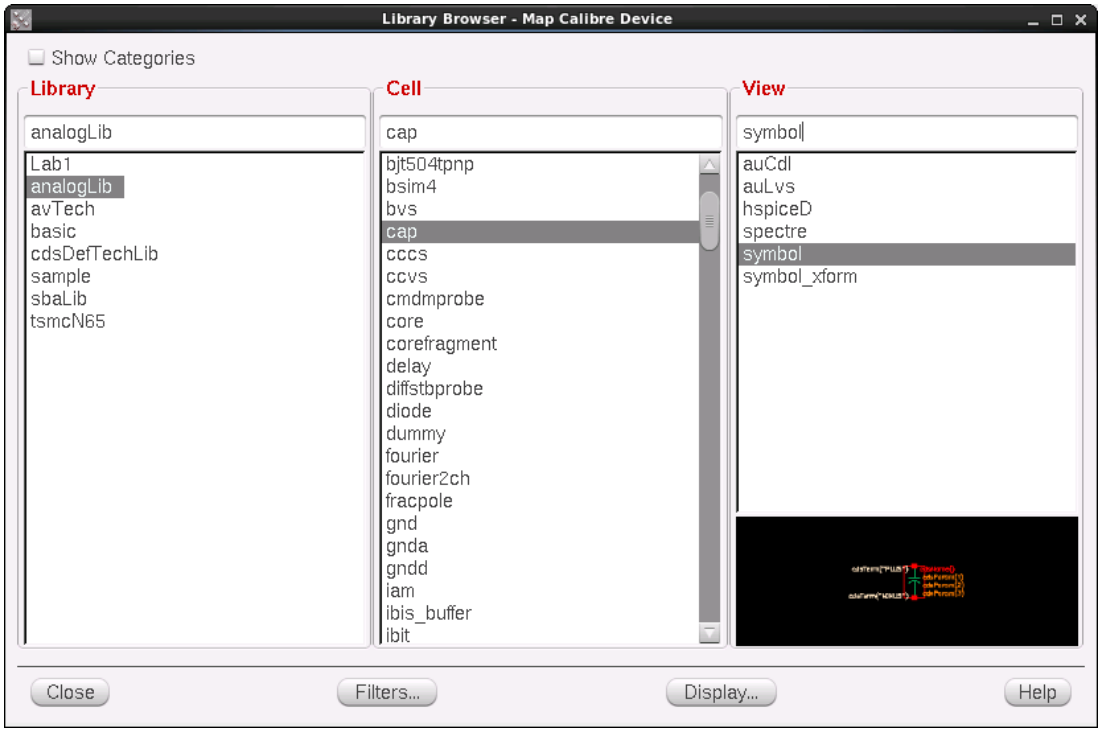
60. Now that everything is setup, let's run the extraction. Click Run PEX.
61. When the extraction is done, the Calibre View Setup window will popup, as well as the PEX Netlist File. Include the text in the PEX Netlist File in your report (we only really care about everything under 'mgc_rve_cell_start "NAND" "GND" "VDD" "C" "B" "A" ').

    Change the View type to Schematic, Select Create all Terminals, change the device placement to Arrayed, and Open the Calibre CellView in Read-Mode or Edit-Mode.

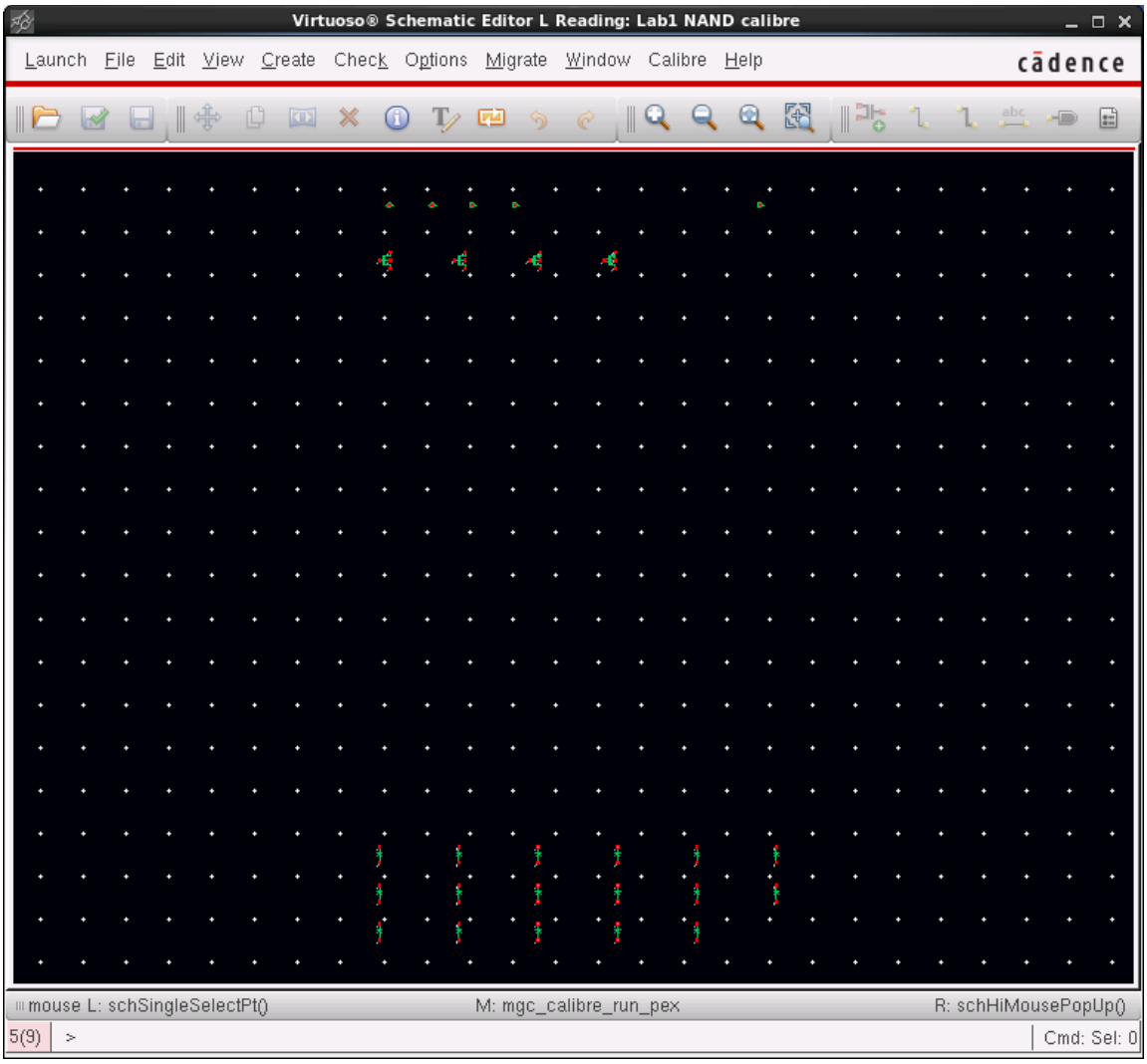


62. Hit OK.
63. A new window should popup asking you to map the Capacitance (c) device. We will use the ideal capacitor supplied in the analogLib Library since we are only concerned with the capacitances. Type “analogLib” in the Library, “cap” in Cell, and “symbol” in view”. Then hit Auto Map Pins. Hit Ok.

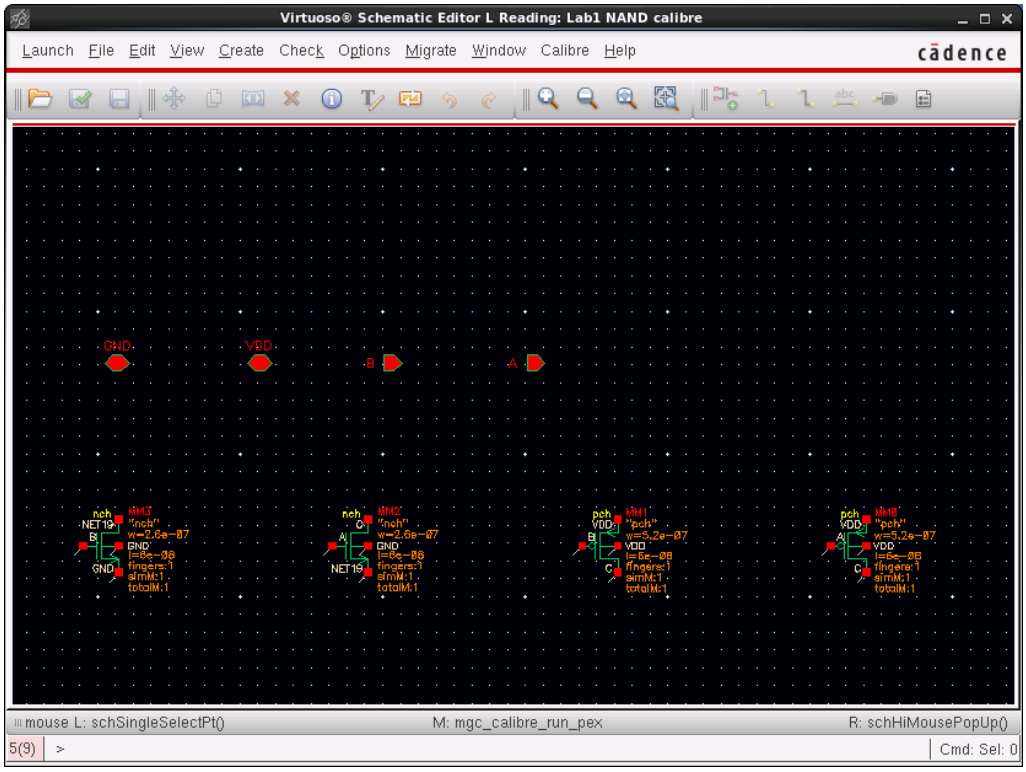




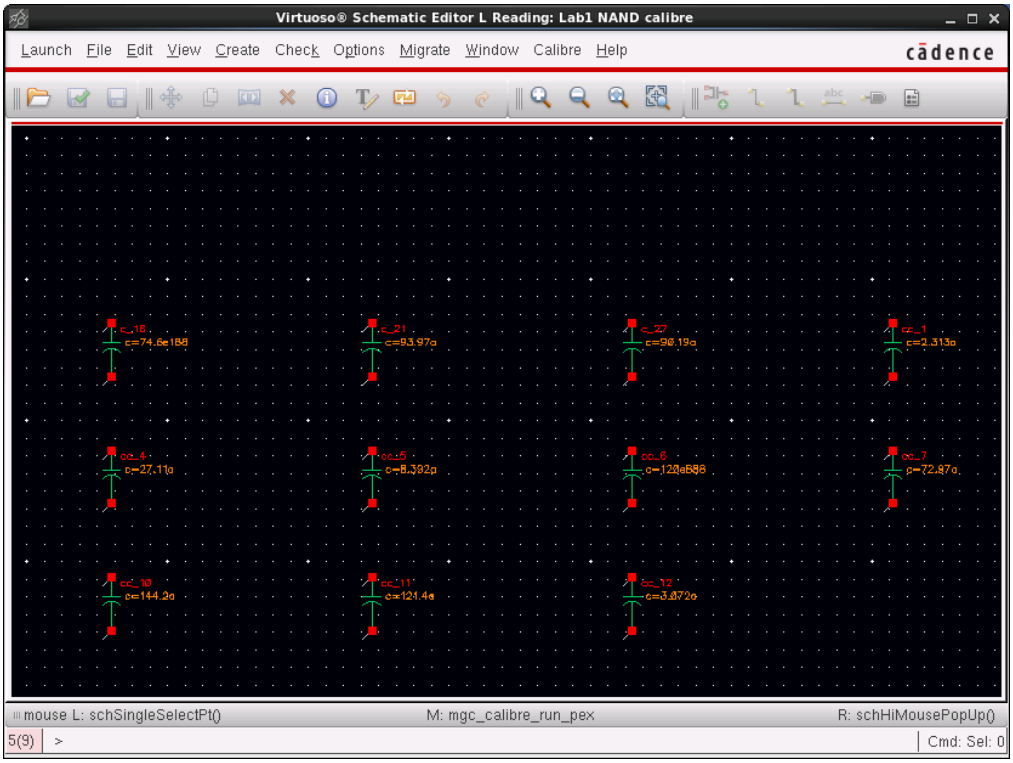
64. If everything went fine, you will receive a message like the one below and Virtuoso Schematic Editor will popup with your extracted circuit.



65. The schematic will look odd to you since we told Calibre to array the devices (not doing so can cause devices to overlap) and because the devices are connected by short wires and label names. If you take a closer look, you will see the 4 transistors in your NAND gate and the input pins.



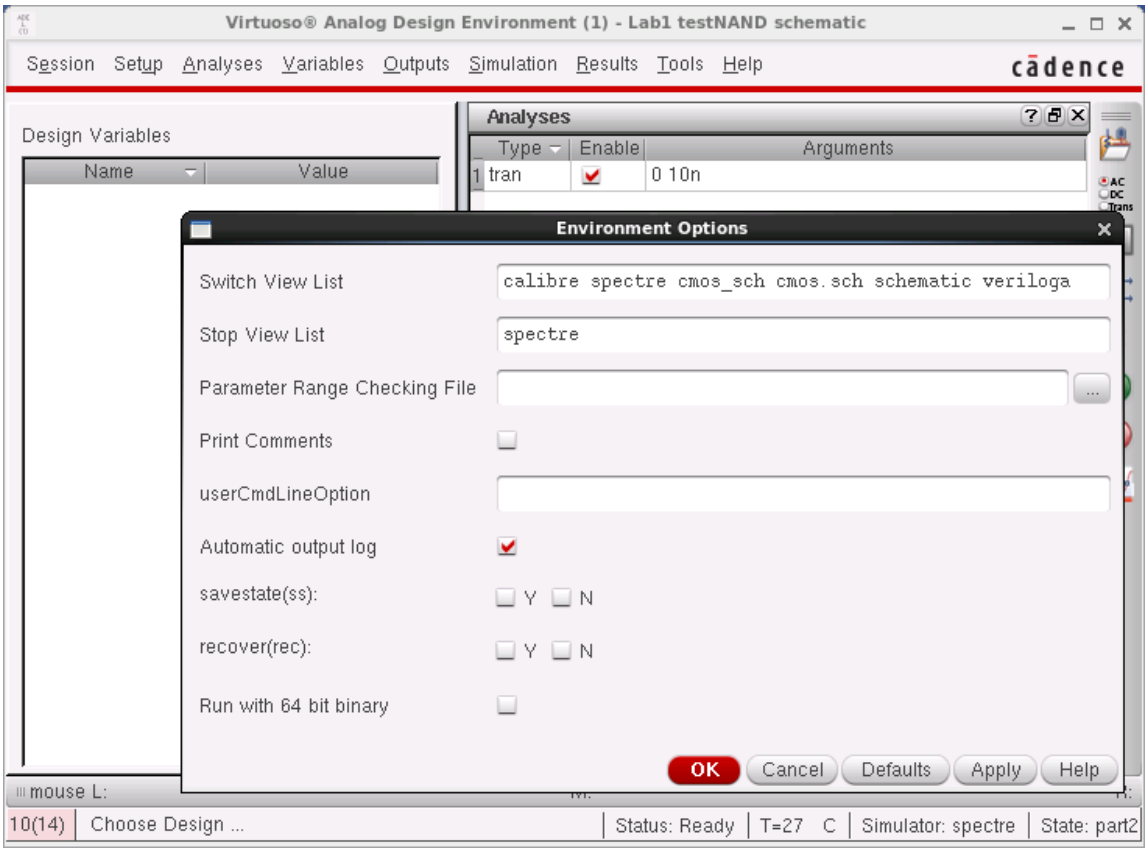
Below that, you will see all the extracted parasitic capacitances.



66. When you go into the library manager and select your NAND cell, you should now see a “calibre” view, along with layout, schematic, and symbol.

Simulation:

67. Now that we have the extracted schematic, how do we run simulations using it?
    Open up the testbench that you used in Part A (testNAND in the previous tutorial).
68. Open the Analog Design Environment (ADE L)
69. If you saved the states in the previous lab, load up the state you wish to use (Session -> Load State).
70. Select **Setup->Environment**. The Environment Options window will popup.



71. Add “calibre” to the front of the Switch View List. Hit Ok and rerun your simulations.