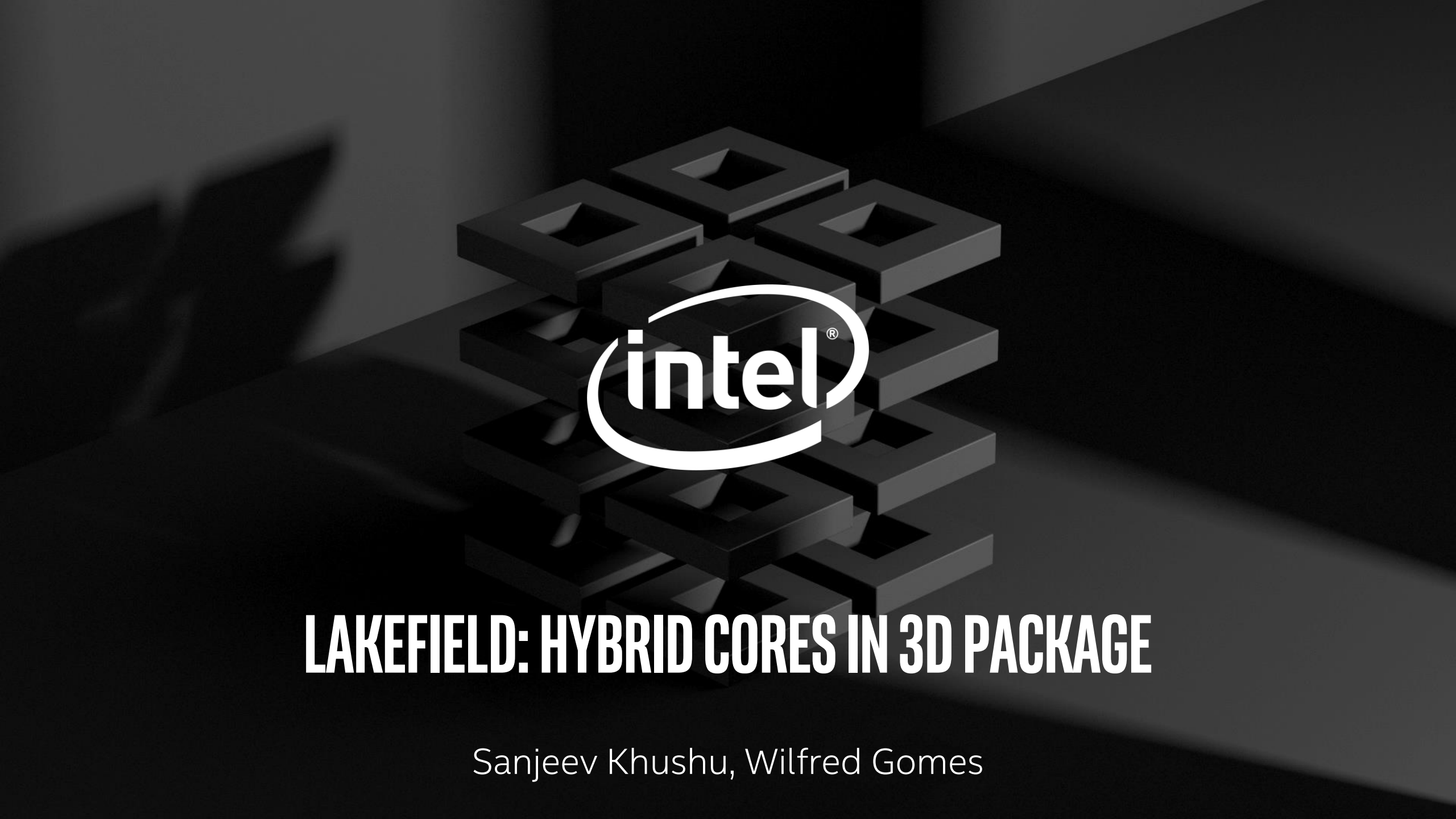



# LAKEFIELD: HYBRID CORES IN 3D PACKAGE

Sanjeev Khushu, Wilfred Gomes

# LAKEFIELD: DESIGN GOALS

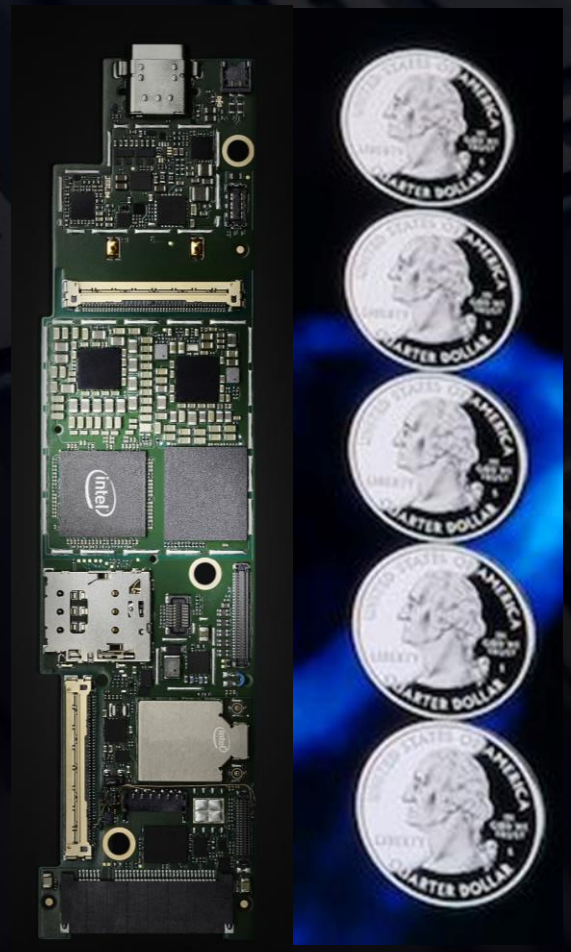
- High level goal:
  - Enable new class of compute devices in Mobility form factor (converged Mobility)
  - Best in class Compute performance in lower TDP
  - Always on, always connected, very low standby Power

- What this meant to Compute SOC
  - Migrate to latest Process technology/ Intel 10nm
  - Significant Gen over Gen improvements:
    - ~1/10th Standby Power
    - ~50% GFX improvement
    - ~40% Core area reduction
    - ~40% Z reduction

- How do you achieve this in 1 Generation?
  - Birth of Lakefield!

# LAKEFIELD BIG PICTURE: SMALL FORM FACTOR DEVICES

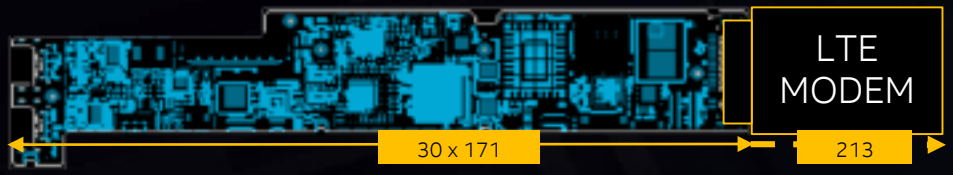




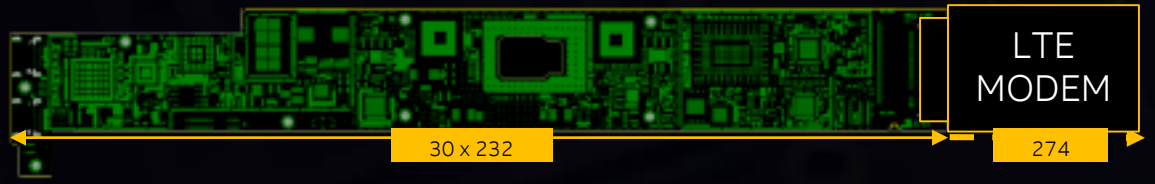
# LAKEFIELD VS PREV GEN VS COMP

### LKF DUAL DISPLAY AEP

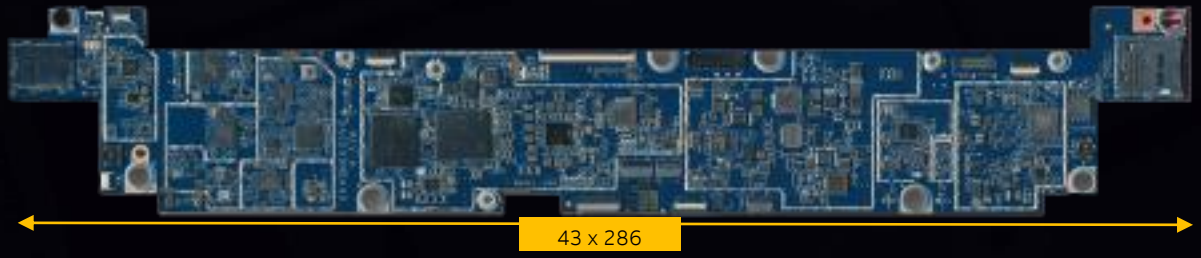

### LKF CLAMSHELL AEP




### GEN-1 AEP

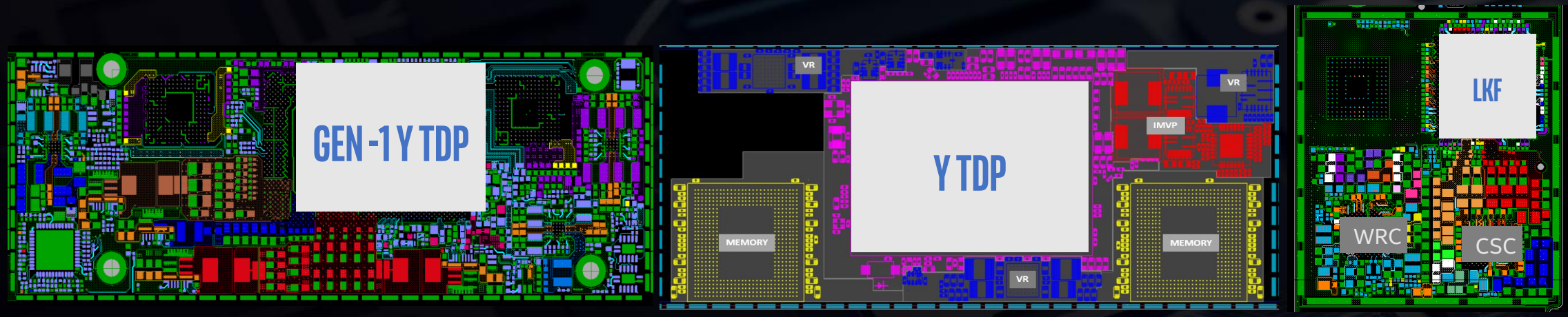



### COMP MOTHERBOARD




| KEY ENABLING VECTORS | |
|---|---|
| **SoC** | • Hybrid CPU architecture |
| **Package** | • 3D Foveros packaging |
| **PCB** | • Compact 30x123mm LKF motherboard design<br>• 0.6mm, 10L, ALV, complete single sided |
| **EC** | • EC-lite architecture |
| **Boot** | • SPI-less boot from UFS |
| **Form factors** | • Dual/foldable displays; thin clamshells |

# CORE AREA ATTRIBUTES




| | Y SKU Gen-1 | Y SKU | LKF |
|---|---|---|---|
| | **mm2** | **mm2** | **mm2** |
| **Core** | 1x | 0.9x | 0.4x |
| **Package** | 20.5x16.5 | 26.5x18.5 | 12x12 |
| **Memory** | LP3 11x11.5 | LP4-4x 12.5x12.5 | LP4-4x POP |
| **Power Delivery** | Discrete VR | FIVR/<br>Discrete VR | PMIC |

# LAKEFIELD ARCH: HYBRID CORES + 3D DIE STACKING

Latest Display core 4 pipes, 5k60 or 4k120

New Hybrid IA cores
1x SNC + 4x TNT

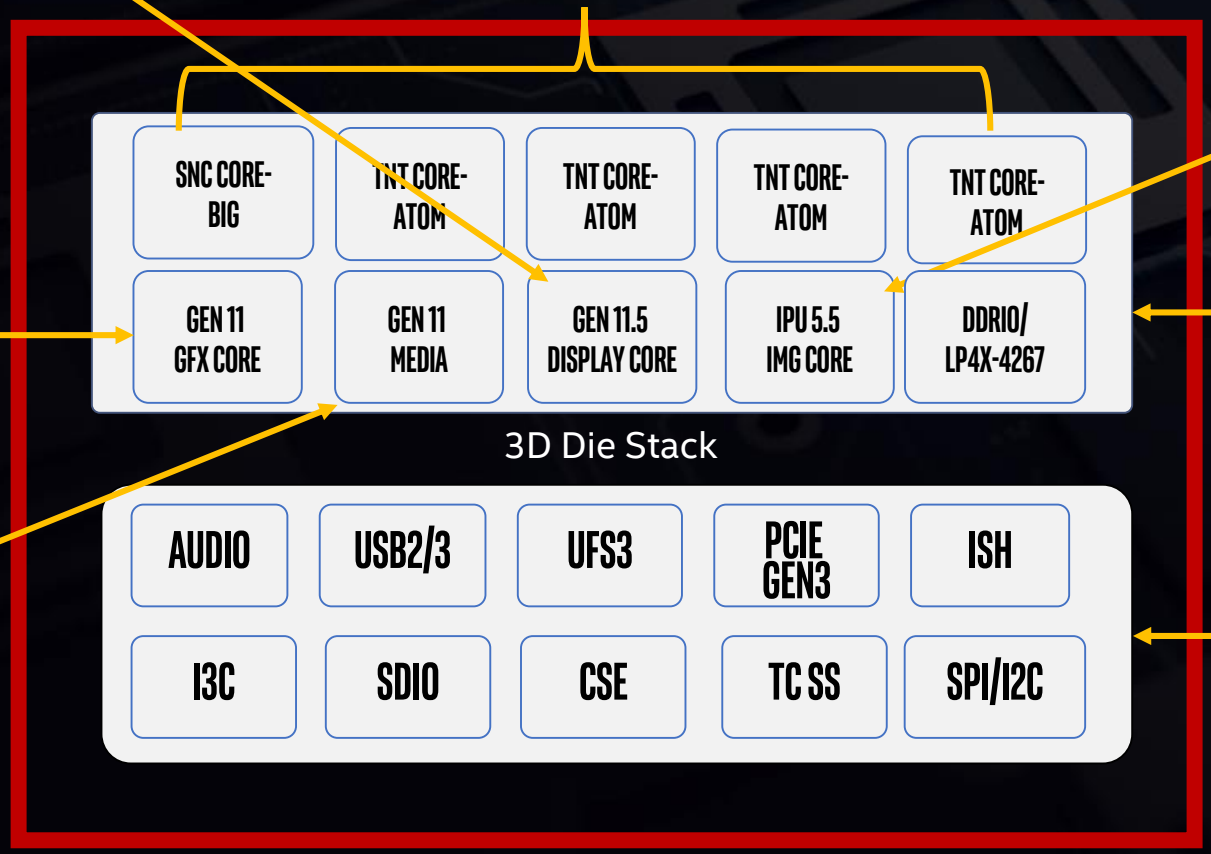
Latest IPU5.5, up to 16MP, x6 connected cameras

Latest GFX core Gen 11 64EUs

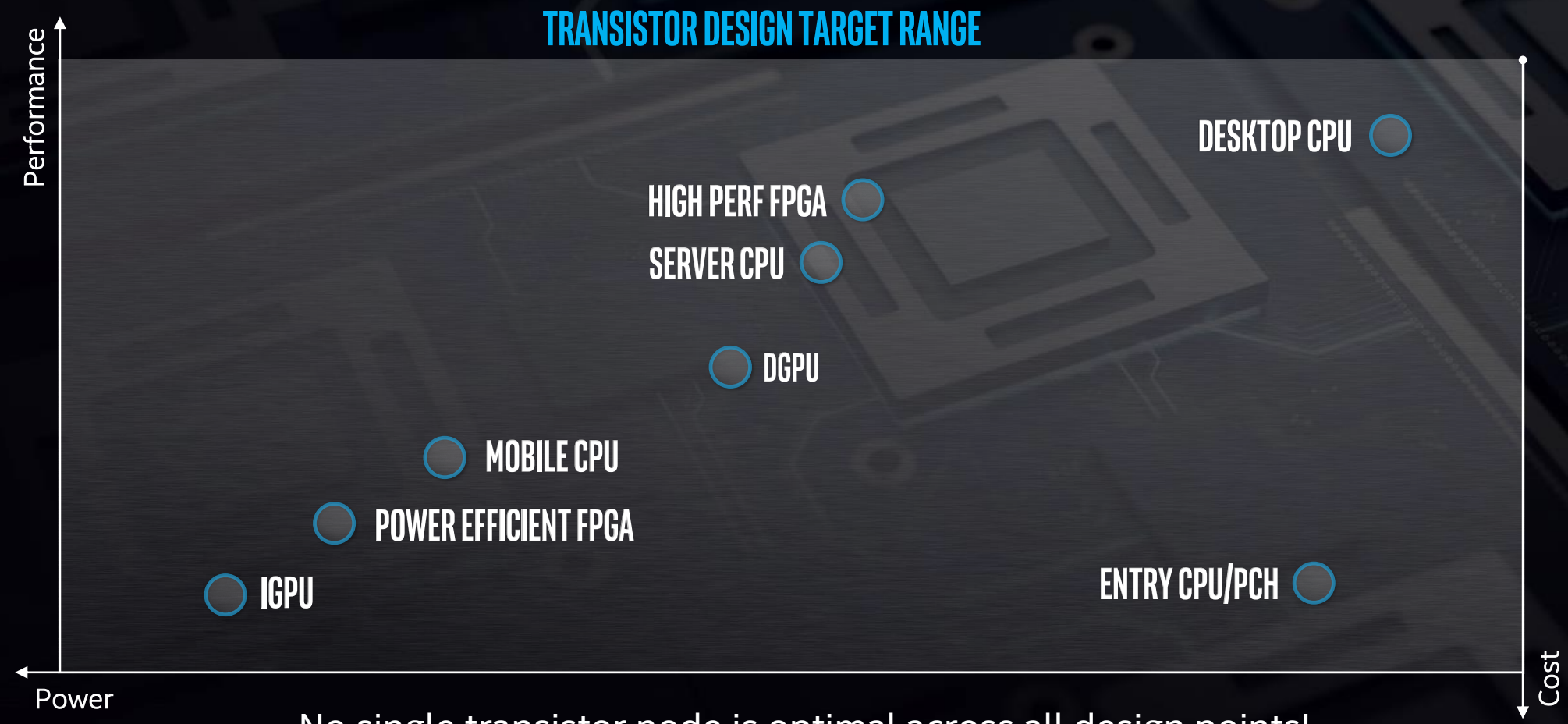
Compute die: 10nm

Latest Media core 4k60/ 8k30

Base die: P1222



# CASE FOR ADVANCED PACKAGING




No single transistor node is optimal across all design points!

# INTEL PROCESS DEVELOPMENT MODEL W/ FOVEROS

## LAKEFIELD IMPLEMENTATION

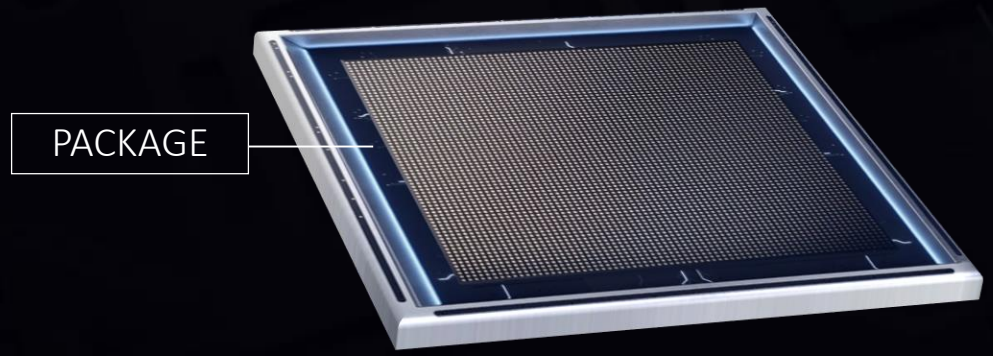
| | Manufacturing | Development | Path finding |
|---|---|---|---|
| Optimized for Compute | 1274(10nm) | 1276(7nm) | 1278 |
| "FOVEROS" | P1222 | 1274.FV | 1276.FV |

Optimized X/Y, board area
Mix and Match of IP and process nodes.
Highest Performance & Lowest Leakage
Allows IPs to be developed independently, faster time to market

Ultra-Mobile form factor (12x12x1 mm package)
~2.x mW Standby Battery Life
Leadership CPU Performance

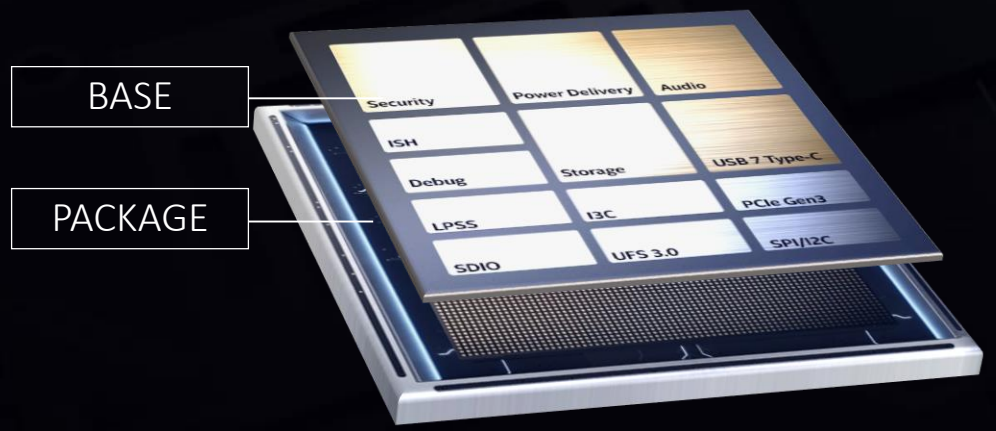
# LAKEFIELD FOVEROS

PC IN MOBILE FORM FACTOR – 12X12



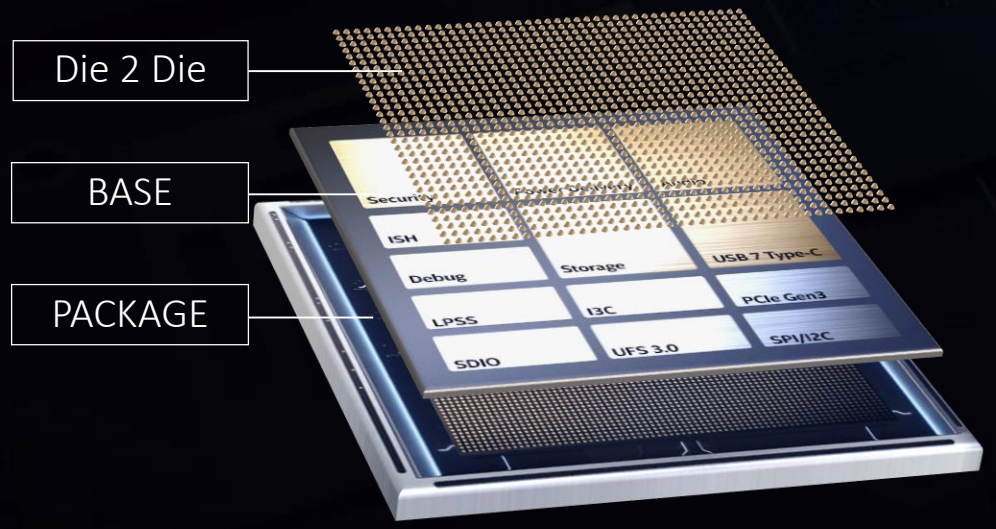
# LAKEFIELD FOVEROS

CHIPSET, POWER DELIVERY, LOW POWER LOGIC - P1222 BASE



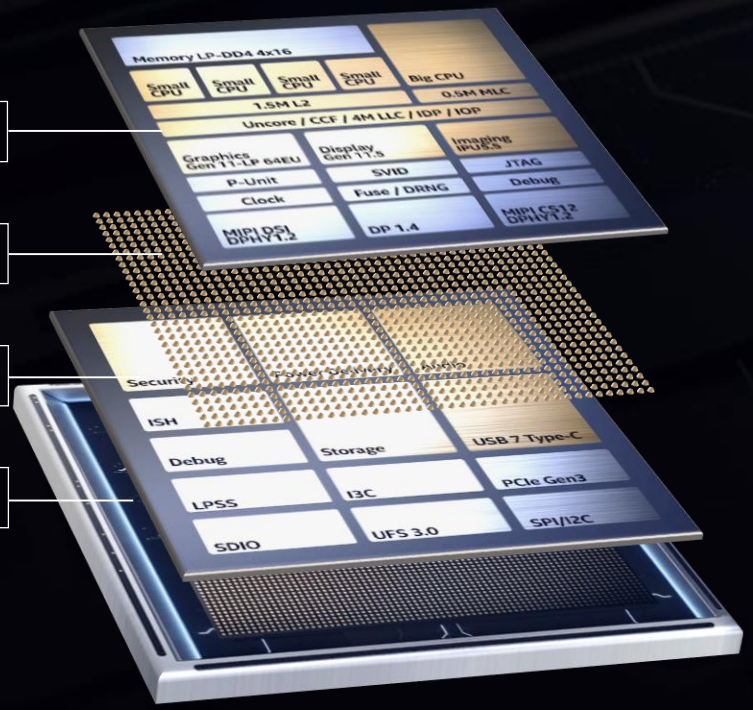
# LAKEFIELD FOVEROS

HIGH BANDWIDTH , ULTRA LOW POWER CONNECTIVITY BETWEEN DIES
SCALABLE TSV FOR POWER DELIVERY
HIGH YIELDING PROCESS FOR DIE 2 WAFER ATTACH, THERMAL SOLUTION TO ENABLE 3D STACKING



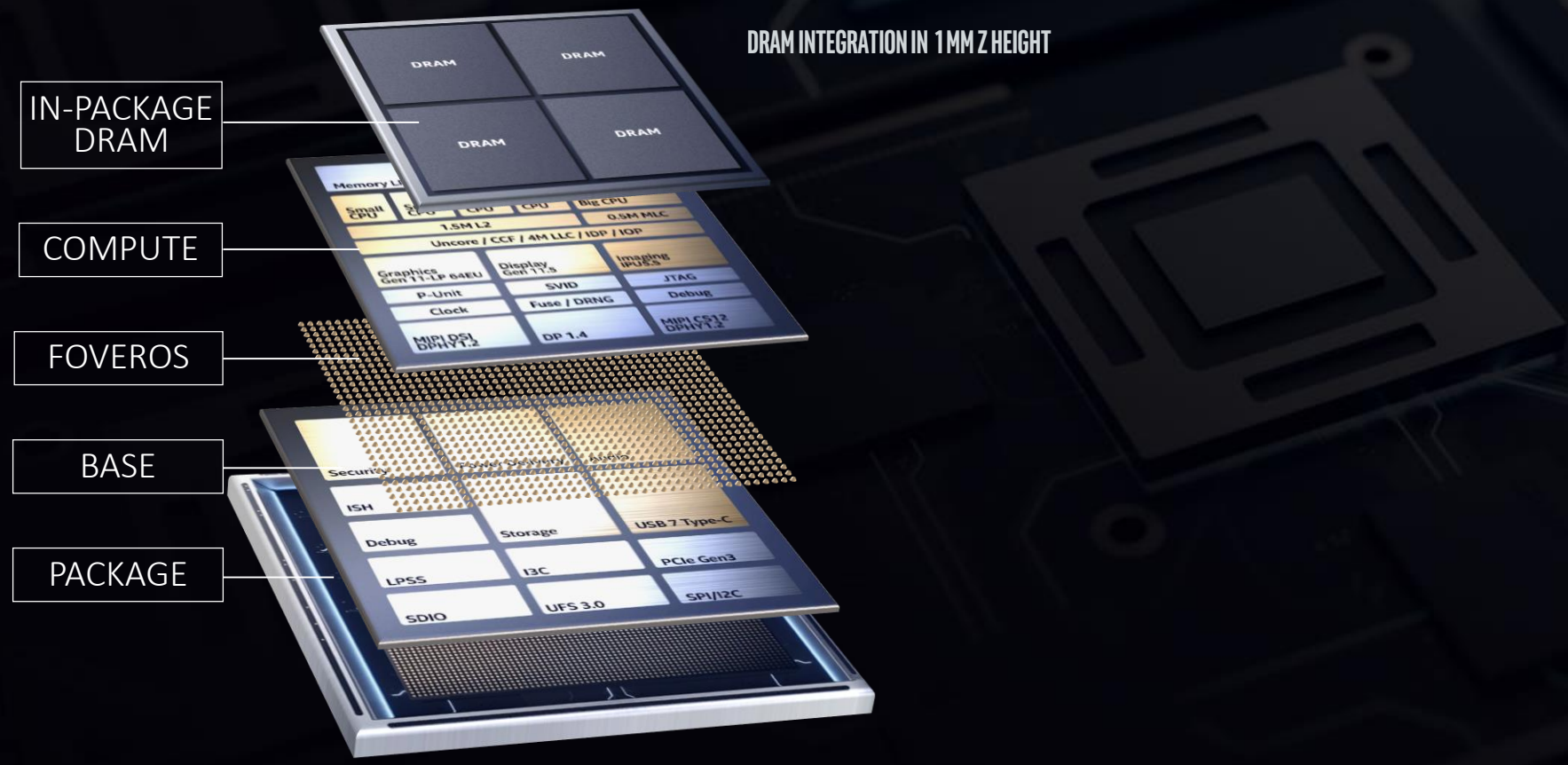
# LAKEFIELD FOVEROS

10 NM COMPUTE PROCESS FOR CORES AND GRAPHICS



# LAKEFIELD FOVEROS

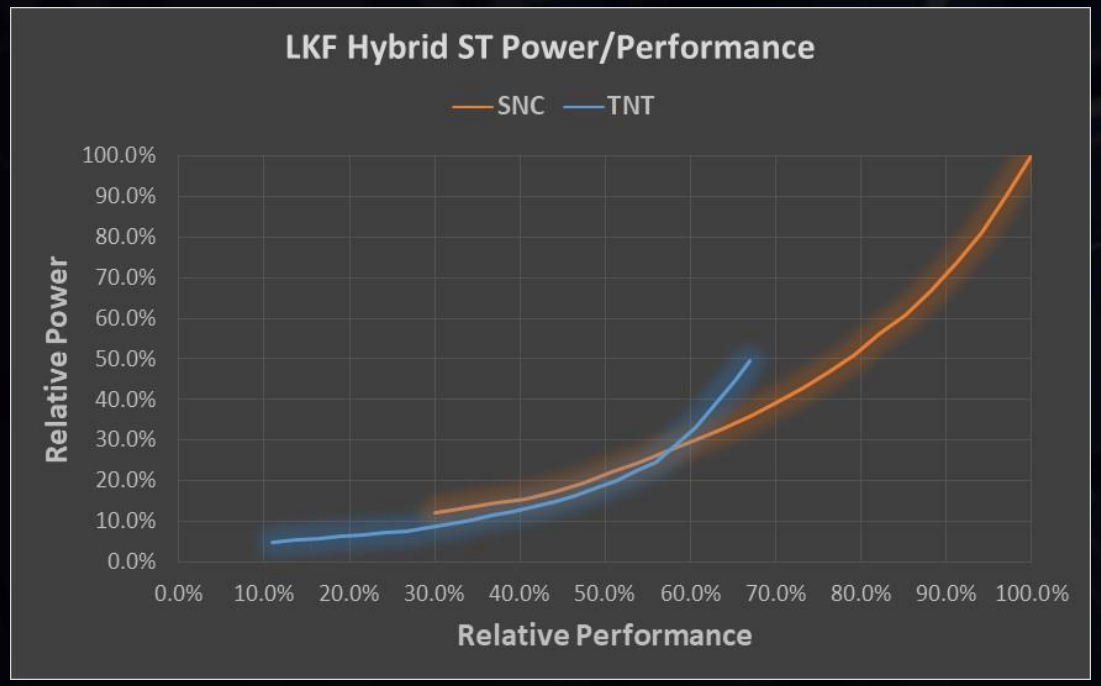
DRAM INTEGRATION IN 1MM Z HEIGHT

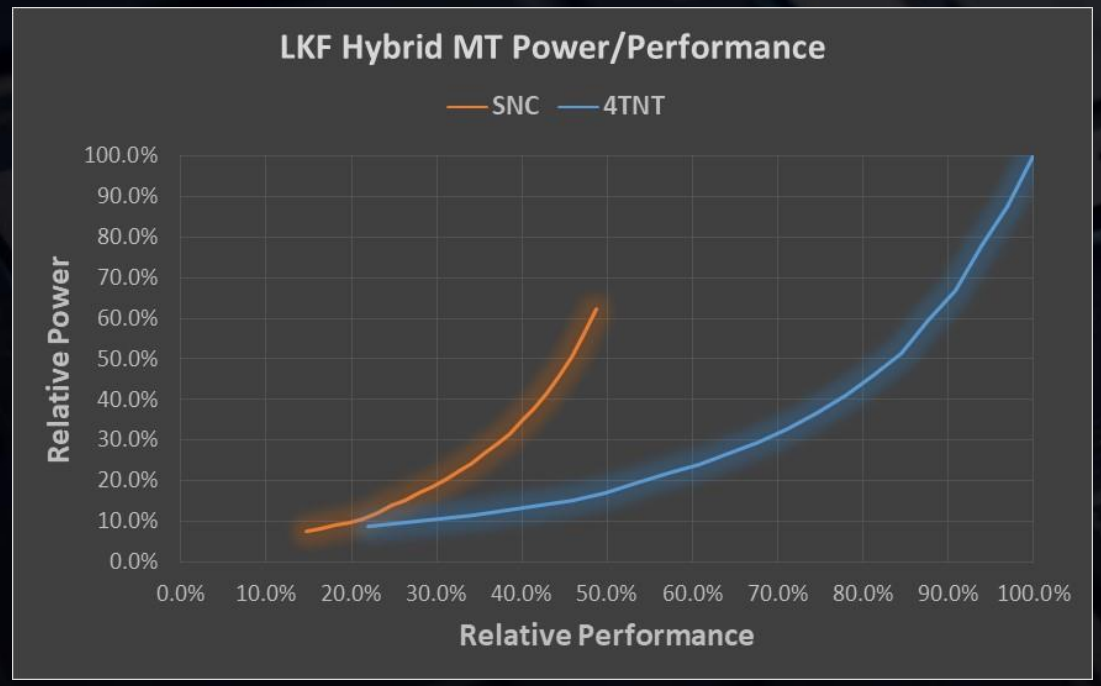


# ADVANTAGES OF HYBRID COMPUTE

- Big-Bigger Compute combination, ideal for mobility compute use case
- Heavy compute, bursty workload on SNC core
- Light compute workload on ATOM/Tremont, w/o compromising on performance
- Low power scenarios that are key to Battery life run on Tremont cores

# LKF HYBRID POWER PERFORMANCE




**SNC Bigger Core** delivers

- Single Thread Performance and Efficiency at burst

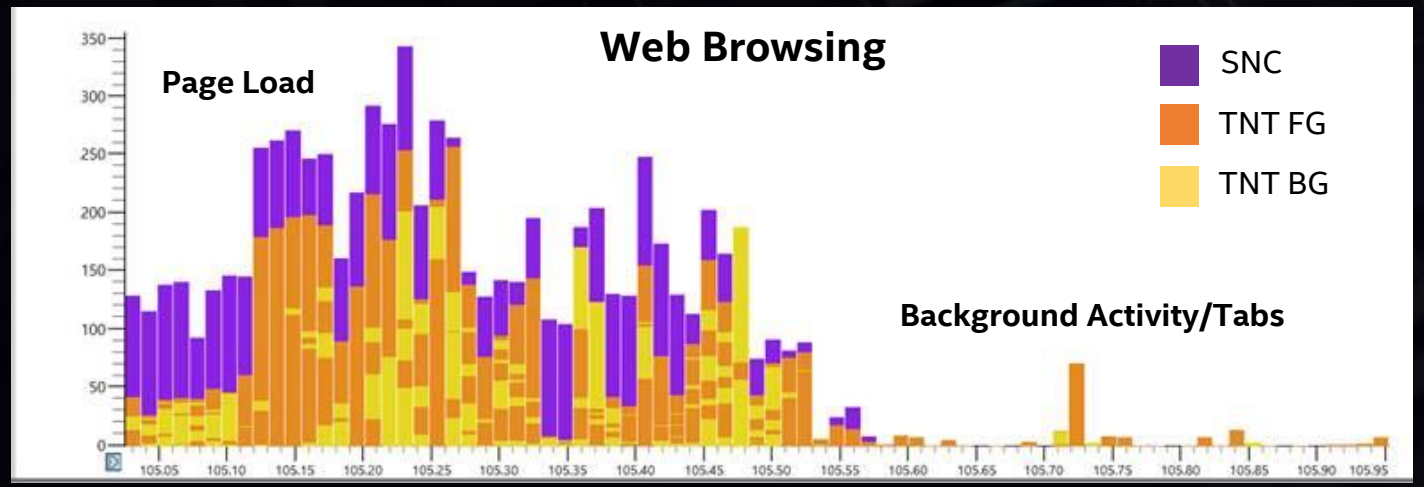
**TNT Efficient Atom** cores deliver

- **MT perf** and core count/area efficiency
- **Power Efficiency** with realistic workloads
- **Battery Life** (HoBL)

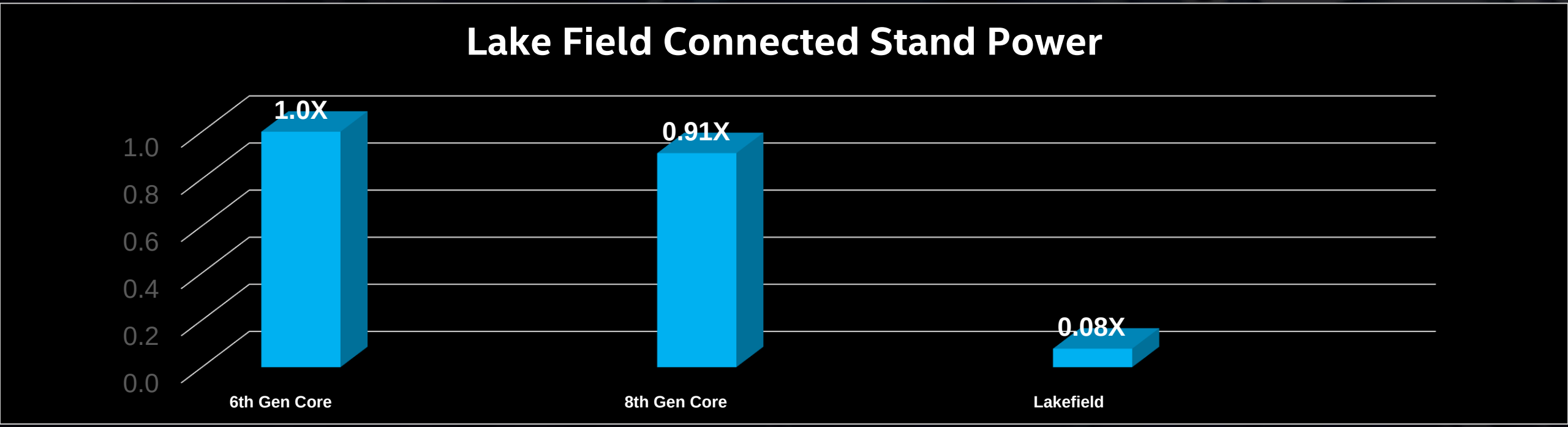
For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.

# IA HYBRID ARCHITECTURE

- Dynamic feedback to the OS/SW on Hybrid Core PnP capabilities
- Performance/responsiveness threads scheduled on SNC core
- Background and threads scheduled on TNT cores
- All cores execute threaded/concurrent applications



# GEN OVER GEN CONNECTED STANDBY IMPROVEMENTS

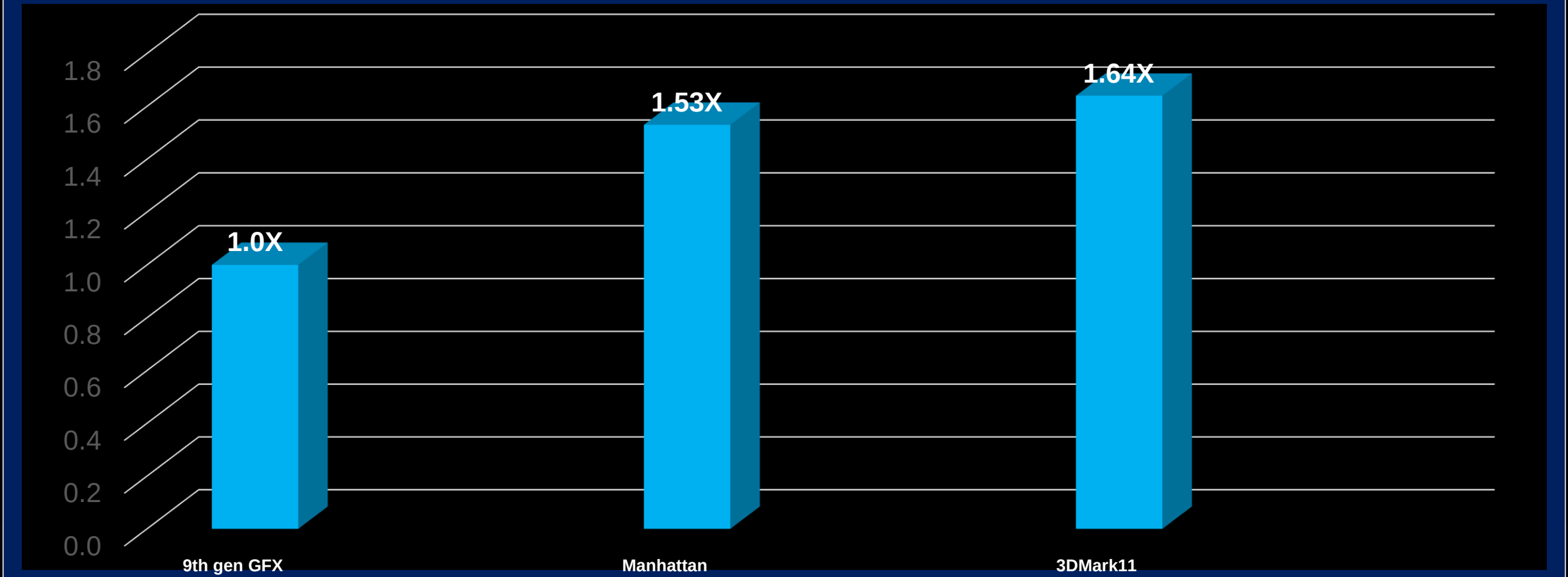



**Architecture, Process & Design Optimizations**

1. IP partitioning between Compute & Base
2. Vnn Removal, LDO removal and low leakage power gating in base die
3. USB and DDR Phy improvement
4. Very Low leakage transistor usage
5. Logic, Memory, and Clock IP Power scaling

# LAKEFIELD GRAPHICS IMPROVEMENTS

## Lakefield GFX performance @7W



# LAKEFIELD SUMMARY

- LKF introduces first in the industry, a product with 3D stacking, and IA hybrid computing
- First PC Compute SOC with dimensions of 12 x 12 x 1 mm, and Standby power of 2.x mW
- LKF designed for lower power, to enable new thin/ form-factors, 2 in 1's, dual-display devices
- LKF architecture has significant improvements over previous generation with ~0.1x S0iX3, ~0.5x PCB Core area and ~1.5x GFX performance
- Silicon is in final phase of production readiness targeting end of Q4'19

Background Activity/Tabs

# NOTICES AND DISCLAIMERS

- Performance results are based on testing as of 08/01 /19 and may not reflect all publicly available security updates. See configuration disclosure for details. No product can be absolutely secure.
- Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information about performance and benchmark results, visit http://www.intel.com/benchmarks]
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