ENT-AN1026
Application Note
Layout and Assembly Considerations for TQFP Packages with Inner Leads

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Layout and Assembly Considerations for TQFP Packages with Inner Leads

The purpose of this document is to provide PCB design reference information and surface mount guidelines relating to the novel integration of inner leads in TQFP packages used for Microsemi products, including VSC7420/VSC7421/VSC7422 SparX-III Ethernet switches and VSC8522 12-port 10/100/1000BASE-T PHY. The Microsemi VSC5609EV reference board, featuring the VSC7422 and VSC8522, is used as the primary reference for this application note.

The PCB Design section includes detailed PCB land pattern information, recommended escape routing, and center exposed pad layout guidelines. The Surface Mount Guidelines section provides stencil information and rework procedures.

For further reference, please consult the VSC7420, VSC7421, VSC7422, and VSC8522 Datasheet; VSC7420, VSC7421, and VSC7422 Hardware Manual; and VSC8522 Design and Layout Guideline. A datasheet, application notes, and other information for the FusionQuad package can be downloaded from the Amkor website.

3 PCB Design

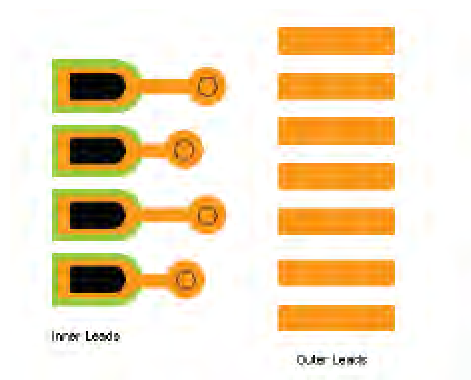
The following table shows the dimensions of the metal pad and solder mask opening sizes for both the inner and outer leads.

Table 1 • PCB Land Pattern Dimensions

Leads	Metal Pad	Solder Mask Opening Sizes
Inner	0.25 mm x 0.70 mm	0.35 mm x 0.80 mm
Outer	0.25 mm x 1.6 mm	0.30 mm x 1.70 mm

The following illustration shows the recommended escape routing from the inner leads.

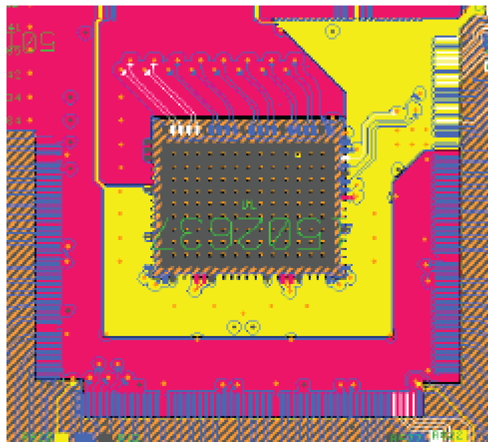
Figure 1 • Escape Routing



Do not align the vias, as this may result in plane breakage.

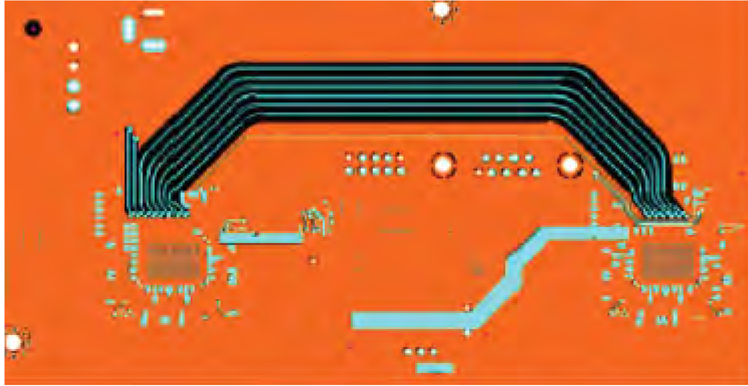
The following illustration shows heat dispersion.

Figure 2 • Thermal Vias Placed on Center Exposed Pad



The recommended thermal via type that should be placed on the center exposed pad is 0.3 mm in diameter through the hole without solder mask. In the case of the Microsemi VSC5609EV reference board, there are a total of 117 thermal vias placed on each VSC7422 and VSC8522 center exposed pad. The center exposed pad is the main path for heat dispersion from the die, through which thermal vias translate heat from the PCB top layer to copper planes located either internal to or on the bottom surface of the board. For a typical 2-layer PCB design, power planes are created on the top layer surrounding the center exposed pad (in the previous illustration, yellow denotes the 2V5 power plane and pink denotes the 1V0 power plane), with the bottom layer serving as the only layer that provides a copper plane for heat dispersion. Thus, it is strongly recommended to make as many thermal via connections as possible from the center exposed pad area to the copper plane on the bottom side. An inadequate thermal path here could cause device junction temperature increases of 10 °C or more. The following illustration demonstrates a good example extracted from the Microsemi VSC5609EV reference board layout file.

Figure 3 • Maximizing Copper Connections to Facilitate Heat Dispersion

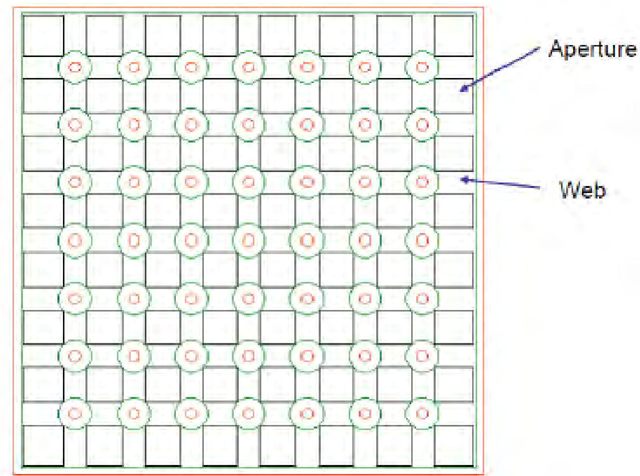


4 Surface Mount Guidelines

The following is stencil information:

- Thickness: 100 to 125 µm
- Outer leads aperture: same size as outer land pattern on board
- Inner leads aperture: same size as inner land pattern on board

Figure 4 • Example Stencil Design for Center Exposed Pad



In order to avoid solder from wicking through the vias, the apertures should not be placed above thermal vias on the PCB.

For an effective rework procedure, the following steps are recommended.

1. Remove the package.
2. Clean the board site.
3. On the replacement package, paste print on the inner leads and center exposed pad. The following illustration shows an example stencil.

Figure 5 • Example Stencil for Inner Leads Paste Printing

4. Flip package on the board.
5. Reflow.

6. Hand solder the outer leads.

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