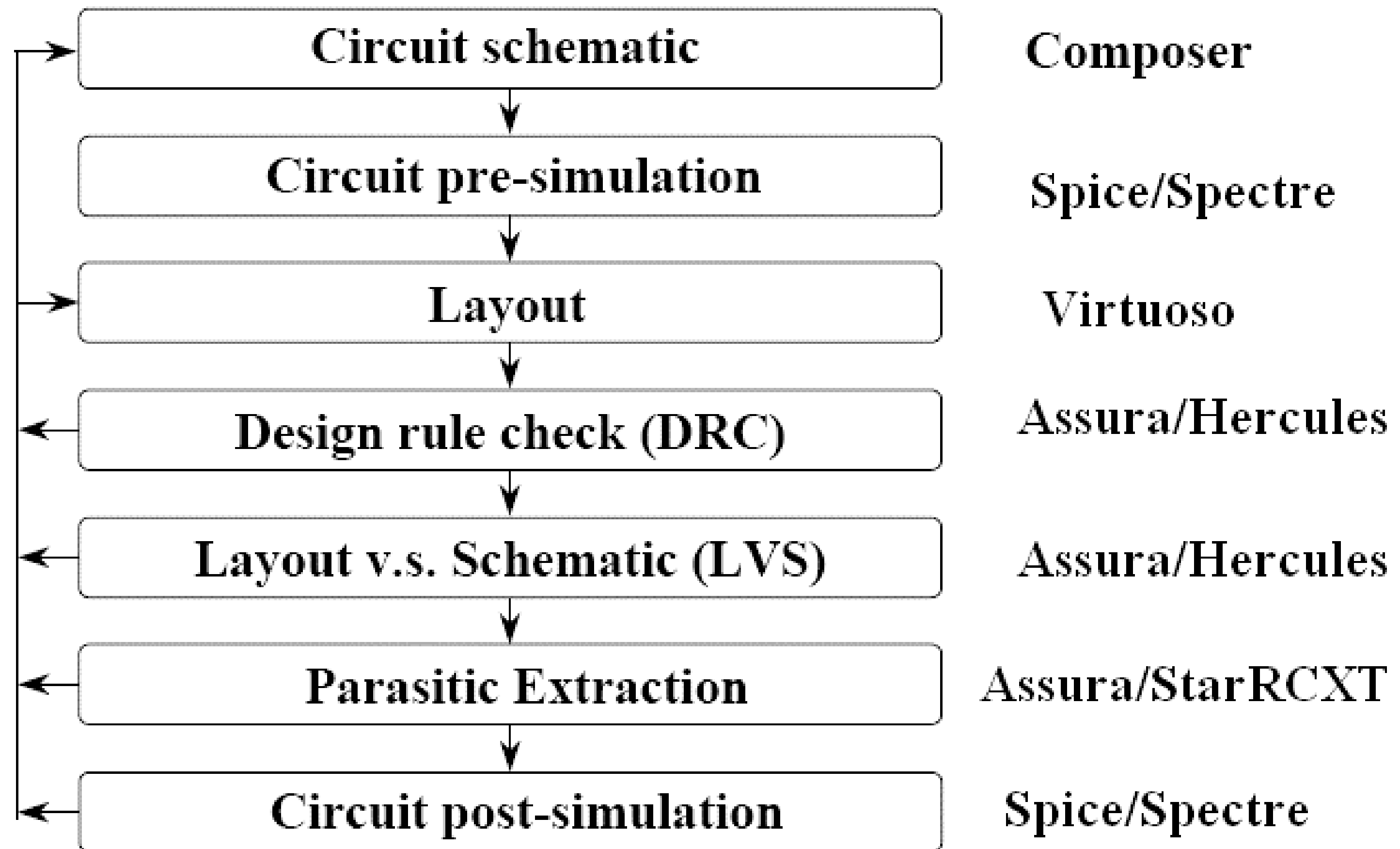
# Layout of Analog Circuits

Jyotirmoy Ghosh

Asudeb Dutta

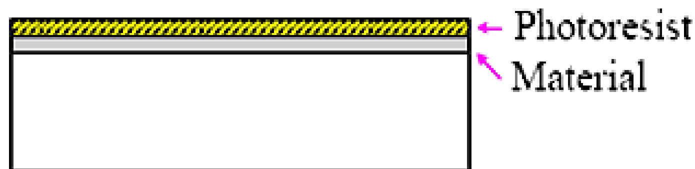
Advanced VLSI Design Lab


Fully Custom IC Design Flow
Circuit schematic
Composer
Circuit pre-simulation
Spice/Spectre
Layout
Virtuoso
Design rule check (DRC)
Assura/Hercules
Layout v.s. Schematic (LVS)
Assura/Hercules
Parasitic Extraction
Assura/StarRCXT
Circuit post-simulation
Spice/Spectre

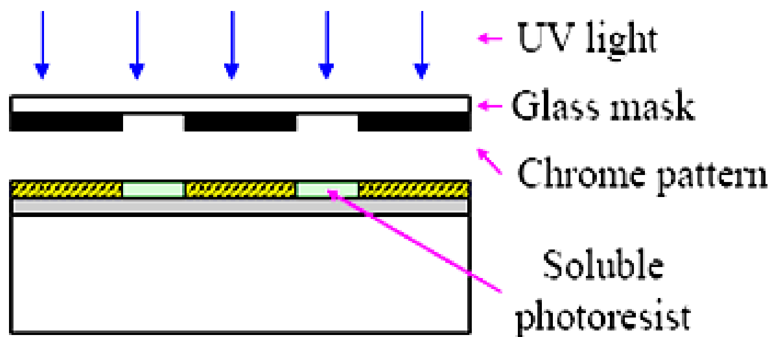
# IC Photolithographic Process

- Apply material to wafer to be patterned

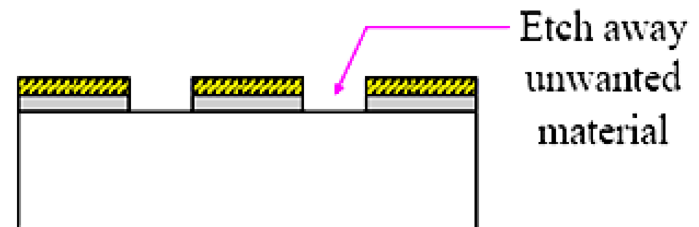
- Spin on positive photoresist



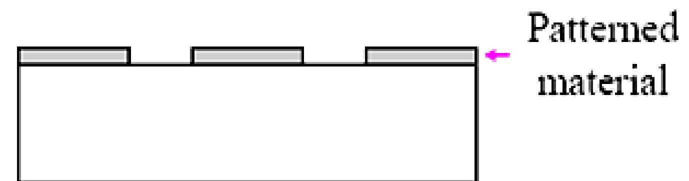

- Pattern photoresist with UV light through glass mask



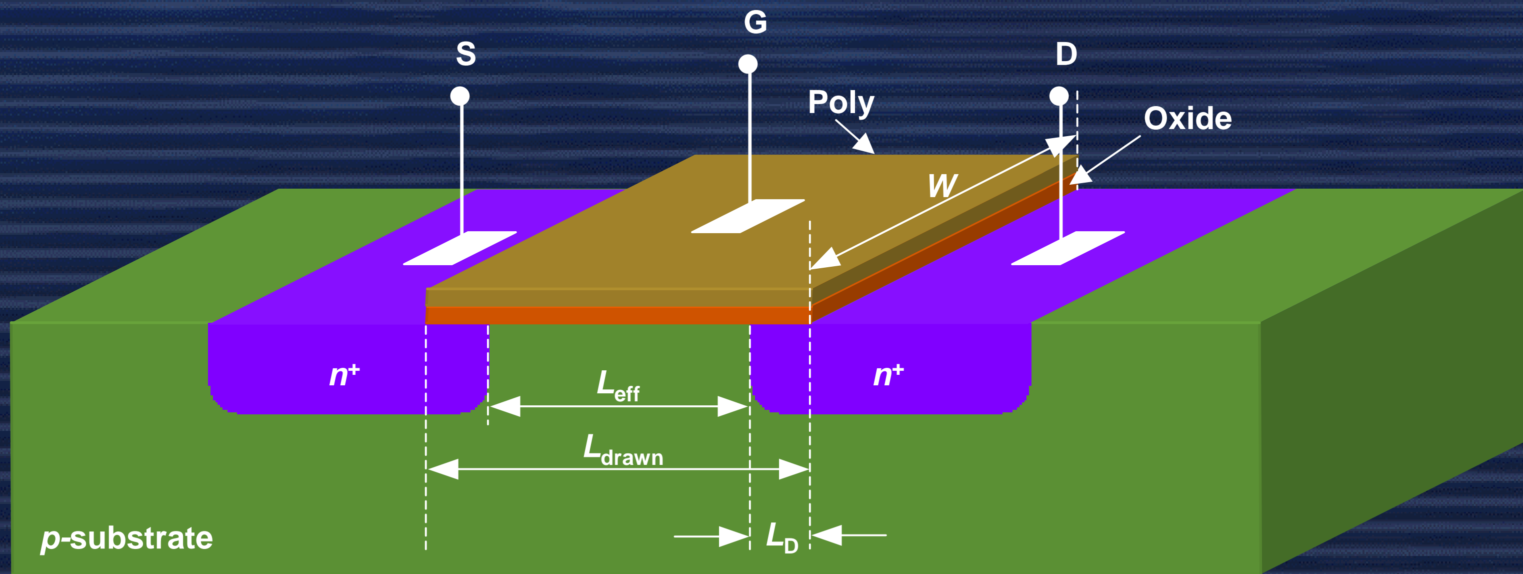

- Etch and apply specific processing step




- Wash off photoresist

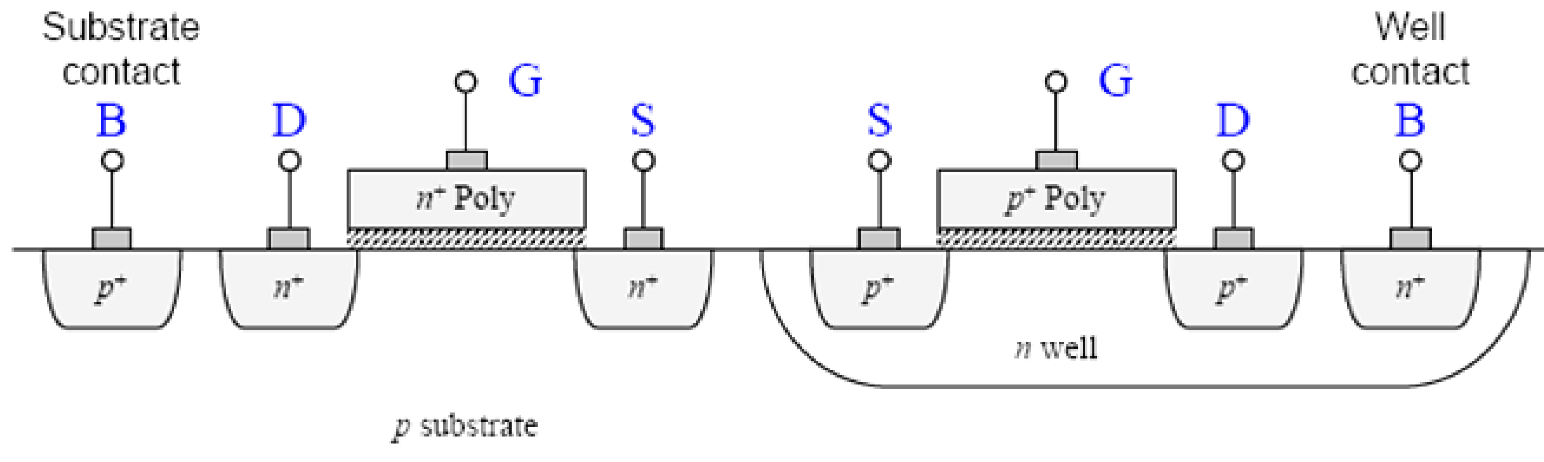


# MOSFET (NMOS) Structure



# CMOS P-Substrate Process Flow

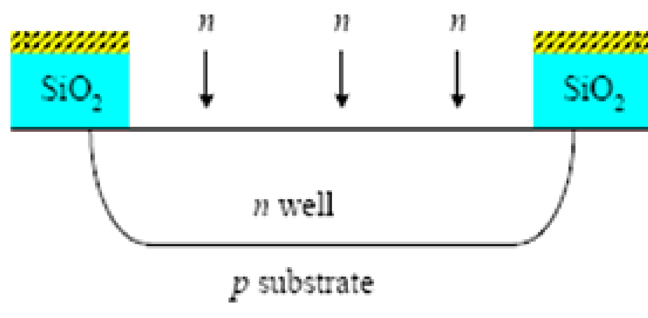
- **Cross section view**



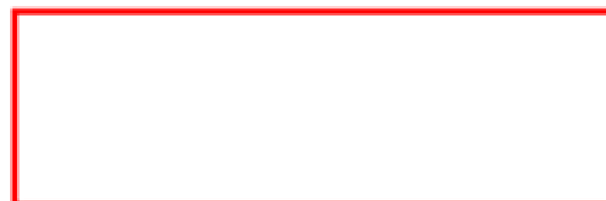

- **NMOS process steps**
  - Active region, poly gate, p+/n+ implant, metal contact/line
- **PMOS process steps**
  - N well, active region, poly gate, p+/n+ implant, metal contact/line

# Process Flow v.s. Layout

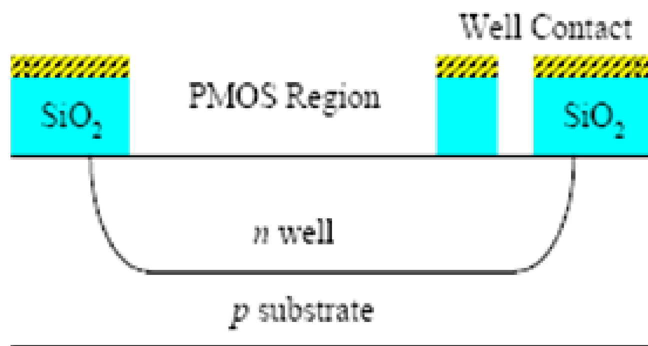
- N well




- NWELL layer (NW)



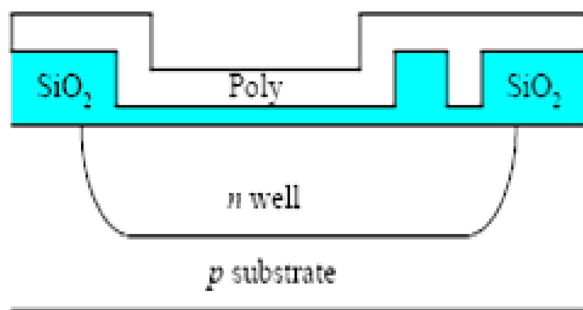
- Active region

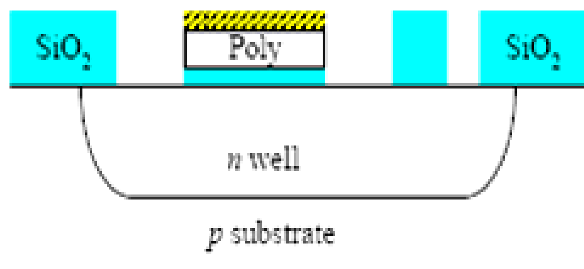


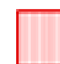

- DIFF layer (OD)

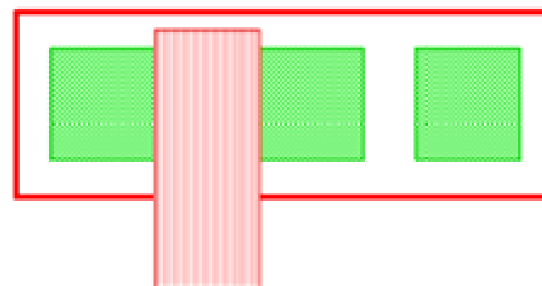
# Process Flow v.s. Layout

- Poly gate



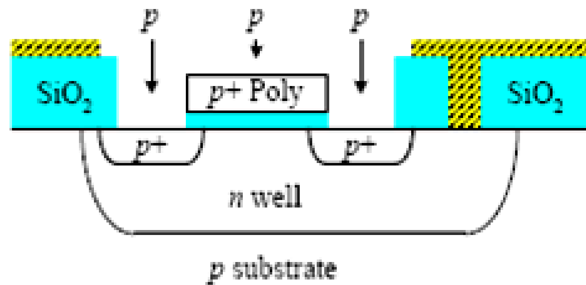


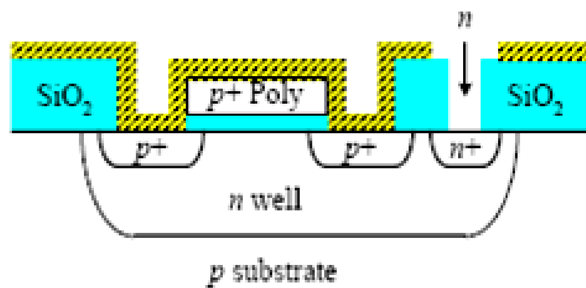

- POLY1 layer (PO) 

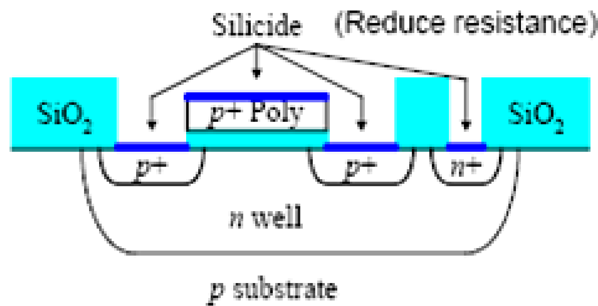


# Process Flow v.s. Layout

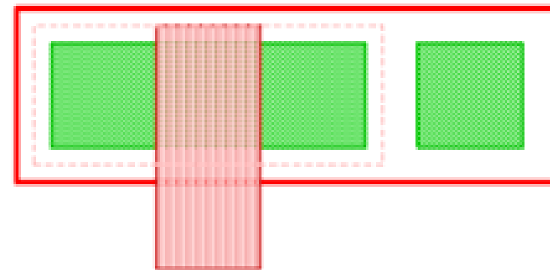
- **P+/N+ implant**



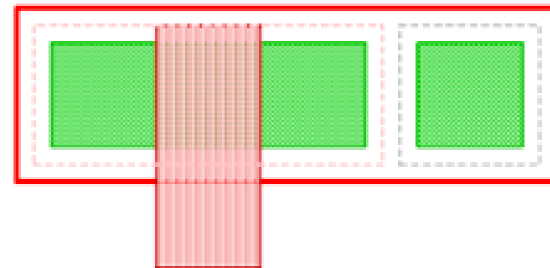




- **PIMP layer (PP)**

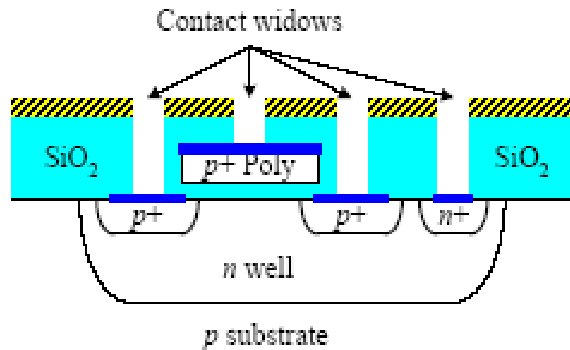


- **NIMP layer (NP)**

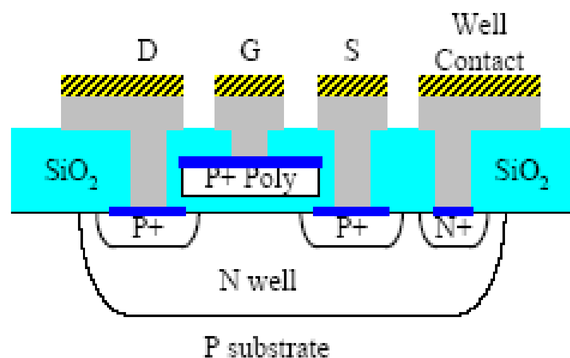


# Process Flow v.s. Layout

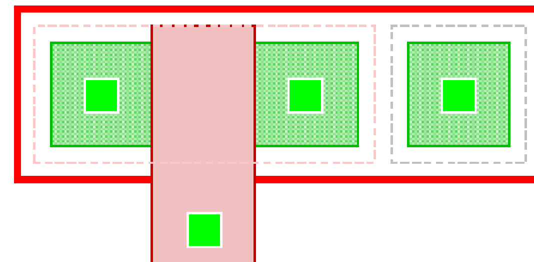
- **Metal contacts/lines**

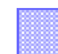


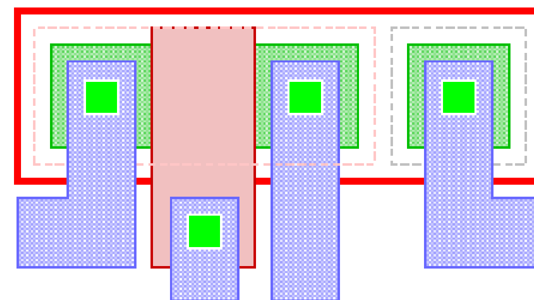

Metal: Al or Cu




- **CONT layer (CO)**

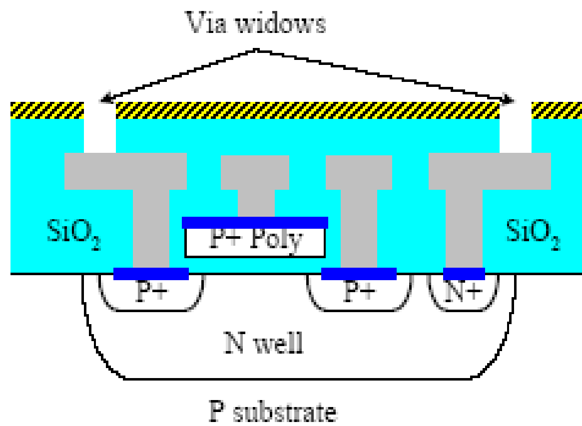


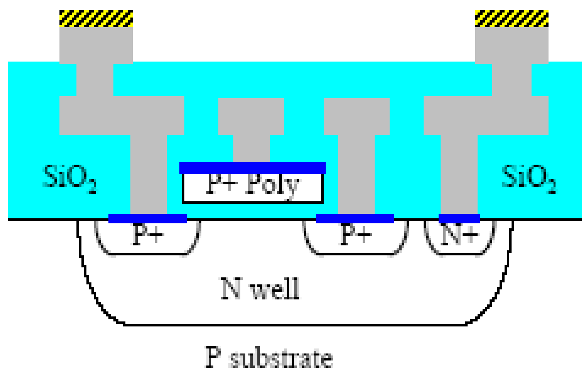
- **METAL1 layer (M1)** 



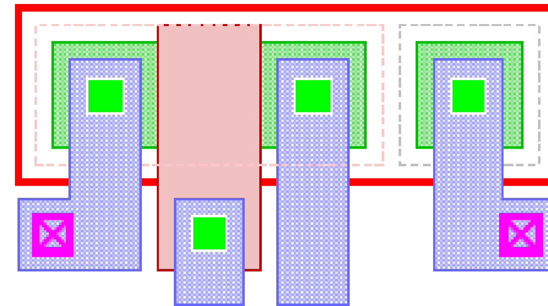
# Process Flow v.s. Layout

- **Metal vias/lines**

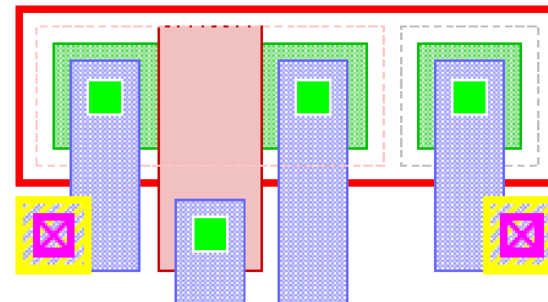


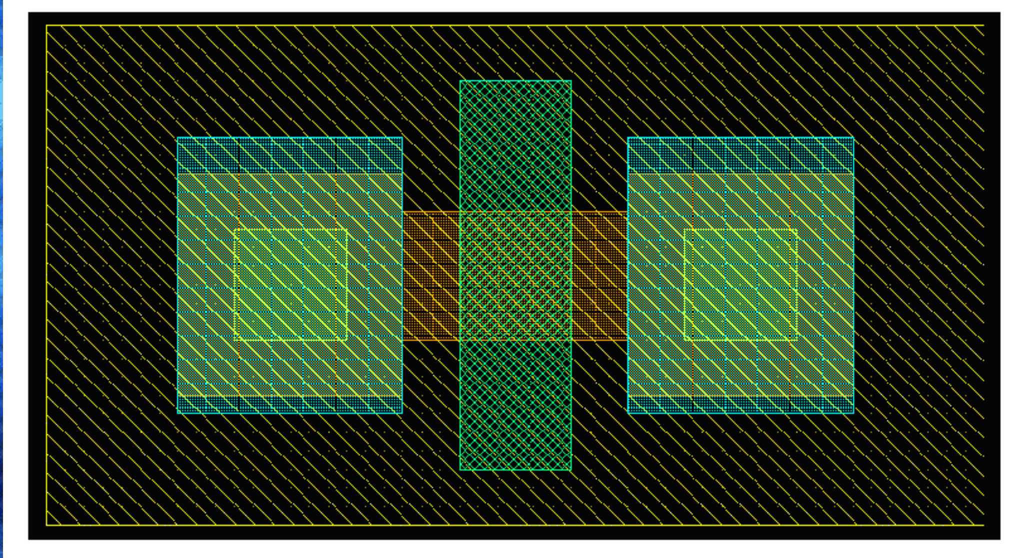

- **VIA12 layer (VIA1)**



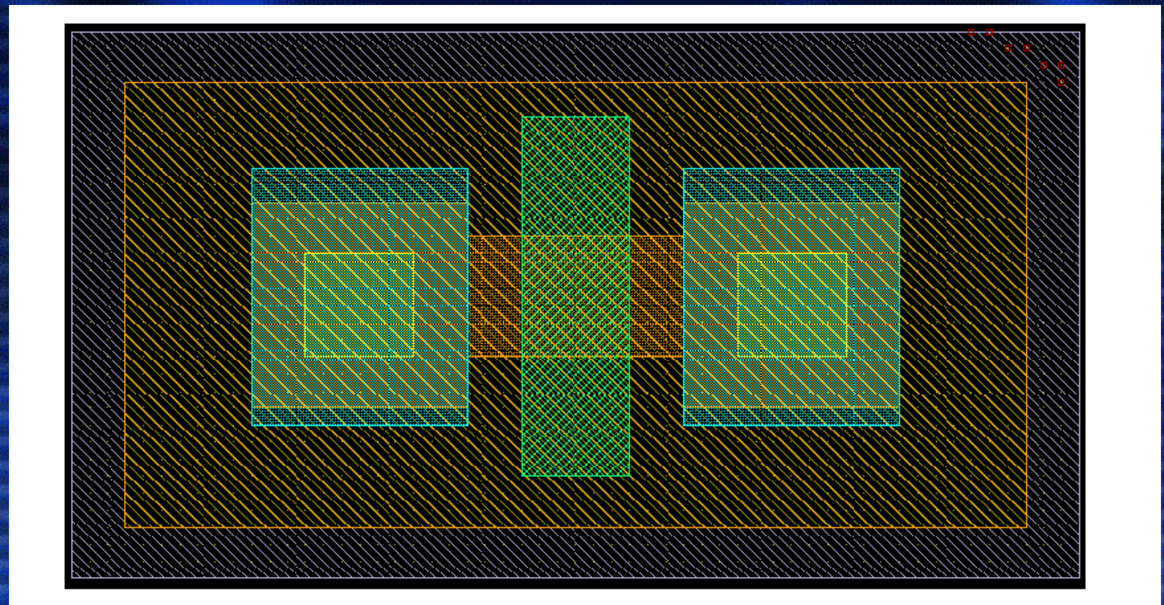
- **METAL2 layer (M2)**



# MOS Device Layout



NMOS Layout



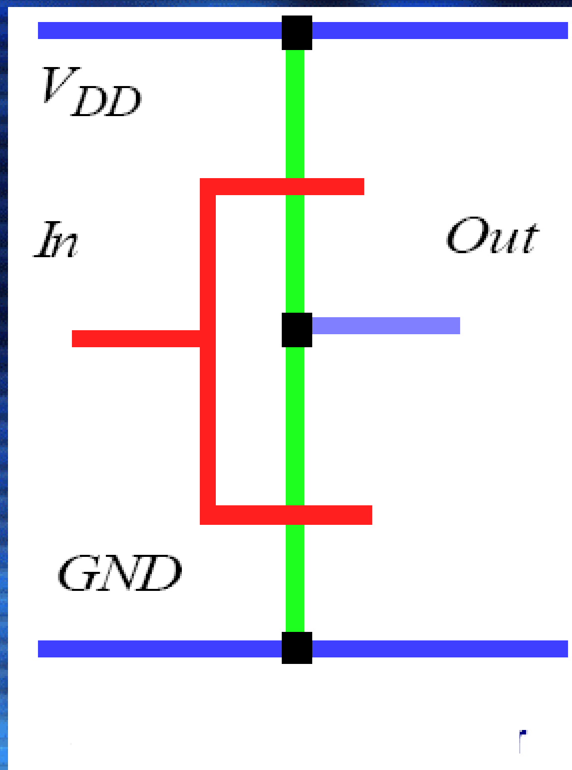
PMOS Layout

# Stick Diagram (Symbolic Layout)

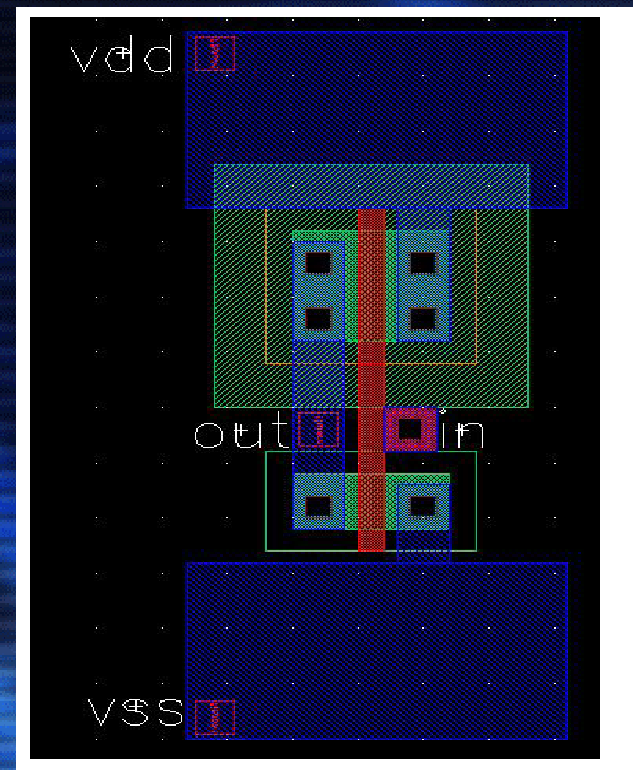
In stick diagram the lines represents the corresponding layers in layout .i.e. rather than drawing a rectangle to draw poly you are just drawing a line. this simplify designer's work in drawing layout "on paper"

1 Dimensionless layout entities with legend for each layer

2 Only topology is important



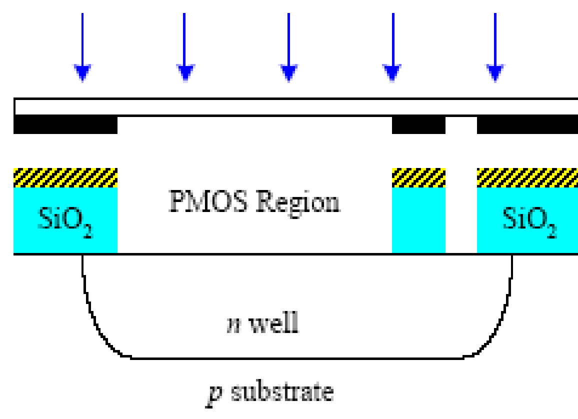

Stick Diagram of Inverter

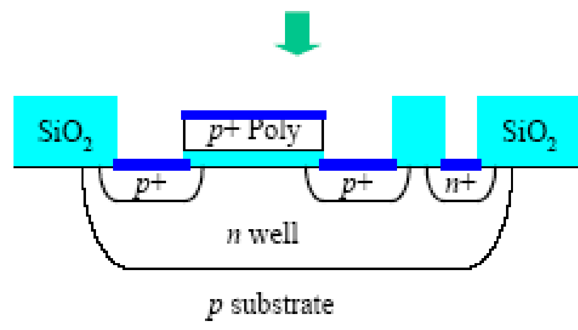


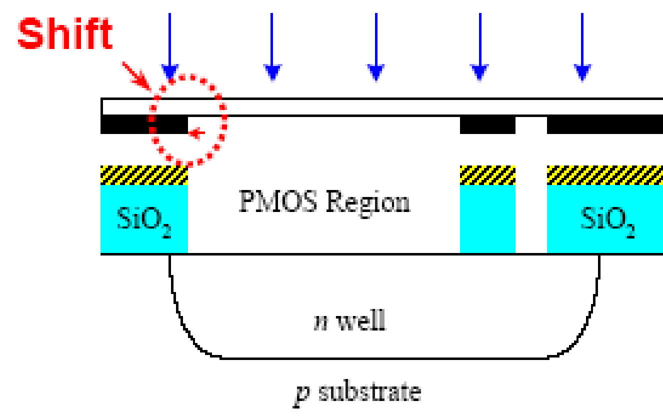

Actual Layout of Inverter

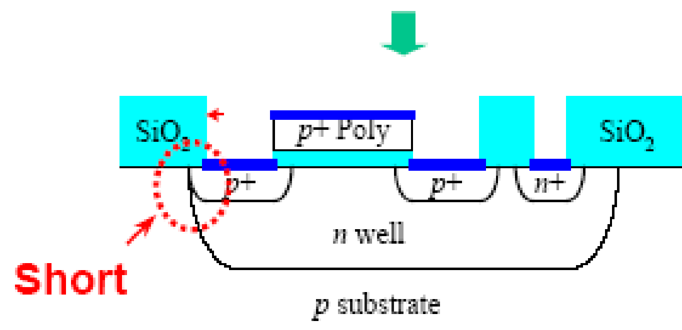
# Design Rule Check (DRC)

- **Tolerate nonideal effects and guarantee device successful fabrication**
  - Mask alignment error
    - Ex: alignment of N well and active region masks



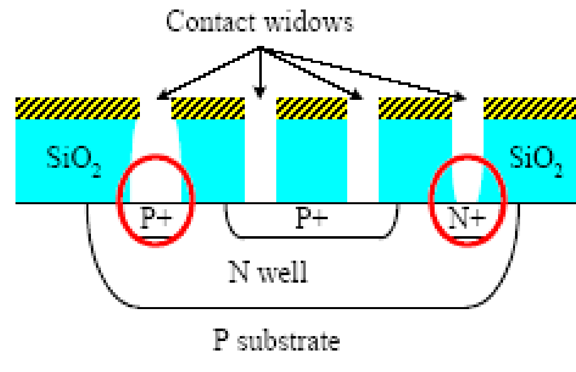



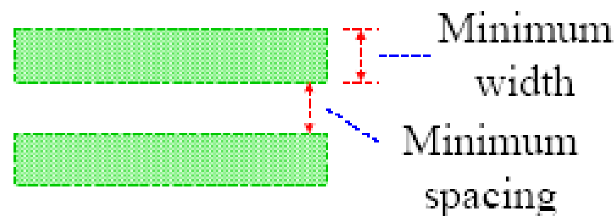



# Design Rule Check (DRC)

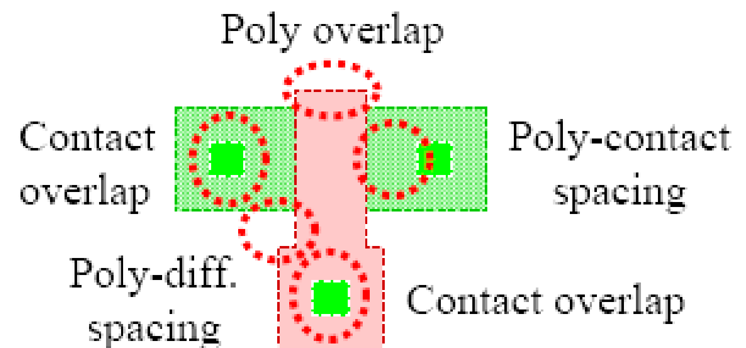
- Exposure and etching variation
  - Ex: different contact windows ➡ different contact resistance




- **Two types of design rules**



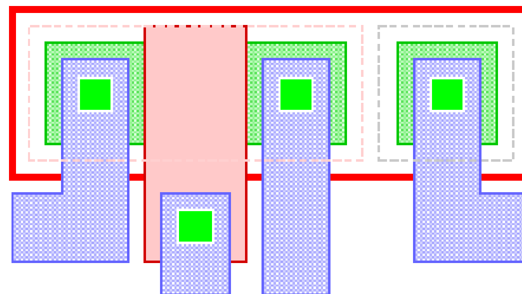

**Resolution**

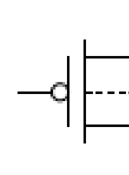



**Alignment**

# Layout v.s. Schematic (LVS)

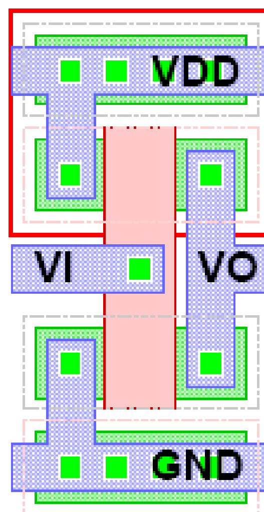
- **Guarantee the fabricated circuits is the same as the simulated one**
  - Check device parameters

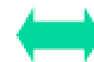
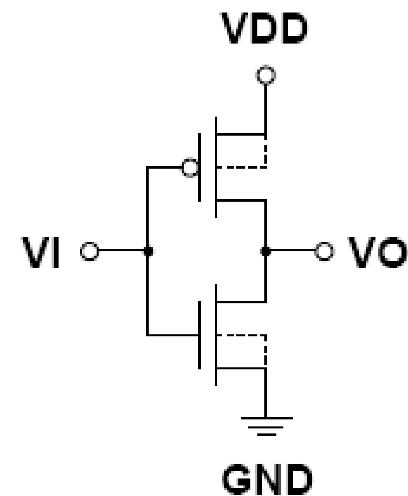




Model name
Channel width
Channel length

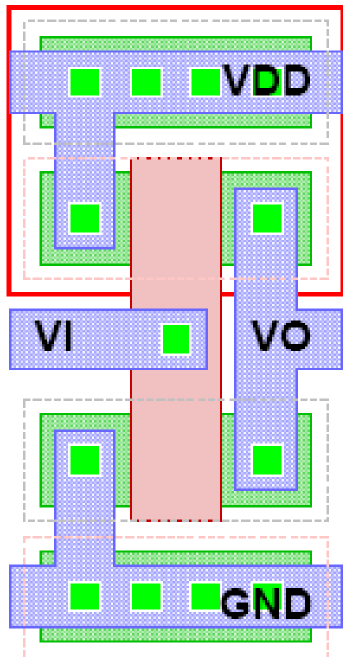
  - Check device interconnections and circuit input/output ports

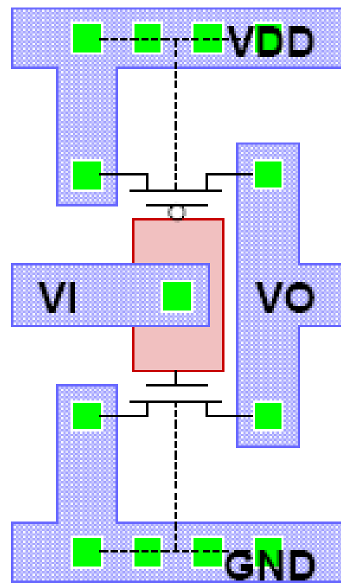


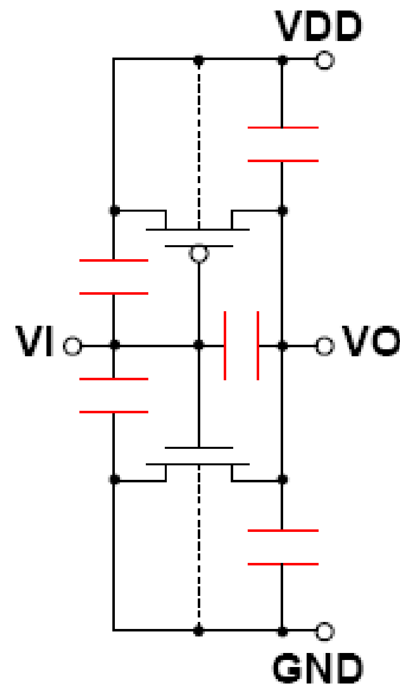



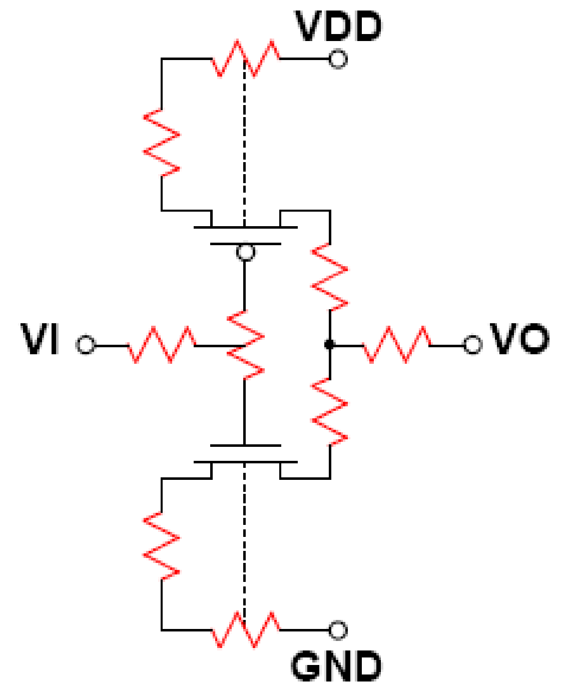
# Parasitic Extraction (PEX)

- Evaluate interconnection *RC* effects




Only *C* effect

Only *R* effect

# Layout Steps

- Floor planning

  Division of the entire die area among subcomponents to facilitate interconnection and effectively utilize the area.

- Placement

  Placing the modules in the layout.

- Routing

  Connecting the modules with different metal layers.

# Issues of Analog Layout

- Use of more number vias
- Fingering and proper orientation
- Device matching
- Symmetrical and common centriod layout design
- Use of Guard ring and substrate trapping

# Passive devices

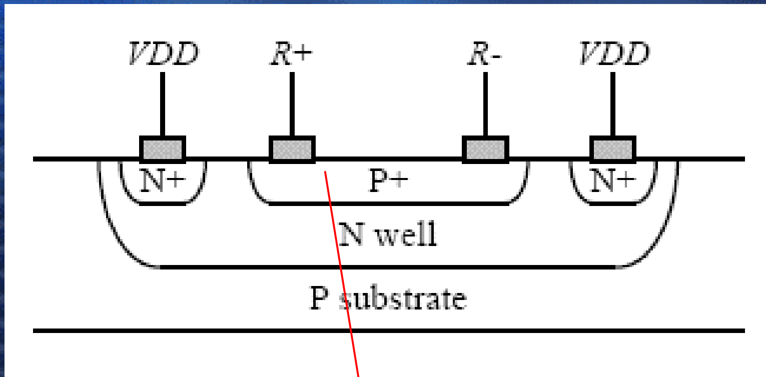
## Resistance (*cont'd*)

Resistors:

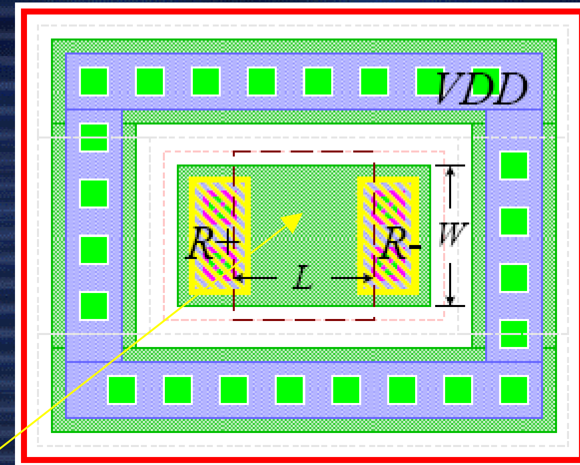
1) RPD (P+ Diffusion) -> R (sheet)= 83 ohm/

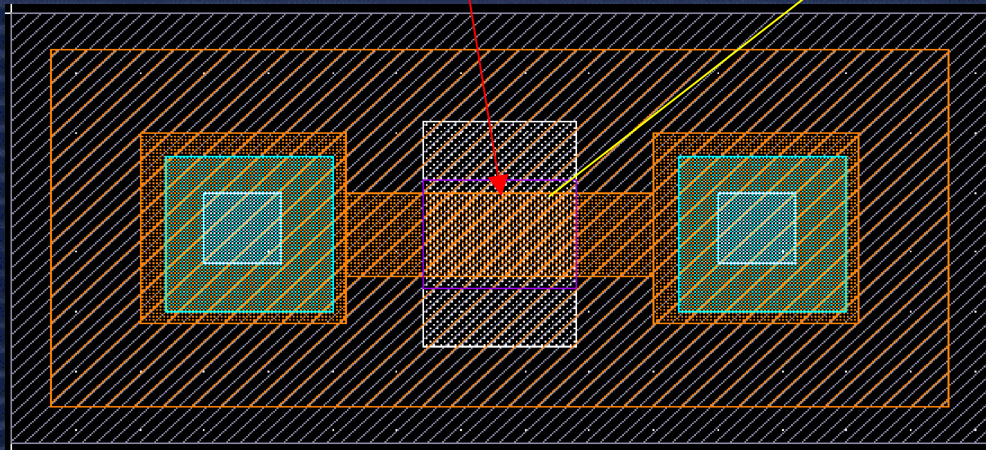
# Passive devices

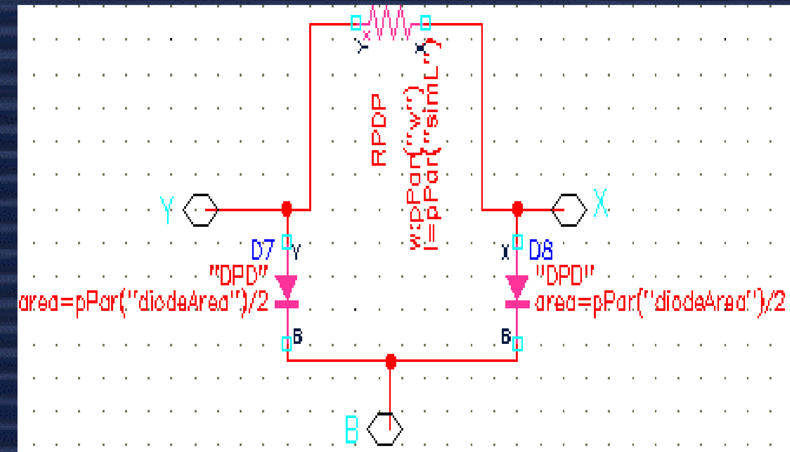
## Resistance (*cont'd*)




P+ Diffusion (RPD)






Equivalent Model

# Passive devices

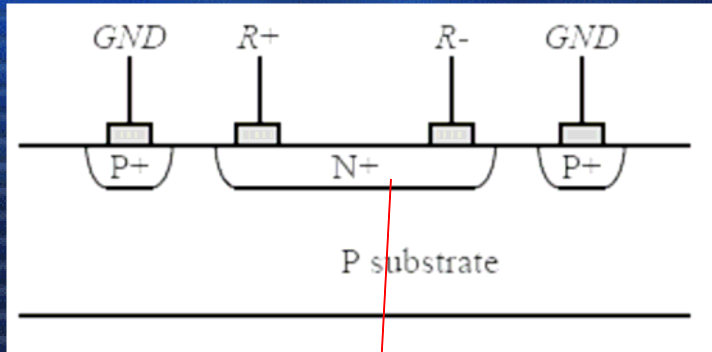
## Resistance (*cont'd*)

Resistors:

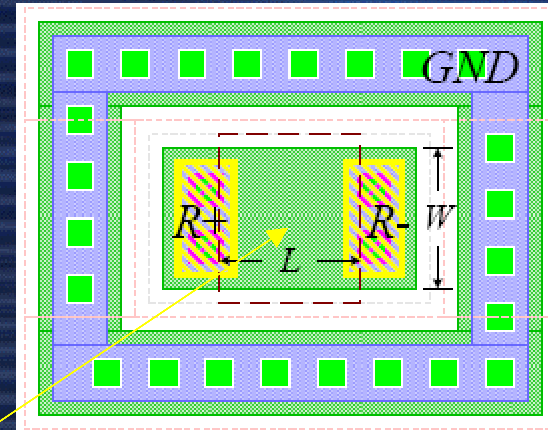
1) RND (N+ Diffusion) -> R (sheet) = 32 ohm/

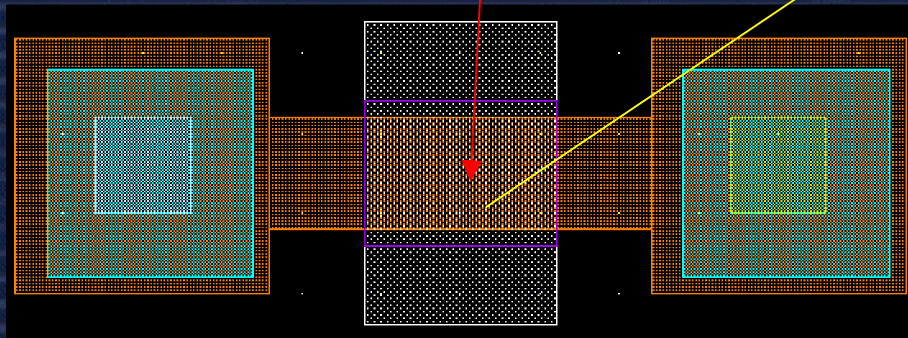
# Passive devices

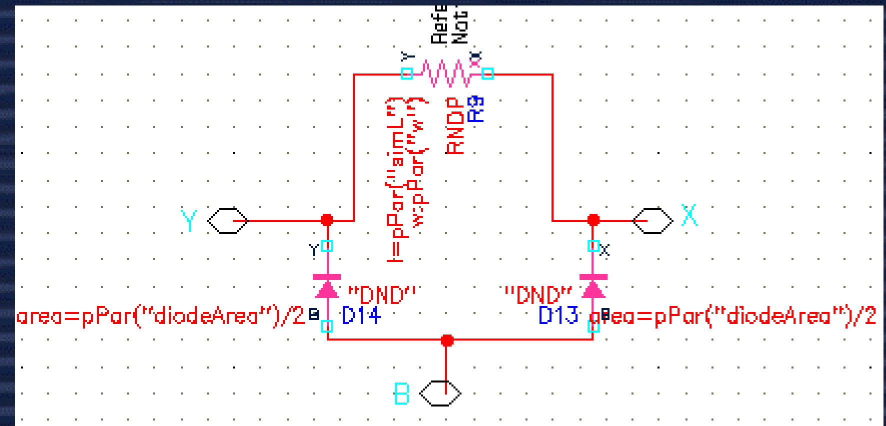
## Resistance (*cont'd*)




**N+ Diffusion (RND)**






**Equivalent Model**

# Passive devices

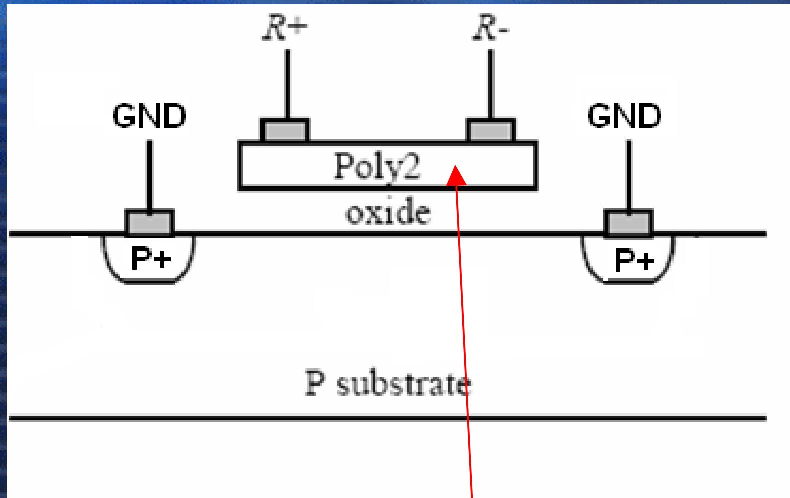
## Resistance (*cont'd*)

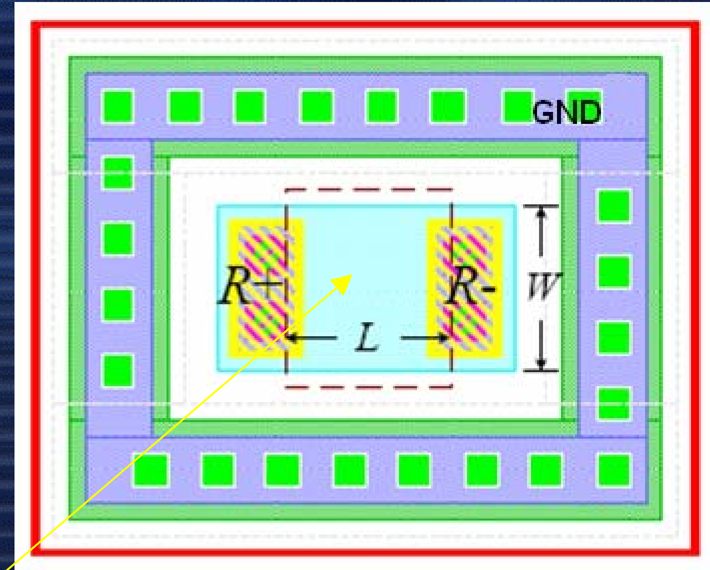
Resistors:

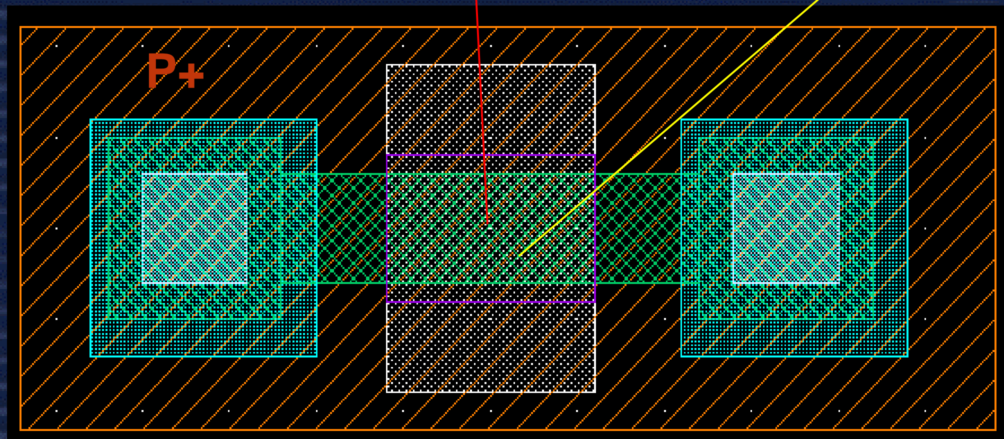
1) RPP (P+ Poly) -> R (sheet) = 175 ohm/

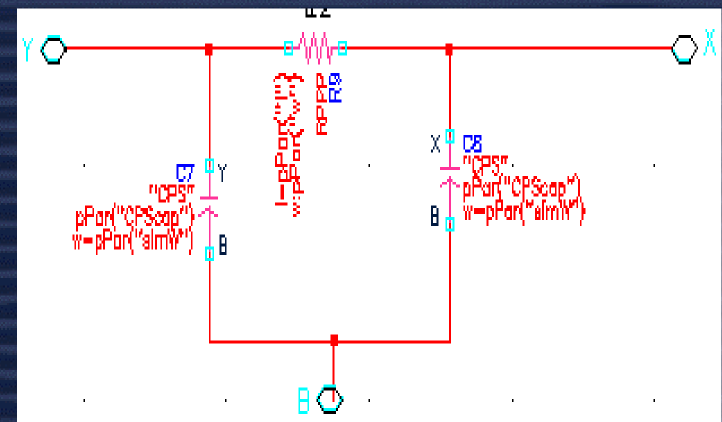
# Passive devices

## Resistance (*cont'd*)



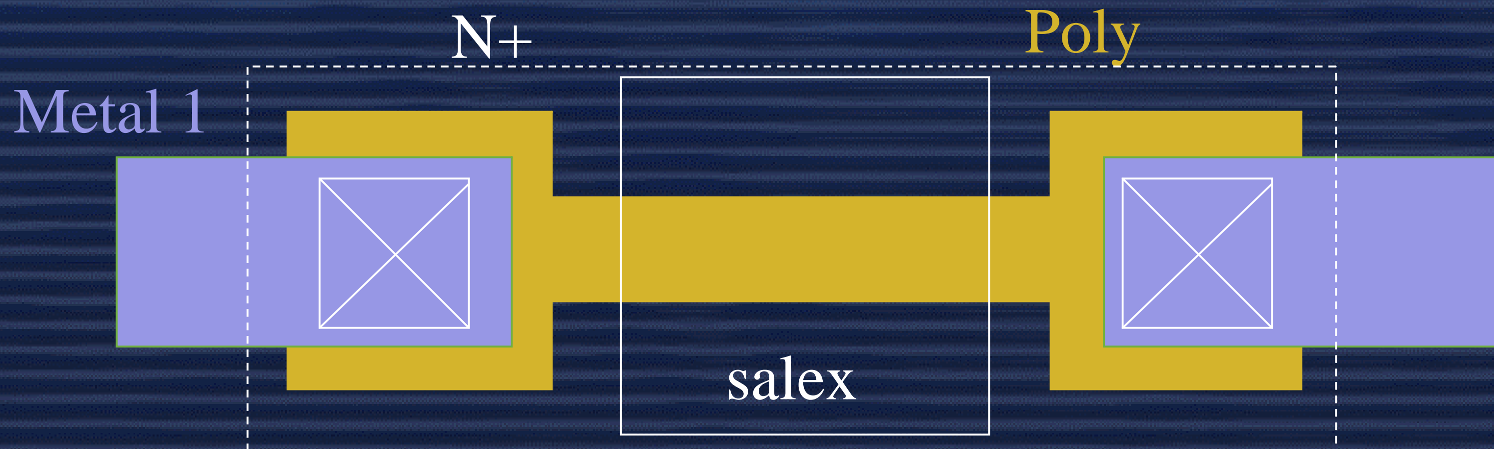

Equivalent Model

# Passive devices

## Resistance (*cont'd*)

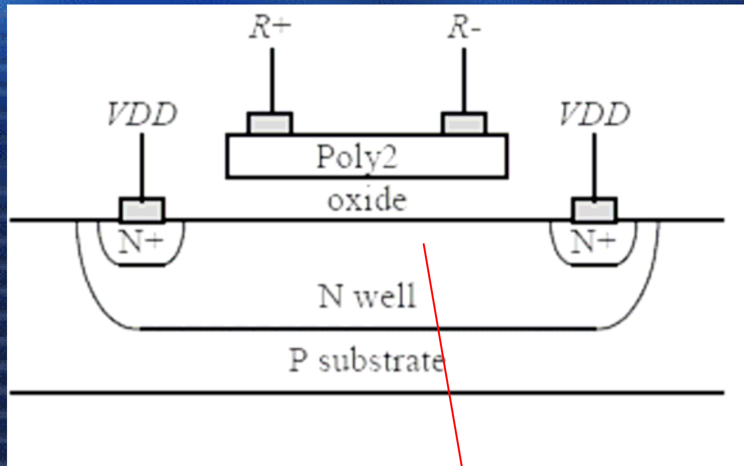
Resistors:

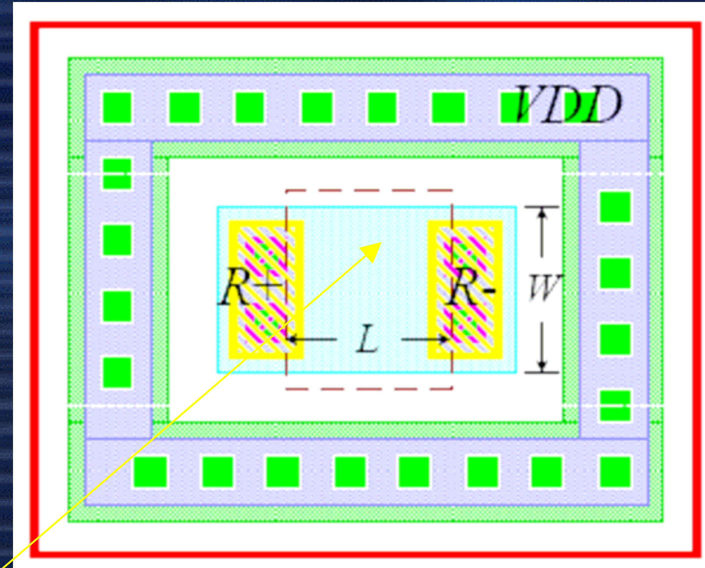
1) RNP (N+ Poly) -> R (sheet) = 125 ohm/

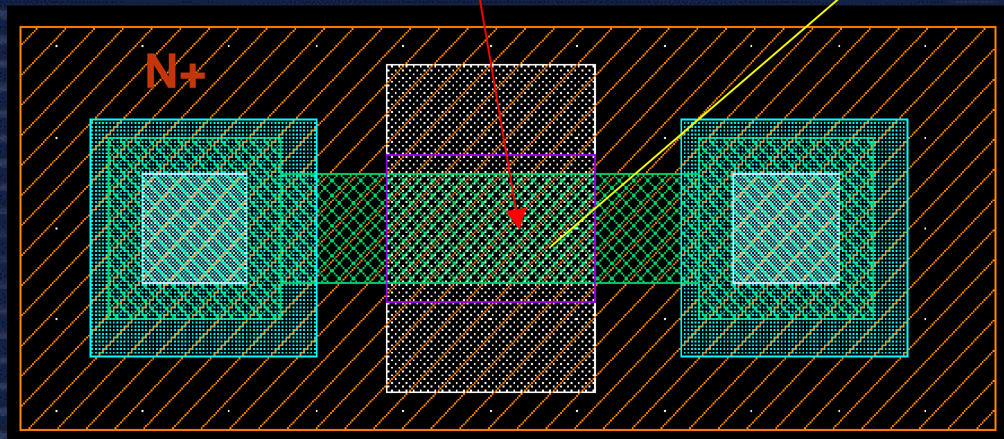


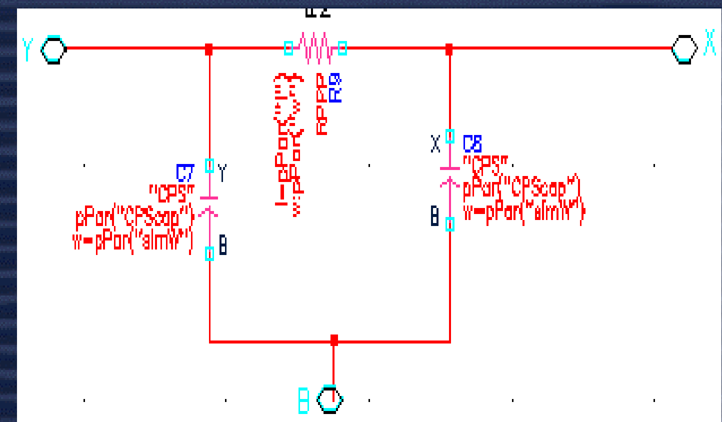
# Passive devices

## Resistance (*cont'd*)




**Equivalent Model**

# Passive devices

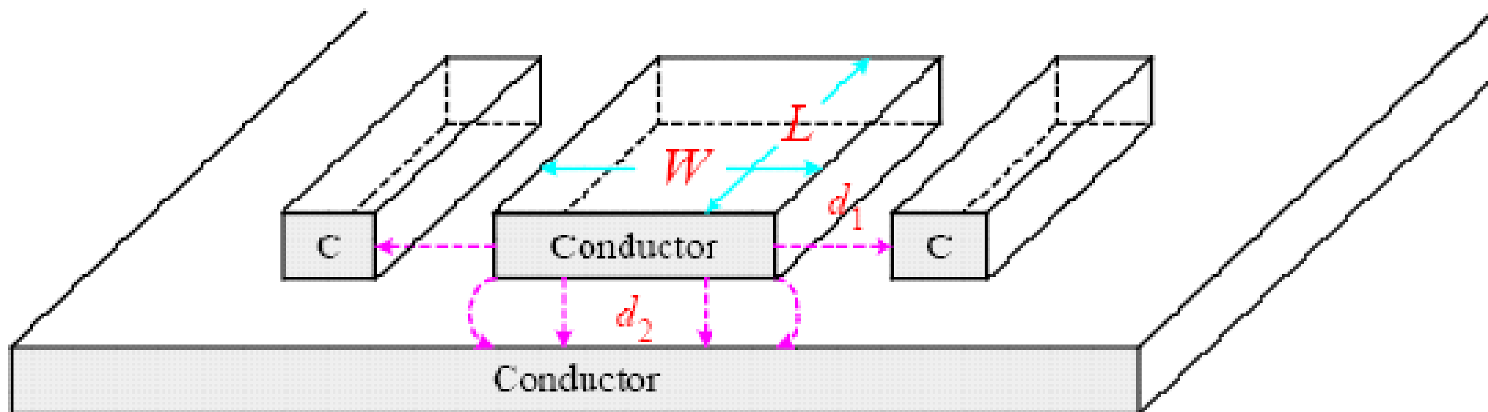
## Resistance (*cont'd*)

Choice of Resistances:

- Parasitic effect
- Process variation,
- Temperature variation,
- Operating frequency
- Area of resistance
- There are many others resistors : RWA, PHVPP,RHVNP etc

# Passive devices
## Capacitance

- **Capacitance types**
  - Area - Area ∝ area ($W \times L$), 1/distance ($1/d_2$)
  - Fringe - Area ∝ length ($L$), 1/distance ($1/d_2$)
  - Fringe - Fringe ∝ length ($L$), 1/distance ($1/d_1$)

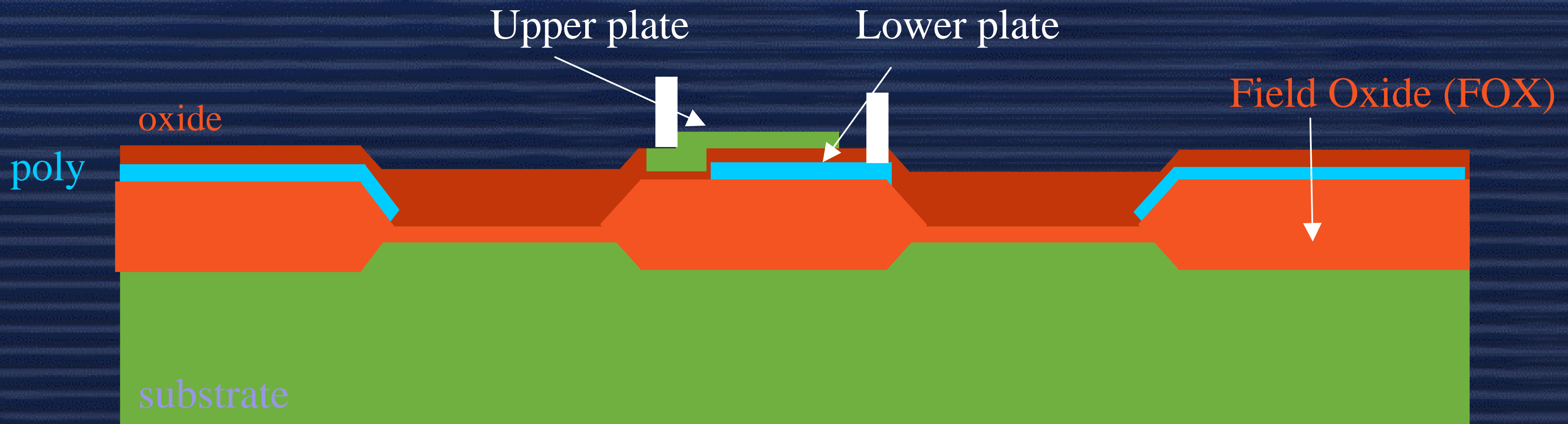


# Passive devices

## Capacitance (*cont'd*)

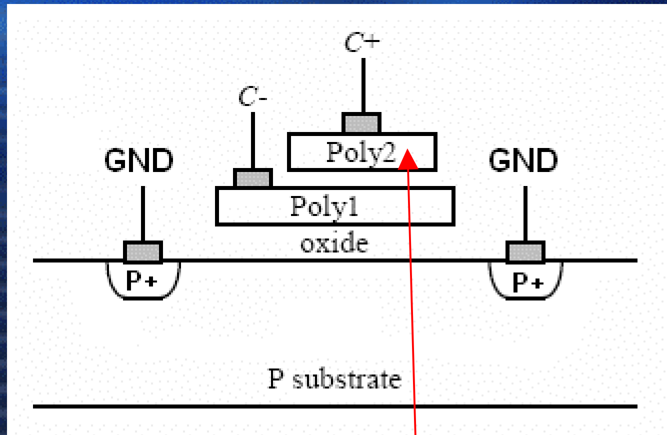
Capacitor:

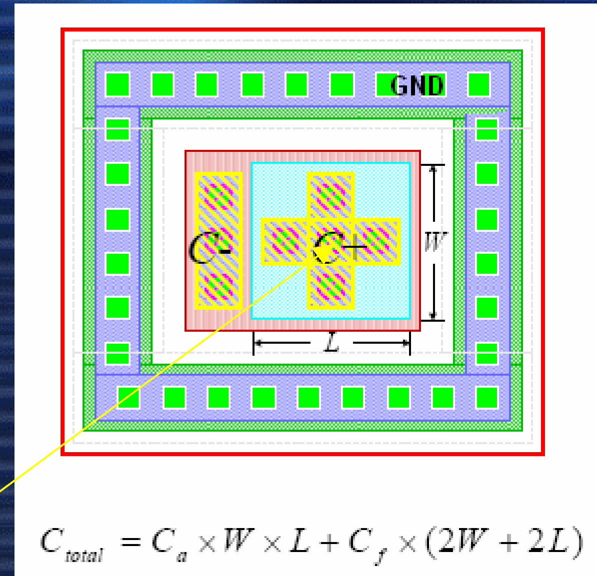
CPP (over the substrate) : $0.86 \times 10^{-3}$ F/m$^2$



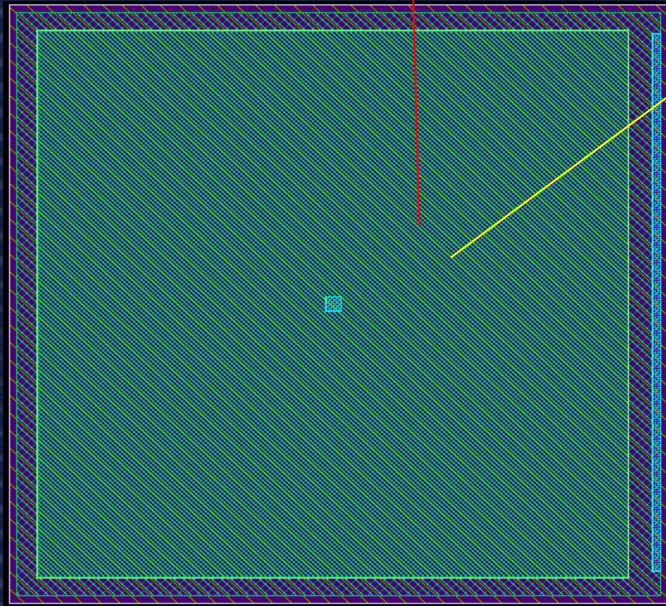
# Passive devices

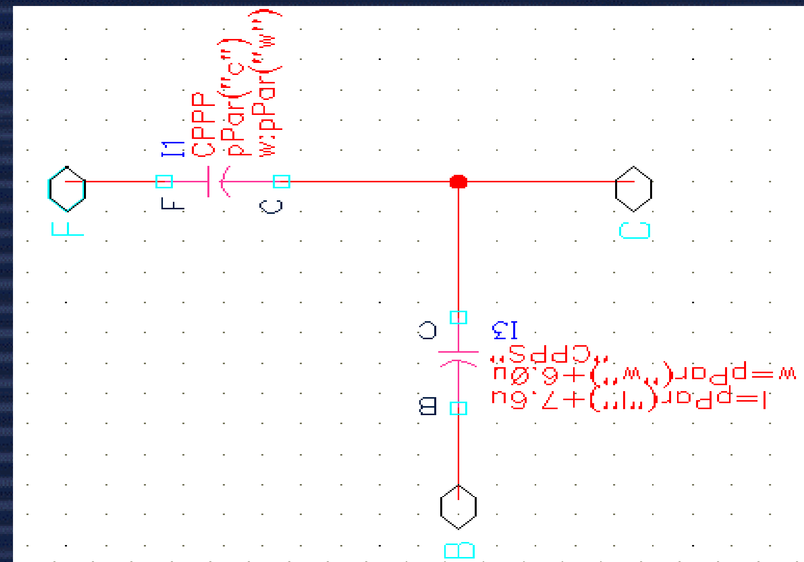
## Capacitance (*cont'd*)




$C_a$ =0.8629e-3 $C_f$ = 0.8629e-3 (F/m^2)



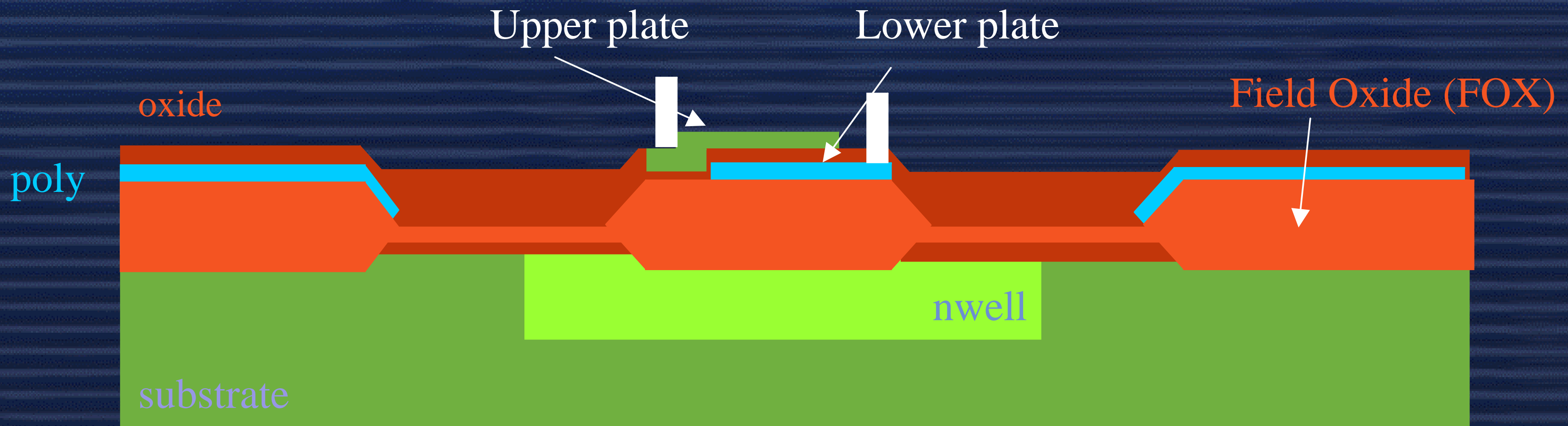


# Passive devices

## Capacitance (*cont'd*)

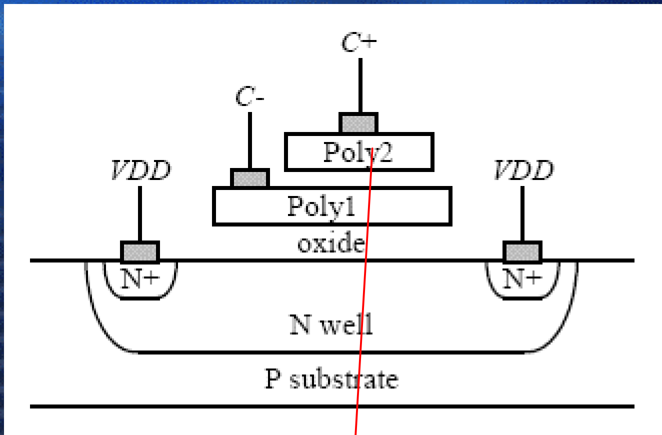
Capacitor:

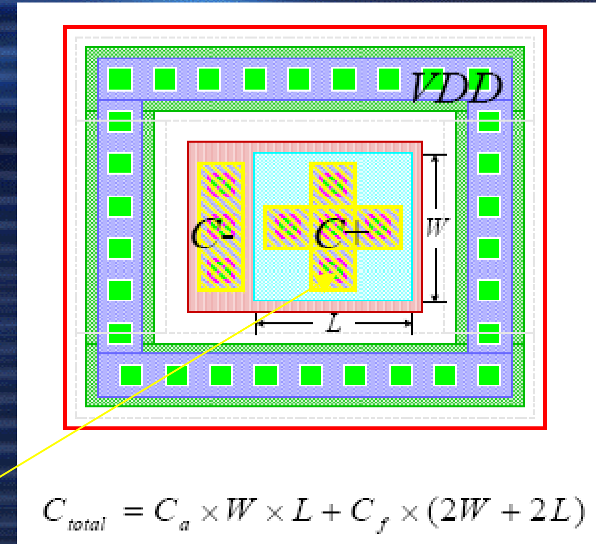
CPP (over the Nwell) : $0.86*10^{-3}$ F/m$^2$



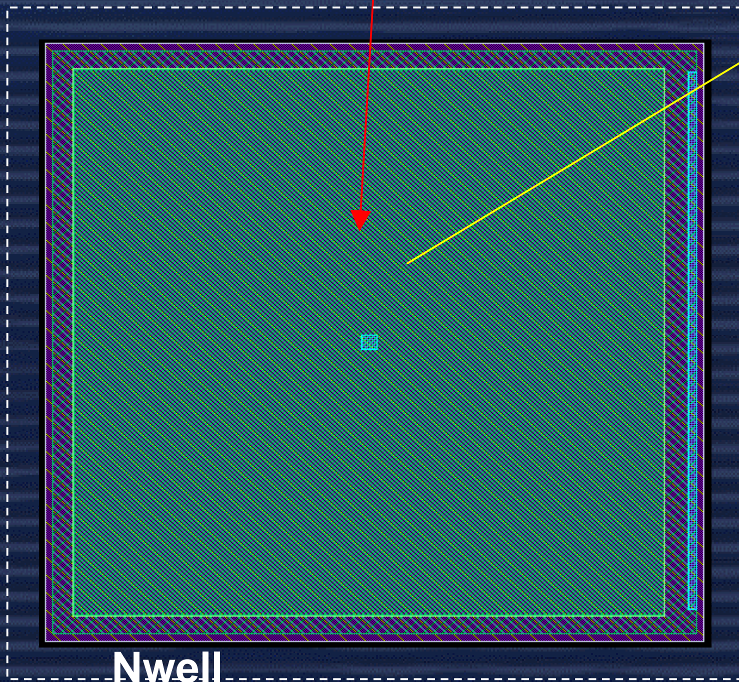
# Passive devices

## Capacitance (*cont'd*)

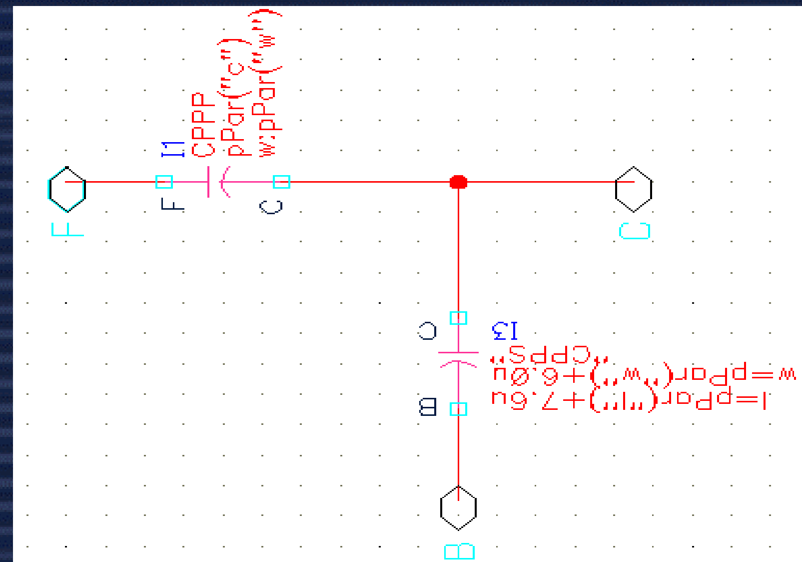



$$C_{total} = C_a \times W \times L + C_f \times (2W + 2L)$$




$C_a$ =0.8629e-3 $C_f$ = 0.8629e-3 (F/m^2)

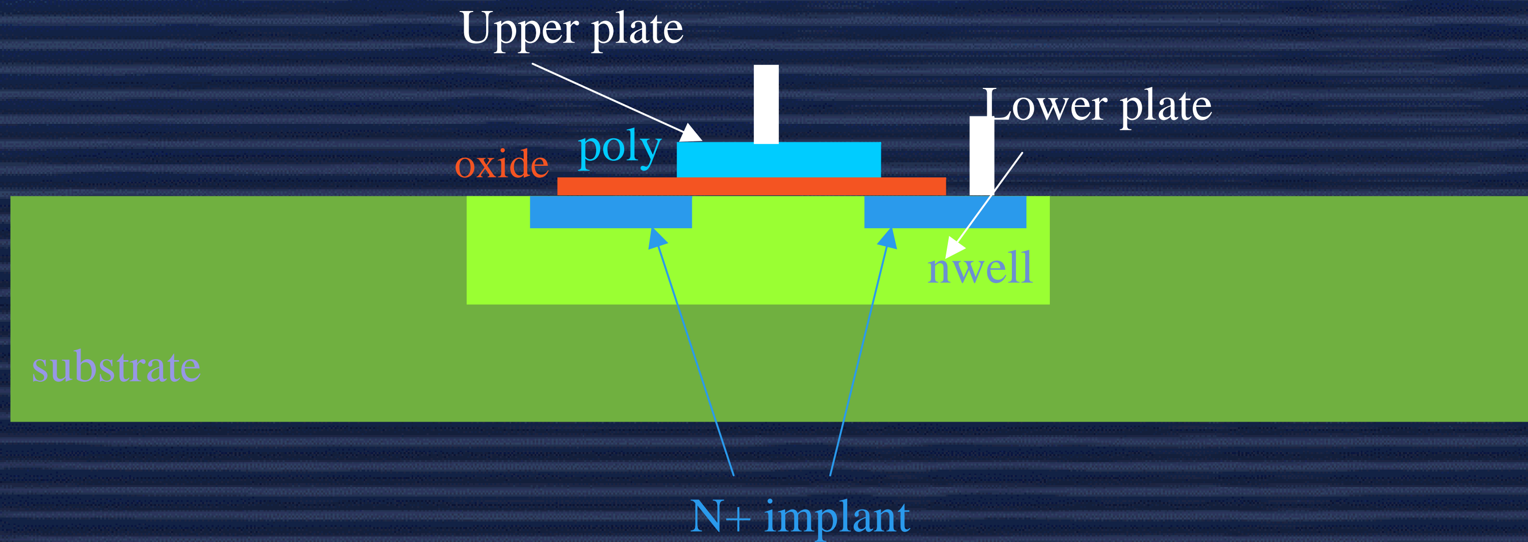


# Passive devices

## Capacitance (*cont'd*)

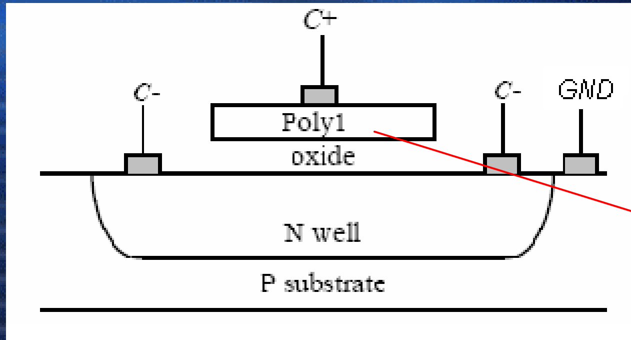
Capacitor:

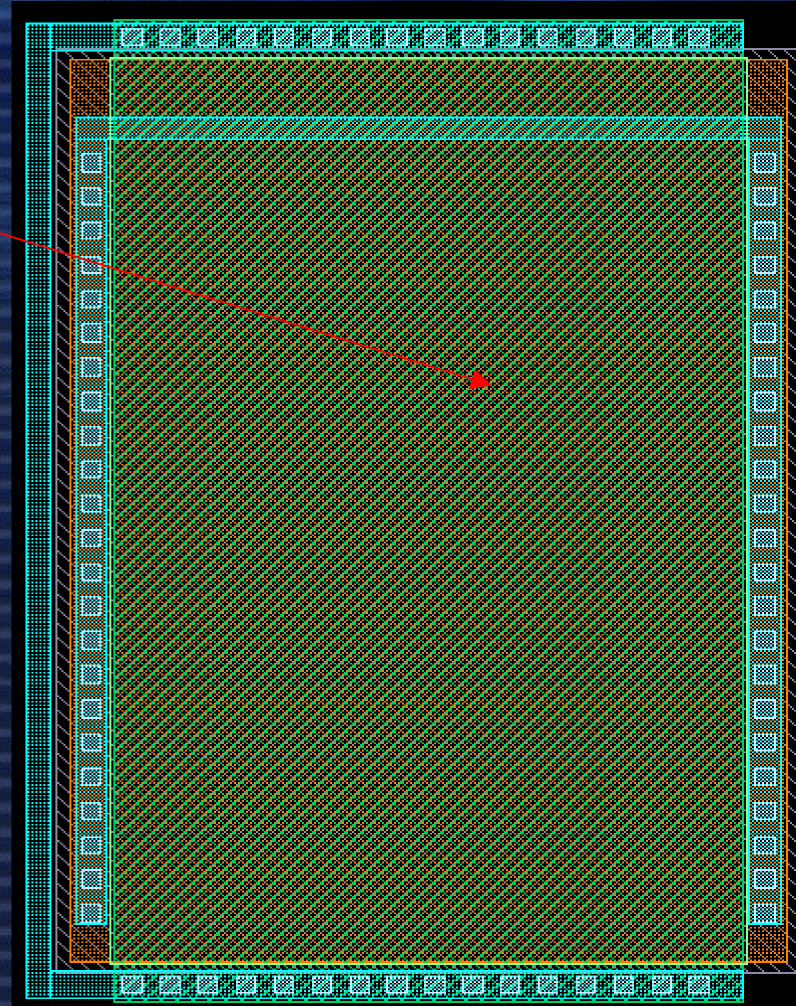
Accumulation capacitor : $6.166*10^{-3}$ F/m$^2$

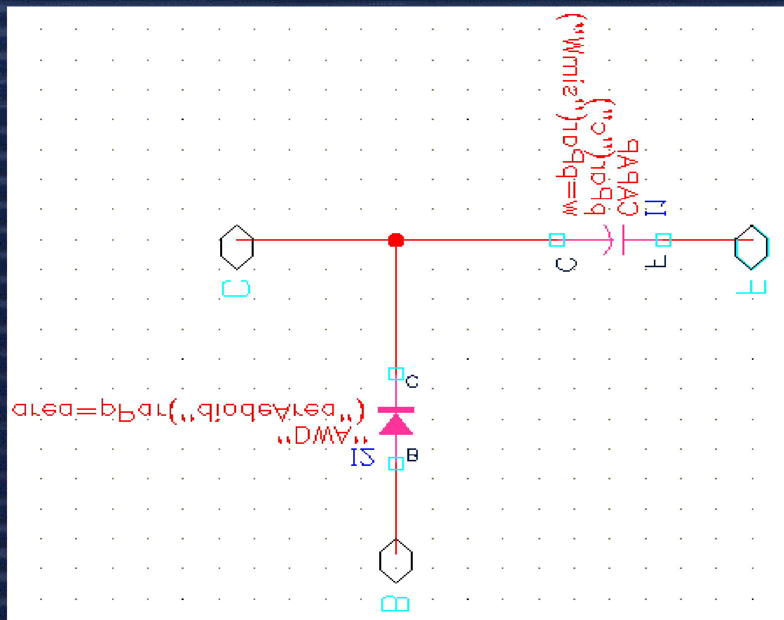


# Passive devices

## Capacitance (*cont'd*)





There are many others capacitors :COMB cap, Interdigtized Cap, MOS Varactor cap

# Passive devices

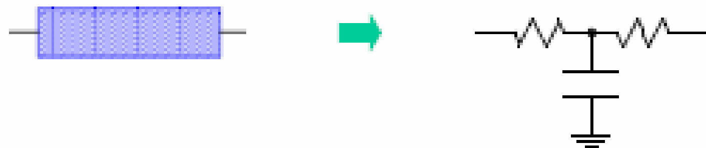
## Capacitance (*cont'd*)

Capacitor:

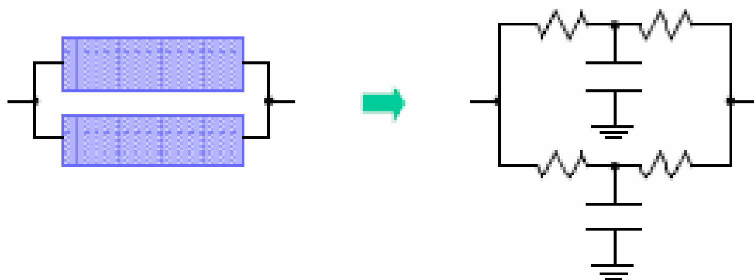
- Good matching accuracy
- Low voltage coefficient
- Less parasitic capacitance
- High capacitance per area
- Low temp. coefficient

# Interconnection

- **CMOS static logic**
  - Only consider *RC* delay
  - ➡ **Use minimum metal width**



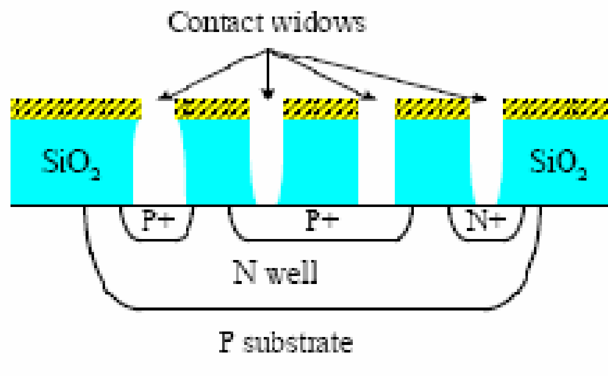
||| *RC* constant

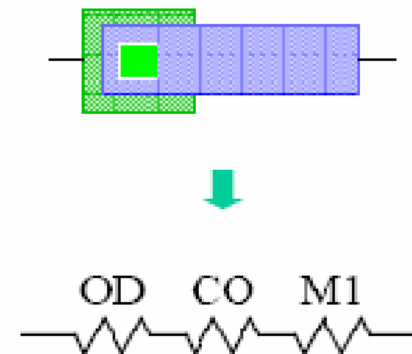


- **Analog circuits**
  - Metal width is decided by
    - **Current density**
      - Ex: 1 mA/μm for M1
    - **Parasitic resistance**
      - Ex: M1 < 0.13 Ω/square
    - **Parasitic capacitance**
      - Ex: M1-Sub (0.4 μm width) ~ 0.073 fF/μm

# Interconnection (*cont'd*)

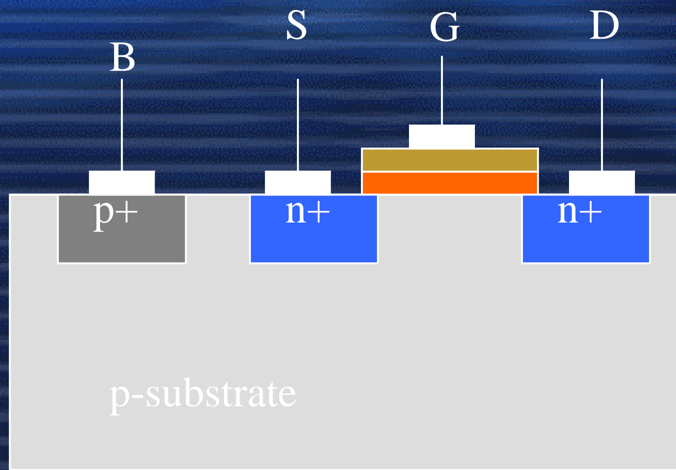
- **CMOS static logic**
  - Contact/Via resistance is minor effect in *RC* delay
  - **➡ One contact/via can be used.**
- **Analog circuits**
  - Contact/Via resistance may degrade circuit performance
  - **➡ At least two contact/via**
  - Current density
    - Ex: 0.6 mA/via for VIA12

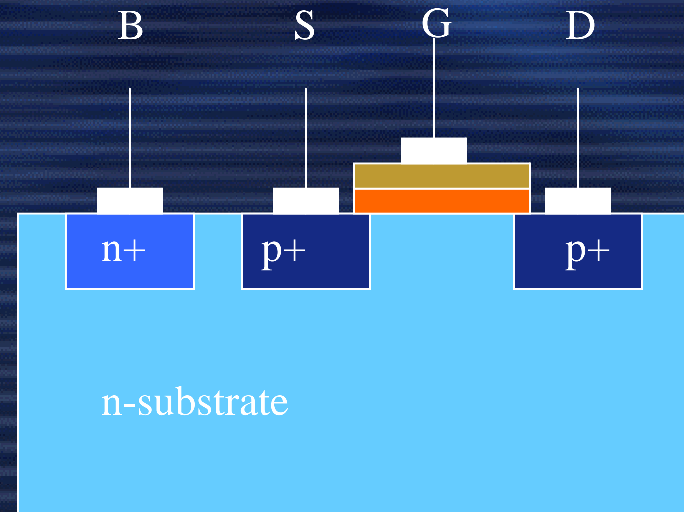


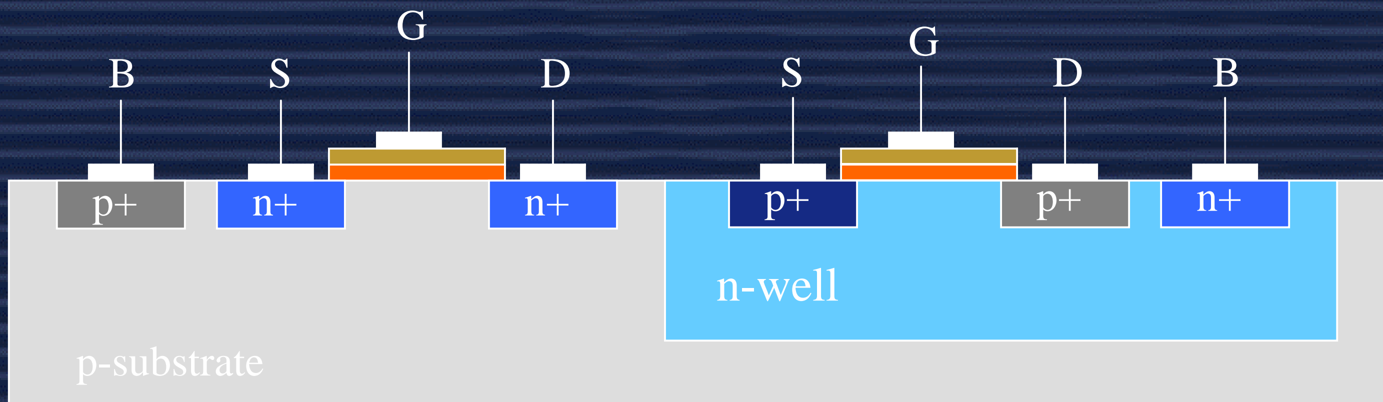




One Via resistance = 4- 5 ohm

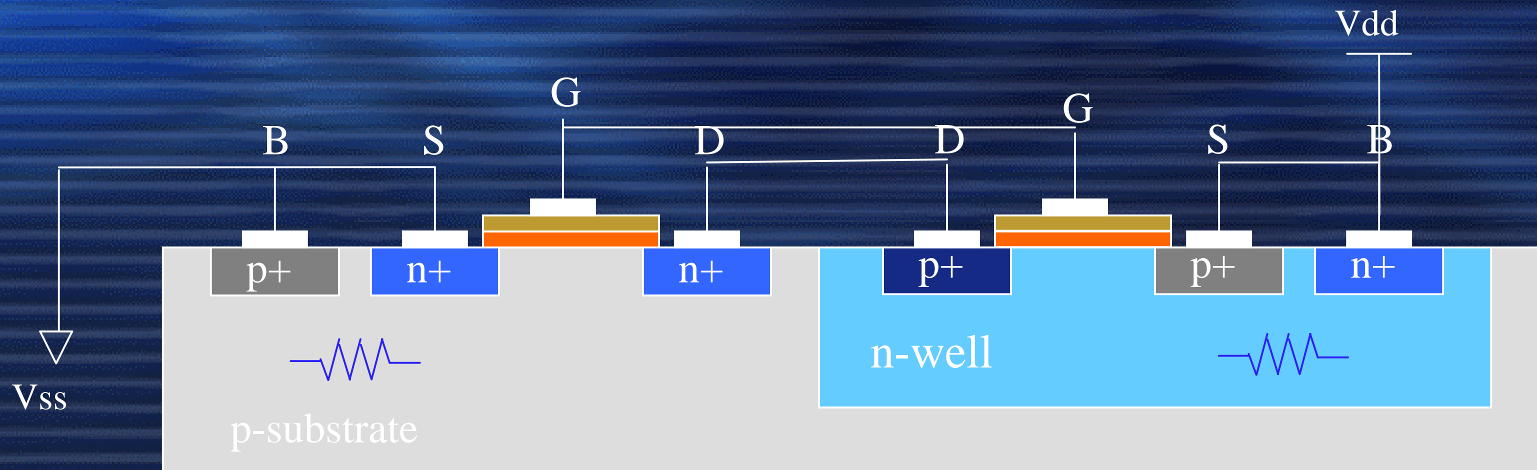
# NMOS & PMOS (CMOS) on same substrate

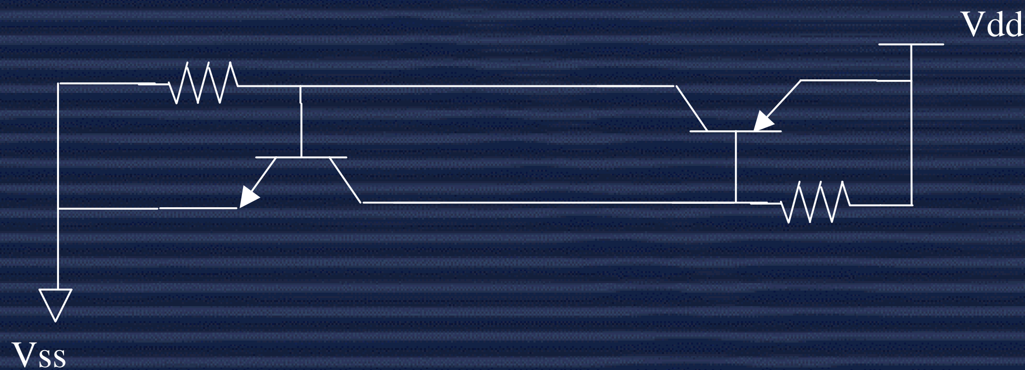


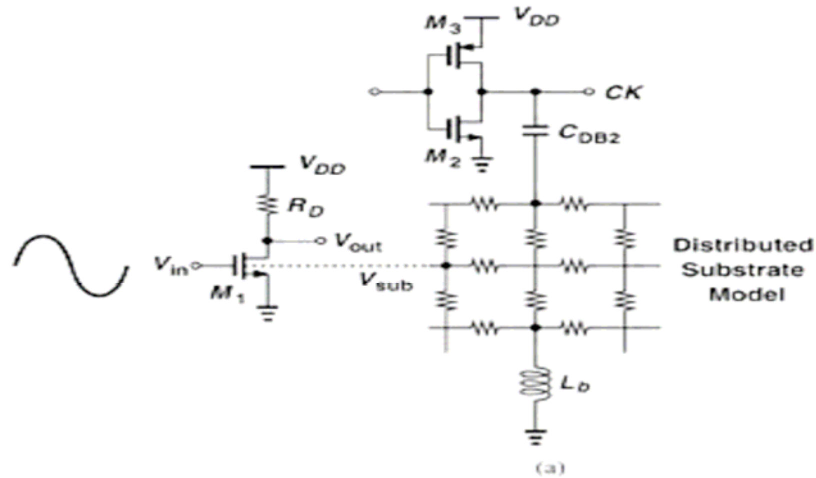
# Latch up problem



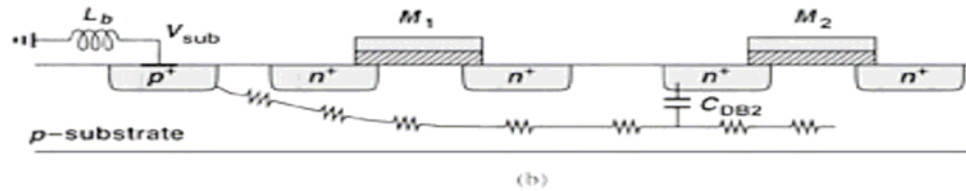




**Permanent current flow between Vdd and Vss**

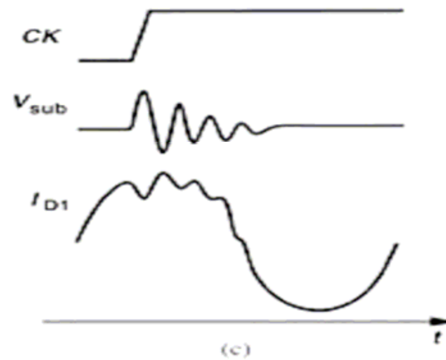
# Substrate Coupling




(a)

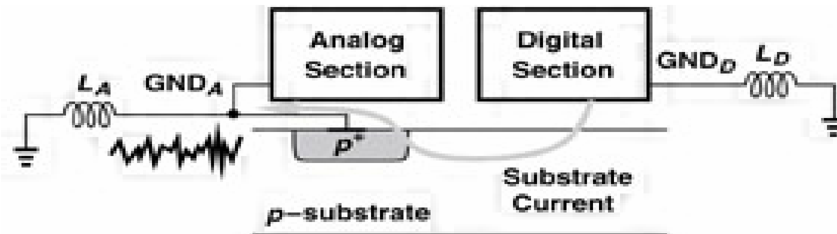



(b)

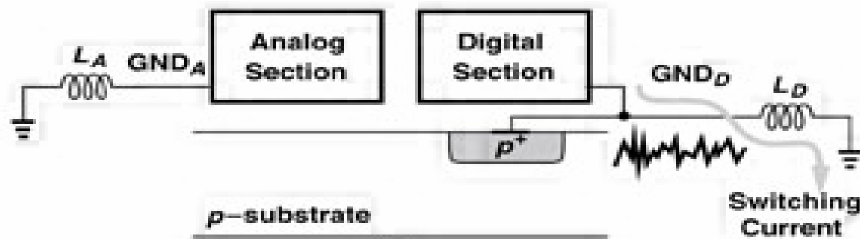



(c)

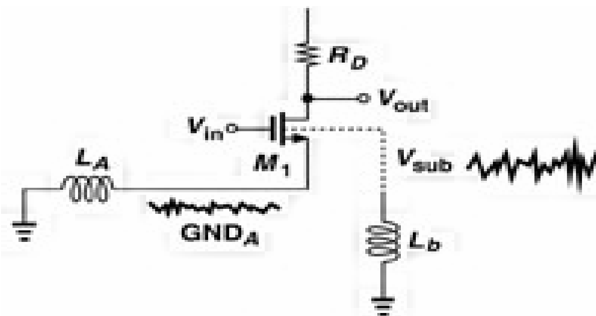
# Substrate Coupling



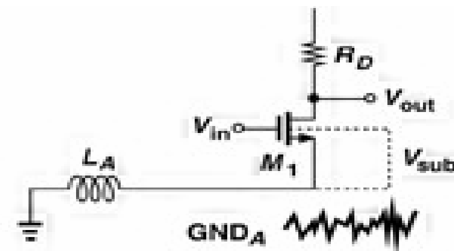
(a)



(b)

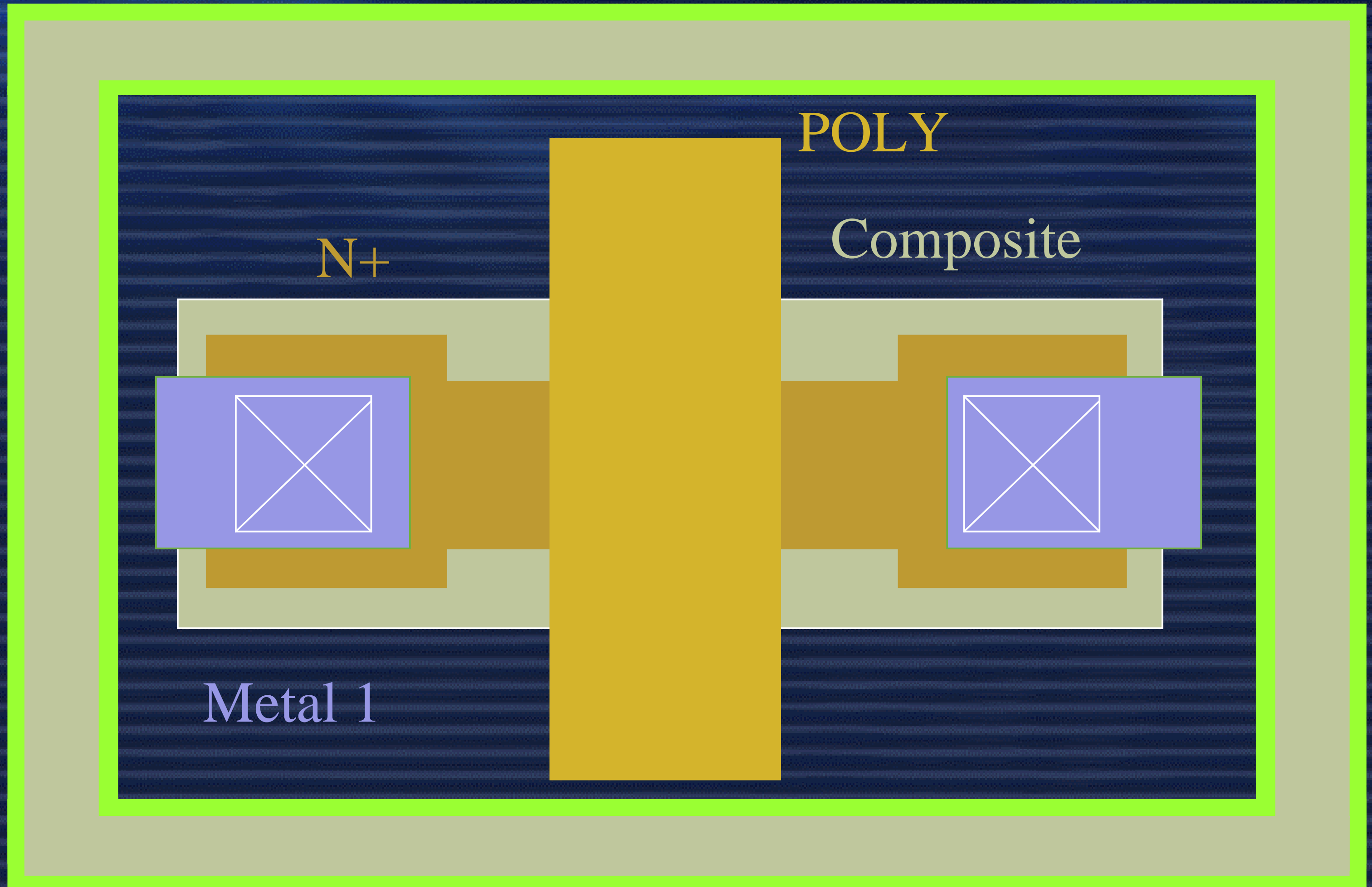


(a)



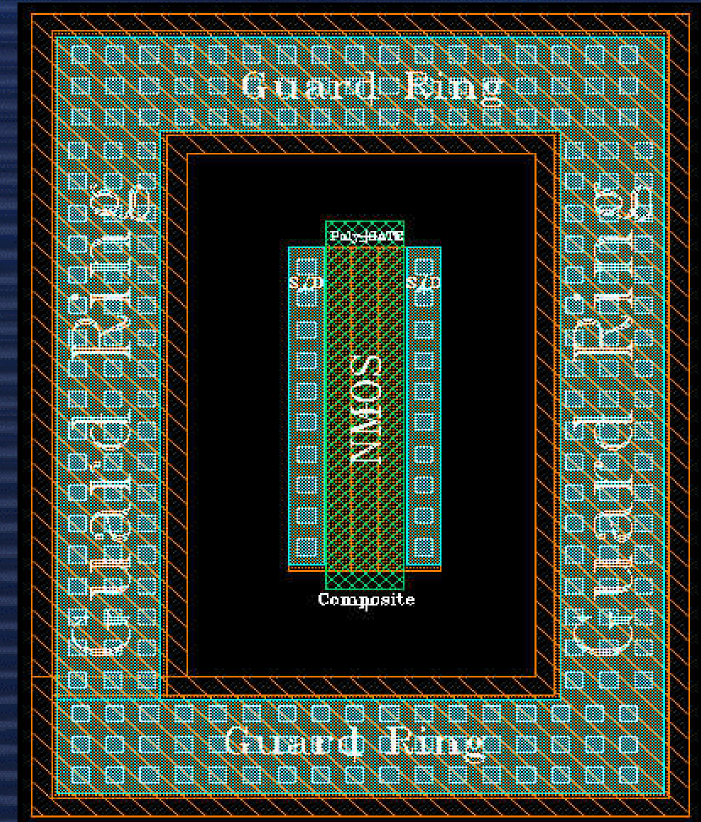
(b)

# Guard ring



# Guard ring and Substrate Contact

- Many MOSs may in a single ring.
- The purpose of the ring is to bias the bulk also.
- It removes the latch up problem also.
- It is used around the passive devices also.
- It reduces the interference from the adjacent blocks.
- Width of the ring should not be bigger than a limit to ensure proper biasing.



# Proper ground connection

- All the modules of the chip should be properly grounded.
- Use star ground.
- Ground metal should be wider.
- Vdd metal should also be wider.
- Try to avoid same Vdd line for a noisy and sensitive blocks.
- Use different pins for the noisy and sensitive blocks.

# Star Ground

# Things to remember

- Keep sufficient spacing between power blocks and sensitive blocks.
- Two high frequency carrying pins should not be side by side.
- Use ground pin to avoid magnetic coupling between two pins.

# Matching of the devices

# Why Special attention on Matching ?

- A large variety of analog circuits rely on matching of transistors. Circuits like differential pair rely on gate to source voltage matching while current mirrors rely on current matching.

- Most integrated resistors and capacitors have a tolerance of about 20% to 30%. But ratio of two similar components can be controlled to a tolerance of 15 or even 0.1% by proper matching of the components.

# Reasons of Mismatch

Mismatch in integrated circuits are generally of two types :

- Random mismatches due to microscopic fluctuations in dimensions, doping, oxide thickness and other parameters that influence component values.

- Systematic mismatches which are caused by :

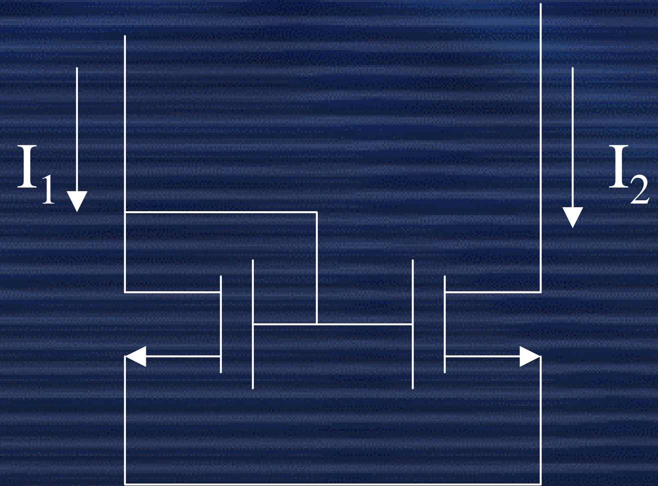
- Process biases
- Mechanical stress
- Temperature gradients
- Polysilicon etch rates etc.

# How does mismatch affect the performance of the circuit ?

❖ Current Mirror

$$I_1 = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_1 (V_{GS} - V_{t1})^2$$

$$I_2 = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_2 (V_{GS} - V_{t2})^2$$




Defining average and mismatch quantities, we have

$$I = (I_1 + I_2)/2 , \quad \Delta I = I_1 - I_2 , \quad W/L = [(W/L)_1 + (W/L)_2]/2$$

$$V_t = (V_{t1} + V_{t2})/2 , \quad \Delta V_t = V_{t1} - V_{t2}$$

# How does mismatch affect the performance of the circuit ? (*cont'd*)

Substituting these expressions and neglecting higher order terms we obtain :

$$\frac{\Delta I}{I} = \frac{\Delta(W/L)}{W/L} - \frac{\Delta V_t}{(V_{GS} - V_t)/2}$$

Thus from the above equation we can see that the mismatch in the current depend upon

1) Mismatch in the (W/L) values of the transistors.
2) Mismatch in the threshold values of the transistors which increases as the overdrive voltage ( $V_{GS}$-$V_t$) is reduced.

# Input Offset voltage of a differential pair

$$V_{OS} = \Delta V_t + \frac{(V_{GS} - V_t)}{2} \left[ \frac{-\Delta R_L}{R_L} - \frac{\Delta(W/L)}{W/L} \right]$$

Thus we see that the offset voltage depends upon two parameters :

- The first component is the threshold voltage mismatch of the transistors . This depends upon the layout and it can be reduced by careful layout.
- The second component of the offset scales with the overdrive voltage and is related to mismatch in the load elements and mismatch in the W/L values.

# Rules for MOS transistor matching

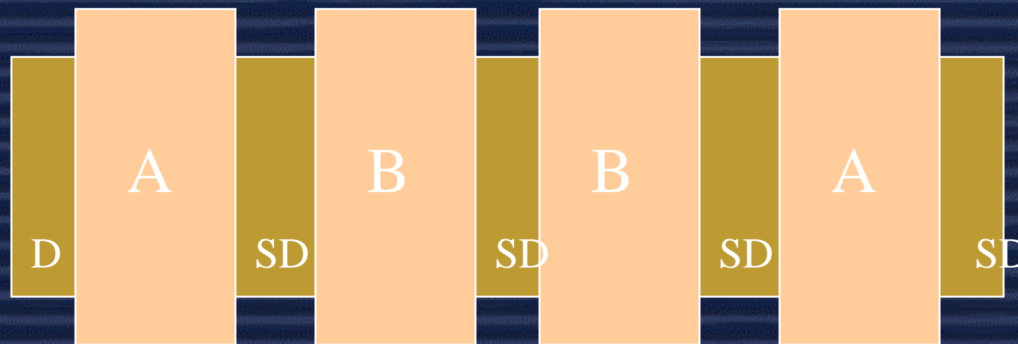
- Place transistors in close proximity.
- Orient transistors in the same direction.
- Keep the layout of the transistors as compact as possible
- Whenever possible use Common centroid layouts.
- Place transistors segments in the areas of low stress gradients.
- Place transistors well away from the power devices.
- For current matching keep overdrive voltage large.
- For voltage matching keep overdrive voltage smaller.

# Rules for resistor and capacitor matching

- Construct matched resistors of same type.
- Make matched resistors of the same width.
- Orient matched resistors in the same direction.
- Place matched resistors in close proximity.
- Place the matched resistors in such a way that their centroids coincide i.e. interdigitate arrayed resistors.
- Place dummies on either end of the resistor array.
- Connect matched resistors to cancel thermoelectric effects.

# Common Centroid Layout

- Gradient-induced mismatches can be minimized by reducing the distance between the centroids of the matched devices. The layouts which actually reduce the distance between centroids of the matched pair to zero are called common centroid layouts.




Common Centroid Layout of two MOS

# Common Centroid Layout (*cont'd*)

- Interdigitation can also be done in 2 dimensions

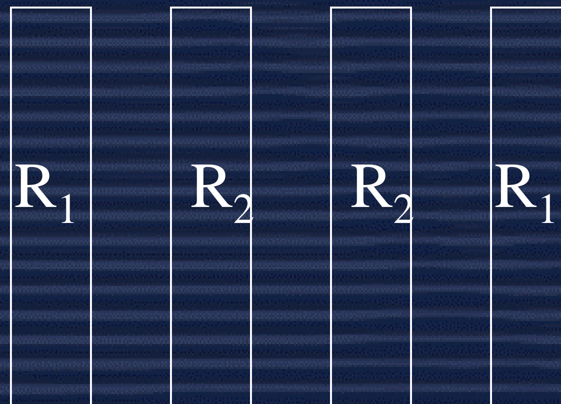
$_{D}A_{SD}B_{S}$

$_{D}B_{SD}A_{S}$

$_{D}A_{SD}B_{SD}B_{SD}A_{S}$

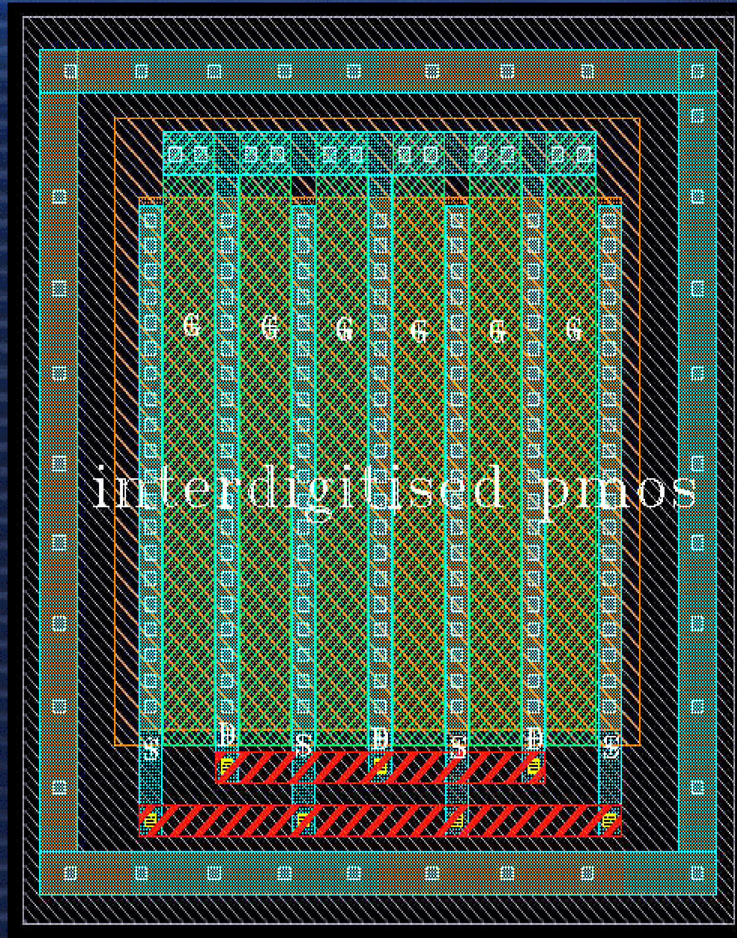
$_{D}B_{SD}A_{SD}A_{SD}B_{S}$

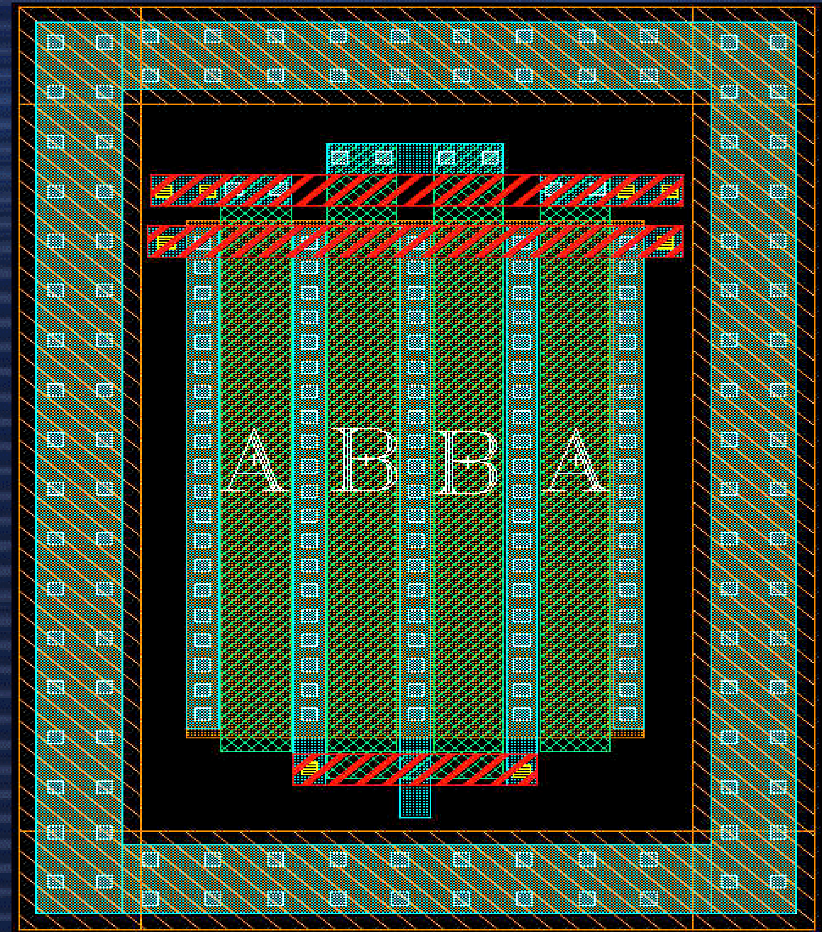
Common Centroid Layout for Resistors



# Layout of Matched Resistors

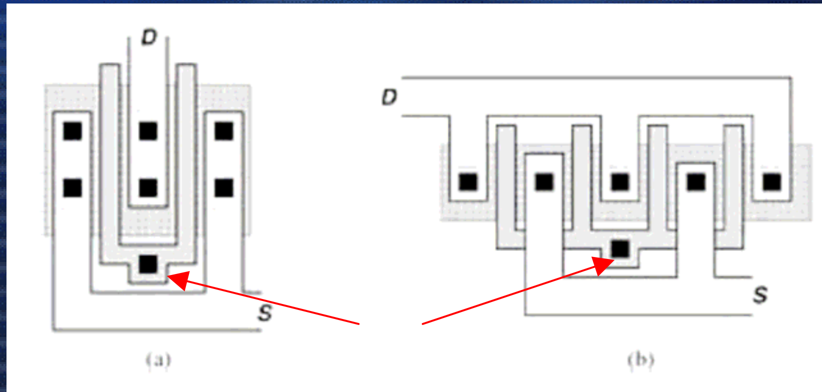
# Fingering of MOS and Common-centroid Layout example



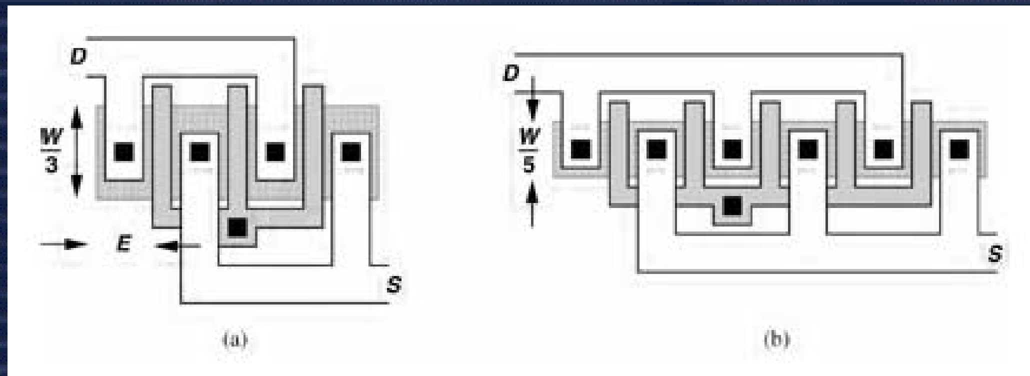
# Layout of Multi-finger Transistors

## *Fingering*




**Reduces gate resistance.**
**Improves noise and delay**

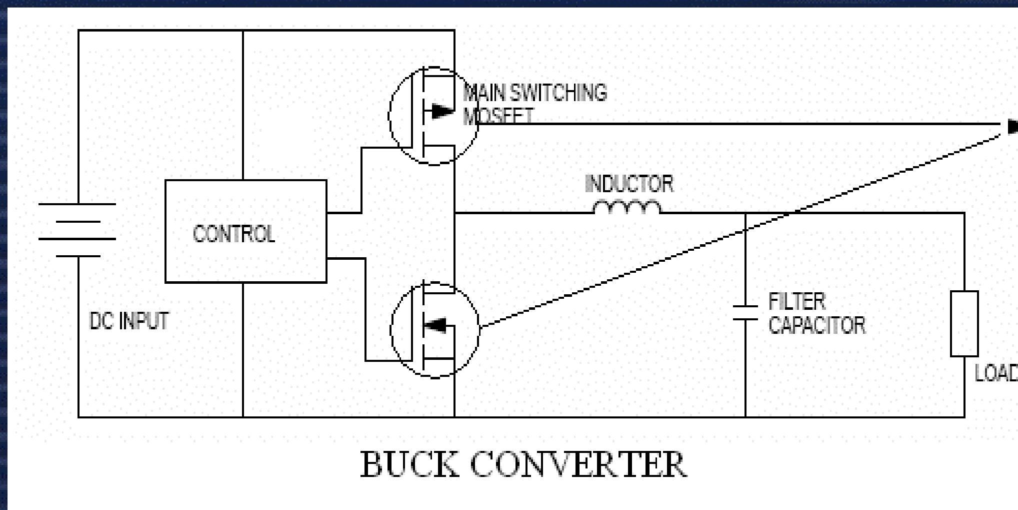
## *Drawback of Fingering*

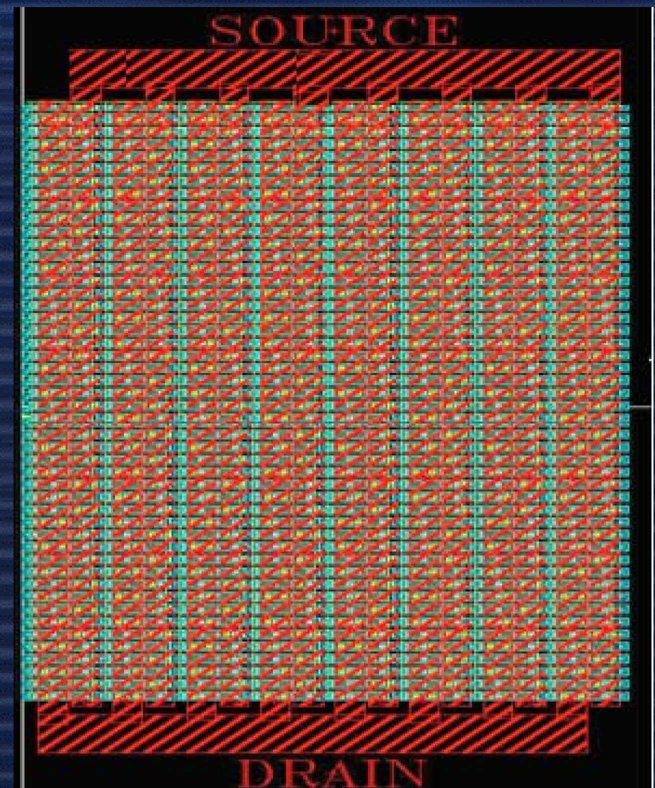



**Increases drain and source side-wall capacitance.**

# Example of MOS Layout with fingers

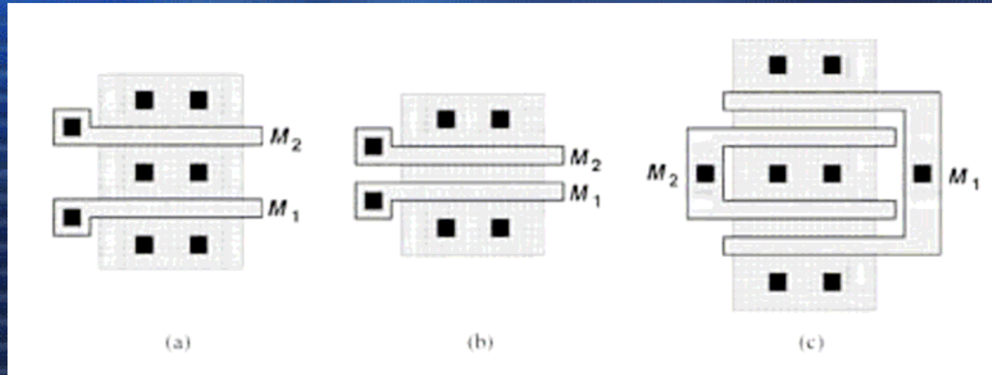
- Power MOSFET layout with large W/L ratio (in the order of $10^5$-$10^6$)



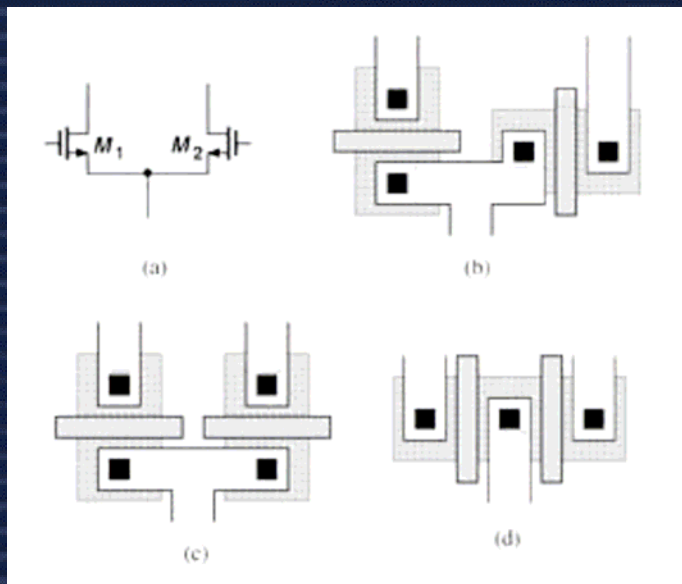



# Layout of Standard blocks

## *Cascode Transistors*

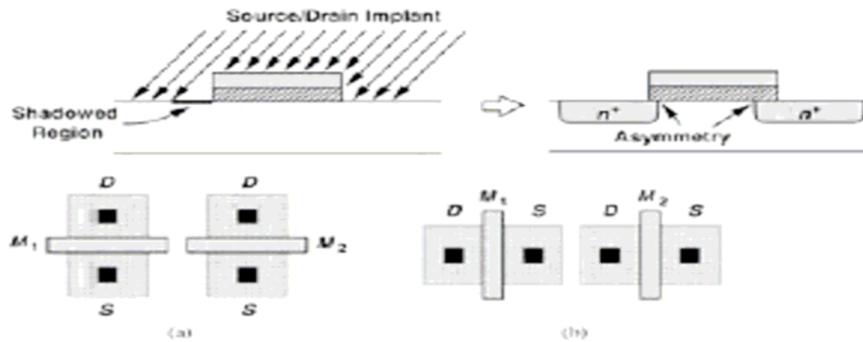



## *Differential Pair*



# Layout of Standard blocks (*cont'd*)

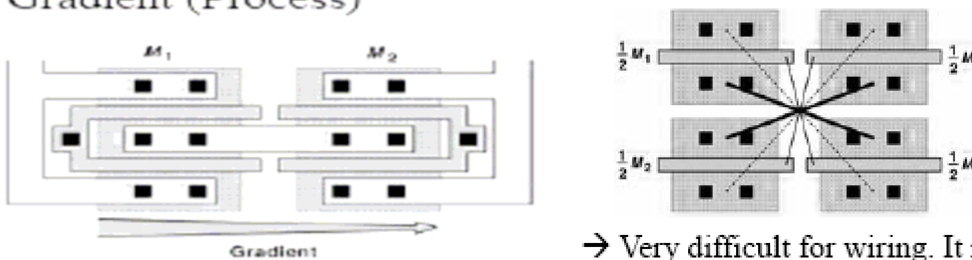
Shadowing effect




Dummy (To provide very symmetric environment)

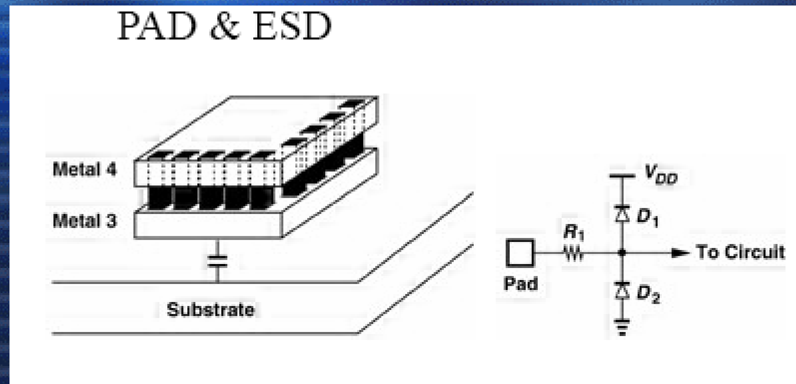
High frequency asymmetric due to the crossover of the wire

Gradient (Process)

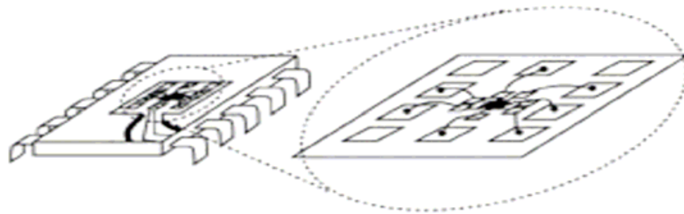



→ Very difficult for wiring. It may introduce high-frequency

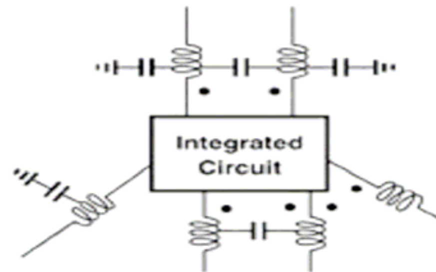
# PAD, PIN & PACKAGE




**Package**



(a)




(b)

**Pad cap ~80f-2pF**

**Bondwire Inductor=1nH/mm**

**Pin Inductor=1-2nH**

**Pin Cap=300fF**

Thank You