Lecture 12: MOS Transistor Models

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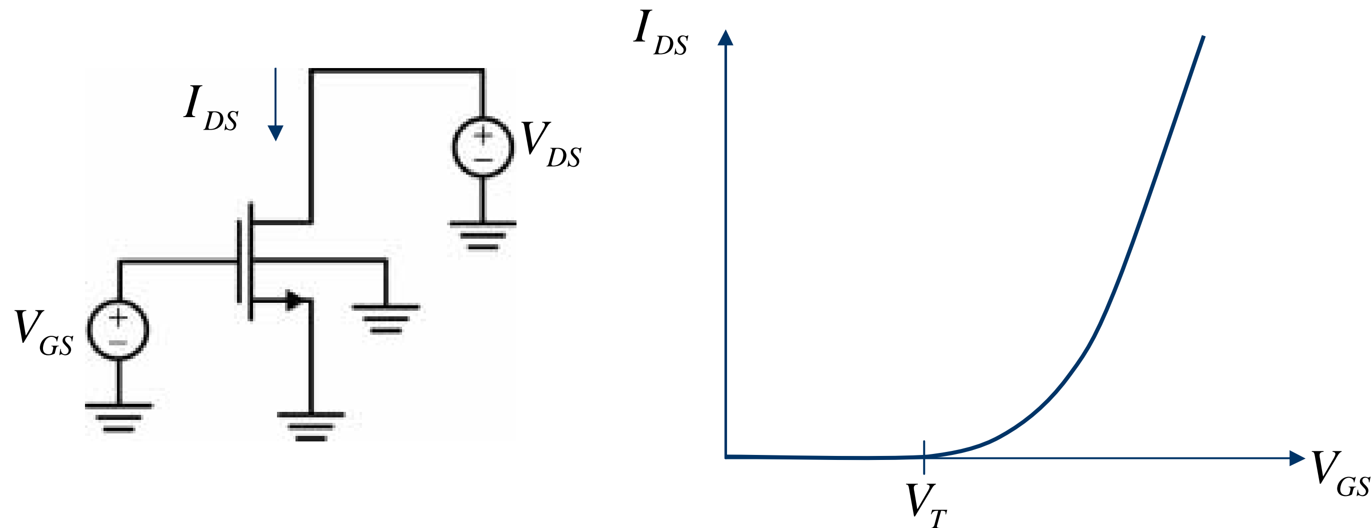
Lecture Outline

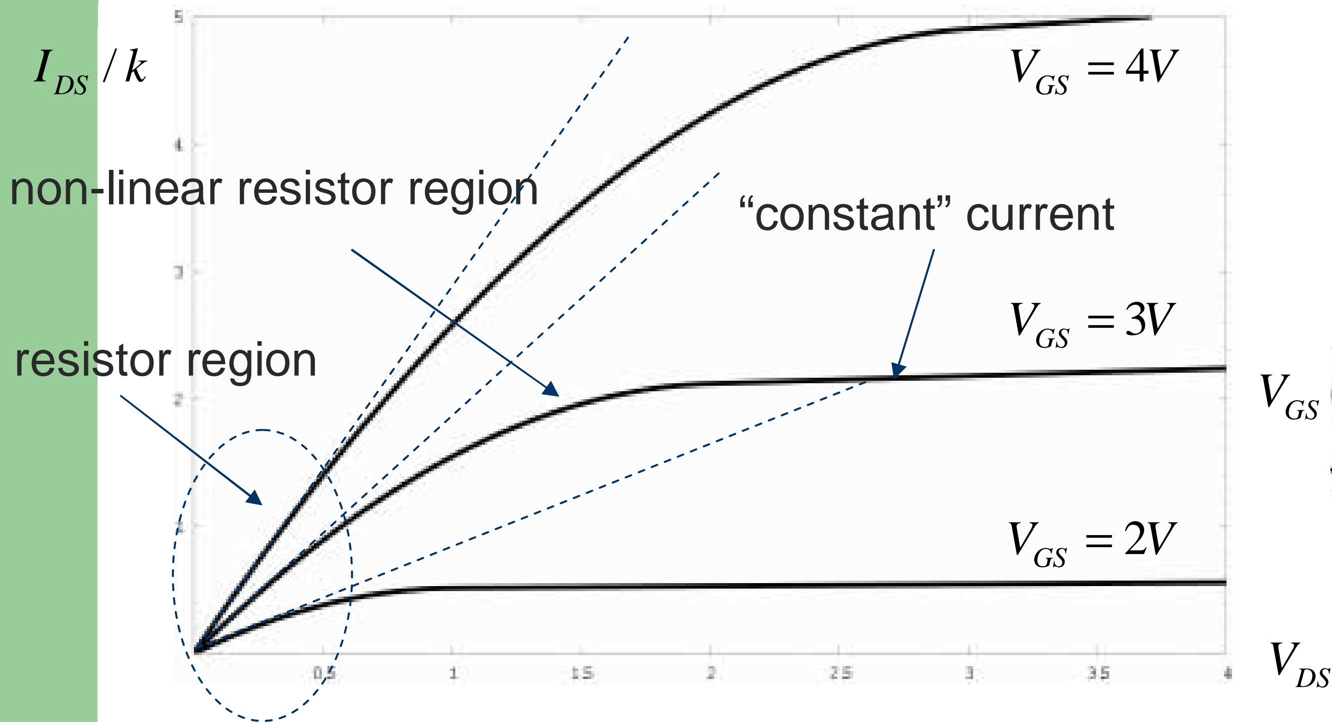
- MOS Transistors (4.3 – 4.6)
  - I-V curve (Square-Law Model)
  - Small Signal Model (Linear Model)

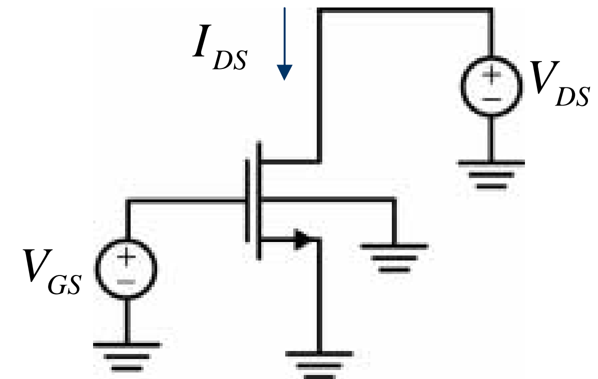
Observed Behavior: I_D-V_{GS}



- Current zero for negative gate voltage
- Current in transistor is very low until the gate voltage crosses the threshold voltage of device (same threshold voltage as MOS capacitor)
- Current increases rapidly at first and then it finally reaches a point where it simply increases linearly

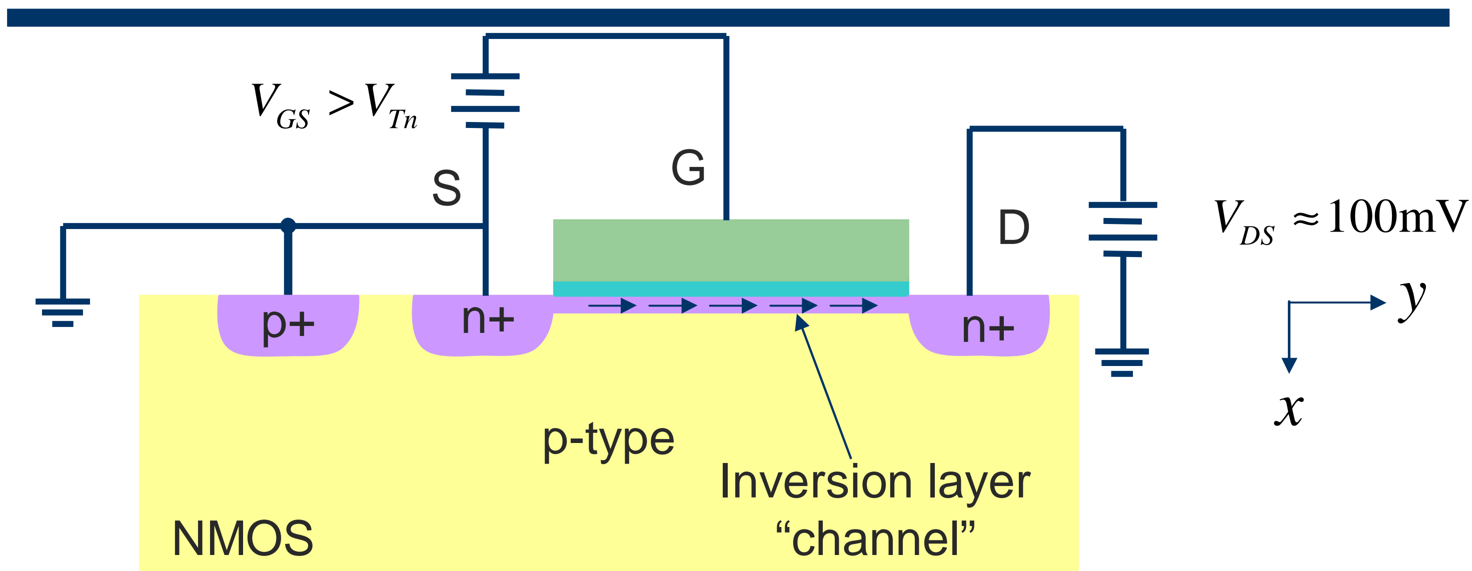
Observed Behavior: I_D-V_{DS}





- For low values of drain voltage, the device is like a resistor
- As the voltage is increases, the resistance behaves non-linearly and the rate of increase of current slows
- Eventually the current stops growing and remains essentially constant (current source)

"Linear" Region Current



- If the gate is biased above threshold, the surface is inverted
- This inverted region forms a channel that connects the drain and gate
- If a drain voltage is applied positive, electrons will flow from source to drain

MOSFET: Variable Resistor

- Notice that in the linear region, the current is proportional to the voltage

$$I_{DS} = \frac{W}{L}\mu_n C_{ox}(V_{GS} - V_{Tn})V_{DS}$$

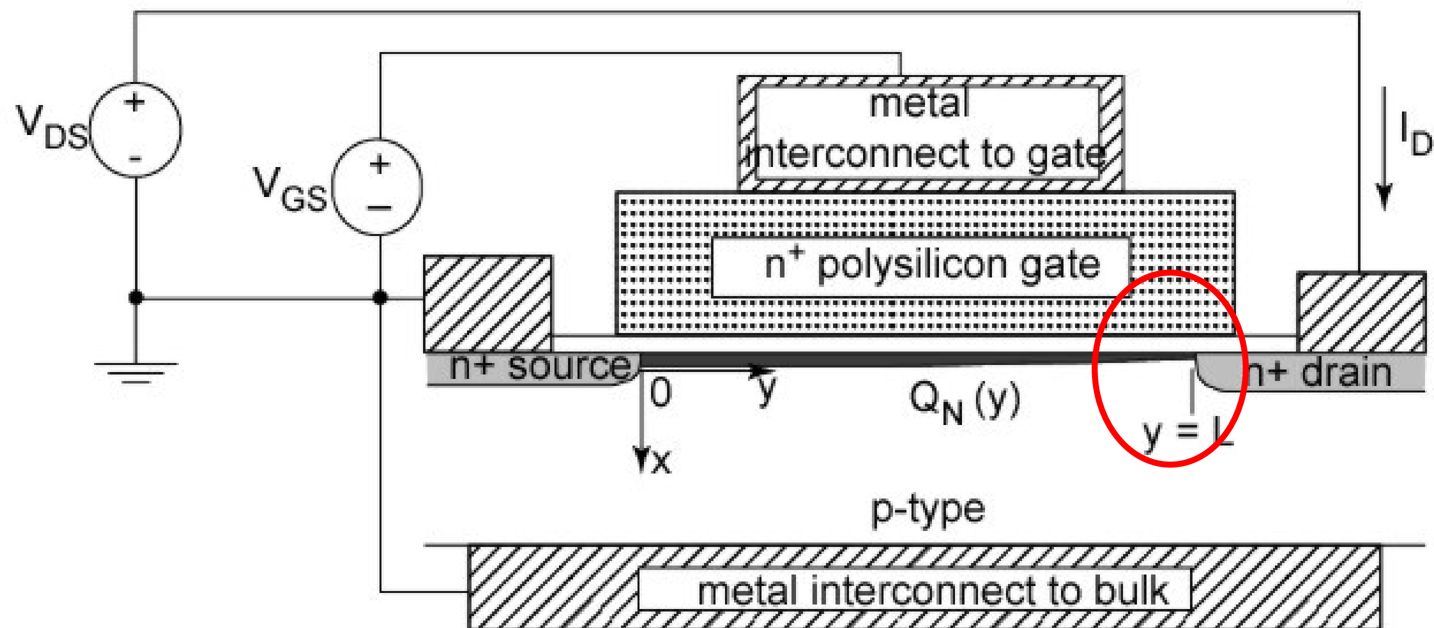
- Can define a voltage-dependent resistor

$$R_{eq} = \frac{V_{DS}}{I_{DS}} = \frac{1}{\mu_n C_{ox}(V_{GS} - V_{Tn})}\left(\frac{L}{W}\right) = R_{\square}(V_{GS})\frac{L}{W}$$

- This is a nice variable resistor, electronically tunable!

Finding $I_D = f(V_{GS}, V_{DS})$

- Approximate inversion charge $Q_N(y)$: drain is higher than the source → less charge at drain end of channel



Inversion Charge at Source/Drain

$$Q_N(y) \approx Q_N(y=0) + Q_N(y=L)$$

$$Q_N(y=0) = -C_{ox}(V_{GS} - V_{Tn})$$

$$Q_N(y=L) = -C_{ox}(V_{GD} - V_{Tn})$$

$$GD = V_{GS} - V_{DS}$$

Average Inversion Charge

Source End Drain End

$$Q_N(y) \approx -\frac{C_{ox}(V_{GS}-V_T)+C_{ox}(V_{GD}-V_T)}{2}$$

$$Q_N(y) \approx -\frac{C_{ox}(V_{GS}-V_T)+C_{ox}(V_{GS}-V_{SD}-V_T)}{2}$$

$$Q_N(y) \approx -\frac{C_{ox}(2V_{GS}-2V_T)-C_{ox}V_{SD}}{2} = -C_{ox}(V_{GS}-V_T-\frac{V_{DS}}{2})$$

- Charge at drain end is lower since field is lower
- Simple approximation: In reality we should integrate the total charge minus the bulk depletion charge across the channel

Drift Velocity and Drain Current

"Long-channel" assumption: use mobility to find v

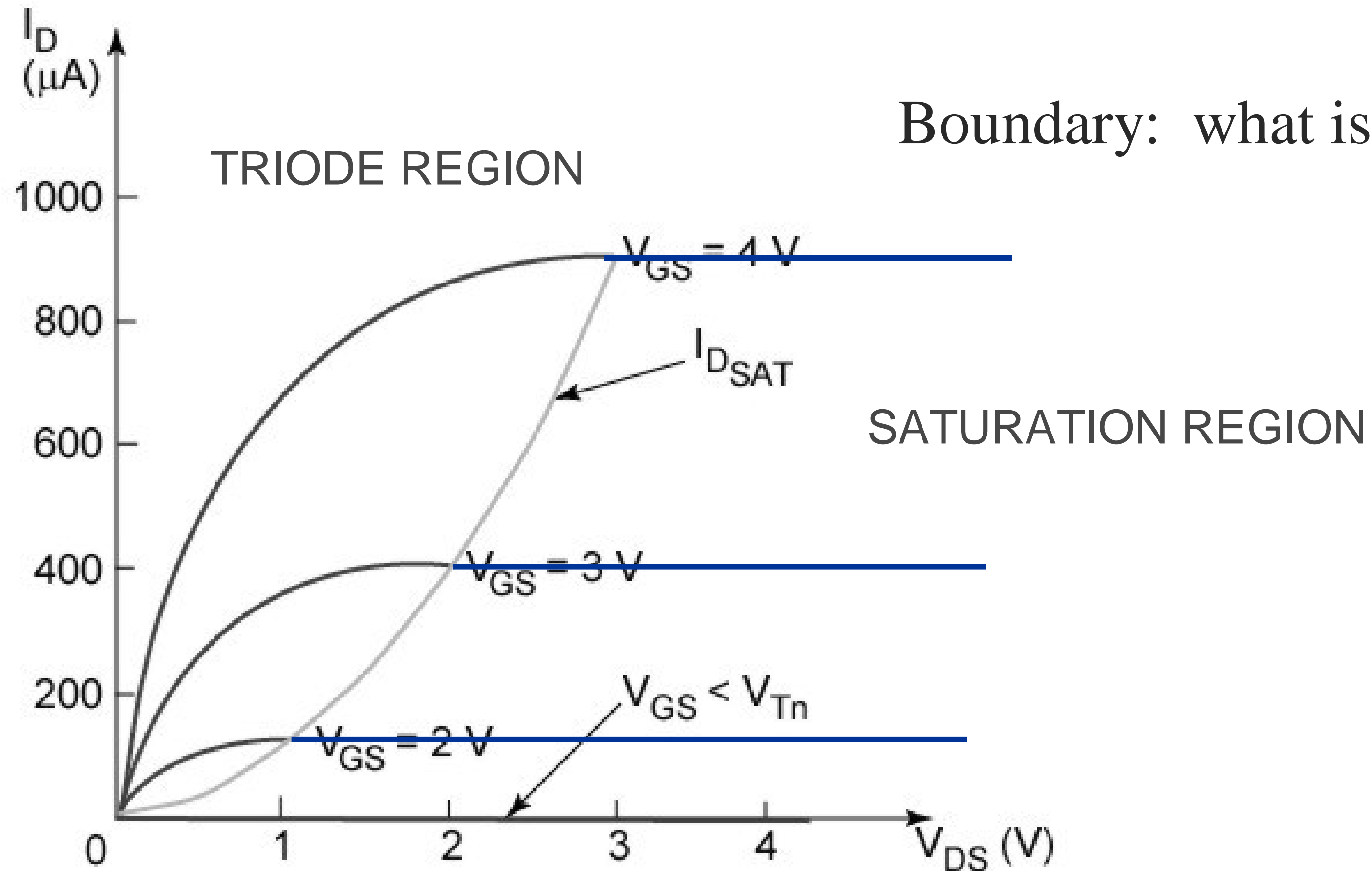
$$v(y) = -\mu_n E(y) \approx -\mu_n(-\Delta V / \Delta y) = \frac{\mu_n V_{DS}}{L}$$

Substituting:

$$I_D = -WvQ_N \approx W\mu \frac{V_{DS}}{L} C_{ox}(V_{GS} - V_T - \frac{V_{DS}}{2})$$

$$I_D \approx \frac{W}{L}\mu C_{ox}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$$

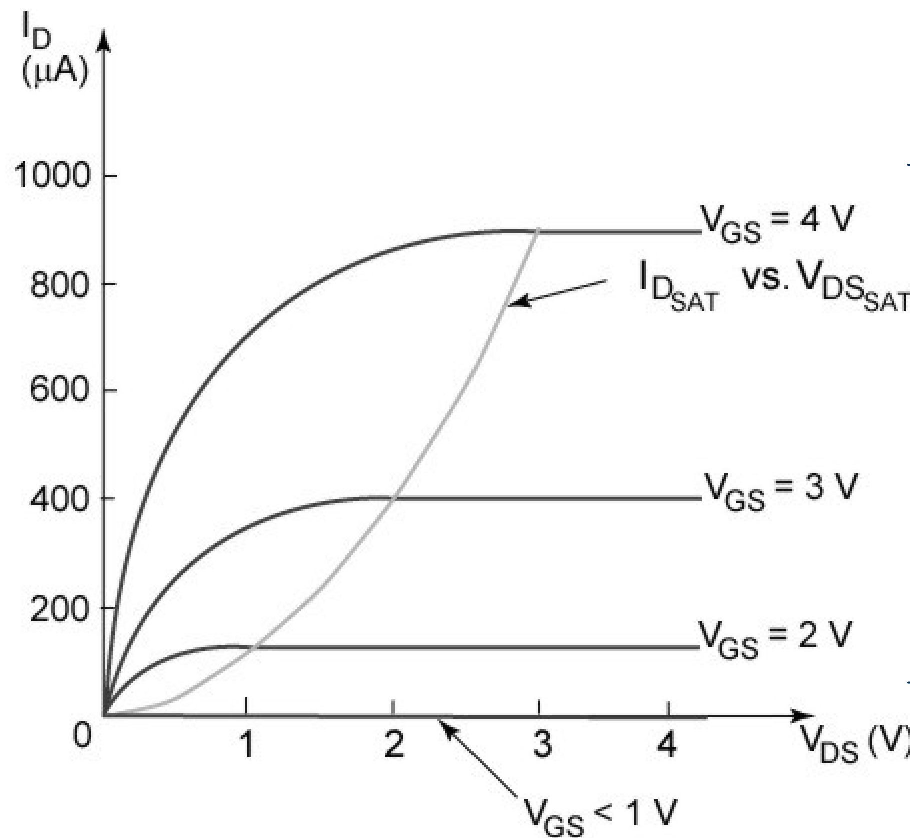
Square-Law Characteristics



Boundary: what is $I_{D,SAT}$?

The Saturation Region

When $V_{DS} > V_{GS} - V_{Tn}$, there isn't any inversion charge at the drain … according to our simplistic model



Why do curves flatten out?

Square-Law Current in Saturation

Current stays at maximum (where $V_{DS} = V_{GS} - V_{Tn} = V_{DS,SAT}$)

$$I_D = \frac{W}{L}\mu C_{ox}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$$

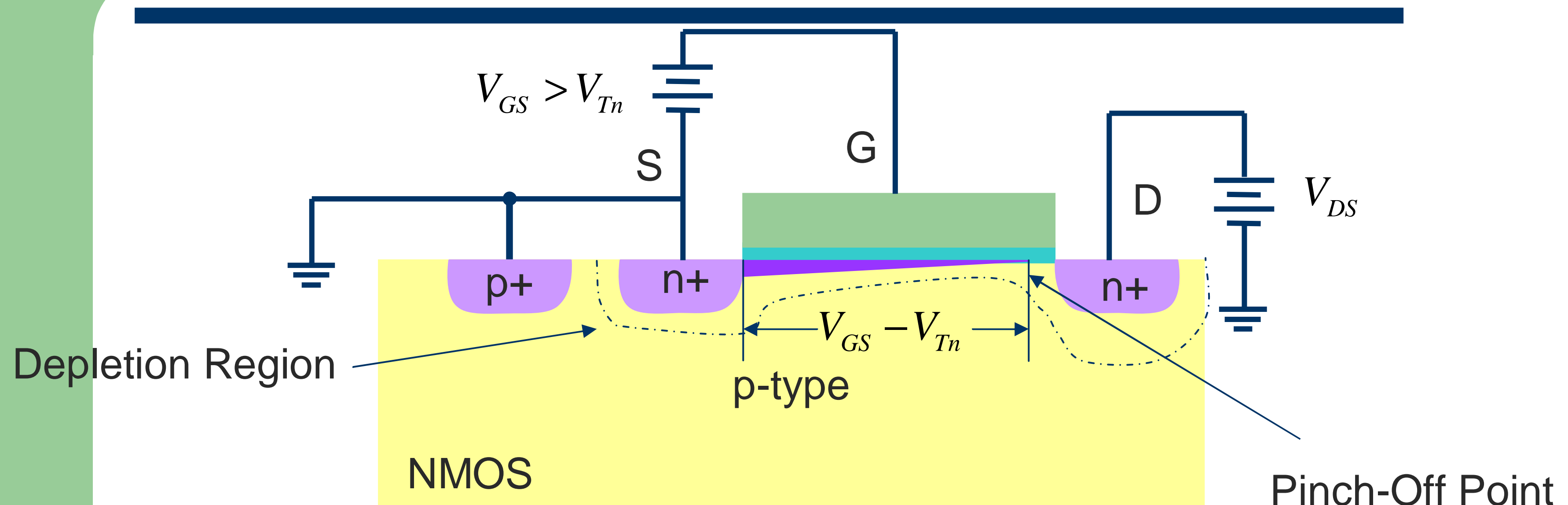
$$I_{DS,sat} = \frac{W}{L}\mu C_{ox}(V_{GS} - V_T - \frac{V_{GS} - V_T}{2})(V_{GS} - V_T)$$

$$I_{DS,sat} = \frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS} - V_T)^2$$

Measurement: I_D increases slightly with increasing V_{DS}
model with linear "fudge factor"

$$I_{DS,sat} = \frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

Pinching the MOS Transistors



- When $V_{DS} > V_{DS,sat}$, the channel is "pinched" off at drain end (hence the name "pinch-off region")
- Drain mobile charge goes to zero (region is depleted), the remaining elecric field is dropped across this high-field depletion region
- As the drain voltage is increases further, the pinch off point moves back towards source
- Channel Length Modulation: The effective channel length is thus reduced → higher I_{DS}

Linear MOSFET Model

Channel (inversion) charge: neglect reduction at drain

Velocity saturation defines $V_{DS,SAT} = E_{sat} L =$ constant

$- v_{sat} / \mu_n$

Drain current:

$$I_{D,SAT} = -WvQ_N = -W(v_{sat})[-C_{ox}(V_{GS} - V_{Tn})],$$

$|E_{sat}| = 10^4$ V/cm, $L = 0.12$ μm → $V_{DS,SAT} = 0.12$ V!

$$I_{D,SAT} = v_{sat} W C_{ox}(V_{GS} - V_{Tn})(1 + \lambda_n V_{DS})$$

Why Find an Incremental Model?

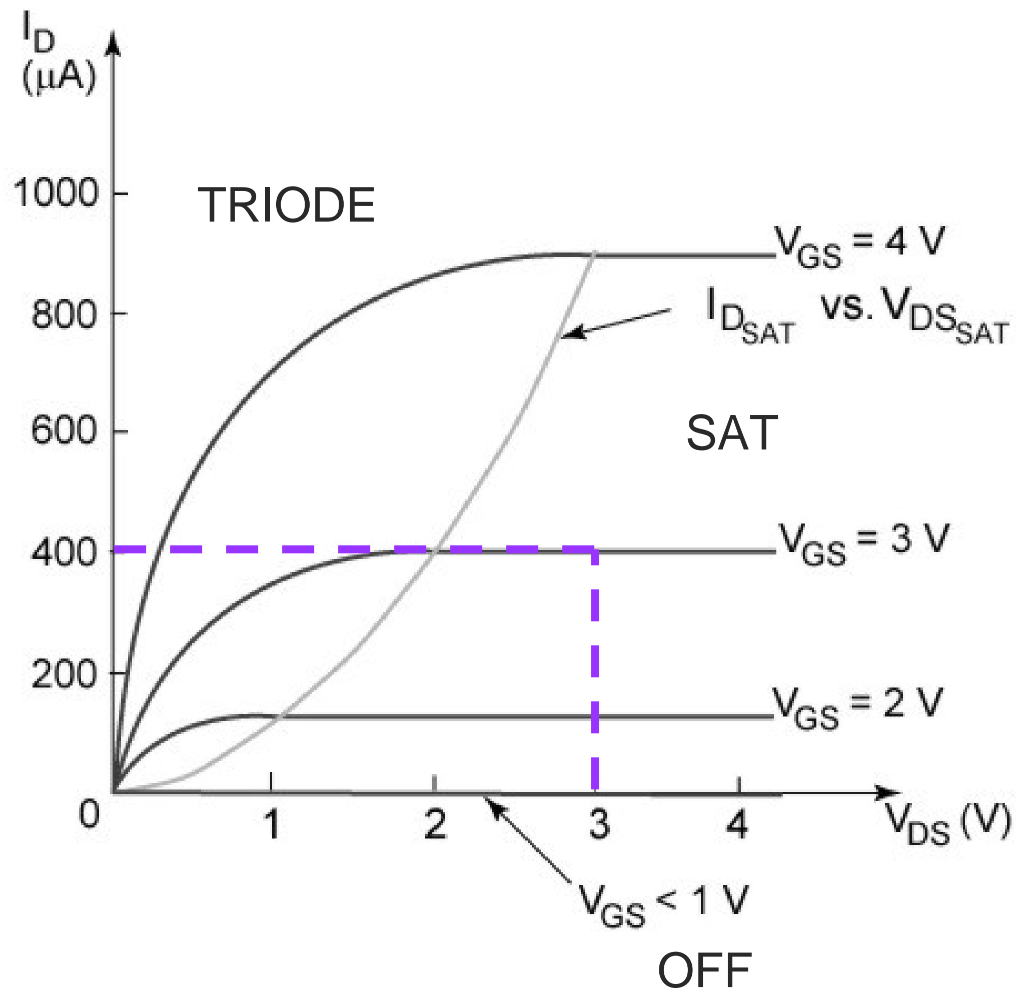
- Signals of interest in analog ICs are often of the form:

$$v_{GS}(t) = V_{GS} + v_{gs}(t)$$

Fixed Bias Point (points to V_{GS}) Small Signal (points to $v_{gs}(t)$)

Direct substitution into $i_D = f(v_{GS}, v_{DS})$ is tedious AND doesn't include charge-storage effects … pretty rough approximation

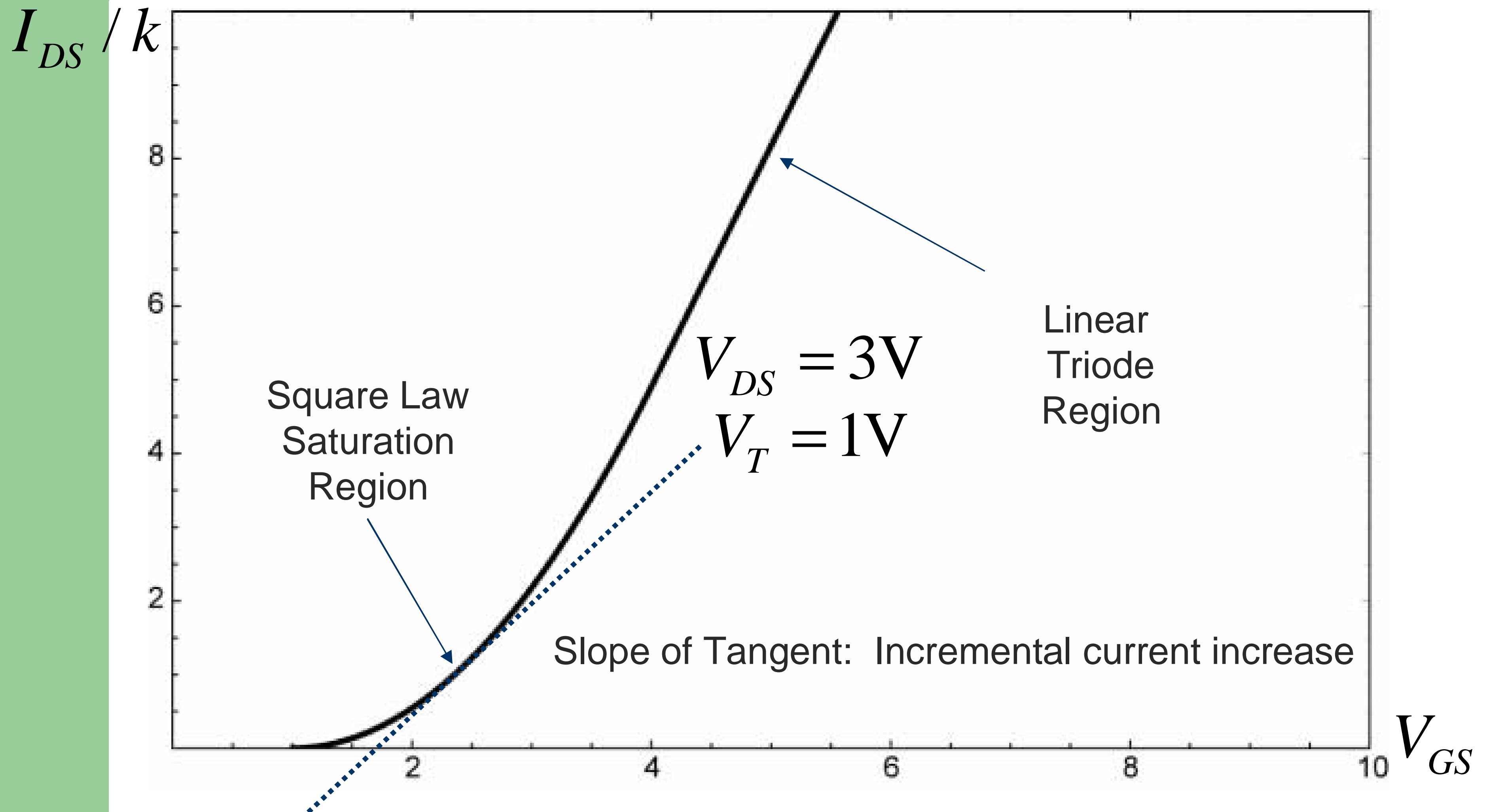
Which Operating Region?



$$V_{GS} = 3\text{V}$$

$$V_{DS} = 3\text{V}$$

Changing One Variable at a Time



Assumption: $V_{DS} > V_{DS,SAT} = V_{GS} - V_{Tn}$ (square law)

The *Transconductance* g_m

Defined as the change in drain current due to a change in the *gate-source* voltage, with *everything else constant*

$$I_{DS,sat} = \frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

$$g_m = \left.\frac{\Delta i_D}{\Delta v_{GS}}\right|_{V_{GS},V_{DS}} = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{GS},V_{DS}} = \mu C_{ox}\frac{W}{L}(V_{GS} - V_T)(1 + \lambda V_{DS})$$

$\lambda V_{DS} \approx 0$

$$g_m = \mu C_{ox}\frac{W}{L}(V_{GS} - V_T)$$

← Gate Bias

$$g_m = \mu C_{ox}\frac{W}{L}\sqrt{\frac{2I_{DS}}{\frac{W}{L}\mu C_{ox}}} = \sqrt{2\mu C_{ox}\frac{W}{L}I_{DS}}$$

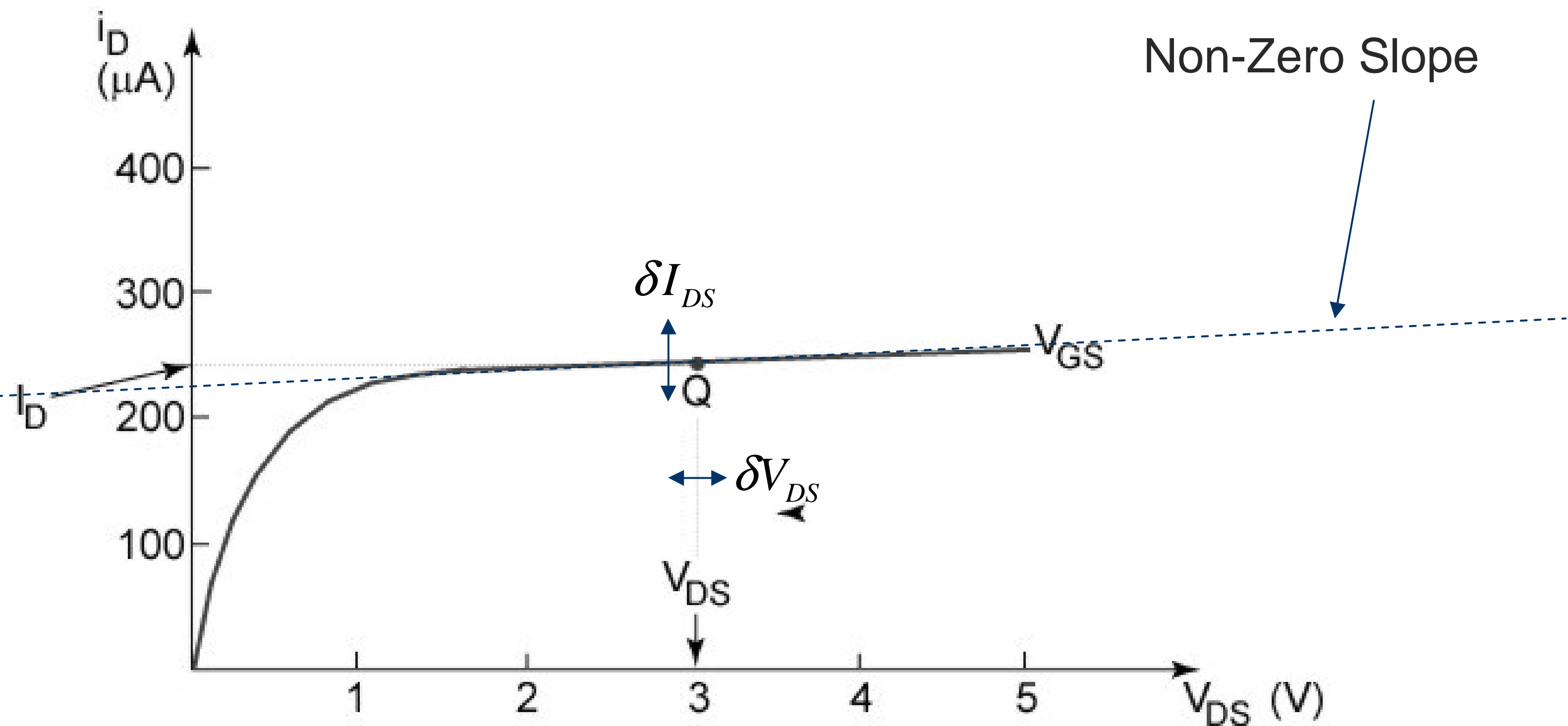
← Drain Current Bias

$$g_m = \frac{2I_{DS}}{(V_{GS} - V_T)}$$

← Drain Current Bias and Gate Bias

Output Resistance r_o

Defined as the inverse of the change in drain current due to a change in the *drain-source* voltage, with *everything else constant*



Evaluating r_o

$$i_D = \frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

$$r_o = \left(\left. \frac{\partial i_D}{\partial v_{DS}} \right|_{V_{GS}, V_{DS}} \right)^{-1}$$

$$r_0 = \frac{1}{\frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS} - V_T)^2 \lambda}$$

$$r_0 \approx \frac{1}{\lambda I_{DS}}$$

Total Small Signal Current

$$i_{DS}(t) = I_{DS} + i_{ds}$$

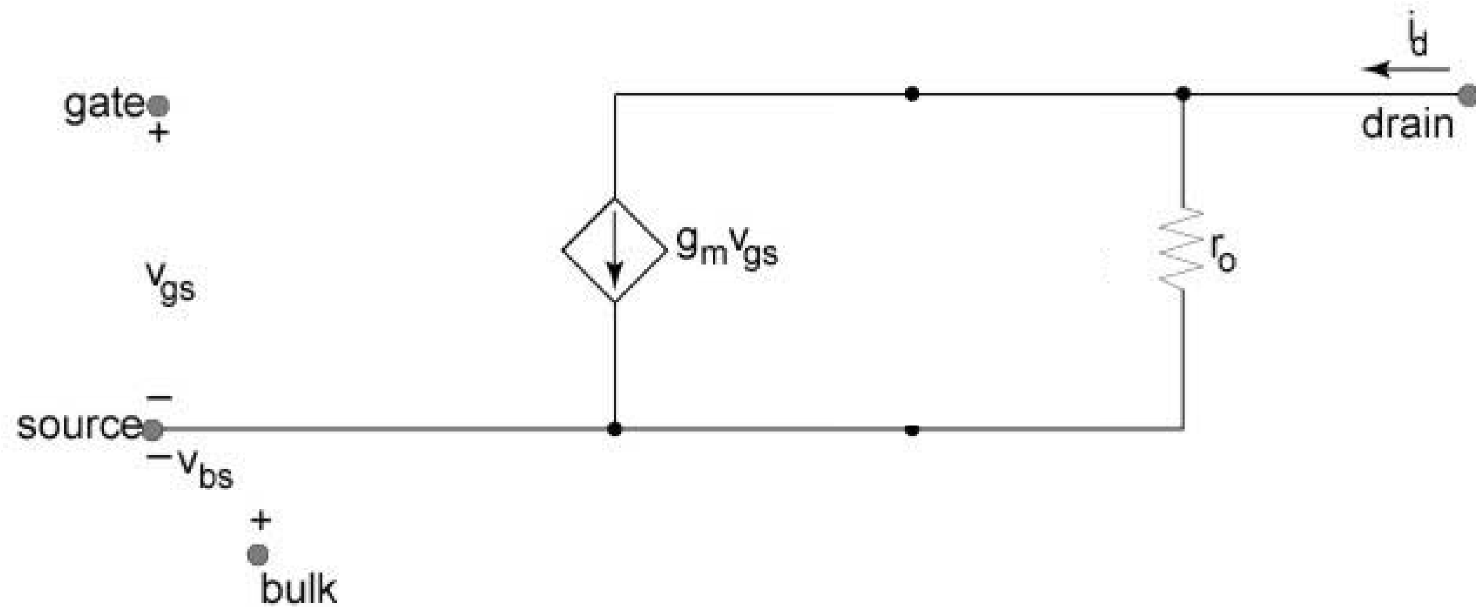
$$i_{ds} = \frac{\partial i_{DS}}{\partial v_{gs}} v_{gs} + \frac{\partial i_{DS}}{\partial v_{ds}} v_{ds}$$

$$i_{ds} = g_m v_{gs} + \frac{1}{r_o} v_{ds}$$

*Trans*conductance

Conductance

Putting Together a Circuit Model



$$i_{ds} = g_m v_{gs} + \frac{1}{r_o} v_{ds}$$

Role of the Substrate Potential

Need not be the source potential, but $V_B < V_S$

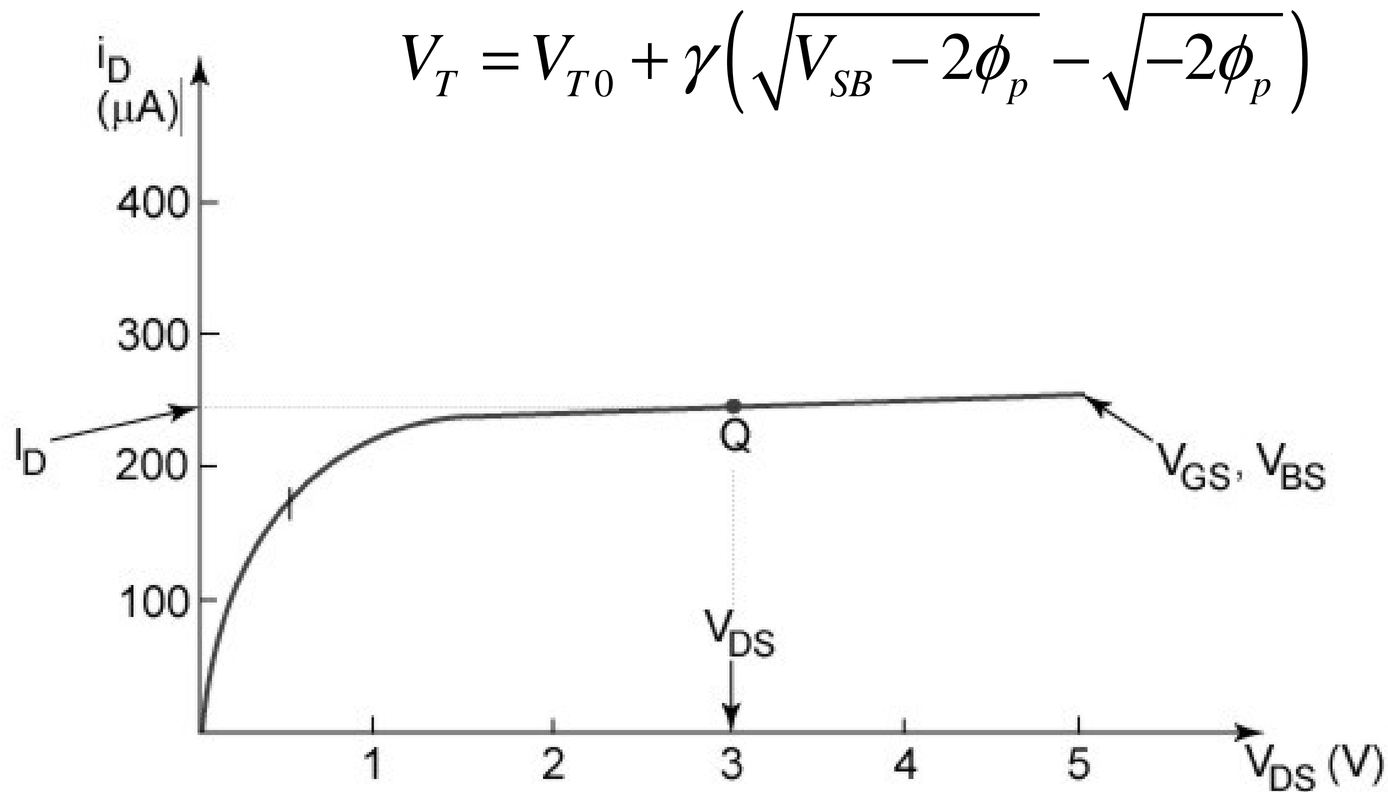
Effect: changes threshold voltage, which changes the drain current … substrate acts like a "backgate"

$$g_{mb} = \left.\frac{\Delta i_D}{\Delta v_{BS}}\right|_Q = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q$$

$Q = (V_{GS}, V_{DS}, V_{BS})$

Backgate Transconductance

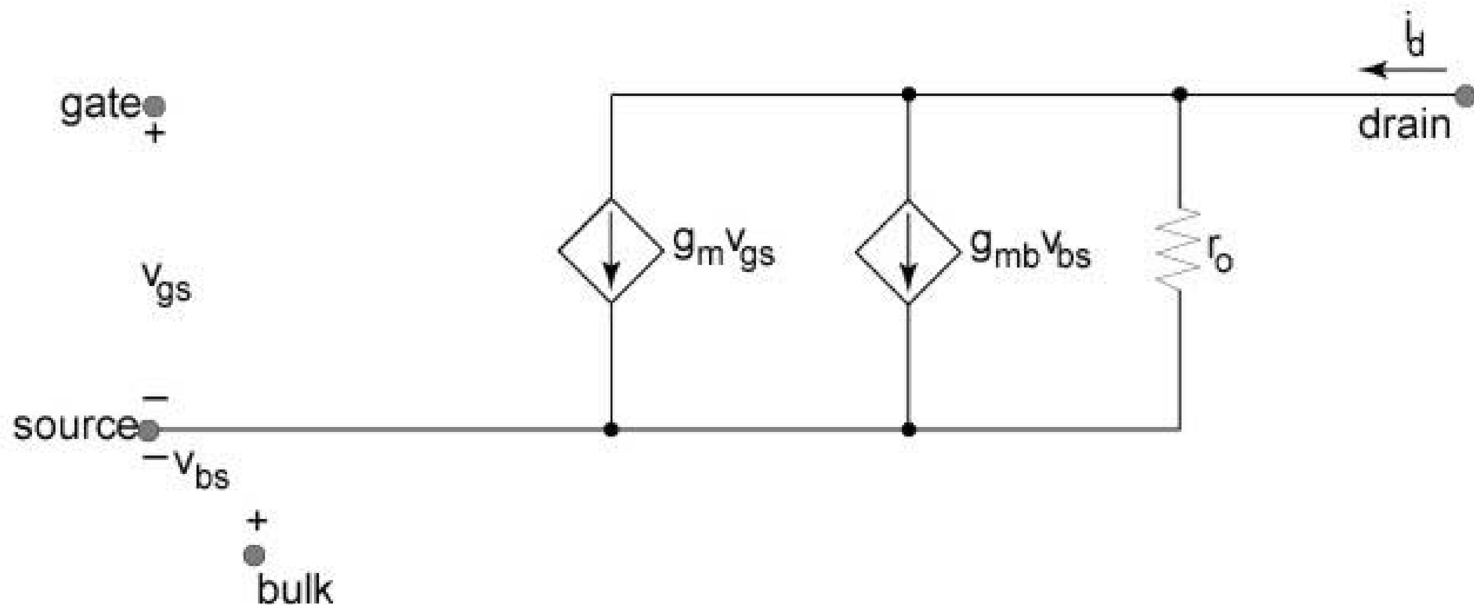
$$V_T = V_{T0} + \gamma\left(\sqrt{V_{SB} - 2\phi_p} - \sqrt{-2\phi_p}\right)$$



Result:

$$g_{mb} = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q = \left.\frac{\partial i_D}{\partial V_{Tn}}\right|_Q \left.\frac{\partial V_{Tn}}{\partial v_{BS}}\right|_Q = \frac{\gamma g_m}{2\sqrt{-V_{BS} - 2\phi_p}}$$

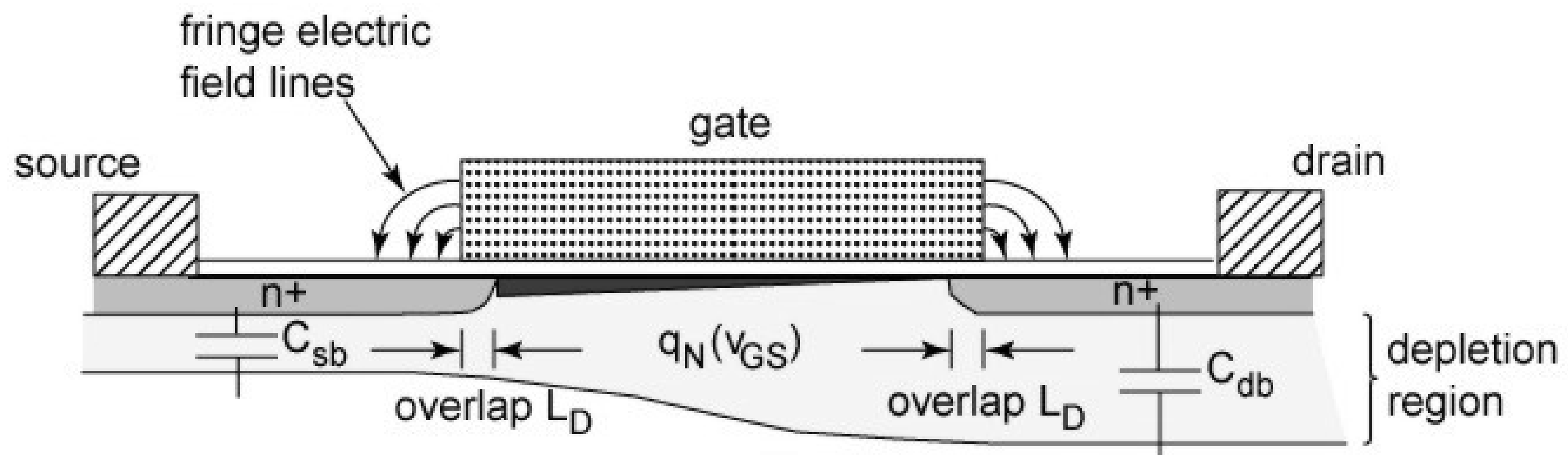
Four-Terminal Small-Signal Model



$$i_{ds} = g_m v_{gs} + g_{mb} v_{bs} + \frac{1}{r_o} v_{ds}$$

MOSFET Capacitances in Saturation

Gate-source capacitance: channel charge is not controlled by drain in saturation.



Gate-Source Capacitance C_{gs}

Wedge-shaped charge in saturation → effective area is (2/3)*WL* (see H&S 4.5.4 for details)

$$C_{gs} = (2/3)WLC_{ox} + C_{ov}$$

Overlap capacitance along source edge of gate →

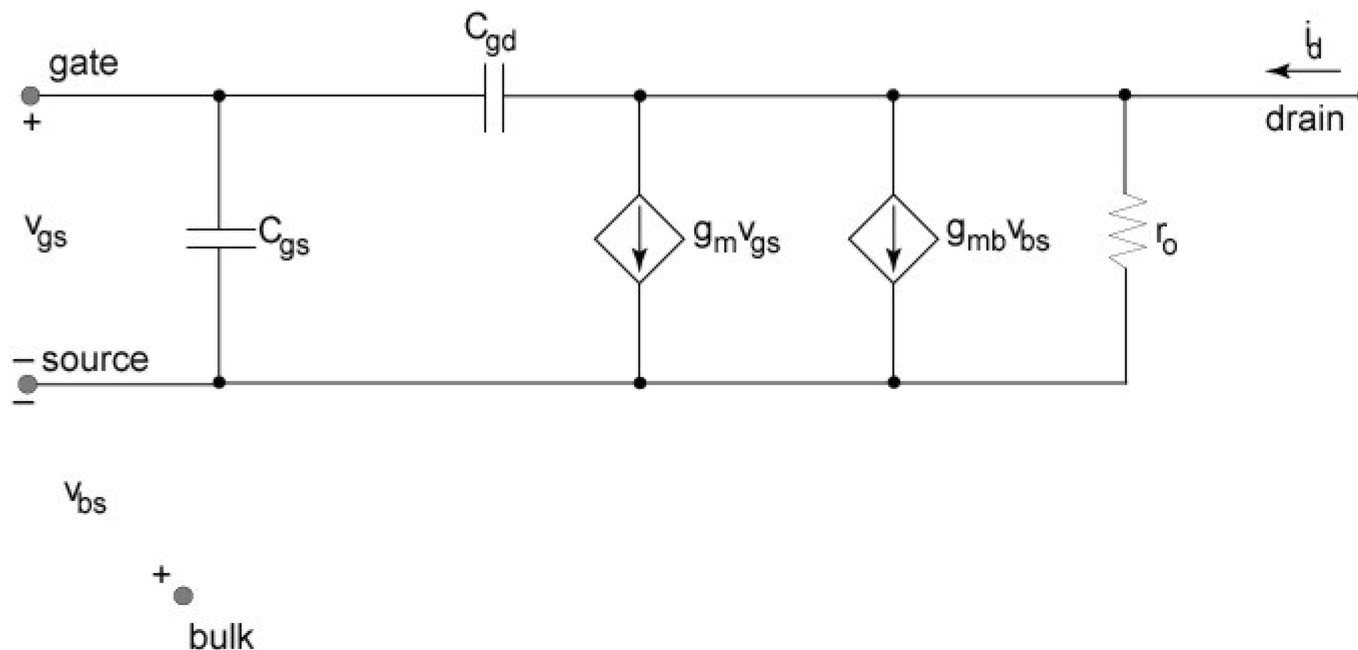
$$C_{ov} = L_D W C_{ox}$$

(Underestimate due to fringing fields)

Gate-Drain Capacitance C_{gd}

Not due to change in inversion charge in channel

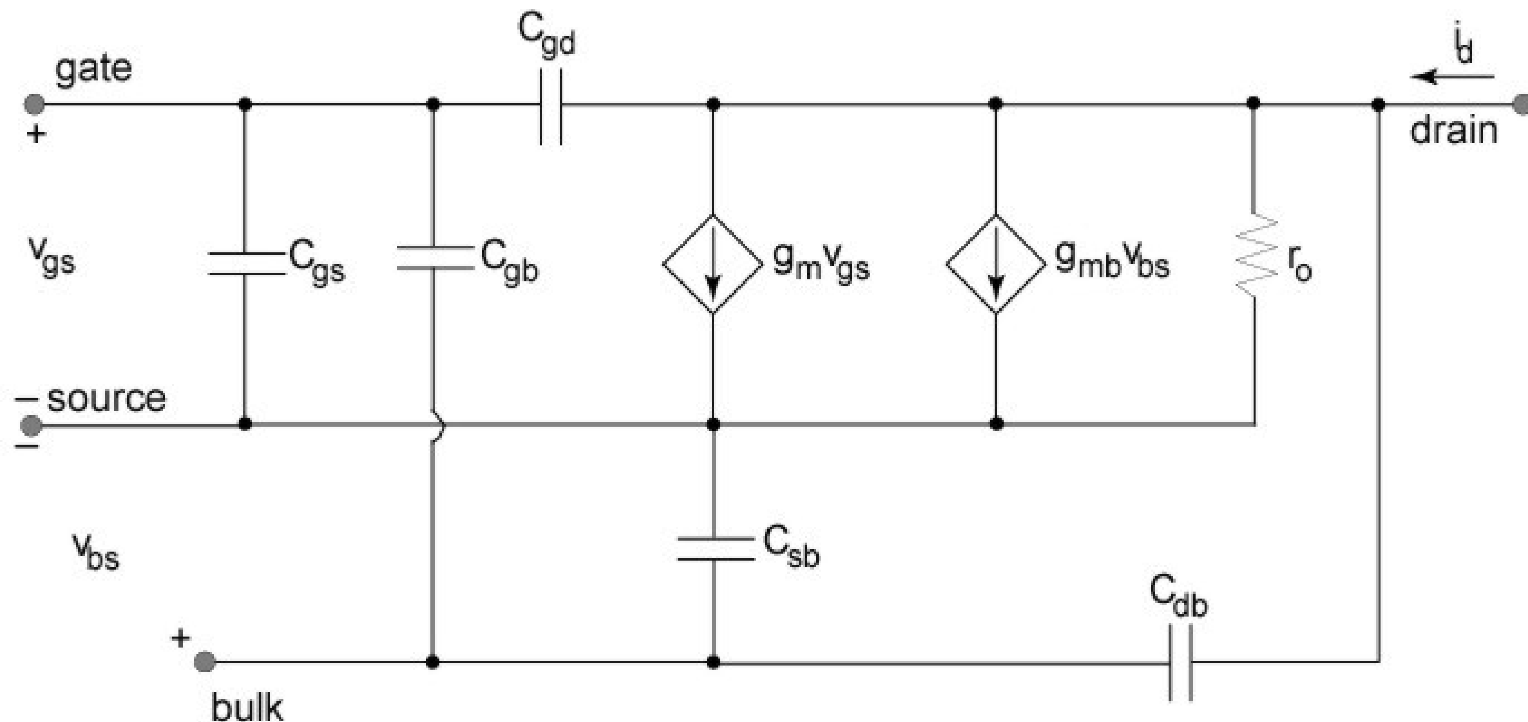
Overlap capacitance C_{ov} between drain and source is C_{gd}



Junction Capacitances

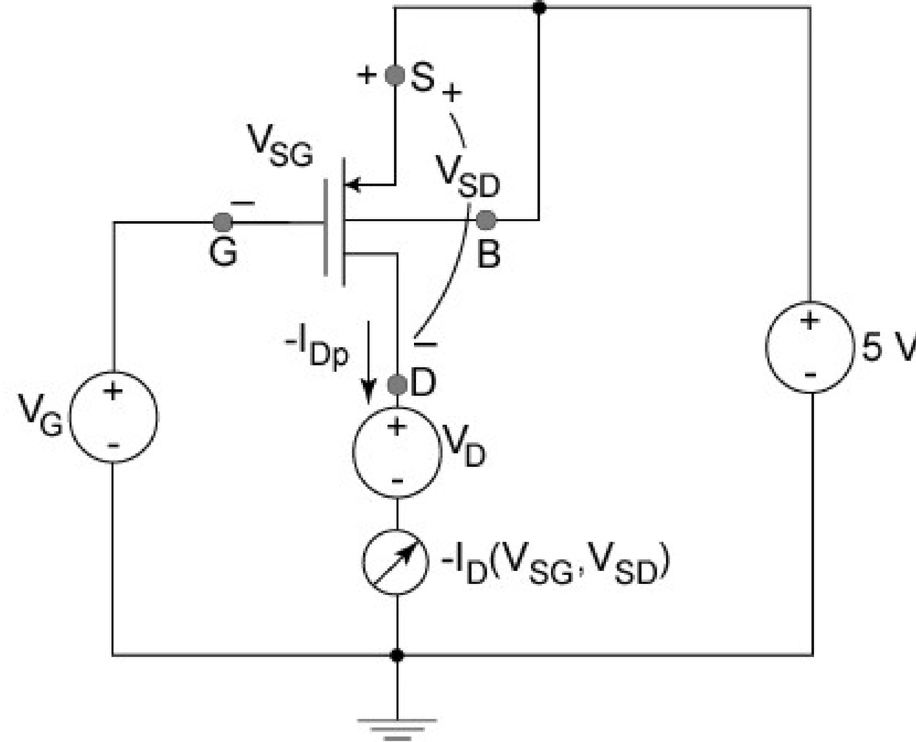
Drain and source diffusions have (different) junction capacitances since V_{SB} and $V_{DB} = V_{SB} + V_{DS}$ aren't the same

Complete model (without interconnects)

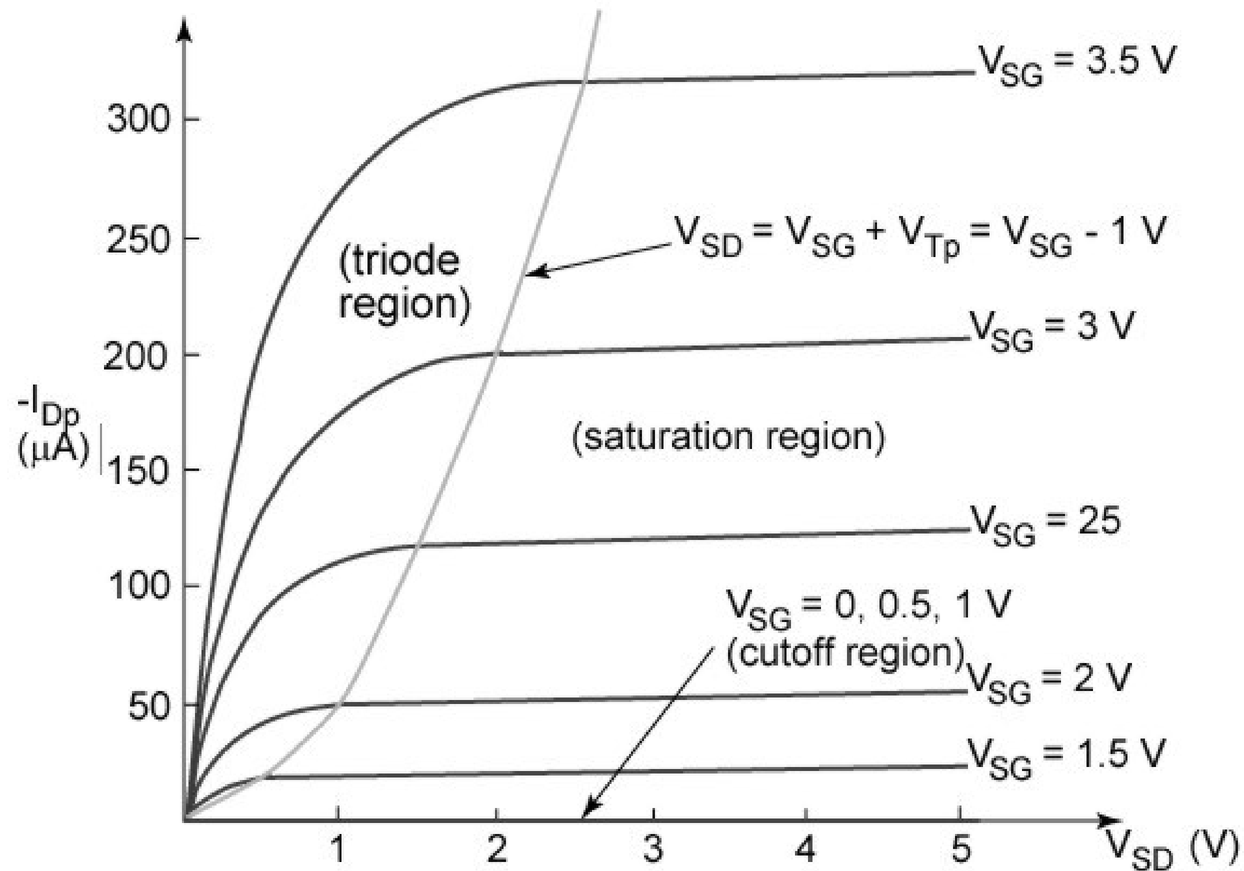


P-Channel MOSFET

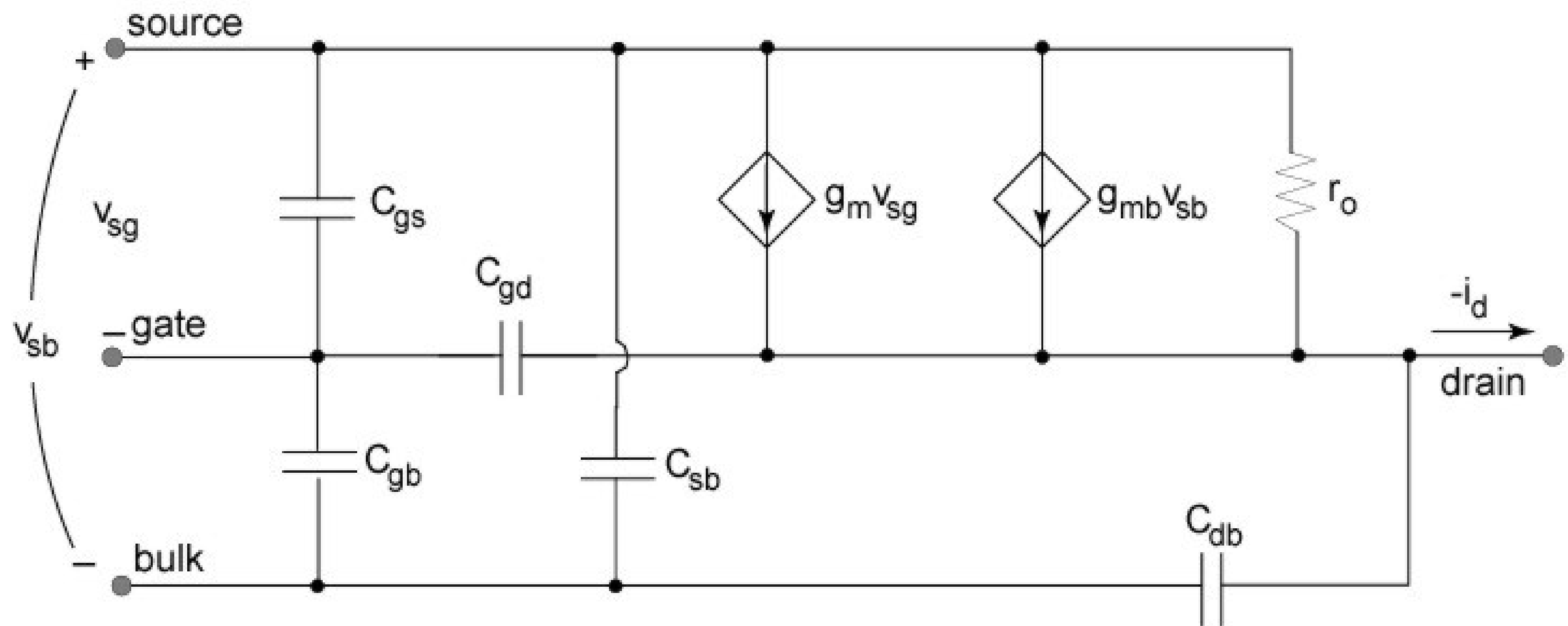
Measurement of $-I_{Dp}$ versus V_{SD}, with V_{SG} as a parameter:



Square-Law PMOS Characteristics



Small-Signal PMOS Model



MOSFET SPICE Model

Many "levels" … we will use the square-law "Level 1" model

See H&S 4.6 + Spice refs. on reserve for details.

```
.MODEL MODN NMOS LEVEL = 1 VTO = 1 KP = 50U LAMBDA = .033 GAMMA = .6
+ PHI = 0.8 TOX = 1.5E–10 CGDO = 5E–10 CGSO = 5E–10 CJ = 1E–4 CJSW = 5E–10
+ MJ = 0.5 PB = 0.95
.MODEL MODP PMOS LEVEL = 1 VTO = –1 KP = 25U LAMBDA = .033 GAMMA = .6
+ PHI = 0.8 TOX = 1.5E–10 CGDO = 5E–10 CGSO = 5E–10 CJ = 3E–4 CJSW = 3.5E–10
+ MJ = 0.5 PB = 0.95
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