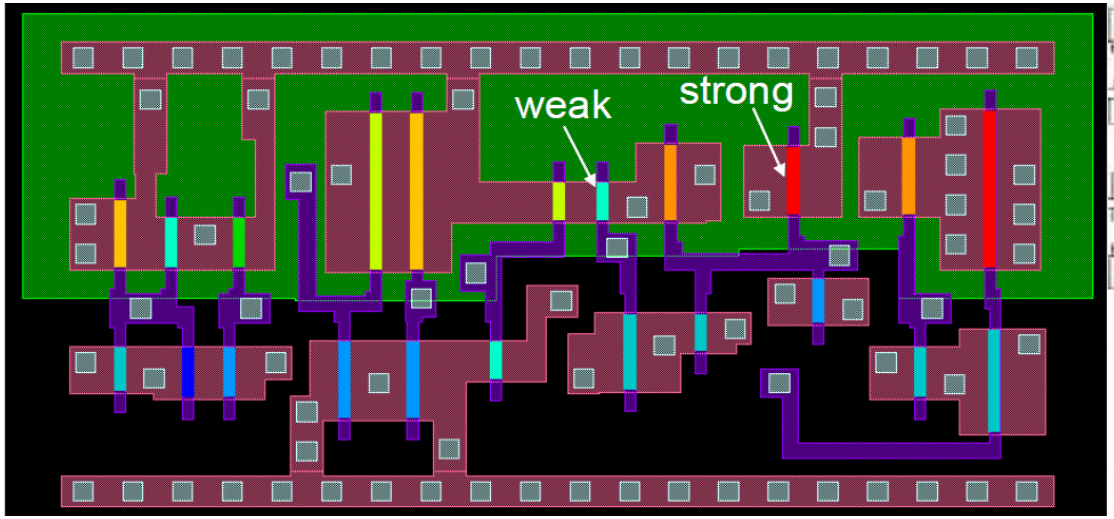
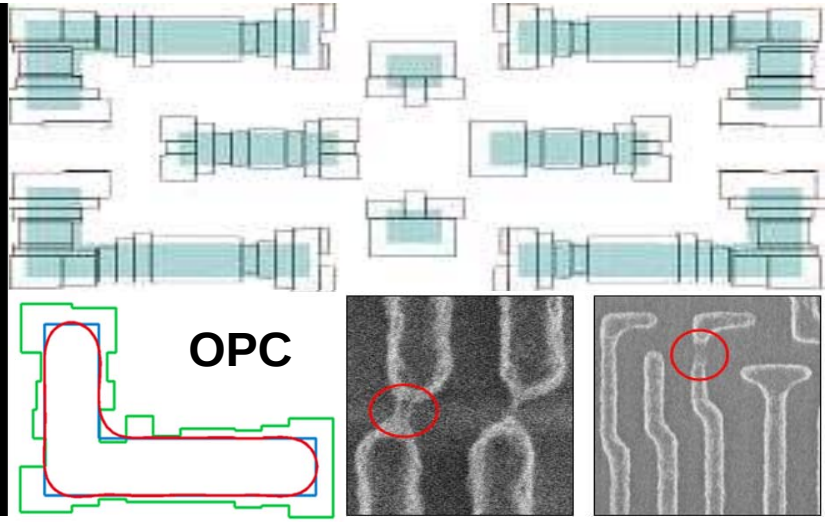


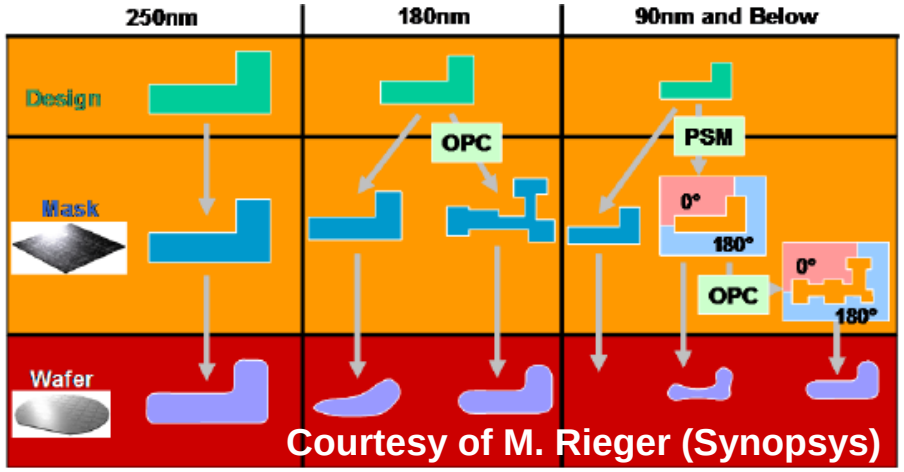


Lecture 12

- **Process-induced Variations II: Systematic**
  - Lithographic Proximity Effect
  - Layout Dependent Strain
  - Well Proximity Effect

Reading: multiple research articles (reference list at the end of this lecture)

Lithography Proximity Effect (LPE)



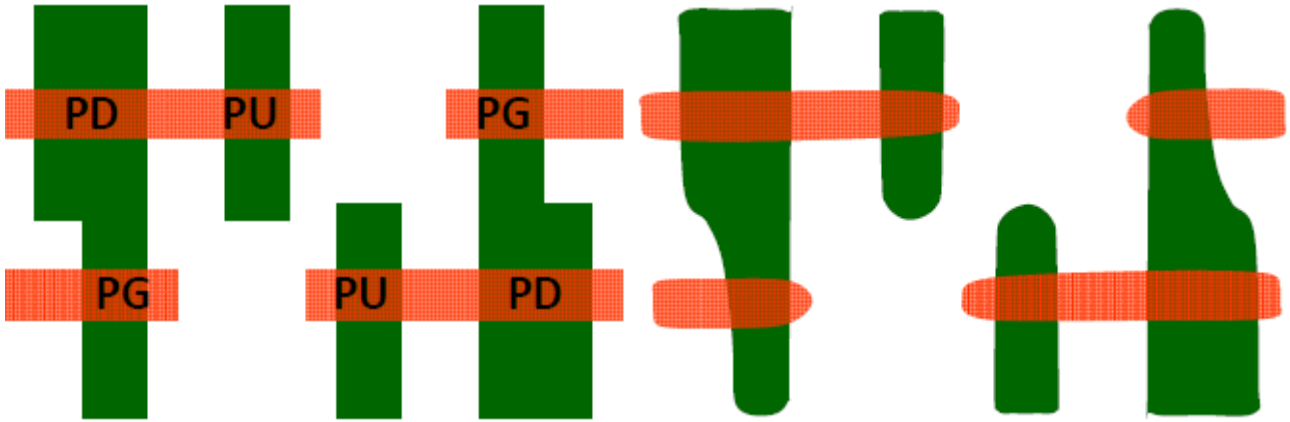
- **Optical Proximity Correction (OPC)**

used to compensate for image errors due to diffraction effects by adding extra polygons to the pattern on the photomask

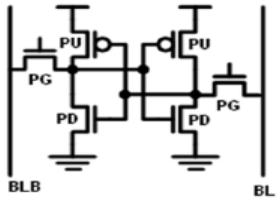
- **Phase Shift Mask (PSM)**

used to reduce the light interference by changing the thickness of transmitting patterns on the photomask (*i.e.* creating a phase shift light)

Desired 6T SRAM Layout

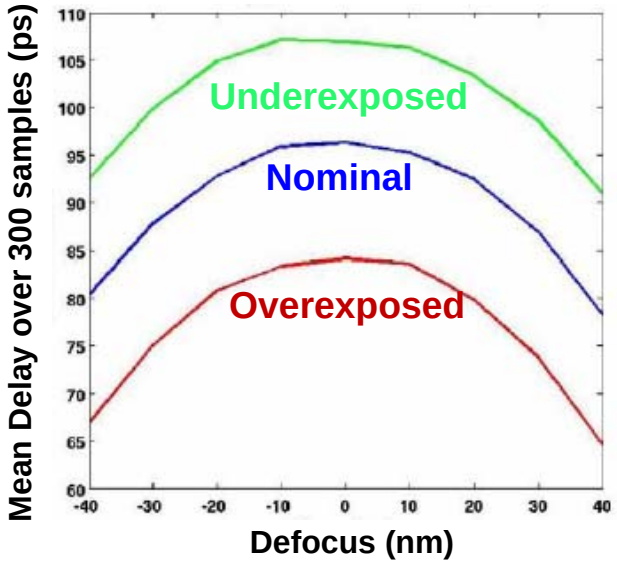


Actual Layout

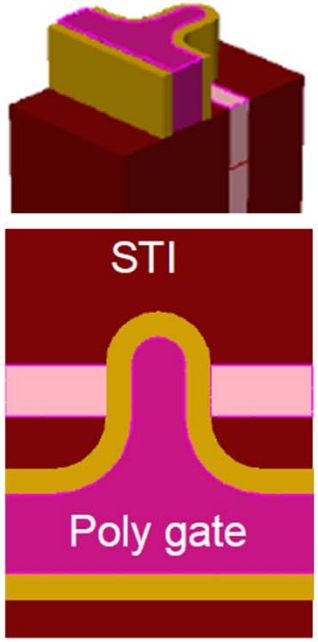


➢ These resolution enhancement techniques help to reduce the pattern distortions, yet still end with round corners.

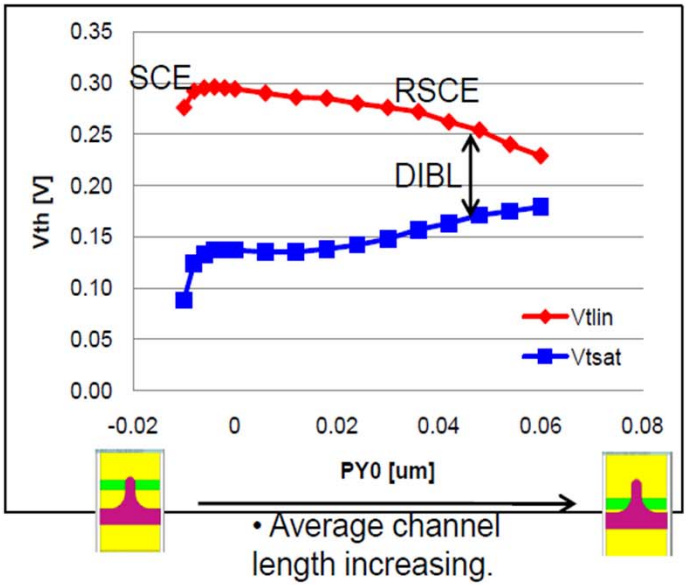
NAND2 Delay Distributions



Impact of Poly Corner Rounding: Gate-Extension Dependence

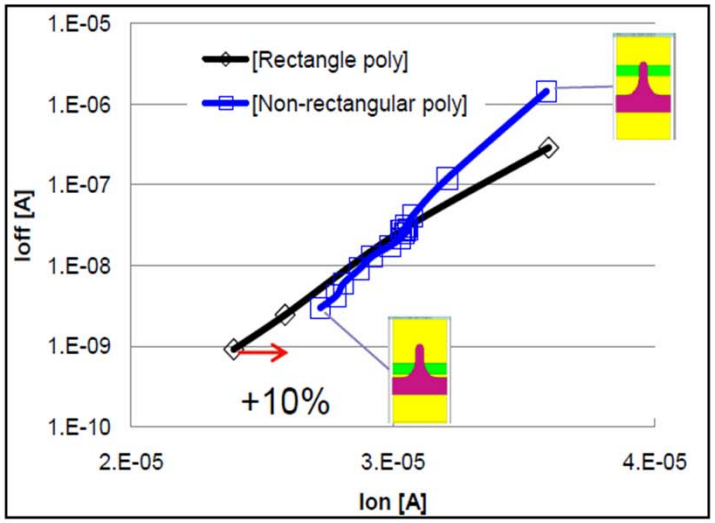


➢ Threshold voltage



• Average channel length increasing.

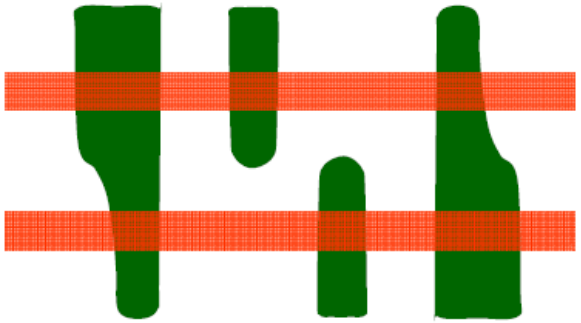
➢ I_{on}/I_{off} performance



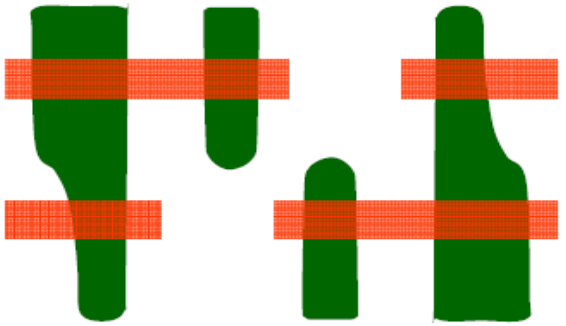
M. Choi, SPIE (2009)

- Poly corner rounding can be improved by using multiple patterning/exposure techniques.

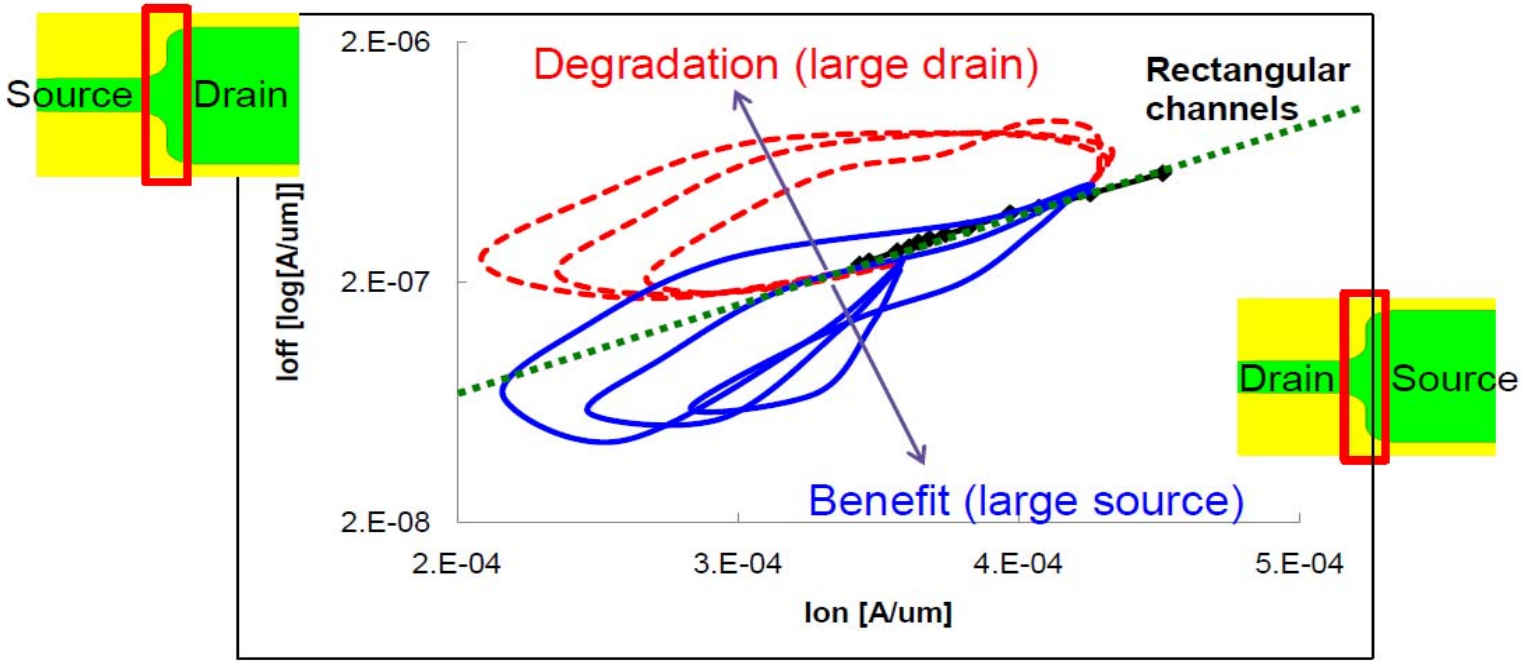
1st Gate Patterning



2nd Gate Patterning



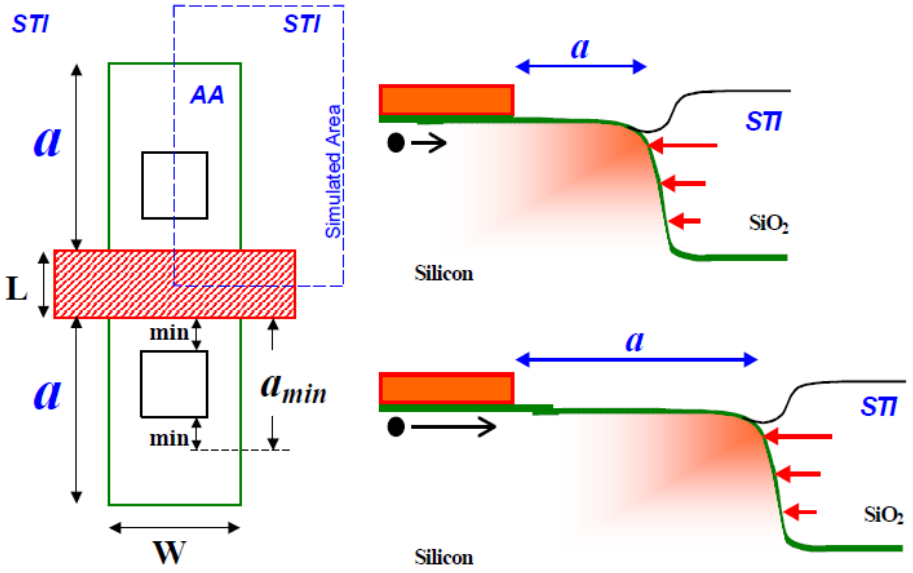
Impact of Active Region Rounding: Asymmetric Source/Drain

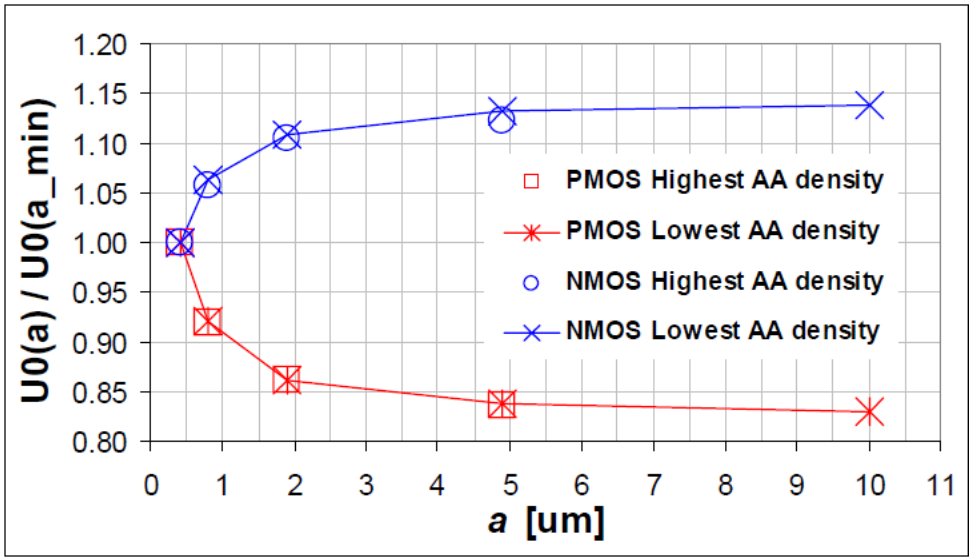


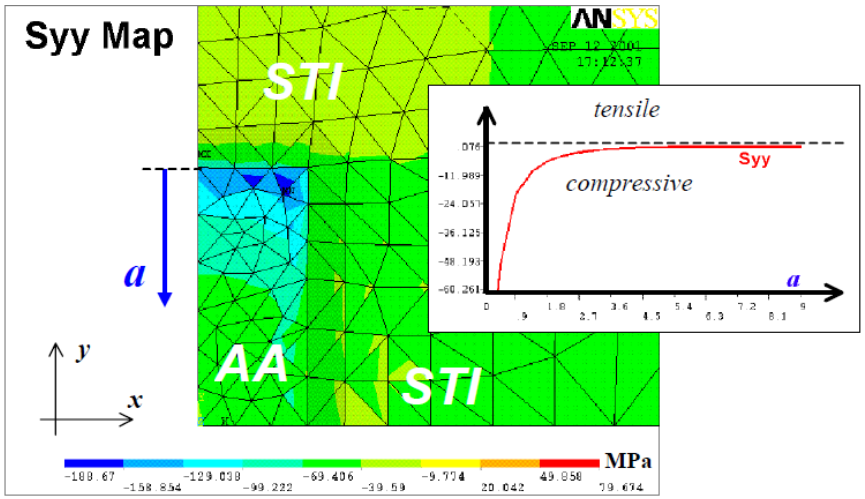
- Large source structure provides better performance
  - 10% Ion gain or 3x Ioff reduction
- Large drain structure degrades performance
  - 50% Ion degradation or 3x Ioff leakage

M. Choi, SPIE (2009)

STI Proximity Effect





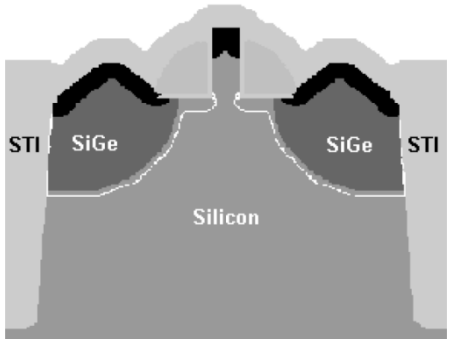


- Due to the different thermal expansion coefficients between Si and STI, there exists **biaxial compressive** residual stress in the active region after processing.
- STI-stress generally increases PMOS current and decreases NMOS current.
- Stress relaxes exponentially with increased distance from Si/STI boundary.

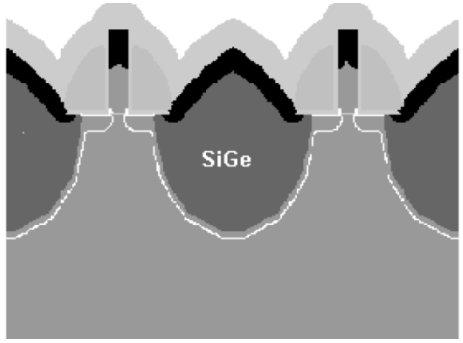
R. A. Bianchi, IEDM (2002)

Layout Dependent Strain: eSiGe Source/Drain

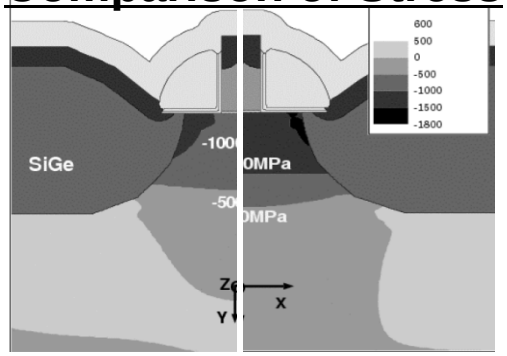
Isolated PMOS

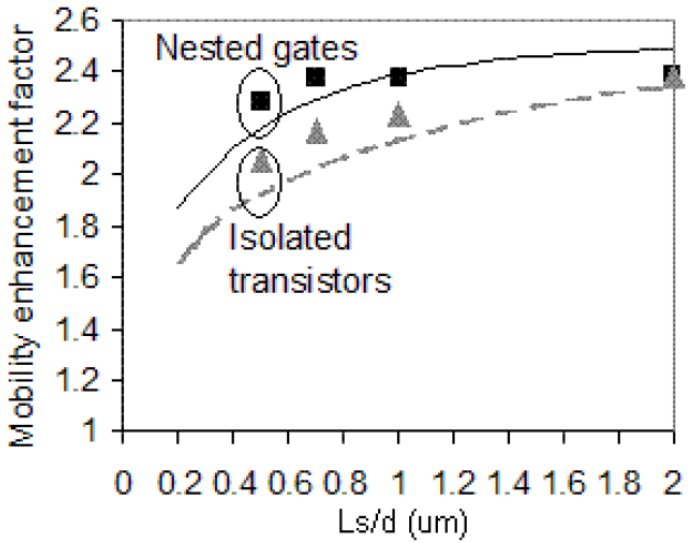


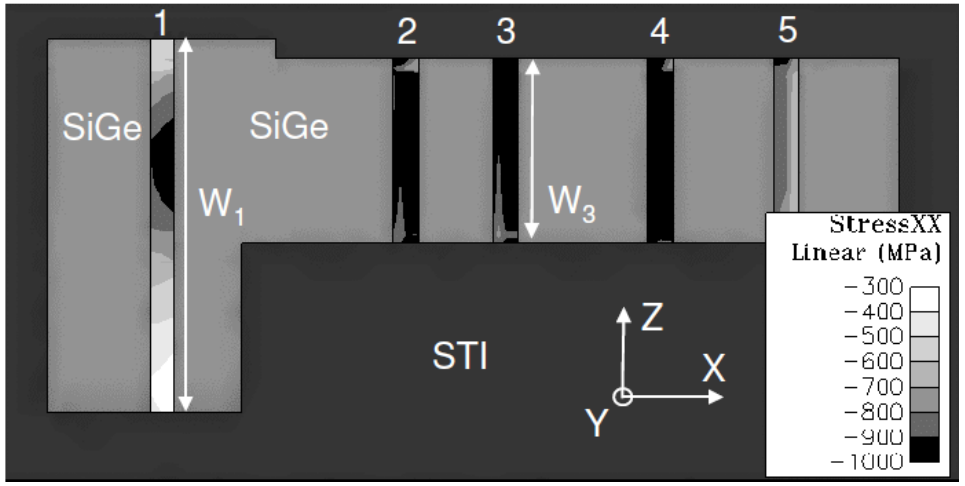
Nested PMOS



Comparison of Stress





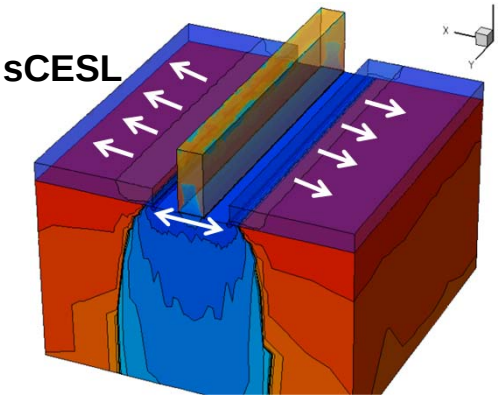


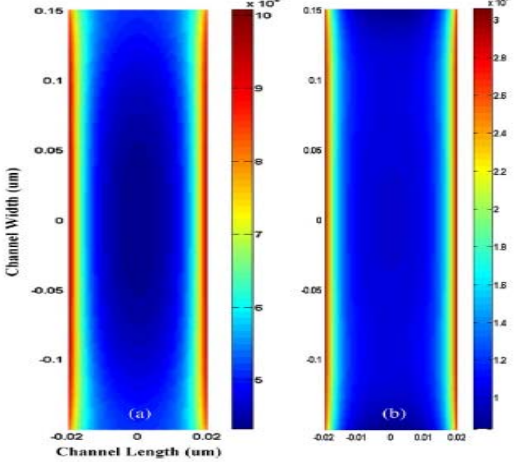
V. Moroz, SISPAD (2008)

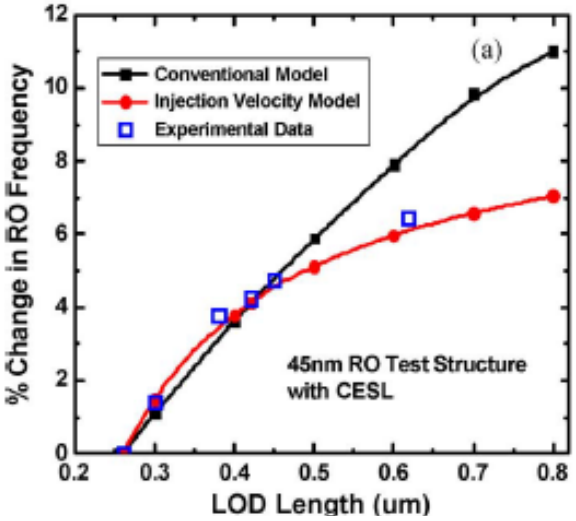
Other Sources for Layout Dependent Strain

sCESL-induced Strain

N. Xu, TDMR (2011)

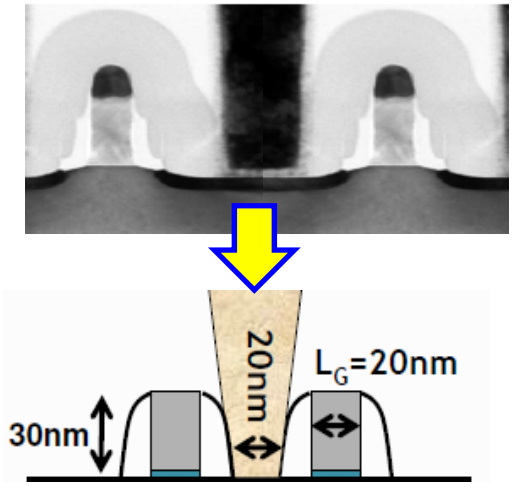


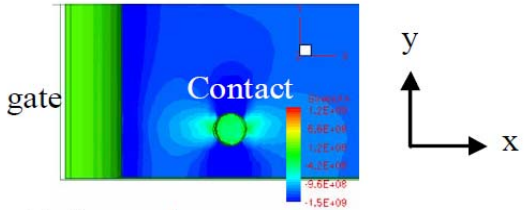




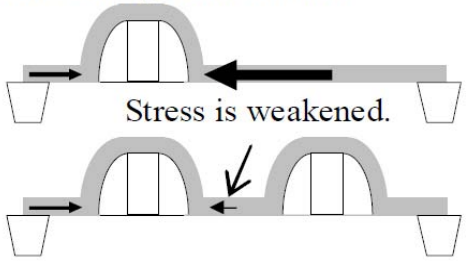
Contact-induced Strain

H. Aikawa, VLSI-T (2008)

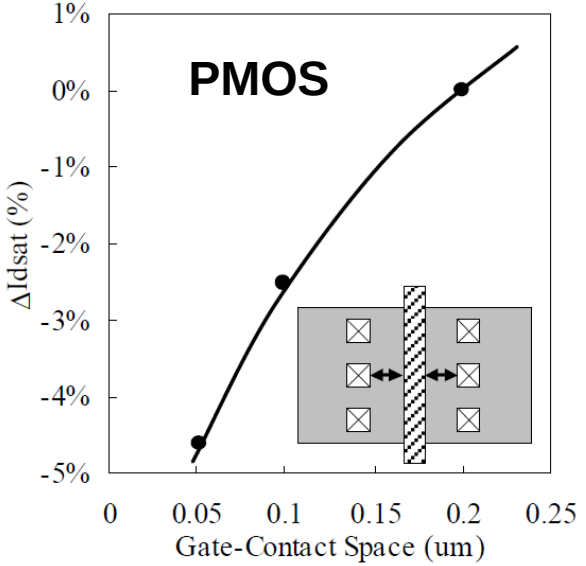




(a) Stress change near contact

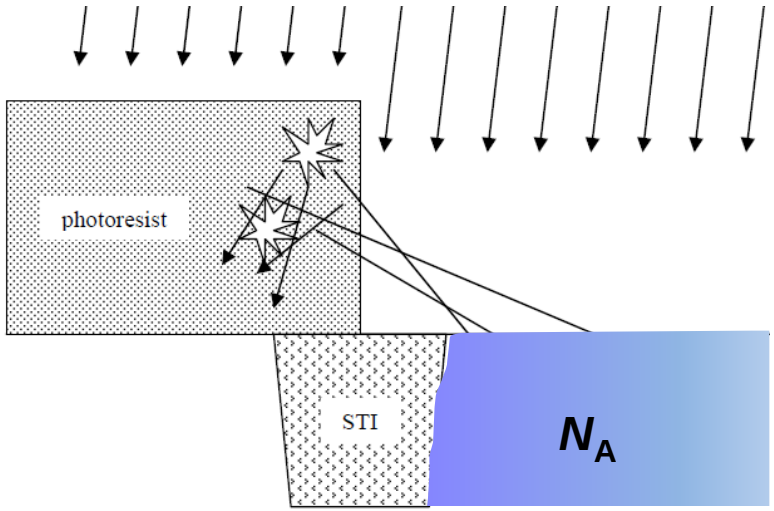


(b) The effect of neighboring gates

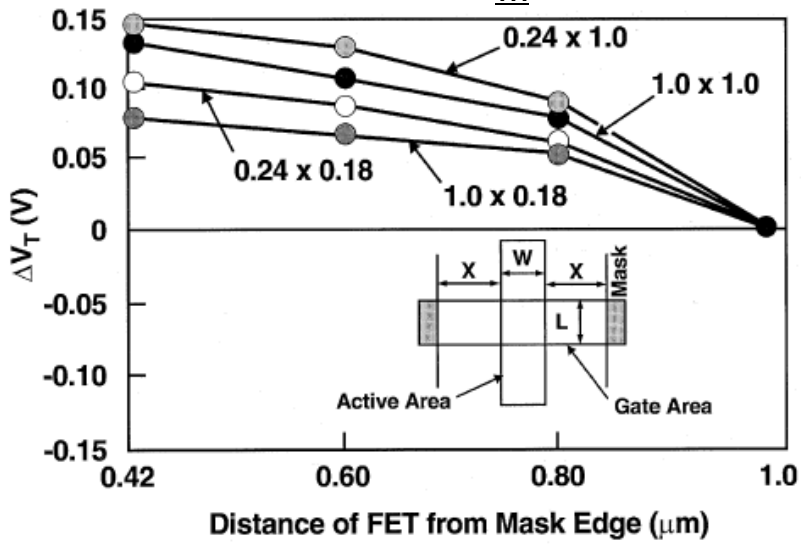


Well Proximity Effect (WPE)

Illustration of WPE

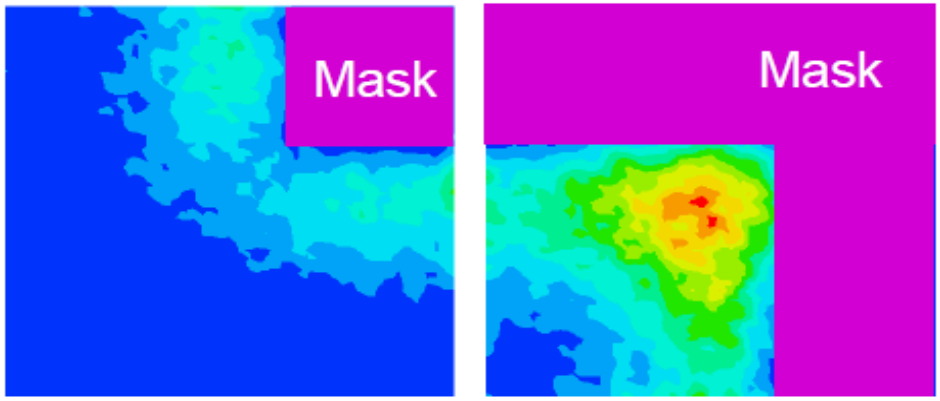


N-MOSFET V_{TH} *vs.* WP



T.B. Hook, T-ED (2003)

2-D WPE

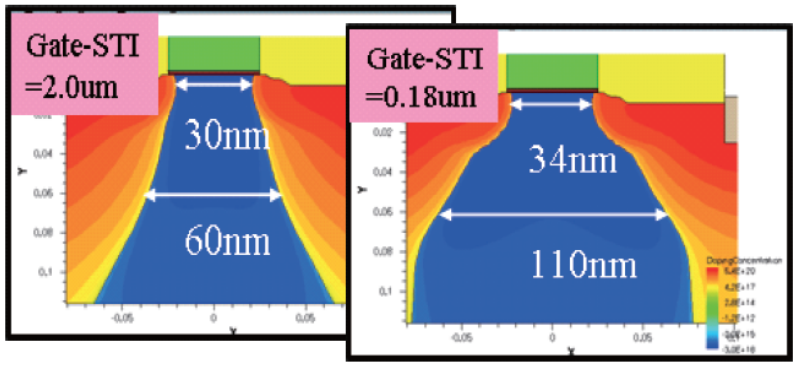


- During ion implantation, kinetic ions scatter back out of PR and become embedded in the Si near PR edge, causing V_{TH} shift.
- The affected distance is ~ 1um.
- Small angle II helps, but never avoids WPE.

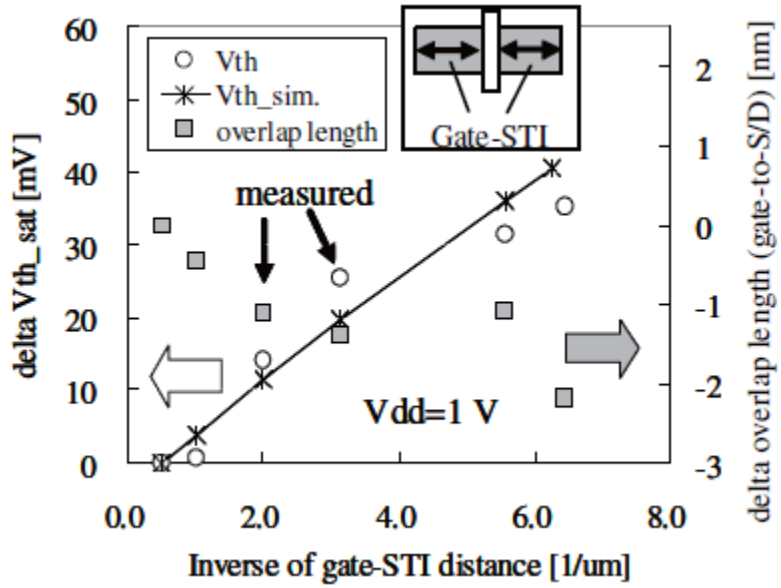
Another WPE: Stress-induced Enhanced/Retarded Diffusion

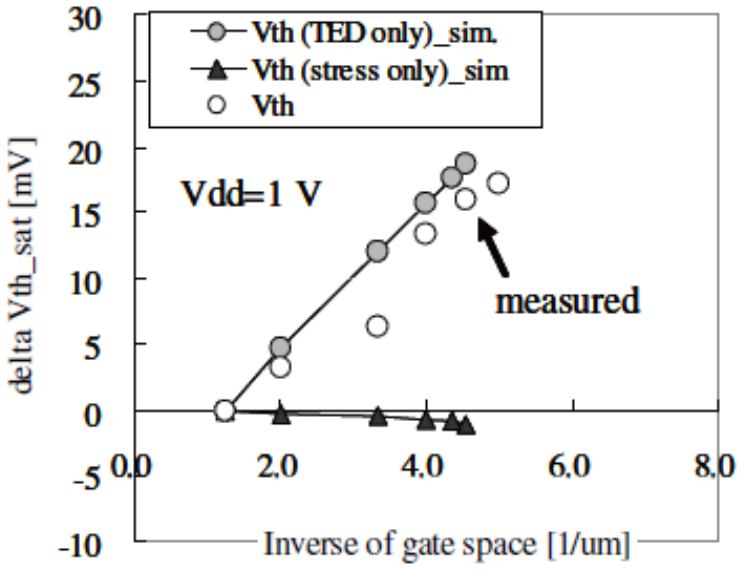
H. Tsuno, VLSI-T (2007)

Layout parameters shrinkage	NFET			PFET	
	B	As	P	B	As
Gate-STI	-9%	-17%	-34%	-23%	-43%
Gate space	1%	1%	3%	2%	4%
STI width	4%	8%	15%	11%	18%

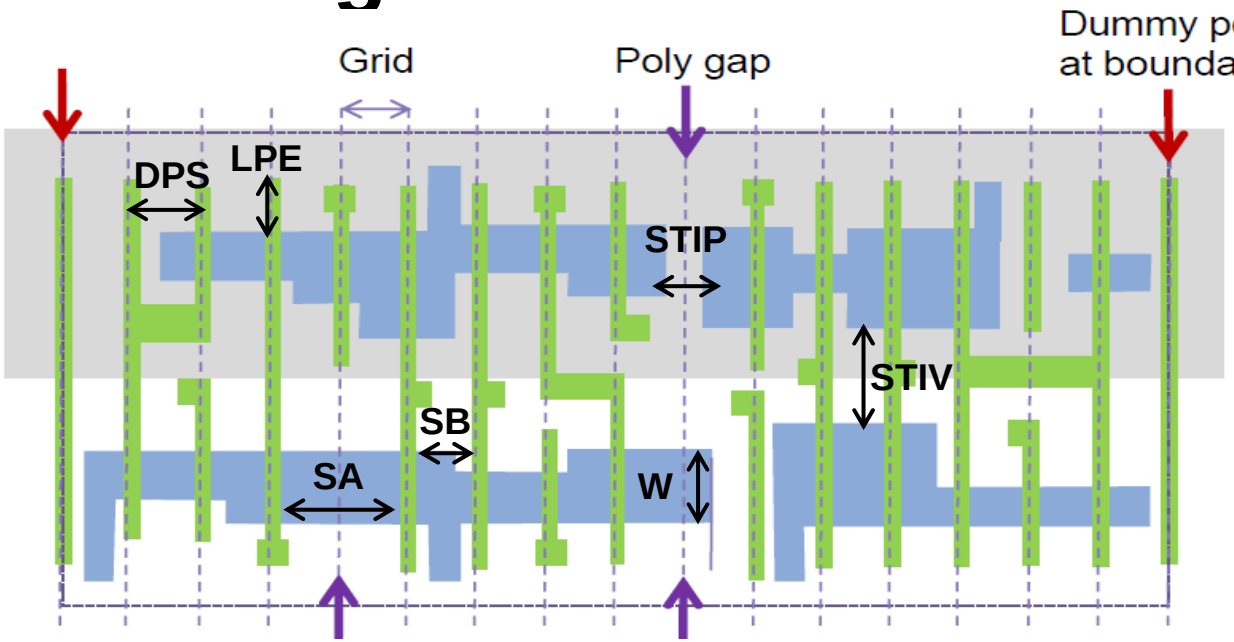


N-MOSFET V_{TH} Shift *vs*. Inverse of (*l*) STI-Gate Distance and (*r*)Gate Spacing





Design for Manufacturability (DFM)



- W, L (dominant)
- DPS: dummy poly(gate) spacing
- LPE: poly-extension (over active region) length
- SA/B: active region length
- STIP/V: STI distance to active region
- …

Carrier Mobility

$$\mu = \mu_{ref} \frac{1 + K_\mu \left(\frac{1}{SA + L/2} + \frac{1}{SB + L/2} \right)}{1 + K_\mu \left(\frac{1}{SA_{ref} + L/2} + \frac{1}{SB_{ref} + L/2} \right)}$$

Threshold Voltage

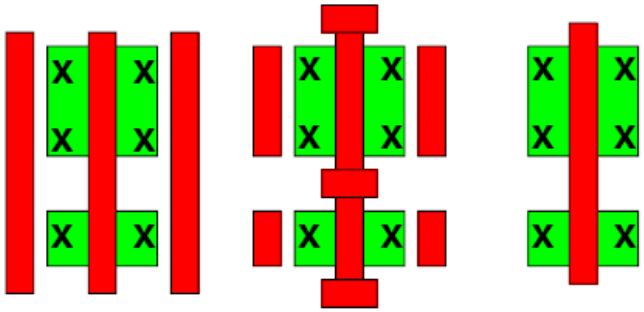
$$V_{TO} = V_{TO\,ref} + K_V \left(\frac{1}{SA + L/2} + \frac{1}{SB + L/2} - \frac{1}{SA_{ref} + L/2} - \frac{1}{SB_{ref} + L/2} \right)$$

where $$K_V = \frac{K_{VTO}}{1 + \frac{L_{KVTO}}{L^{LLODKVTO}} + \frac{W_{KVTO}}{W^{WLODKVO}} + + \frac{P_{KVTO}}{L^{LLODKVTO} W^{WLODKVTO}}}$$

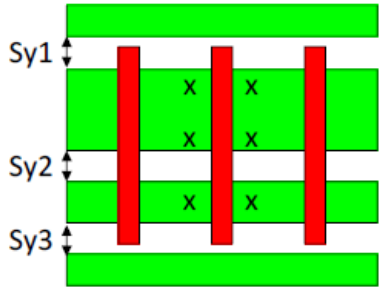
- Compact modeling is the best solution to leverage between the accuracy and design complexity.

Monitors for Systematic Variability

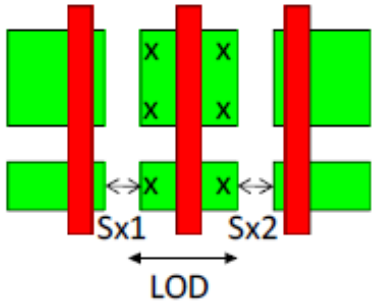
Defocus and LPE



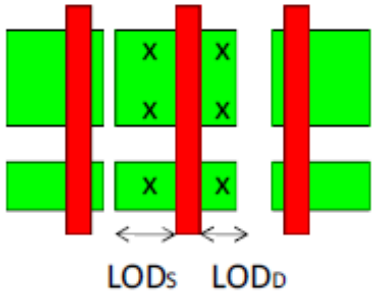
Vertial STIS & WPE



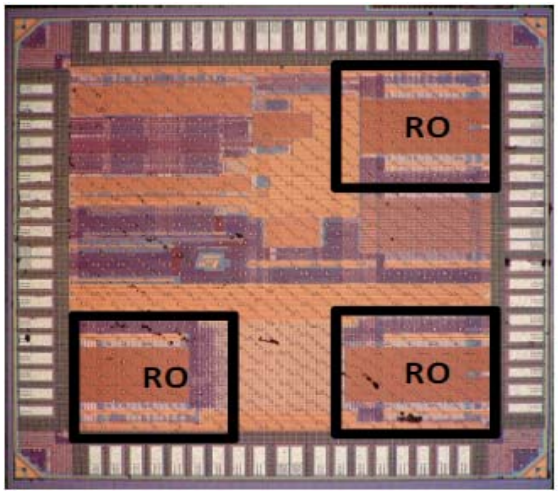
Multi-Level CESL Strain

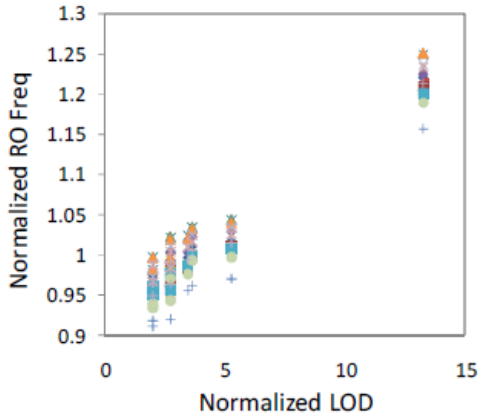


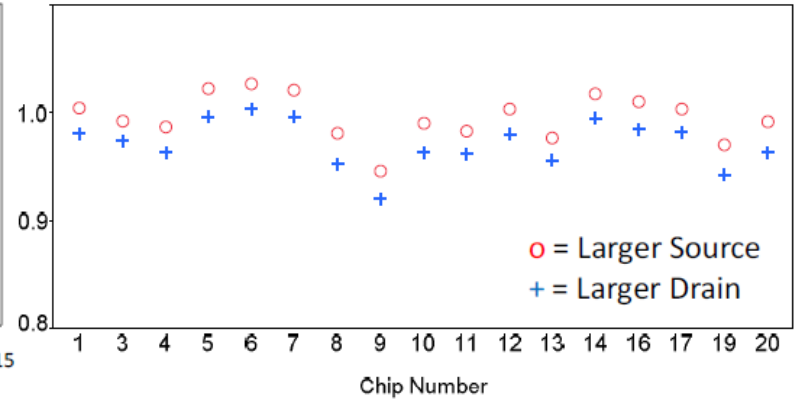
S/D Asymmetry



45nm Si Test Chip







L. Wang & N. Xu, CICC (2010)

- **Ring oscillators (RO) and OFF-state transistors are often used to characterize transistors' performance and leakage.**

Summary of Systematic Variability on Planar Bulk MOSFETs

Layout Variation	Typical I_{on} variation range	Typical V_{th} variation range
Length of diffusion (LOD) (SiGe or STI)	~30%	~50mV
Spacing to adjacent diffusion	~5%	~15mV
Active diffusion corners	~5%	~15mV
Poly spacing	~15%	~30mV
Poly corner rounding	~5%	~20mV
Well boundary (WPE)/ Dual stress liner (DSL)	~15%	~90mV
Contact to gate distance	~3%	~10mV

delay(ps) leakage power(nW)		no well proximity model		using well proximity model	
25C/1.0V		value	ratio	value	ratio
inverter	cell rise	27.98	1	30.12	1.08
	cell fall	19.34	1	21.19	1.10
	leakage	4.654	1	2.448	0.53
NAND	cell rise	31.18	1	33.34	1.07
	cell fall	28.83	1	31.55	1.09
	leakage	5.095	1	3.007	0.59
NOR	cell rise	55.67	1	59.88	1.08
	cell fall	20.52	1	22.38	1.09
	leakage	10.107	1	6.222	0.62

impacts of different systematic variability sources

Courtesy of X.-W. Lin (Synopsys)

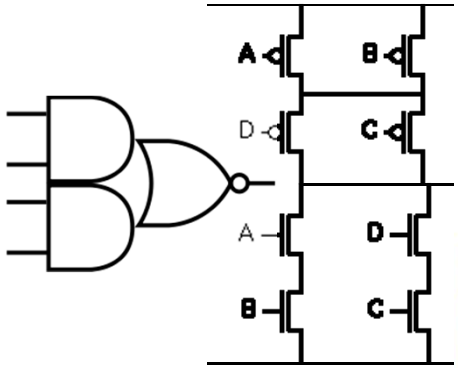
- **Layout-dependent strain and WPE play the dominant role on transistor performance's drift.**

standard logic circuit performance shift w/ WPE

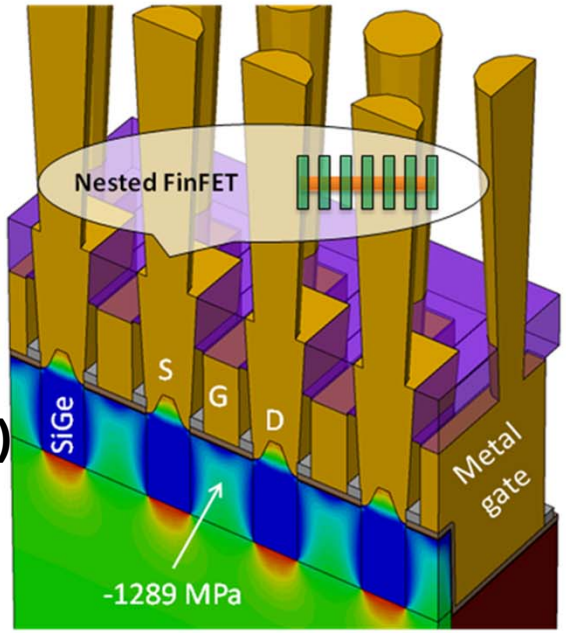
Y.-M. Sheu, CICC (2005)

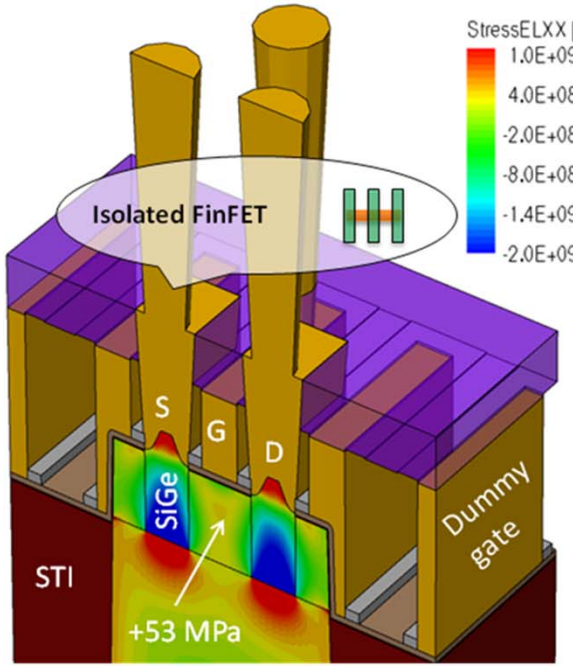
- **Small active-region area cells suffer more from systematic variability.**

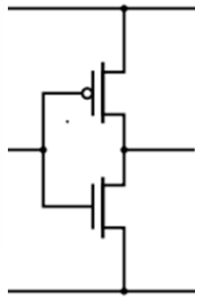
Impact of Layout Dependent Strain on FinFETs



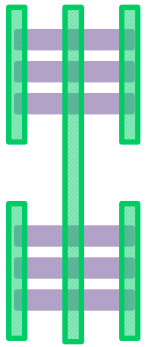
Pull-up network of AOI (AND-OR-Invert)

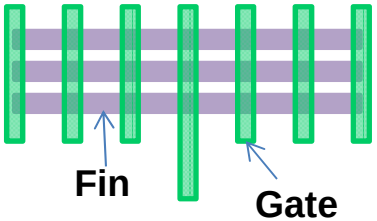






Inverter



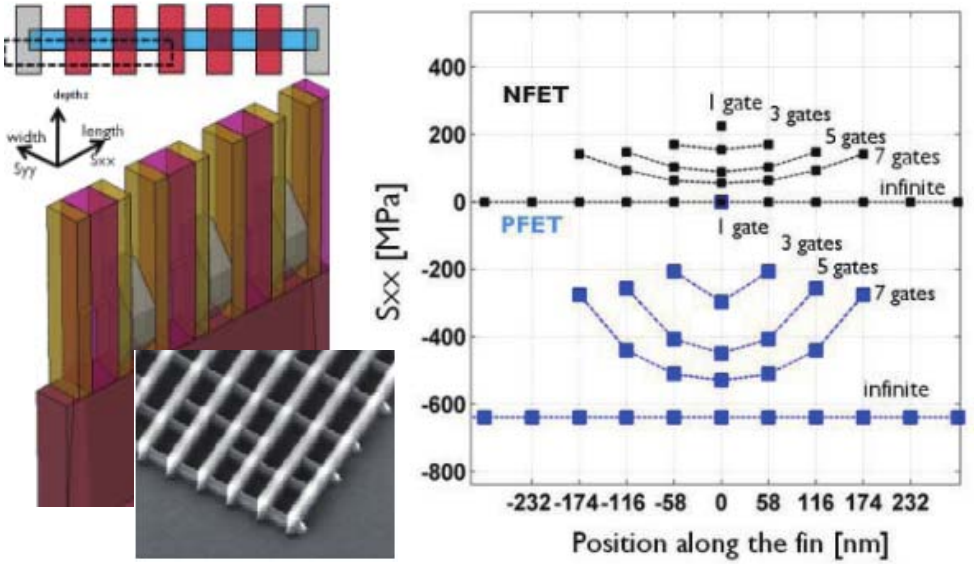


- Topologies of nested and isolated FinFET are unavoidable.
- Mobility of nested FinFET will be enhanced by ~80%.
- Stress of isolated FinFET is almost relaxed.

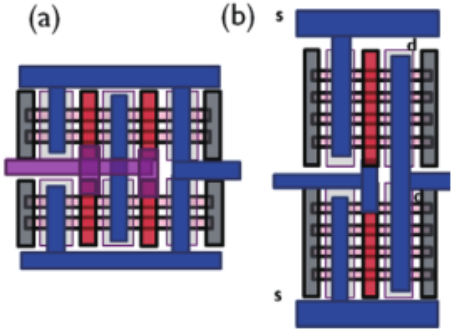
M. Choi, ISTDM (2012)

Strained FinFET Inverter Performance

stress profiles from a nested FinFET



CMOS Inverter performance benchmark



Inverter Layout		STI comp. – 1 GPa	STI tensile 1 GPa
(a)	2 gates 2 fins	reference	+6.15 %
(b)	1 gate 4 fins	- 4.69 %	- 5.14 %

- PMOS stress (induced by eSiGe) boosts with fin length and # of gates per fin and degrades with increasing fin pitch.
- NMOS stress (induced by tensile STI) boosts with increasing fin pitch, and degrades with increasing # of gates per fin.
- For a CMOS invertor, the best configuration comes from a multiple-gate yet moderate fin-pitch design.

M. G. Bardon, VLSI-T (2013)

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