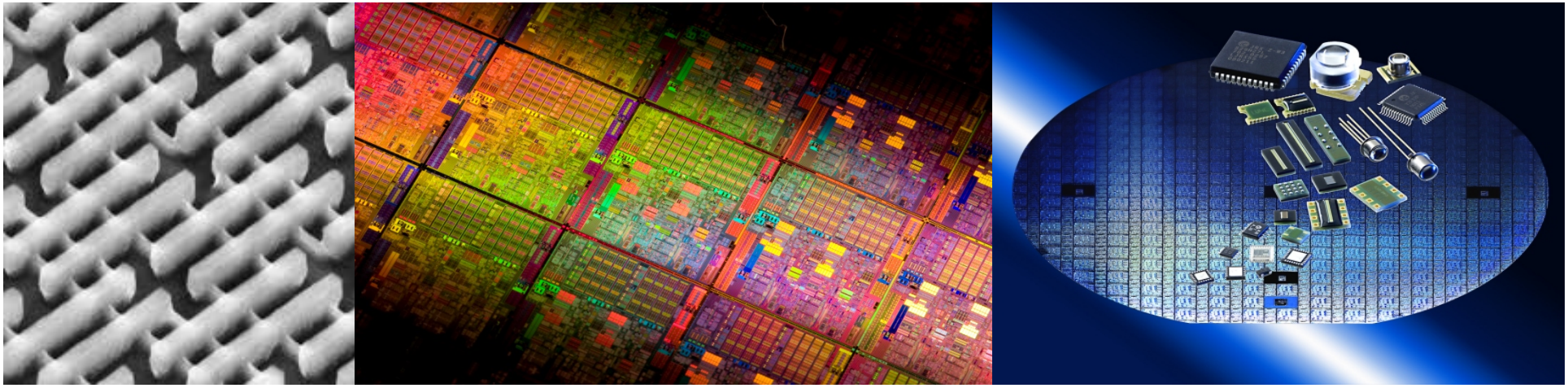
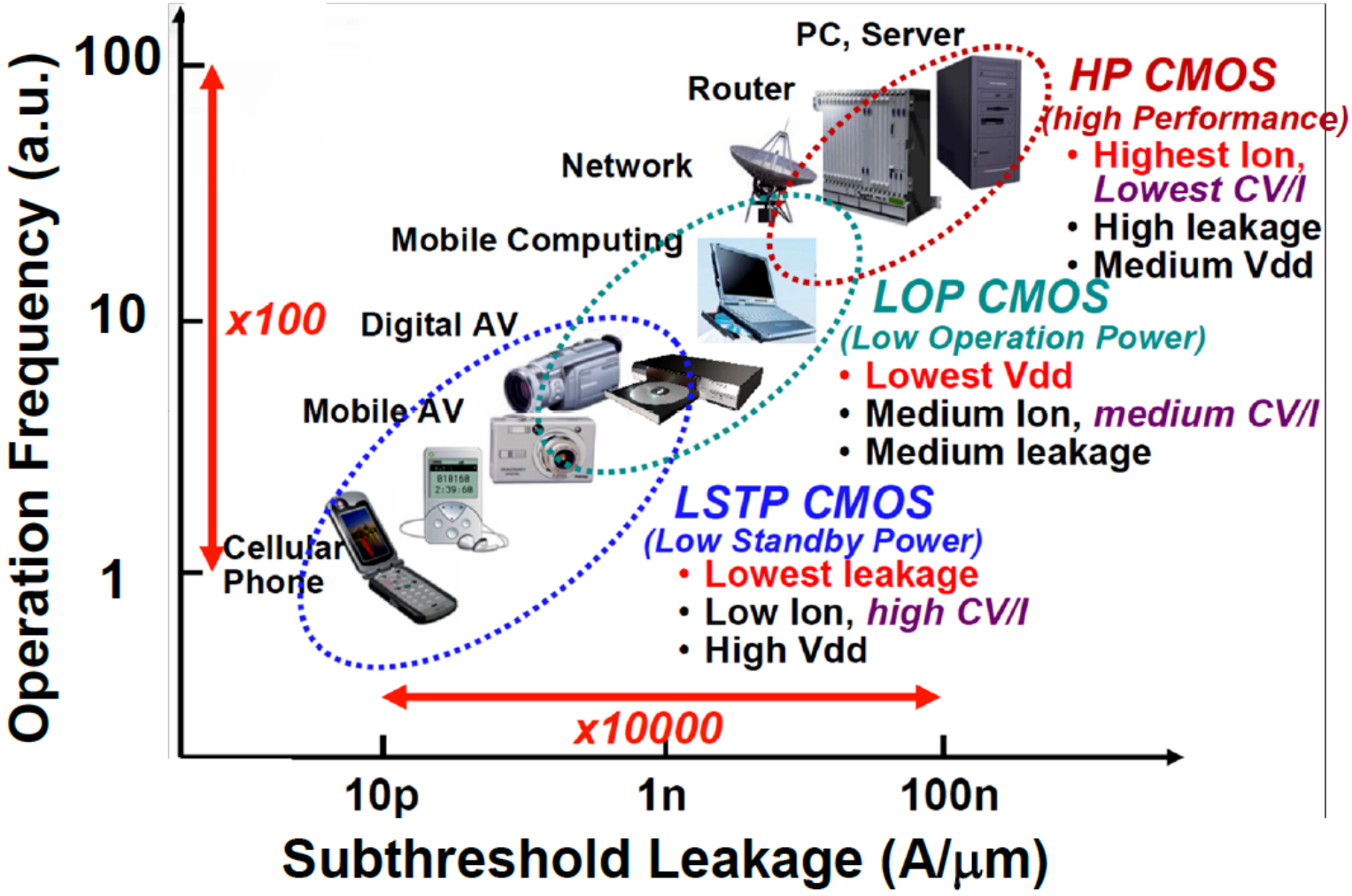


Lecture 15

- Advanced Technology Platforms
  - Background and Trends
  - State-of-the-Art CMOS Platforms

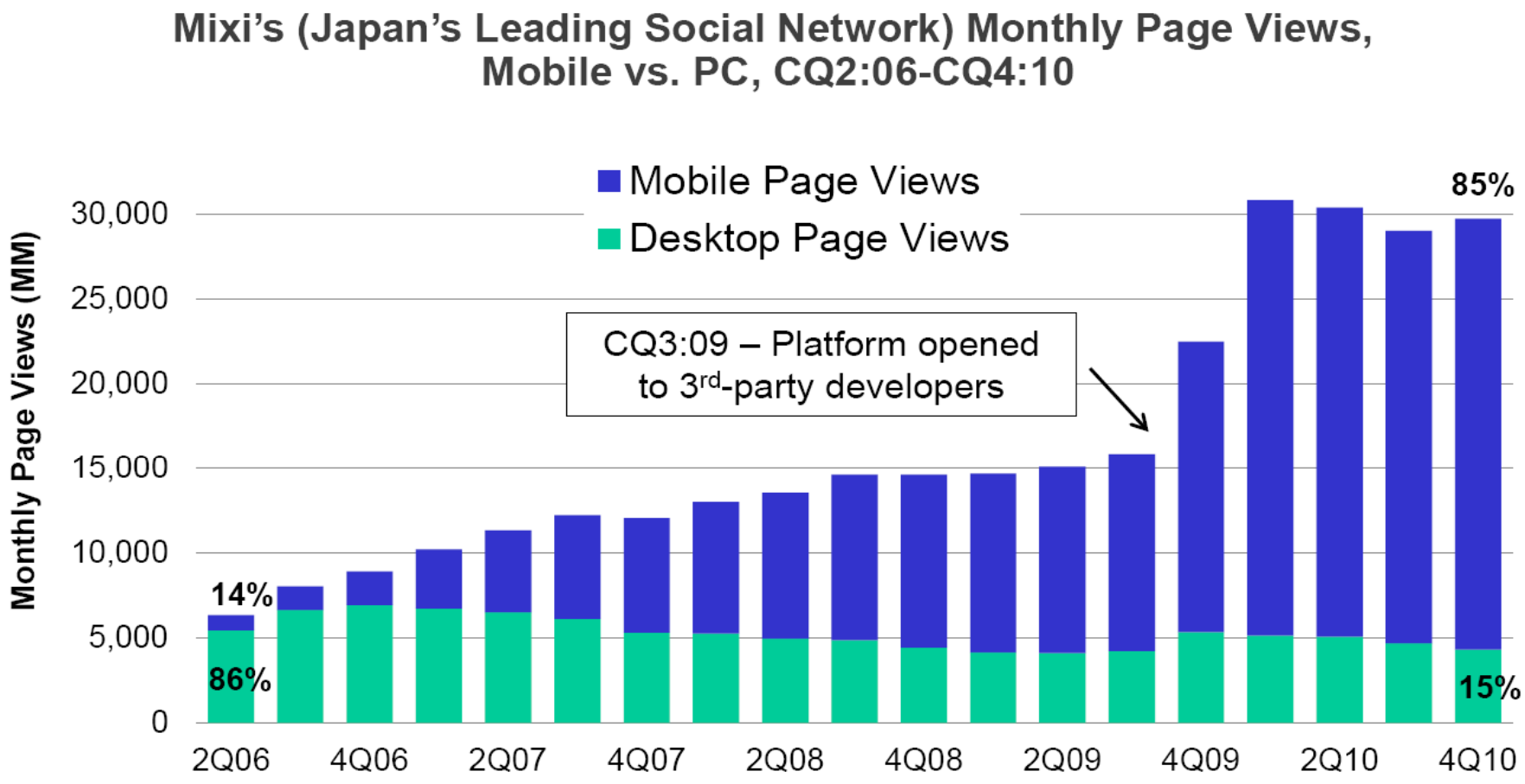
Reading: multiple research articles (reference list at the end of this lecture)

Technology and Applications



Source: 2007 ITRS Winter Public Conf.

Evolution of the Mainstream Computing Media



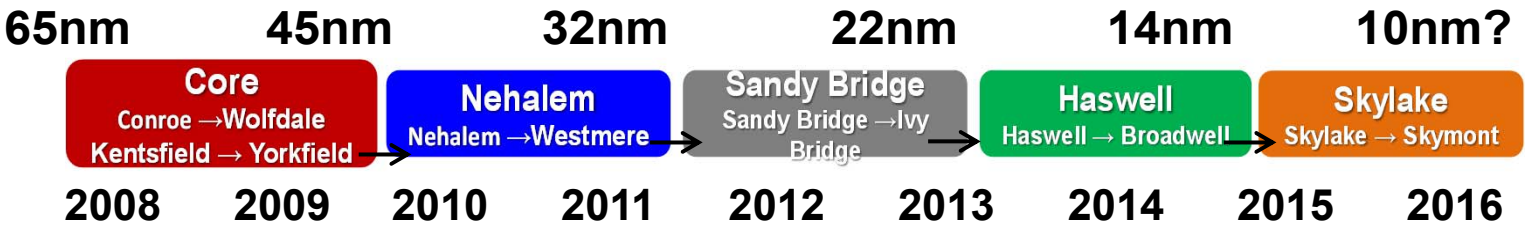
Note: Mixi is one of Japan's leading social networking sites on PC and mobile with 20MM registered users as of 12/31/10. It monetizes mobile usage via sales of avatars, customized homepages and other premium services.
Source: Company reports, Naoshi Nema, Morgan Stanley Research

http://www.slideshare.net/kleinerperkins/kpcb-top-10-mobile-trends-feb-2011

Microarchitecture Trends

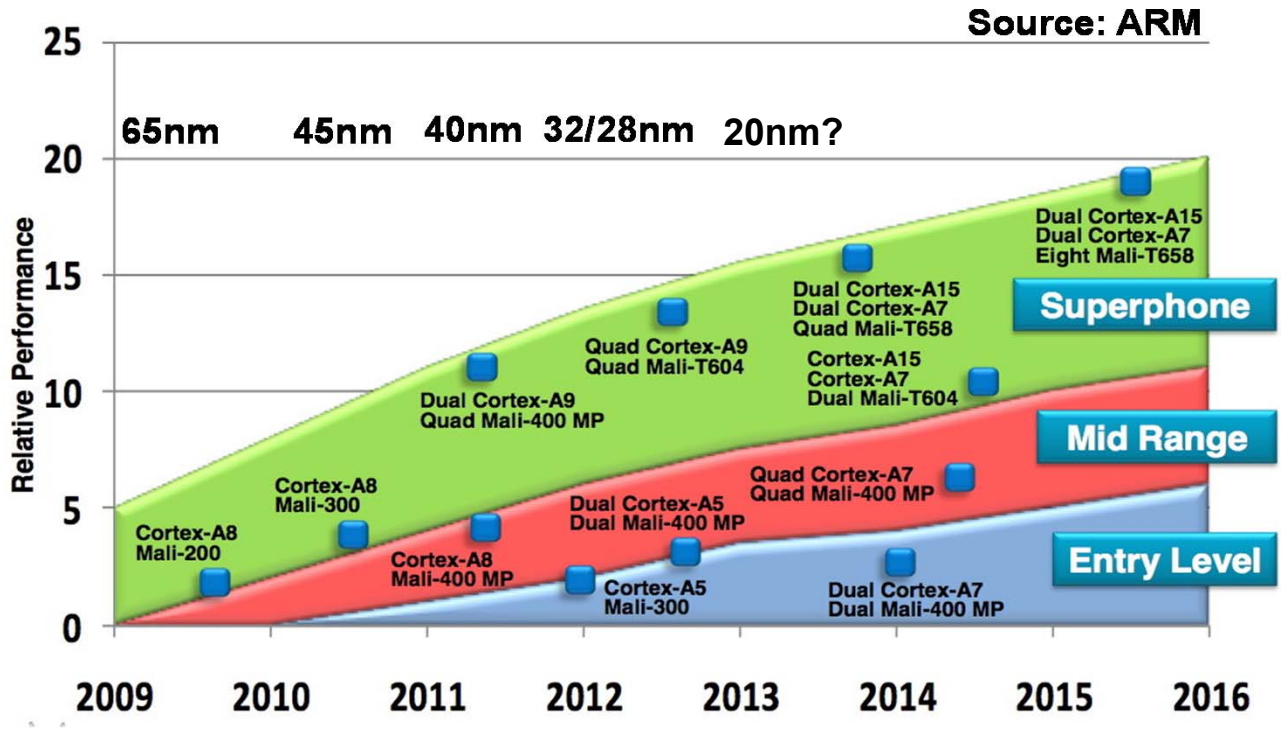
PC/Server:

Source: Intel



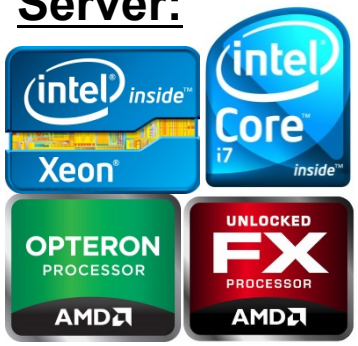
Mobile:

Source: ARM



State-of-the-Art MPUs

Server: **PC:**



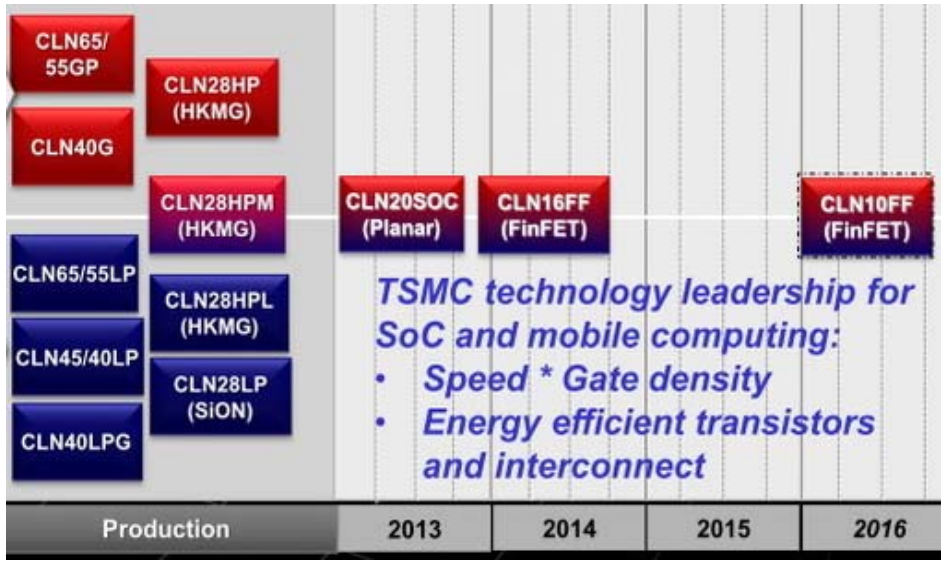
Mobile:

Qualcomm snapdragon

Samsung Exynos PROCESSOR

Processor	Architecture	Technology	Foundry	Frequency
Xeon E5	Ivy Bridge	22nm TriGate	Intel	2.5-3.6 GHz
Core i7				1.8-3.0 GHz
Opteron 4200	Piledriver	32nm PDSOI	Global-foundries	1.8-3.3 GHz
FX-8350				2.9-4.2 GHz
A6	ARMv7	32nm	Samsung	1.3 GHz
A7	ARMv8a	28nm	Samsung	1.8 GHz
Tegra 4	Cortex A15	28nm HPL	TSMC	
Tegra 4i	Cortex A9	32nm LP	Samsung	1.7 GHz
Snapdragon 800	Krait 400	28nm LP	TSMC	1.9 GHz
Snapdragon 600	Krait 300	28nm HPM	TSMC	2.3 GHz
Exynos 5 Octa (5410)	Cortex A15	28nm LP	Samsung	1.8 GHz
Exynos 4 Quad (4412)	Cortex A7	32nm LP	Samsung	1.6 GHz

Mobile MPU/SoC Technology Trends



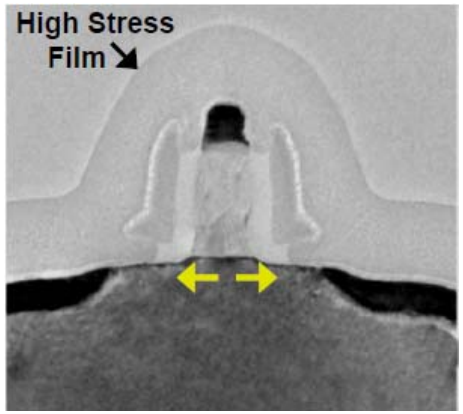
	HP	HPL	HPM	LP
Definition	High Performance	High-Perf Low-Leakage	High-Perf Mobile	Low Power
Applications	High-perf CPUs, GPUs, NPUs, FPGAs	Mobile & fixed embedded processors	Mobile embedded processors	Mobile embedded processors
Geometry	28nm	28nm	28nm	28nm
Substrate	Bulk Si	Bulk Si	Bulk Si	Bulk Si
Gate Type	HKMG	HKMG	HKMG	Poly/SiON
Gate Process	Gate-last	Gate-last	Gate-last	Gate-first
Core Voltage	0.85V	1.0V	0.9V	1.05V
Transistor V_t	4 options	4 options	5 options	2 options
Performance	High	Medium	Highest	Lowest
Leakage	Highest	Lowest	Relatively low	Unimproved
Example Customers	Altera, NetLogic	Xilinx	Undisclosed	Altera, Qualcomm
Risk Production	4Q10	1Q11	4Q11	3Q10
Full Production	3Q11*	4Q11*	3Q12*	2Q11*

Source: TSMC (2012)

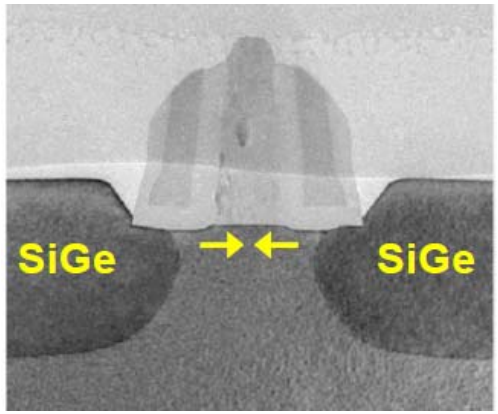
- **Technology (more than V_{TH}) varies for different applications, because of performance specifications and cost purposes.**
- **Due to the process complexity and transistor structural change, future technology nodes will likely introduce small variations for different applications.**

90nm Platforms

NMOS XTEM



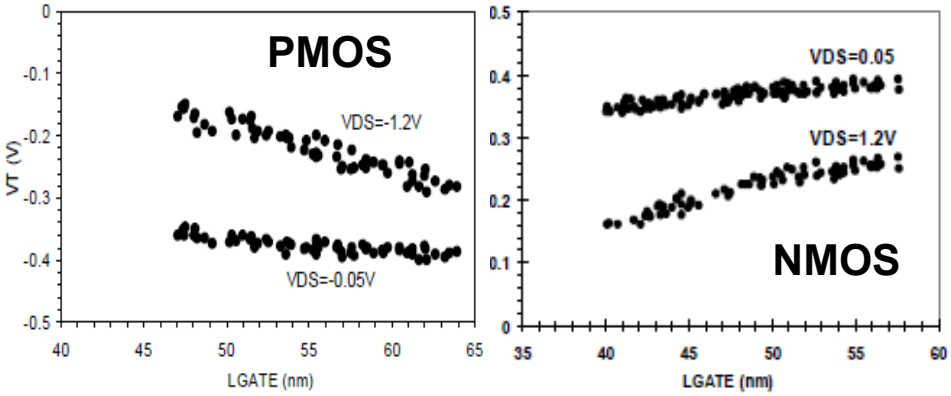
PMOS XTEM



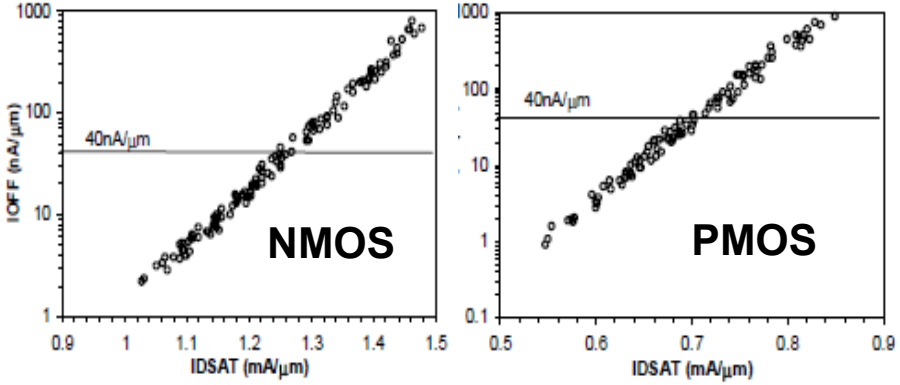
Process Flow

- Shallow Trench Isolation
- Wells & VT Adjust Implants
- Gate Oxide & Poly Patterning
- Tip / Halo Implants & Spacer Formation
- **Si Recess Etch & SiGe S/D Epi Deposition**
- Source Drain Formation & Salicidation

Short Channel Effect



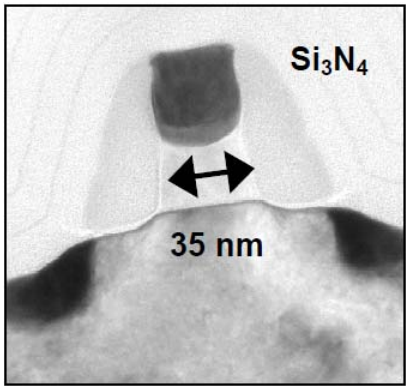
I_{OFF} *vs.* I_{ON} plots



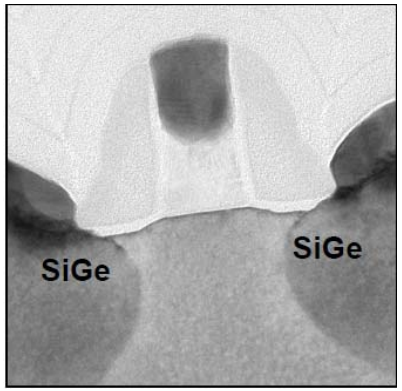
- **Structure: planar bulk**
- **Strained-Si technology: eSiGe for PMOS; sCESL for NMOS**
- **V_{DD} = 1.2V; $L_{g,NMOS}$ = 45nm; $L_{g,PMOS}$ = 50nm**

65nm Platforms

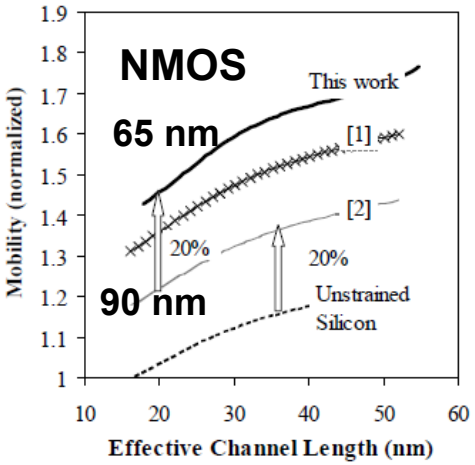
NMOS XTEM

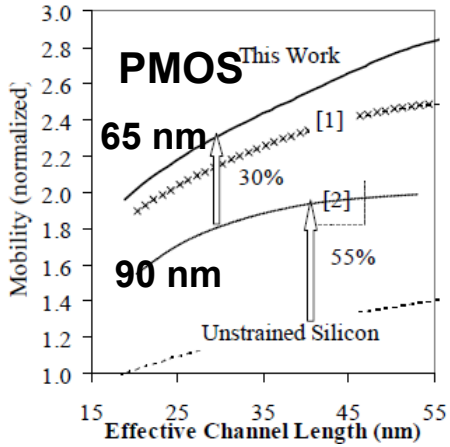


PMOS XTEM

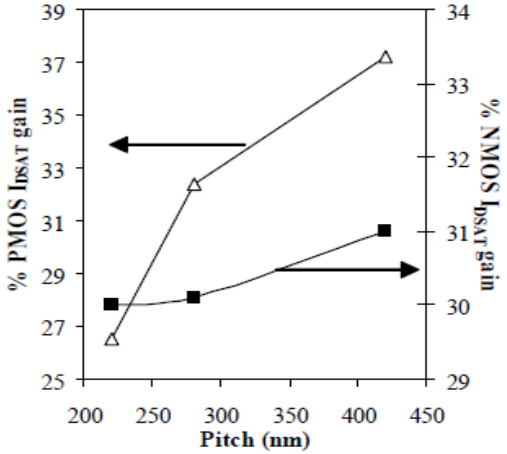


Mobility Enhancement

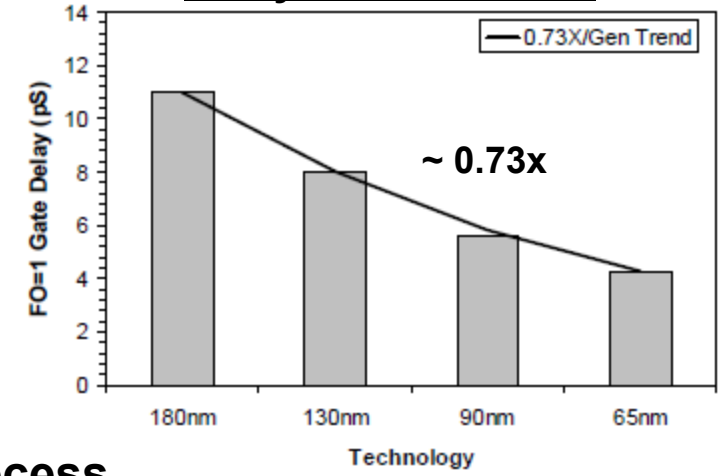




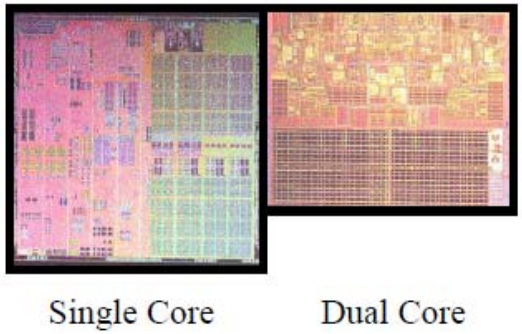
Layout Dependent Stress



Delay *vs.* Tech. Gen.



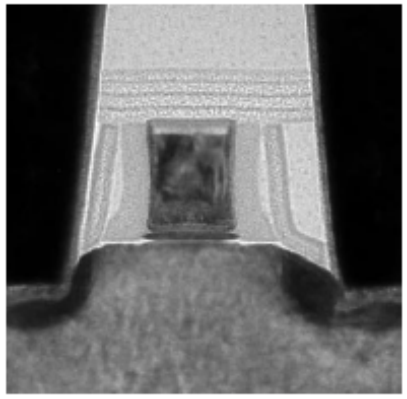
Architecture Innovation



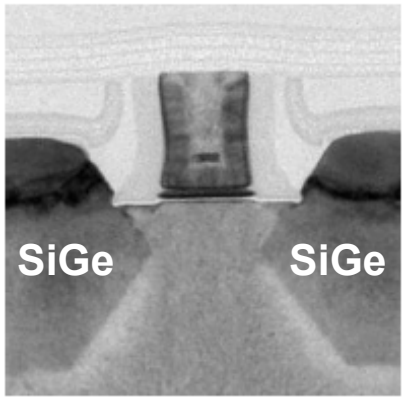
- L_g = 35nm
- Dual-Poly/SiON process

45nm Platforms

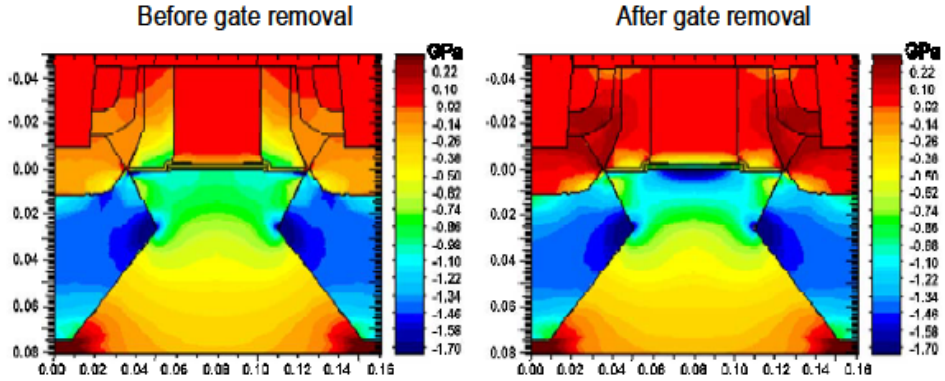
NMOS XTEM



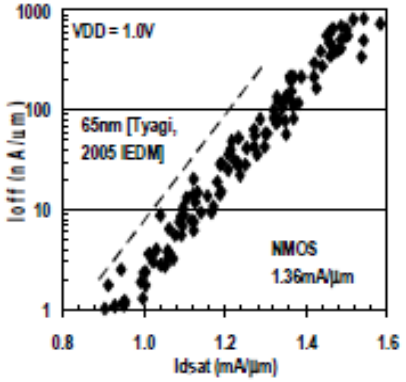
PMOS XTEM

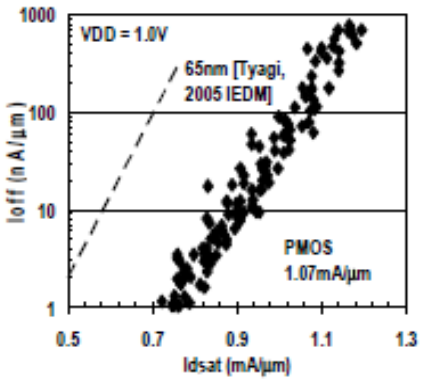


TCAD Simulation of PMOS S_{xx}



I_{OFF} *vs.* I_{ON} plots

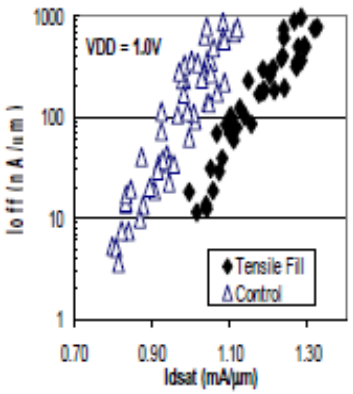


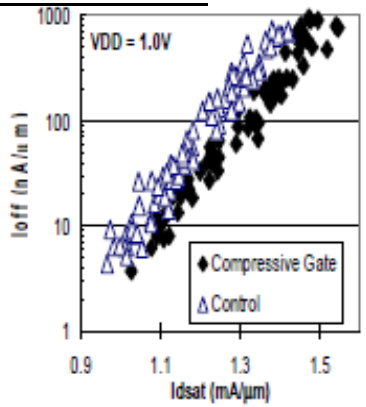


Perf. Improvement over 65nm

Component	Benefit
PMOS Idsat	+13
PMOS Idlin	+18
NMOS Idsat	+3
NMOS Idlin	+2
Cjunction	+2
Cgate/Cov	-8%
Voltage Scaling	-7%
Total	+23%

Tensile Contact & Compressive Gate Stress on NMOS



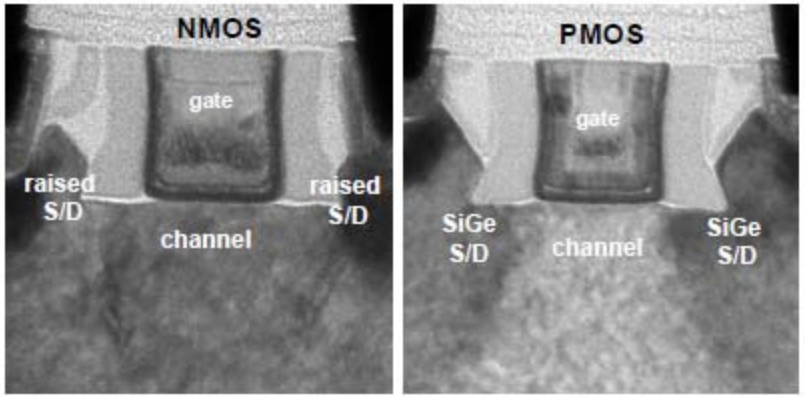


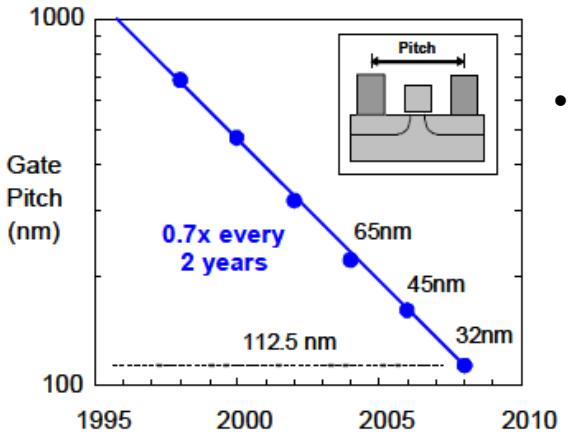
- **Strained-Si technology: eSiGe for PMOS; SMT for NMOS**
- **High-κ First + Metal Gate Last**
- **V_{DD} = 1.0V; $L_{g,HP}$ = 35nm; $L_{g,LP}$ = 45nm**

C. Auth, VLSI-T (2008)
C.-H. Jan, IEDM (2008)

32nm Platforms

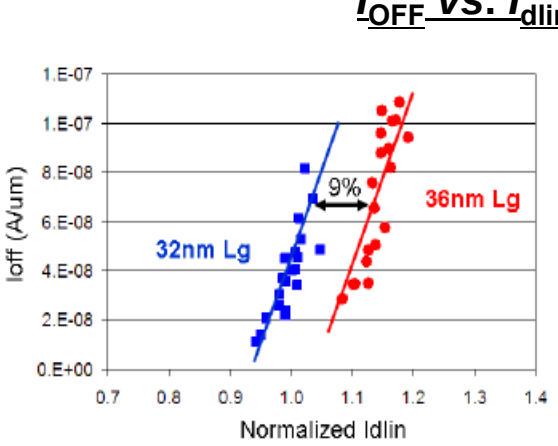
XTEMs

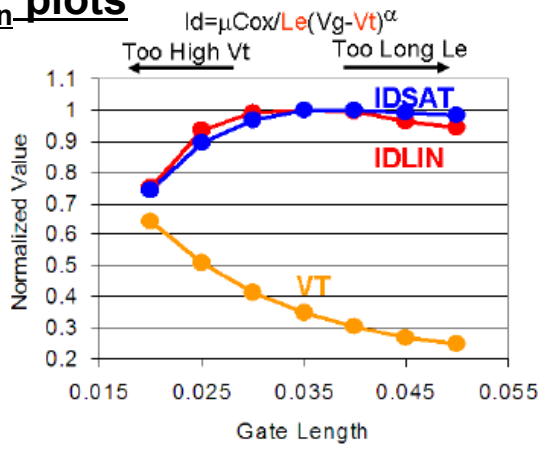


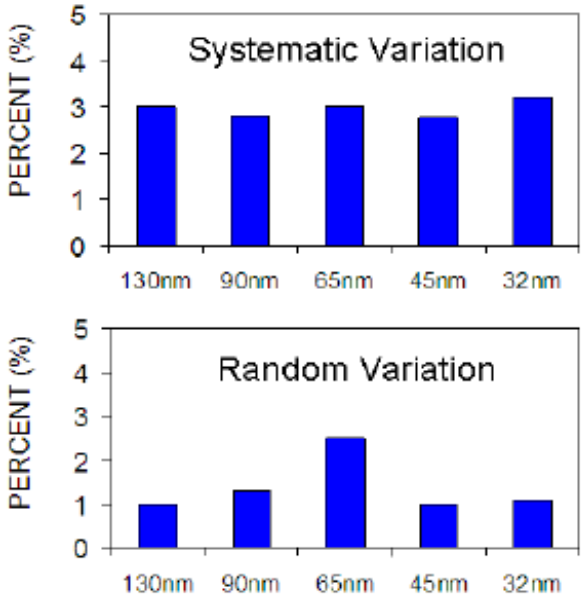


- **Gate pitch scaling can continue for some generations…**

I_{OFF} *vs.* I_{dlin} plots





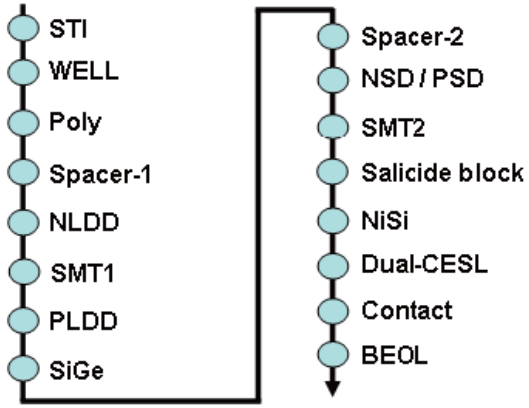


- **Raised Source/Drain**
- **High- κ + Metal Gate Last**
- **$L_{g,HP}$ = 36nm, the performance benefit by reducing L_g stops from this node.**

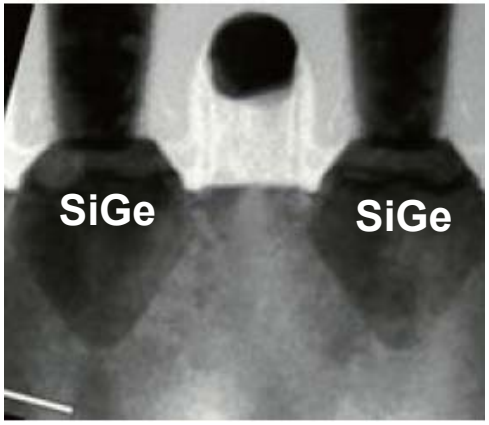
P. Packan, IEDM (2009)

28nm Foundry Platforms

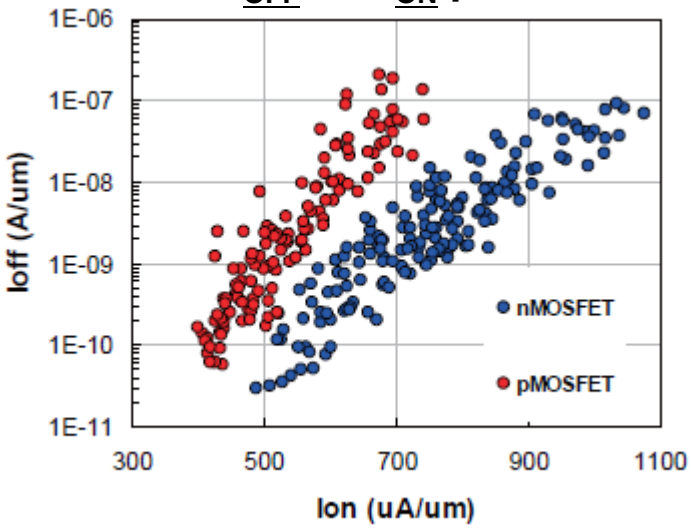
Process Flow



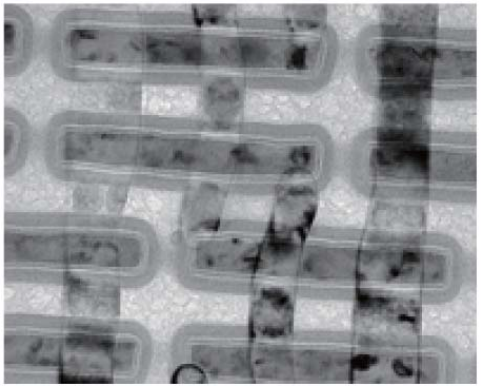
PMOS XTEM



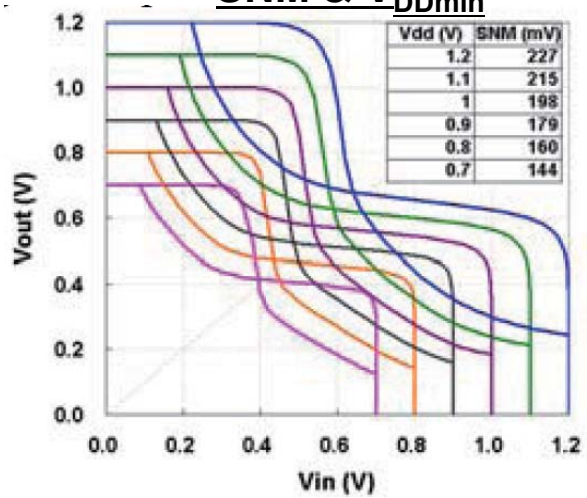
I_{OFF} *vs.* I_{ON} plots



6T SRAM SEM



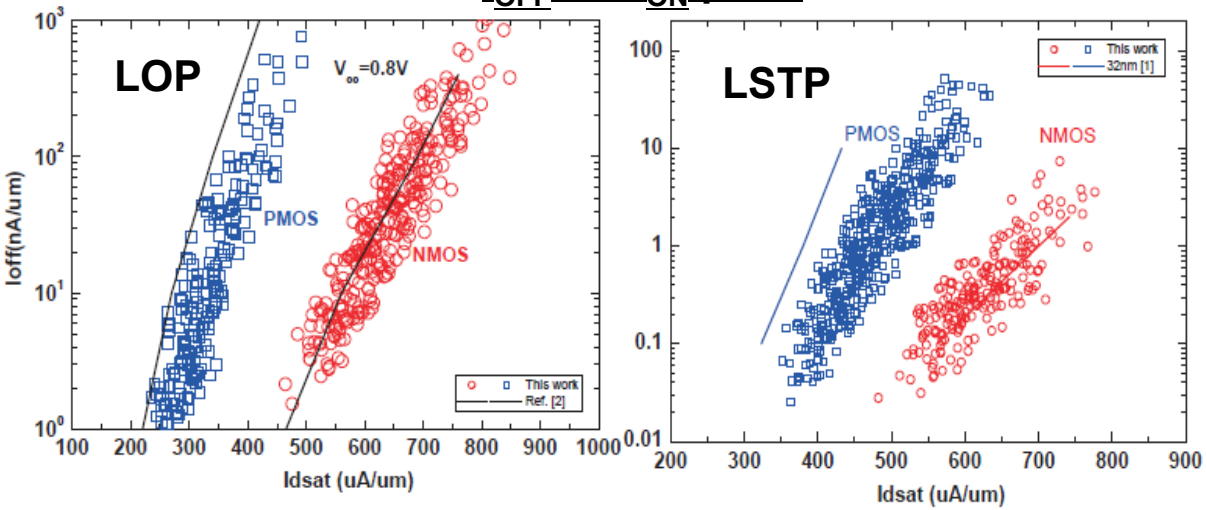
SNM & V_{DDmin}



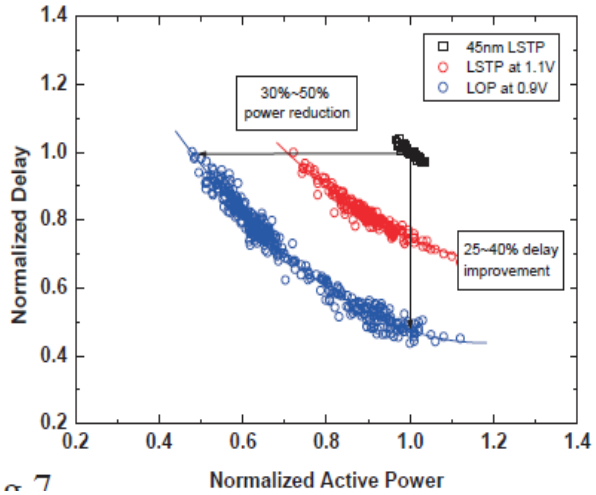
- Poly Si/SiON gate stack → EOT_{elec} = 1.93nm
- tCESL+SMT for NMOS; eSiGe for PMOS
- V_{DD} = 1.0/0.7V
- Cu/Ultra Low-κ (2.5)/11 MLs for BEOL
- w/o HKMG → Low Cost + High Yield

28nm Foundry Platforms (Cont'd)

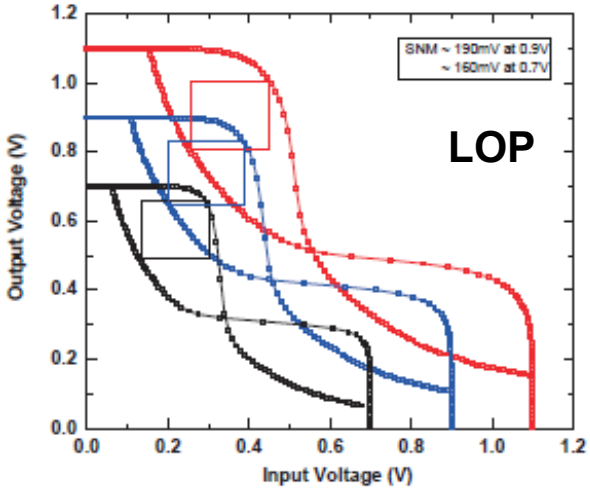
I_{OFF} *vs.* I_{ON} plots

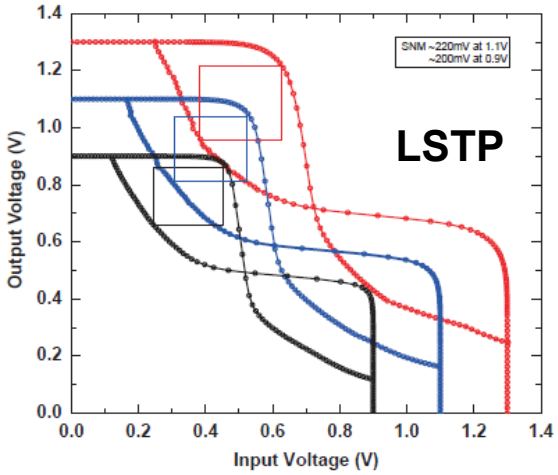


Delay *vs.* Power plots



SRAM SNM

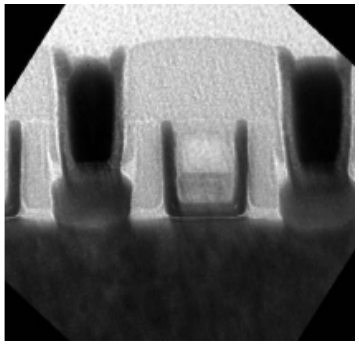




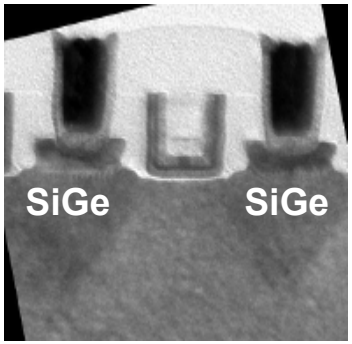
- LOP and LSTP can be achieved by V_{TH} tuning
- $V_{DD,LSTP}$ = 1.1 V; $V_{DD,LOP}$ = 0.8V
- almost comparable performance to 32nm HKMG
- Improved BEOL process: Cu/ULK, MIM, Inductors…

20nm Bulk Platform

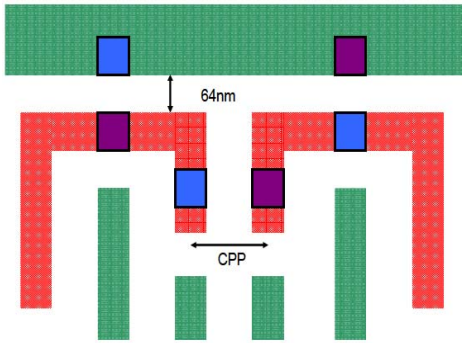
NMOS XTEM



PMOS XTEM

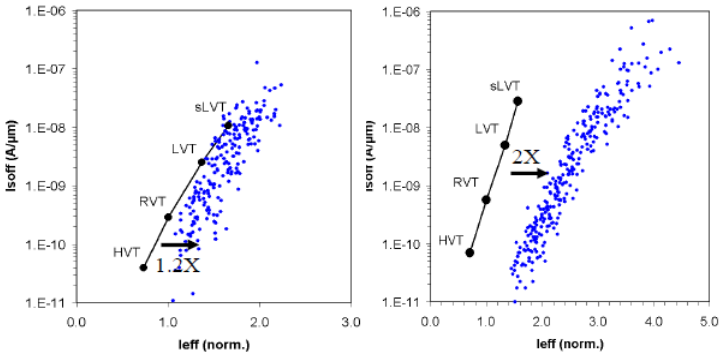


Double-Patterning enabled Pitch Scaling



Design	28LP	20LPM
Lgate (nm)	30	20
Contacted Poly Pitch (CPP)	114	86
Gate Contact pitch (nm)	114	86
Active Contact Pitch (nm)		86
N+/P+ (nm)	70	52
V0 pitch (nm)	NA	84
M1 (nm)	90	64
standard library cell size	1X	0.55X

I_{OFF} vs. I_{EFF} plots

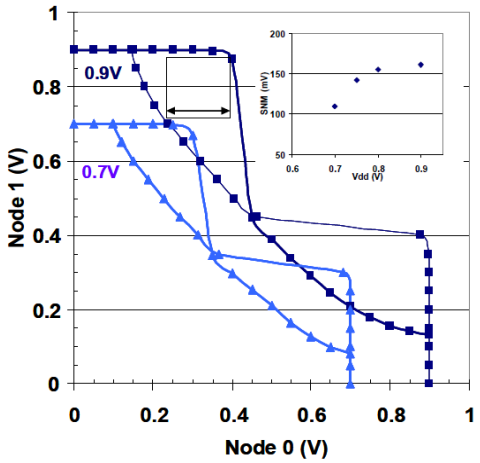


Technology Flavors

	Core SG				
	HVT	RVT	LVT	sLVT	uLVT
Vdd (V)	0.9				
Ldesign (nm)	34	20			
CPP (nm)	100	86			
Ioff (nA/um)	0.07	0.6	6	60	200

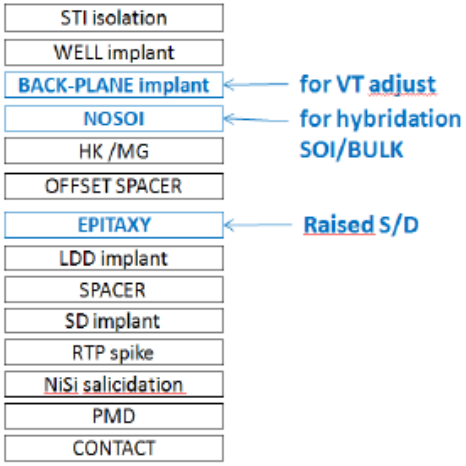
	IO EG		
Vdd (V)	1.2V	1.5V	1.8V
Lgate (nm)	70	100	150
CPP (nm)	170	200	270
Ioff (nA/um)	6/2	0.13/0.075	0.013/0.003

SRAM SNM

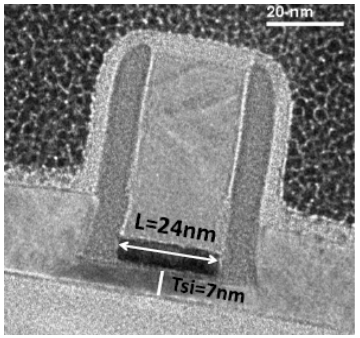


- High-κ + Metal Gate Last
- Strain: eSiGe for PMOS, no stressors for NMOS
- Speed Improvement: 30% faster for LP, 15% faster for HP than 28nm node

28nm UTBB FDSOI Platform

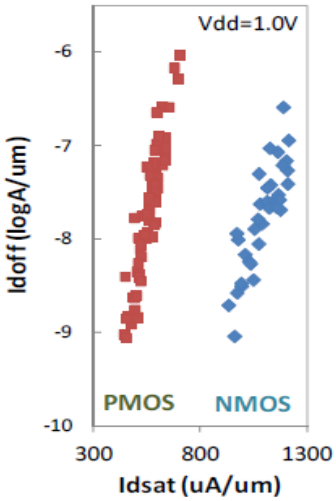


XTEM

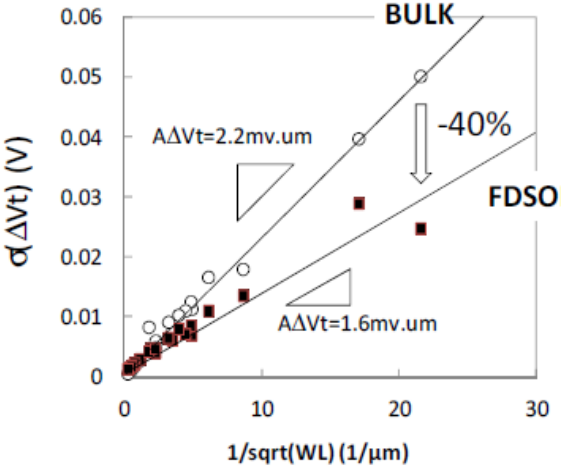


L_g=40nm for SRAM

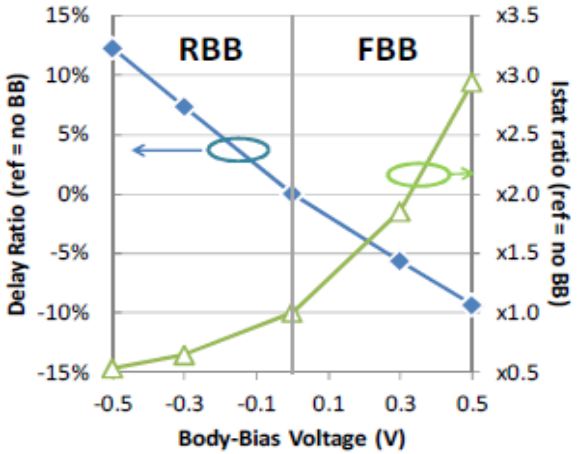
***I_{OFF} vs. I_{ON}* plots**



***Pelgrom* plots**



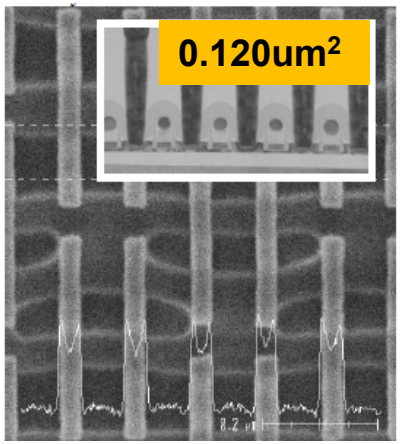
Back Biasing



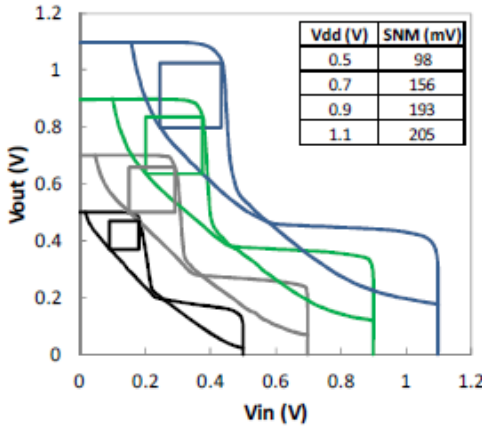
- 12nm-Si/25nm-BOX SOI wafer; Final t_{SOI}=7nm
- HKMG First, T_{inv}=1.5(1.65)nm
- Doped GP, causing a splitting of 2 V_{TH} (RVT, LVT); Dynamic V_{TH} by FBB/RBB?
- No HALO doping
- N(P)MOS: I_{ON}=1070(610)uA/um; I_{OFF}=16(30)nA/um DIBL=90-95mV; SS=85-90mV/dec @1V V_{DD}

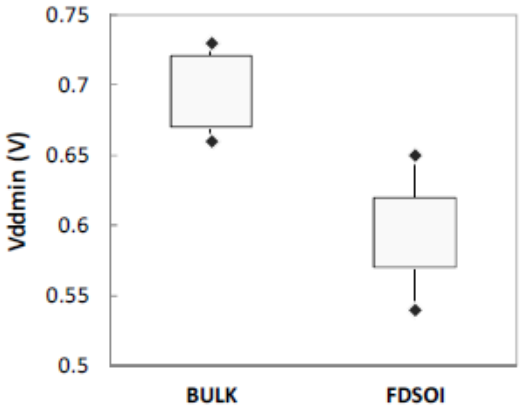
28nm UTBB FDSOI Platform (Cont'd)

6T SRAM cell



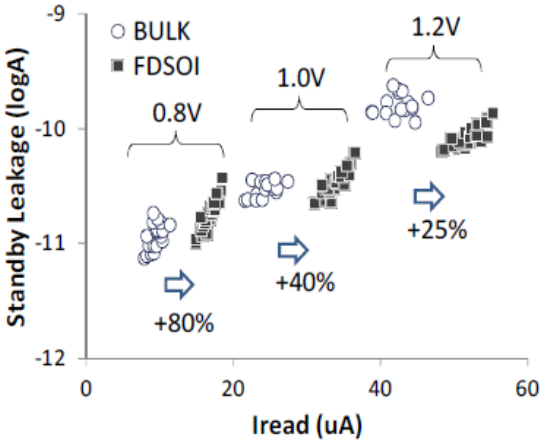
Static Noise Margin & $V_{DD,min}$





- SRAM V_{DDmin} improves by 0.1V
- SRAM read speed largely improved: same leakage, 2x faster!

I_{leak} *vs.* I_{read} for SRAM cells



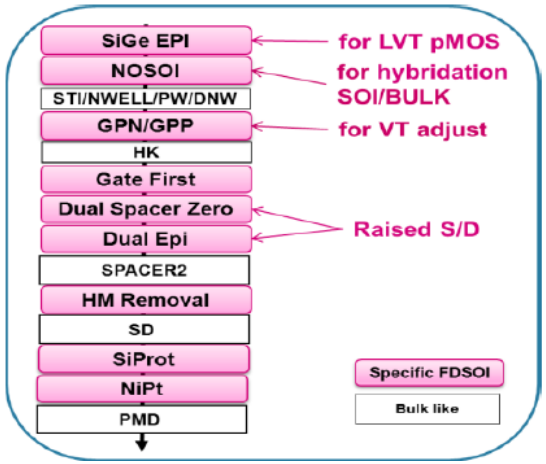
N. Planes, VLSI-T (2012)

Source: Wikipedia

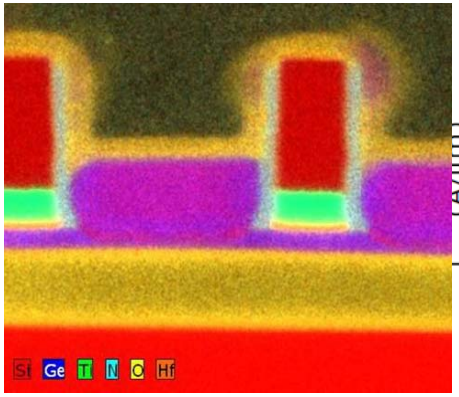
Model Number	Semiconductor technology	CPU Instruction Set	CPU	GPU	Memory Technology	Wireless Radio Technologies	Availability
Nova A9500[16]	45 nm	ARMv7	1.2 GHz Dual-core ARM Cortex-A9	ARM Mali 400 MP	LP-DDR2	None	2011
NovaThor L9540[22]	32 nm	ARMv7	1.85 GHz Dual-core ARM Cortex-A9	PowerVR SGX 544	Dual-channel LP-DDR2	LTE FDD/TDD, HSPA+, TD-SCDMA, EDGE (external Thor M7400 modem)	Cancelled
NovaThor L8540[23]	28 nm	ARMv7	1.85 GHz Dual-core ARM Cortex-A9	PowerVR SGX 544 @ 500 MHz[24]	Dual-channel LP-DDR2	LTE FDD/TDD, HSPA+, TD-SCDMA, EDGE (integrated modem)	Cancelled
NovaThor L8580 (eQuad+)[25]	28 nm FD-SOI	ARMv7	2.5-3.0GHz Quad-core ARM Cortex-A9	PowerVR SGX 544 @600 MHz	Dual-channel LP-DDR2	LTE FDD/TDD, HSPA+, TD-SCDMA, EDGE (integrated modem)	Cancelled

20nm UTBB FDSOI?

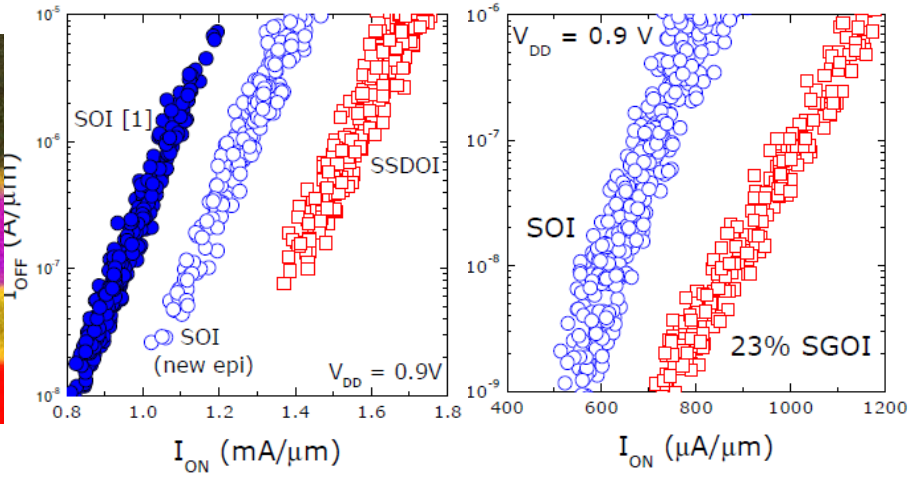
20nm FD process wrt 20nm bulk process



Chemical analysis of 20nm FD-PFET



NFET and PFET Current Enhancement

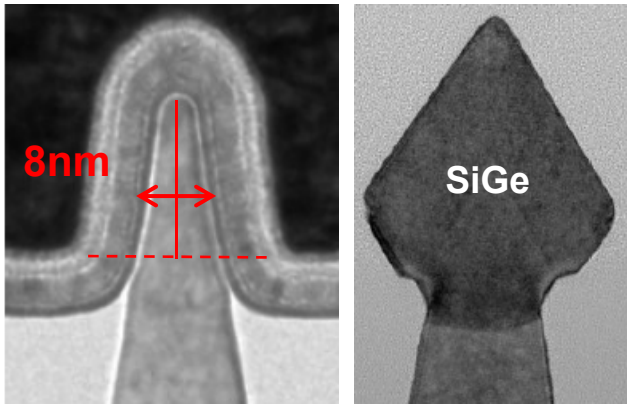


- **20nm FDSOI development goal: 30%** performance boost over bulk reference
  This comes from: 8-12% parasite capacitance; 4-6% *SS* and 8-10% I_{EFF} improvement.
- **Biggest difference compared to ST's 28nm FD:**
  - **Low V_{TH} FDSOI-PFET uses 27%Ge-SiGe channel**, (epi SiGe on top of SOI, then oxidize) → a V_{TH} lowering of 200mV can be achieved.
  - BOX thickness reduces from 25nm to 20nm.
  - NFET: in-situ P-doped S&D;
  - No LDD, pocket, HALO, HDD implants used

M. Haond, Int SOI Conf. (2012)

22nm FinFET Platforms

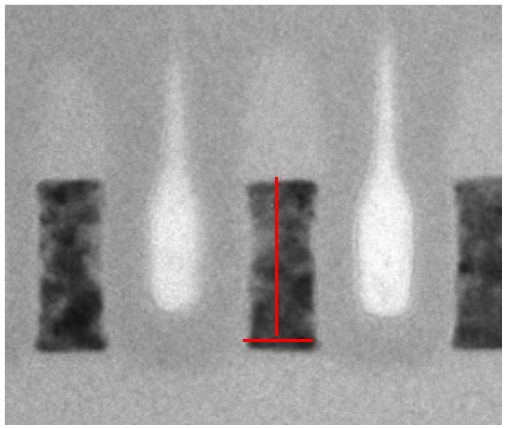
Intel 22nm Tri-Gate



- L_g=30nm
- CPP 90nm
- Bulk Si substrate
- Fin aspect ratio: 2:1
- HKMG Last

C. Auth, VLSI (2012)

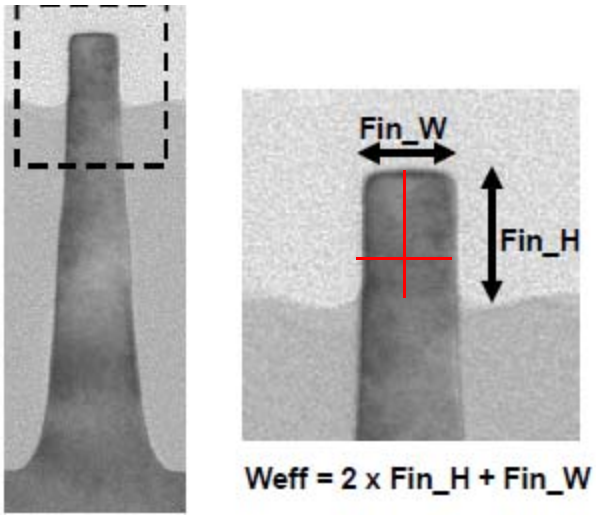
IBM 22nm FinFET



- L_g=25nm
- CPP 100nm
- Gate Pit. 80-100nm
- SOI substrate
- Fin aspect ratio: 2.3:1
- HKMG First

V.S. Basker, VLSI (2010)

TSMC 22nm FinFET



- L_g=25nm
- Bulk Si substrate
- Fin aspect ratio: <2:1
- HKMG Last ?

C.C. Wu, IEDM (2010)

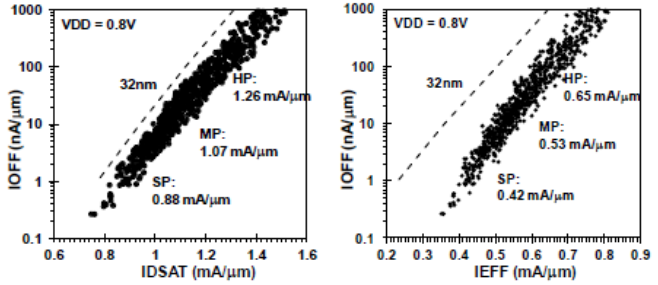
22nm FinFET Performance

@I_{OFF} of 100nA/um

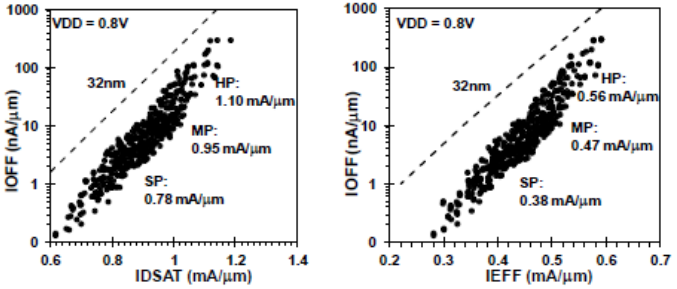
Intel 22nm Tri-Gate

VLSI 2012

NMOS



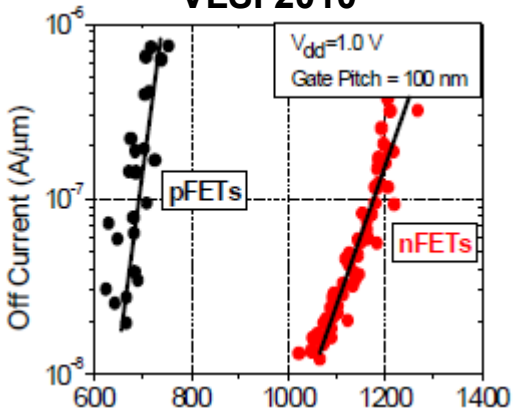
PMOS



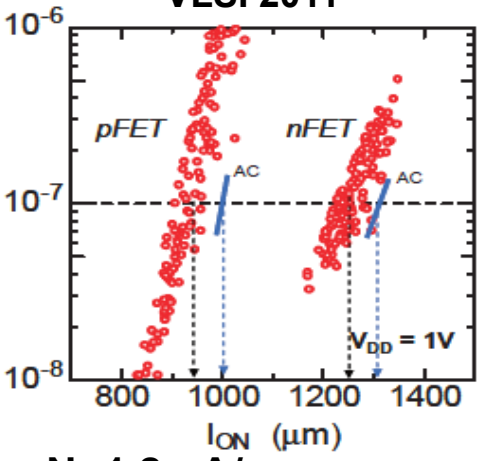
N: 1.26mA/um
P: 1.10mA/um
@ 0.8V V_{DD}

IBM 22nm FinFET

VLSI 2010



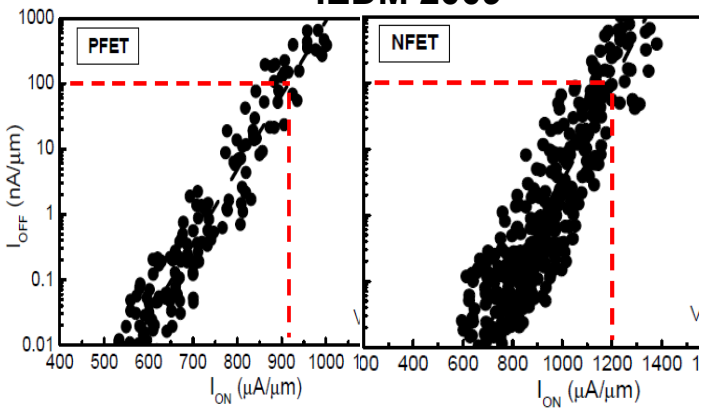
VLSI 2011



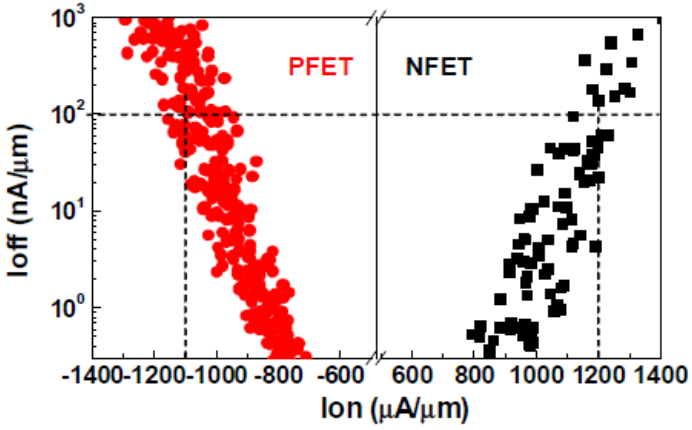
N: 1.2mA/um
P: 950uA/um
@ 1V V_{DD}

TSMC 22nm FinFET

IEDM 2009



IEDM 2010



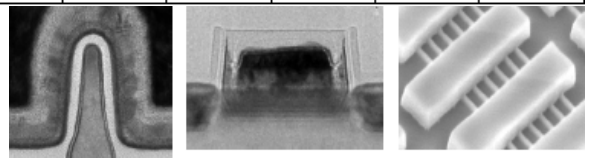
N: 1.2mA/um
P: 1.1mA/um
@ 1V V_{DD}

22nm Bulk FinFET: to Probe Further

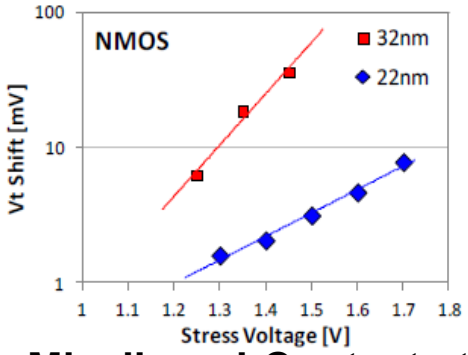
Technology Flavors

Transistor Type	High Speed Logic		Low Power Logic		High Voltage	
Options	High Performance (HP)	Standard Perf./ Power (SP)	Low Power (LP)	Ultra Low Power (ULP)	1.8 V	3.3 V
Vdd (Volt)	0.75 / 1	0.75 / 1	0.75 / 1	0.75/1.2	1.5/1.8/3.3	3.3 / >5
Gate Pitch (nm)	90	90	90	108	min. 180	min. 450
Lgate (nm)	30	34	34	40	min. 80	min. 280
N/PMOS Idsat/Ioff (mA/um)	1.08/ 0.91 @ 0.75 V, 100 nA/um	0.71 / 0.59 @ 0.75 V, 1 nA/um	0.41 / 0.37 @ 0.75 V 30 pA/um	0.35 / 0.33 @ 0.75 V 15 pA/um	0.92 / 0.8 @ 1.8 V 10 pA/um	1.0 / 0.85 @ 3.3 V 10 pA/um

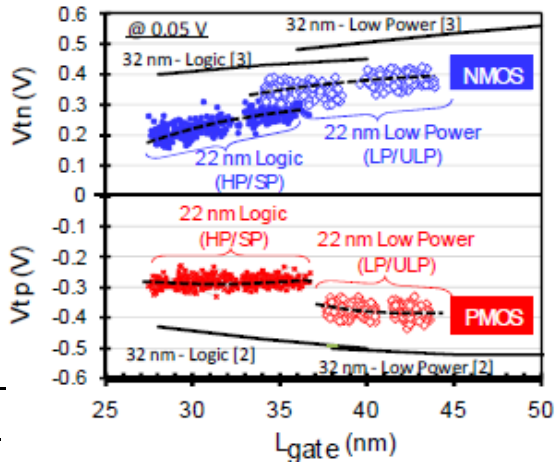
I/O Devices



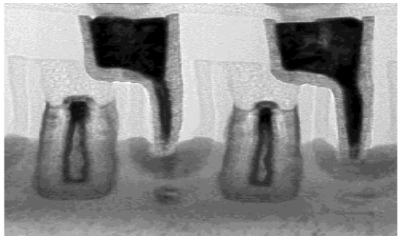
NMOS PBTI Improvement



Short-Channel Effect



Misaligned-Contacts to avoid Gate/SD Shorting

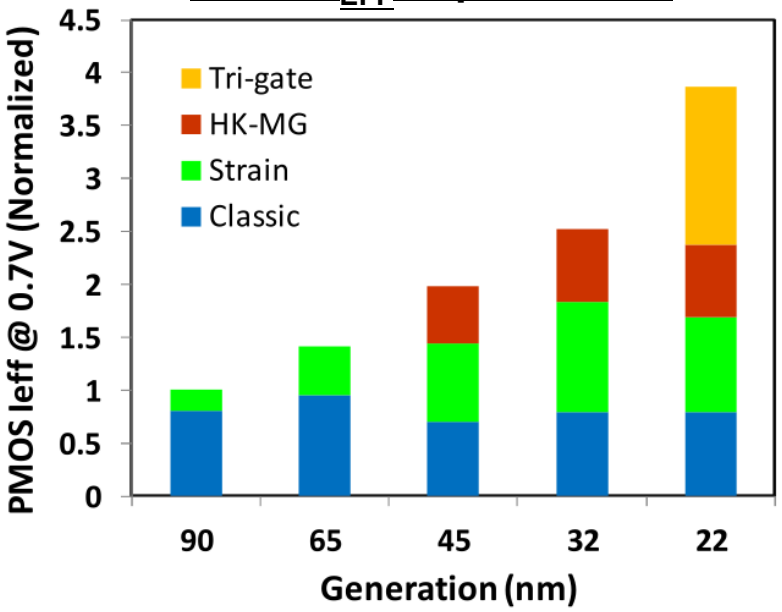


- Almost idea electrostatics: N(P) FET
  - DIBL=46(50) mV/V;
  - SS=69(72) mV/dec; @0.8V V_{DD}
- Threshold voltage engineering by tuning L_g + doping
- 193nm Immersion litho. to achieve 8nm Fin width, corner rounding (3.5nm radius)
- 5th-gen strained-Si tech: $Si_{0.5}Ge_{0.5}$ S/D + Gate-Last for PFET; "some technique" for NFET
- Misalignment at CESL to form contacts; contact wrap around the fin
- 9-layer Cu interconnect; MIM introduced between M8 & M9

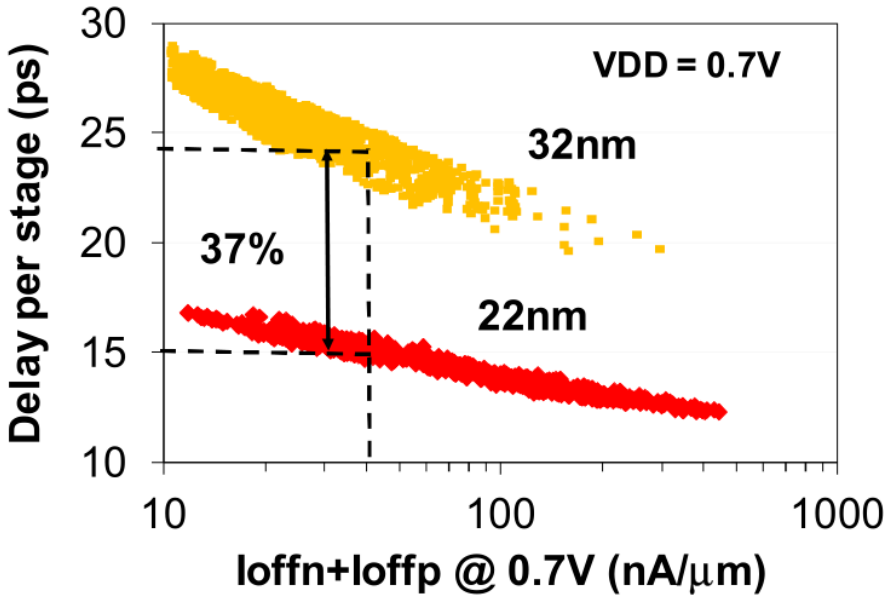
C. Auth, VLSI-T (2012)
C.-H. Jan, IEDM (2012)

Improvement over 32nm Planar Platforms

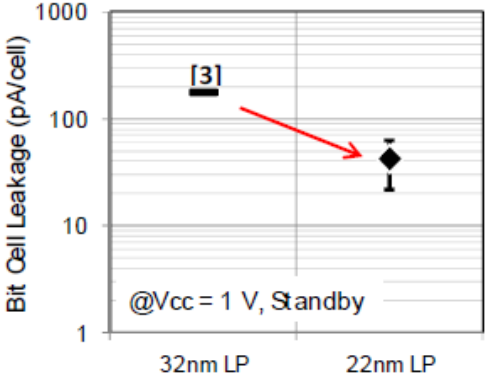
PMOS I_{EFF} Improvement

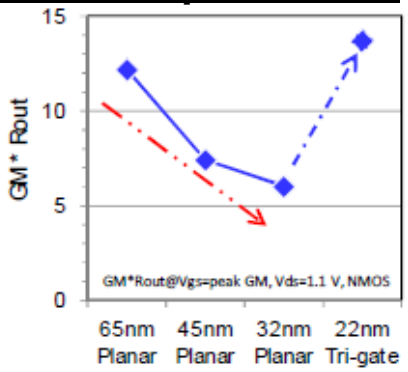


Delay *vs.* Power plots



SRAM Power & Intrinsic Gain Improvement





- **As compared to precedent planar platforms, most of the performance enhancement comes from electrostatics improvement!**

C.-H. Jan, IEDM (2012)
K. Kuhn, IEDM (2012)

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3. (Intel 45nm) C. Auth *et al*., "45nm High-k+Metal Gate Strain-Enhanced Transistors," *Symposium on VLSI Technology Dig*., pp.128-129, 2008.
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7. (IBM 20nm Bulk) H. Shang *et al*., "High Performance Bulk Planar 20nm CMOS Technology for Low Power Mobile Applications," *Symposium on VLSI Technology Digest*, pp. 129-130, 2012.
8. (ST 28nm FDSOI) N. Planes *et al*., "28nm FDSOI Technology Platform for High-Speed Low-Voltage Digital Applications," *Symp. VLSI Tech. Dig*., pp. 133-134, 2012.
9. (ST 20nm FDSOI) M. Haond *et al*., "20 nm FDSOI Process and Design Platforms for High Performance/Low Power Systems on Chip," *IEEE International SOI Conference*, 2012.
10. (Intel 22nm Fin) C. Auth *et al*., "A 22nm High Performance and Low-Power CMOS Technology Featuring Fully-Depleted Tri-Gate Transistors, Self-Aligned Contacts and High Density MIM Capacitors," *Symposium on VLSI Technology Dig*., pp. 131-132, 2012.

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11. C.-H. Jan *et al*., "A 22nm SoC Platform Technology Featuring 3-D Tri-Gate and High-k/Metal Gate, Optimized for Ultra Low Power, High Performance and High Density SoC Applications," *IEEE International Electron Device Meeting Tech. Dig*., pp.44-47, 2012.
12. K. Kuhn *et al*., "The Ultimate CMOS Device and Beyond," *IEEE International Electron Device Meeting Tech. Dig*., pp. 171-174, 2012.
13. (IBM 22nm Fin) V.S. Basker *et al*., "A 0.063um^2 FinFET SRAM Cell Demonstration with Conventional Lithography using a Novel Integration Scheme with Aggressively Scaled Fin and Gate Pitch," *Symposium on VLSI Technology Dig*., pp.19-20, 2010.
14. (TSMC 22nm Fin) C.C. Wu *et al*., "High Performance 22/20nm FinFET CMOS Devices with Advanced High-κ/Metal Gate Scheme," *IEEE International Electron Device Meeting Tech. Dig*., pp.600-603, 2010.