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Lessons Learned from Early Microelectronics Production at Sandia National Laboratories

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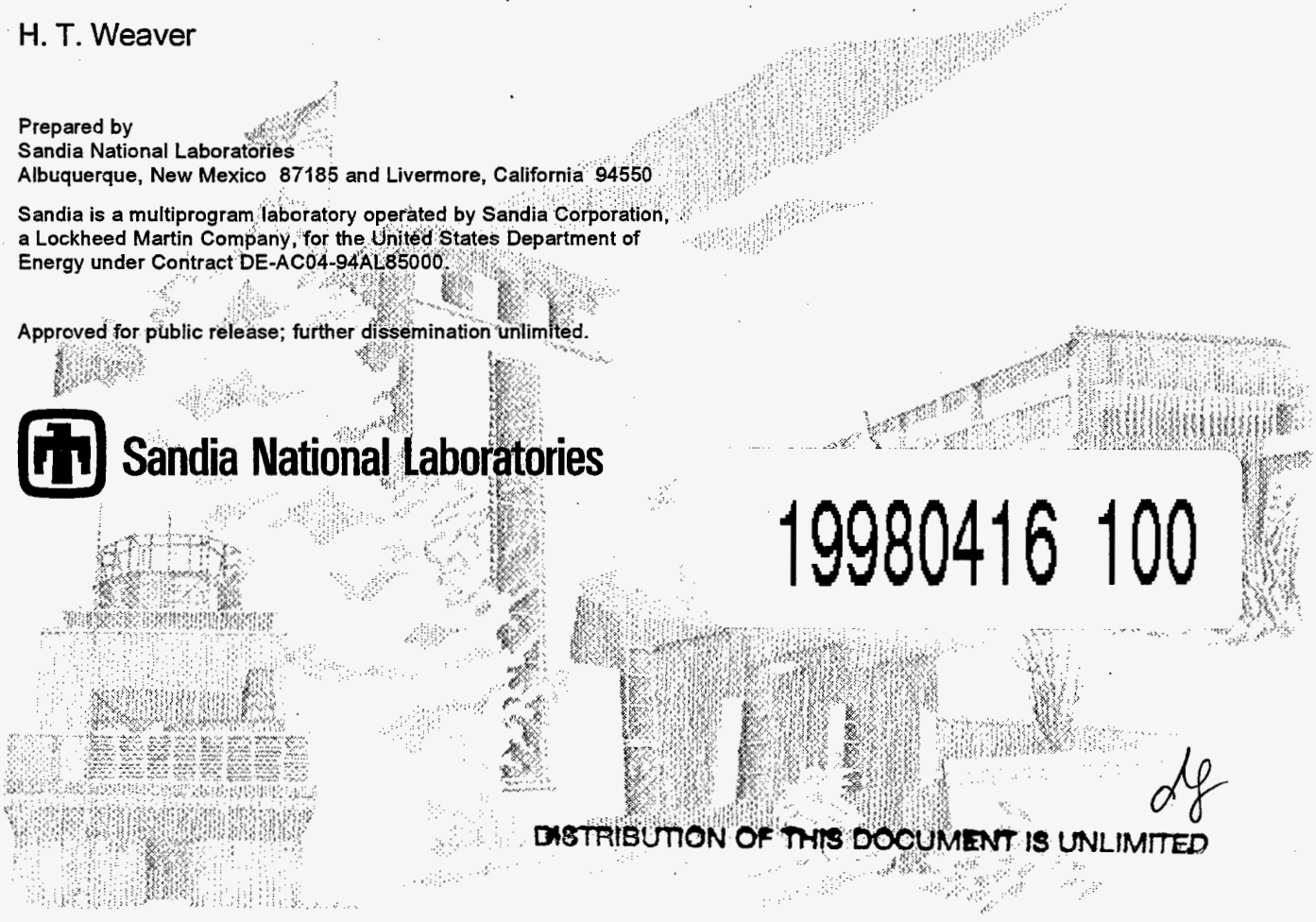

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Abstract

During the 1980s Sandia designed, developed, fabricated, tested, and delivered hundreds of thousands of radiation hardened integrated circuits (IC) for use in weapons and satellites. Initially, Sandia carried out all phases, design through delivery, so that development of next generation ICs and production of current generation circuits were carried out simultaneously. All this changed in the mid-eighties when an outside contractor was brought in to "produce" ICs that Sandia developed, in effect creating a crisp separation between development and production. This "partnership" had a severe impact on operations, but its more damaging effect was the degradation of Sandia's microelectronics capabilities. This report outlines microelectronics development and production in the early eighties and summarizes the impact of changing to a separate contractor for production. This record suggests that low volume production be best accomplished within the development organization.

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Summary

Delivery data for ICs to Sandia systems are shown which indicate the successful initiation of Sandia's microelectronics fabrication capabilities. As IC technology evolved to newer generations with increased performance levels, Sandia's approach to producing die changed. Rather than have Sandia alone develop and produce ICs a separate company was employed to produce ICs using Sandia technology. The change had a negative impact on both development and production. Before initiating new IC production, it is well that these two periods of Sandia microelectronics be reviewed.

Lessons Learned from Early Microelectronics Production at Sandia National Laboratories

Introduction

Throughout the history of Sandia's microelectronics fabrication program there has been some controversy associated with decisions to produce, in house, integrated circuits (IC) for use in systems. While production of components is traditionally the responsibility of the DOE complex, ICs present an unusual situation in that the dividing line between development and production is not sharp. Further, the number of ICs that result from a single fabrication run is at least comparable to the total number required for many DOE systems. As a consequence, excess ICs at the completion of a development cycle are often sufficient in number to meet production requirements. While this situation creates an almost unique niche for procurement of special purpose ICs, production (compared to development) does involve a much more structured accounting, for both method and material. There is inevitably some contention between concurrent development and production.

The primary reason for Sandia's large investments in fabrication of ICs is the development of radiation hardening techniques. The magnitude of this investment is dictated by the fact that radiation effects on ICs are mainly associated with the integration of active components rather than with the individual transistors. Thus, while many government labs were capable of fabricating discrete devices and studying their response to radiation, only Sandia made the threshold investment required to fabricate high density ICs and, as a result, was the premier lab for innovations in rad hard technology and for state-of-the-art product.

This situation changed around the mid-eighties, following which progress in developing rad hardening methods essentially stopped at Sandia and Sandia's hardened technology was no longer preeminent. Our ability to fabricate hardened ICs of any type was also severely limited. This change was in part due to conscious decisions to de-emphasize development of rad hard ICs, a decision that resulted from the appearance of several commercial suppliers of rad hard ICs. But the initial slide in Sandia's capabilities was due to unintended consequences of decisions associated with the question of production vs. development. Specifically, action was taken to separate IC production from IC development by segregating these responsibilities between Sandia and a contractor (Allied Signal). Subsequently, under a separate action a partnership with AT&T was established to develop next generation rad hard ICs. While the overall success of either of these actions can be debated, there is no debate over the fact that both had a detrimental effect on Sandia's ability to develop and fabricate rad hard ICs.

The purpose of this report is to review Sandia's IC fabrication activities in the period 1980 to 1985, a review that supports the thesis that small volume production and significant development can occur in a National Lab. Today, as IC technology continues its relentless advance and as the number of rad hard IC vendors continues to diminish the question of what constitutes Sandia's role in IC production, not to mention IC development, is relevant.

Integrated Circuit Terminology

Fabrication of ICs requires executing a series of **processes** such as film deposition, pattern definition (photolithography), and film etching on a single crystal disc of silicon, known as a **wafer**. Combinations of these processes form a recipe and specific recipes are known as **technologies**. A single technology or recipe is used to fabricate a variety of logic or memory circuits where function is determined by circuit design. The main electrical element of an IC is the transistor and in highly integrated ICs (large number of transistors per unit area) the most frequently used transistor types are designated **P-MOS** or **N-MOS**, depending on whether positive or negative charges are transported through the transistor, respectively. The historical acronym **MOS** refers to the constituent materials (metal-oxide-semiconductor) in the layers making up the transistors of early integrated circuits. Since the control electrode was metal, a technology was referred to as metal-gate-P-MOS, for example.

In time a technology was developed that employed both types of transistors and was known as complementary MOS or **CMOS**. In addition, silicon replaced metal as the gate electrode so that modern ICs are often designated by silicon-gate-CMOS. Finally, a technology generation is defined by its **minimum feature size**. Thus, we would find 2 μm-silicon-gate-CMOS as a high performance IC technology in 1980, while today 0.35 μm-silicon-gate-CMOS is used for high performance, high density circuits like the Pentium microprocessor found in many personal computers.

The operating voltage of an IC is determined by the minimum feature size. That is, the voltage is reduced as the features become smaller in order to roughly maintain constant the electric fields within the IC insulators. Practically, it is the operating voltage rather than the field that is maintained constant for several generations. The voltage is reduced only when reliability is threatened. Higher voltages tend to enhance radiation hardening so that there is a motivation at Sandia to push the operation voltages upward. However, this is not without reliability costs.

Finally, as fabricated on the silicon wafers ICs are referred to as **die**. These die are sawed from the **wafer** and assembled into "packages". The assembly processes result in some losses so that a delivery of die is larger that the actual IC needs. Since Sandia fabricates die, all the numbers presented in this report are for **die** deliveries. The number of packaged ICs needed for the different systems is significantly smaller than the number of die shipped. Thus, there is no way to associate the number of weapons, for example, with the number of die.

Sandia Integrated Circuits

I. Technology:

Sandia has primarily used CMOS, first metal then silicon gate, due to intrinsic radiation tolerance and low power characteristics of the CMOS designs. Since 1978 Sandia has prototyped six generations of digital CMOS (10 μm, 7 μm, 3 μm, 2 μm, 1.25 μm, and 0.5 μm) and delivered war reserve (WR) product in four. The 10 and 7 μm technologies were metal gate, all subsequent work was silicon gate. Other WR deliveries include analog circuits and non-volatile memories, primarily using CMOS with resistors, capacitors, or nitride transistors added as needed.

A commercial recipe embodying a specific IC technology might have several hundred individual processing steps. Only about 10-15% of these steps must be modified to achieve radiation tolerance. The equipment sets for fabricating commercial and radiation hardened ICs are identical. Changes in process parameters such as temperature, film thickness, doping levels, etc. accomplish the hardening. While only well defined changes in equipment settings are required for producing a hardened IC, it is just these variations on a standard recipe that introduce unacceptable financial risks for most IC companies, that in turn creates the niche in which Sandia operates.

It is important to emphasize that evaluation of hardening techniques requires the testing of complete, fully functioning ICs. Individual transistor performance simply does not provide adequate information to develop a technology. Sandia is unique among government labs by virtue of its investment in a facility and organization capable of fabricating high density ICs, in effect a medium sized integrated circuit company. Therefore, Sandia was able to develop generation after generation of radiation hardening techniques and deliver WR ICs when needed. During the early 1980s Sandia was recognized as the clear leader in radiation hardening technology for ICs and served as supplier for important national initiatives when no commercial company was available.

II. Facilities:

All IC fabrication for WR deliveries was carried out in Building 870 which was a Class 100 clean room constructed in a converted warehouse. The fabrication area was reasonably modern, employing 2-inch diameter silicon wafers until 1982 at which time the equipment was converted to handle 4-inch diameter material. Both silicon gate and metal gate radiation hardened technologies were used to fabricate ICs. By 1980, the minimum features were 6 or 7 μm in both technologies.

During this period, lithography techniques were changing dramatically. For example, Sandia produced most of the early ICs using "contact aligners", but newer "projection aligners" became upgrades and subsequently "step and repeat" aligners were required to define 2 μm features. At

one time all three types of photolithography equipment were in operation simultaneously in the fabrication area.

These rapidly advancing processing methods and the variety of technologies under development required that Sandia operate under a mode that was rarely used in production facilities. The term used to describe operations was "model maker" where individual technicians carried out every step in a recipe, which contrasts to the more commonly used "station mode" where individual technicians only carry out one type of process (etch, deposition, lithography, etc.) as the silicon wafers are moved through the lab. A successful model maker must be highly trained and most of the Sandians were college educated, though not necessarily in electrical engineering.

A transition to "station mode" was needed for two reasons. First, fabrication equipment had become more complicated to operate, making training and subsequent daily operations very difficult. Second, the need for production volumes, though small, pushed the balance toward an advantage for station mode. Simply hiring contractors to work on baseline technologies, such as used in the WR deliveries, began the transition. For a short period, both model makers and station mode technicians worked side by side using common equipment for development and production. The fabrication area was operated seven days per week using two shifts. Model makers were formed into teams, with at least one team member working during all shifts. In this hybrid mode Sandia was able to achieve rapid turn-around times for development lots and reasonable volumes for product.

Today Sandia operates the Microelectronics Development Laboratory[1] (MDL) a 33,000 ft^2 Clean room with 12,500 ft^2 of Class 1 area. Modern equipment capable of 0.5 μm CMOS and 0.25 μm test structures is available. Die containing millions of transistors are routinely fabricated in this facility. The appropriations for constructing the MDL were approved in the mid-eighties against the background of successful deliveries described below.

III. Commitments:

Sandia made commitments in the early 1980s to deliver some tens of thousands of IC die to NASA's Galileo project and to deliver many more tens of thousands of die to a wide collection of weapon systems. Packaging of high reliability ICs was not done at Sandia, but contracted out to Fairchild for Galileo and Allied Signal was responsible for packaging weapon components. Galileo used silicon gate CMOS exclusively and the weapons were primarily metal gate.

The transition from 2 to 4-inch diameter wafers was needed to support these relatively large commitments. That is, we needed more ICs per wafer and the larger diameter wafers provided a factor of four increase. However, there resulted a number of start-up problems so that 1982 began with virtually zero yield. The fabrication problems were systematically worked out, but the very existence of these problems gave an unrealistically bleak picture of Sandia's capabilities for production and were factors in the programmatic decisions to solicit help, first in production, then in development of rad hard ICs.

While making deliveries of WR quality ICs Sandia was engaged in an extensive development program to advance technologies for the newer weapon designs and for satellite applications. There were four major technology development programs initiated by early 1982. First, a silicon gate, 3 μm CMOS development was begun to support Peacekeeper and Trident II. Second, a CMOS metal gate non-volatile memory (NVM), to support these same programs, was developed. Sandia ultimately lost the Peacekeeper program, but these technologies, particularly the NVM, enabled what is probably the most sophisticated AF&F programmer in the U.S. arsenal for Trident II. Third, a silicon gate, 4 μm NVM technology was initiated to support code storage. And finally, a 2 μm silicon gate CMOS was begun as our most advanced IC and thousands of 16 Kbit memories were ultimately delivered to the MILSTAR program.

There were a number of other small deliveries made in the 1980-85 period, including MILSTAR, Magelian, and several Sandia satellites, but the main efforts are the ones described below. Sandia's capability to make deliveries concurrent with the development of four new technologies is the basic thesis of this report.

Galileo Project

Sandia was contracted by JPL to fabricate some 50,000-60,000 radiation hardened ICs for the Jupiter probe Galileo. These were mainly 1 Kbit static random access memories (SRAM), but also included a microprocessor and some read only memories (ROM). The circuit designs were done at RCA using a closed geometry CMOS designated by CCL. The CCL technology was slightly different from the silicon gate work at Sandia, but minimum features of 6 μm were consistent with our process equipment. We experienced a number of technology problems with the CCL, particularly with radiation hardening 10V silicon gate processes.

Techniques for radiation hardening change with each generation. In these early CMOS circuits individual transistors would fail to turn off after radiation. Early in the Sandia program, it was noted that reducing the thickness of the transistor insulator (gate thickness) could minimize this "leakage". For metal gate technologies radiation hardening was never a difficult problem due to intrinsic properties of the technology itself. However, the move to silicon gate required significant thinning of the gate insulator. The resulting reliability issue remained a problem for all 10 V silicon gate products and was only contained by screening, both for the JPL deliveries and later for Trident II. We have evidence from field data that the screening is adequate in that the Galileo probe, which has been in space for nearly 7 years, has exhibited IC failure rates below projections.

Figure 1 shows our delivery of die[2] to the packaging house (Fairchild) where they were packaged, burned-in, and returned to Sandia for final delivery to JPL. This plot chronicles deliveries but does not properly convey the real difficulties Sandia had in establishing reliability of the packaged parts. The initial deliveries exhibited a radiation effect known in jargon as "rebound". Although previously observed by specialists[3], it was not discovered in the Sandia testing but showed up in sub system radiation tests at JPL. Thinner gate parts fabricated after the conversion to 4-inch diameter wafers did not show this effect. However, the thin gate ICs often failed reliability certification and had to be screened. Much of this testing, screening, etc. took place after delivery of packaged parts and required a subsequent increase in the initial order. Ultimately, all deliveries were completed and the space probe was a success.

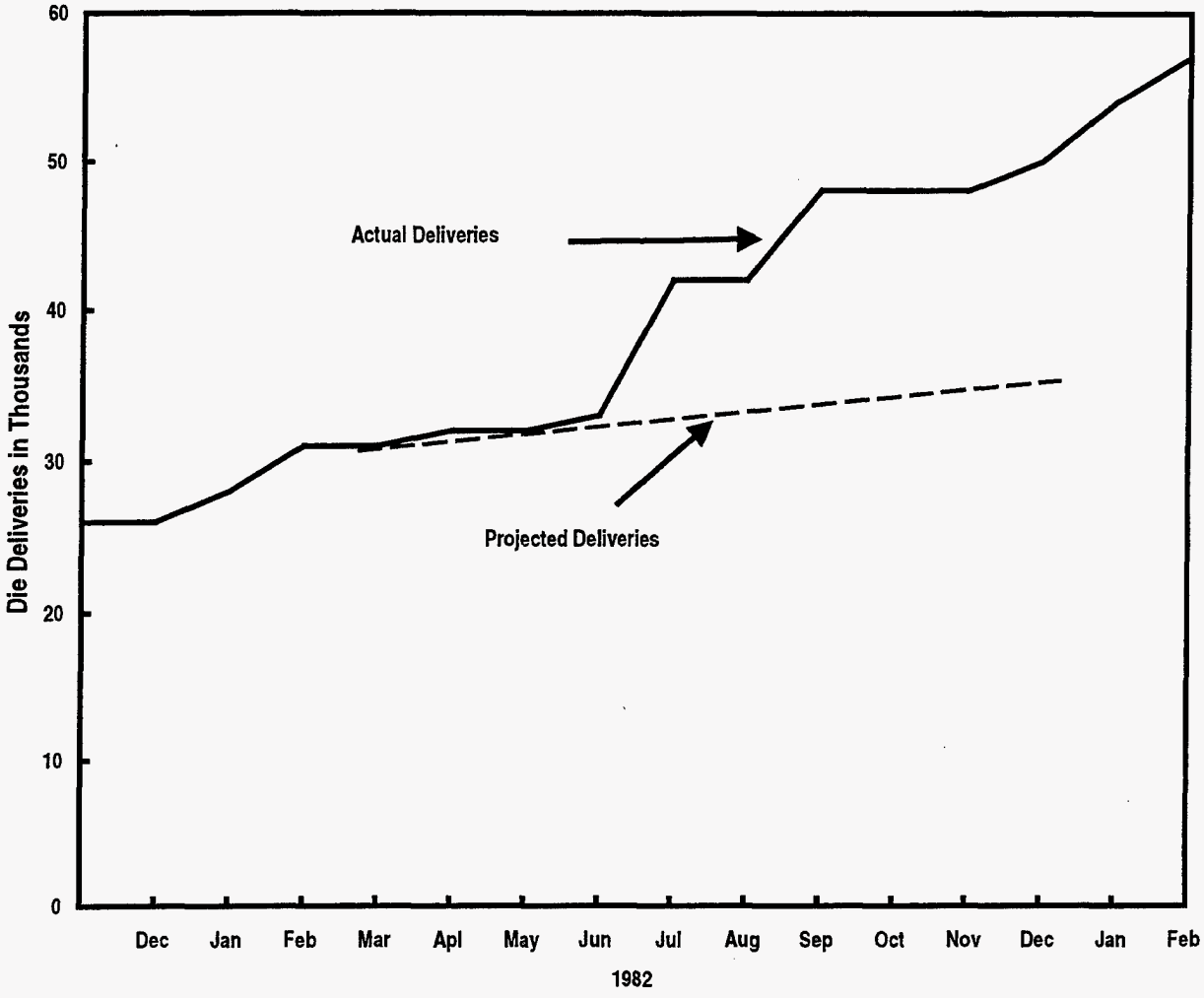

Figure 1. Summary of die deliveries to JPL for Galileo. Most of the die were 1K-bit static RAM, but a few hundred microprocessors and ROM are included.

There was one program development for which Sandia received significant praise from JPL and which demonstrated the quick response capability of a national lab to a technical problem. After the program was well into its final stages, studies of the Jovian environment revealed an unexpected flux of high-energy sulfur ions. These ions could produce soft errors in unhardened ICs and, in particular, would almost certainly produce soft errors in a bipolar microprocessor during Galileo's probe descent to Jupiter's surface. Sandia took the logic design for the processor, converted it to our 2 μm CMOS technology, and fabricated replacement chips. The Sandia microchips were inserted into the Galileo system and functioned flawlessly during the probe descent.

While this microprocessor project was a critical element in the Galileo program and an excellent demonstration of Sandia's ability to respond quickly to a government need, it was a very minor part of Sandia's overall contribution to Galileo. In context, it represented a couple of FTEs and a few die, compared to the tens of FTEs and tens of thousands of die supplied in total to the spacecraft.

Weapons Programs and the AMO Decision

During the early eighties weapon commitments for radiation hardened ICs increased dramatically. Most of these ICs were 7 μm-metal-gate-CMOS operated at 10 V. There were a significant number of non-volatile memories and a few silicon gate ICs. In Table 1 are shown descriptions of ICs and the weapon systems in which they were applied[4,5]. All of these ICs were delivered to Allied Signal in Kansas City (then Bendix) in die form. The requirements for ICs were increasing significantly during 1982 at the same time that Sandia was making large deliveries to Galileo.

Table 1
Integrated Circuits Fabricated at Sandia for Weapon Systems

IC	Function	Weapon System
SA2475	Non-Volatile Memory	B83, B61JTA, W84
SA2575	Universal I/O	B83
SA2614	Clock Control	B83
SA2723	1K RAM	B83
SA2774	Unique Signal Gen	W78
SA2800	Interface Chip	B83, W84
SA2892	MOSFET Array	W84
SA2902	Decoder	W81, B83, W84
SA2908	Data Acquisition	B83JTA, W84JTA
SA2941	μMicroprocessor	B83, B83JTA, W84JTA, W82JTA, W84
SA2984	DAS A-D Converter	W82JTA, W87JTA
SA2992	Non-Volatile Memory	B83, W84,
SA3046	DAS Control Chip	B83JTA, W84JTA

The transition in 1982 from 2-inch to 4-inch diameter silicon wafers impacted the weapon ICs as severely as it did the Galileo program. For a period, there were essentially no working die. We illustrate the situation in Figure 2 that shows the growing die requirements and the lagging deliveries[2]. It was actually much worse than Figure 2 indicates in that many of the 1982 deliveries were from lots fabricated earlier. The production rates were not nearly adequate to meet schedules. This was a very serious situation involving a new Sandia endeavor (delivering IC product) which had severe implications for our weapons program in general.

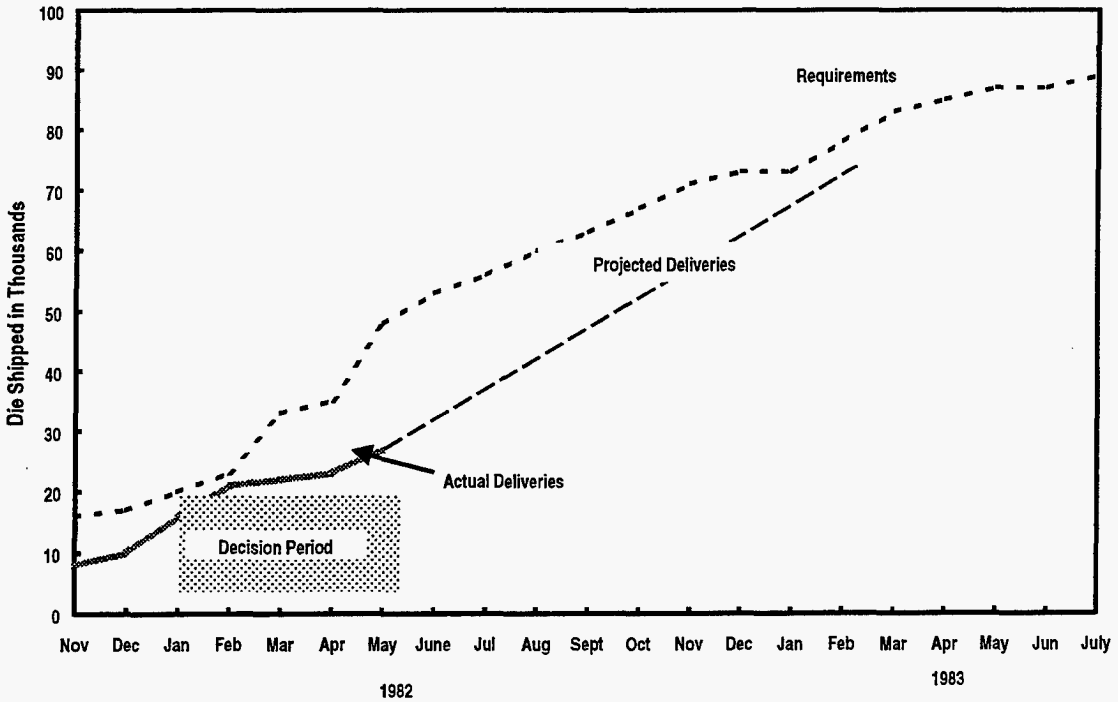

Figure 2. Sandia's weapon die commitments and early deliveries are shown. Using the delivery rate shown we were not able to assure meeting these commitments.

It was during this period that top Sandia managers were wrestling with the general problem of how best to produce low volumes of ICs. They were also being confronted with potential delays in weapon production as a result of Sandia's efforts to produce these ICs. In addition, the need for radiation hardened ICs was expected to increase during the eighties due to the strategic defense initiative. Since there was no history of Sandia delivering a significant number of ICs the idea of a separate contractor to help was more than reasonable -- it seemed essential.

The situation on the "floor" of the fabrication area yielded a different picture. Here it was easy to project that with previously demonstrated yields, that is with yields obtained before the conversion to 4-inch diameter wafers, all deliveries could be met within a time period consistent with our commitments. Said another way, the IC fabrication problems were technical but understood and, hence, tactical in nature, while the decision being made had strategic, long-term effects. First and second level managers, who had direct access to fabrication data and understood the implications of various changes that were occurring in the lab, were optimistic. However, it was difficult to project credence for this perspective.

In any case, the decision to bring in a contractor was made. Ultimately a member of the production complex, Allied Signal, was chosen. They had, however, no IC fabrication experience. An Albuquerque presence was established under the name of Albuquerque Microelectronics Office or simply AMO. The date for switching over was approximately 1985 allowing Sandia to complete ongoing IC deliveries before AMO took charge of operations.

Figure 3 shows the actual delivery history for the weapon ICs. The large increase in capacity reflects our yield increase and is characteristic of batch processing where large numbers of ICs, or more generally parts, can be fabricated in a short period. There is some irony in the dates for arrival of AMO managers in that the problem of deliveries to weapons that was surely a major factor in precipitating their mission was completely solved by that time, although their actual assignment, beginning with Trident II support, had not begun.

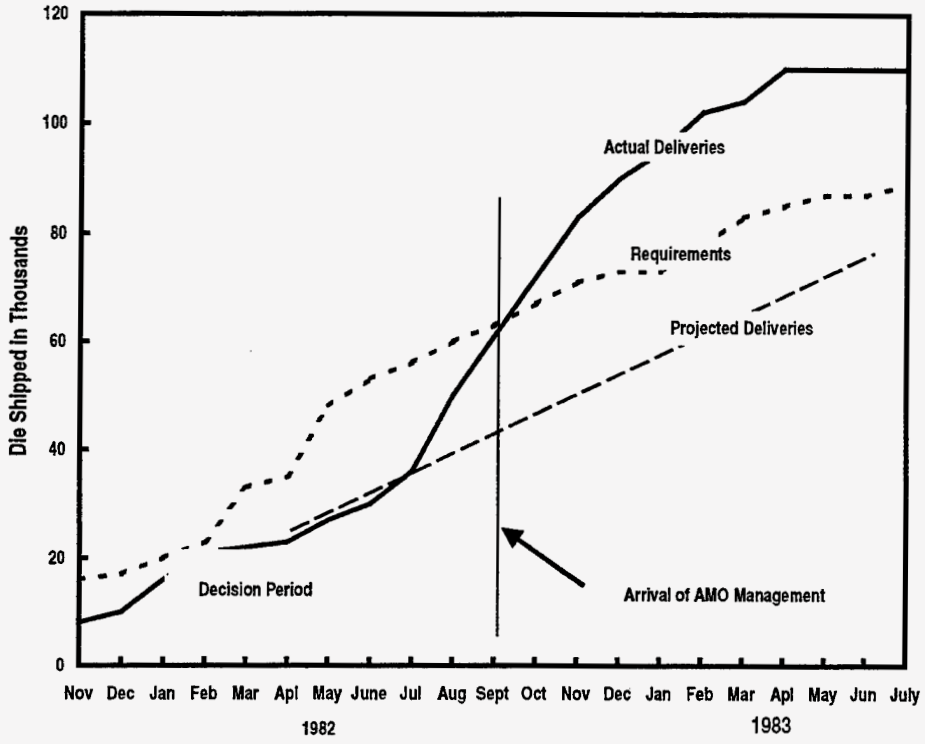

Figure 3. Data for weapon commitments, projected deliveries, and actual deliveries. The actual deliveries far exceeded both commitment rate and projections. For reference is shown the time for deciding on establishing a relationship with AMO and the arrival of AMO managers. Note that the delivery problem that was paramount during the decision period had been resolved by the arrival time of AMO.

Included in the IC deliveries were a few thousand non-volatile memories (SA2992). These particular circuits were used for code storage and contained only 256 bits and only a small fraction of these were used. All NVM used metal gate transistors with nitride storage films in a PMOS technology. Most of the features of this technology were never used again, but development work on this memory provided the fundamentals for beginning a much more aggressive design of a fast writing non-volatile memory that was a system enabler for a strategic application in the Trident II fuzing system. The development work on the Trident II memory overlapped deliveries of this earlier memory.

Development to Production with a Partner

The early eighties were undoubtedly the most aggressive period for IC development at Sandia. We initiated work on four new technologies, all significantly different from each other. As noted earlier, the technologies were (1) 3 μm silicon gate CMOS, (2) 7 μm metal gate fast writing non-volatile memories, (3) 4 μm silicon gate (long data retention time) non-volatile memories, and (4) 2 μm silicon gate CMOS. Fully functioning prototypes from each of these technologies were demonstrated by 1983, the same period during which our largest number of production deliveries was made. The 2μm technology provided SRAM to MILSTAR and microprocessors to Galileo before the AMO take over in 1985.

By 1985 Sandia had advanced at least one generation in IC prototyping capabilities relative to 1980 and was in a position analogous to the 1980 period when Galileo and early weapon commitments were being addressed. However, AMO was assuming control of the fabrication area and taking responsibility for all production deliveries. As was the case with earlier weapon and Galileo deliveries, various reliability problems were encountered as production began. The types of problems we encountered are typically not seen in prototypes. That is, the electrical functionality was adequate, but certification was prevented by failures in radiation or in reliability testing. In a way, these are more subtle issues than usually occur in early development.

Now, however, the situation for recovery was very different from earlier periods. Sandia had developed the technology and AMO was trying to produce parts. AMO had no experience with ICs and the interfaces between organizations were not solid. Consequently, the needed fixes were significantly delayed. Not only were deliveries delayed but also ancillary problems developed as a direct consequence. For example, confidence in the metal gate NVM was so low that the silicon gate NVM was substituted in an application (code activated processor, CAP) for which it was not designed. This action led to reliability problems that would not occur in a more conservative application. A domino type effect continued as more and more resources were devoted to the Trident II chip set, in effect bringing down any other technology that experienced problems.

The inability of Sandia to act unilaterally to solve technical problems and AMO's lack of experience with IC fabrication differentiated this period from the similar period in 1982.

Sandia management intervened at this point by instituting a common reporting structure for AMO and Sandia employees. Several middle level Sandia managers were replaced. These changes brought stability to the situation, but confidence in Sandia microelectronics was damaged severely and in many ways irreparably. In the end an outside vendor (Harris Semiconductor) was used to supplement the 3 μm CMOS technology deliveries for Trident II, and the MILSTAR program was terminated. Once the deliveries were complete the AMO fabrication capability was essentially dissolved (although a number of AMO employees became Sandians) and AT&T was brought in as a partner for next generation CMOS development.

The entire situation did not reflect well for Sandia microelectronics.

Perspectives

Sandia's microelectronics capabilities were significantly diminished by the end of the decade. There was no "production" capability and, worse, radiation hardened IC development was in decline. This was true despite occupancy in 1988 of the MDL, a world class microelectronics fabrication facility. Tracking Sandia technology advances against the commercial world provides evidence for this decline. Figure 4 shows an historical comparison of our maximum transistor density with that for Intel's microprocessors[6]. The Intel chips represent state-of-the-art IC technologies. While this plot is not a one for one comparison, it does provide a measure of Sandia's rate of progress.

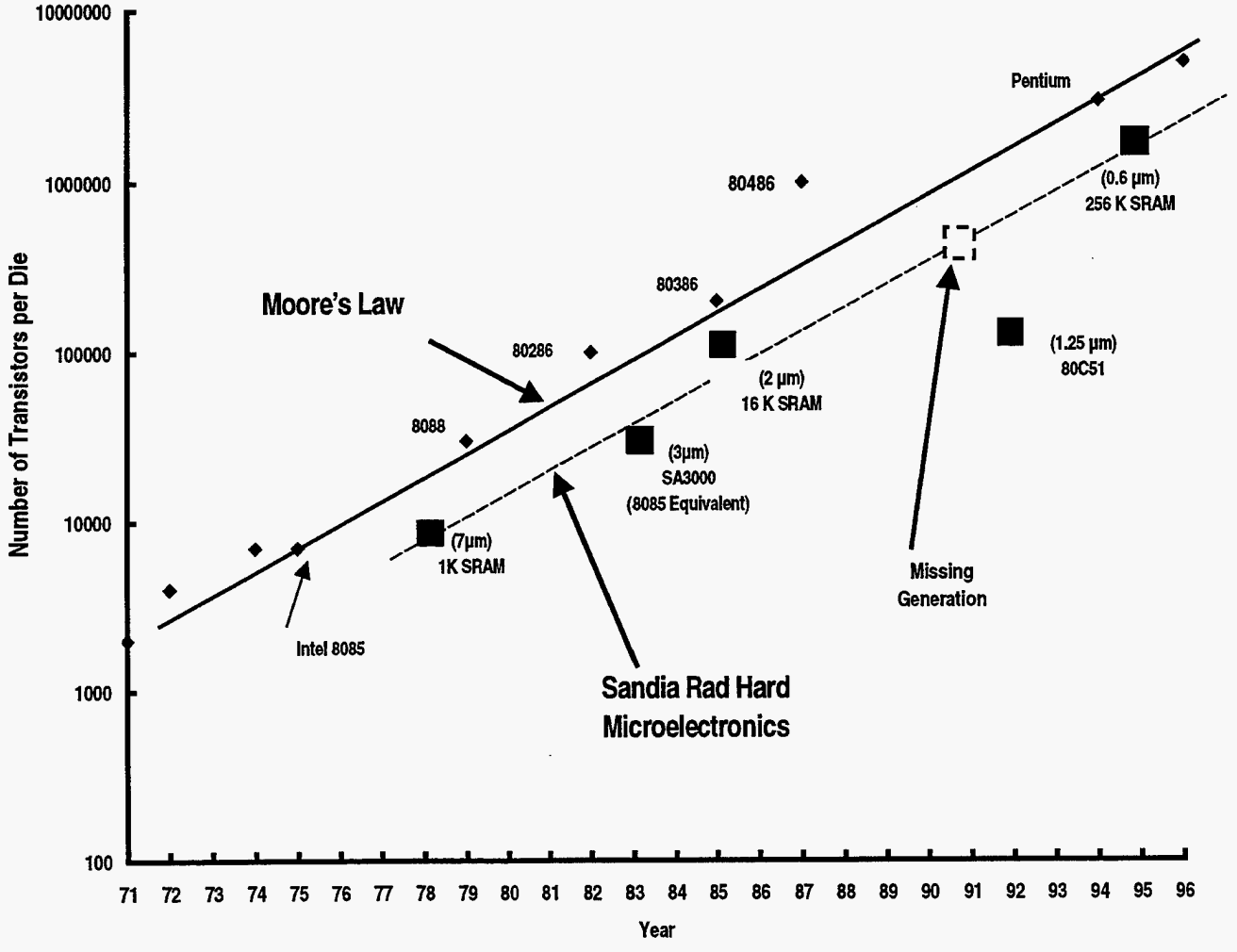

Figure 4. Plot comparing the complexity of ICs as a function of time for commercial microprocessors and for Sandia produced circuits. The commercial products are all Intel microprocessors while a variety of Sandia memories and processors are shown.

Note that in the period from mid-eighties to mid-nineties Sandia demonstrated no advance in transistor density, even for prototypes. Sandia, which was in a partnership with AT&T during this period, was able to bring up the next generation technology (1.25 μm CMOS) and yielded some lower density circuits, but the difficult task of yielding high density ICs within this technology was never accomplished.

Sandia moved back on its original growth path only after IBM donated a modern IC fabrication equipment set. Following the donation Sandia top management made a commitment, both in manpower and resources, to fabricate high-density circuits. We were, consequently, able to skip two generations of IC technology, essentially bringing us back to our original growth path.

While there are several parameters associated with Sandia's decline, the fundamental issue is our response to the question of how to handle low volume, multiple technology production. In a traditional sense, such deliveries are not a production activity at all. The low total numbers of circuits and the short fabrication time do not allow for a "learning curve" under which yield and product quality are improved. Stated differently, the technologies are never fully developed. This complicates any fabrication effort as we found in the early eighties. But technology transfer to a second party becomes an additional and perhaps unsustainable burden, particularly when the partner is inexperienced, as was the case with Allied Signal. There is little doubt that this combination of incomplete development and inexperience diminished Sandia microelectronics.

An alternative model for low volume, special purpose IC production has been adopted at NSA where National Semiconductor runs an IC fabrication facility on the NSA site[7]. At first this appears the same as the AMO model, but the clear, fundamental difference is that the technology used at NSA is a National Semiconductor technology executed by personnel, either National or NSA, who are trained by National engineers. This model works very well for producing special purpose circuits. The difficulty applying the NSA model at Sandia is (1) it is very expensive and (2) it does not allow the development of special technologies like rad hard, integrated sensors, or micromachines that are increasingly important within Sandia's mission.

Whatever our conclusions on procurement of radiation hardened or other special purpose ICs, the low product volume orders and continuous development of new technologies do represent the niche in which Sandia is most needed. It will most likely continue to be a significant part of our microelectronics mission and successful execution will provide a clear differentiating strength for the entire Lab.

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