NASA/TM–2011-217047

Lightning Pin Injection Test: MOSFETS in "ON" State

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Table of Contents

Table of Figures

1 Background and Introduction

This publication builds upon NASA/TM-2009-215794 "Lightning Pin Injection Testing on MOSFETs", where standard lightning waveforms were pin-injected into power metal-oxide-semiconductor field-effect transistors (MOSFETs) to induce fault modes and degrade performance. [1] Previous testing showed that MOSFET (IRF520NPBF) Gate-Source connections may be susceptible to lightning-induced failure, even when installed in systems in well-shielded and partially-shielded aircraft locations. MOSFET Drain-Source connections were shown to be significantly less susceptible. Previous testing also showed that device impedance decreased (current increased) after every failure. Such a failure mode may lead to cascading failures, as the damaged MOSFET may allow excessive current to flow through other circuitry. Analysis of the characteristic curves of the devices showed that for certain injection modes the devices can accumulate noticeable damage.[2] In the previous testing, the MOSFETs were not connected to any external circuitry other than the lightning transient generator, and as such, without any bias voltage applied between Gate and Source (i.e. "OFF" state).

The NASA Aviation Safety Integrated Vehicle Health Management (IVHM) Project is conducting this research to determine early warning indicators of avionic semiconductor component degradation which can be used to predict the onset of system failures. To understand the interplay between lightning-induced surges and aging on component performance, a collaborative research effort has been established between NASA Langley Research Center (LaRC) HIRF Lab personnel and researchers at the NASA Ames Research Center (ARC) Prognosis Center of Excellence to determine the effects of lighting induced electrical transients on MOSFET components. The purpose of this research is to develop validated tools, technologies, and techniques for automated detection, diagnosis and prognosis that enable mitigation of adverse events during flight, such as from lightning transients.[3] The effort fits within "Aircraft Systems Health Management" Discipline-Level research, Diagnosis milestone 2.1.2.2 and Prognosis milestone 2.1.3.1; and "Advanced Sensors and Materials" Foundational-Level Research milestone 1.1.2.1. This report describes lightning environmental testing which was performed in May 2009, where MOSFETS were tested in the "ON" state.

2 Objective

The test objective was to evaluate MOSFETs for induced fault modes caused by pin-injecting a standard lightning waveform into them while operating (i.e. connected to a Gate-driver circuit and electrical current flowing between Drain and Source.). Lightning Pin-Injection testing was performed at NASA LaRC. Subsequent fault-mode and aging studies were performed by NASA ARC researchers using the Aging and Characterization Platform for semiconductor components. This report documents the test process and results, to provide a basis for subsequent lightning tests. The ultimate IVHM goal is to apply prognostic and health management algorithms using the features extracted during aging to allow calculation of expected remaining useful life. This will counteract some of the negative effects of damage incurred by lightning by providing information prior to the components failure such that safe operation of the system is maintained.

3 Approach

NASA ARC IVHM researchers supplied 300 IRF520NPBF power MOSFETs. IRF520NPBF MOSFETs are manufactured in a TO-220 package as shown in Figure 1. The IRF520NPBF was selected to be representative of devices that are present in DC-DC power supplies and electromechanical actuator circuits that will be used on board future aircraft. Most of the MOSFETs were characterized prior to

arriving at LaRC using the NASA ARC Aging and Characterization Platform for power transistors.[4] Elements of the system were transported to NASA LaRC to use for characterizing damage caused by lightning pin-injected transients. Damage is characterized by measuring key static parameters, namely, threshold voltage, leakage current and breakdown voltage. The MOSFETs were tested in the "ON" state by applying a bias-voltage between Gate-Source or Drain-Source during lightning pin-injection. "ON" state testing required transient voltage protection of the DC sources used for biasing, as well as additional load resistors to limit DC current through the MOSFET. (More test setup details are provided in Section 3.3.)

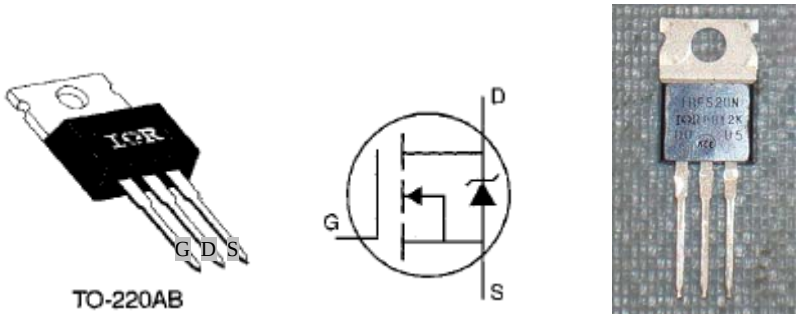


Figure 1: IRF520NPBF MOSFET package (left), Schematic (center) and photograph (right). Gate, Drain and Source are labeled "G", "D", and "S", respectively.

3.1 RTCA/DO-160 Lightning Waveform #4

The RTCA/DO-160E "Environmental Conditions and Test Procedures for Airborne Equipment", Section 22 "Lightning Induced Transient Susceptibility", was used.[5] DO-160E Section 22 includes procedures for pin-injection and cable bundle tests, and is intended for establishing flight worthiness of airborne equipment. DO-160E test processes are intended for assembled electronic systems, rather than individual components, so these tests were modified to accommodate the special situation of testing individual components. The DO-160E lightning- induced voltage Waveform 4 "6.4us-Rise Double Exponential" was selected for these tests. (See Figure 2.) DO-160E recommends Waveform 4 for airborne equipment that may be subjected to lightning-induced magnetic fields coupled onto their wiring. (Waveform 3, "Damped Sinusoid"[6] is also recommended for pin injection testing, however Waveform 4 was favored by the NASA team because Waveform 4 contains more energy per event, and is thus more likely to induce damage than Waveform 3. The NASA equipment is also capable of testing at lower voltage levels using Waveform 4.) Peak DO-160E Test Levels for Waveform 4 are shown in Table 1. DO-160E allows devices to be un-powered during pin-injection testing, which may lead to results that are not representative of airborne equipment operating in an actual lightning environment.

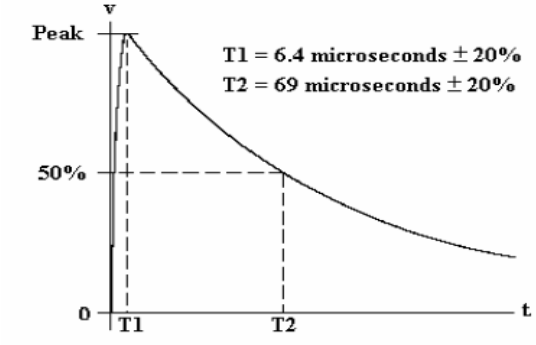


Figure 2: RTCA/DO-160E Section 22 Voltage Waveform 4.

Table 1: DO-160E Generator Setting Levels for Pin Injection (Source Impedance for WF4= 5 Ohms)

Level	Representative Environment	Waveform 4 Voc/Isc
1	Well Shielded	50/10
2	Partial Shielded	125/25
3	Partial Exposed	300/60
4	Severe	750/150
5	More Severe	1600/320

3.2 Facility and Equipment

All testing was conducted in NASA's High Intensity Radiated Field (HIRF) Laboratory, located in Building 1220, Room 144, on 1 South Wright Street at NASA LaRC, between May 5 and May 29, 2009. The HIRF Laboratory is typically used for reverberation chamber radiated emissions and immunity testing. However, the reverberation chambers are easily adapted to lightning testing. An overview of HIRF Laboratory capability is provided in the Reference section[7,8,9]. The HIRF Laboratory is equipped with EMC Partner MIG-System generators for lightning indirect effects testing, and is capable of performing DO-160E Section 22, up to Test Level 5 for pin, cable and ground injection for Waveform 4. The HIRF laboratory is also able to perform other waveform and multiple stroke and multiple burst tests, as well as additional test types beyond DO-160E. Figure 3 shows the EMC Partner equipment that was used for pin-injection tests, and Table 2 summarizes the test equipment used.

Table 2: Test Equipment

Equipment Item	Manufacturer/Model	SN/ECN	Cal. Due
Impulse Gen.	EMC Partner MIG0600MS	260/2104741	N/A
Step Down 1:8 Transformer	EMC Partner NW-MS-Level1	SN002	N/A
Oscilloscope	Tektronix DPO4054	ECN1641291	1/9/2010
Current Sensor 100X	Pearson 5046	120468/A037686	7/9/2008*
Current Sensor 100X	Pearson 4997	121314/A037687	7/9/2008*
High Voltage Probes (2)	Tektronix P5100	N/A	N/A
DC Power Supply (20V, 5A)	Tenma 72-6152	A014924	N/A
DC Power Supply (30V, 3A)	Tenma 72-2010	A014923	N/A
Transient Voltage Supressor	FCC-450A-7-L	N/A	N/A
Transient Voltage Supressor	FCC-450A-10-L	N/A	N/A
Transient Voltage Supressor	FCC-450A-18-L	N/A	N/A
Biasing/Lightning Injection Interface Board	Designed & Fabricated by John Mielnik	N/A	N/A
MOSFET Test Board	Provided By NASA Ames	N/A	N/A

*The Pearson 5046 and 2997 Current Sensor calibrations were expired during this test. Subsequently, on August 28, 2009, the probe calibrations were verified to be within specification.
(NASA Ames personnel used a Component Evaluation System, consisting of a Keithley 2410 SourceMeter, a Dell PP05XA Notebook computer and a National Instruments GPIB-USB-HS adapter for their MOSFET characterizations. The NASA Ames equipment was not part of the pin injection test setup but is later described in Section 5 of this report.)

Figure 3: Lightning-generating equipment was used for pin-injection tests. (EMC Partner MIG0600MS shown on right.)

3.3 Test Setup

MOSFETs are active circuit devices. Operationally, the Drain-Source (D-S) impedance varies as the Gate-Source (G-S) voltage changes. Operation of a MOSFET requires external biasing circuitry. For the previous NASA/TM-2009-215794 testing, the MOSFET was not part of an active circuit, so test setup consisted of simply connecting the lightning generator and oscilloscope to two terminals of the MOSFET. Pin injecting lightning transients into a MOSFET that is "ON" requires consideration of the biasing circuitry in several different ways:

- Protection of biasing circuitry from the lightning transient.
- Protection of the MOSFET from excessive current applied by biasing circuitry.
- Protection of the Lightning Generator from excessive current applied by biasing circuitry.
- Assurance that biasing circuitry does not corrupt the MOSFET test results by modifying the lightning transient waveform.

A test circuit satisfying these requirements was designed by the test team. The schematic is shown in Figure 4. Essentially V_{DS} and V_{GS} function to bias the MOSFET D-S and G-S junctions such that the device is in the ON state as the lightning pin injected transient is applied. A Fischer Custom Communications (FCC) Transient Voltage Suppressor (TVS) was installed in parallel to both voltage sources. The TVS devices function to bypass the voltage sources when the lightning transient is applied

(thereby protecting the voltage sources). Current Sense Resistors (R1= 0.01 Ohms and R2= 0.01 Ohms) are at the Drain and Gate inputs to facilitate measurement of direct current, using a differential probe. Current-limiting resistors (R3 and R4, 10 Ohms each) are in-line with V_{GS} and V_{DS} to limit the direct current through the G-S and D-S junctions, so as not to cause unnecessary heating to the MOSFET or excessive direct current through the lightning waveform generator.

The lightning transient was applied to either the G-S junction or the D-S junction, but not both simultaneously. The lightning waveform generator has an internal impedance of 5 Ohms, so it was replaced by a 5 Ohm resistor (R5) when not present. The G-D pin-injection configuration was not tested because such a test would require significant additional effort to protect the lightning generator and power supplies in the event of a G-D short-circuit MOSFET failure mode. The MOSFET Source terminal is usually referenced to ground, so the G-S and D-S junctions are more likely to provide a lightning transient path than the G-D junction (i.e. lightning transients impart much more energy to common-mode rather than differential-mode coupling to aircraft wiring bundles). This rationale for not testing G-D is also supported by RTCA/DO-160, which notes that pin injection is usually conducted between each pin and case ground.[10]

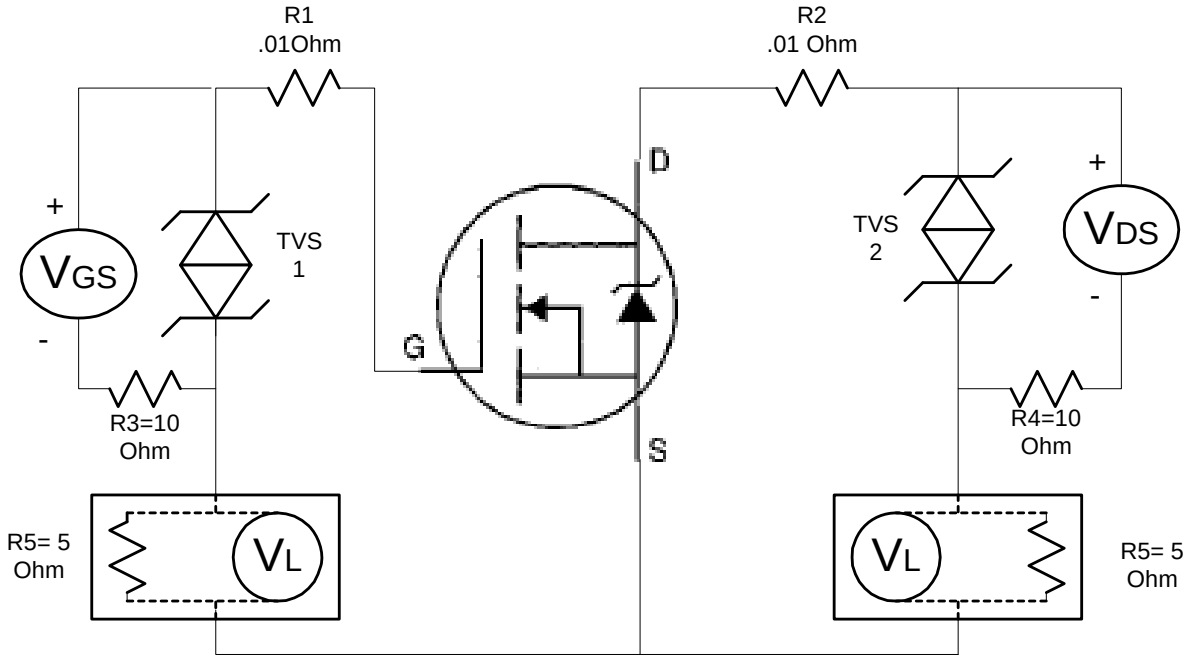


Figure 4: Pin Injection Test Setup Schematic.

In order to implement the MOSFET test circuit with safe, repeatable hookups, and test port access for oscilloscope and DC voltmeters, and to allow the use of interchangeable components (i.e. TVS devices), a Component Testing Biasing/Lightning Injection Interface Board was designed and fabricated. High voltage components, recessed banana jacks and wide circuit-board traces were used to ensure personnel safety. A photograph of the board is shown in Figure 5.

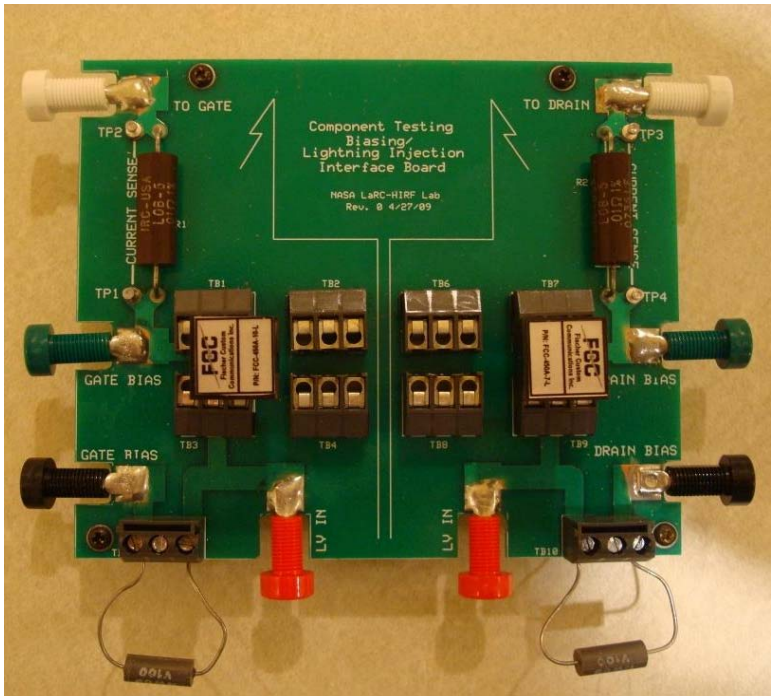


Figure 5: Component Testing Biasing/Lightning Injection Interface Board.

The Component Testing Biasing/Lightning Injection Interface Board was the focal point of the pin injection test hookup. The MOSFET under test was mounted in the NASA Ames IV-Curve Test Board used in previous testing (NASA/TM-2009-215794), which was connected to the Component Testing Biasing/Lightning Injection Interface Board. Two handheld digital voltmeters were used to monitor the DC current flowing through the MOSFET G-S and D-S circuits, using the current sense resistors. The use of a four channel oscilloscope, two high-voltage probes, and two current transformer probes allowed simultaneous monitoring of injected lightning voltage and current on both G-S and D-S circuits. A complete Pin Injection Test Hookup diagram is provided in Figure 6. A photograph of the hookup is provided in Figure 7. Oscilloscope settings are provided in Table 3 and the Lightning Generator connections & settings are provided in Table 4.

Table 3: Oscilloscope Setings

Parameter	**Setting**			
Timebase	20 uS (WF4)			
Trigger	Edge, Source=Ext. Coupling=DC, Slope=Pos, Level= 8000mV			
	Channel 1 (G-S Voltage)	**Channel 2 (G-S Current)**	**Channel 1 (D-S Voltage)**	**Channel 2 (D-S Current)**
Level	Varied	Varied	Varied	Varied
Coupling	DC	DC	DC	DC
Position	0 Div	0 Div	0 Div	0 Div
Offset	0 V	0 A	0 V	0 A
Probe=	100X Voltage	100X Current	100X Voltage	100X Current
Input Impedance	1M Ohm	1 MOhm	1M Ohm	1 MOhm

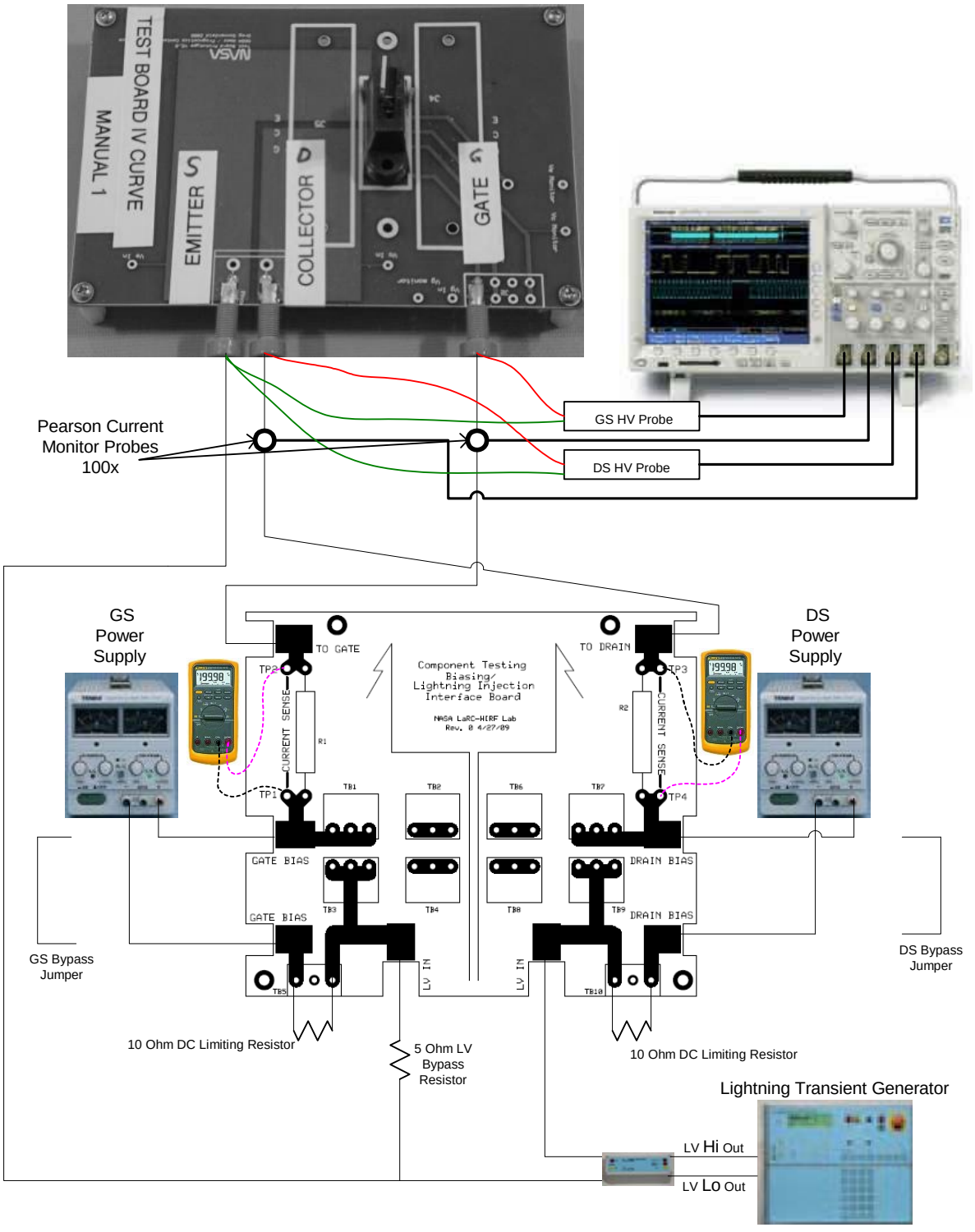


Figure 6: Pin Injection Test Hookup diagram. (HV Lines were each 81.5”+43.0”= 124.5 inches long. Two sections allowed connection-to/bypass-of Attenuator Box.)

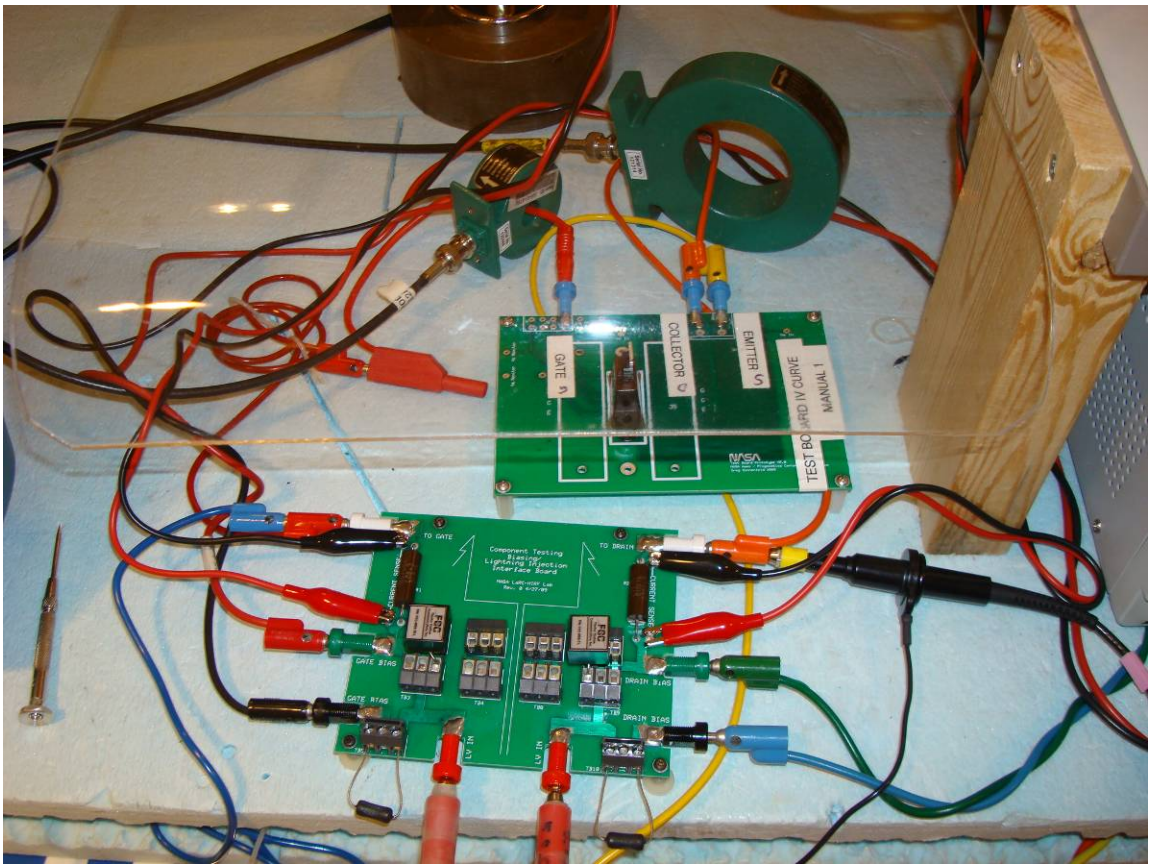
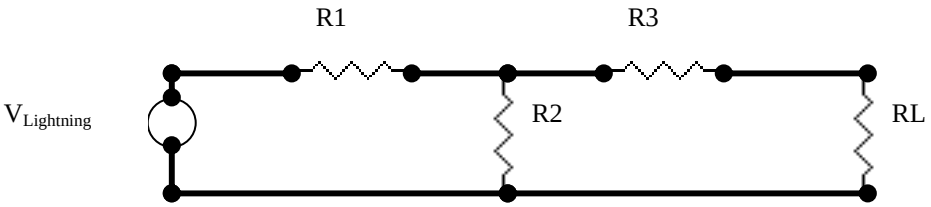


Figure 7: Pin Injection Test Hookup Photograph

Table 4: MIG0600MS Lightning Generator Connections & Settings

Connections	-HV -Trigger -Use NW-MS-LEVEL1 Attenuator box if VPeak below 50V -Use Resistor Network if VPeak between 50V and 70V
Settings	1. On/Stby Press 2. Safety Ckt- Closed 3. Waveform 4 4. VPeak: Test Matrix 5. Polarity: “Pos” or “Neg” 6. Trig. Mode: SS=Manual, MS=Auto, Test Time, Repetition

Some testing required pin-injection levels below DO-160 Level 1. The EMC Partner MIG0600MS Lightning Waveform generator does not allow testing below 70V peak. The NW-MS-Level1 Box reduces the open circuit voltage (OCV) to 1/8 the output of the MIG0600MS, allowing 9 to 50V OCV test. To accommodate test voltages between 50V and 70V, a resistor network was used to reduce Open-Circuit voltage of Waveform 4 by half, while still maintaining the correct source impedance. Operationally, the MIG0600MS is set to a voltage 2 times higher than the desired OCV when using the resistor network. A schematic of the resistor network is shown in Figure 8, and photographs of the implementation are shown in Figure 9. As an accuracy check, Waveform 4 with MIG0600MS setting of 40V was applied across the MOSFET GS terminals. 47.7V was measured when using the resistor network (19% change from 40V), whereas 52.3V was measured when using the NW-MS-Level1 (31% change from 40V). Based upon these results, the resistor network was more accurate, and was preferred for the 35V to 50V overlapping range.



- R1= 5 Ohm Lightning Generator Source Impedance
- RL= Load Impedance of Test Device (unknown)
- R2= 5 Ohms (tested to within 0.1 Ohm)
- R3= 2.5 Ohms (tested to within 0.1 Ohm)

Figure 8: Circuit Schematic to enable Waveform 4 testing down to 40V Peak with MIG0600MS Transient Generator.

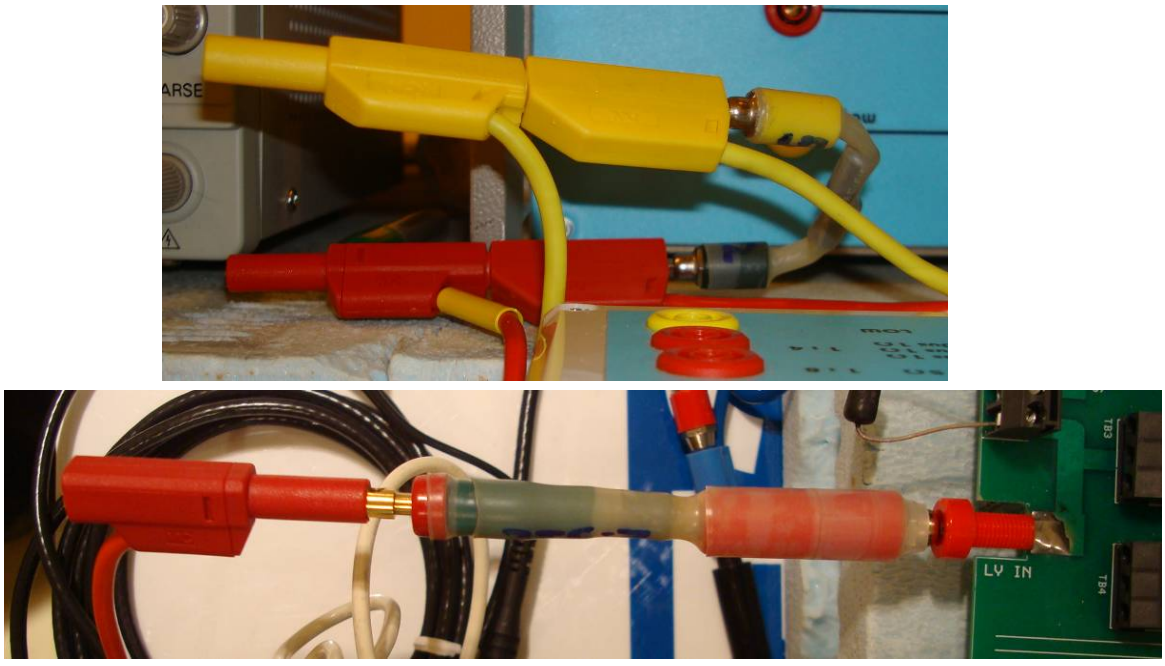


Figure 9: R2=5 Ohms (in parallel, top photograph), R3=2.5 Ohms (in series, bottom photograph), implementation.

3.4 Safety Hazards & Precautions

Test Personnel were briefed on the standard HIRF Laboratory Safety procedures, including:

- Location of Exits
- Marshalling Areas
- Location of Fire Extinguishers and AEDs, qualified AED Responders
- Out-Of-The-Ordinary operations: (i.e. construction, blocked exits, auditory alarms, other testing, etc.)

The following warning was prominently displayed in the test Plan:

WARNING
The transient generators used in these tests produce lethal voltage and current levels.
Exercise all operational safety precautions to prevent injury or death of test and support personnel.

A Hazards Identification Meeting was held to discuss additional safety hazards and to identify precautions and controls to mitigate them. Table 5 shows the hazards identified and their precautions and controls.

Table 5: Lightning Generator Connections & Settings

Hazard	**Precaution**
1. High Voltages (HV): Source Measurement Unit	All Personnel: 1ft Clearance from Device and all HV connections when Keithley 2410 SourceMeter Blue Light is ON.
2. High Voltages: Lightning Transient Generator	All Personnel: 1ft Clearance from Device and all HV connections when Generator is in RUN Mode.
3. Un-Authorized Personnel in Test Area	-Post “DANGER: TEST IN PROGRESS” sign during all HV test operations. -Test Personnel instructed to Stop Test when Unauthorized personnel in Chamber B.
4. Device Destruction during HV Test	Place Clear Safety Shield over device during lightning transient testing.
5. Inadvertent Operation Lightning Transient Generator	-Push SAFETY CIRCUIT button to OFF on Lightning Transient Generators when test operations are not being conducted.

4 Results Summary

4.1 Pre-Test

A Pre-Test procedure was used to determine the single-stroke test level required to cause permanent damage, for each input pin configuration. The pin-configuration nomenclature used in this report is based upon NASA/TM-2009-215794 (MOSFET in the "OFF" state) for consistency and comparison, but was modified because the MOSFET biasing circuitry responds differently to MIG0600MS lead-reversal versus polarity change. (Lead reversal versus polarity change is discussed in Section 4.1.2.)

Table 6: Pin Connection & Polarity Nomenclature

Pin Configuration	MIG0600MS Waveform	+ Lightning Voltage Connected To:	- Lightning Voltage Connected To:
② G-S	4+	Gate	Source
❷ G-S	4-	Gate	Source
③ D-S	4+	Drain	Source
❸ D-S	4-	Drain	Source

The Lightning Transient Generator was connected as shown in Figures 4 and 6. Single stroke Waveform 4 was used for all tests because it is representative of a voltage waveform likely to be present on aircraft interconnecting wiring paths due to the Current Component A wave shape, caused by structural IR voltages and diffusion coupling.[11] Also, Waveform 4 was used for most of the previous NASA/TM-2009-215794 data, so it is preferred for comparisons with new data. For a particular pin-configuration, the test level was increased until a change was observed on the current & voltage waveforms displayed on the oscilloscope. The MOSFET was then evaluated using the NASA ARC source and measurement unit characterization system.

MIG0600MS Lightning Generator display data is used for the "V Peak Setting" in test data tables. MIG0600MS Lightning Generator display of peak Open Circuit Voltage (Voc) was measured at several setting points, and found to understate the actual peak Voc by 3% to 14%, which is within the RTCA/DO-160F allowance of +/- 20%. Oscilloscope-measured peak Voc data are published in NASA/TM-2009-215794, and are repeated here in Table 7. Oscilloscope-measured peak voltage and peak current values are also recorded in all data tables, and full voltage and current oscilloscope waveform data were stored for every test.

Table 7: Peak Voc Data for MIG0600MS

V_{out} Setting (Displayed)	Measured Peak Voc (Waveform 4)
10	11.0 * (110%)
20	22.6 * (113%)
40	45.6 * (114%)
80	82.0 (103%)
160	164 (103%)
320	332 (104%)
640	682 (107%)
1280	1359 (106%)
1700	1798 (106%)

*(NW-MS-LEVEL1 Step-down 1:8 transformer required)

4.1.1 MOSFET Biasing

MOSFETS exhibit different D-S current-voltage (I-V) curve characteristics depending upon V_{GS}. Each I-V curve on Figure 10 represents a different V_{GS} trace for the IRF520PBF MOSFET. Because of the I-V characteristic, energy deposited by an injected lightning transient across the Drain-Source junction will vary with V_{GS}. Therefore the D-S Fail voltage is expected to vary with V_{GS}. Two $V_{GS\text{-}bias}$ settings were selected for testing: 8 and 16VDC. The rationale was that 16 VDC is the highest rated V_{GS} rating, and 8 VDC is midscale. ($V_{GS\text{-}bias}$=0 VDC was tested as part of the previous effort reported in NASA/TM-2009-215794.)

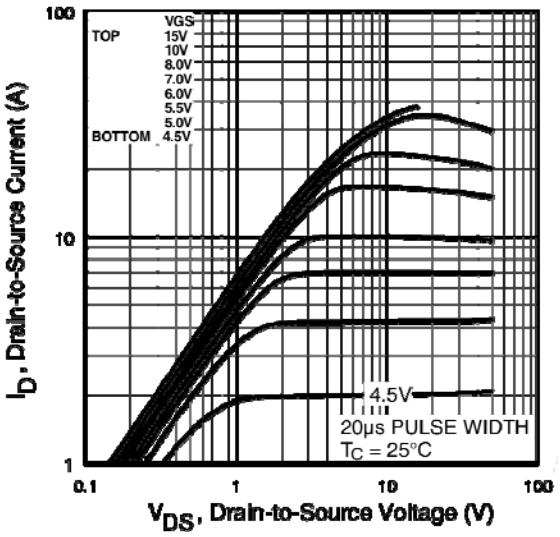


Figure 10: I-V Curves for IRF520PBF (25 Deg. C).

To accommodate the two different $V_{GS\text{-}bias}$ settings, appropriate TVS devices were needed to prevent lightning transients from back-driving the V_{GS} power supply. Devices with 10V and 18V clamping voltages were selected to protect the $V_{GS\text{-}bias}$ power supply set to 8V and 16V respectively. (TVS devices change from open-circuit to short-circuit at a specified voltage, over range of about 2 volts. A margin of 2V was selected to ensure the TVS would only be activated in the event of an applied transient, but still provide highest possible protection to the V_{GS} power supply.) Also, to provide DS forward bias (i.e. Drain ON) a 5VDC power supply was used. For no forward bias (i.e. Drain OFF), a bypass jumper was installed across the V_{DS} power supply terminals. Table 8 shows the test biasing configurations.

Table 8: MOSFET Test Biasing Configurations

Config.	Config. Description	$V_{GS\text{-}bias}$ Setting	GS TVS Selected	$V_{DS\text{-}bias}$ Setting	DS TVS Selected	Notes
G1 D0	Gate Lo, Drain OFF	8	FCC-450A-10-L	OFF	Bypass	Not Tested
G2 D0	Gate Hi, Drain OFF	16	FCC-450A-18-L	OFF	Bypass	
G1 D1	Gate Lo, Drain ON	8	FCC-450A-10-L	5	FCC-450A-7-L	
G2 D1	Gate Hi, Drain ON	16	FCC-450A-18-L	5	FCC-450A-7-L	

Only one Drain OFF configuration was tested, primarily due to a shortage of test time. Figure 11 shows the DS voltage and current with a 240V peak lightning WF4 injected into the DS terminals. Figure 11 shows that V_{DS} and I_{DS} levels due to the lightning transient are slightly higher when the power supply is bypassed (blue), likely because the bypass jumper has slightly lower impedance than routing through the power supply (black).

Data are also shown from NASA/TM-2009-215794 testing (Green), where 240V WF4+ was injected across DS terminals with no other circuitry connected. Without Gate biasing, more current flows through DS with a correspondingly lower voltage. As expected, V_{GS} biasing lowers the impedance of the DS junction.

Similarity between the black and blue (TVS and V_{DS} bypass) waveforms provided confidence that the TVS devices were not modifying the lightning waveform enough to violate DO-160F allowance of +/- 20%.

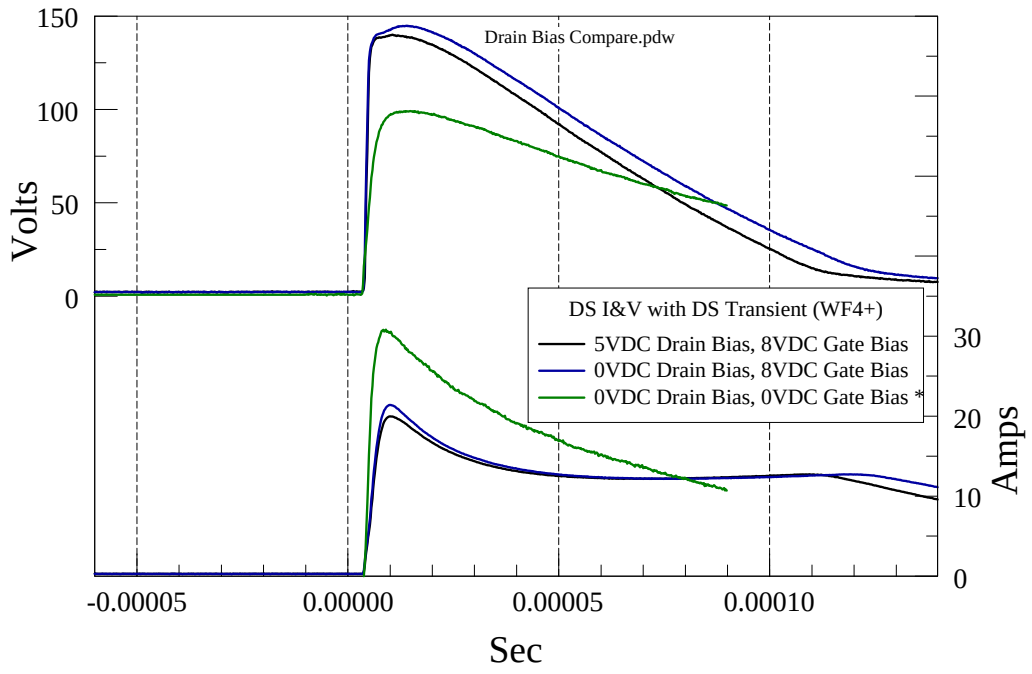


Figure 11: Drain ON versus Drain OFF Comparison. Peak Voc= 240V WF4+ was injected into the DS terminals, with $V_{GS\text{-}bias}$= 8VDC and $V_{DS\text{-}bias}$= 5VDC (Black) versus 0VDC (Blue, Bypassed). (Device AO, Tests 19 & 20.) *Data are also shown from NASA/TM-2009-215794 testing (Green), where 240V WF4+ was injected across DS terminals with no other circuitry connected to the MOSFET. (Device H1, Test 214)

4.1.2 Polarity Versus Lead-Reversal

The test team initially assumed that inverting the lightning waveform could be accomplished by simply reversing the HV test leads connected to the Biasing/Lightning Injection Interface Board. This approach was found to be experimentally invalid. Figure 12(a) shows the GS voltage and current with peak Voc= 70V WF4 injected into the GS terminals. Clearly, the MIG0600MS Negative Polarity waveform (blue, WF4+) is the inverse of the Positive Polarity waveform (black, WF4-). Reversing the MIG0600MS leads (red) does not produce an inverse waveform. Figure 12(b) shows the D-S voltage and current, lightning transient leakage to the D-S side of the circuit when the GS-injection leads are reversed. It is interesting to note that the negative-polarity GS-injected lightning transient switches D-S ON, but the positive-polarity transient does not. Based upon normal MOSFET theory of operation, the positive-polarity GS-injected transient could be expected to switch D-S to ON instead. This phenomenon may be investigated further.

Post-test, it was verified that both DC power supplies were isolated from facility-ground. The MIG0600MS high-voltage outputs are isolated from facility-ground also.

Based upon this evaluation, using the MIG0600 Negative Polarity waveform setting was determined to be the appropriate method of generating an inverse waveform for the tests described herein.

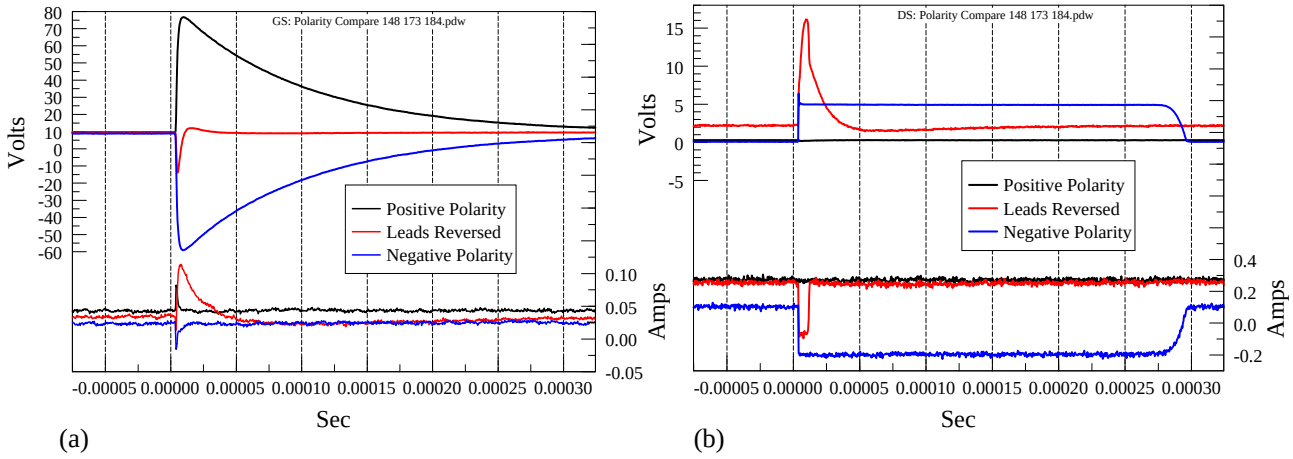


Figure 12: Comparison of Positive Polarity, Lead Reversal and Negative Polarity. Peak Voc= 70V WF4 was injected into the G-S terminals, with $V_{GS\text{-}bias}$= 8VDC and $V_{DS\text{-}bias}$= 5VDC. (a) Shows the GS voltages and currents. (b) Shows the D-S voltages and currents.

4.1.3 MOSFET Fail Levels: Pre-Test

Over 300 tests were performed in Pre-Test, with the goal of finding the MOSFET Fail Levels when injecting WF4+ and WF4- into the GS or DS terminals. $V_{GS\text{-}bias}$= 8VDC and 16VDC were tested. Oscilloscope data were evaluated to determine the actual MOSFET terminal voltage and current at failure (V_{Fail} Meas & I_{Fail} Meas). Figures 13 through 16 compare the V_{GS}, I_{GS}, V_{DS} and I_{DS} levels before and after failure.

GS Injection, $V_{GS\text{-}bias}$= 8V: Figure 13 shows Fail Level data when WF4+/- was injected into the GS terminals with $V_{GS\text{-}bias}$= 8V. Black traces show measured V and I using a MIG0600MS Peak Voc setting ("Voc set") below the level observed to cause failure. Red traces show measured V and I with peak Voc set at the level observed to cause failure.

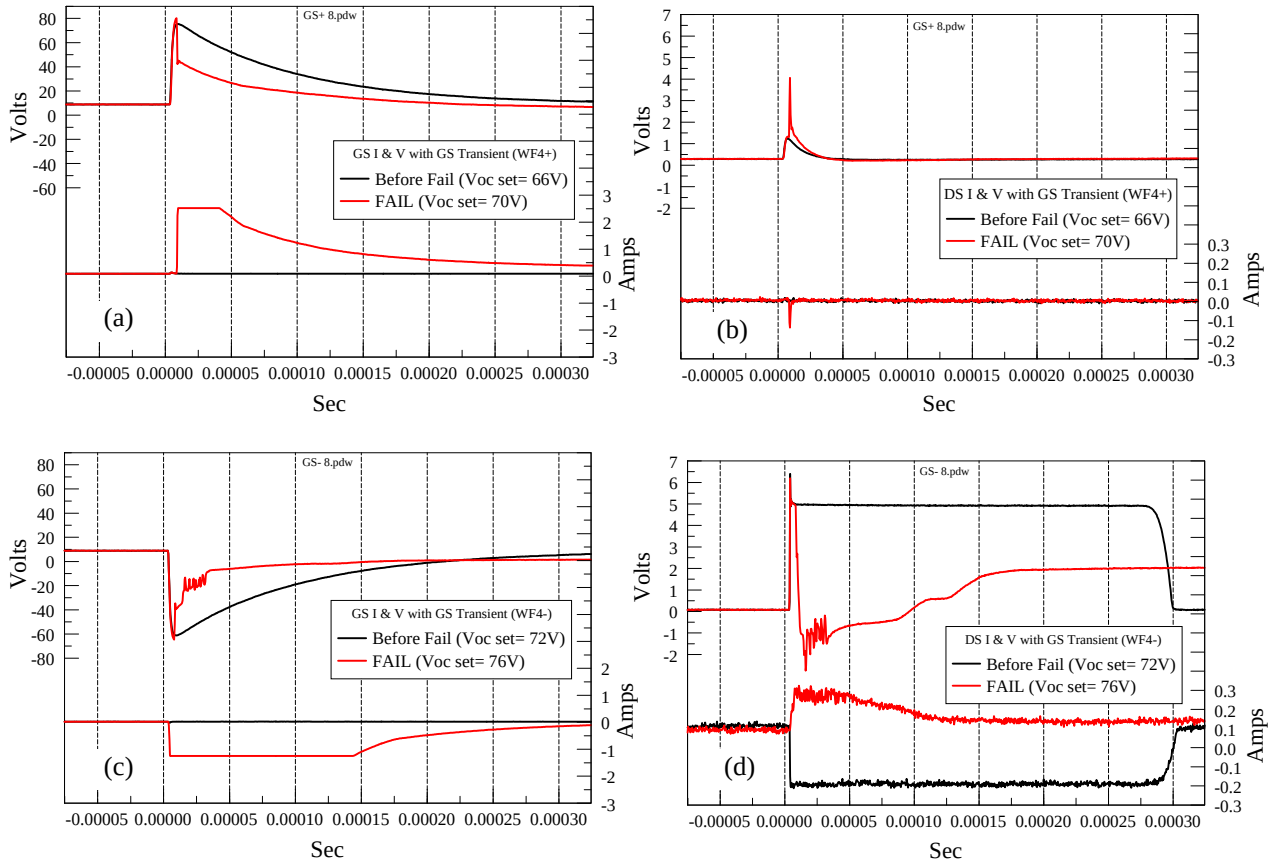


Figure 13: Comparison of Fail Levels with WF4+ and WF4- injected into MOSFET GS terminals. (WF4+, ②G-S pin config. Top: a & b) (WF4-, ❷ G-S pin config. Bottom: c & d) $V_{GS\text{-}bias}$= 8 Volts for these data. The plots on the left (a & c) are GS voltages and currents. The plots on the right (b & d) are the corresponding DS voltages and currents resulting from the injection on the GS terminals. (Note: Data from File 0188 is shown in (c) and (d), where Voc set=76V, rather than the actual fail level: Voc set=75V.)

Time-of-failure was rather simple to determine from the G-S injection data because the MOSFET GS impedance would dramatically and permanently decline at some peak GS voltage point, thus causing the GS current to increase from milliamps to amps. Comparing (a) and (c), the WF4- failure response essentially mirrors the WF4+ failure response. The difference in $V_{oc\ set}$ needed to damage the MOSFET is 6 Volts. Comparing (b) and (d), it appears that when a WF4+ transient damages the GS junction, damage

is not evident from the DS junction I & V data (b). However, when a WF4- transient damages the GS junction, damage is clearly revealed in the DS junction I &V data too (d).

DS Injection, $V_{GS\text{-}bias}$= 8V: Figure 14 shows fail data when WF4+/- was injected into the DS terminals with $V_{GS\text{-}bias}$= 8V. Black traces show measured V and I using a MIG0600MS Peak Voc setting ("Voc set") below the level observed to cause failure. Red traces show measured V and I with peak Voc set at the level observed to cause failure.

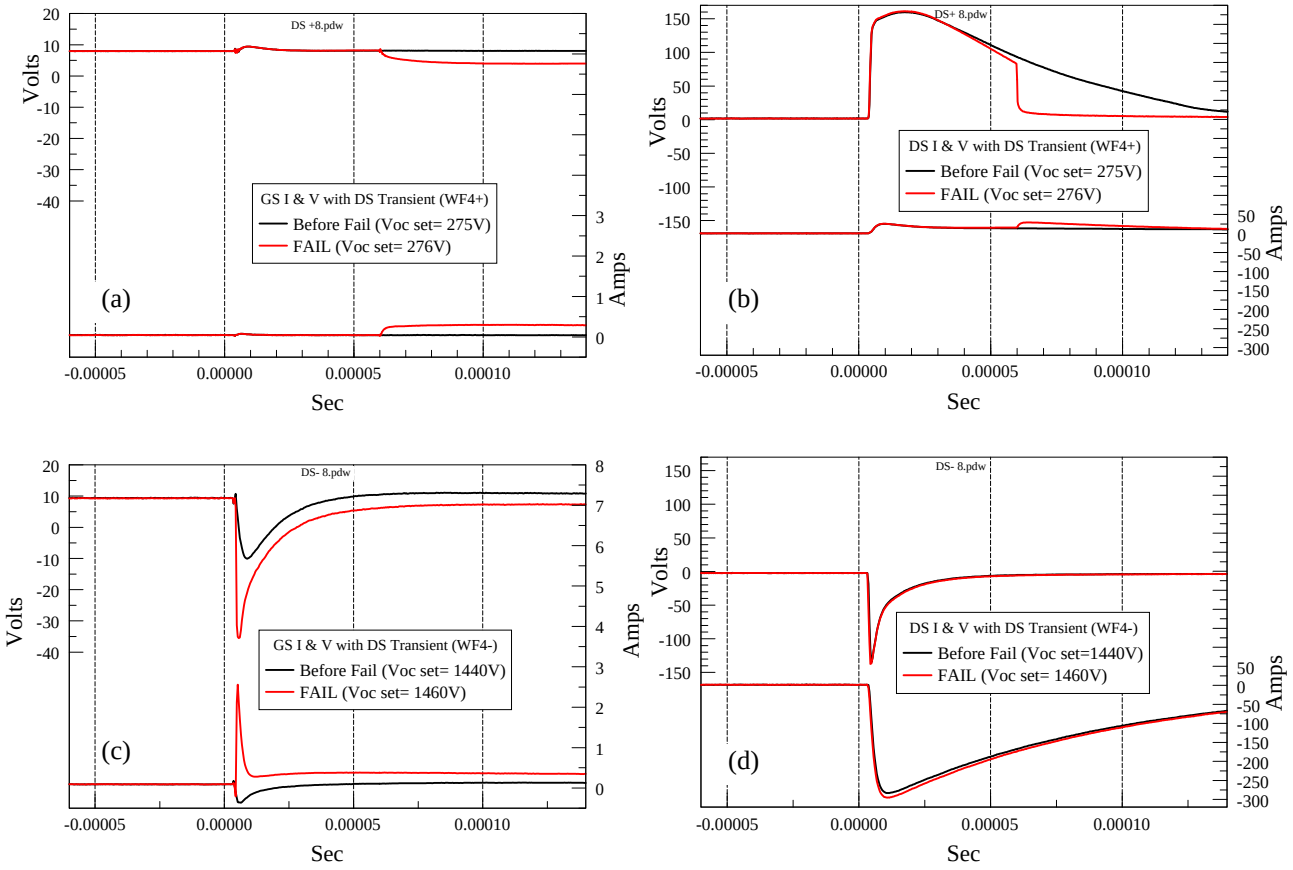


Figure 14: Comparison of Fail Levels with WF4+ and WF4- injected into MOSFET DS terminals. (WF4+, ③D-S pin config. Top: a & b.) (WF4-, ❸ D-S pin config. Bottom: c & d.) $V_{GS\text{-}bias}$= 8 Volts for these data. The plots on the right (b & d) are the DS voltages and currents. The plots on the left (a & c) are the corresponding GS voltages and currents resulting from the injection on the DS terminals.

Interestingly, GS junction I & V data reveal damage more readily than the DS data, even when injecting the lightning waveform into the DS terminals. Time-of-failure appeared delayed about 50us when injecting WF4+ into the DS terminals, possibly indicating a thermal damage characteristic. WF4+ induced failure permanently lowered the GS impedance. Comparing (b) and (d), when a WF4- transient damages the GS junction, damage is not evident from the DS junction I & V data (d). Comparing (a) and (c), the WF4+ and WF4- injections cause entirely different I & V failure responses.

GS Injection, $V_{GS\text{-}bias}$= 16V: Figure 15 shows fail data when WF4+/- was injected into the GS terminals with $V_{GS\text{-}bias}$= 16V. Black traces show measured V and I using a MIG0600MS Peak Voc setting ("Voc set") below the level observed to cause failure. Red traces show measured V and I with peak Voc set at the level observed to cause failure.

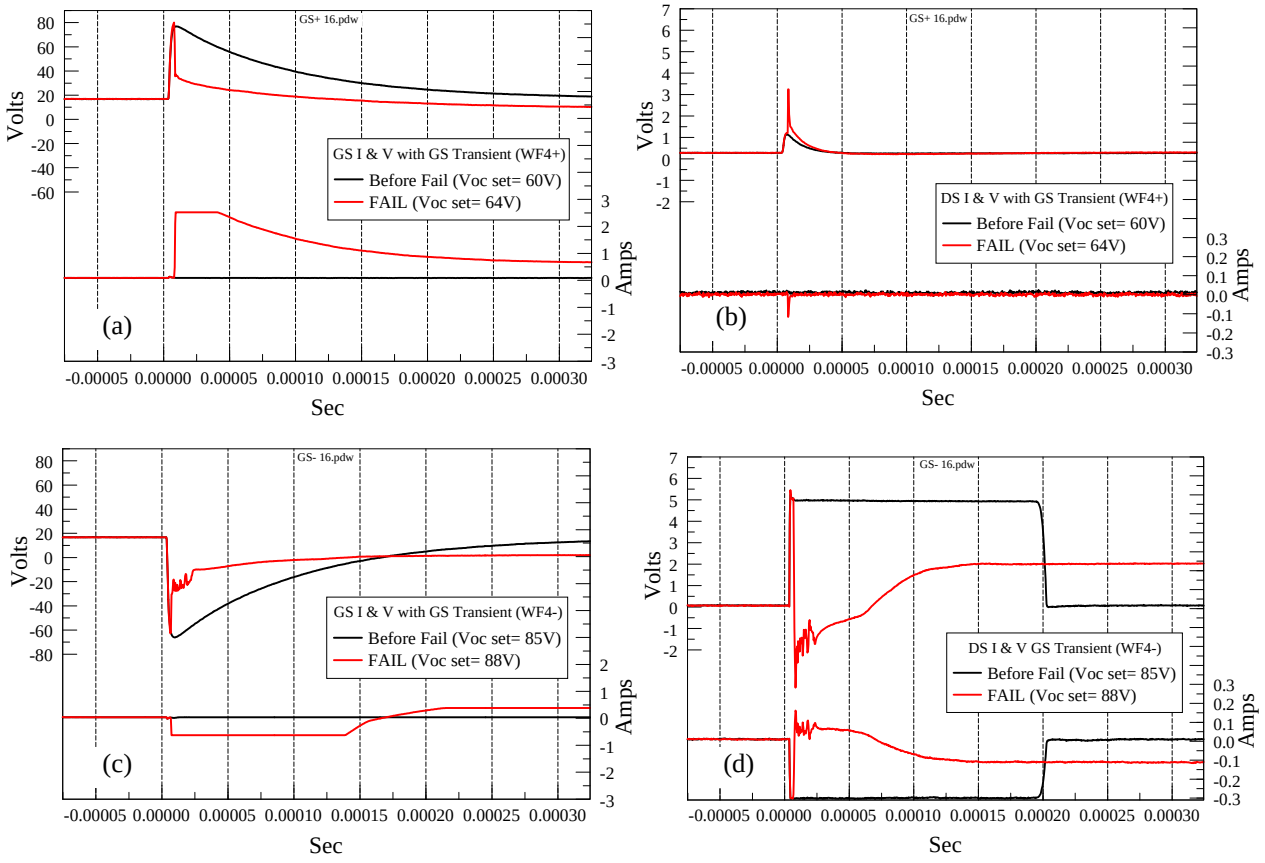


Figure 15: Comparison of Fail Levels with WF4+ and WF4- injected into MOSFET GS terminals. (WF4+, ②G-S pin config. Top: a & b) (WF4-, ❷ G-S pin config. Bottom: c & d) $V_{GS\text{-}bias}$= 16 Volts for these data. The plots on the left (a & c) are GS voltages and currents. The plots on the right (b & d) are the corresponding DS voltages and currents resulting from the injection on the GS terminals.

Figure 15 ($V_{GS\text{-}bias}$= 16 Volts) should be compared with Figure 13 ($V_{GS\text{-}bias}$= 8 Volts). The four plots appear remarkably similar, with a few observations. When injecting WF4+, device failure tended to occur with V_{GS}= 80V (80.00 for $V_{GS\text{-}bias}$=16V, 80.17 for $V_{GS\text{-}bias}$=8V). When injecting WF4-, device failure tended to occur with V_{GS}= 63.5V (-62.88 for VGS-bias=16V, -64.71 for VGS-bias=8V). Thus GS Fail levels appear related to absolute peak V_{GS}.

DS Injection, $V_{GS\text{-}bias}$= 16V: Figure 16 shows fail data when WF4+/- was injected into the DS terminals with $V_{GS\text{-}bias}$= 16V. Black traces show measured V and I using a MIG0600MS Peak Voc setting ("Voc set") below the level observed to cause failure. Red traces show measured V and I with peak Voc set at the level observed to cause failure.

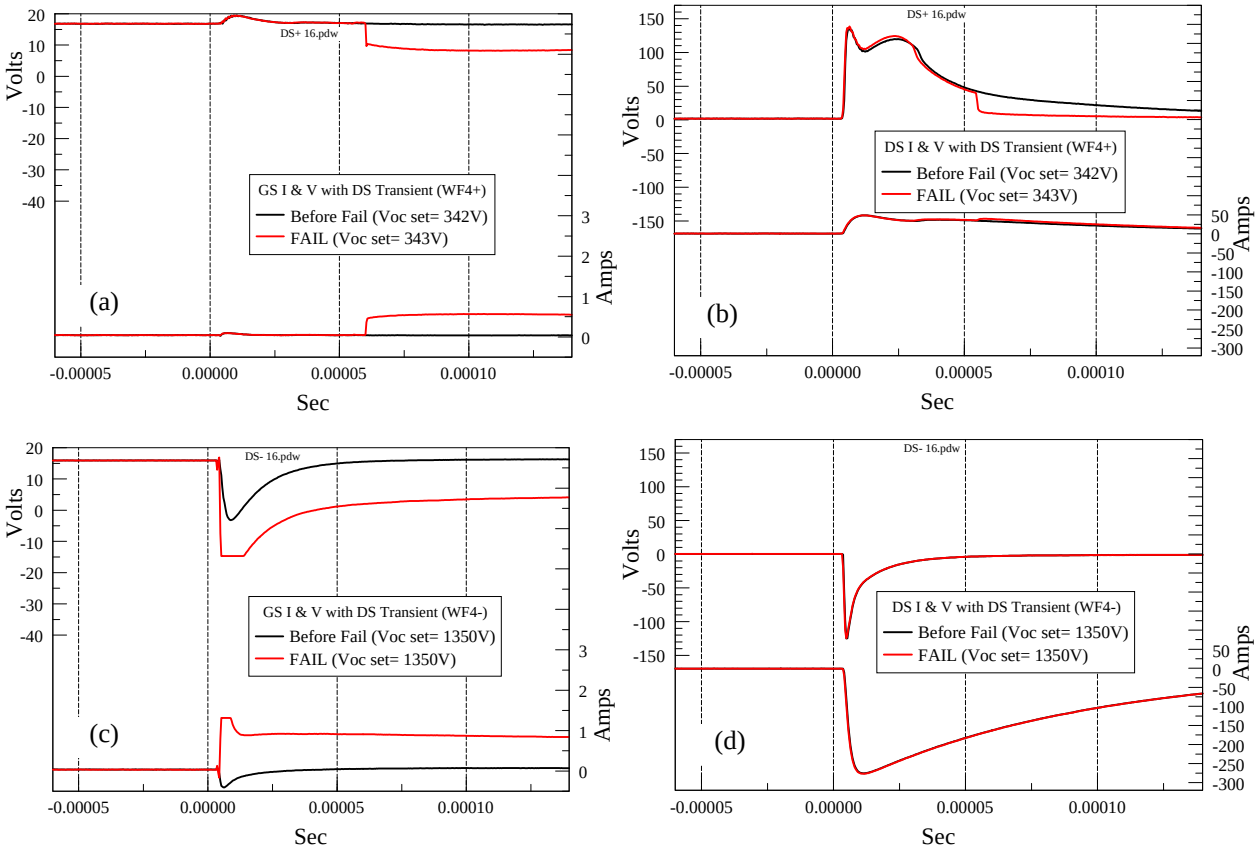


Figure 16: Comparison of Fail Levels with WF4+ and WF4- injected into MOSFET DS terminals. (WF4+, ③D-S pin config. Top: a & b.) (WF4-, ❸ D-S pin config. Bottom: c & d.) $V_{GS\text{-}bias}$= 16 Volts for these data. The plots on the right (b & d) are the DS voltages and currents. The plots on the left (a & c) are the corresponding GS voltages and currents resulting from the injection on the DS terminals.

The four plots of Figure 16 ($V_{GS\text{-}bias}$= 16 Volts) are similar to the four plots of Figure 14 ($V_{GS\text{-}bias}$= 8 Volts). For both, the time-of-failure appeared delayed about 50us when injecting WF4+ into the DS terminals, possibly indicating a thermal damage characteristic. For WF4+, increasing $V_{GS\text{-}bias}$ to 16 volts increased the damage tolerance of the V_{DS} junction about 25% (ΔVoc Set= 67 Volts), and nearly doubled the maximum I_{DS} (25.4A for $V_{GS\text{-}bias}$ = 8V, vs. 48.5A for $V_{GS\text{-}bias}$ = 16V). Injecting high enough WF4+ into the DS terminals permanently lowered the GS impedance, even after the transient had passed (see Table 9).

As in Figure 14, when a WF4- transient is injected into the DS terminals, damage becomes evident when observing the GS junction rather than the DS junction data. Increasing $V_{GS\text{-}bias}$ to 16 volts *decreased* the maximum V_{DS} about 7% (ΔVoc Set= -110 Volts), and *decreased* the maximum $|I_{DS}|$ about 6% (-295A for $V_{GS\text{-}bias}$ = 8V, vs. -277A for $V_{GS\text{-}bias}$ = 16V). Injecting high enough WF4- into the DS terminals permanently lowered the GS impedance, with $V_{GS\text{-}bias}$ = 16V enhancing the effect (see Table 9).

Table 9: R_{GS} Before and After DS Injection

Threat Waveform	**$V_{GS\ Bias}$ (Volts)**	**$R_{GS\text{-}Normal}$ (V_{Normal}/I_{Normal}, Ohms)**	**$R_{GS\text{-}Fail}$ (V_{Fail}/I_{Fail}, Ohms)**
4+ (③D-S)	8	186 (8.0V/0.043A)	13.8 (4.0V/0.29)
	16	391 (16.8V/0.043A)	19.2 (9.6V/0.50A)
4- (❸D-S)	8	103 (9.3V/0.09A)	22.7 (6.8V/0.30A)
	16	454 (15.9V/0.035A)	**6.7** (5.0V/0.75A)

Oscilloscope data were evaluated to determine the actual MOSFET terminal voltage and current at failure (V_{Fail} Meas & I_{Fail} Meas). Table 10 shows lightning generator settings (Voc Set) required to cause MOSFET failure ("failure" is defined as device malfunction) for each Waveform and $V_{GS\text{-}bias}$ setting. ($V_{DS\text{-}bias}$ was always set at 5VDC.)

Table 10: MOSFET Fail Levels

Device SN	**WF**	**Pin Config.**	**$V_{GS\text{-}bias}$ (VDC)**	**Voc Set (Volts)**	**V_{Fail} Meas (Volts)**	**I_{Fail} Meas (Amps)**	**Filename**	**Figure**
D8	4+	② G-S	8	**70**	V_{GS}= 80.2	I_{GS}= 0.0958	0257	13
C7	4-	❷ G-S	8	**75**	V_{GS}= -64.7	I_{GS}= 0.0046	0190	
A2, A3	4+	③ D-S	8	**276**	$R_{GS\text{-}Normal}$= 186Ω; $R_{GS\text{-}Fail}$= 13.8Ω See Fig. 14a&b		0029, 0030	14
D7	4-	❸ D-S	8	**1460**	$R_{GS\text{-}Normal}$= 103Ω; $R_{GS\text{-}Fail}$= 22.7Ω See Fig. 14c&d		0237	
D9	4+	② G-S	16	**64**	V_{GS}= 80.0	I_{GS}= 0.0966	0260	15
C8	4-	❷ G-S	16	**88**	V_{GS}= -62.9	I_{GS}= 0.0335	0206	
A8	4+	③ D-S	16	**343**	$R_{GS\text{-}Normal}$= 391Ω; $R_{GS\text{-}Fail}$= 19.2Ω See Fig. 16a&b		0085	16
D5	4-	❸ D-S	16	**1350**	$R_{GS\text{-}Normal}$= 454Ω; $R_{GS\text{-}Fail}$= 6.7Ω See Fig. 16c&d		0232A	

4.1.4 Test Levels for Multiple Stroke Test Matrix

Previous testing has shown that a MOSFET may function within specification after surviving a test at a given Voc setting, but may fail at that same Voc setting on subsequent tests. The research team experimentally determined the highest Voc setting where a MOSFET can tolerate up to 20 lightning strokes without apparent failure. Such a test models a scenario where a MOSFET is subjected to about two lightning strikes. (A typical lightning strike contains about 10 strokes.[12]) Using the data from Table 9 as a guide, more MOSFETs were tested to determine the highest peak Voc setting where the device could tolerate 20 strokes without failure. The final data are shown in Table 11. As expected, the 20-stroke Pass Level was lower than the Single Stroke Fail Level for most pin configurations.

Table 11: MOSFET Pass Levels after 20 Strokes

Device SN	WF	Pin Config.	$V_{GS\text{-}bias}$ (VDC)	Voc Set (Volts)	Filename
E2	4+	② G-S	8	**65**	0269
G5	4-	❷ G-S	8	**68**	0298
S6	4+	③ D-S	8	**265**	0885*
G8	4-	❸ D-S	8	**1360**	0301
E7	4+	② G-S	16	**57**	0279
G1	4-	❷ G-S	16	**80**	0294
F3	4+	③ D-S	16	**320**	0286
F9	4-	❸ D-S	16	**1210**	0292

*Note: Significant testing of WF4+, ③ D-S, $V_{GS\text{-}bias}$= 8V was required due to "ringing" problem, discussed in Sec. 4.3.

NASA/TM-2009-215794 reported V_{Fail} Meas and I_{Fail} Meas data, assuming that MOSFET failures would occur instantaneously, as the applied voltage or current exceeded some threshold level. While WF4 injections into the G-S terminals tend cause failure as some peak threshold is exceeded, injections into the D-S terminals tend to cause failure about 50 microseconds after the WF4 peak amplitude has passed. Therefore, V_{Fail} Meas and I_{Fail} Meas data were considered not useful for inclusion into Table 11.

The 20-Stroke Pass Levels were taken to be the "High" setting for subsequent testing. "Medium" and "Low" settings were taken to be 90%, and 80% of "High", respectively. The values 80% and 90% were selected, somewhat arbitrarily, expecting that some statistical difference may be obtained from device failures after subsequent aging processes (thermal, vibration, etc.) subsequently being conducted at NASA Ames. A summary of the High, Medium, and Low Test Levels, along with Fail Levels is shown in Table 12.

Table 12: Final Test Voltage Levels (Voc Set) determined from Pre-Test

WF	Pin Config.	$V_{GS\text{-}bias}$ (VDC)	FAIL (Voc set)	HI Pass 20 Strokes (Voc set)	MED =90% of HI (Voc set)	Lo 1 =80% of HI (Voc set)	Lo 2 (Voc set)	Lo 3 (Voc set)
4+	② G-S	8	**70**	**65**	59	52		
4-	❷ G-S	8	**75**	**68**	61	54		
4+	③ D-S	8	**276**	**265**	239	212	200	120
4-	❸ D-S	8	**1460**	**1360**	1292	1224		
4+	② G-S	16	**64**	**57**	51	46		
4-	❷ G-S	16	**88**	**80**	72	64		
4+	③ D-S	16	**343**	**320**	288	256		
4-	❸ D-S	16	**1350**	**1210**	1150	1089		

4.2 Test Matrix

Table 11 provides a basis of Test Voltage Levels for the Test Matrix. The next step was to produce multiple samples of MOSFETS having been subjected to different test levels, varying numbers of strokes, different GS biasing, and varying pin-injection configurations, but still functional. The devices could then be subjected to various aging processes and statistical data obtained for latent failures. Table 13 shows the planned Test Matrix.

Table 13: MOSFET Test Matrix

Pin Config. & Polarity	**$V_{GS\text{-}bias}$ (VDC)**	**Voc Set Levels**	**Strokes**	**Samples Each**	**Devices Tested**
② G-S (WF4+)	8, 16	H, M, L	5, 10, 20	5	1 x 2 x 3 x 3 x 5= 90
③ D-S (WF4+)	8, 16	H, M, L	5, 10, 20	5	1 x 2 x 3 x 3 x 5= 90
❷ S-G (WF4-)	8, 16	H, M, L	5, 10, 20	5	1 x 2 x 3 x 3 x 5= 90
❸ S-D (WF4-)	8, 16	H, M, L	5, 10, 20	5	1 x 2 x 3 x 3 x 5= 90
Total Devices Needed					360

All MOSFET Test Matrix data are summarized in Table 14. The MOSFETS are subsequently being evaluated by NASA Ames researchers using their Aging and Characterization Platform for semiconductor components, for the purpose of developing predictive algorithms as part of IVHM prognostic health management program goals.

Table 14: MOSFET Test Matrix Data Summary

Pin Config	V_{GS}	Strokes	Level	Device SN & (Filenames)	Pin Config	V_{GS}	Strokes	Level	Device SN & Filenames
②G-S (WF4+)	8V	5	HI	G9 H0 H1 H2 H3 (0302 to 0311)	③D-S (WF4+)	8V	5	HI	RC RD RE RF RG (0835 to 0844); T2 T3 T4 T5 T6 (0896 to 0905)*; KM KN KP KR KS (1115 to 1124)
			MED	J1 J2 J3 J4 J5 (0330 to 0334)				MED	T7 T8 T9 U0 U1 (0906 to 0915)*; LT LU LV MK ML (1145 to 1154)
			LO1	J9 K0 K1 K2 K3 (0345 to 0349)				LO1	V2 V3 V4 V5 V6 (0936 to 0945)* NM NN NP NR NS (1175 to 1184)
		10	HI	H4 H5 H6 H7 H8 (0312 to 0321)				LO2	CT CU CV DK DL (0966 to 0975)
			MED	I4 I5 I6 I7 I8 (0335 TO 0339)				LO3	EM EN EP ER ES (0996 to 1005)
			LO1	K4 K5 K6 K7 K8 (0350 TO 0354)			10	HI	RH RI RJ ~~R0 R1~~ (0845 to 0854); S7 S8 S9 TO T1 (0886 to 0895)*; KT KU LK KV LL (1125 to 1134)
		20	HI	H9 I0 I1 I2 I3 (0322 to 0329)				MED	U2 U3 U4 U5 U6 (0916 to 0925)*; MM MN MP MR MS (1155 to 1164)
			MED	I9 J0 J6 J7 J8 (0340 to 0344)				LO1	V7 V8 V9 CK CL (0946 to 0955)* NT NU NV PK PL (1185 to 1194)
			LO1	K9 L0 L1 L2 L3 (0355 to 0359)				LO2	DM DN DP DR DS (0976 to 0985)
	16V	5	HI	BH BI BJ CA CB (0567 to 0576)				LO3	ET EU EV FK FL (1006 to 1015)
			MED	DC DD DE DF DG (0595 to 0604)			20	HI	S2 S3 S4 S5 S6 (0876 to 0885)*; LM LN LP LR LS (1135 to 1144)
			LO1	EH EI EJ FA FB (0625 to 0634)				MED	U7 U8 U9 V0 V1 (0926 to 0935)*; MT MV MU NK NL (1165 to 1174)
		10	HI	CC CD CE CF CG (0577 to 0586)				LO1	CM CN CP CR CS (0956 to 0965)*; PM PN PP PR PS (1195 to 1204)
			MED	DH DI DJ EA EB (0605 to 0614)				LO2	DT DU DV EK EL (0986 to 0995)
			LO1	FC FD FE FF FG (0635 to 0644)				LO3	FM FN FP FR FS (1016 to 1025)
		20	HI	CH CI CJ DA DB (0587 to 0594)		16V	5	HI	GC GD GE GF GG (0655 to 0664)
			MED	EC ED EE EF EG (0615 to 0624)				MED	HH HI HJ IA IB (0685 to 0694)
			LO1	FH FI FJ GA GB (0645 to 0654)				LO1	JC JD JE JF JG (0715 to 0724)
❷G-S (WF4-)	8V	5	HI	L7 L8 L9 P0 P1 (0388 to 0397)			10	HI	GH GI GJ HA HB (0665 to 0674)
			MED	N2 N3 N4 N5 N6 (0417 to 0426)				MED	IC ID IE IF IG (0695 to 0704)
			LO1	M7 M8 M9 W0 W1 (0447 to 0456)				LO1	JH JI JJ KA KB (0725 to 0734)
		10	HI	P2 P3 P4 P5 P6 (0398 to 0407)			20	HI	HC HD HE HF HG (0675 to 0684)
			MED	N7 N8 N9 M0 M1 (0427 to 0436)				MED	IH II IJ JA JB (0705 to 0714)
			LO1	W2 W3 W4 W5 W6 (0457 to 0466)				LO1	KC KD KE KF KG (0735 to 0744)
		20	HI	P7 P8 P9 N0 N1 (0408 to 0416)	❸ D-S (WF4-)	8V	5	HI	FT FU FV GK GL (1026 to 1035)
			MED	M2 M3 M4 M5 M6 (0437 to 0446)				MED	HM HN HP HR HS (1055 to 1064)
			LO1	W7 W8 W9 X0 X1 (0467 to 0476)				LO1	IT IU IV JK JL (1085 to 1094)
	16V	5	HI	AC AD AE AF AG (0537 to 0546)			10	HI	GM GN GP GR GS (1036 to 1044)
			MED	Y7 Y8 Y9 Z0 Z1 (0507 to 0516)				MED	HT HU HV IK IL (1065 to 1074)
			LO1	X2 X3 X4 X5 X6 (0477 to 0486)				LO1	JM JN JP JR JS (1095 to 1104)
		10	HI	AH AI AJ BA BB (0547 to 0556)			20	HI	GT GU GV HK HL (1045 to 1054)
			MED	Z2 Z3 Z4 Z5 Z6 (0517 to 0526)				MED	IM IN IP IR IS (1075 to 1084)
			LO1	X7 X8 X9 Y0 Y1 (0487 to 0496)				LO1	JT JU JV KK KL (1105 to 1114)
		20	HI	BC BD BE BF BG (0557 to 0566)		16V	5	HI	KH KI KJ LA LB (0745 to 0754); PT PU PV RK RL (1205 to 1214); VM VN VP VR VS (1295 to 1304)
			MED	Z7 Z8 Z9 AA AB (0527 to 0536)				MED	MC MD ME MF MG (0775 to 0784); SM SN SP SR SS (1235 to 1244); WT WU WV XK XL (1325 to 1334)
			LO1	Y2 Y3 Y4 Y5 Y6 (0497 to 0506)				LO1	NH NI NJ PA PB (0805 to 0814); TT TU TV UK UL (1265 to 1274)
							10	HI	LC LD LE LF LG (0755 to 0764); RM RN RP RR RS (1215 to 1224); VT VU VV WK WL (1305 to 1314)
								MED	MH MI MJ NA NB (0785 to 0794); ST SU SV TK TL (1245 to 1254); XM XN (1335 to 1338)
								LO1	PC PD PE PF PG (0815 to 0824); UM UN UP UR US (1275 to 1284)
							20	HI	LH LI LF MA MB (0765 to 0774); RT RU RV SK SL (1225 to 1234); WM WN WP WR WS (1315 to 1324)
								MED	NC ND NE NF NG (0795 to 0804); TM TN TP TR TS (1255 to 1264)
								LO1	PH PI PJ RA RB (0825 to 0834); UT UU UV VK VL (1285 to 1294)

Notes: -Red Devices were "shiny" devices- Not Type N. (Hi Level: Voc Set=275V only for the IRF520 devices. More information below. See Fig. 17.)
-Failed Devices are labeled with ~~strikethrough~~
-* "Ringing" observed on some tests. Resolved with Ferrite placed on GS power supply beginning with file 0966. (See Section 4.3 for more information.)
-Blue Devices tested, but only Ch4 Oscilloscope data were saved.

4.2.1 IRF520 Versus IRF520N Devices

During the course of testing with DS pin-injection, some IRF520 devices were accidentally mixed-in with the IRF520N test samples. Data for these devices was collected, and is differentiated in red color in Table 14. The difference was discovered, and the tests were repeated on IRF520N devices. It was experimentally determined that the IRF520 devices could sustain 20 strokes at Voc set at 275V, but the IRF520N devices needed Voc set to 265V in order to sustain 20 strokes without failure. Figure 17 shows a photograph of the two different types of MOSFET. Figure 18 shows oscilloscope data comparisons between the IRF520 (Black) and IRF520N (Blue).

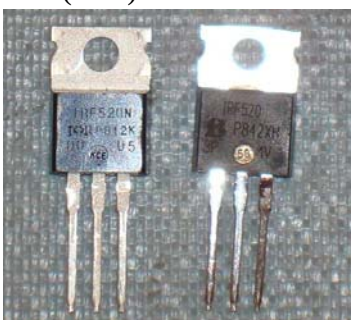


Figure 17: IRF520N (left) versus IRF520 (right, "shiny") MOSFETS.

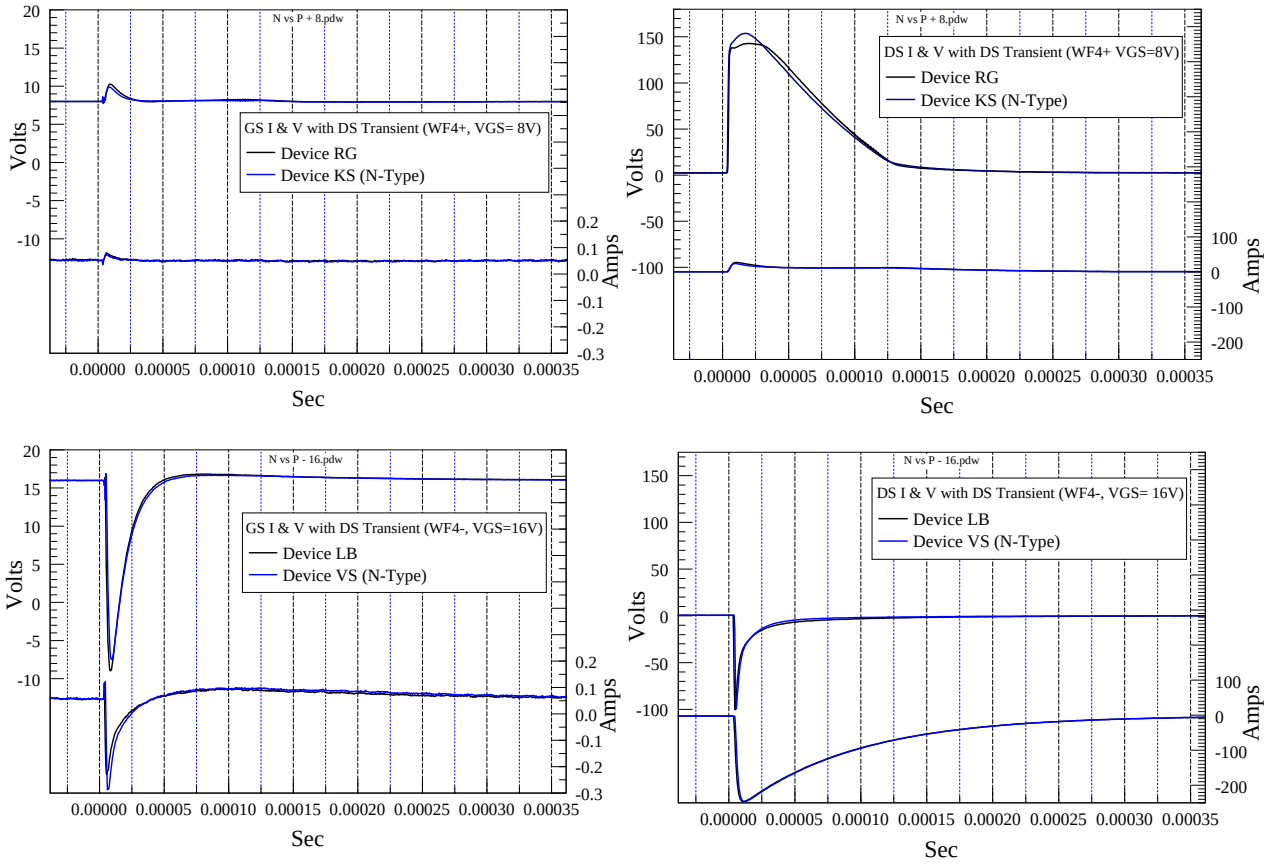


Figure 18: Comparison of Fail Levels with WF4+ and WF4- injected into MOSFET DS terminals. (WF4+, ③D-S pin config. $V_{GS\text{-}bias}$= 8 Volts, Top: a & b.) (WF4-, ❸ D-S pin config. $V_{GS\text{-}bias}$= 16 Volts, Bottom: c & d.) for these data. The plots on the right (b & d) are the DS voltages and currents. The plots on the left (a & c) are the corresponding G-S voltages and currents resulting from the injection on the D-S terminals.

4.3 The "Ringing" Anomaly

During D-S injection testing with WF4+ and $V_{GS\text{-}bias}$= 8VDC, "ringing" was observed on all four oscilloscope channels (see Fig. 19, Ch. 1: V_{GS}, Ch. 2: I_{GS}, Ch. 3: V_{DS}, Ch. 4: I_{DS}). Ringing was increasingly likely with Voc Set levels exceeding 160V. The ringing randomly occurred for about half the injection tests, otherwise it was not present. Initial troubleshooting included replacing TVS devices, the MOSFET circuit board, R4 and MOSFET, but these did not influence the ringing phenomena.

When performing D-S injection testing with $V_{GS\text{-}bias}$= 16VDC, the ringing phenomena did not re-occur for either WF4+ or WF4-.

Subsequent D-S injection testing with $V_{GS\text{-}bias}$= 8VDC and WF4+ again caused ringing, randomly, for about half the injection tests. It was observed that placing a ferrite core around either the positive or negative terminal of the $V_{GS\text{-}bias}$ power supply eliminated the ringing. Placing the ferrite core over either $V_{DS\text{-}bias}$ power supply terminal had no effect. The Test Matrix was completed using the ferrite core installed on the $V_{GS\text{-}bias}$ power supply positive terminal. A photograph of the ferrite core, installed, is provided as Figure 20.

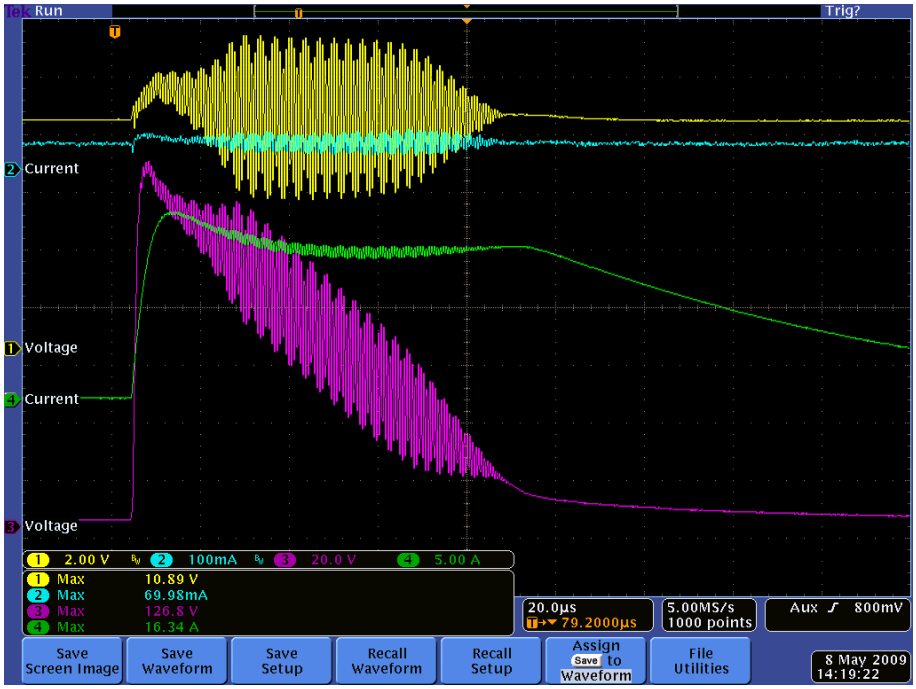


Figure 19: Oscilloscope display of "ringing" phenomena. (Ch. 1: V_{GS}, Ch. 2: I_{GS}, Ch. 3: V_{DS}, Ch. 4: I_{DS})

After completion of the Test Matrix, other options for providing low-pass filtering on the GS biasing circuit were evaluated. All options essentially eliminated higher frequency coupling to the power supply, and mitigated the ringing. These included the following:

- Replace V_{GS} power supply with 9V battery
- Replace V_{GS} power supply with 4 "D" cells (6.43V)
- Place 22,000 uF capacitor in parallel with V_{GS} power supply terminals.

Figure 20: Installation of ferrite core on V_{GS}+ Power supply terminal.

4.4 Survey of Damage Assessment Techniques Based Upon Inspection

The ability to understand the physics of semiconductor failure is useful for diagnosis and prognosis of failures caused by lightning and other EMI events. The research team evaluated several damage assessment techniques based upon inspection. Optical and electron microscopy inspection requires removal of semiconductor packaging and cross-sectioning, rendering the device unusable for inspection of other cross-sections. Non-destructive inspection techniques use wavelengths that penetrate the semiconductor package, without damaging it, and include X-Ray and ultrasonic imaging of the die and wiring internal to the package. These imaging technologies are available to many research facilities and universities. MIL-STD-883E describes some use of X-Ray, ultrasonic imaging and microscope inspection techniques for evaluating workmanship and durability of microcircuits.

After the Test Matrix was completed, 24 additional MOSFETs were subjected to lightning transient tests, for the purpose of providing samples for damage assessment based upon inspection. After review of the Fail Level data, test conditions were set for the following rationale:

- Reference Device: No Transient applied. (Device SN 2R)
- 3 Voc Set Levels: V_{Fail}, 2 x V_{Fail}, $V_{Hi\text{-}20\ Strokes}$: Intent was to ensure damage on one device (2x), while inducing varying degrees of damage for comparison.
- Both G-S and D-S pin configurations (Not G-D): Pre-Test data indicate that different failure mechanisms are occurring on GS versus DS injections.
- Both Polarities of WF4, + and –: Pre-Test data indicate that different failure mechanisms are occurring for + and – waveforms.
- Gate Bias= 16V: Fail levels for DS injection were lower for V_{GS}= 16V than for V_{GS}= 8V, and were so high that a 2x test was not possible anyway. V_{GS}= 16V provided higher confidence of more damage.
- 2 Samples of Each Device.

A Test Matrix for the 24 devices is shown in Table 15.

Table 15: Devices Tested to Fail, for Damage Assessment Based Upon Inspection.

Device SN	Device Sample	WF4 +/-	Inj. Term.	V_{GS}	Voc Set	Stroke #	Results	Filename
1G	1	4+	G-S ②	16	64	1	V_{Fail}	1351
1H	2	4+	G-S ②	16	64	1	V_{Fail}	1352
1I	1	4+	G-S ②	16	128	1	$2xV_{Fail}$	1353
1J	2	4+	G-S ②	16	128	1	$2xV_{Fail}$	1354
1K	1	4+	G-S ②	16	57	20	$V_{Hi\text{-}20\ Strokes}$	1355
1L	2	4+	G-S ②	16	57	20	$V_{Hi\text{-}20\ Strokes}$	1356
1M	1	4+	D-S ③	16	343	1	V_{Fail}	1357
1N	2	4+	D-S ③	16	343	1	V_{Fail}	1358
1P	1	4+	D-S ③	16	686	1	$2xV_{Fail}$	1359
1R	2	4+	D-S ③	16	686	1	$2xV_{Fail}$	1360
1S	1	4+	D-S ③	16	320	20	$V_{Hi\text{-}20\ Strokes}$	1361
1T	2	4+	D-S ③	16	320	20	$V_{Hi\text{-}20\ Strokes}$	1362
1A	1	4-	G-S ❷	16	88	1	V_{Fail}	1345
1B	2	4-	G-S ❷	16	88	1	V_{Fail}	1346
1C	1	4-	G-S ❷	16	176	1	$2xV_{Fail}$	1347
1D	2	4-	G-S ❷	16	176	1	$2xV_{Fail}$	1348
1E	1	4-	G-S ❷	16	80	20	$V_{Hi\text{-}20\ Strokes}$	1349
1F	2	4-	G-S ❷	16	80	20	$V_{Hi\text{-}20\ Strokes}$	1350
XP	1	4-	D-S ❸	16	1350	1	V_{Fail}	1339
XR	2	4-	D-S ❸	16	1350	1	V_{Fail}	1340
XS	1	4-	D-S ❸	16	1700	1	$2xV_{Fail}$	1341
XT	2	4-	D-S ❸	16	1700	1	$2xV_{Fail}$	1342
XU	1	4-	D-S ❸	16	1210	20	$V_{Hi\text{-}20\ Strokes}$	1343
XV	2	4-	D-S ❸	16	1210	20	$V_{Hi\text{-}20\ Strokes}$	1344

(Device SN 2R was not exposed to any lightning transient: i.e. Reference Device)

4.4.1 Microscope Inspection

Solid state devices are packaged to provide reliable operation under extreme thermal, vibration and chemical environments. Evidence of heating or burning on the solid state package may be observable if the device is subjected to sufficient energy input, however it's far more likely that damage to the semiconductor die, adhesive, or wire bonding would occur prior to damage to the packaging. Such device damage is not possible to see without the packaging removed. Figure 21 shows an IRF520 MOSFET that was cross-section cut to reveal the die and bonding wire.

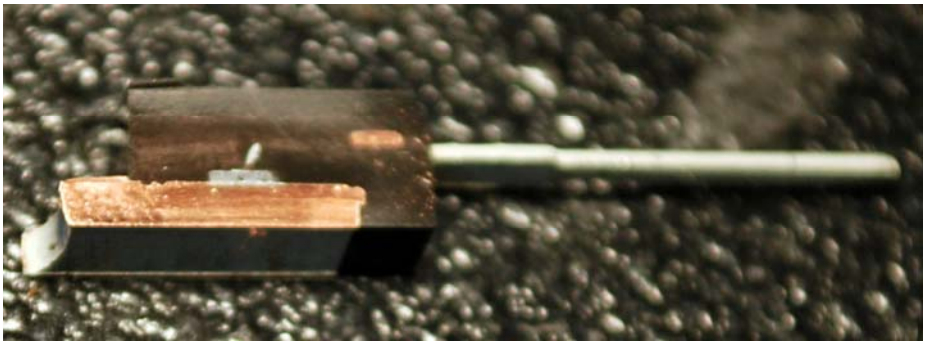


Figure 21: Cross Section cut performed on IRF520 MOSFET.

Microscope inspection of the die is possible, but requires precision cutting and maybe polishing to allow proper focusing on a particular region of interest. Overall die dimensions are about 2mm x 2mm. It may be possible to chemically dissolve the packaging material, while leaving the semiconductor die, adhesive, or wire bonding intact, but this was not pursued.

Determining specific damage using microscopic inspection would also require prior knowledge of the die design, and where to look for damage. The difficulty of performing microscopic inspection increases significantly for more complex logic devices. Images of electrostatic discharge (ESD) damage to integrated circuits may be found on the Internet, some obtained by using a scanning electron microscope (SEM). Inspection using a SEM requires extremely precise positioning of the target and a metalized coating to be applied to the inspection region.

4.4.2 X-Ray Inspection

The NASA LaRC Nondestructive Evaluation Sciences Branch (D313) provided the service of an X-TEK HMX ST X-Ray and computed tomography (CT) scanner. Figure 22 shows images obtained of a IRF520N MOSFET die and internal wiring.

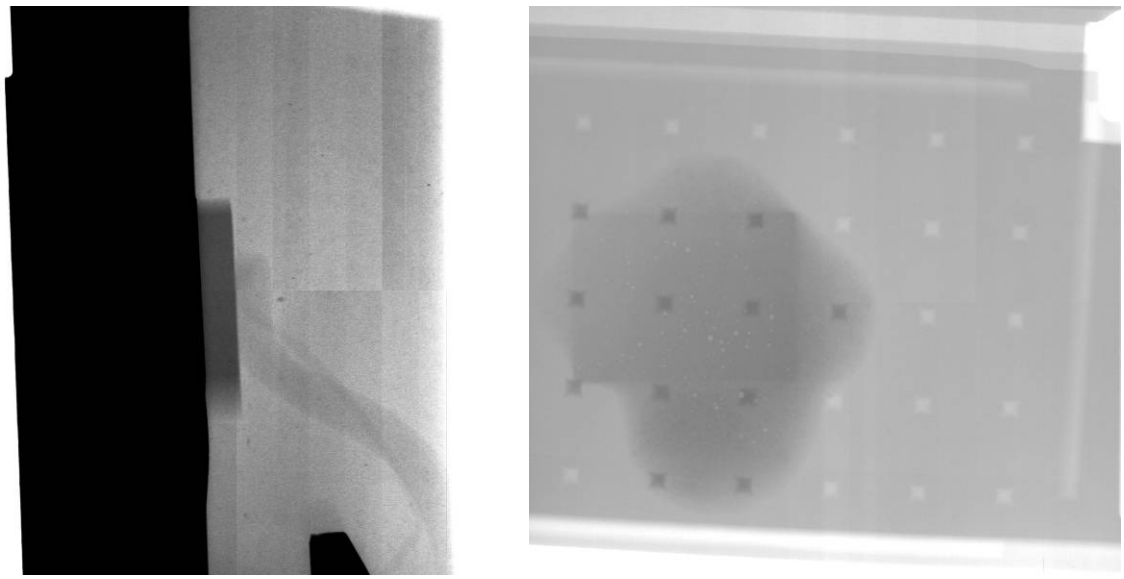


Figure 22: X-Ray images of IRF520N MOSFET die, adhesive and internal wiring.

X-Ray scans were particularly suited for revealing the major components present within the MOSFET package: heat sink, wiring, adhesive, and the semiconductor die. However, it was not possible to resolve details on the die itself, or the integrity of wire-bonding to the die. Often, it was difficult to resolve the internal wiring. Several other semiconductor packages were also imaged, with varying degrees of success, but did not provide confidence that X-ray inspection is useful for detecting damage within the die caused by lightning waveforms.

Further evaluation of the devices shown in Table 15 may occur at a later date.

5 Preliminary Damage Assessment Based on Electrical Parameters

The primary objective of the testing was to provide a set of MOSFETs suitable for analysis of damage effects, aging, and development of damage propagation models. Electrical characterization tests were performed to obtain an approximate measurement of the damage incurred by the injected-devices using a source measurement unit (SMU). The SMU used was a Keithley 2410 series. Specifically, the parameters that were tested are described below:

- Breakdown voltage $V_{(BR)DSS}$: Voltage level at which the drain-source path of the device starts conducting drain current, given that the gate is not biased. Essentially measures the breakdown rating of the body diode. Thus, under normal operation, this current should be very low (in the μA range) since the drain-source path behaves like an open circuit when the gate-bias is 0. As the applied voltage V_{DS} increases it approaches the breakdown rating of the diode and a significantly large current starts flowing through the drain.
- Leakage Current I_{DSS}: Current flowing from drain to source as the gate is shorted with the source (no gate bias). Represents the leakage current characteristics of the body diode.
- Threshold Voltage $V_{GS(th)}$: Minimum voltage required to bias the gate in order for the device to switch ON and allow drain current to flow. The SMU equipment provides a voltage sweep and measures the corresponding drain current till V_{GS} reaches a value where the drain current starts growing exponentially.

NASA/TM-2009-215794 provides additional information about Breakdown Voltage, Leakage Current and Threshold Voltage, including schematic diagrams.

It was generally observed from the SMU analysis that for WF4-, D-S (❸), extremely high voltages were required to produce any significant damage. Similarly for WF4+, D-S (③), high levels of injection (lower than that for the WF4-, D-S ❸ configuration) were required to observe any damage. In most cases, for such high levels of injections, the devices were completely destroyed. However, significant damage could be observed in many cases with much lower injection voltage for the G-S (both ② and ❷) configurations. Thus, it is of more interest to analyze these cases as they are more susceptible to damage. This preliminary assessment will focus on the injections using WF4+, G-S (②) configurations only.

Table 16 shows the damage levels observed using the SMU for the injection at the gate. The normalized change in parameter values for the affected devices was calculated in order to estimate the effect of the different configurations. The mean values of the normalized parameter changes are also shown in the Table 16.

For the G-S configuration, it was observed that the threshold voltage decreased with increase in the voltage intensity, gate bias, number of strokes and a combination of these factors. It was also observed that in the injection configuration with high intensity and 20 strokes, a very high deviation occurred in the device behavior. Not only was significant leakage (I_{DSS}) observed, in many cases the breakdown characteristic was completely altered. This was observed for both gate bias voltage values of 8V and 16V. Figures 22, 23 and 24 are shown for one such case. As observed from these characteristics, the devices have incurred very high damage and in general may not be used for further normal operation. However, for lower levels of injection intensity, such high levels of damage were not observed, as seen in Table 16 only the threshold voltage decreased. Figure 25 shows the decrease in threshold voltage for such a device. The authors suggest that this decrease in threshold voltage may be explained in the following manner: As the intensity of the injection applied at the gate is increased, the oxide and the underlying silicon started incurring damage which starts modifying the turn-on behavior. As this injection is further intensified, the

gate-oxide starts to breakdown which can then lead to conductive paths within the oxide. Such conduction paths would create various sources of leakage currents leading to significantly non-ideal behavior of the device. In addition, the body of the device also undergoes very high stress due to the high current flowing through it, as well as the presence of the high electric field. Damage to the body gets reflected in our characterization curves through the breakdown voltage and leakage current characteristics (Figures 23 and 24).

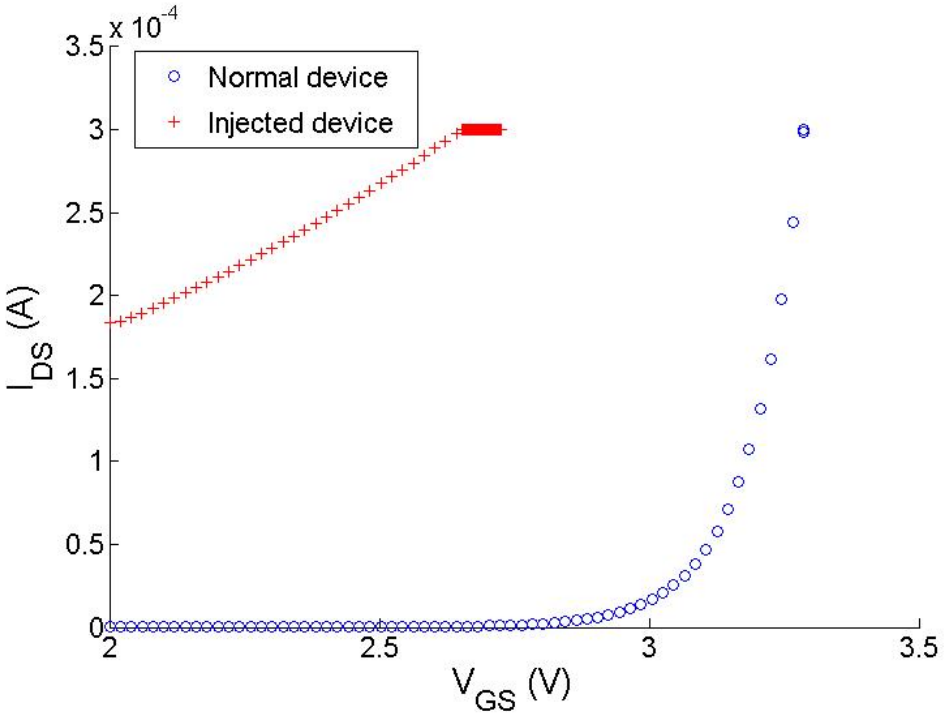


Figure 22: Turn-On characterization for lightning injected device in GS configuration, injection intensity H, strokes = 20 and gate bias = 8V

Table 16: Summary of change in device characterization after lightning waveform injection. All data is with WF4+ pin injection (②).

Pin Config.	**Voc Set Levels**	**$V_{GS\text{-}bias}$ (VDC)**	**Strokes**	**Results**
G-S	H	8	5	Mean decrease in $V_{GS(th)}$ by 0.0243V
G-S	H	8	10	Mean decrease in $V_{GS(th)}$ by 0.0647V
G-S	H	8	20	Devices were significantly damaged with high leakage
G-S	M	16	All	Mean decrease in $V_{GS(th)}$ by 0.0095V
G-S	H	16	5	Mean decrease in $V_{GS(th)}$ by 0.0361V
G-S	H	16	10	Mean decrease in $V_{GS(th)}$ by 0.0847V
G-S	H	16	20	Devices were significantly damaged with high leakage

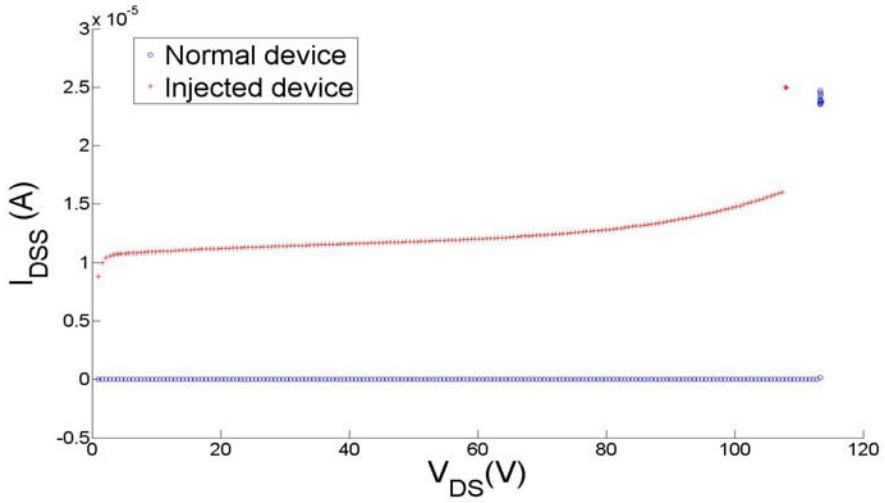


Figure 23: Leakage characterization for lightning injected device in GS configuration, injection intensity H, strokes = 20 and gate bias = 8V.

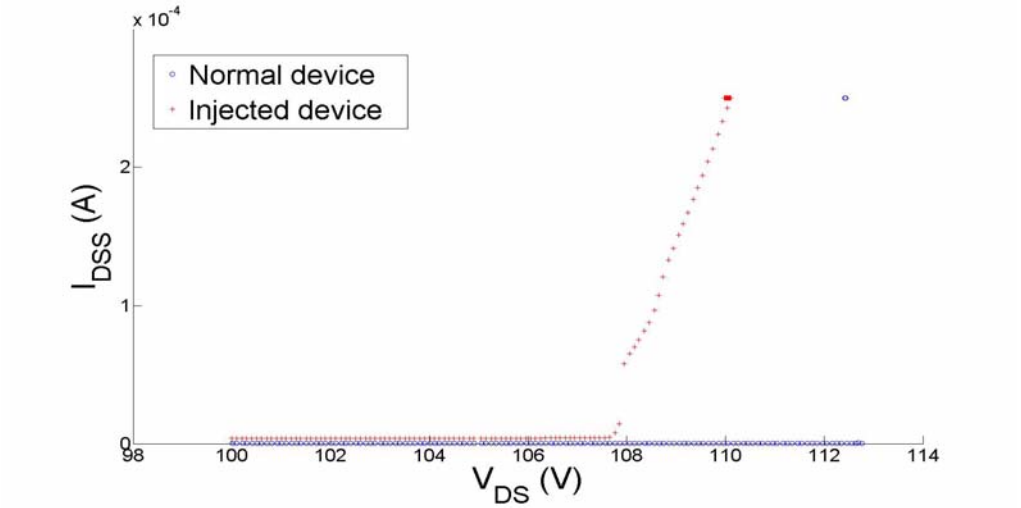


Figure 24: Breakdown characterization for lightning injected device in GS configuration, injection intensity H, strokes = 20 and gate bias = 8V.

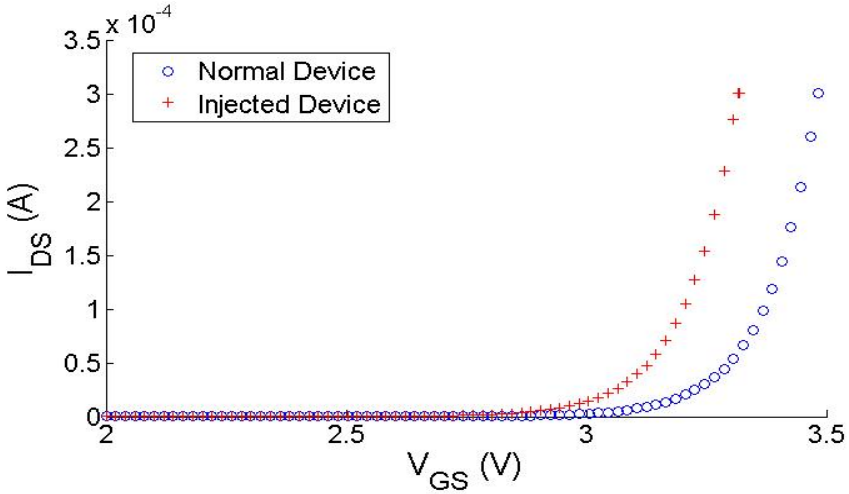


Figure 25: Turn-On characterization for lightning injected device in GS configuration, injection intensity M, strokes = 10 and gate bias = 8V.

6 Summary and Conclusions

This report describes lightning pin injection tests with IRF520N MOSFETs in the "ON" state. Test setups, test problems and solutions, device fail-levels, Test Matrix, and survey of damage assessment techniques based upon inspection, are provided herein. Table 14 includes a comprehensive matrix of all MOSFETs available to for ongoing NASA Ames semiconductor fault mode and aging research.

A pin-injection test circuit was designed, fabricated and demonstrated to meet the necessary criteria:

- Protection of biasing circuitry from the lightning transient.
- Protection of the MOSFET from excessive current applied by biasing circuitry.
- Protection of the Lightning Generator from excessive current applied by biasing circuitry.
- Assurance that biasing circuitry does not corrupt the MOSFET test results by modifying the lightning transient waveform.

Results show that GS-injection failures appear related to peak applied voltage and DS-injection failures appear related to energy input. DS–injection failure results show that lightning transient susceptibility characteristics of MOSFETs are significantly affected by $V_{GS\text{-}bias}$. When performing certification testing on aircraft equipment, it's important to carefully consider the fact that lightning damage levels are dependent upon circuit operational parameters at the time of the strike.

RTCA/DO-160E suggests that connecting the lightning waveform generator via cable induction may be a suitable alternative to direct injection, especially if it becomes too difficult to meet the above criteria. (Direct injection was performed for this test.) Cable induction testing may provide the advantage of preserving system impedances and biasing levels to values representative of actual operation, however it may be difficult to ensure that the MOSFET biasing levels are representative of the entire range of operation.

RTCA/DO-160E also allows a representative circuit to be pin-injection tested, so that pins of a similar group can be qualified by similarity. Again, it's important to ensure that the MOSFET biasing levels on the other circuits are representative of their operational range.

A survey of damage assessment techniques based upon inspection is provided, and includes data for optical microscope and X-ray inspection. Microscope inspection of the semiconductor die requires precision cross-section cutting and prior knowledge of the die design just to know where to look for damage. Even then, it's uncertain what damage may look like. With X-Ray inspection, it was not possible to resolve details on the die itself, or the integrity of wire-bonding to the die.

Preliminary damage assessments based upon electrical parameters show that the threshold voltage ($V_{GS(th)}$) may decrease with subsequent lightning waveform strokes. Such changes are expected to affect the switching behavior of the device, since with a lower threshold voltage the MOSFET would take less gate voltage to turn ON and hence the device would switch ON much earlier. Thus the device may continue to function in a degraded manner, before complete failure eventually occurs.

Research to computationally model damage and better understand failure modes is ongoing. Device aging studies are focused upon inducing intrinsic failure mechanisms. With improved understanding of the aging process, the next step will be to age the MOSFETS that have been injected (see Table 14).

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14. ABSTRACT
The test objective was to evaluate MOSFETs for induced fault modes caused by pin-injecting a standard lightning waveform into them while operating. Lightning Pin-Injection testing was performed at NASA LaRC. Subsequent fault-mode and aging studies were performed by NASA ARC researchers using the Aging and Characterization Platform for semiconductor components. This report documents the test process and results, to provide a basis for subsequent lightning tests. The ultimate IVHM goal is to apply prognostic and health management algorithms using the features extracted during aging to allow calculation of expected remaining useful life. A survey of damage assessment techniques based upon inspection is provided, and includes data for optical microscope and X-ray inspection. Preliminary damage assessments based upon electrical parameters are also provided.

15. SUBJECT TERMS
IVHM; MOSFET; X-ray; Lightning; Pin injection

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