# Low-cost and accurate DAC linearity test with ultrafast Segmented Model Identification of Linearity Errors and Removal Of Measurement Errors (uSMILE-ROME)

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***Abstract*—The Digital–to–Analog-Converter (DAC) is one of the fundamental components of Analog and Mixed-signal circuits. Static linearity testing of high resolution high performance DACs traditionally requires a long time and is very expensive. In this paper, a low-cost ultrafast method of testing DACs is presented. The method utilizes a low cost on-board measurement device for capturing the output of the DAC, instead of a precise digital voltmeter. By using a segmented non-parametric model for the DAC's INL curve and thus reducing the number of unknowns, the test time is drastically reduced. Additionally, the linearity requirement on the measurement device is significantly relaxed by removing its non-linearity. The combination of these two methods results in drastic reduction in linearity test cost for DACs.**

***Keywords— digital-to-analog-converters, static linearity testing, segmented model, low-cost***

## I. Introduction

As one of the most fundamental blocks of analog and mixed signal (AMS) circuits, the digital-to-analog converter (DAC) is widely used in many areas such as audio, high definition television and cellular telephones. The DAC is usually deeply embedded in a system-on-chip (SoC). With the growth of the Internet-of-things, the DAC volume and performance requirements have improved significantly, while the test cost keeps increasing. Thus, there is an urgent need to develop low-cost methods for characterization and testing of DACs.

DAC testing includes the measurement of integral nonlinearity (INL) and differential nonlinearity (DNL), offset, gain error, spurious free dynamic range (SFDR), signal-to-noise ratio (SNR), total harmonic distortion (THD) etc. [1], [2]. It is challenging to accurately test the DAC in a cost-effective way for various reasons. Traditional testing of DAC static linearity is done using a digital voltmeter (DVM) or a digital waveform recorder [2]. The equipment is required to have significantly better accuracy and resolution than the specifications of the DAC itself. Moreover, multiple samples are needed to average out the noise. The testing time is long and the test equipment is expensive.

In the past, many researchers have proposed methods to reduce the cost of DAC testing. The proposed method in [3] applied stimulus error identification and removal (SEIR) [4] to obtain the ADC linearity first and estimate DAC INL/DNL with the ADC. However, the accuracy of the DAC INL/DNL estimation is limited and the test time is long. In [5], the authors developed a circuit with deterministic dynamic element matching (DDEM) ADC and a dithering DAC to test the DAC. It is capable of testing a 14-bit DAC with ADC at 6-bit linearity. But it has to use the proposed ADC circuit and it also has the long test time problem. In [6], Huang, et al, improved the test accuracy with DAC scaling using local histogram test with DAC to test the ADC performance. Then the ADC is used to test the DAC with voltage scaling. It is architecture dependent and it takes long testing time. In [7], Ting, et al, tested the current-steering DAC by measuring the major transition current difference with a current-controlled oscillator and counter. This method is fast and low-cost but it is highly architecture-dependent.

In this paper, a new testing method and algorithm are introduced for accurate linearity testing of DACs with dramatically reduced test time and cost. This is done in two ways. Firstly, the algorithm exploits the fact that the number of truly independent error sources is much smaller than the number of DAC codes at which linearity has to be tested. This enables linearity testing with much fewer samples than is traditionally required, and so, saves on test time. Secondly, the method proposes use of an on-board digitizer for measurement of the DAC output, instead of the traditionally used high accuracy digital voltmeter. This results in less test time per sample. This reduction in test time directly translates to reduction in test cost. Moreover, the algorithm relaxes the stringent linearity requirement on the measurement device by removing the errors introduced due to the nonlinearity of the

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device. This results in further cost savings.

## II. PROBLEM STATEMENT

To test the linearity of a DAC, the digital stimulus needs to be generated and the analog response needs to be captured. In the conventional method, the DAC input code is swept from 0 to the maximum code, and the output voltage at each code is measured using a digital voltmeter (DVM). To average out the noise, multiple samples are taken for each DAC code. These voltages are compared to the ideal expected voltage for each code, and the INL and DNL are calculated.

As the resolution of the DAC grows, the number of input codes and therefore the number of INLs/DNLs to be estimated grows exponentially. For an n-bit DAC, if H samples per code are needed for noise averaging, then a total of $H \times 2^n$ output voltages will have to be measured. Measuring these $H \times 2^n$ voltages takes a long time, and so the test cost is also high. For a 16-bit DAC, with H=64, over 4 million samples would be required. If the DAC has a sampling rate of 500KSPS, the data acquisition time alone would be around 10 seconds. Multi-site testing will reduce this time, but this still corresponds to a significant test cost.

Conventional wisdom also dictates that the measuring device must be much more accurate and precise than the device under test. In the case of DAC testing, the digitizer in the DVM must be at least 10 times more linear than the DAC under test. If the INL of the DAC is at the +/-2 LSB level, then the digitizer's non-linearity must be in the range of +/-0.2 LSB. This stringent requirement on the linearity means that a highly accurate DVM is required, thus increasing the test cost even further.

## III. THE PROPOSED METHOD

### A. Segmented model of DAC's INL

The conventional method essentially treats the INL/DNL error at each code as unrelated to each other, and so, the number of variables to be estimated is equal to the number of DAC codes. In reality, especially for high resolution DACs, the number of truly independent error sources is much smaller than the number of codes. For example, take a 16-bit R-2R DAC. The number of resistor mismatches is just $2 \times 16 - 1 = 31$ which is dramatically less than $2^{16} = 65,536$. Although there will be many more error sources, it is true that the non-idealities (mismatches, voltage coefficients, etc.) of a limited number of analog components determines the errors in the input output transfer curve of the DAC. In other words, all the INL/DNL errors are highly correlated and are deterministic functions of a much smaller number of independent errors.

This correlated nature of the INL/DNL DAC errors makes a strong case for a model based approach to DAC linearity testing. Instead of basing the model on circuit laws, the proposed method takes a fundamentally different approach. It models the DAC's INL curve with a segmented non-parametric model. The idea is very similar to the uSMILE algorithm developed previously for ADCs [8], and is described in detail in the following paragraphs.

The INL curve of the DAC is broken into many MSB segments according to the MSB (Most Significant Bits) value of the DAC input code. Take a 16-bit DAC for example. If 6 bits are used as the MSB, then the INL curve is divided into 64 different segments. Each of these segments has an error term associated with it. Let's call this error as $e_M(C_{MSB})$. The error terms associated with the MSB segments will then be $e_M(0), e_M(1), e_M(2)$ ..... $e_M(63)$ corresponding to the MSB code. Each of these segments in turn can be further divided into smaller segments. Say the next 5 bits are used as ISB (Intermediate Significant Bits), then each MSB segment gets divided into 32 ISB segments, each of which has an error term associated with it, denoted as $e_I(C_{ISB})$. If we stop the segmentation here, the variations within each ISB segment away from the ISB average values are captured by the 32 LSB errors (5 LSB bits). The error term associated with each LSB segment is denoted as $e_L(C_{LSB})$. The final INL value for code $C$ will be:

$$INL(C) = e_M(C_{MSB}) + e_I(C_{ISB}) + e_L(C_{LSB}) \quad (1)$$

Most DAC architectures are inherently segmented in this fashion, like binary weighted, R-2R, mDAC etc., and so, this segmented non-parametric model can be applied to the INL curve. Note that this segmented model is not valid for string or thermometer-coded type architectures. For example, if you had a segmented 15-bit DAC implemented as a 7-bit thermometer coded resistor DAC and an 8-bit R-2R DAC, then the segmentation of the INL curve must be carefully chosen such that the MSB bits are greater than or equal to 7, since the thermometer coded part does not have a segmented architecture. For example, a 7-4-4 segmentation of the INL curve is valid, and so is an 8-3-4 segmentation, but a 6-5-4 segmentation is not valid.

This segmented model of the DAC's INL drastically reduces the number of variables to be estimated, thus enabling us to estimate the INL/DNL of the DAC at each code with a much-reduced number of samples.

### B. Removal of error due to measurement device

As mentioned previously, conventional DAC outputs are captured with an accurate and precise digital voltmeter, which is costly and time-taking. In the proposed method, a non-linear on-board digitizer is used for this purpose. We say "non-linear" here because the error introduced due to the nonlinearity of the digitizer is completely removed by the method and algorithm proposed. This will be explained in detail later.

The basic idea of the Removal Of Measurement Error (ROME) method used here is similar to the USER-SMILE [9] method which has been proposed for accurate linearity testing of ADCs with non-linear input sources. For ADC static linearity testing, the ramp generator (stimulus) can be non-ideal and have non-linearities whereas the output is digital and thus assumed to have no error while being captured. For DAC testing, the input is ideal (sweep of digital code from all 0s to all 1s) but there can be errors in the measurement device,

which can be non-linear. Hence, in USER-SMILE, the stimulus error is removed, whereas in ROME, the measurement error is removed. The details of the method are described below.

The test setup is as follows. The DAC output voltage is sent to an on-board digitizer whose linearity can be much less than the linearity of the DAC. This digitizer should have sufficiently small quantization errors, meaning it cannot have large "dead-zones", where a very large voltage range gives the same output code. This is an easy condition to guarantee even if the digitizer has bad linearity performance. It should have no, or sufficiently small kickback to the DAC output. For static linearity test, this should be very easy to meet, and means that the measurement device's transient settles faster than the DAC settling time. This is not an extra requirement. High performance measurement devices also need to satisfy this. But this might be easier to satisfy for low cost measurement devices since the accuracy requirement is more relaxed. As an example, an ADC is used as the digitizer in this paper, but the method is not limited to using an ADC. The reference voltages for the DAC and the ADC are such that the output range of the DAC is less than the input range of the ADC. For each DAC code, two ADC output codes are obtained. The first ADC code is obtained when a positive voltage shift $\alpha$ is added to the output voltage of the DAC and then sent to the ADC for digitization. The second ADC code is obtained when the output voltage of the DAC is sent directly to the ADC. We assume that this shift $\alpha$ is constant for all the measurements. The value of this shift is not required to be accurate or known, but must be reasonable. There are several methods to generate this constant shift. Many of the constant shift generation methods developed for the SEIR algorithm [10], [11] can be used for this purpose. It is important to note that the ADC must not have wide codes or dead-zones which will result in many DAC codes giving the same ADC output code.

### C. Derivation of equations

For a given DAC code $C1_{DAC}$, let's say that the output voltage after addition of shift is $V1$. This voltage can be expressed as:

$$V1 = \left(C1_{DAC} + INL_D\left(C1_{DAC}\right)\right)l_{DAC} + o_{DAC} + \alpha + w1_{DAC} \quad (2)$$

where $INL_D$ is the INL function of the DAC, $l_{DAC}$ is the actual LSB of the DAC, $o_{DAC}$ is the offset of the DAC, $\alpha$ is the added voltage shift, and $w1_{DAC}$ is the additive noise. This same $V1$ becomes the input voltage to the ADC to give $C1_{ADC}$. The following equation can be written, with all variables corresponding to the ADC this time:

$$V1 = \left(C1_{ADC} + INL_A\left(C1_{ADC}\right)\right)l_{ADC} + o_{ADC} - w1_{ADC} - q1_{ADC} \quad (3)$$

Where $C1_{ADC}$ is the ADC output code, $o_{ADC}$ is the offset of the ADC, $w1_{ADC}$ is the additive noise, and $q1_{ADC}$ is the quantization noise of the ADC.

Similarly, for any DAC code $C2_{DAC}$, let's say that the DAC output voltage, without shift, is $V2$, which can be expressed as:

$$V2 = \left(C2_{DAC} + INL_D\left(C2_{DAC}\right)\right)l_{DAC} + o_{DAC} + w2_{DAC} \quad (4)$$

This voltage, when sent directly to the ADC for measurement, gives ADC code $C2_{ADC}$. The voltage $V2$ can again be expressed as:

$$V2 = \left(C2_{ADC} + INL_A\left(C2_{ADC}\right)\right)l_{ADC} + o_{ADC} - w2_{ADC} - q2_{ADC} \quad (5)$$

Subtracting equations (2) and (4) and then equating that to the difference of equations (3) and (5), we get:

$$\begin{aligned}&\left[\left(C1_{DAC} - C2_{DAC}\right) + \left(INL_D\left(C1_{DAC}\right) - INL_D\left(C2_{DAC}\right)\right)\right]l_{DAC} + \alpha = \\ &\left[\left(C1_{ADC} - C2_{ADC}\right) + \left(INL_A\left(C1_{ADC}\right) - INL_A\left(C2_{ADC}\right)\right)\right]l_{ADC} \\ &+\left(w2_{DAC} - w1_{DAC} + w2_{ADC} - w1_{ADC} + q2_{ADC} - q1_{ADC}\right)\end{aligned} \quad (6)$$

Equation (6) can finally be re-arranged to get:

$$\begin{aligned}&INL_D\left(C1_{DAC}\right) - INL_D\left(C2_{DAC}\right) + \frac{\alpha}{l_{DAC}} = \\ &\frac{\left(C1_{ADC} - C2_{ADC}\right)}{g} - \left(C1_{DAC} - C2_{DAC}\right) \\ &+\frac{\left(INL_A\left(C1_{ADC}\right) - INL_A\left(C2_{ADC}\right)\right)}{g} + wq\end{aligned} \quad (7)$$

Where $g = l_{DAC} / l_{ADC}$, and $wq$ is the variable with all the additive and quantization noise terms. The reason for writing equation (7) in this manner will become apparent very soon. Now, if (i) the 2 ADC codes $C1_{ADC}$ and $C2_{ADC}$ are the same or close to each other, and (ii) they belong to the same "LSB segment" of the ADC, then the term $er = \left(INL_A\left(C1_{ADC}\right) - INL_A\left(C2_{ADC}\right)\right)/g$ will be negligible. The underlying assumption in the above stated conditions is that the linearity within the LSB segment of an ADC is good, and so, the difference in INLs will be negligible compared to the noise. Or in other words, if the LSB segment of the ADC is linear, then the difference in input voltages to the ADC is approximately equal to the difference in ADC codes multiplied by the slope. In order to guarantee that conditions (i) and (ii) are true, we need to carefully select from our (DAC input code, ADC output code) pairs for the shifted and non-shifted measurements.

When taking the measurements, we have two ADC output codes $k1_{ADC}, k2_{ADC}$ for each DAC input code $k_{DAC}$. We can create two matrices with rows of the form (DAC input code, ADC output code). One matrix for the shifted version ($A1$ with rows of the form $(k_{DAC}, k1_{ADC})$) and the other matrix for the non-shifted version ($A2$ with rows of the form $(k_{DAC}, k2_{ADC})$). First, sort the rows of $A1$ in the increasing order of $k1_{ADC}$ codes. The whole row is sorted, so DAC codes will get rearranged too. Similarly, sort rows of $A2$ in the increasing order of $k2_{ADC}$ codes. Next, group together the rows

in $A1$ in which the ADC codes belong to the same ADC LSB segment. Similarly, group together the rows in $A2$ which belong to the same ADC LSB segment. For those rows in $A1$ and the rows in $A2$ which belong to the same ADC LSB segment group, we can identify corresponding rows in which the ADC codes are almost the same or differ by a few codes. Some excess rows, and rows near the transition between LSB segments can be removed. Since the codes are already sorted, this task is easy to do. Figure 1 gives a clearer visual representation of the preceding operations and what happens to the ADC columns of the matrices. The result is that we now have two matrices $A1$ and $A2$, with each corresponding row of the form $(C1_{DAC}, C1_{ADC})$ and $(C2_{DAC}, C2_{ADC})$ respectively. For the same row number, $C1_{ADC}$ and $C2_{ADC}$ are either exactly equal or within a few codes of each other.

Our goal is to form an equation like (7) for each row of the final matrices $A1$ and $A2$ with unknowns on the left side and knowns on the right side. On the right side, if we ignore the error terms $er$ and $wq$, then $g$ is the only other "unknown". We know that $g = l_{DAC} / l_{ADC}$ is nothing but the gain from the DAC codes to the ADC codes. Since the ADC can be highly nonlinear, this gain should be calculated separately within each ADC LSB segment. Within a specific ADC segment, the actual LSB of the DAC can be written as:

$$l_{DAC} = \frac{V1|_{\max\_DAC\_code} - V1|_{\min\_DAC\_code}}{\max\_DAC\_code - \min\_DAC\_code} \tag{8}$$

The actual LSB of the ADC can be written as:

$$l_{ADC} = \frac{V1|_{\max\_DAC\_code} - V1|_{\min\_DAC\_code}}{ADC\_code|_{\max\_DAC\_code} - ADC\_code|_{\min\_DAC\_code}} \tag{9}$$

From (9) and (10), $g$ can be estimated as :

$$g = \frac{ADC\_code|_{\max\_DAC\_code} - ADC\_code|_{\min\_DAC\_code}}{\max\_DAC\_code - \min\_DAC\_code} \tag{10}$$

For the case of a general digitizer, equation (7) still applies. We can simply form the equations only when the output codes are equal. This might lead to a lot discarded rows. To avoid this loss of information, equations can also be formed when the codes are nearby. The gain term required on the right-hand side can be approximated by $l_{DAC}$ divided by the weight of the digitizer.

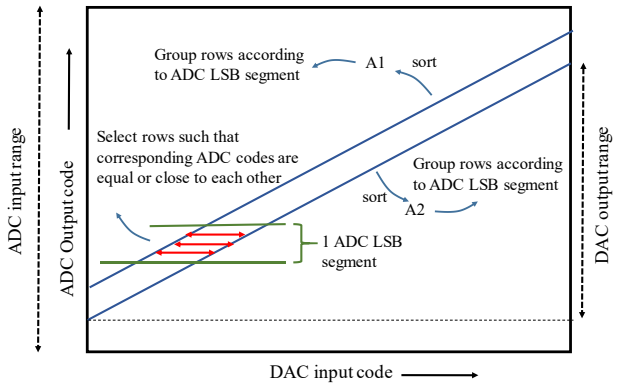


Fig. 1. Visual representation of various operations performed

### D. uSMILE-ROME

Now that the measurement error has been removed in the previous section, equation (7) can be combined with equation (1) to get the final equation:

$$\begin{aligned} & e_M(C1_{DAC,MSB}) + e_I(C1_{DAC,ISB}) + e_L(C1_{DAC,LSB}) \\ & -e_M(C2_{DAC,MSB}) - e_I(C2_{DAC,ISB}) - e_L(C2_{DAC,LSB}) + \beta \\ & = \frac{(C1_{ADC} - C2_{ADC})}{g} - (C1_{DAC} - C2_{DAC}) \\ & + er + wq \end{aligned} \tag{11}$$

Where $\beta = \alpha / l_{DAC}$ is treated as an unknown. We can form one such equation for each row in the matrices. $er$ is the error term which is negligible, and $wq$ can be treated as random noise (the quantization noise can also be approximated to be whitened). Let's say we do nMSB-nISB-nLSB segmentation of the DAC's INL. Since we are estimating end-point fit INL, $e_M(0) = e_I(0) = e_L(0) = 0$. We should also add an extra equation $e_M(2^{nMSB} - 1) + e_I(2^{nISB} - 1) + e_L(2^{nLSB} - 1) = 0$. If we take just 2 samples per DAC code (with and without shift), the number of equations will be $2^{nDAC} - r + 1$ where $r$ is the total number of discarded rows. The number of unknowns will be $2^{nMSB} + 2^{nISB} + 2^{nLSB} - 3 + 1$. The +1 here is for $\beta$. For a high resolution DAC and correct INL segmentation, the number of unknowns will be much less than the number of equations. For this over-determined system, the method of least squares can be applied to estimate the unknown vectors $e_M$, $e_I$, and $e_L$, and the shift. The noise term will be effectively averaged out. The full code INL of the DAC can be reconstructed after the least squares estimation.

## IV. SIMULATION RESULTS

To verify the effectiveness of the proposed method, extensive simulations were performed with different DAC architectures and INL levels. The R-2R DAC was particularly studied due to its wide usage, high resolution and low power. A 16-bit R-2R DAC, modeled with resistor mismatches was used as the device under test. A 16-bit SAR ADC, modeled with capacitor mismatches, was used as the measurement device. The SAR ADC had a scale down capacitor after 8 MSB bits. It was ensured that the ADC did not have any wide codes or dead zones. The additive noise added to the output of the DAC was set to around 0.5 LSB level.

First, to show that the method reduces the linearity requirement on the measurement device, a relatively low-linearity ADC is taken. The INL of the ADC is plotted in Figure 2. As can be seen in the figure, the INL of the ADC is around the +/-10 LSB level, which means that the ADC is only around 12-bit linear.

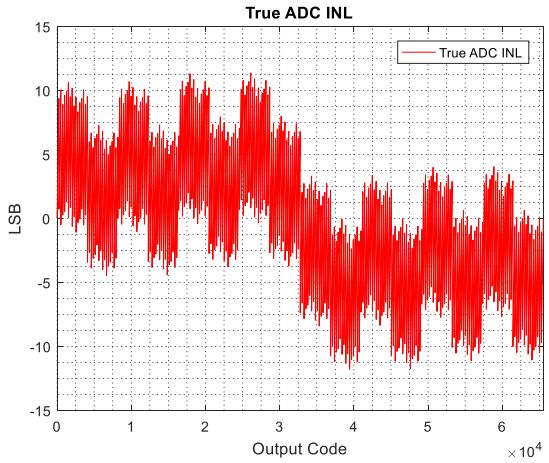


Fig. 2. INL of ADC used for measurement

While estimating the INL of the DAC using the uSMILE-ROME method, the INL curve is segmented as 8-4-4. The number of unknowns is 286. Say the number of equations that remain after the discarded rows is around 80% of 2^16. The average number of equation per variable is around 180. This should be sufficient to average out the noise. The true and estimated INL of the DAC, along with the error in estimation for each DAC code is shown in Figure 3. It can be seen that the DAC INL estimation is very accurate in spite of the ADC used for measurement being highly non-linear.

To further test the robustness of the method, 100 simulations were run with 100 randomly generated 16-bit DACs and 16-bit ADCs. The maximum and minimum of the DAC INL estimation errors for each run is shown in figure 4. All the estimation errors are within +/- 0.4 LSB. A different view of the estimation accuracy is presented in figure 5. The

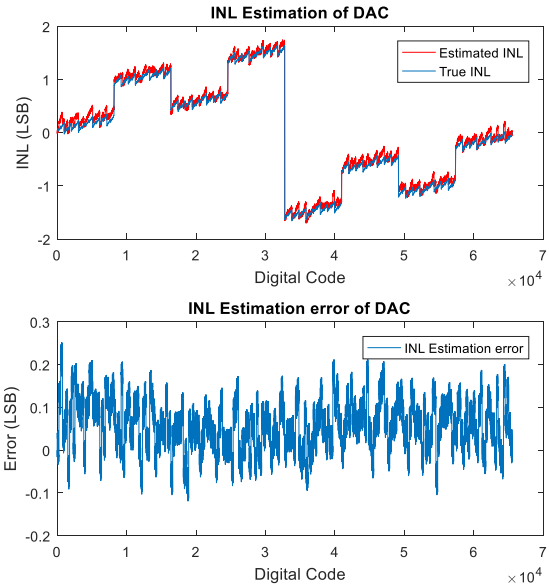


Fig. 3 (a). True and estimated DAC INL (b) Error in INL estimation

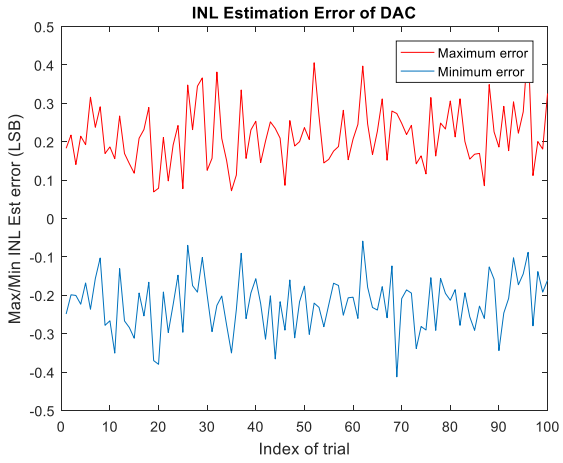


Fig. 4. Maximum and minimum INL estimation errors over 100 runs

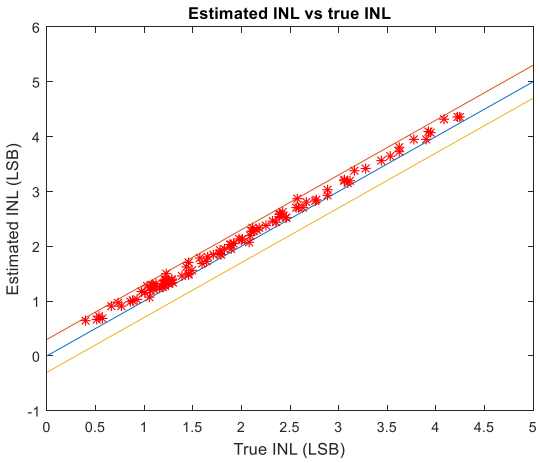


Fig. 5. Estimated INL vs True INL over 100 runs

X-axis is the true maximum absolute INL and the y-axis the estimated maximum absolute INL. Ideally, all the points should lie on the y=x line. +/-0.3 LSB bands around y=x are also plotted. All the points are contained within this band, which implies that the accuracy of the uSMILE-ROME algorithm is very high. The simulation results show that the proposed method is robust over different DAC linearity levels.

## V. Conclusion

A fast, low-cost method for static linearity testing of DACs is presented in this paper. The uSMILE-ROME method allows the testing of high linearity DACs with low-linearity on board digitizers, while considerably reducing the test time and the test cost. This is enabled by using a segmented non-parametric model for the INL curve of the DAC, which reduces the number of unknowns to be estimated. Additionally, the measurement error introduced due to the on-board digitizer is removed in the algorithm, thus allowing it to be orders of magnitude less linear than the DAC under test. All of this is combined in the uSMILE-ROME method, and results in significant reduction in time and cost for static linearity testing of DACs as compared to the traditional method.

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