Low Power ISM band receiver front end

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Abstract

This report discusses the design and simulation results of an ultra low power receiver front end circuit for the ISM band(2.4GHz). The design has been done using a 65nm CMOS process. The direct conversion receiver architecture employs synchronous detection using a local oscillator whose frequency is same as the carrier frequency of the signal. As a result, the circuit complexity is significantly reduced, enabling integration with the baseband circuitry. Using simultaneous Inphase(I) and Quadrature(Q) mixing, the image problem is eliminated. This project investigates both active and passive downcoversion techniques. Besides, driver circuits have also been designed to amplify and buffer the VCO output to drive the Local Oscillator(LO) ports of the mixer. The receiver based on the active mixer has a simulated noise figure of 4.8dB, IIP3 of -19dBm and a power consumption of 1.95mW including the LO drivers. The receiver based on the passive mixer has a simulated noise figure of 4.8dB, IIP3 of -15dBm and a power consumption of 1.92mW, with the mixers and LNA alone consuming 1.6mW. The active mixer is based on a single balanced topology whereas the passive mixer is based on a fully differential Transimpedance Amplifier(TIA) to convert the mixer current to voltage output. A CMOS Transimpedance amplifier along with Common Mode Feedback(CMFB) circuit have also been designed for implementing the passive mixer. The LO driver-buffer stage comprises of an amplifier and series of invertors for achieving the requisite fanout to drive the LO input ports of the mixer. All circuits have been implemented at transistor level and have realistic passives with a quality factor of 10 for inductors and 50 for capacitors. The maximum supply voltage is 1V. This power constrained design is a tradeoff between noise, linearity and power dissipation.

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1. Introduction

1.1. Receiver Architecture

With the ever-increasing need for the integration of RF front end circuitry with baseband circuitry, direct conversion has become a favored receiver architecture. The image rejection is improved since the received RF signal is downconverted using an exponential signal rather than sinusoid. Nevertheless, the receiver architecture still suffers from fundamental limitations from the hardware such as low frequency flicker noise, I/O mismatch as well as linearity, each of which can be improved at the cost of power dissipation.

With the ever increasing demand for seamless integration of "devices" by way of the Internet of Things(IoT), low power operation is even more critical for current and upcoming sub-6GHz communications. A key ingredient of IoT architectures is multiple "connected" nodes that constantly send and receive wireless data. With several such nodes in the network, each node will be severely constrained in terms of DC power in order to conserve battery life. In a typical mobile platform that has both transmit, receive and processing, a large section of the power budget is usually allocated to the processor (which includes sensor interface (for an IoT application) and data processing). This is followed by the transmitter (owing to limited PA efficiencies). The last segment of the power budget is for the receiver which is usually much smaller when compared with the power budget of the other two segments.

In many practical applications, the mobile device is not continuously transmitting data. Therefore, it is turned off when not in transmit mode, allowing power savings. However, for the most part, the device is in "listening" mode which means that the receiver is "on" for a significant amount of time. Given the minimal power budget allocated for the receiver, it is even more essential to squeeze every microwatt of available DC power to design an optimal receiver with best performance tradeoffs that can be achieved within the small available power budget. This calls for judicious circuit topologies and techniques that can best utilize the available power budget.

This project investigates circuit architectures for meeting the key RF receiver specifications with a very low power dissipation that will make it attractive for wide deployment especially on mobile platforms. Figure 1 below is a block diagram of the direct conversion receiver. The first block following the antenna is a band pass filter. This is followed by a Low Noise Amplifier. The output of the LNA is split using a directional coupler and then downconverted using two mixers where the Local Oscillator(LO) frequency of one mixer is out of phase by 90^0 from the LO frequency of another. The output of these mixers is then amplifier using a variable gain amplifier(VGA) and then digitized using an Analog to Digital Convertor(ADC). The key elements of the front end are the low noise amplifier and the mixer. The Local Oscillator (LO) signal is fed into the mixer though a driver-buffer network which in this project has been integrated with the mixer core. The noise performance is limited by the LNA and the linearity performance is limited by the mixer.

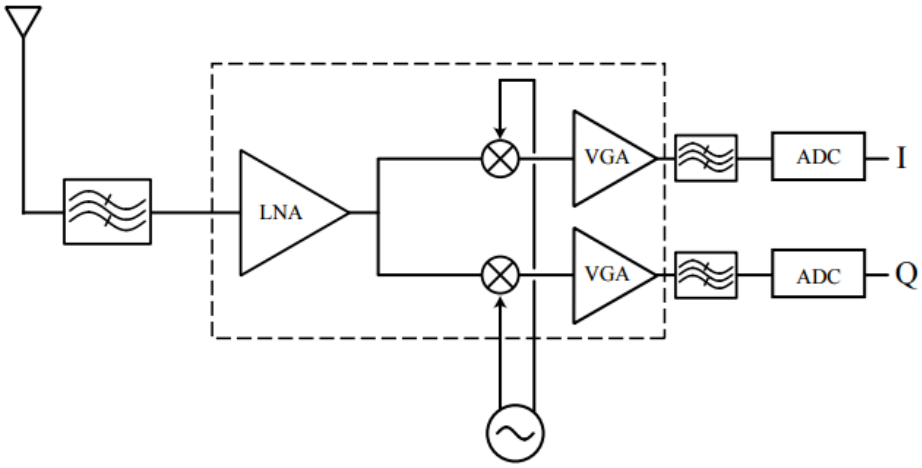

Figure 1: Block diagram of the receiver

1.2. Design objectives

The goal of this project is to design a 2.4GHz RF direct conversion receiver in a 65nm CMOS process with a total power consumption of less than 2mW, overall noise figure less than 5dB, input IIP3 of at least -20dBm, operating at 1V supply. Both active and passive mixer architectures have been investigated. While a 65nm Predictive Transistor Model(PTM) has been used for all the FETs, lumped element models with a quality factor (Q) of 10 was used for inductors and 50 for capacitors have been used. The receiver also includes the LO buffer-driver circuitry.

A link budget analysis was performed for determining the circuit level specifications. The band pass filter preceding the LNA is assumed to be noiseless. Assuming a gain of 15dB for the LNA, the LNA noise figure can be calculated using Friis' equation

$$F_{rx} = F_{LNA} + \frac{F_{MIX}}{G_{LNA}} \quad (1)$$

Where F_{rx} is the receiver noise figure, F_{LNA} is the LNA noise figure. F_{MIX} is the mixer noise figure, G_{LNA} is the LNA gain. Assuming that the LNA and mixer are the dominant contributors of noise, if the mixer noise figure is assumed to be 10dB, the maximum noise figure of the LNA is 4.5dB.

Maximum swing at ADC output is 0.5V. This means swing at mixer output is 50mv for a VGA gain of 60dB. Maximum allowable baseband signal = 100mV.The VGA input saturates at 100mv. If the VGA load resistance is 1kΩ, this corresponds to an IIP3 of -20.dBm at the input of the VGA.

$$\frac{1}{IIP3^2} = \frac{1}{IIP3^2,LNA} + \frac{G_{LNA}}{IIP3^2,Mixer} + \frac{G_{LNA} \times G_{Mixer}}{(IIP3^2,Mixer) \times (IIP3^2,LNA)} \quad (2)$$

Where IIP3, LNA is the IIP3 of the LNA. IIP3, Mixer is the IIP3 of mixer. If we set $IIP3_{LNA}$ = -15dBm, $IIP3_{mixer}$ must be ~ -5dBm.

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2. Receiver Design

2.1. Investigation of device technology

Since LNA noise figure is critical, roughly 50% of the power budget has been allocated to LNA. This was reduced to 35% after optimization and have sufficient margin for the power dissipation of the LO buffers. The remaining 50% to each of the mixers. The process used is the 65nm CMOS process. Keysight Advanced Design System(ADS) has been used for all the design and simulation endeavors. DC simulations on the device were done to determine the optimal sizing. Figure 3 (left) below is the simulation result of sweeping the gate voltage for fixed DC current of 1mA. For a drain-source voltage of 1V and a current of 1mA, the device transconductance is ~ 5ms. The transconductance peaks at V_{GS} ~ 0.45V as show in Figure 3. The optimum V_{GS} based on noise performance was later found to be ~0.38V.

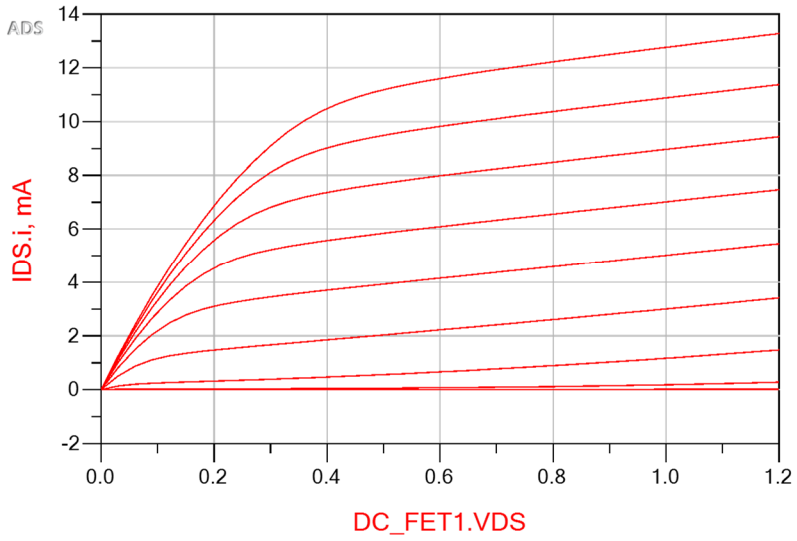


Figure 2: I-V simulations on a 1µm/65nm NMOS

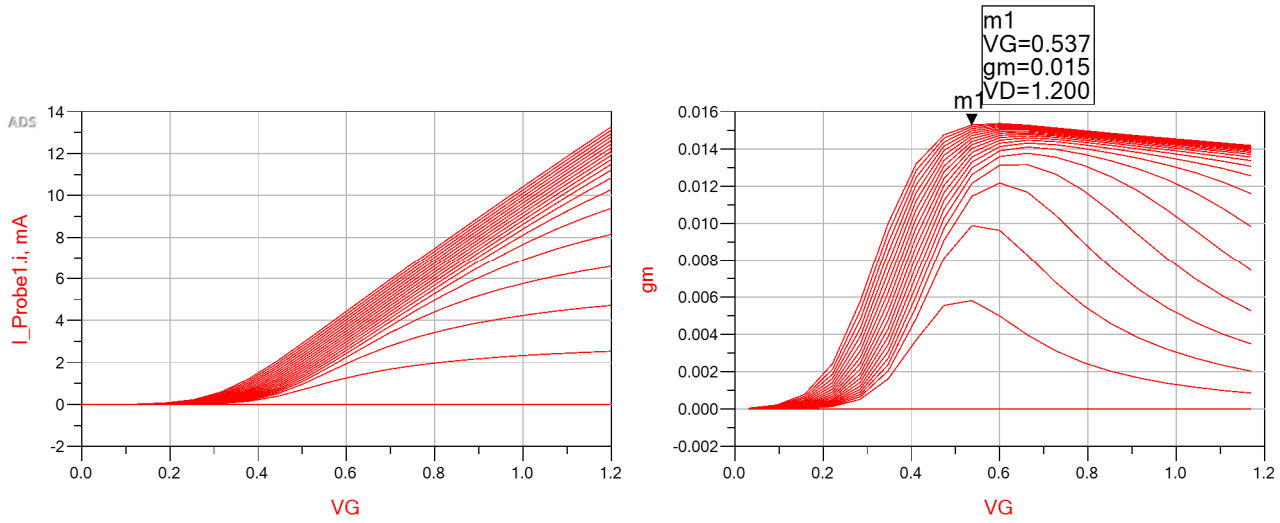


Figure 3: (left)DC IV simulations on a 1µm/65nm NMOS and (right) transconductance vs V_{GS}

2.1. LNA design

At a DC current of 1mA the simulated NF_{min} was 0.7dB for a width of 60µm as shown in Figure 4.

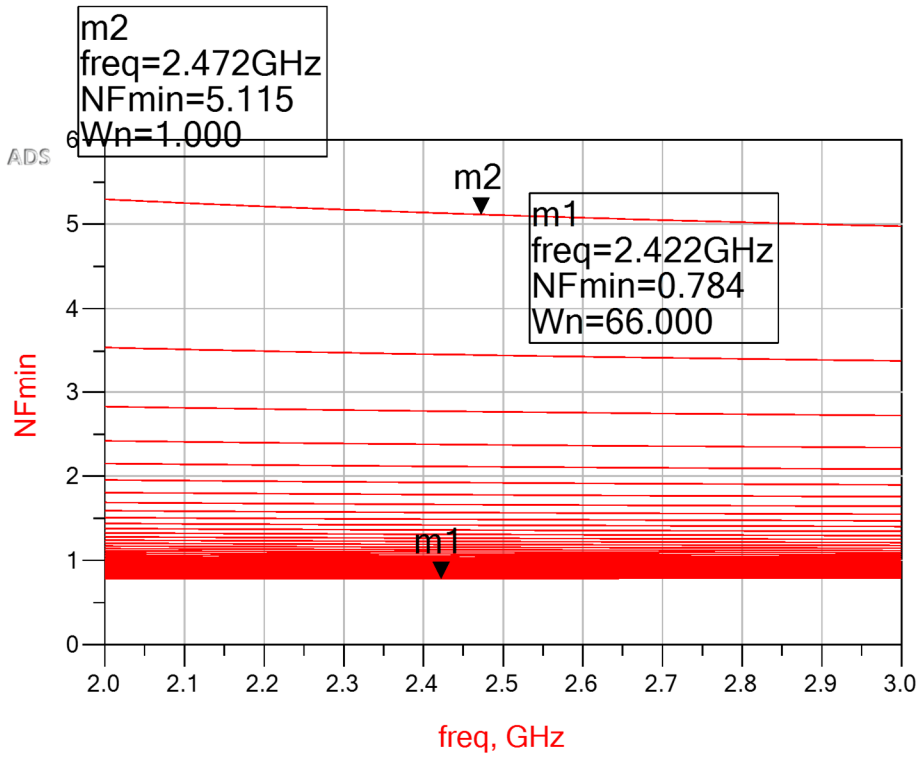


Figure 4: NF_{min} Vs Device width for dc current of 1mA and VDS~0.4V

However, in order to accurately determine the noise figure-match limitation, the input had to be matched to 50Ω. Cascode amplifiers are well understood. The cascode topology is a standard narrowband LNA topology that optimizes gain and matching. When biased correctly, the common gate device is degenerated. Therefore, the noise contribution from the common gate device is minimal. Inductive degeneration was used for matching the input to 50Ω.

The input impedance is

$$Z_{in} = j\omega L_g + \frac{1}{j\omega C_{gs}} + \frac{g_m L_S}{C_{gs}} \quad (3)$$

In order to reduce the cutoff frequency, a capacitance was added between gate the source terminals. The effective gate to source capacitance is negated by the series inductance at the gate. The term ($g_m L_s/C_{gs}$) is used to match the real part of the input impedance(50Ω). Matching can be improved by increasing the degeneration inductance. This however decreases the gain and bandwidth. Therefore, a 'T' network was used for matching. This is shown in Figure 5. A capacitor was also added in shunt with the load inductor to improve the second order intermodulation performance.

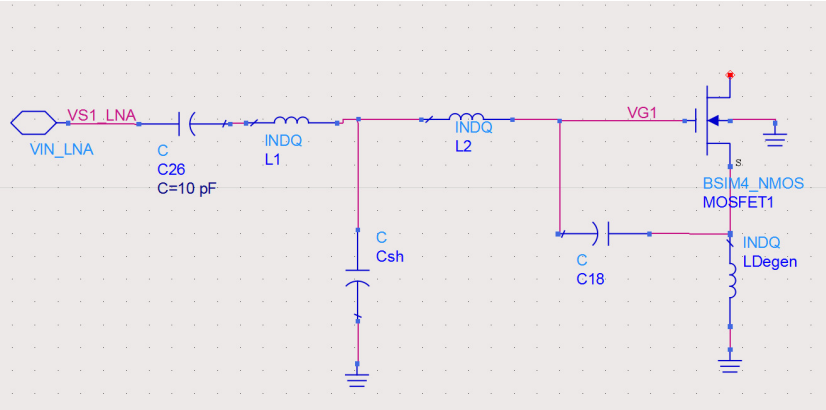


Figure 5: Input matching network

The optimum device sizing for the common gate and common source was 18µm/65nm. Figure 6 is the schematic of the cascode LNA.

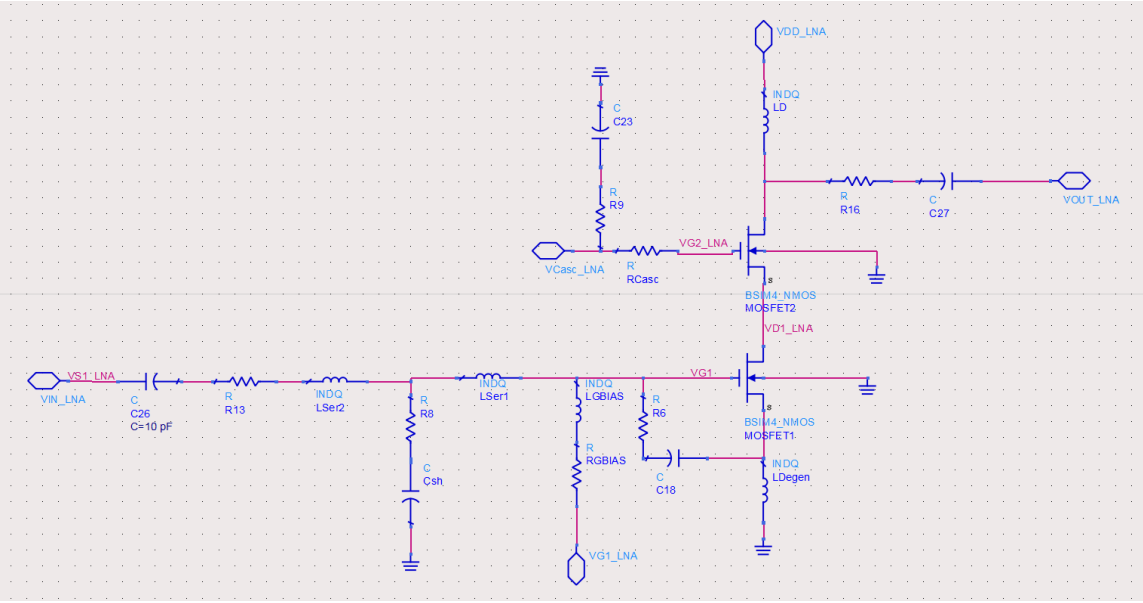


Figure 6: Cascode LNA

Table 1 below lists the details of the active and passive devices used in the design.

Table 1: LNA design details

Device	**Value**	**Remarks**
MOSFET1	18µm(W) by 65nm(L)	Common Source
MOSFET2	18µm(W) by 65nm(L)	Common Gate
C_{sh}	60fF	Matching
C_{23}	3.65pF	Cascode Stability
L_D	10nH	Drain Choke
R_{GBIAS}	5kΩ	Bias Resistor
L_{GBIAS}	10nH	Gate Choke
L_{ser2}	10nH	Matching
L_{ser1}	7nH	Matching
C_{18}	0.23pF	Q=50
R_{Casc}	50Ω	Cascode Stability
VG1_LNA	0.37V	CS Bias
Vcasc_LNA	0.79V	CG Bias
VDD_LNA	1V	I_D=648µA

2.1.1. Simulation results

Figure 7 below is the test bench of the LNA. Harmonic Balance (HB) simulations were used for linearity analysis and S-Parameter simulations were used for analyzing the match and noise performance.

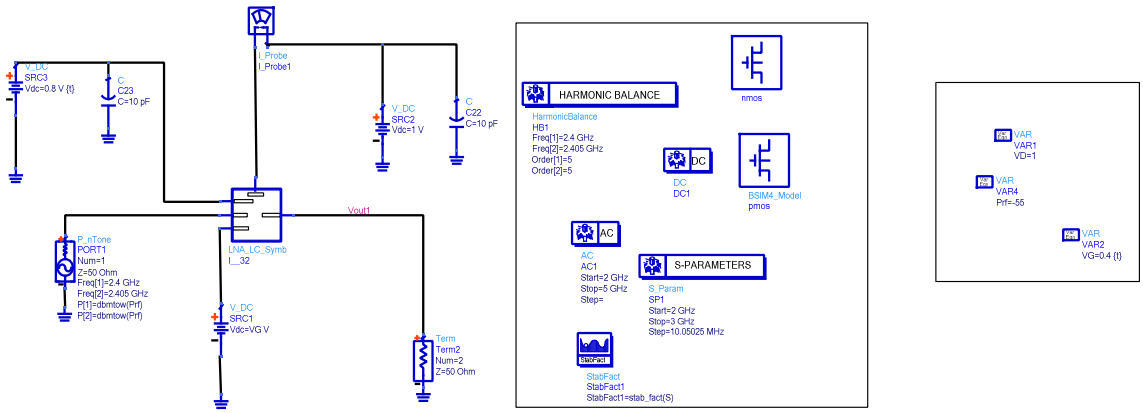


Figure 7: LNA Test Bench

Figure 8 below is the simulated input return loss(S_{11}) of the LNA. The S_{11} at the center frequency of 2.4GHz is -24dB.

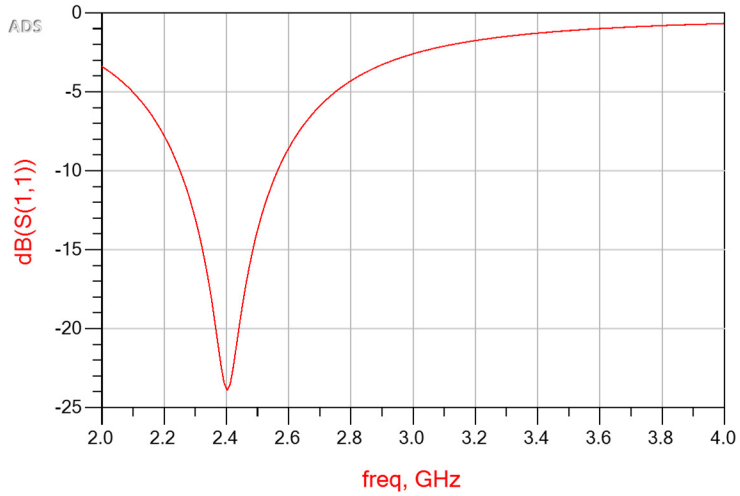


Figure 8: Input return loss of the LNA

Stability Analysis

The standard K-factor analysis is normally used for predicting stability with K>a meaning unconditional stability. S-probe analysis is a non-invasive technique to validate the stability of circuits with feedback. Based on the S-probe analysis [1], S-probe circuit elements were used to probe the stability of the LNA at various device planes in the circuit. Figure 9 below is the ADS schematic of the S-probe pair.

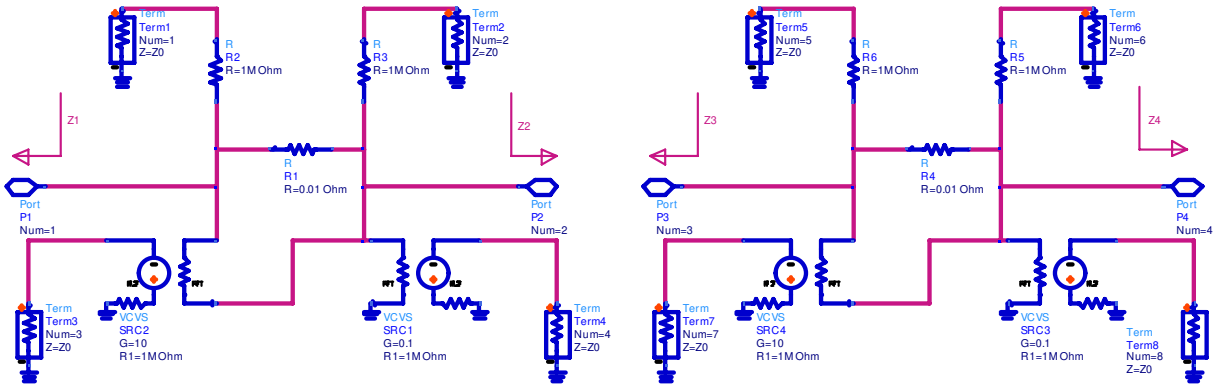


Figure 9: Schematic of the S-probe pair

The S-probes extract the terminating impedances on either side of an active device. Based on the analysis described in reference [1], a network is stable when the two stability indices (defined in equation 2) are less than unity:

$$S_1 = \mathrm{Re}\{\Gamma_s \Gamma_{IN}\} < 1$$
$$S_2 = \mathrm{Re}\{\Gamma_{Out} \Gamma_L\} < 1 \quad (4)$$

where S_1 and S_2 are the stability indices, Γ_s and Γ_{IN} are the reflection coefficients at the input termination of the network, and Γ_{out} and Γ_L are the reflection coefficients at the output termination.

S-probe pairs were placed at following locations in the circuit:

- Gate and drain of common source device
- Gate and drain of common gate device

Figure 10 below is a plot showing the stability indices. Both Γ_s and Γ_{IN} and and Γ_{out} and Γ_L are <1. Figure 11 below is the plot showing the stability factor(K). K>1 at all frequencies in the range indicating unconditional stability.

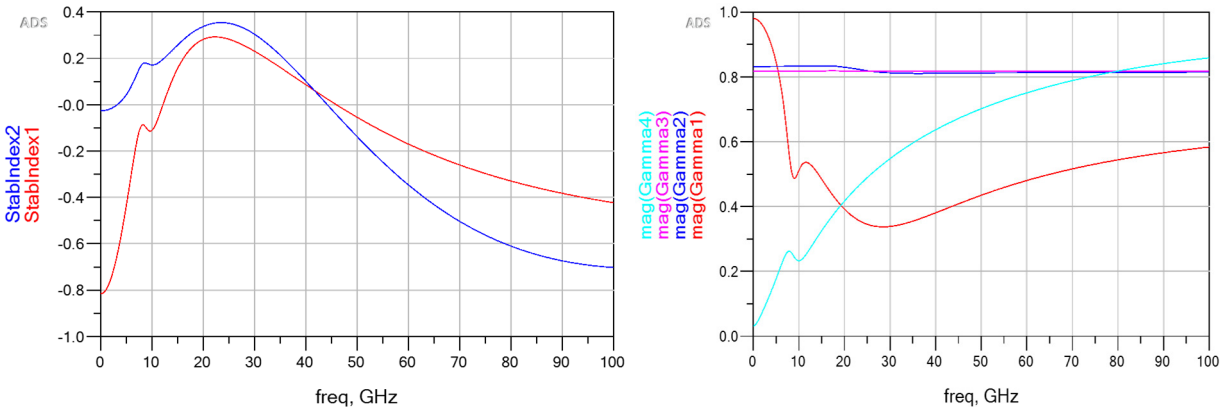


Figure 10: Stability indices for the LNA (left) and the reflection coefficients at each node(right)

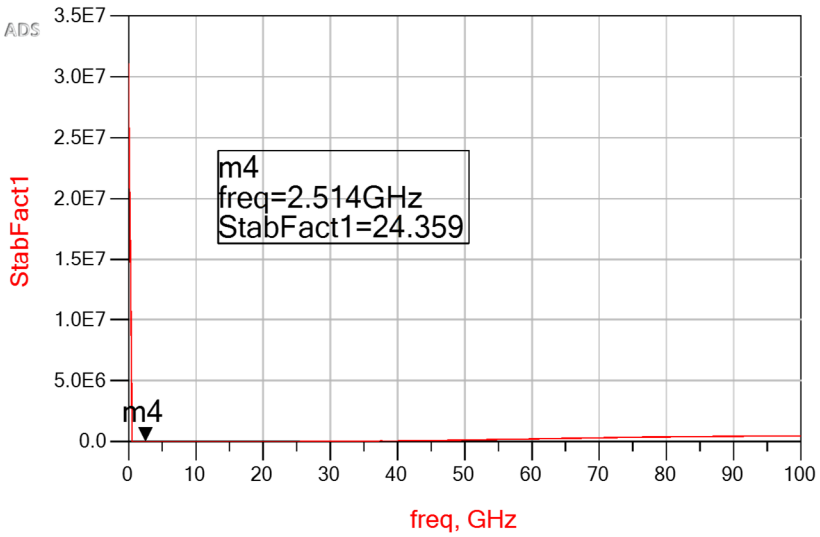


Figure 11: Stability factor(K)

Figure 12 below is a plot showing the simulated voltage gain of the LNA. The LNA voltage gain is 16.1dB with a 1dB bandwidth of 220MHz.

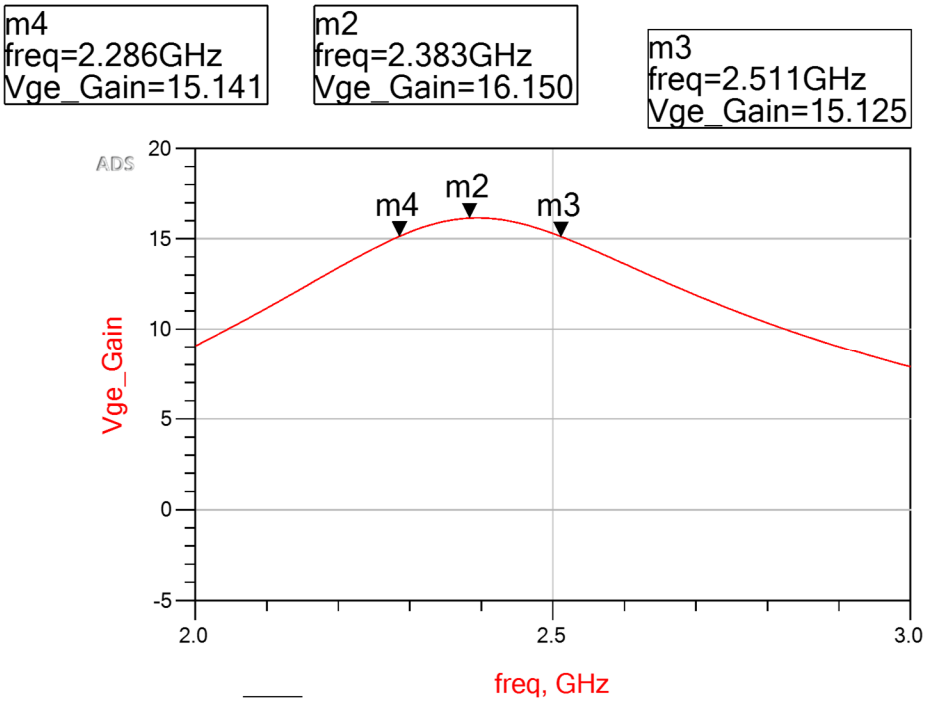


Figure 12: LNA voltage gain

Figure 13 is a plot showing the simulated noise figure of the LNA. The noise figure is 3.7dB at 2.4GHz. The DC bias was then optimized. Table 2 below summarizes the DC operating points of the LNA devices.

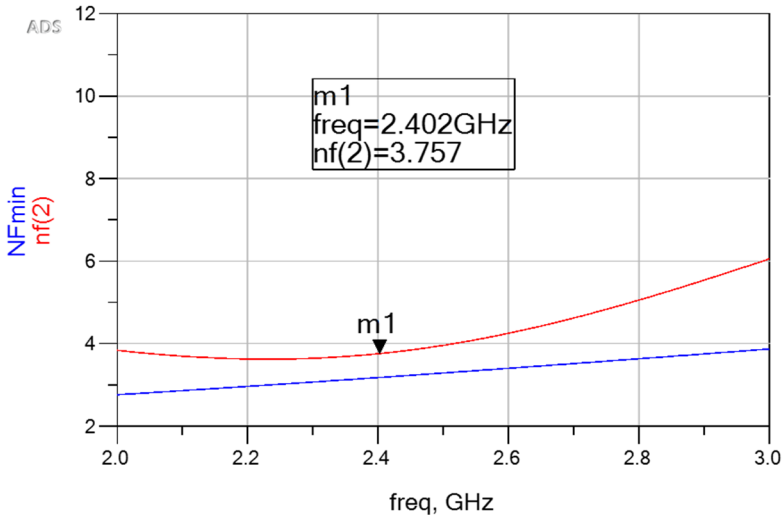


Figure 13: LNA Noise figure

Table 2: Optimized LNA bias

freq	I_Probe1.i	VD1_LNA	VD2_LNA	VG2_LNA	VG1
0.0000 Hz	607.8 uA	393.3 mV	999.5 mV	861.0 mV	413.0 mV

Figure 14 below is a plot showing the reverse isolation (S_{12}) of the LNA.

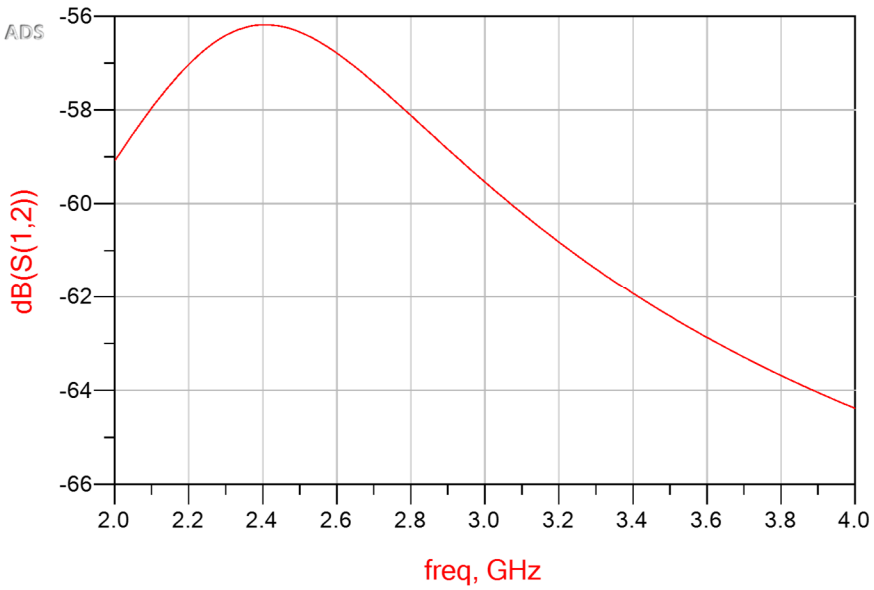


Figure 14: LNA reverse isolation

Non-Linearity Analysis

Harmonic Balance analysis was used for simulating the LNA non-linearity. For simulating gain compression, the LNA input power was swept from -60dbm to 30dBm with input signal frequency fixed at 2.4GHz. Figure 15 below is a plot showing the gain compression. The 1dB gain compression point is -17.9dBm.

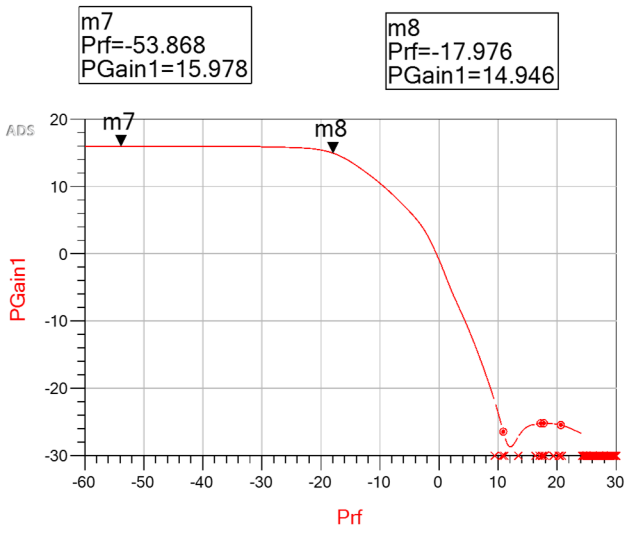


Figure 15: Gain compression of the LNA

A two tone simulation was performed for simulating the LNA intermodulation. The two different signal tones (spaced 1MHz apart) were fed to the LNA input and the input power level was swept. The power level of intermodulation products and the fundamental were plotted with respect to input power. This is shown in Figure 16. The LNA IIP3 was found to be -4.8dBm. The LNA IIP2 was found to be -3dBm.

Prf	ip3out_calc
<invalid>	-4.815

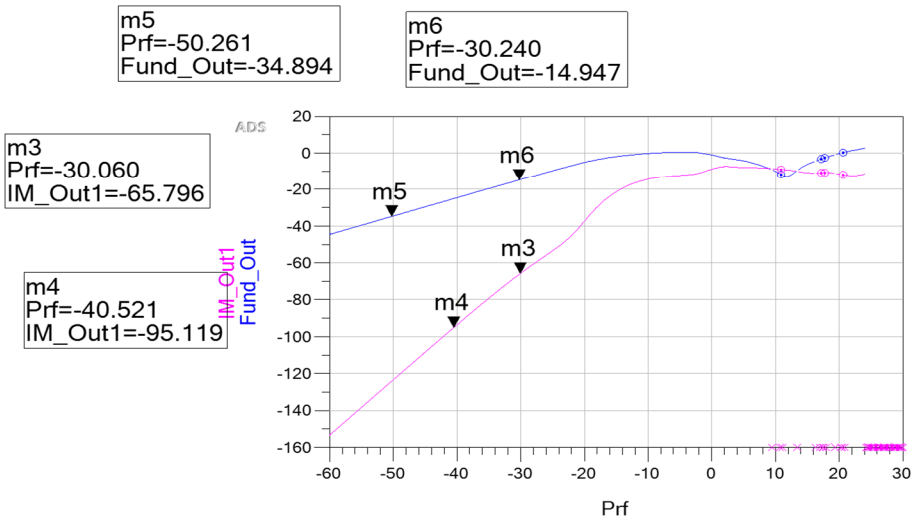


Figure 16: Third order intermodulation and fundamental v/s input power

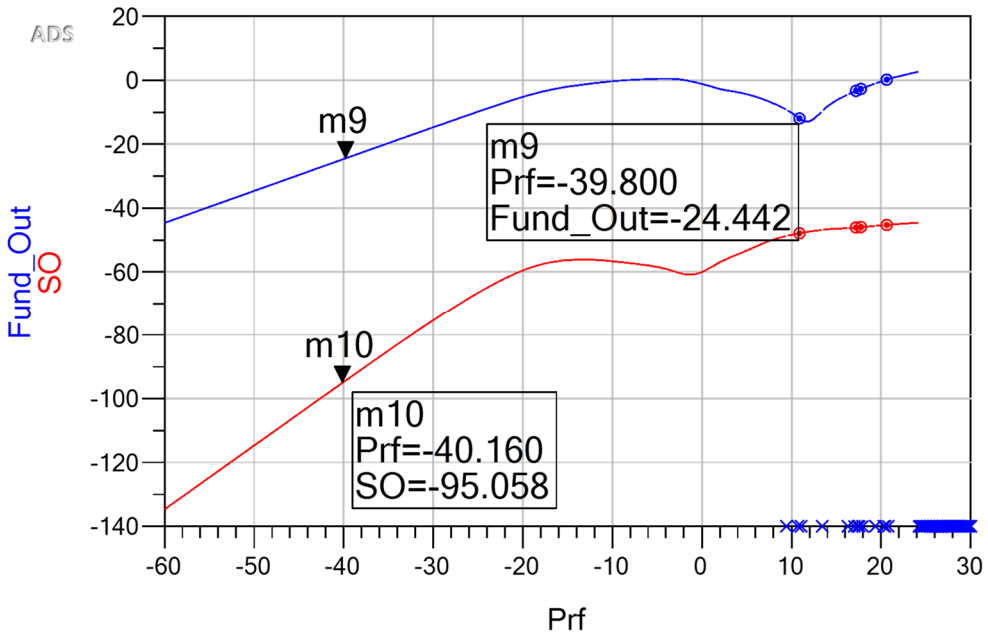


Figure 17: Second order intermodulation and fundamental v/s input power

2.2. Active Mixer

A single balanced topology was used for the active mixer. The active mixer comprises of the transconductor stage and the LO switching stage. The input of the transconductor stage is matched to the LNA output. The LNA output impedance is 18+j*147Ω.

Inductive degeneration to match mixer input impedance and LNA output. The sizing of the transconductor stage was optimized for low power and noise performance. Inductive degeneration was used for matching. This also improves linearity. Figure 18 is a plot showing the input return loss of the active mixer.

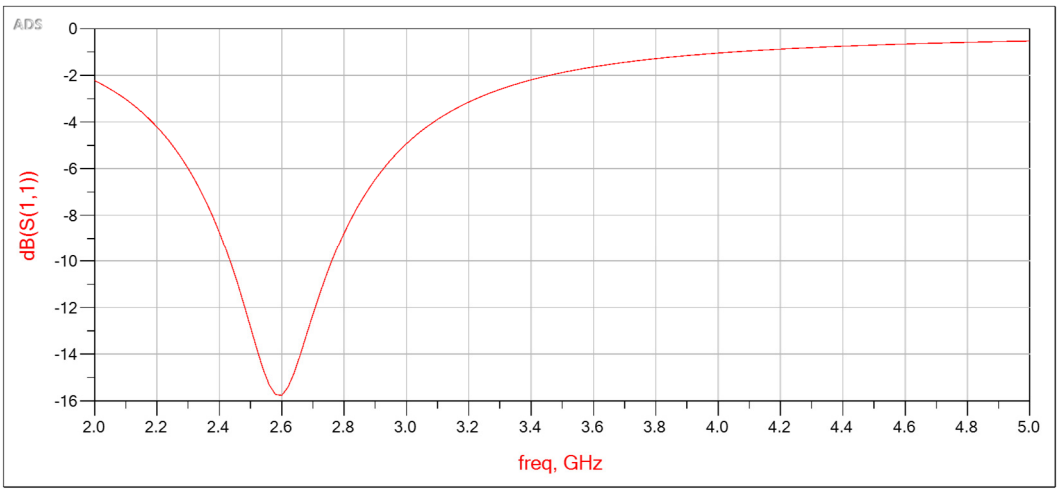


Figure 18: Input return loss(S_{11}) of the active mixer

In order to maintain the transconductor stage in saturation region, the drain of the transconductor device must always be biased at VDS>$V_{OV.}$ To facilitate this, a bleeder resistor R_{DGM} was used. A load resistance at the drain of the LO switching stage converts the downconverter current into voltage. Table 3 summarizes the details of the mixer design including the device sizing. Figure 19 below is the schematic of the active mixer.

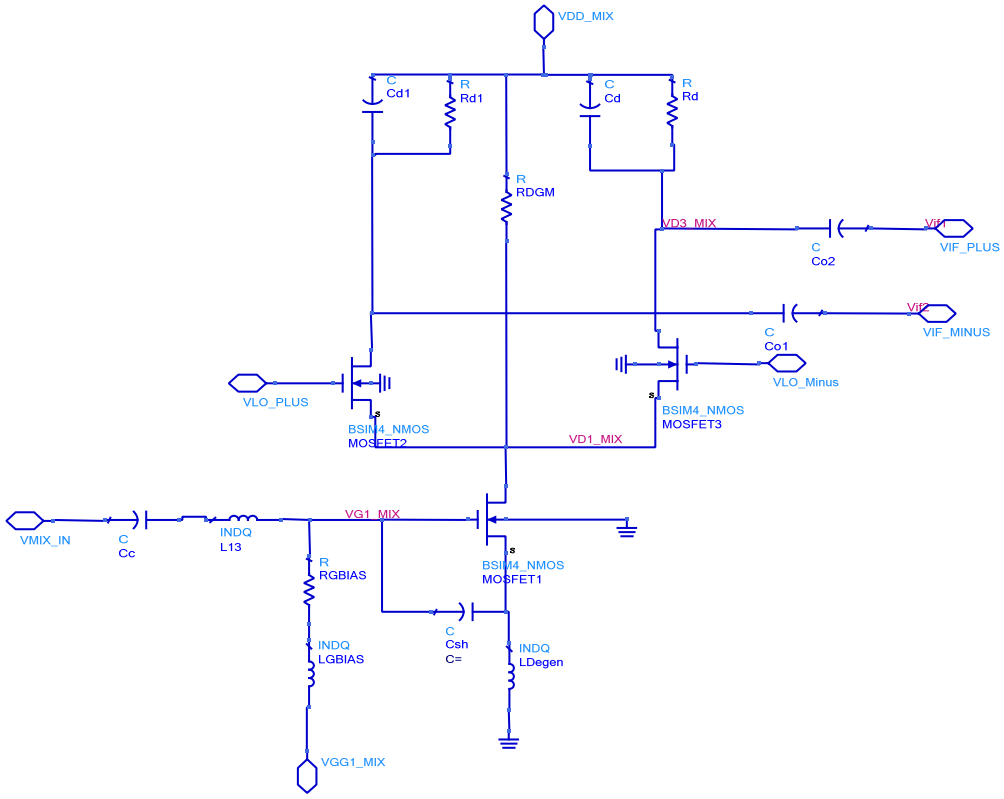


Figure 19: Active mixer schematic

Table 3: Active mixer design details

Device	**Value**	**Remarks**
MOSFET1	16µm(W) by 65nm(L)	Gm Stage
MOSFET1,MOSFET3	13µm(W) by 65nm(L)	LOStage1,2
L_{13}	1.1nH	Input Match
L_{Degen}	0.8nH	Degeneration Ind.
C_{sh}	0.42pF	Q=50
R_{DGM}	1.7kΩ	Bleeder Resistor
R_d	3kΩ	Load resistor
C_c, C_{o2}, C_{o1}	10pF	DC Bypass
LO Swing	0.95V	
VGG1_MIX	0.42V	Vth=0.38V
VDD_MIX	1V	I_D=454µA

2.2.1. Active Mixer Simulation Results

Noise and linearity simulations were performed on the mixer. Figure 20 below is the schematic of the test bench of the active mixer.

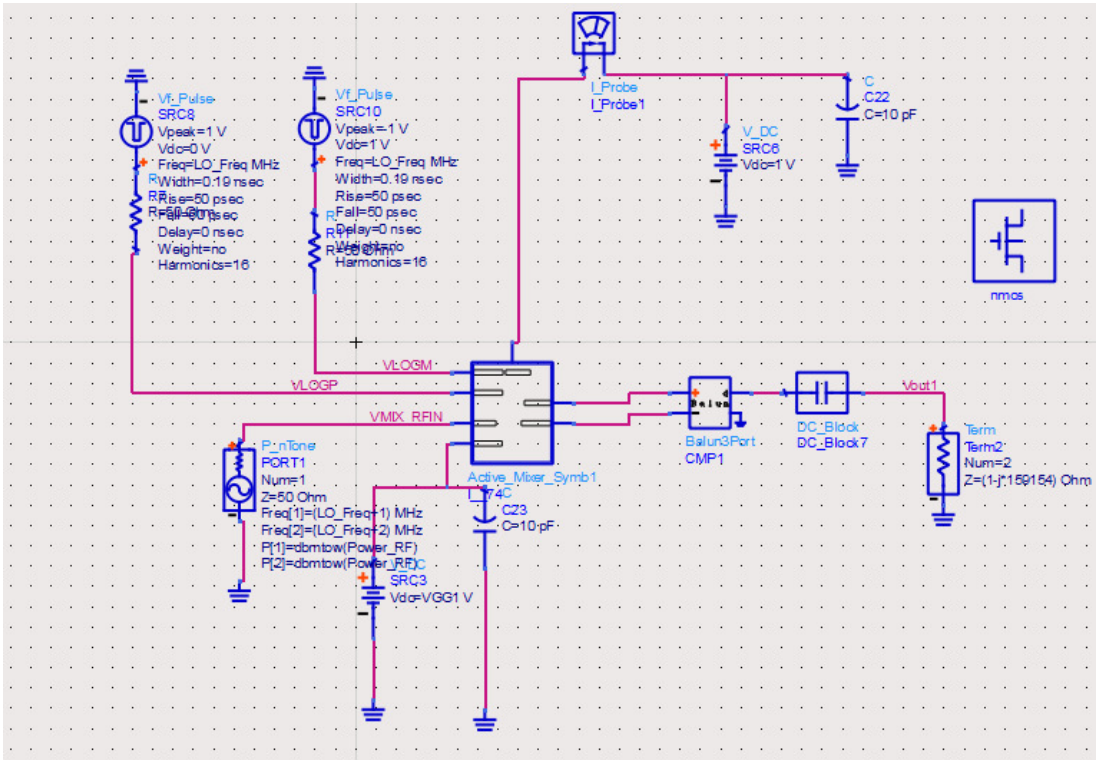


Figure 20: Active mixer test bench

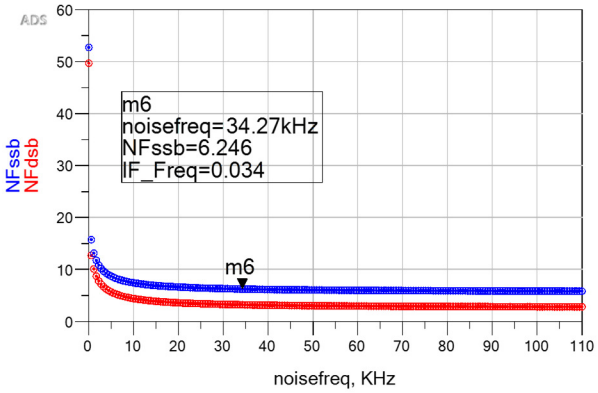
The LO signal was a square wave with a swing of 0.9V. The mixer consumes a DC quiescent current of 455µA. The gate capacitance of the LO stage was 17fF. The dynamic power from the LO stage is calculated as:

$$P_{switch} = f_{lo} * V_{LO}^2 * C_{GG} \quad (5)$$

This translates to 0.04mW at f_{LO} of 2.4GHz. This does not include the power dissipated by the LO buffer.

Noise Figure Simulation

The simulated noise figure was 6.3dB and the mixer has a conversion gain if 12.9dB



IF_Freq	C_Gain_dB
1.000E-7	12.954
0.001	12.954
0.001	12.954
0.002	12.954
0.002	12.954
0.003	12.954
0.003	12.954
0.004	12.954
0.004	12.954
0.005	12.954
0.006	12.954
0.006	12.954
0.007	12.954
0.007	12.954
0.008	12.954
0.008	12.954
0.009	12.954
0.009	12.954
0.010	12.954
0.011	12.954
0.011	12.954
0.012	12.954
0.012	12.954
0.013	12.954
0.013	12.954
0.014	12.954
0.014	12.954
0.015	12.954
0.015	12.954
0.016	12.954

Figure 21: Active Mixer Noise Figure and Conversion Gain

2.2.1.2 Non Linearity Simulation

Harmonic Balance analysis was used for simulating the mixer non-linearity. A two tone simulation was performed for simulating the mixer's intermodulation. The two different signal tones (spaced 1MHz apart) were fed to the mixer input and the input power level was swept. The power level of intermodulation products and the fundamental were plotted with respect to input power. This is shown in Figure 22. The mixer IIP3 was found to be -13.58dBm. Table 4 below summarizes the performance of the active mixer.

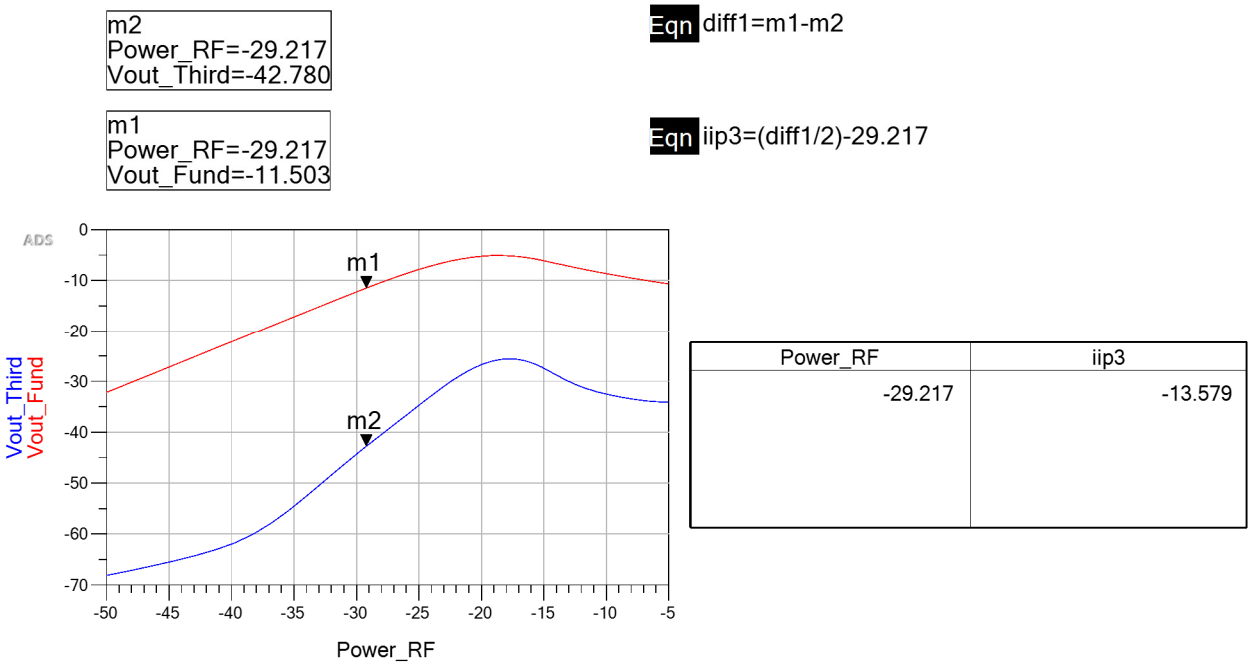


Figure 22: Active Mixer IIP3

Table 4: Active mixer performance

Parameter	**Active Mixer**
Power	455µW(gm) +4 µW (LO switch)+136 µW (Driver)
Gain(dB)	12
NF(dB)	6
IIP3	-14dBm
S11	<-10dB

2.3. Integration: LNA + Active Mixer

The LNA was integrated with the in phase(I) and quadrature(Q) mixer. The mixer's input matching was optimized since the LNA is connected to two mixers. Figure 23 is a plot showing the S_{11} of the mixer after optimizing the input match.

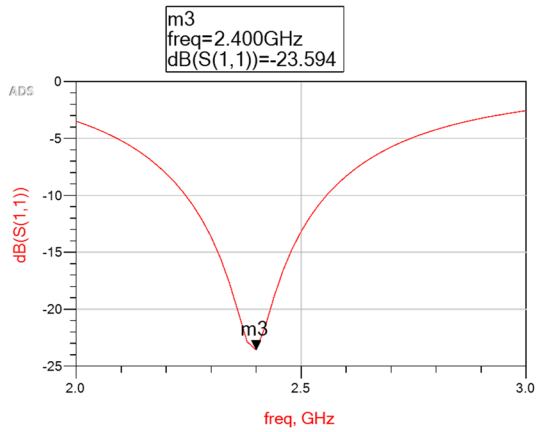


Figure 23: optimized input match for the active mixer

Figure 24 is the test bench showing the I and Q mixers and the LNA.

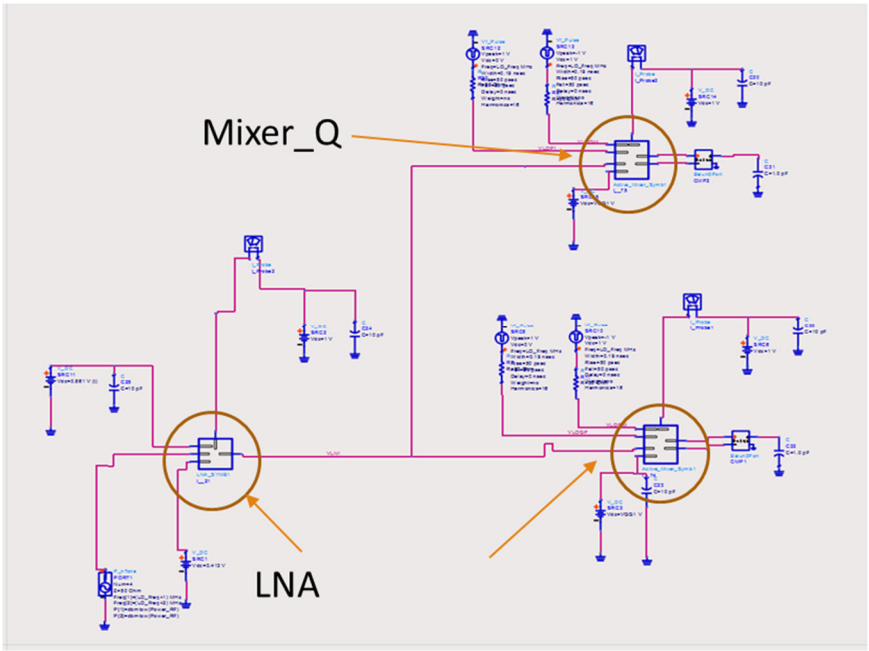


Figure 24: Receiver front end test bench

Figure 25 is the simulated noise figure of the receiver. Figure 26 is a plot showing the integrated noise figure of the receiver.

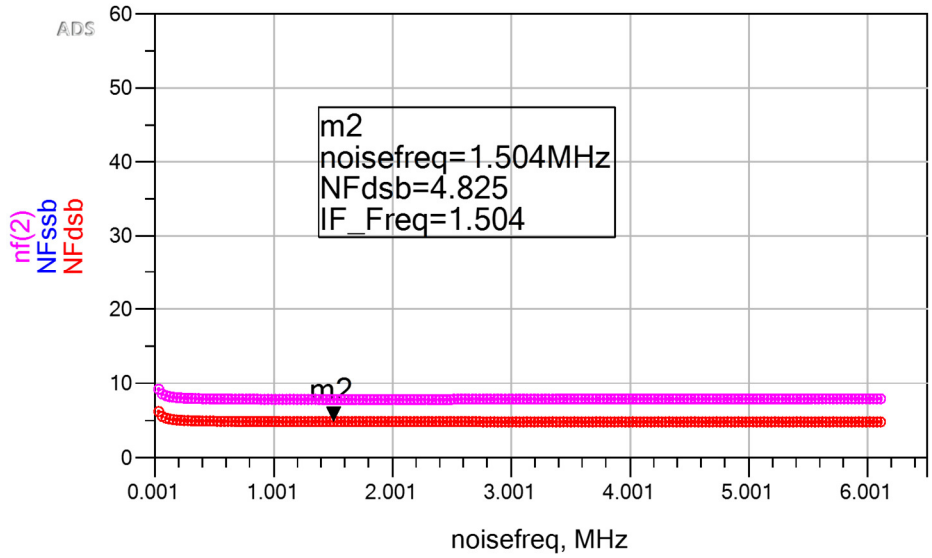


Figure 25: Noise figure of the receiver front end

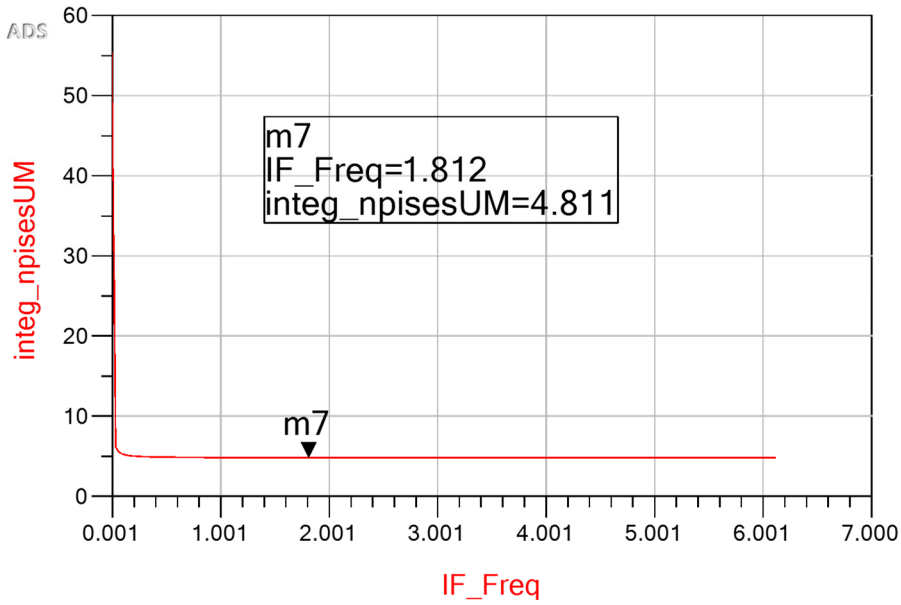


Figure 26: Integrated noise figure of the receiver

Figure 27 is a plot showing the simulated third order intermodulation and fundamental output of the receiver when the input power is swept. The simulated IIP3 was -19dBm. Figure 28 is a plot showing the simulated IIP2 of the receiver front end.

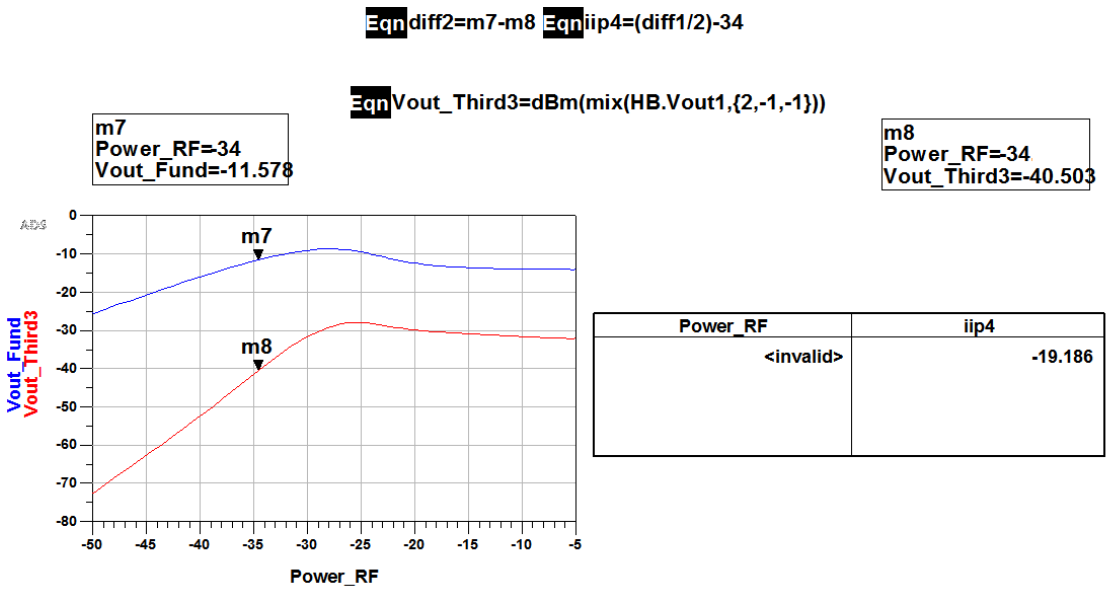


Figure 27: Receiver IIP3

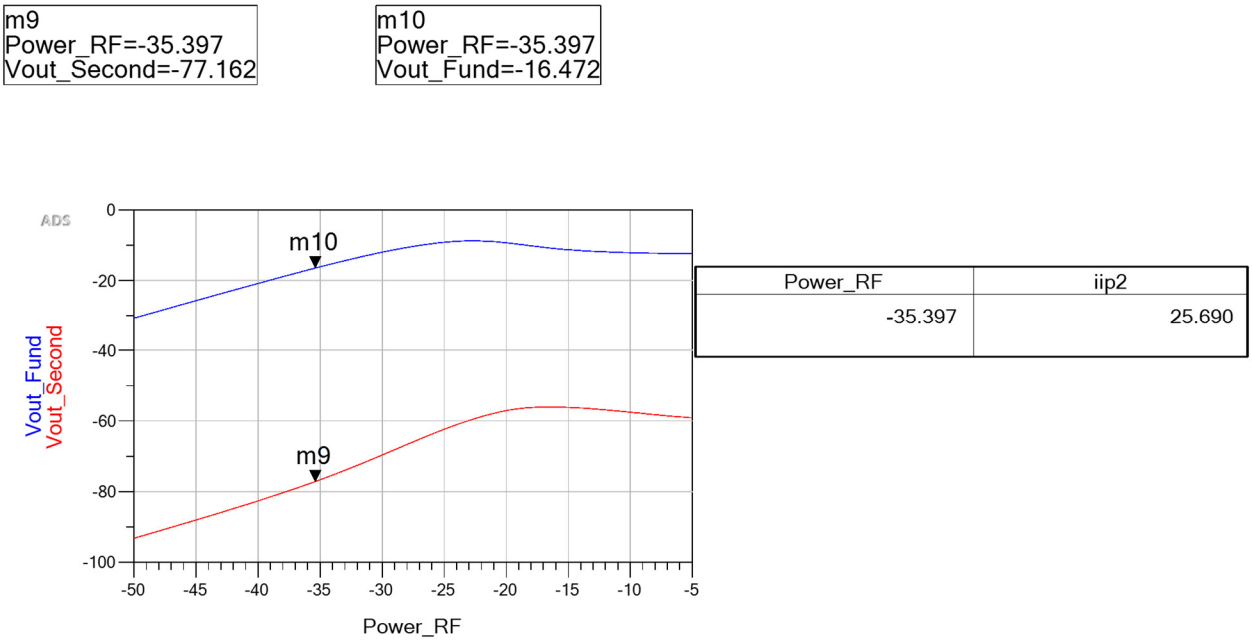


Figure 28: Simulated IIP2 of the receiver

Table 5 below summarizes the performance of the receive using the active mixer.

Table 5: Performance summary of the receiver using active mixer

Parameter	**Target**	**Design**	**LNA**	**Mixer**	**LO Amp+Driver**
Power	<2mW	1.68mW	0.615mW	0.535mW	0.136mW
Gain(dB)	20	27	16	11	
NF(dB)	<5	4.8[1]	3.77	6	
IIP3	>-20dBm	-19.1dBm[2]	-5	-13	
S11	<-20dB	-23	-23	-11	
LO Isolation	100dB	128dB[2]		-69.9dBm	
RF Bandwidth[3]	100MHz	225MHz	225MHz		

[1] 1MHz tone spacing

[2] LO power measured at LNA input

[3] 1dB bandwidth at LNA input

3. LO Buffer

The LO input to the mixer is a square wave of 1V amplitude. However, this signal must be generated by a LO buffer and driver circuit. This circuit was added to the mixer. An LO buffer and driver comprising of an invertor with feedback (linear amplifier) and a series of invertors was designed and simulated.

As shown in Figure 29 below, the circuit comprises on an amplifier stage (which is an invertor with a feedback resistor that sets the DC bias) and a series of invertors.

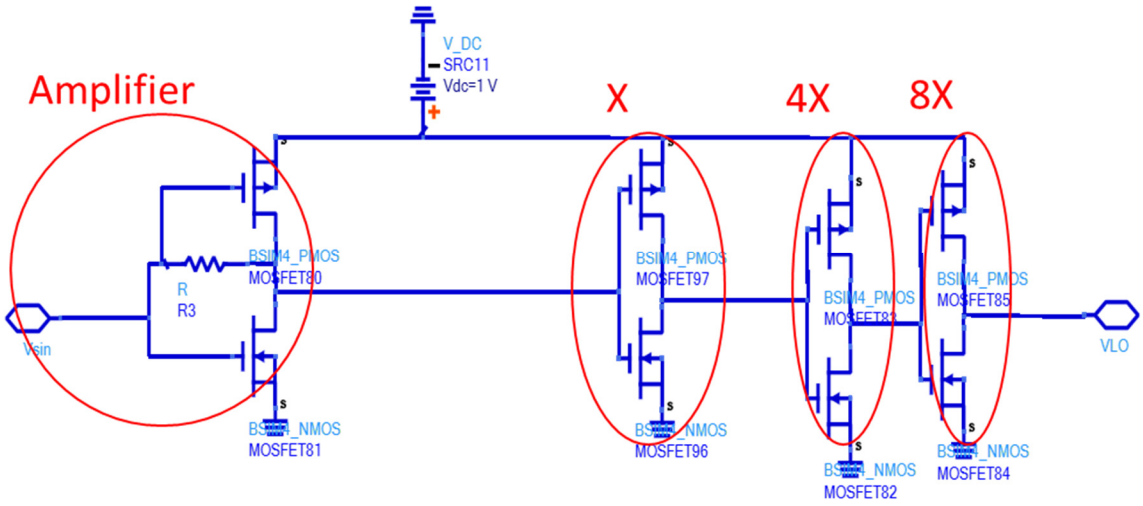


Figure 29: LO Buffer-Driver Schematic

The this heavily power constrained design is a tradeoff between fanout and power dissipation. The amplifier sizing was initially based on minimum size transistors. The invertors were sized for minimum delay. The LO device (used in the passive mixer) has in input capacitance of 14fF whereas the minimum size invertor in this process has an total input capacitance of 0.3fF. The standard geometric progression sizing was used for the invertors. Several other options were also investigated for the driver. The initial design was based on a standard F04 invertor sizing. This meant that the sizing of each invertor stage progressively increased at $(14/0.3)^{(1/4)}$ or ~3. The optimal invertor sizing (based on transient simulations for minimal delay) was found to be have an effective capacitance of 4fF(with PMOS: NMOS ratio of 1.8:1). This meant that the F04 power dissipation is prohibitively huge. Therefore, the sizing shown in Figure 29 was used.

3.1. LO Buffer Simulation

To mimic practical VCO, the input to the buffer was a sinusoid of amplitude 150mV. A transient simulation was performed. Figure 30 below shows the transient simulation result of this buffer. The sharp 1V peak -peak square wave output has a time period of ~415ps. This corresponds to an LO frequency of ~2.4GHz.

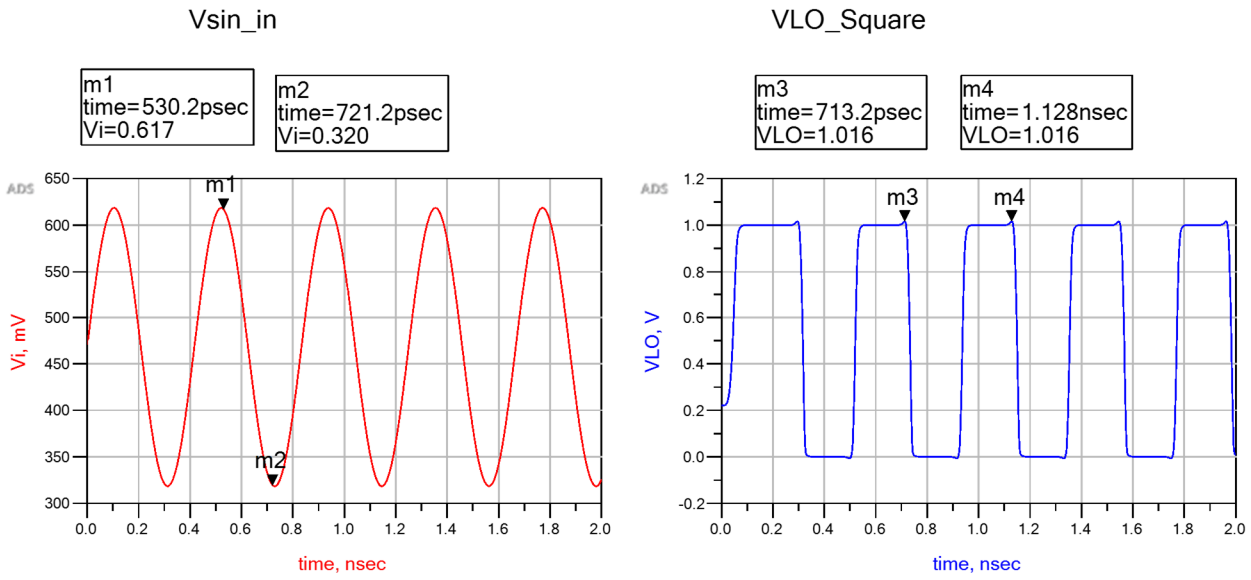


Figure 30: 300mV sinusoidal input(left) and 1V square wave output(right) from the LO buffer-driver circuit

Table 6 below summarizes the stage capacitance of the LO buffer-driver stage.

Table 6: Stage capacitance of LO driver

Stage	**1**	**2**	**3**
$C_{effective}$(fF)	4.1	8.4	16.3

The input amplifier stage(operating in the linear region) consumes 12µA. The total power consumed each LO buffer was calculated using equation 5 and sums up to be 68µW per driver. There are 4 drivers in the circuit. The total power from this buffer is ~272µW.

4. Passive Mixer

Passive mixers are inherently more linear than active mixers. As shown in Figure 31, the passive mixer comprises of the gm stage and an LO switching stage. In order to convert the commutating

current to voltage, a Transimpedance Amplifier(TIA) is used. The circuit shows a double balanced mixer. The passive mixer used in this design uses a single RF stage, complementary LO switch and a CMOS TIA. This is shown in Figure 32.

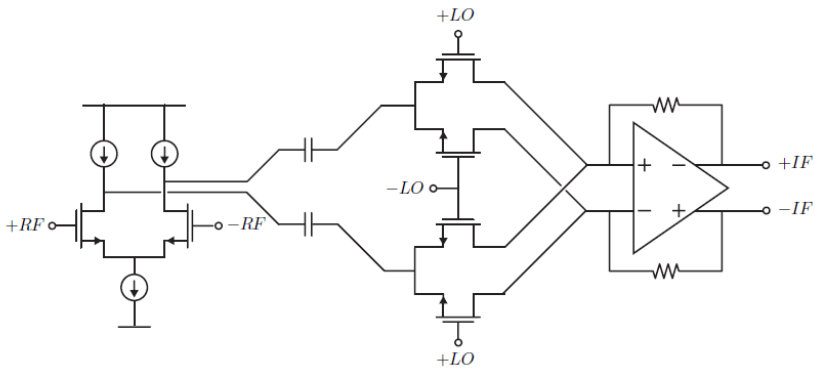


Figure 31: Passive Mixer

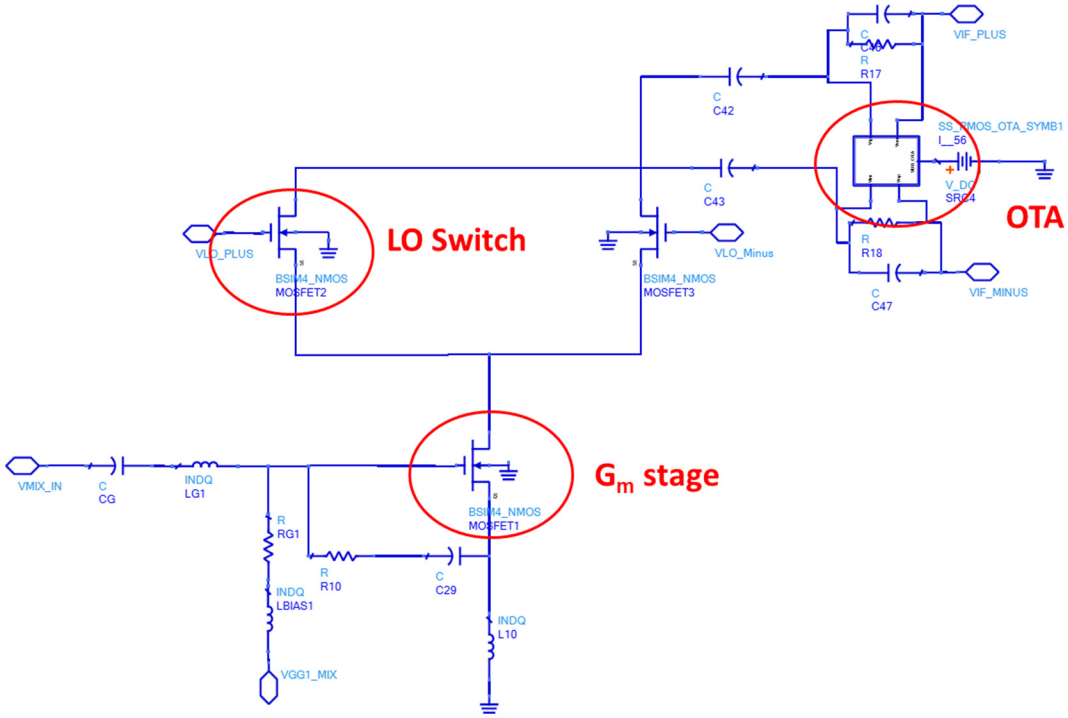


Figure 32: Passive mixer schematic

4.1. TIA design

A CMOS transimpedance amplifier was designed. As in the active mixer, the transconductor stage was biased in the saturation region. The gate of the LO stage was biased at 0.6V. The

LO swing was 1V. The sizing of the g_m stage was also reduced to (14µm by 65nm) as opposed to 16µm used in the active mixer.

The common mode voltage of the output of the LO stage was 0.3V. The core of the TIA is a fully differential Operational Transconductance Amplifier(OTA). The OTA is a fully differential amplifier comprises of a PMOS input stage and NMOS load. A common mode feedback(CMFB) circuit was also designed to maintain a common mode voltage of 0.3V. A PMOS input stage was chosen taking into account the common mode voltage level as well as lower noise contribution than the NMOS input device. Figure 33 is a schematic showing the fully differential OTA used in this project. Table 7 list the devices sizes.

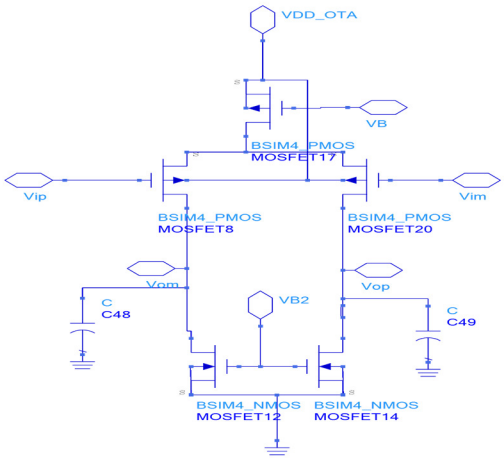


Figure 33: Fully differential OTA topology

Table 7: OTA used in the TIA

Device	**Value**	**Remarks**
MOSFET12, MOSFET 14	7µm(W) by 3µm(L)	Load
MOSFET8, MOSFET20	14µm(W) by 1µm(L)	Input Device
MOSFET17	9.8µm(W) by 0.27µm(L)	Current Source
I_{DC}	19.8µA	Total DC Current

The common mode feedback circuit comprises of a common mode sensing stage, an operational amplifier to generate the common mode bias. For this project, the common mode sensinng resistor was chosen to be 1MΩ.

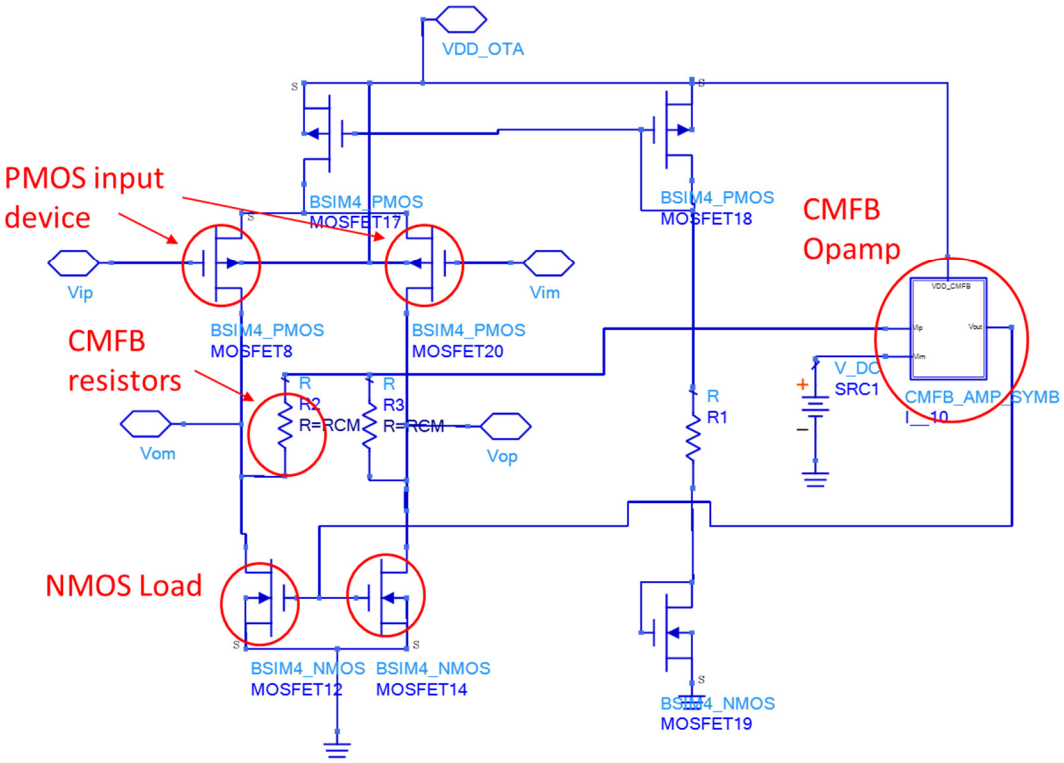


Figure 34: OTA with CMFB used in this project

4.1.1. CMFB Opamp

The CMFB Operational Amplifier(Opamp) is a single stage Opamp comprising of a PMOS input stage an NMOS current mirror active load. Table 8 below details the devices sizes of the OPAMP. All the devices are in saturation. The total DC current of the Opamp is 11µA.

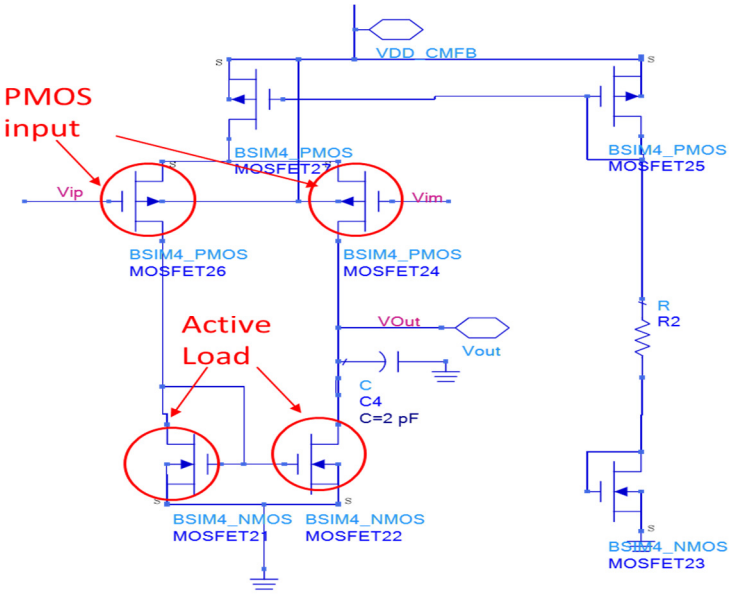


Figure 35: Opamp used for CMFB

Table 8: CMFB Opamp Design Parameters

Device	**Value**	**Remarks**
MOSFET26, MOSFET 24	7µm(W) by 3µm(L)	Input Device
MOSFET21, MOSFET22	14µm(W) by 1µm(L)	Load
R2	8KΩ	Bias resistor
MOSFET25	6µm(W) by 1µm(L)	Bias FET
MOSFET27	9.8µm(W) by 0.27µm(L)	Current Source
I_{DC}	11µA	Total DC Current

Figure 36 below is a plot showing the simulated open loop gain and phase of the CMFB Opamp. The open loop DC gain is 48dB and phase margin is 65^0.

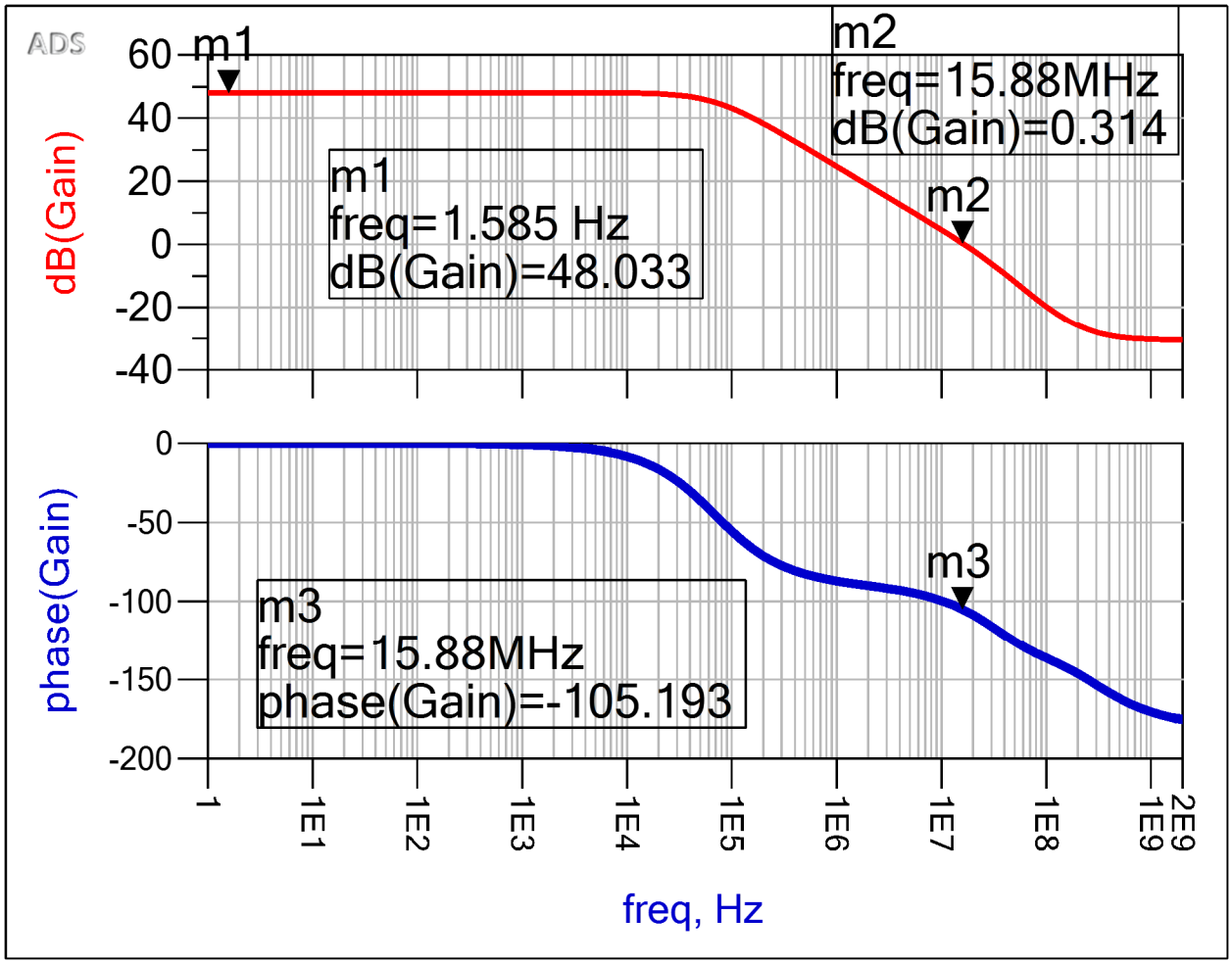


Figure 36:CMFB Opamp gain and phase

Figure 37 is the plot showing the simulated open loop gain and phase of the OTA with common mode feedback. The open loop gain is 44dB and phase margin is 87^0. The OTA with the CMFB amplifier consumes a total current of 32.5µA with 11µA coming from the CMFB Opamp alone.

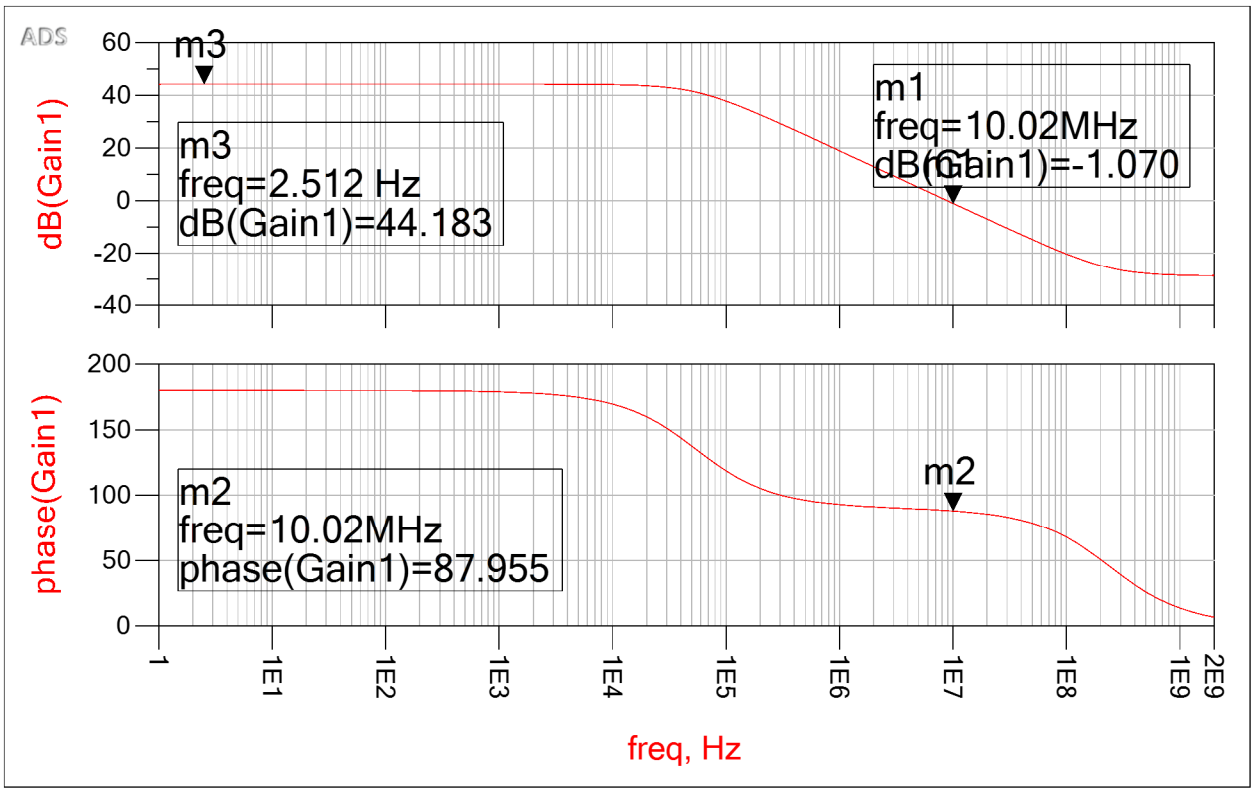


Figure 37: Gain and Phase Margin of the OTA used in the TIA

4.2. Passive Mixer simulation : Ideal LO Source

The feeback resistsnce of the TIA is a tradeoff between noise and linarity performance. The thermal noise from the resistor is input refered to the RF stage input. The thermal noise of see at the TIA output is:

$$V_{no} = \left(1 + \frac{R_f}{R_{par}}\right) \times V_{ni} \qquad (6)$$

Where R_f is the TIA feedback resistor, V_{ni} is the noise at the input of the TIA, R_{par} is the effective resistance of the switching LO pair. Noise amplificaiton can be reduced by reducing R_f. The optimal R_f was found to be 1.5kΩ.

Noise and linearity simulations were performed on the mixer. Figure 38 below is the schematic of the test bench of the passive mixer.

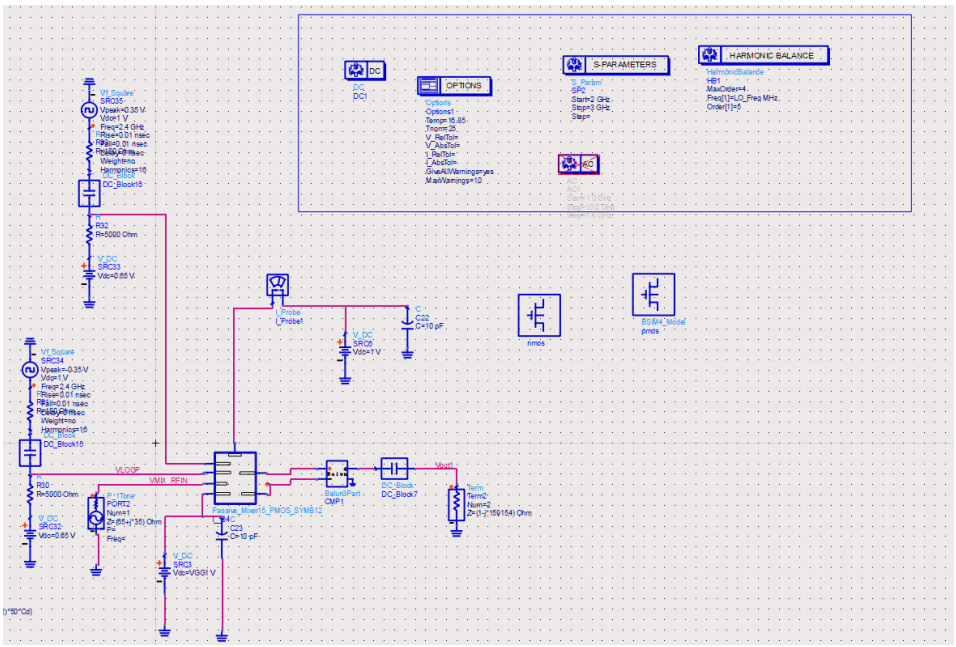


Figure 38: Passive mixer test bench

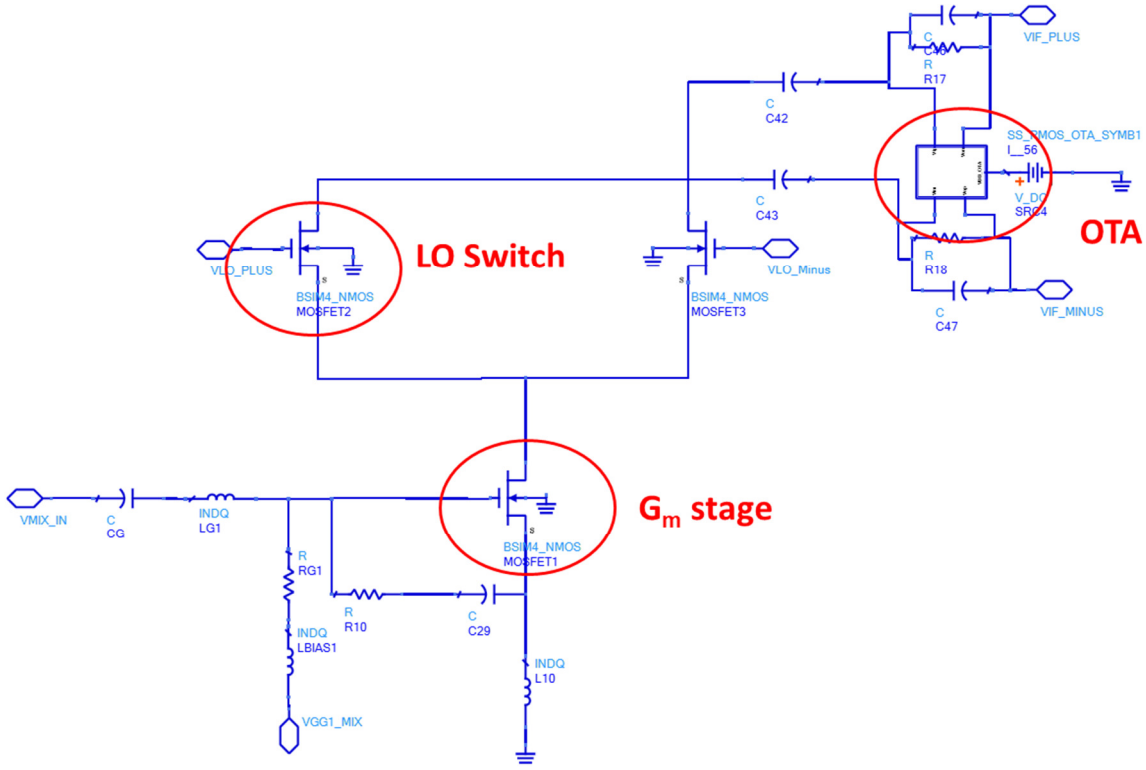


Figure 39: Passive mixer schematic

The input impedance of the mixer is 91+j*22Ω.Table 9 below summarizes the design features of the passive mixer.

Table 9: Passive Mixer Design Specifications

Device	**Value**	**Remarks**
MOSFET2,MOSFET3	22µm(W) by 65nm(L)	LO Stage
MOSFET1,	14µm(W) by 65nm(L)	LOStage1,2
R_{17}, R_{18}	1550	Feedback resistance
C_{47}, C_{48}	2pF	Q=50, feedback cap
R_{G1}	8kΩ	Gate Bias
L_{BIAS1}	10nH	Gate Choke
L_{15}	10nH	Input Match
L_{10}	2.1nH	degeneration inductance
R_{CM}	1MΩ	CMFB sensing
C_{29}	0.12pF	C_{GS} shunt
LO Swing	1	Q=50
V_{GG1_MIX}	0.4V	RF stage gate bias
VG_LO	0.6	LO Gate Bias
I_{DC}	504µA	Total DC current(RF+TIA)

Noise Figure Simulation

The simulated noise figure was 7.6dB and the mixer has a conversion gain if 11.3dB. Figure 40 is a plot showing the noise figure of the passive mixer. As shown in the figure, there is no flicker noise.

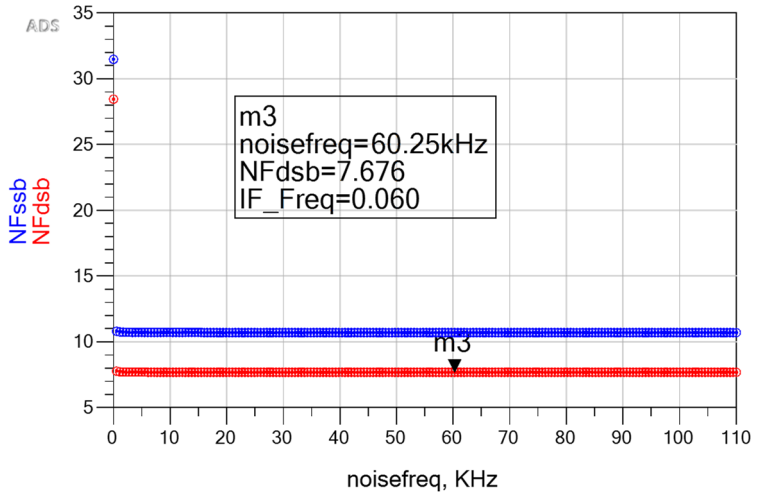


Figure 40:Passive Mixer Noise Figure

4.2.1. Non Linearity Simulation

Harmonic Balance analysis was used for simulating the mixer non-linearity. A two tone simulation was performed for simulating the mixer's intermodulation. The two different signal tones (spaced 1MHz apart) were fed to the mixer input and the input power level was swept. The power level of intermodulation products and the fundamental were plotted with respect to input power. This is shown in Figure 41. The mixer IIP3 was found to be -6dBm which is significantly higher than that with the active mixer.

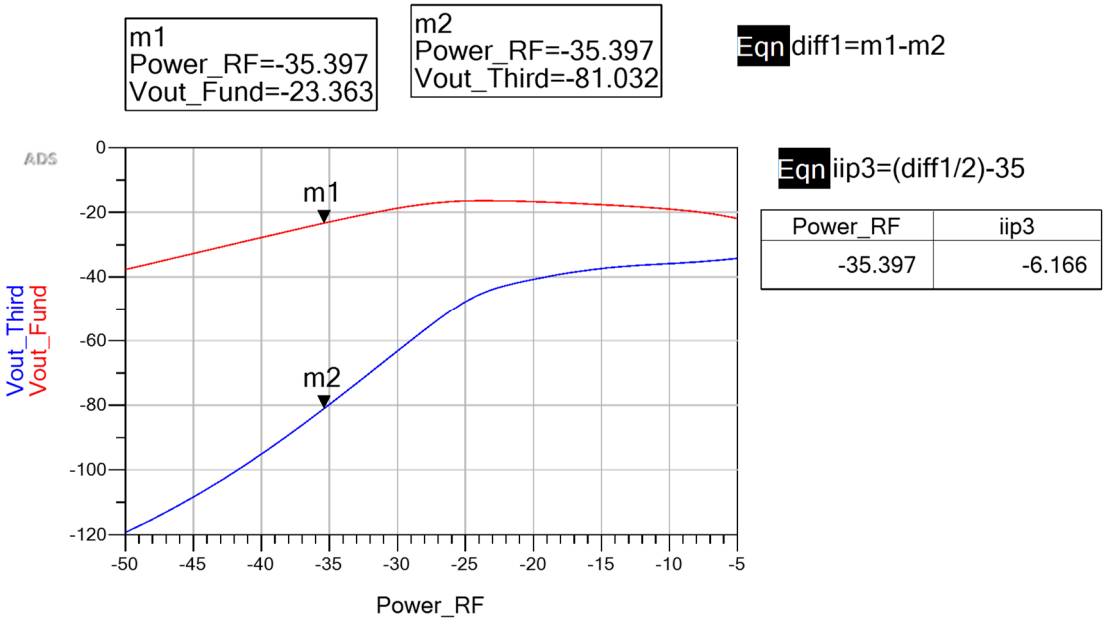


Figure 41: Passive Mixer IIP3

Table 10: Passive mixer performance

Parameter	**Passive Mixer**
DC Power	478µW(gm) +5µW(LO switch)+32.5µW(TIA)
Gain(dB)	11.35
NF(dB)	7.6
IIP3	-6dBm
S11	<-10dB

Figure 42 is the test bench showing the I and Q mixers and the LNA.

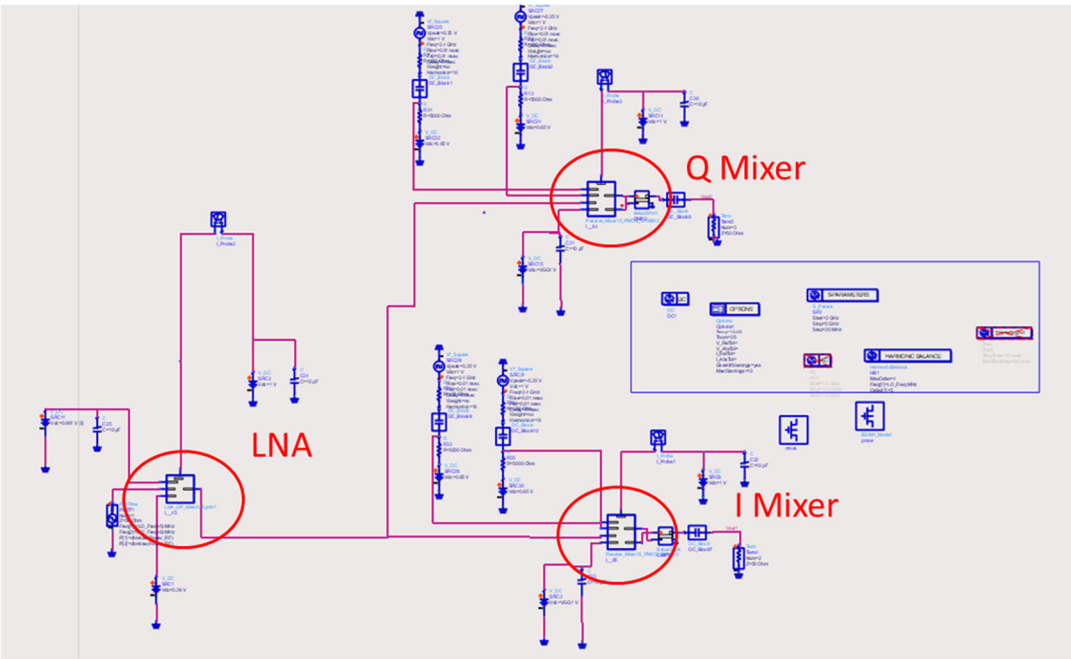


Figure 42: Receiver front end test bench

Figure 43 is the simulated noise figure of the receiver with the passive mixer.

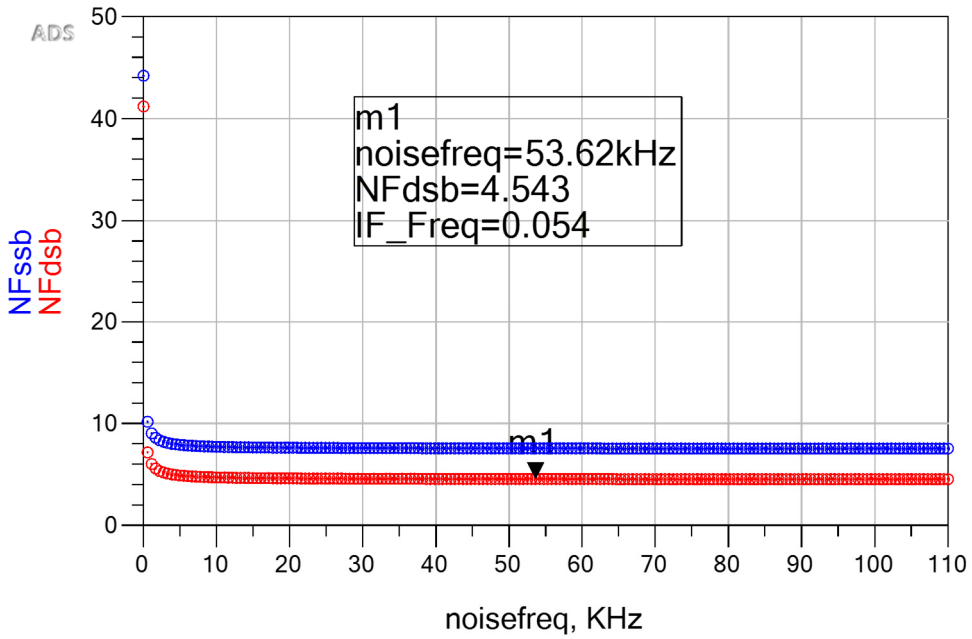


Figure 43:Noise figure of the receiver front end

Figure 44 is a plot showing the simulated third order intermodulation and fundamental output of the receiver when the input power is swept. The simulated IIP3 was -13.71dBm which is higher than that of the active mixer. Figure 45 is a plot showing the simulated IIP2. The IIP2 is 25dBm.

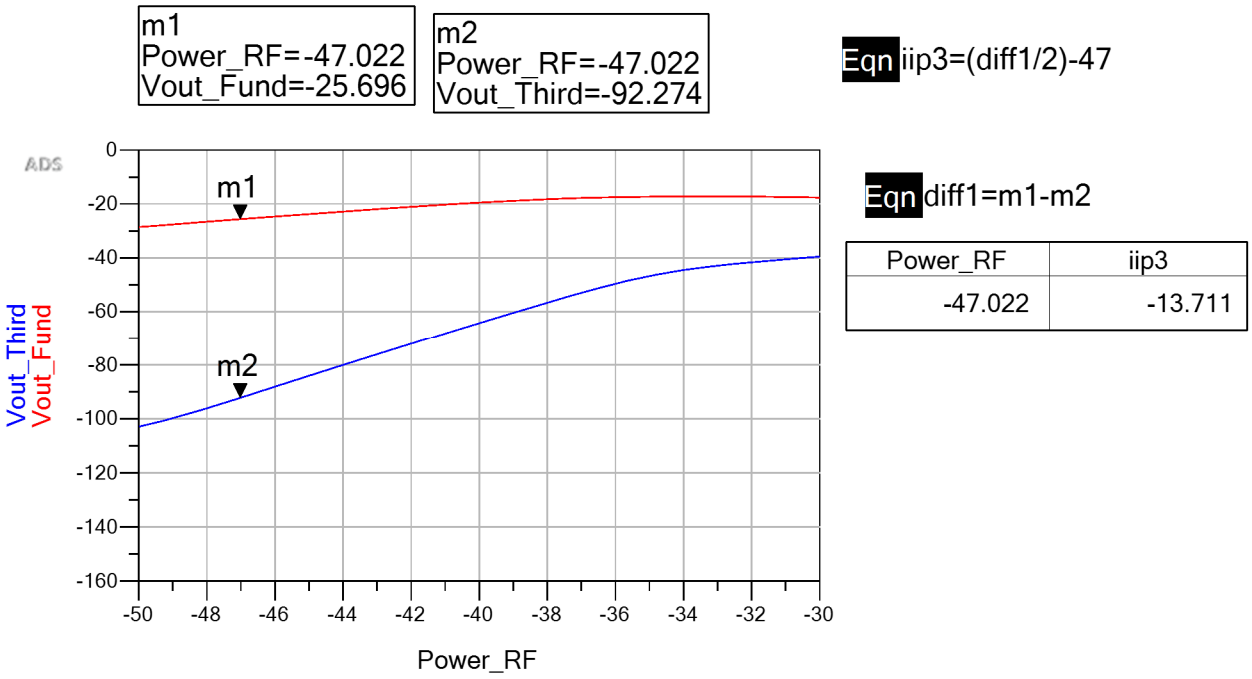


Figure 44: Receiver with passive mixer IIP3

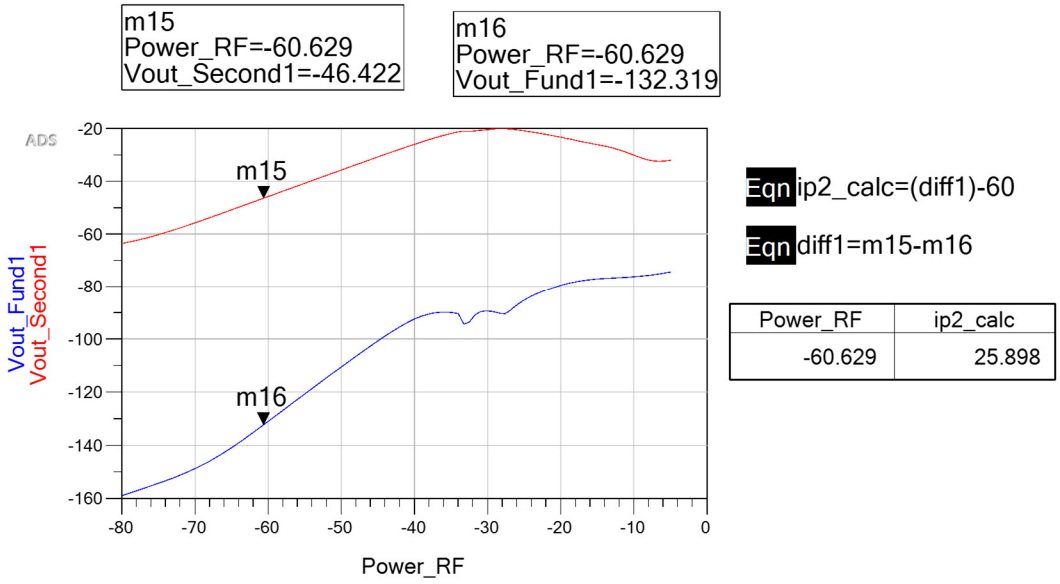


Figure 45: Simulated IIP2 of the receiver with passive mixer

Table 11 below summarizes the performance of the receive using the active mixer

Table 11: Performance summary of receiver front end using passive mixer

Parameter	**Target**	**Design**	**LNA**	**Mixer**
Power	<2mW	1.65mW	0.648	0.478
Gain(dB)	20	27	16	11
NF (dB)	<5	4.6	3.77	10
IIP3	>-20dBm	-13.7dBm[2]	-5	-6.16
S_{11}(dB)	<-20dB	-23	-23	-11
RF Bandwidth[3]	100MHz	225MHz	225MHz	

[1] 1MHz tone spacing
[2] LO power measured at LNA input
[3] 1dB bandwidth at LNA input

4.3. Passive Mixer Simulation: With LO Driver

The LO buffer-driver circuit shown in Figure 29 was integrated with the receiver shown in Figure 42.

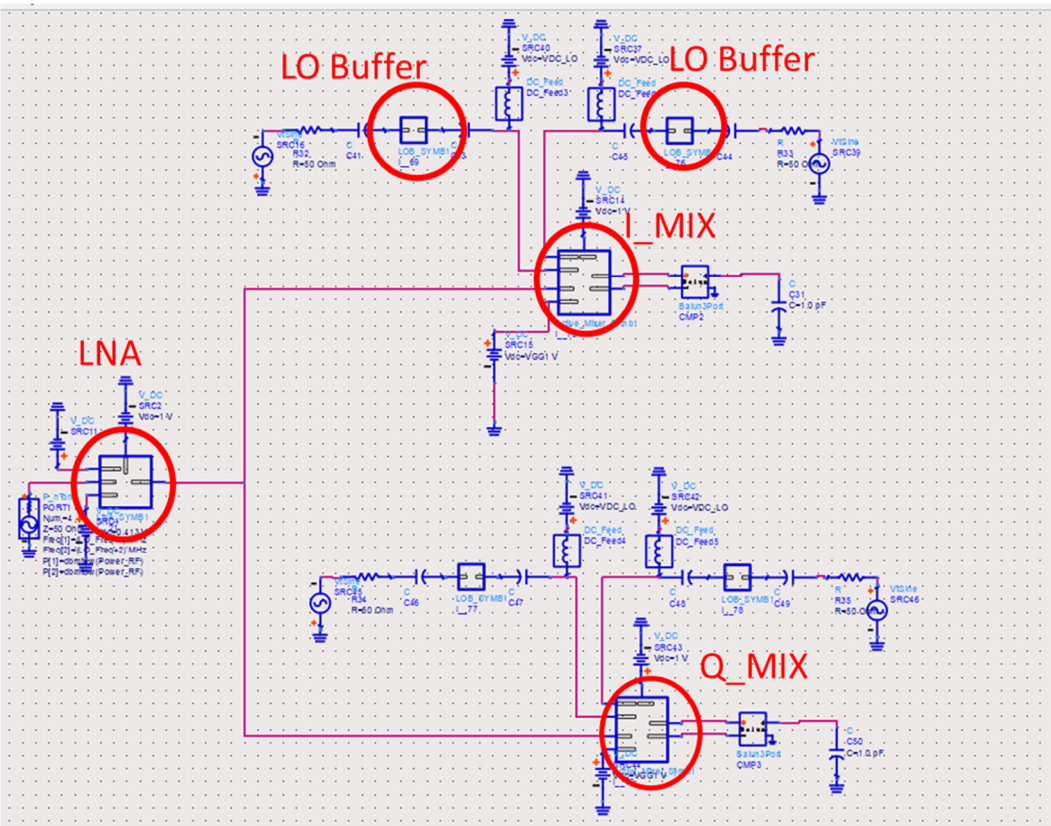


Figure 46: Receiver with LO buffer-driver integrated

Figure 47 below the 300mv sinusoidal input to the LO Driver-Buffer Circuit. Figure 48 is the transient response showing the square wave input to the LO ports of the mixer. The rise time of the pulse is ~ 40ps as shown in Figure 49 The transition point is exactly at 500mV, thereby minimizing any overlap. It is essential to avoid overlap between the LO switches tuning on or off. An overlap will cause the LO switch to operate in the linear region thereby adding to thermal noise. Besides, it also causes distortion. This point can be adjusted by the feedback resistor in the invertor of the LO buffer. The optimum value was found to be ~4kΩ.

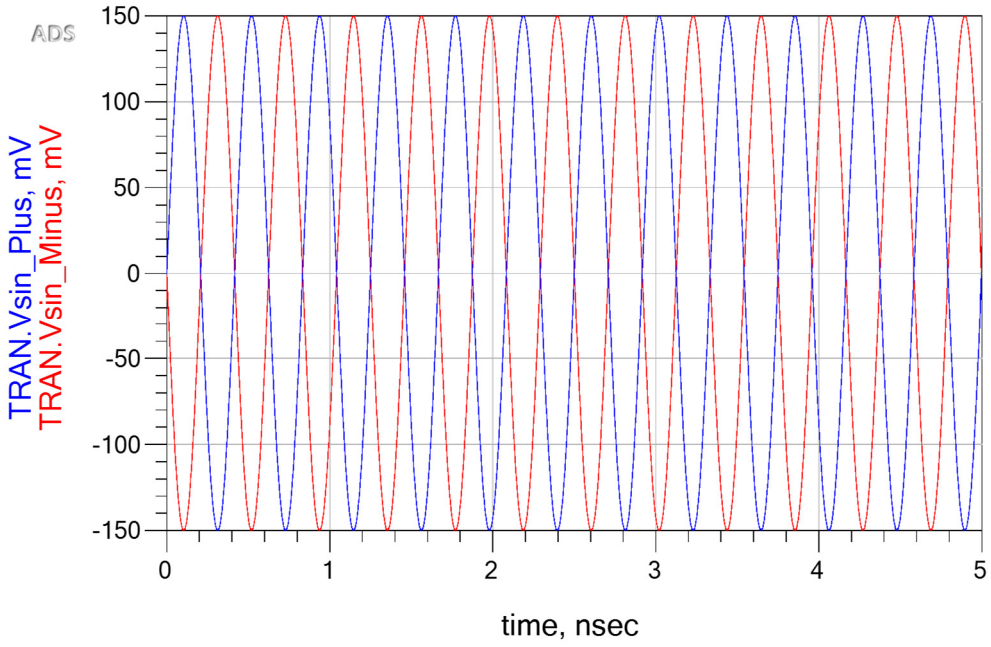


Figure 47: Sinusoidal input(300mv) to the LO Driver-Buffer Circuit

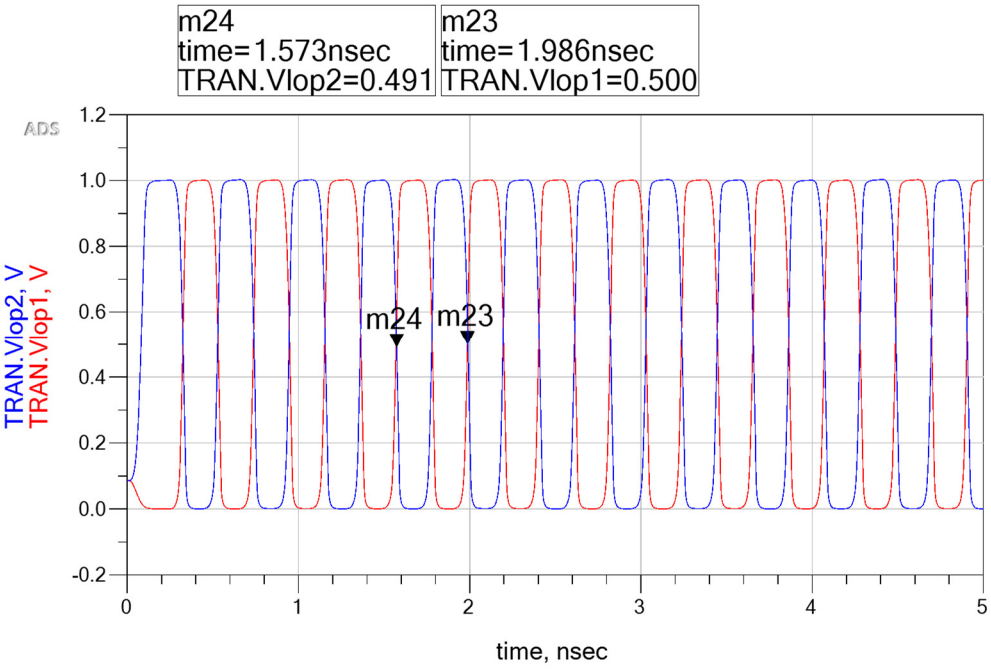


Figure 48: Transient signal at the input of the LO gate

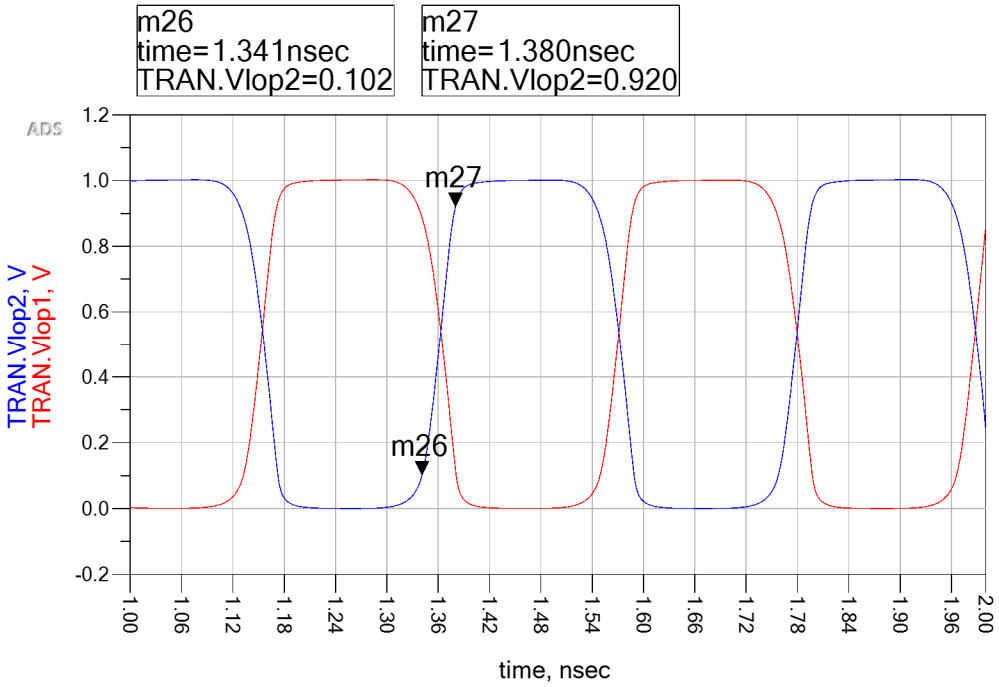


Figure 49: Square wave at the LO input showing finite rise time of 40ps

The non-idealities such as finite rise/fall time of the LO pulse, limited fanout and noise will impact the performance of the receiver. Therefore, after integrating the LO buffers, linear and non- linear simulations were performed on the receiver once again. Figure 50 is the simulated noise figure of the receiver with the passive mixer with the LO buffer. The noise figure is 4.8dB. The noise increased by ~0.2dB compared with the case where the LO ports were driven by an ideal source. Figure 51 below is a plot showing the third order intermodulation and fundamental output of this receiver when the input power is swept. The IIP3 is ~-15.5dBm which is a 2dBm increase from the case when the LO port was driven by an ideal source.

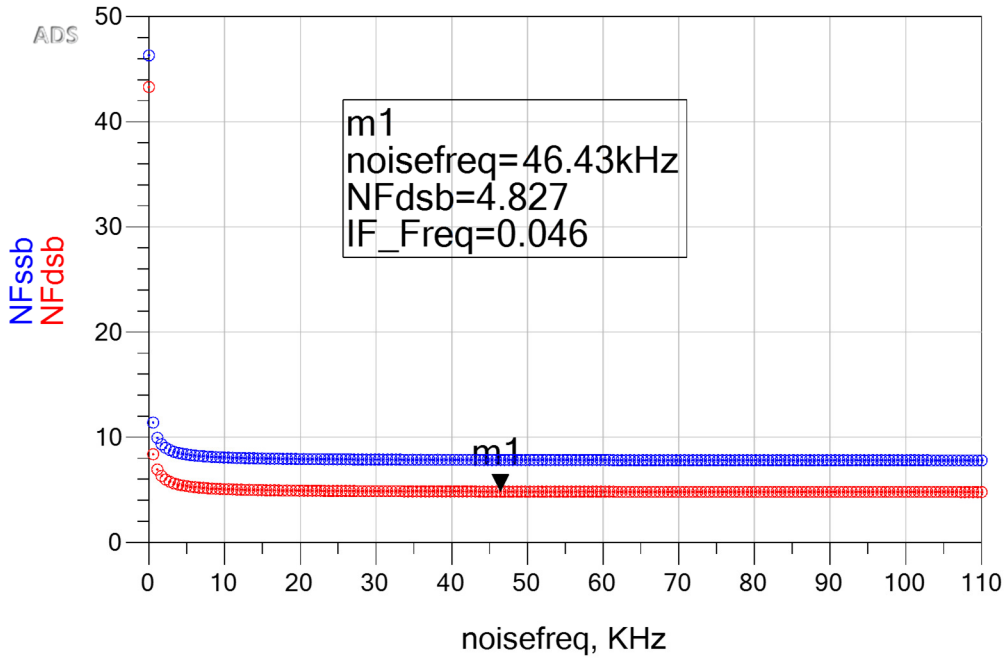


Figure 50: Noise figure of receiver with passive mixer (with LO buffer integrated)

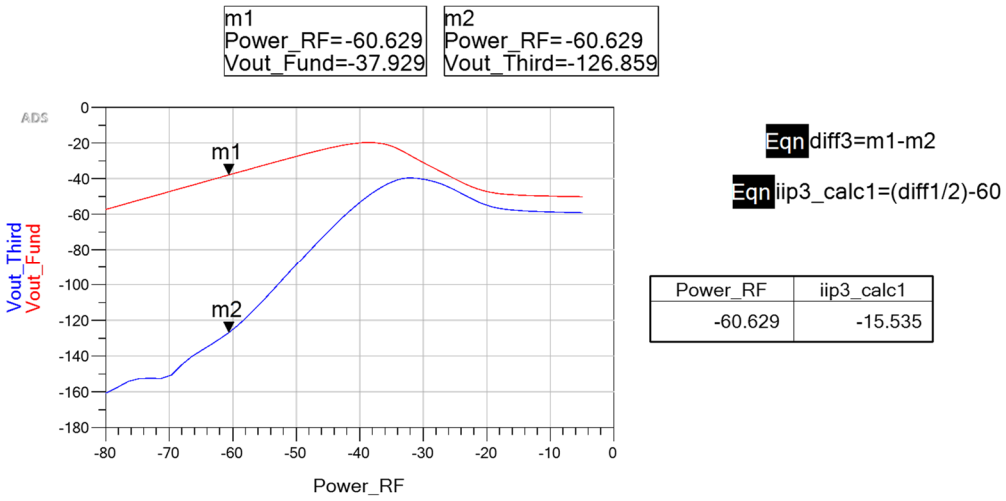


Figure 51: Third order intermodulation and fundamental output of the receiver with passive mixer and LO driver

Table 12 below summarizes the performance of the receive using the passive mixer integrated with the LO buffer-drivers

Table 12: Performance summary of receiver front end using passive mixer integrated with the LO driver-Buffer

Parameter	**Target**	**Design**	**LNA**	**Mixer (w/ TIA)**	**LO Driver**
Power	<2mW	1.928mW	0.648mW	0.504mW	0.272mW
Gain(dB)	20	27	16	11	-
NF(dB)	<5	4.8	3.7	9	-
IIP3	>-20dBm	-15.5dBm[2]	-5	-6.16	-
S_{11} (dB)	<-20dB	-23	-23	-11	-
RF Bandwidth[3]	100MHz	225MHz	225MHz		-

5. Summary

Two different direct conversion receiver front ends have been designed and simulated using a 65nm CMOS process. The primary difference between the two circuits is the implementaiton of the mixer. The first front end circuit uses a single balanced active mixer. The second type of front end circuit comprises of a passive mixer. Both front end circuits achieve an integrated noise figure less than 5dB, IIP3<-20dBm and power consumption less than 2mW. The front end end with an active mixer consumes 1.956mW of power, acheives a noise figure of 4.82dB,IIP3 of -19.1dBm and IIP2 of 25dBm. The front end with the passive mixer consumes a DC power of 1.92mW, noise figure of 4.82dB, IIP3 of -15dBm and IIP2 of 25.9dBm. The passive mixe comrpises of micropower CMOS Transimpedance Amplifier(TIA). TIA is based on an OTA which consumes 32µA with an open loop gain of 45dB. Both the front end circuits are entirely transistor based. In both cases, the LO buffer driver circuit alone consumes ~270µW.

The design approach involved a link budget analyses and practical assumptions of key parameters like noise figure and IP3 of individual blocks. Individual sub-circuits were then designed and optimized. The design space for the LNA is a tradeoff between noise figure, match, gain and bandwidth. The design space for the mixer(both active and passive) is a tradeoff between noise performance, power, LO swing and linearity. The receiver based on the passive mixer is slightly more linear than the receiver based on the active mixer. The LO driver circuit is a critical area of power dissipation with LO driver and switches consuming almost as much power as the mixer core.

The design is heavily constrained by the low power requirement of 2mW. Both linearity and noise performance can be improved at the cost of DC power. The initial simulation showed that the LNA noise can be reduced to 2.8dB for a DC current increase of 25%. Similarly, the mixer linearity can be improved at the cost of current increase in the transconductor stage and power dissipation from the LO stage.

References

[1] C. Campbell and S. Brown, "Modified S-Probe Circuit Element For Stability Analysis", *https://awrcorp.com/download/kb.aspx?file=S_Probe_White_Paper.pdf C. Campbell modified S-probe analysis*