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Low-Voltage Fully Differential CMOS Switched-Capacitor Amplifiers

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1. Introduction

Analog signal amplification in discrete-time system can be performed by switched-capacitor amplifiers (Martin et al., 1987). Switched-capacitor amplifier has been used in the design of digital-to-analog converter (Yang & Martin, 1989). The schematic for the switched-capacitor amplifier is shown in Figure 1.

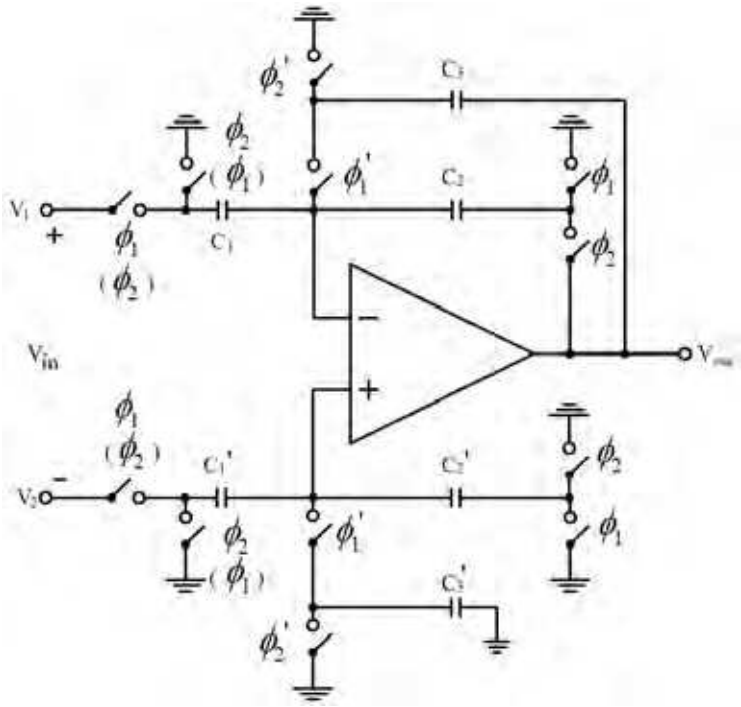

Fig. 1. A differential-to-single-ended CMOS switched-capacitor amplifier. Depending on the input-stage clock signals, the amplifier can be either noninverting (as shown) or inverting (input-stage clocks shown in parentheses).

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Assuming an infinite op amp gain, the output voltage at end of ϕ_2 is given by

$$V_{out}(nT) = \frac{C_1}{C_2} V_{in}(nT - \frac{T}{2}), \quad (1)$$

irrespective of the op amp offset voltage. If the clock waveforms shown in parentheses are used, then an inverting function is realized, and

$$V_{out}(nT) = -\frac{C_1}{C_2} V_{in}(nT), \quad (2)$$

again independent of the op amp input offset voltage. During the reset phase (ϕ_1), C_3 is connected in feedback around the op amp which causes the output change only by the op amp input offset voltage. The switches are realized as CMOS transmission gate. For low supply voltages, a conductance gap begins to appear around the middle of the supply range (Crols & Steyaert, 1994). This means that under low-voltage operation, this configuration no longer works. Existing solutions of low-voltage operation of switched-capacitor circuits include using low threshold voltage process (Matsuya & Yamada, 1994), switched-opamp technique (Baschirotto & Castello, 1997; Cheung et al., 2001; Cheung et al., 2002; Cheung et al., 2003; Crols & Steyaert, 1994; Peluso et al., 1997; Peluso et al., 1998; Sauerbrey et al., 2002; Waltari & Halonen, 2001; Wu et al., 2007), opamp-reset switching technique (Chang, & Moon, 2003; Keskin et al., 2002; Wang &. Embabi, 2003), voltage multiplier (charge pump) technique (Nicollini et al., 1996; Rombouts et al., 2001), clock multiplier (clock booster) technique (Au & Leung, 1997; Rabii & Wooley, 1997), and bootstrapping switch technique (Abo & Gray, 1999; Dessouky & Kaiser, 2001; Park et al., 2004). First, the use of low-threshold transistors involves special and high-cost technology (Matsuya & Yamada, 1994). The switched-opamp technique (Baschirotto & Castello, 1997; Cheung et al., 2001; Cheung et al., 2002; Cheung et al., 2003; Crols & Steyaert, 1994; Peluso et al., 1997; Peluso et al., 1998; Sauerbrey et al., 2002; Waltari & Halonen, 2001; Wu et al., 2007) and opamp-reset switching technique (Chang, & Moon, 2003; Keskin et al., 2002; Wang &. Embabi, 2003) can only be applicable to filters, delta-sigma modulators, and pipelined analog-to-digital converters. The main limitations of voltage multiplier (charge pump) technique (Nicollini et al., 1996; Rombouts et al., 2001) regards: the gate-oxide breakdown reliability, the need to supply a dc current to the op amps from the multiplied supply (this necessitates the use of an external capacitor, with additional cost), and the conversion efficiency of the charge pump (which is lower than 100%). The clock multiplier (clock booster) technique (Au & Leung, 1997; Rabii & Wooley, 1997) suffers from the technology limitation associated with the gate oxide breakdown. Device reliability can be assured in the bootstrapped switch technique (Abo & Gray, 1999; Dessouky & Kaiser, 2001; Park et al., 2004), owing to keeping the terminal-to-terminal voltages of the MOSFET devices within the rated operating supply voltage of the technology. The bootstrapped switch provides a small, nearly constant input resistance. The switch linearity is also improved, and signal-dependent charge injections is reduced.

To improve the overall linearity, minimize the effect of common-mode interference and noise, the fully differential approach has obtained wider acceptance for accurate and/or high-speed signal processing. The switched-capacitor amplifier in (Martin et al., 1987) is a differential-to-single-ended design. A fully differential switched–capacitor amplifier using series compensation MOSFET capacitors has been presented in (Yoshizawa et al., 1999).

However its operating voltage is ±2.5-V. Consequently there is an increasing demand to extend these improvements to this circuit.
This chapter describes the design of two 1V fully differential CMOS switched-capacitor amplifiers in a standard CMOS technology using improved bootstrapped switches. In section 2, the circuit realization of these two switched-capacitor amplifiers is addressed. In section 3 the circuit design of low-voltage building blocks is described. Experimental results are presented in section 4 to support the ideas put forth in paper. Finally conclusion is given.

2. Circuit Description

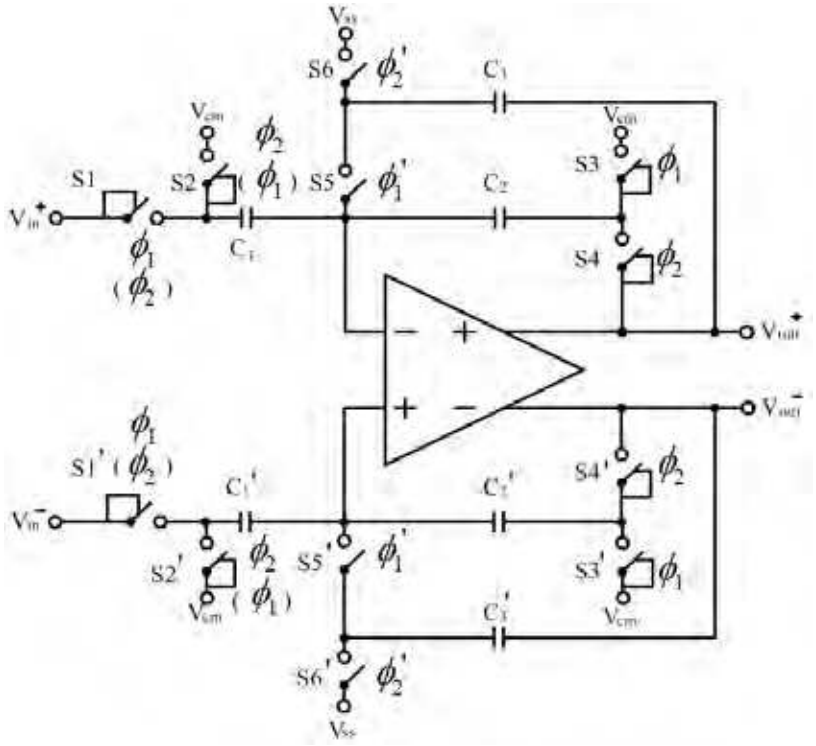


Fig. 2. First low-voltage fully differential CMOS switched-capacitor amplifier. Depending on the input-stage clock signals, the amplifier can be either noninverting (as shown) or inverting (input-stage clocks shown in parentheses).

Figure 2 shows the first low-voltage fully differential CMOS switched-capacitor amplifier based on improved bootstrapped switches described in section 3.2, where switches S1-S4 and S1′-S4′ are matched improved bootstrapped switch pairs and switches S5-S6 and S5′-S6′ are NMOS matched switch pairs. In order to minimize the number of improved bootstrapped switches, two analog reference voltages are used: V_{SS} at the op amp input where a normal NMOS switch can be used to switch the lowest supply voltage, and a $\frac{V_{DD}+V_{SS}}{2}$ common-mode voltage at the op amp output and the circuit input to maximize

the signal swing. The improved bootstrapped switch is used to switch signals at this voltage level. Figure 3 is the single-ended version of Figure 2.

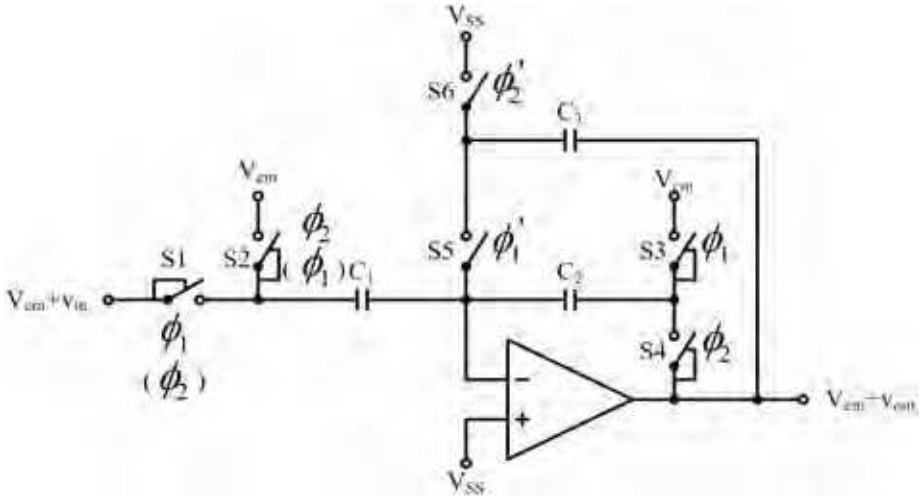


Fig. 3. Single-ended version of Fig. 2.

To see how this circuit operates, consider the inverting circuit during the reset phase (ϕ_1) and during valid output phase (ϕ_2), as shown in Figure 4. Then based on charge conservation principle we can write:

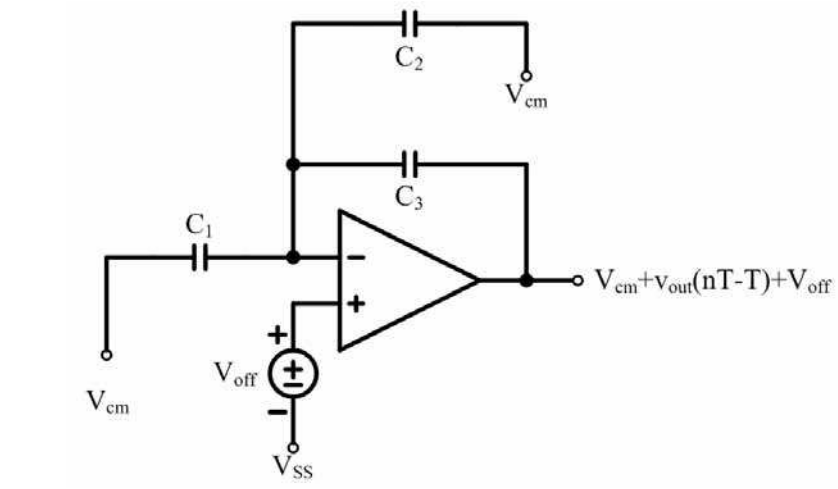
$$C_1(V_{SS}+V_{off}-V_{cm})+C_2(V_{SS}+V_{off}-V_{cm})$$

$$=C_1[V_{SS}+V_{off}-V_{cm}-v_{in}(nT)]+C_2[V_{SS}+V_{off}-V_{cm}-v_{out}(nT)],$$

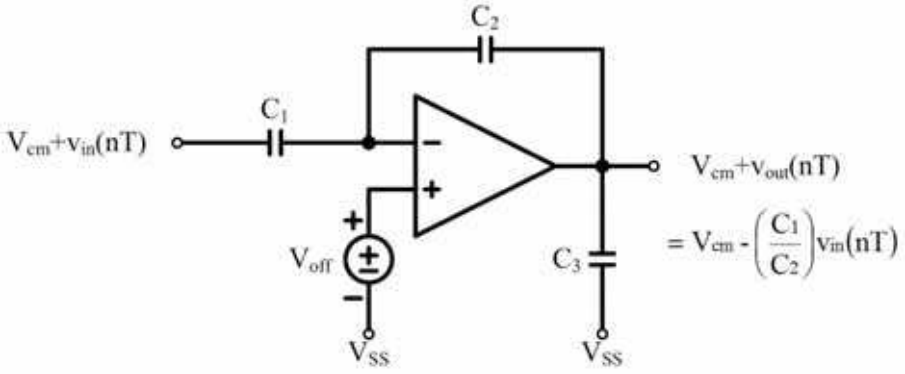
$$\text{or } v_{out}(nT)=-\frac{C_1}{C_2}v_{in}(nT). \tag{3}$$

It should be noted that the clock waveforms with the primed superscripts change before the nonprimed waveforms in order to reduce nonlinearities due to charge injection.

Another technique to further reduce the number of improved bootstrapped switches is shown in Figure 5, where switches S1 and S4 and S1′ and S4′ are matched improved bootstrapped switch pairs. Those switches connected to V_{SS} are realized with NMOS transistors, while those switches connected to V_{DD} are realized with PMOS transistors. In Figure 5 a single reference voltage at V_{SS} is used. However, the signal still varies around $\frac{V_{DD}+V_{SS}}{2}$ at the circuit input as well as at the op amp output to preserve the maximum swing. The difference between the two reference voltages is compensated by injecting a fixed amount of charge at the op amp input using extra capacitor pairs $C_{M1}=\frac{C_1}{2}$ and $C_{M2}=\frac{C_2}{2}$ ($C'_{M1}=\frac{C'_1}{2}$ and $C'_{M2}=\frac{C'_2}{2}$) switching between V_{DD} and V_{SS} (Baschirotto & Castello, 1997). Figure 6 is the single-ended version of Figure 5.



(a)



(b)

Fig. 4. Single-ended CMOS switched-capacitor amplifier, (a) during reset phase (ϕ_1), (b) during valid output phase (ϕ_2).

To see how this circuit operates, consider the inverting circuit during the reset phase (ϕ_1) and during valid output phase (ϕ_2), as shown in Figure 7.
Then based on charge conservation principle we can write:

$$C_1(V_{SS}+V_{off}-V_{SS})+C_2(V_{SS}+V_{off}-V_{SS})+(C_{M1}+C_{M2})(V_{SS}+V_{off}-V_{DD})$$

$$=C_1[V_{SS}+V_{off}-V_{cm}-v_{in}(nT)]+C_2[V_{SS}+V_{off}-V_{cm}-v_{out}(nT)]$$
$$+(C_{M1}+C_{M2})(V_{SS}+V_{off}-V_{SS}),$$

$$\text{or } v_{out}(nT)=-\frac{C_1}{C_2}v_{in}(nT)\,. \tag{4}$$

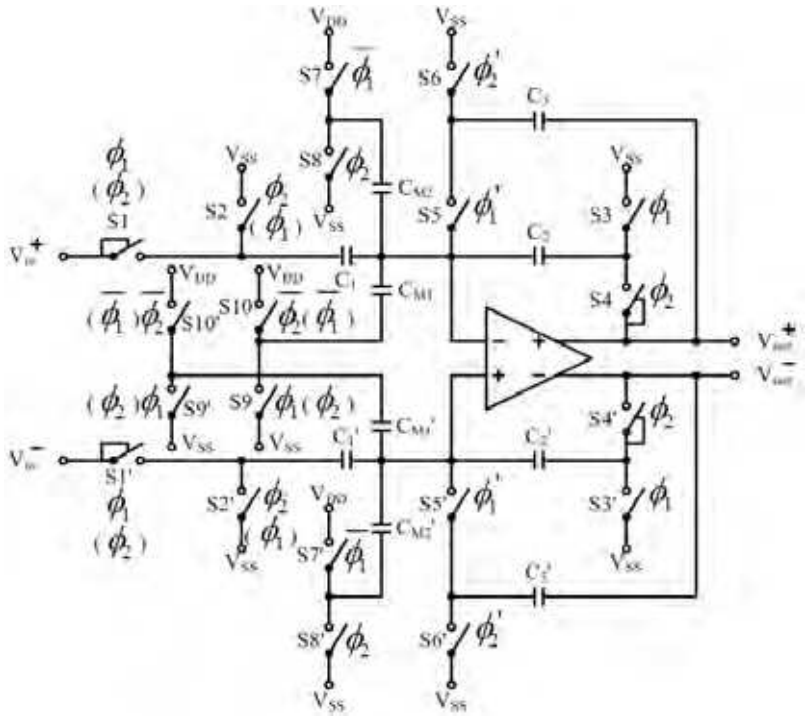


Fig. 5. Second low-voltage fully differential CMOS switched-capacitor amplifier. Depending on the input-stage clock signals, the amplifier can be either noninverting (as shown) or inverting (input-stage clocks shown in parentheses).

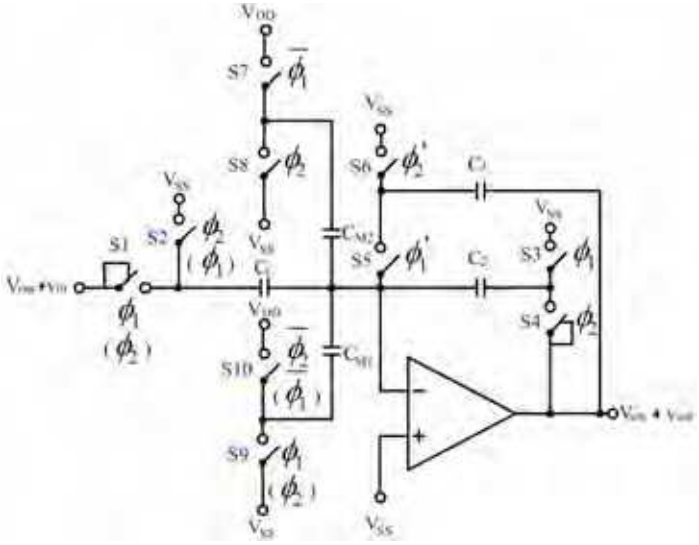


Fig. 6. Single-ended version of Fig. 5.

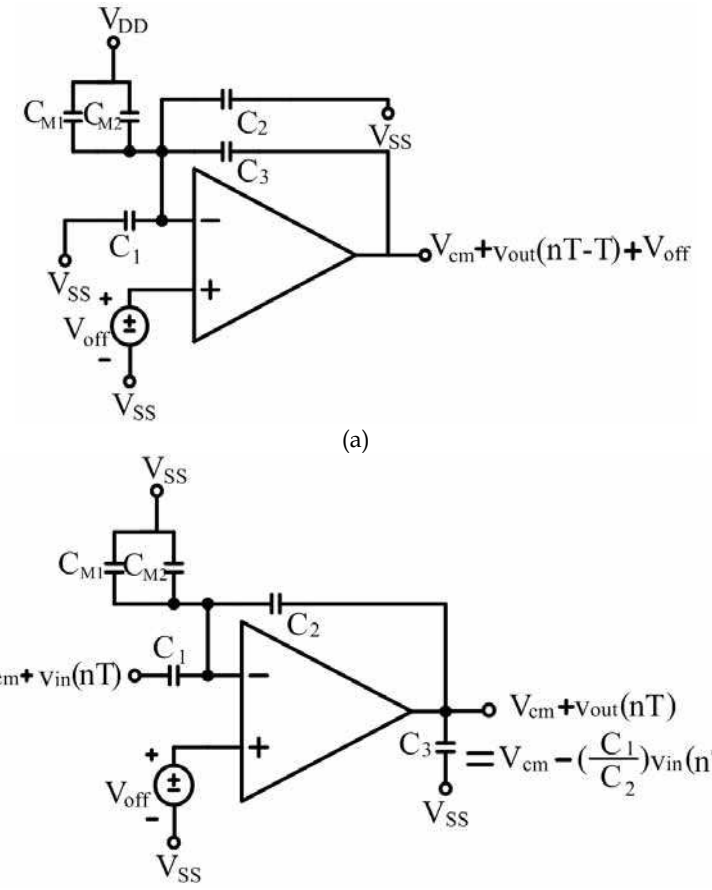


Fig. 7. Single-ended CMOS switched-capacitor amplifier, (a) during reset phase (ϕ_1), (b) during valid output phase (ϕ_2).

3. Low-voltage building blocks

In this section, the low-voltage circuit building blocks used in the two fully differential CMOS switched-capacitor amplifiers are discussed

3.1 Op Amp

Figure 8 shows the used op amp. It is based on a fully differential folded-cascode p-type two-stage Miller-compensated configuration. The second stage is a common-source amplifier with active load which also allows a large output swing. In order to avoid the common-mode feedback (CMFB) circuit for the first stage, transistors *M51*, *M52*, *M61*, and *M62* are used, which is similar to (Waltari & Halonen, 1998). For the second stage, a simple passive switched-capacitor CMFB circuit, shown in Figure 9, is used. The improved bootstrapped switches are used to connect and disconnect the common-mode sensing capacitor.

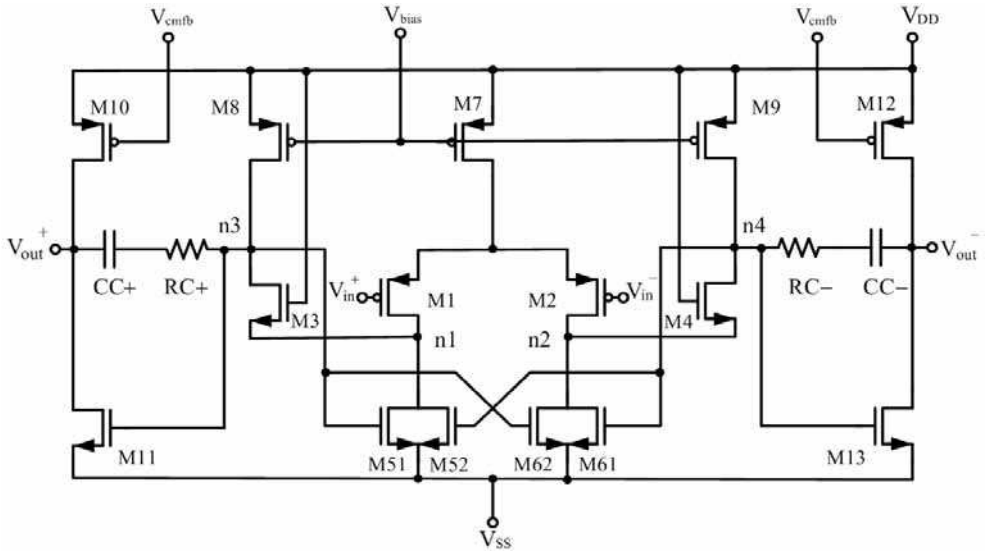


Fig. 8. Low-voltage op amp.

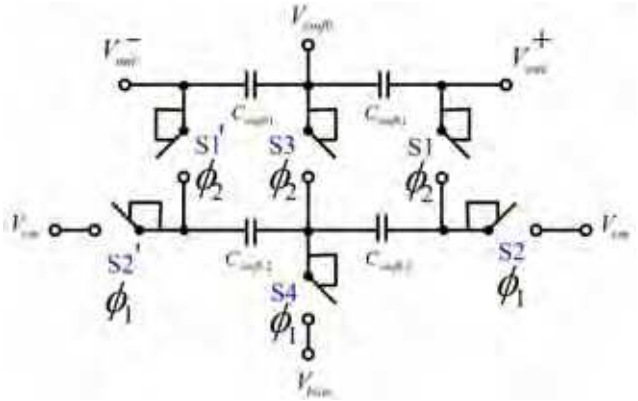


Fig. 9. Common-mode feedback circuit for the low-voltage op amp.

3.2 Improved bootstrapped switch

The improved bootstrapped switch shown in Figure 10 is utilized in the proposed circuit. The circuitry is improved version of that presented in (Abo & Gray, 1999). In the circuit presented in (Abo & Gray, 1999), the voltage at the drain side of the main switch *M11* must be always higher than that at the source side at the switching moment to prevent the gate-drain voltage from exceeding V_{DD} during the turn-on transient. In order to overcome this limitation, an additional transistor *M14* has been added on the drain side, such that the switch *M11* becomes completely symmetrical. This bootstrapping circuit thus allows switch operation (transistor *M11*) from rail-to-rail while limiting all gate-source/drain voltages to V_{DD} avoiding any oxide overstress.

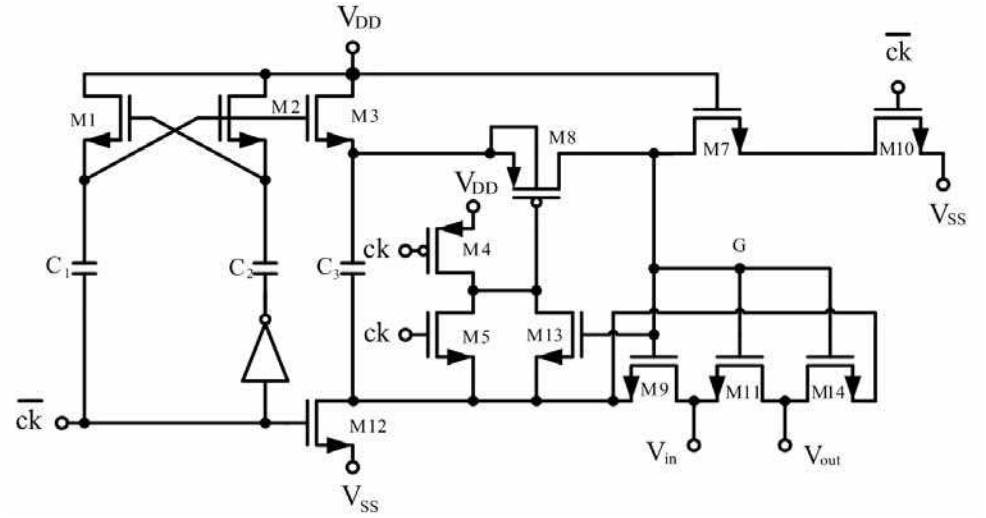


Fig. 10. Improved bootstrapped switch.

4. Experimental results

Based on the principles presented earlier, we have designed two 1-V fully differential CMOS switched-capacitor amplifiers. These two switched-capacitor amplifiers were operated with ±0.5-V. The capacitor sizes used were C_1 =1.25-pF, C_2 =0.25-pF, and C_3 =0.25-pF, for a nominal gain of -5. The circuits of Figure 2 and Figure 5 were fabricated using a TSMC 0.35-μm double-poly four-metal CMOS technology. Figure 11 and Figure 12 show the photomicrographs of Figure 2 and Figure 5, respectively. The chip areas of Figure 2 and Figure 5 excluding bonding pads are 414×278-μm² and 460×330-μm², respectively.

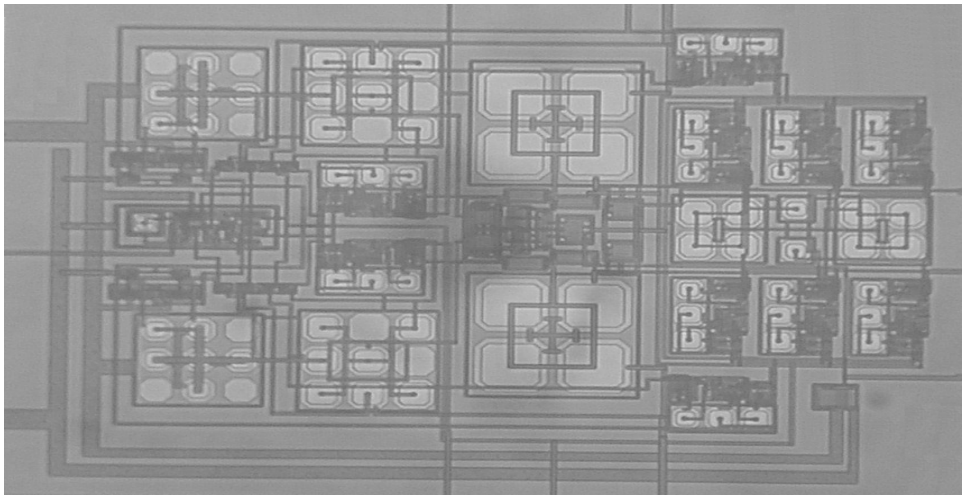


Fig. 11. Photomicrograph of Fig. 2.

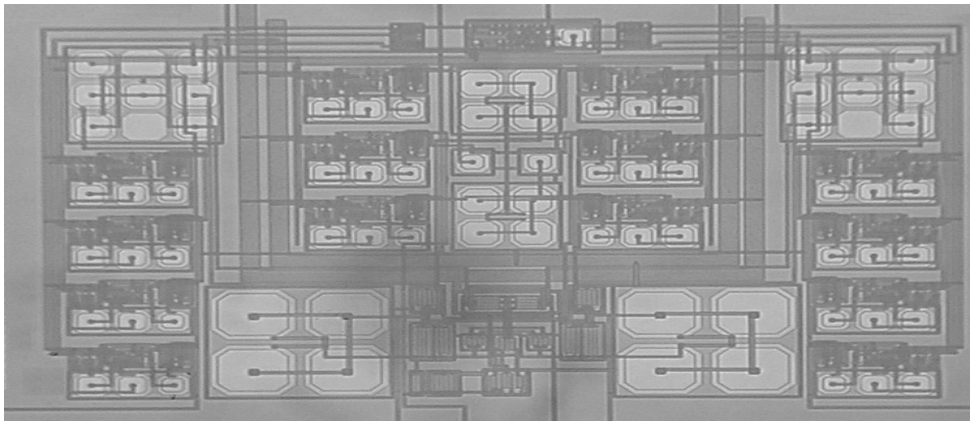


Fig. 12. Photomicrograph of Fig. 5.

Two figures of the measured input/output waveforms for 0.2V peak-to-peak sinusoidal differential input signal are shown in Fig. 13 and Fig. 14, respectively. The input signal was at 10kHz whereas the clock signal was at 1MHz. It can be seen that the gain is very close to the nominal value of -5.

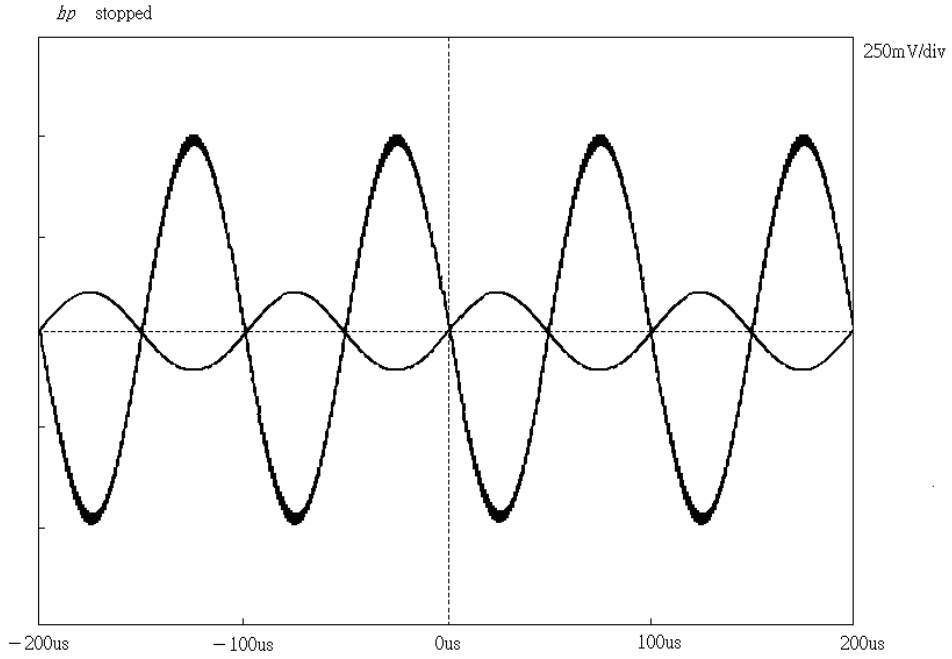


Fig. 13. Measured differential input and output waveforms of Fig. 2 (f_{clk}=1-MHz, f_{in}=10-kHz, sinusoidal differential input voltage=0.2-V_{pp}).

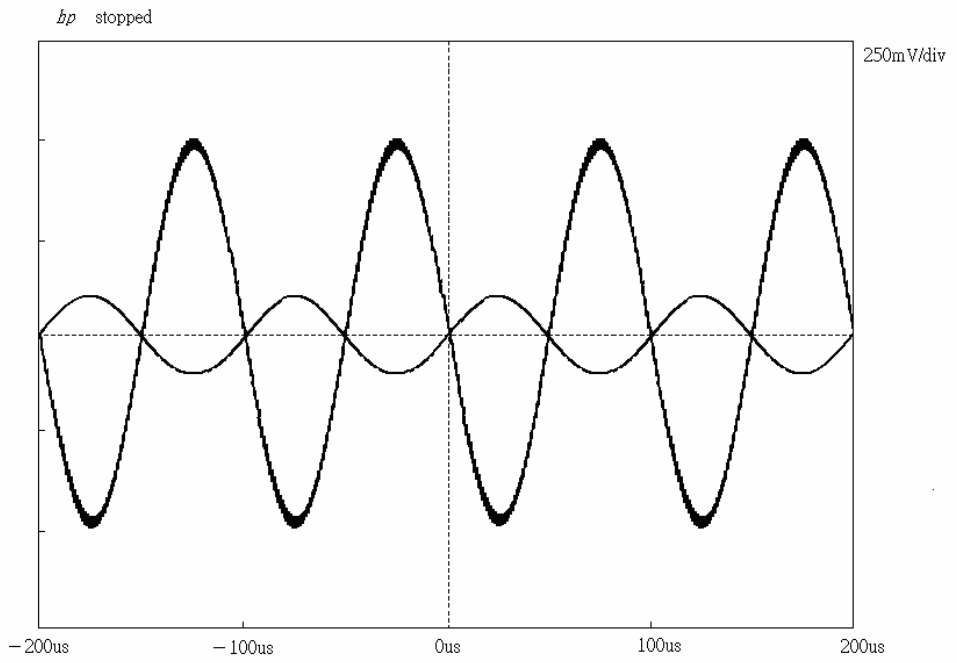


Fig. 14. Measured differential input and output waveforms of Fig. 5 (f_{clk}=1-MHz, f_{in}=10-kHz, sinusoidal differential input voltage=0.2-V_{pp})

Fig. 15 and Fig. 16 show the resulting output spectrum. As shown in Fig. 15 and Fig. 16, the even-order harmonics have been largely attenuated by the fully differential topology and 59dB and 52dB spurious-free dynamic range (SFDR) are exhibited, respectively. The circuits of Fig. 2 and Fig. 5 dissipate 206.5μW and 206.6μW, respectively with a 1V power supply.

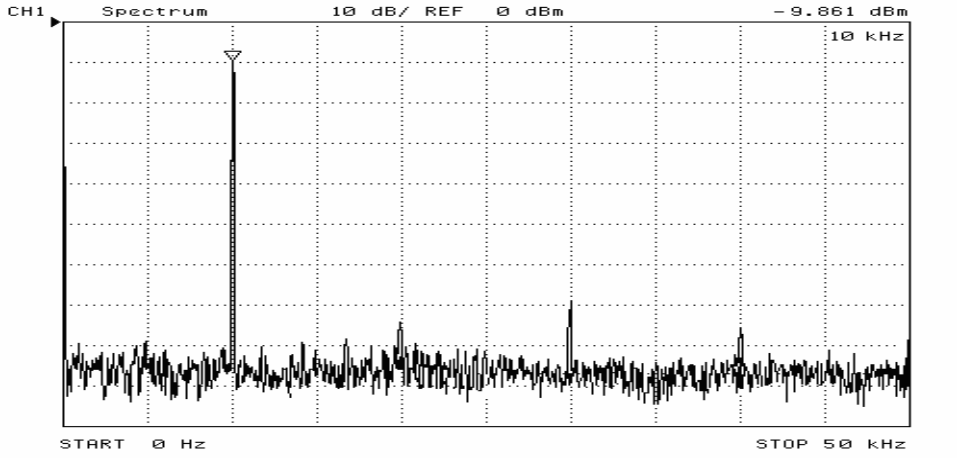


Fig. 15. Measured output spectrum of Fig. 2.

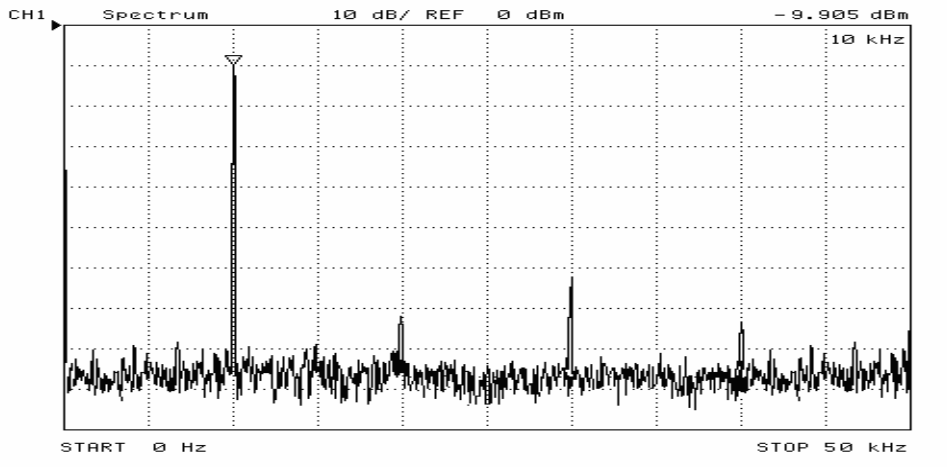


Fig. 16. Measured output spectrum of Fig. 5.

5. Conclusion

Two fully differential CMOS 1-V switched-capacitor amplifiers have been described. Rail-to-rail operation of improved bootstrapped switches allows very low voltage robust switched-capacitor designs in standard CMOS technologies while avoiding transistor gate oxide overstress. The circuits have been fabricated and all aspects of their performance have been confirmed.

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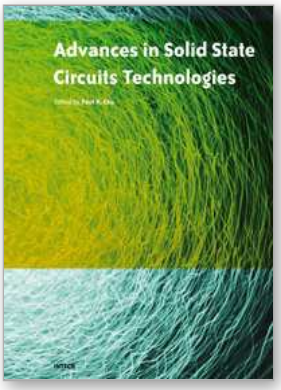

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