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Low-Voltage High-Speed Ring Oscillator With a-InGaZnO TFTs

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ABSTRACT This paper presents a high-speed ring oscillator (RO) with amorphous Indium-Gallium-Zinc-Oxide Thin-film transistors (a-IGZO TFTs). The proposed RO reduces the delay of a single stage inverter using intermediate signals generated within the RO, hence, improving the speed. To validate the proposed idea, two conventional ROs (with diode-load load inverter and bootstrapped pseudo-CMOS inverter) and the proposed RO were fabricated at a temperature $\leq$ 180°C. Measured results of the proposed RO have shown a frequency and power-delay-product (PDP) of 173.2 kHz and 0.7 nJ at a supply voltage of 6 V. Further, it shows approximately 155% (44%) increase in frequency and 14% (24.5%) decrease in PDP compared to diode-load inverter (bootstrapped pseudo-CMOS inverter) based ROs. Therefore, the proposed RO finds applications in low-voltage and high speed designs for timing signal generation.

INDEX TERMS High speed ring oscillators, oxide TFTs, low-voltage designs.

I. INTRODUCTION

Amorphous Indium-Gallium-Zinc-oxide thin-film transistor (a-IGZO TFT) technology has various advantages compared to other TFT (organic and a-Si:H) technologies [1]–[3], which extend its applications into various domains as RFID tags, high-resolution display drivers, biosensor readout circuits or radiation sensing system [4]–[9]. Still, IGZO TFTs have some drawbacks, such as the lack of a stable, reproducible and process-compatible p-type oxide TFT technology to enable power-efficient CMOS topologies, or the modest mobility (around 10-20 cm^2/Vs) when operating frequencies above a few MHz are envisaged. As a result, various circuit techniques [10]–[14] have been adopted to enhance the performance without demanding for miniaturized transistors and/or devices with complex structures, such as self-aligned [15] or dual-gated devices [16], that would result in increased cost.

Ring Oscillators (RO) can be employed as on-chip clock generators. Emerging application areas of oxide TFTs like NFCs, wearable health monitoring systems and smart packaging require clock signals in Kilo-hertz to Mega-hertz range. Oxide TFT based ROs have been widely reported in literature [17]–[24] with frequency ranging in hundreds-thousands of kHz. These designs typically rely on high supply voltages (V_{DD}) ($\geq$15 V) [17]–[23], small channel lengths ($<10\,\mu$m) [18], [20], [22], [23], double gate structures [19], [22], [23], unstable oxide semiconductors (e.g., IZO rather than IGZO) [24] or on a combination of these. ROs working at low supply voltages ($\leq$4 V), have been reported in [25], [26]. The RO reported in [25] employs pseudo-CMOS inverter, which requires two supply voltage sources to obtain rail-to-rail operation. Besides, it employs self-aligned structures to obtain high operating frequency. On the other hand, RO reported in [26] employs MESFETs

and schottky diodes, which requires a negative supply voltage source in addition to the positive supply source and its fabrication requires higher number of processing steps. The low-cost solution would be to address the technology limitation for better performance through circuit design techniques without changing the device structure, materials or fabrication processing steps, and additional supply voltage source. Fulfilling these premises, this work proposes a high speed RO, where high frequency of oscillation is obtained at low V_{DD} by reducing the delay of an inverter stage using intermediate signals generated within RO. Therefore, it can be an optimal choice for on-chip clock generator even in low-voltage applications.

The rest of the paper is organized as follows: Section II gives an overview of the device fabrication and its measured characteristics; Section III describes the high speed RO design; measured results and discussions are presented in Section IV. Finally, conclusions are drawn in Section V.

II. DEVICE FABRICATION AND CHARACTERISTICS

The oxide TFT-based circuits are deposited on glass following the fabrication process described in [27]. In brief, the transistors have a staggered bottom-gate, top contact structure, shown as an inset in Fig. 1(a). The TFTs are based on sputtered materials, including Mo electrodes, a multilayer high-k gate dielectric based on Ta_2O_5 and SiO_2 and a-IGZO semiconductor (In:Ga:Zn 2:1:1 atomic composition). Circuit interconnects are done through an additional Mo level on top of the TFT stack, using a low-k Parylene-C interlevel insulator to minimize parasitic capacitance. The Parylene-C layer is deposited by chemical vapor deposition and also passivates the TFTs. All the layers are defined and patterned using optical lithography and etching processes. Final circuits are annealed at 180 °C for 1 hour on a hot plate.

Linear transfer and output characteristics of a-IGZO TFT with width and length of 40μm and 10μm, respectively, are shown in Fig. 1. The devices exhibit a turn-on voltage close to 0 V, an On-Off ratio exceeding 10^8 and a saturation mobility of 25.7 cm^2/Vs.

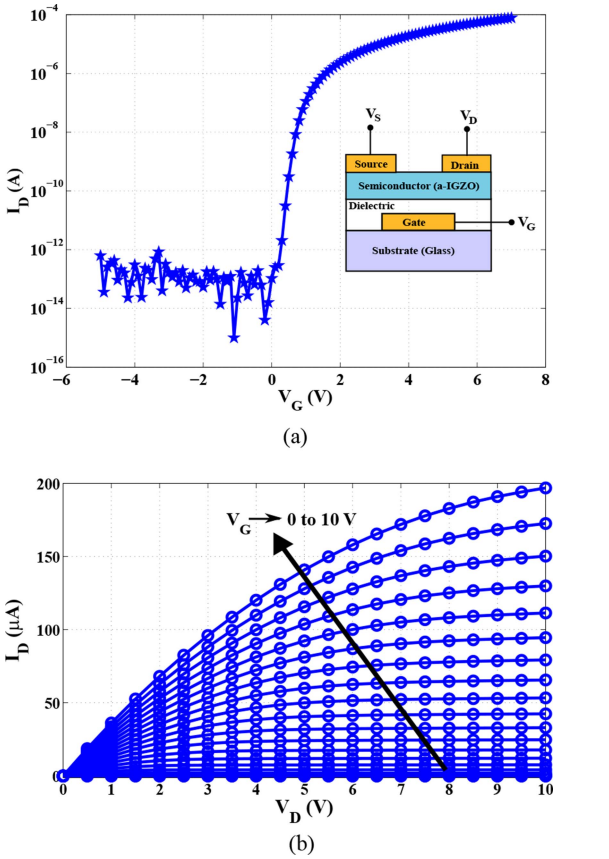

FIGURE 1. Measured characteristics of IGZO TFT with width = 40 μm and length = 10 μm (a) Linear transfer characteristics with drain voltage, V_D = 0.1 V. Device cross-sectional schematic is shown in the inset, and (b) Output characteristics when gate voltage linearly swept from 0 to 10 V with step size of 0.5 V.

III. HIGH-SPEED RING OSCILLATOR DESIGN

The schematic of i^{th}-stage inverter employed in a conventional bootstrapped pseudo-CMOS inverter based RO is shown in Fig. 2(a). Here, i varies from 1 to n for a n-stage RO. However, for $i = 1$, the input comes from the output of n^{th}-stage. In bootstrapped pseudo-CMOS inverter, operation of $M2$ is controlled by a diode-load inverter, whose propagation delay is defined as t_d (see Fig. 2(a)). Therefore, signal at node b is delayed by t_d compared to signal at node a, which increases the overall delay of the inverter stage. Since the frequency of oscillation of the RO is inversely proportional to the propagation delay of a single stage inverter in the RO [28], t_d imposes limitations on its operating frequency.

In order to compensate t_d, the high-speed RO employs bootstrapped pseudo-CMOS inverter stage, which is modified as shown in Fig. 2(b). Here, the gate of $M1$ and $M4$ are separated from each other. The gate of $M1$ (node y) is connected to the output of $(i-1)$-stage inverter, like in the conventional RO. It should be noted that the input to the gate of $M1$ and $M4$ should have nearly the same phase for proper operation. In addition, arrival time of the signal and

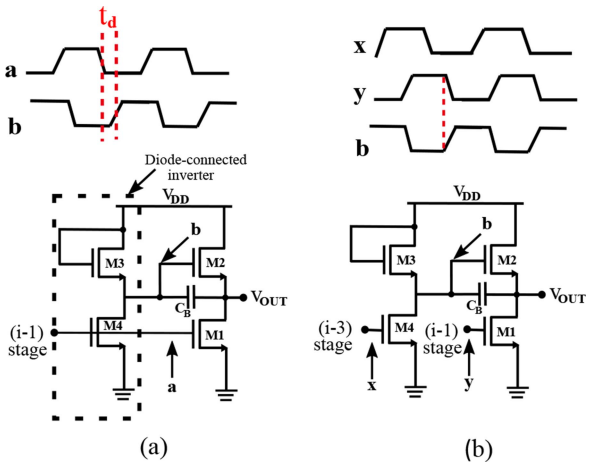

FIGURE 2. Schematic presenting i^{th}-stage inverter of (a) conventional bootstrapped pseudo-CMOS inverter based RO (b) High-speed RO.

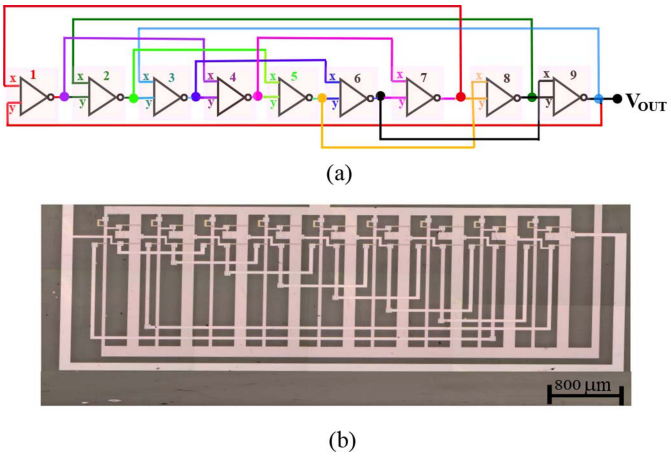

FIGURE 3. Proposed 9-stage RO based on a modified bootstrapped pseudo-CMOS inverter stage (a) Schematic (b) Micro-graph.

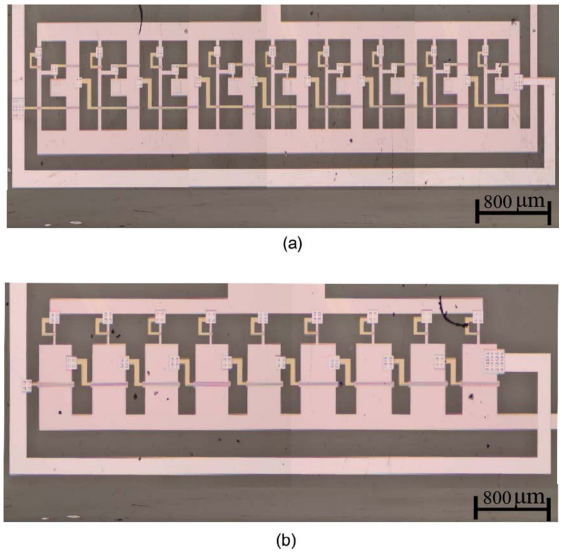

FIGURE 4. Micro-graph of conventional 9-stage ROs (a) with bootstrapped pseudo-CMOS inverters (RO1) and (b) with diode-load load inverters (RO2).

its inverted form at node y and b, respectively, should be the same. Therefore, the gate of $M4$ is connected to the output of $(i-3)$-stage (if $i > 3$, else $(n-(i-3))$-stage) inverter of a n-stage RO. As a result, signal at the gate of $M4$ arrives earlier than that of $M1$, which ensures almost simultaneous arrival of signals at nodes b and y. Therefore, t_d in Fig. 2(a) will be compensated, hence, improving the frequency of oscillations. However, unlike in Fig. 2(a), the diode-load inverter in Fig. 2(b) turns ON before $M1$ and $M2$ are actually operated and hence, consumes slightly more power. Therefore, the proposed RO ensures improved frequency of operation with a slight increment in the power consumption compared to the conventional RO. The schematic and micrograph of a 9-stage proposed RO is shown in Fig. 3. Two conventional (conv.) 9-stage ROs, with bootstrapped pseudo-CMOS inverter (RO1) and diode-load inverter (RO2), were also fabricated along-with proposed 9-stage RO under same conditions, in order to have a fair comparison from measurements. Micro-graphs of conventional ROs are presented in Fig. 4(a)-(b).

IV. RESULTS AND DISCUSSIONS

The voltage transfer characteristics (VTC) of the inverters employed in the ROs were measured using the probe station. The characteristic had been obtained by linearly sweeping the input voltage of the inverter (V_{IN}) from -5 V to 6 V in a step size of 0.1 V. The measured characteristic plot is shown in Fig. 5(a). The plot shows almost rail-to-rail operation for bootstrapped pseudo-CMOS inverter compared to diode-load inverter.

The measurements of ROs were performed at different values of V_{DD} 3, 6 and 9 V under normal ambient using Keysight DSOX2002A, as shown in Fig. 5(b). These ROs employ TFTs with a channel length of 10 μm. From the measurements, frequency of oscillations of RO1, RO2 and proposed RO were observed to be 120 kHz, 68 kHz and 173.2 kHz, respectively, at 6 V supply voltage. It can be noticed that the proposed RO has shown nearly 44% (155%)

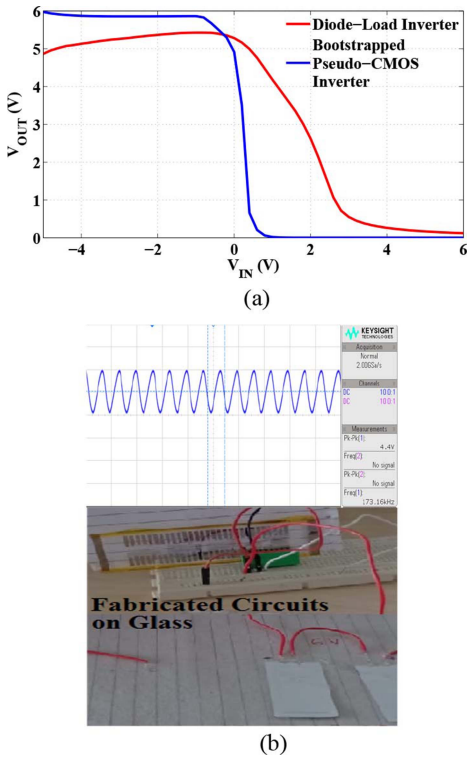

FIGURE 5. (a) Measured VTC of the inverters employed in ROs at V_{DD} = 6V, and (b) Measurement setup showing measured response of the proposed RO at 6 V.

increase in frequency of oscillation by consuming approximately 15% (113%) more power compared to RO1 (RO2). The performance of all the three ROs are compared from experimental characterization, at different supply voltages (V_{DD}) and the plots are shown in Fig. 6(a)-(d). It can be observed from the plot that the proposed RO provides highest

TABLE 1. Performance comparison of the proposed ro with state of the art work.

ROs	Stages	Channel length (μm)	Frequency (kHz)	Supply Voltage (V)	Voltage Swing* (% of supply voltage)	Device Structure & Semiconductor Composition	Employs on-chip output buffer?
[17]	11	11	94.8	20	50	Standard a-IGZO	yes
[18]	11	9	47	15	60	Standard a-IGZO	yes
[19]	11	10	781	20	30	Dual-gate a-IGZO	yes
[20]	11	9	810	25	48.6	Standard a-IGZO	-
[21]	5	10	2100	25	0.5	Standard a-IGZO	no
[22]	7	6	6510	20	3	Dual-gate a-IGZO	yes
[23]	13	6	360	20	100	Dual-gate a-IGZO	yes
[24]	11	10	132	5	96	Standard IZO	yes
This Work	9	10	173.2 @ 6 V | 305 @ 9 V	6	73	Standard a-IGZO	no

*Observed from results reported in the literature.

frequency, lowest power-delay product (PDP) and per stage propagation delay compared to conventional ROs. However, the voltage swing of the proposed RO is inferior compared RO1. For a 6 V supply, the voltage swing of RO was observed to be 73% of supply voltage compared to 91% in RO1. It should be noted that the testing of the ROs have been performed without using any on-chip output buffers. As a result, the large load impedance offered by the DSO (digital storage oscilloscope) cables during measurements, can effect the performance of the ROs significantly. In order to study the effect of the load impedance on the swing of the proposed and other ROs, simulations were performed at a supply voltage of 6 V and the swing is plotted against different loading conditions (see Fig. 6(e)). From the plot it can be observed that under no load condition, RO1 and the proposed RO deliver 100% output voltage swing. However, as the load impedance increases, the voltage swing of the proposed RO degrades more significantly compared to RO1 because the output node of the proposed RO acts as an input to two intermediate stages within the RO (compared to one in RO1). Therefore, the output swing of such stages will also degrade and this degradation in voltage swing propagates through all the stages of the RO, thus, degrading the final output voltage swing. However, by taking into account on-chip output buffers similar to the ones that are used in the literature [17]–[19], [22]–[24], almost a complete output voltage swing and higher frequency of oscillations can be achieved from the proposed RO for a given technology.

Next, the performance of the proposed RO is compared with other ROs reported in the literature. It can be observed from the Table I that ROs reported in [17]–[22] have used higher supply voltages ($\geq$10 V) with the voltage swing not exceeding 60% of V_{DD}. In addition, the RO reported in [23] employs dual-gate TFTs, which requires additional fabrication processing steps. On the other hand, the TFTs employed in [24] have a mobility 40% higher than the mobility of TFTs employed in this work. The RO reported in [28] is limited to simulation results and does not account for the parasitic associated with interconnects. Therefore, compared to state of the art work, the proposed RO has shown a considerable improvement in frequency of oscillations with standard device structure and at low-supply voltages without imposing limitation on fabrication process. In addition, the proposed

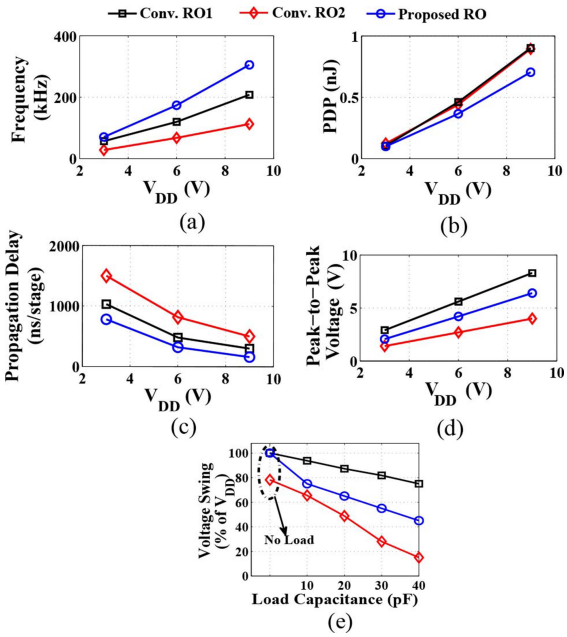

FIGURE 6. Performance comparison of conventional and proposed ROs as a function of V_{DD} (a) Frequency (b) PDP (c) Propagation Delay (d) Peak-to-peak Voltage, and (e) Simulation results showing the effect of load capacitance on the voltage swing of the ROs.

RO can deliver a full output voltage swing if on-chip output buffers are employed in the circuits as discussed previously.

V. CONCLUSION

This work presents a high-speed RO with a-IGZO TFTs at low-supply voltage. The proposed circuit has shown an improvement in the output frequency of 44% and 155%, and reduction of 24.5% and 14% in the power-delay product compared to RO1 and RO2, respectively, from measurements at a V_{DD} of 6 V. Therefore, the proposed RO can be employed in many low-cost applications including smart packaging, biomedical wearable devices, NFC and RFIDs, without requiring miniaturized and/or complex transistor structures.

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