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LPDDR3 Design Considerations

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Introduction

- This section discusses practical advice on how to construct the memory subsystem of an SoC around LPDDR3

Low power memory

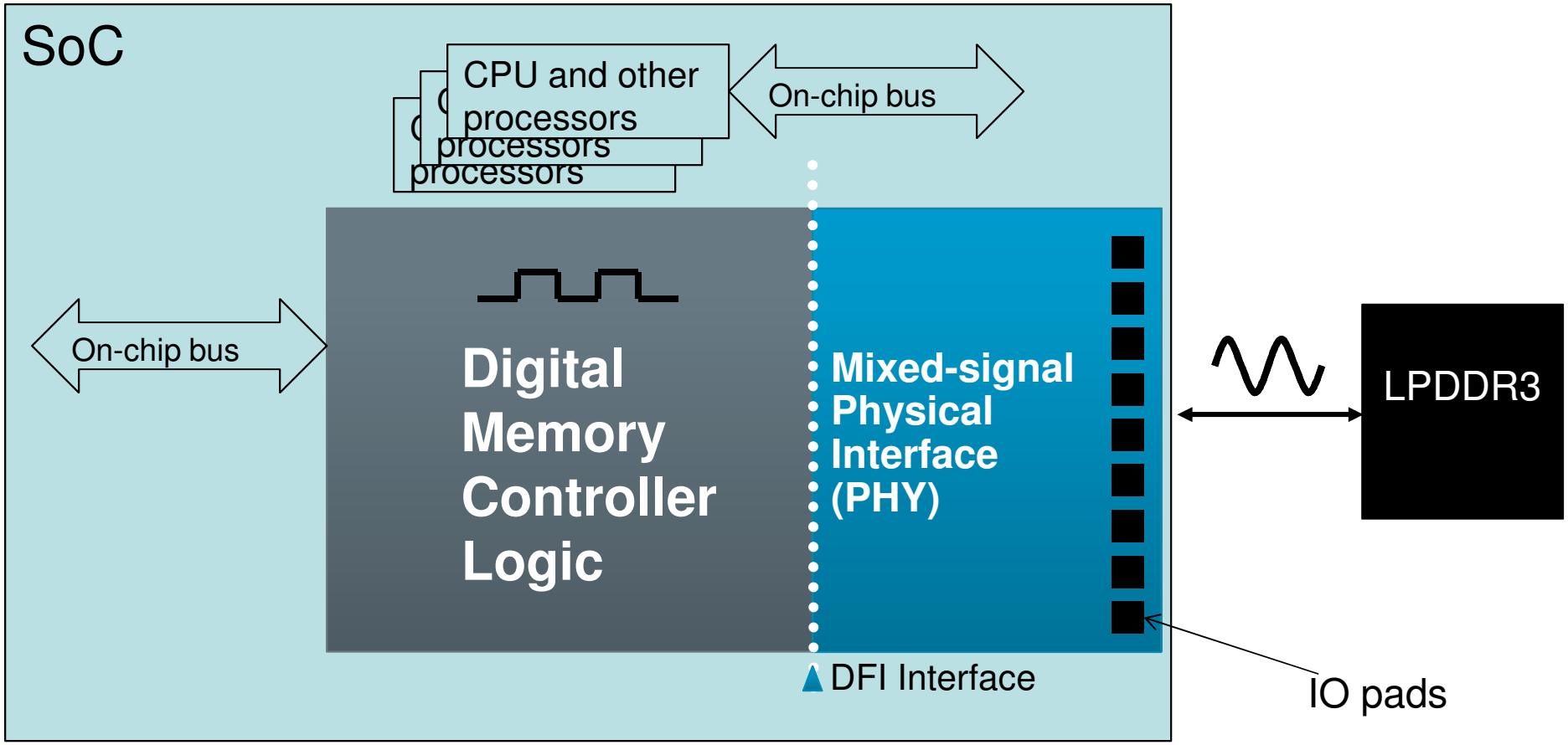
- Never bet against user demand for:
  - Less Cost
  - More Bandwidth
  - Less Power
  - More Capacity

… and a memory that works better when it's hot

Terminology

- SoC: System-on-Chip containing CPU and other processing elements
- Memory Controller: Digital Logic between on-chip bus and DFI
- PHY: Mixed-signal logic between DFI and IO pads
- DFI: Standard for connection of memory controller and PHY

What is a Memory Controller and PHY?



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DFI 3.1 upgrades over DFI 3.0

- DFI 3.1 added support for LPDDR3
- Write Leveling (not present in LPDDR2)
- CA Training (seen previously in GDDR5)
- New training handshake for PHY independent mode
- Low Power Control interface enhancements
- Dfi_lvl_pattern added

Transitioning from DDR3

- Many new/different mode registers
- Mode Register Read
- DDR CA Bus
- Low capacitance
- Optional Per-Bank Refresh
- Termination on CA bus?
- Training reused from DDR3

Per-Bank Refresh

- JESD209-3 Refresh Cycle Times:
  - tRFCab = 210ns for 8Gb die
    - All bank: whole DRAM is offline
    - Opportunity to do internal PHY operations
    - Likely to build a backlog of commands
  - tRFCpb = 90ns for 8Gb die
    - Per bank: one bank is offline
    - Issue command 8x more often
    - Less likely to build a backlog

Transitioning from LPDDR2

- Termination
- Training
- Reduced Capacitance
- 8n Prefetch
- 8 Banks

PHY transition

- Transition from DDR3 PHY
  - Less Power
  - Accurate Impedance Matching
- Transition from LPDDR2 PHY
  - Higher Speed
  - Less Capacitance
  - Training
  - Termination

Training Overview

- MRR0 allowed before CA training
  - But don't try it at speed…
- Train CA bus
- Send ZQ Calibration Command
- DQ Calibration
- Write Leveling

CA Training

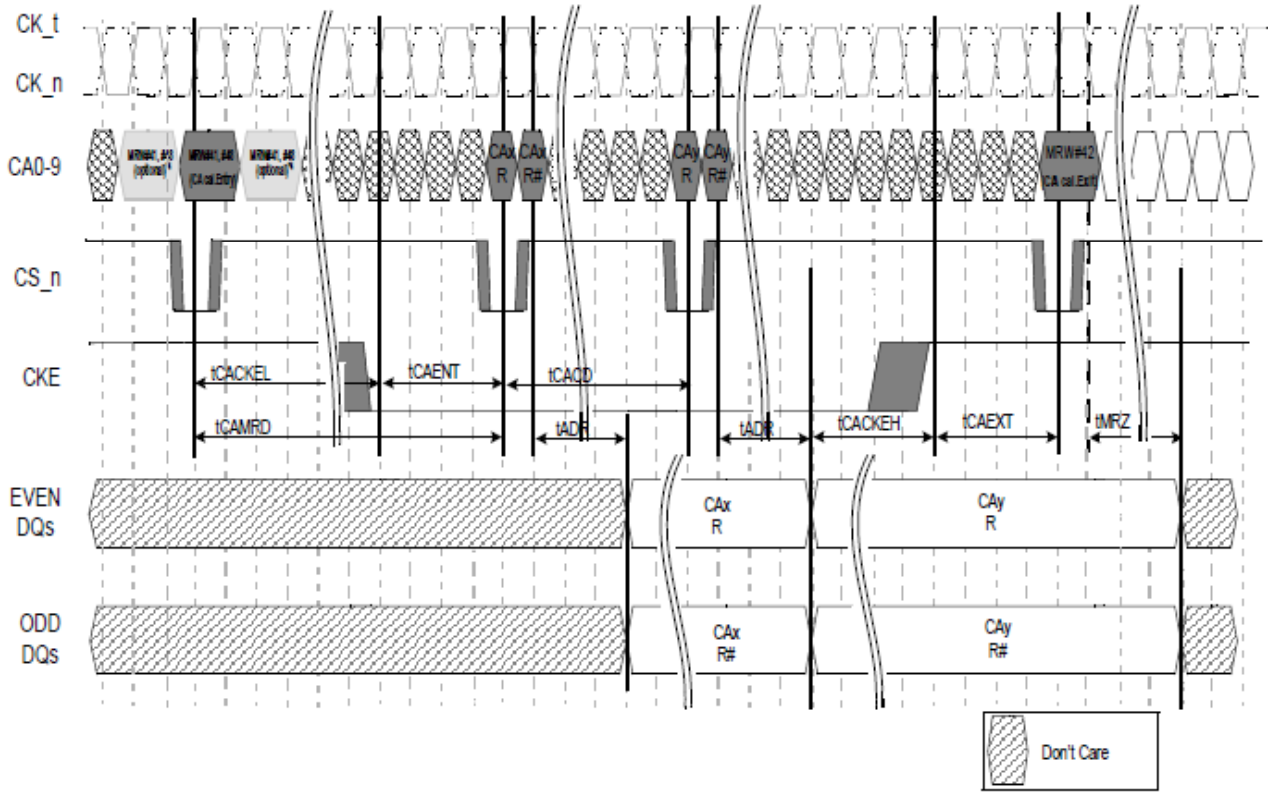
- Aligns CA to CLK
- Both Edges
- Per Bit Allowed / Recommended
- Enter/Exit CA training mode with MRW command
  - Specially selected MRW commands are more tolerant to CA mismatch
- Future: 2 cycle CS pulse?

CA Training Sequence

- Note CA Training Sequence in JESD209-3 4.11.3.1
  - There are 10 CA pins (20 edges) to train but only 16 DQs to do it with
  - Need additional training sequence to train CA4 and CA9

CA Training from JESD209-3

Figure 45 — CA Training Timing chart



ZQ Calibration

- Calibrates output impedance – leads to signal integrity
- Periodic retraining
- Consider AOAC devices and ZQ Long after self-refresh
  - Temperature Sensitivity and drift
  - Voltage sensitivity and drift

ZQ Cal Equation from JESD209-3

LPDDR3 devices are subject to temperature drift rate ($T_{driftrate}$) and voltage drift rate ($V_{driftrate}$) in various applications. To accommodate drift rates and calculate the necessary interval between ZQCS commands, apply the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)} = CalibrationInterval$$

Where T_{sens} = MAX ($dR_{ON}dT$) and V_{sens} = MAX ($dR_{ON}dV$) define temperature and voltage sensitivities.

For example, if T_{sens} = 0.75%/°C, V_{sens} = 0.20%/mV, $T_{driftrate}$ = 1°C/sec, and $V_{driftrate}$ = 15mV/sec, then the interval between ZQCS commands is calculated as:

$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

tDQSCK

- tDQSCK is the skew between the DQS (strobe) and CLK
  - First DQS transition indicates location of first data transition
  - Already an issue in LPDDR2
- tDQSCK is now multicycle
  - Greater variability than DDR
  - Where is your data???
- Need to manage across byte lanes

tDQSCK – From JESD209-3

Figure 8 — Burst Read: RL = 12, BL = 8, $t_{DQSCK} > t_{CK}$

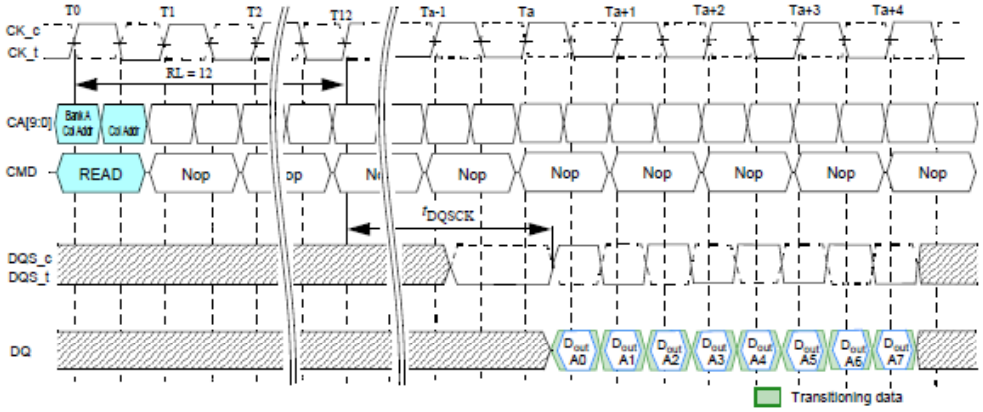
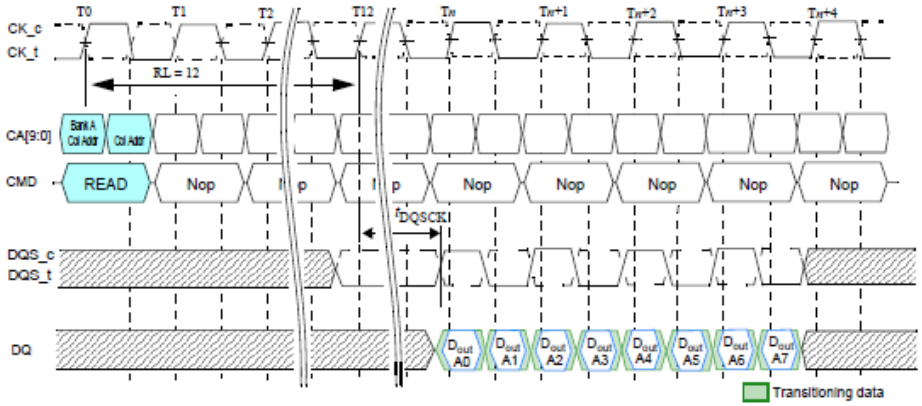
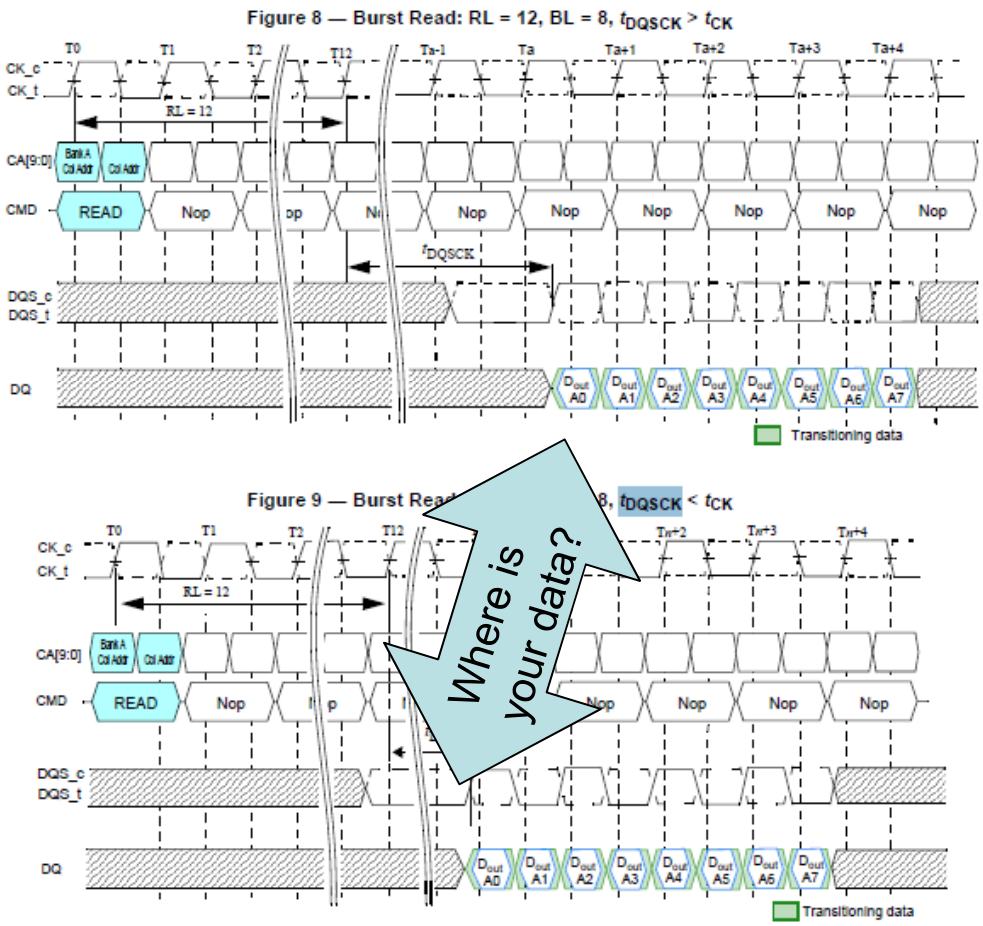


Figure 9 — Burst Read: RL = 12, BL = 8, $t_{DQSCK} < t_{CK}$



tDQSCK – From JESD209-3



tDQSCK is 2500ps – 5500ps per JESD209-3

tCK is 1250ps at DDR1600

First rising edge of DQS can arrive between 2 and 4.4 clocks after RL elapses (practically, 2, 3, or 4 clocks)

Need DQ Calibration to determine where it arrives

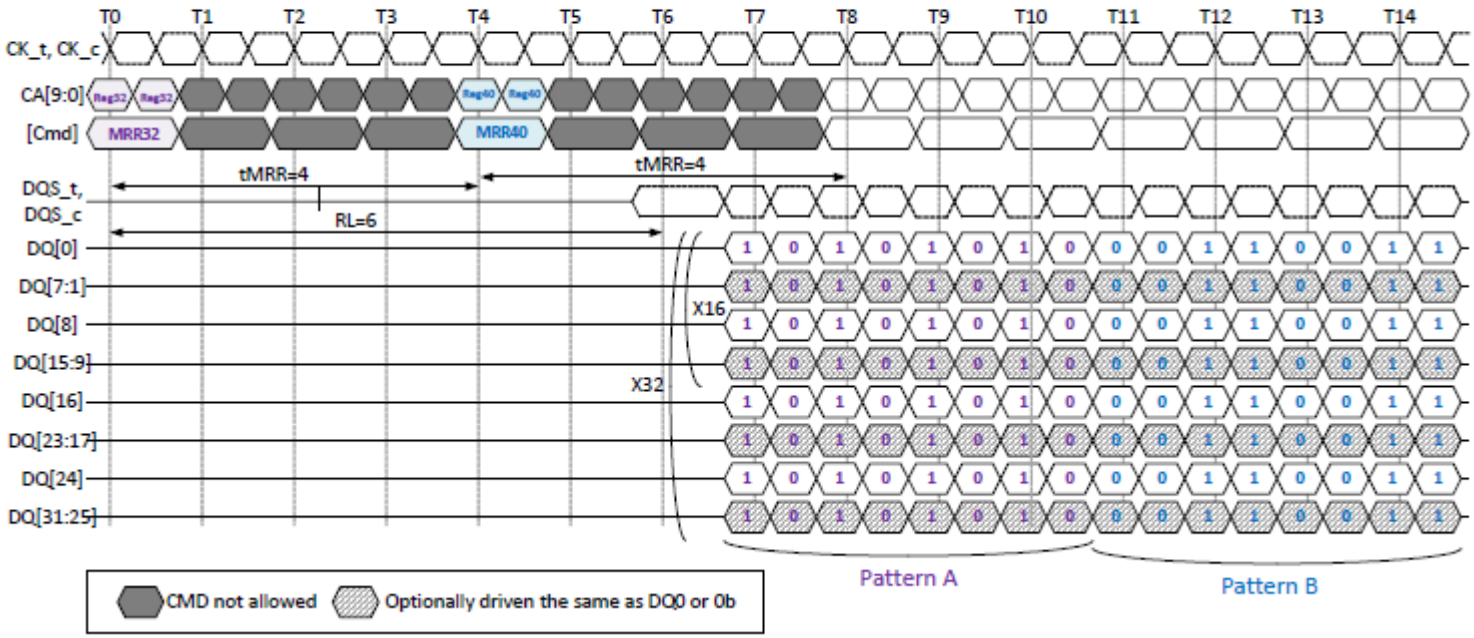
tDQSCK delta parameters describe drift in tDQSCK

DQ Calibration (Read training) – System Level

- DQ Calibration algorithm reused from LPDDR2
- Data **optionally** returned per bit
  - Training data can appear on select bits or all bits. Should your system require per bit?
  - Remind package/PCB designers that DQ0,DQ8,DQ16,DQ24 are significant
- Decide if CPU, MemCtl, or PHY levels
- Can use DRAM for custom algorithms

DQ Calibration from JESD209-3

Figure 39 — DQ Calibration Timing

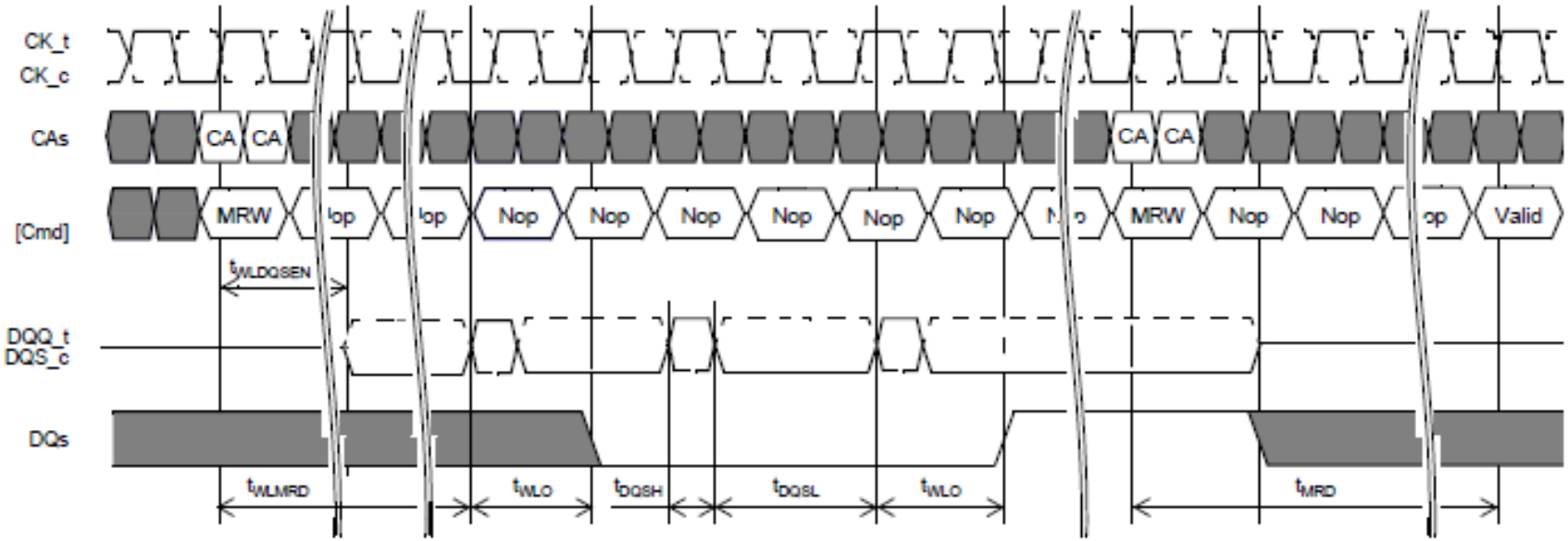


Write Leveling – System level

- Aligns Write DQS to CLK
- DFI mode can assist with leveling
- Enter with MRW
- Send DQSs – DRAM responds with DQ to indicate if DQS is received before or after CLK
- How Often? When to train?
- Where to train: CPU, Controller or PHY?

Write Leveling from JESD209-3

Figure 46 — Write Leveling Timing



ODT – System Level

- 2 Rank Package:
  - Always terminate on Rank 0
  - Cannot have Rank 0 in self-refresh while accessing Rank 1
- Single Rank
  - Can pull ODT high
  - Must use MRR to disable ODT for ZQ Calibration

CMD-CMD Timing in LPDDR3

Parameter	LPDDR3	LPDDR2
Read Latency	3-12	3-8
Write Latency	1-6, 1-9 opt	1-4
tWR min	Up to 12 nCK	Up to 8 nCK
tRP min	Up to 22 nCK	Up to 13 nCK
tRC min	Up to 53 nCK	Up to 36 nCK
tRAS min	Up to 34 nCK	Up to 23 nCK
tCCD min	4 clocks	2 Clocks
tFAW min	Up to 40 nCK	Up to 27nCK

Don’t forget to plan for future expansion…

8n Prefetch in LPDDR3

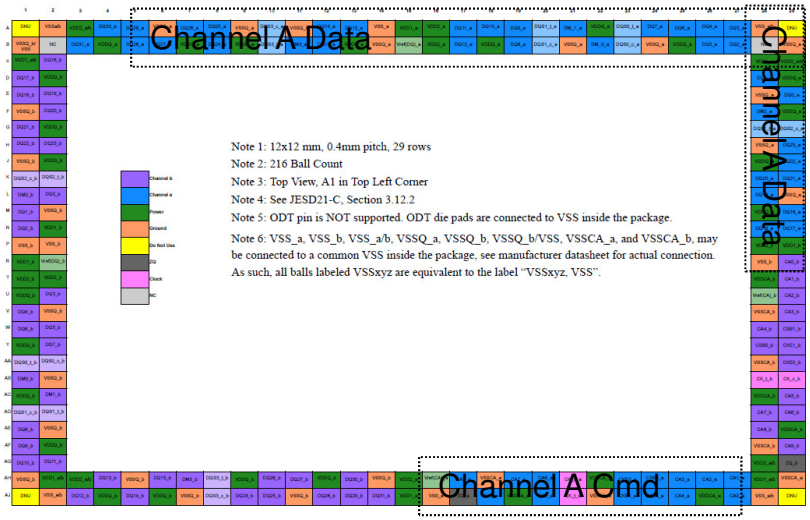
- LPDDR2 has 4n Prefetch
  - Burst lengths 4, 8, 16 supported
- LPDDR3 has 8n Prefetch
  - Burst length 8 only and no BST/Interrupt
  - Minimum 32 Byte burst on X32 DRAM
- System-level effect:
  - OK for most CPUs
  - Consider video and network traffic

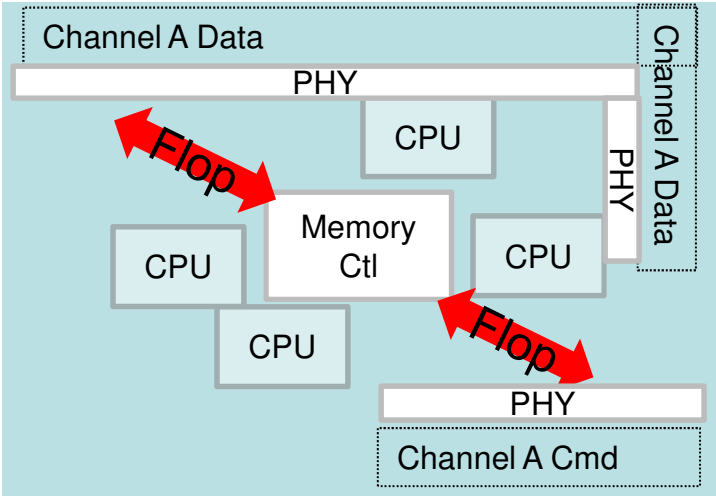
Chip Construction

- Need to plan for CA bus being on opposite edge from the data bus
- Two possible methods:
  - Place Memory Controller centrally and flop long paths on chip if necessary
  - Place Memory Controller at edge and route using package layers

Central Memory Controller placement

- Align pads with LPDDR3 ballout
- Flop long paths internally
  - Adds latency

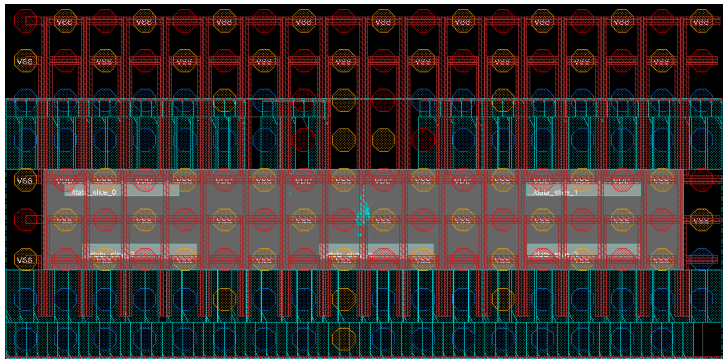


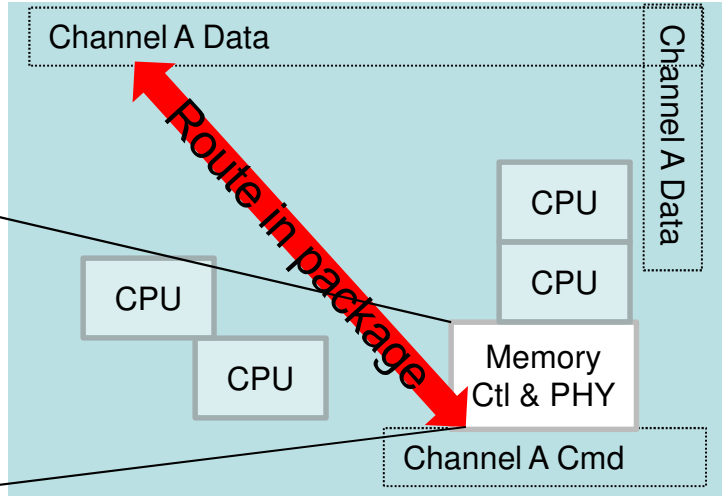


Note: Only one channel shown. Not to scale.

Edge Memory Controller placement

- Produce compact layout for memory controller & PHY
- Route long paths in package layers





Note: Only one channel shown

Conclusions

- LPDDR3 requires many changes from DDR3 or LPDDR2
- Remember Training, ODT, and Capacitance
- Consider Design IP for your next project

About Cadence

- Cadence Memory Solutions include:
  - LPDDR3/LPDDR2/DDR4/DDR3 Controller and PHY
  - Wide-IO Controller and PHY
  - Flash Controller and PHY
  - Memory Models
  - Verification IP
  - Signal Integrity Reference Designs
  - Design, Verification, Physical Verification, and Test tools for
    TSV-based chip designs