Semiconductor Fabrication and Layout Design Rules

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Lecture Objectives

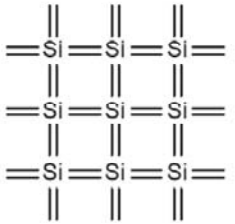
- To have a basic understanding of the semiconductor fabrication process so as to understand
  - Layout design rules
  - Process variation
- Ultimate objectives
  - To understand what you are designing
  - To accomplish better and higher yield design
  - To understand upcoming design challenges caused by fab
- Textbook Reference
  - Chapter 2
- Other References
  - MOSIS TSMC 180nm node design rule files
  - http://www.mosis.org/products/fab/vendors/tsmc/tsmc018/
  - http://www.mosis.org/Technical/Designrules/scmos/scmos-main.html

Today's Topics

- Review of semiconductor physics and devices
- Basic fabrication process
- CMOS fabrication
- Layout design rules
- Process variation and yield
- Manufacturing cost
- Summary

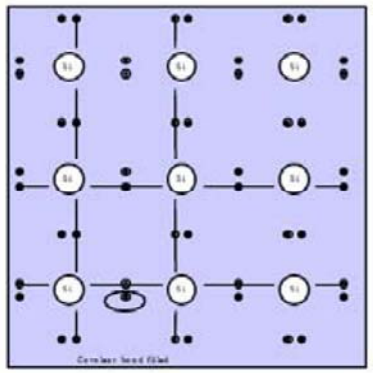
Silicon Lattice

- Transistors are built on a silicon substrate
- Silicon is a group IV material
- Forms crystal lattice with bonds to four neighbours



Silicon Structure

- Pure atoms of silicon
  - An atom of silicon has 4 valence electrons in its outer shell
  - When it forms a solid, the atoms arrange themselves into a crystal structure and share their 4 outer electrons
  - Outer shell of silicon is stable with 8 electrons



Charge Carriers

- There are two types of charge carriers in a semiconductor
  - Free electrons
  - Postive holes
- A free electron is one which breaks away from its covalent bond, it has a charge of –q
- A hole is what is left over after an electron has left, it has a charge of +q
  - A hole is easily filled by a nearby electron, hence holes, like electrons “move” in the crystal

Doping Semiconductors

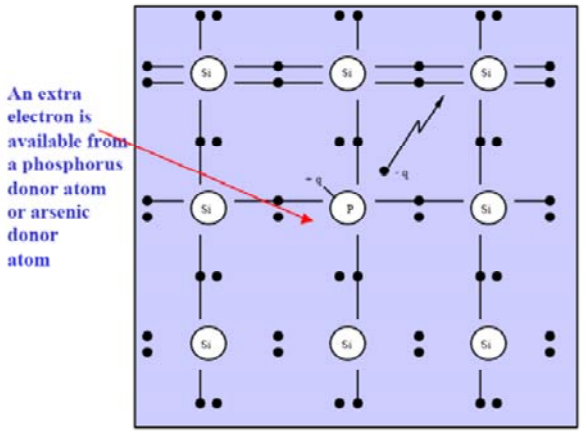
- In pure semiconductors, the number of holes is the same as the number of electrons ($n_i = 10^{10}/cm^3$) at room temperature;
  - Hence, the conductive properties of a semiconductor can be improved if small amounts of specific impurities are introduced into the crystal (called *doping*)

    $(np=n_i^2)$
  - If the dopand has 5 valence electrons, then the crystal will have extra electrons creating an n-type semiconductor

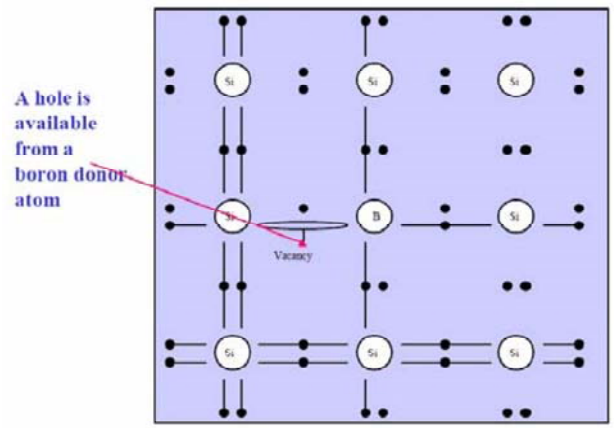
    $n = N_D$ Donor concentration
  - If the impurity has 3 covalent electrons then only 3 of the covalent bonds can be filled resulting in an extra hole (a p-type semiconductor)

    $p = N_A$ Acceptor concentration

n-type Material

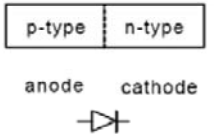


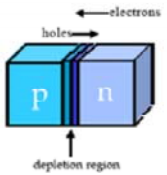
p-type Material

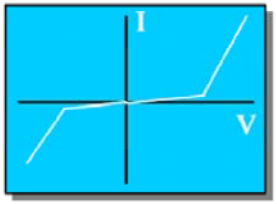


Silicon Property: p-n junctions

- A junction formed between a p-type and n-type semiconductor
  - A Diode
- Two Mechanisms (equilibrium state):
  - Diffusion (Concentration gradient)
  - Drift (Electric Field)
- Current flows onlv in one direction

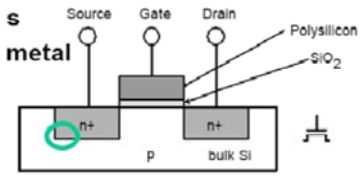






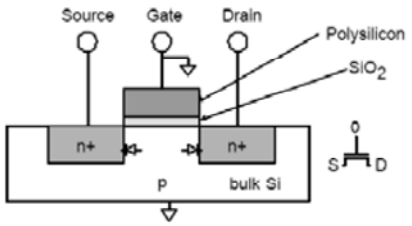
nMOS Transistor

- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - SiO_2 (oxide) is a very good insulator
  - Called metal – oxide – semiconductor (MOS) capacitor
    - Even though gate is no longer made of metal!



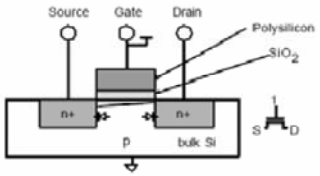
nMOS Operation: Off

- Body is commonly tied to ground (0V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



nMOS Operation: On

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON

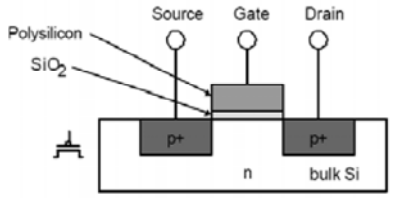


Threshold Voltage V_t:

- Doping level N_A
- Body bias

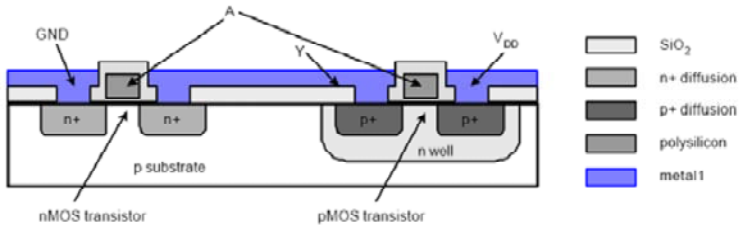
pMOS Transistor

- Similar, but doping and voltages are reversed
  - Body tied to high voltage (VDD)
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior



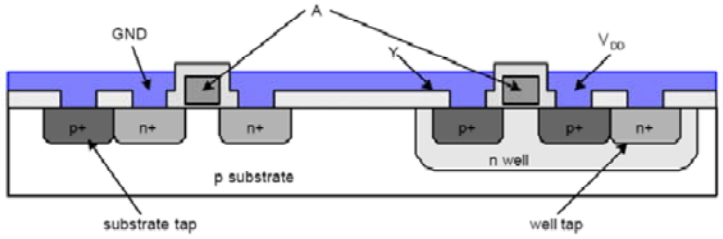
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors

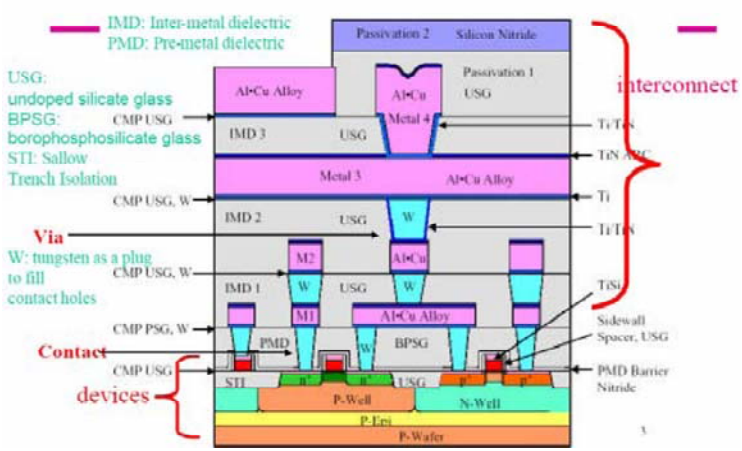


Well and Substrate Taps

- Substrate must be tied to GND and n-well to VDD
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts/taps



A 4-metal CMOS Twin-well Process



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- Process variation and yield
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Movie

- http://museum.toshiba.co.jp/01ubiquitous/sth_mv_semicon02.html

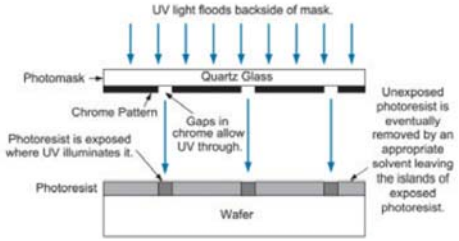
Basic Fabrication Process

- Crystal growing and wafer production
  - Circular ingots of pure silicon are sliced into 200mm or 300mm diameter wafers
- Oxidation
  - Silicon Dioxide (SiO2) is produced by heating the wafer to very high temperatures in the presence of oxygen
- Photolithography: Selective Regions for Doping
  - Circuit patterns are formed by masking and etching processes
- Doping: Well and Channel Formulation. After etching is completed, the exposed surfaces may be doped. Two main methods to add impurity
  - Deposition/Diffusion
  - Ion Implantation

Basic Fabrication Process

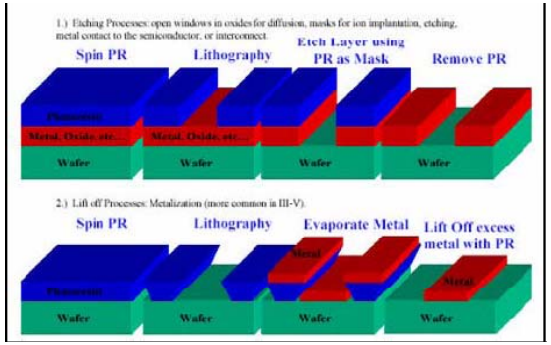
- Interlayer Dielectrics
  - Thin films of various materials (eg SiO2) are deposited on the wafer (*Deposition*). These layers may be planarised using Chemical Mechanical Polishing (CMP)
- Interconnect Creation
  - Conducting circuits are created between individual transistors and devices using techniques such as Chemical Vapor (e) Deposition (CVD), Evaporation
- Testing and Packaging
  - Individual microsystems are tested for quality and placed in protective packages that can later be connected to other devices

Photolithography



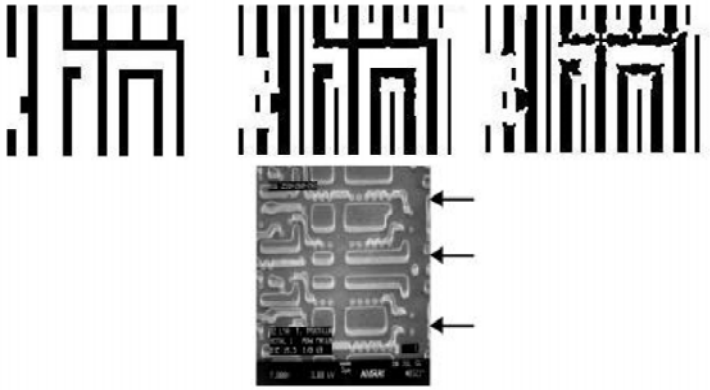
- **Photo Masking** shapes the different components. Resin (photoresist) is put down on the wafer and then exposed to light through a specific mask.
  - Photoresist is a light-sensitive organic polymer
  - Positive photoresist Softens where exposed to light
  - Negative photoresist Hardens where exposed to light

Use of Lithography



- **Etching** process - create the circuit pattern that has been defined during the photomasking process. For instance: the poly gates of a transistor, the aluminum connections.

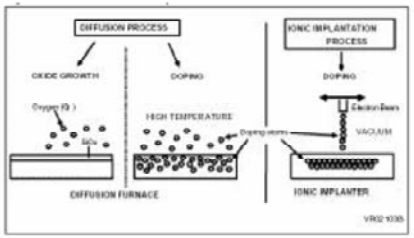
What can go wrong



Challenges with nm Process

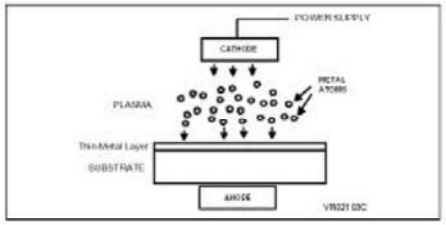
- Challenge 1:
  - The wavelength of the light source influence the minimum feature size that can be printed. Comparable or greater than the feature size cause distortion in the patterns exposed on the photoresist.
- Resolution enhancement techniques (pre-compensate for the amplitude, phase and direction of the incoming lights)
  - Optical proximity correction (OPC): small changes to the mask patterns to compensate local distortion
- Phase shift masks (PSM): vary the thickness of the mask to change the phase such that light from adjacent lines are out of phase and cancel where no light is desired
- Unresolved Challenge: masks too expensive.

Diffusion and Ion Implantation



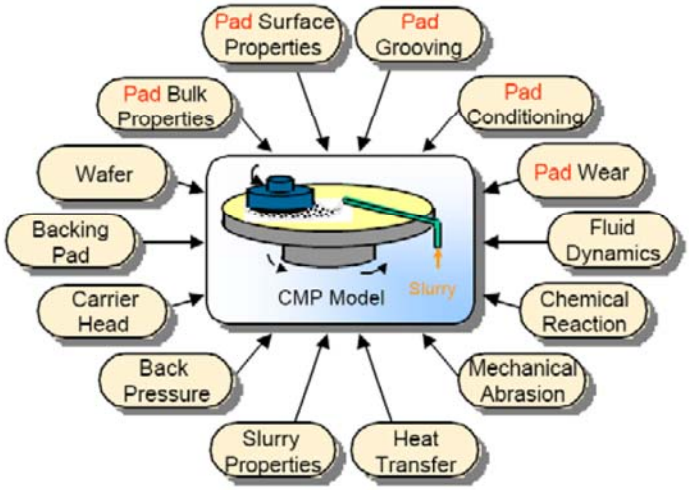
- Diffusion is used to introduce dopants inside the material or to grow a thin oxide layer onto the wafer. Wafers are inserted into a high temperature furnace (up to 1200º C) and doping species penetrate the silicon or gas phase species react with it to grow a silicon oxide layer.
- Ion Implantation allows the introduction of a dopant at a given depth into the material using a high energy ion beam.

Metal Deposition



- **Metal deposition** is used to put down a metal layer on the wafer surface. There are two ways to do that. The process shown on the graph below is called **sputtering**. It consists first in creating a plasma with argon ions. These ions bombard the target surface (composed of a metal, i.e. aluminium) and eject metal atoms from the target. The sputtered atoms are projected in all the directions and a fraction of them condense on the substrate surface.

Chemical Mechanical Polishing (Planarization)



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CMOS Fabrication

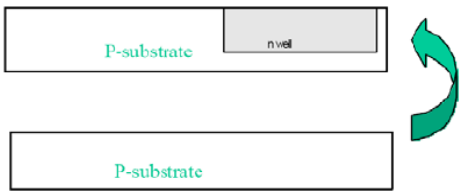
- CMOS: "Complementary" means using both n-type and p-type devices on the same chip
- Two main technologies:
  - P-Well
    - Substrate is N-Type. N-Channel device built in P-Type well within the parent N-Type substrate. P-channel device built directly on the substrate.
  - N-Well
    - Substrate is P-Type. N-channel device built directly on the substrate. P-channel device built into N-type well within the parent P-Type substrate.
- Two advanced technologies:
  - Becoming more popular for sub-micron geometries where device performance and density is pushed beyond limits of conventional p & n-well CMOS processes
  - Twin Tub
    - Both an N-Well and a P-Well are manufactured on a lightly doped N-type substrate.
  - Silicon-on-Insulator (SOI) CMOS Process
    - Allows creation of independent, completely isolated nMOS and pMOS transistors on an insulating substrate.

N-Well CMOS Fabrication Steps

- Start with blank wafer and build from the bottom up
  - Thin wafer cut from a single crystal of silicon of high purity
  - Wafers typically 75-150 mm in diameter, 0.4-1 mm thick
  - For p-type silicon, impurities (e.g. boron) introduced during crystal growth
  - Boron p-type doping concentrations of $10^{15}/cm^3$ - $10^{16}/cm^3$ gives resistivity in range 25 Ω-cm to 2 Ω-cm

Steps to form the N-well

- Cover wafer with protective layer of SiO_2 (oxide)
- Remove layer where n-well should be built
- Implant or diffuse n dopants into exposed wafer
- Strip off SiO_2



Oxidation

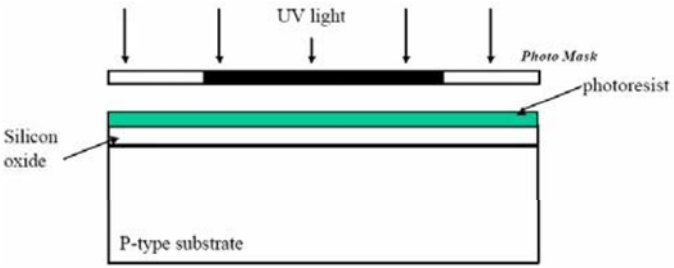
- Silicon dioxide (SiO_2) layer is grown over wafer surface
- typically 1μm thick
- 900 – 1200 ºC with H_2O or O_2 in oxidation furnace
- protects surface
- acts as barrier to dopants during remainder of processing
- provides insulating substrate onto which other layers may be
- deposited & patterned

Photoresist

- Photoresist is deposited onto surface of wafer (and spun to achieve an even distribution)

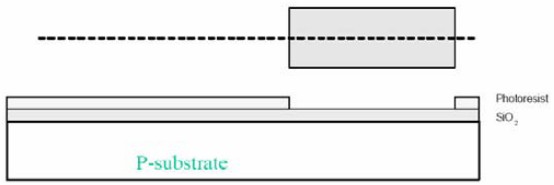
Masking

- Photoresist layer is exposed to UV light through mask
  - Defines regions where diffusion is to take place



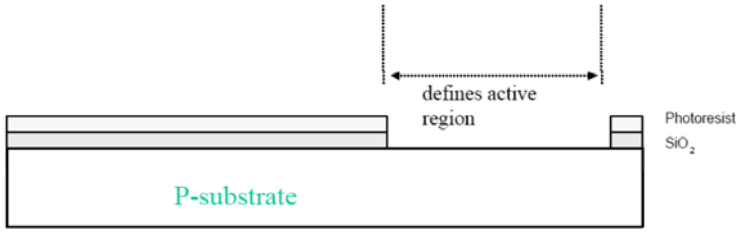
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



Etching

- The exposed oxide areas are etched away with hydrofluoric acid (HF) to expose the wafer surface in the window defined by the mask
  - HF seeps through skin and eats bone, nasty stuff!!
- Only attacks oxide where resist has been exposed

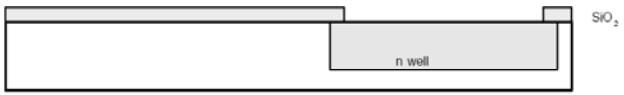


Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranha etch
- Necessary so resist doesn't melt in next step

N-Well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si



Strip Oxide

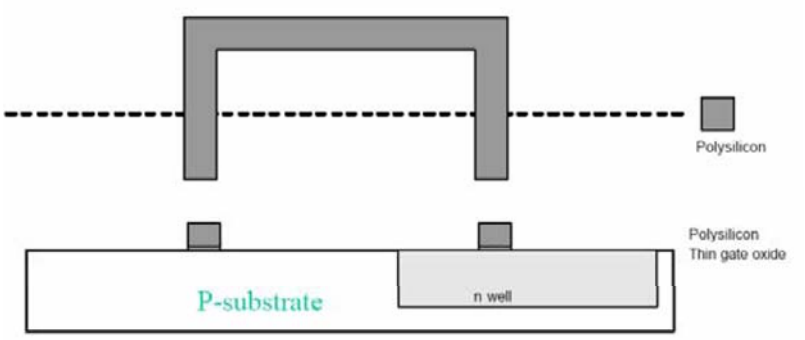
- Strip off the remaining oxide using hydrofluoric acid (HF)
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

Polysilicon Gate Deposition

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Heavily doped polysilicon deposited by Chemical Vapor Deposition (CVD)
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor

Polysilicon Gate Patterning

- Use same lithography process to pattern polysilicon

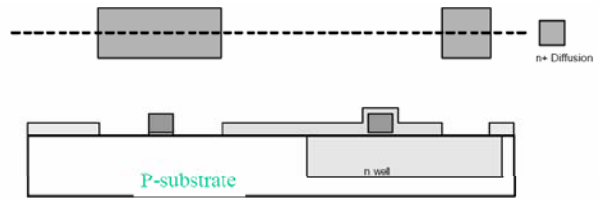


Form N-Diffusion

- Now consider how to form N-diffusion to make nMOS source, drain, and n-well contact
  - Use oxide and masking to expose where n+ dopants should be diffused or implanted
- First to oxide the entire region

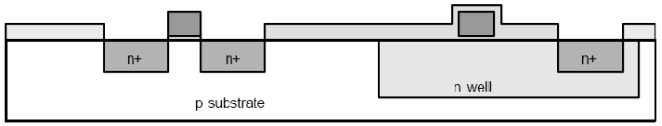
N-diffusion Formation

- Pattern oxide and form n+ regions
  - *Self-aligned process* where gate blocks diffusion
    - This is a major enabling feature of CMOS processing
  - Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



N-diffusion Formation: Doping

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion

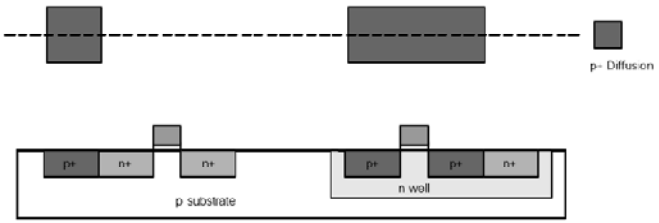


N-diffusion Formation: Etching

- Strip off oxide to complete patterning step

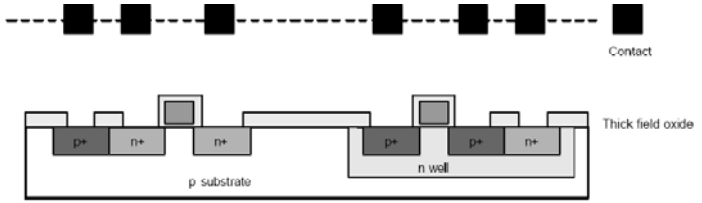
P-diffusion Formation

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



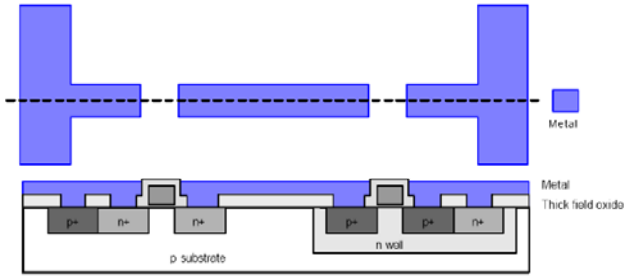
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed

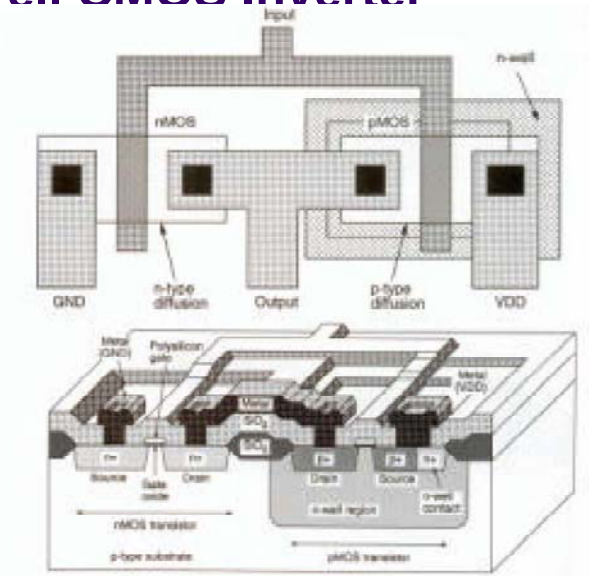


Metalization

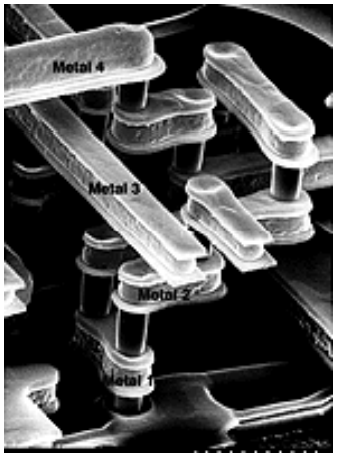
- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires



N-Well CMOS Inverter



Advanced Metalization



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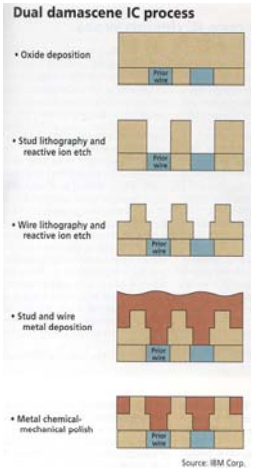
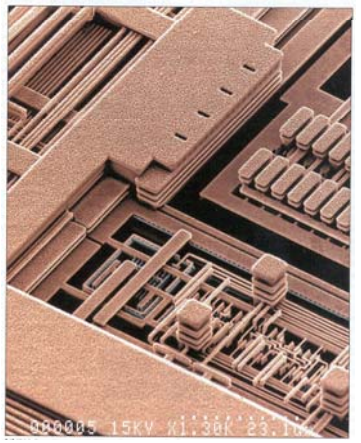
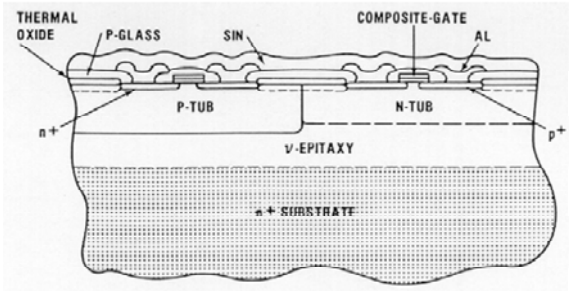




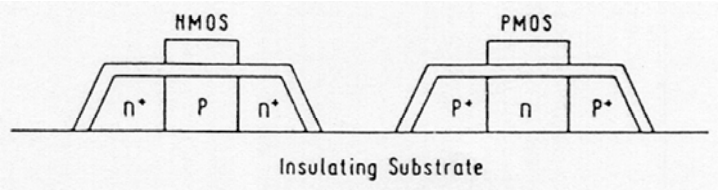
Twin-well CMOS Process

- Allows separate optimization of the nMOS and pMOS transistors
  - Independently tune threshold voltage, body effect, and channel transconductance
  - Independent doping steps -> doping concentrations can be carefully optimized
  - Typical p & n-well process, doping density of well is typically 1 order of magnitude higher than the substrate
- Starting material is n+ or p+ substrate, with a lightly doped epitaxial layer on top
  - Epitaxial layer provides substrate for n-well and p-well
- **More Costly to Fab!**



Silicon-on-Insulator (Sol) Process

- Use an insulating substrate
- Independent, completely isolated nMOS and pMOS transistors
- Main advantages of this technology
  - higher integration density (because of the absence of well regions)
  - complete avoidance of the latch-up problem
  - lower parasitic capacitances compared to the conventional p & n-well or twin-tub CMOS processes
- SOI CMOS process considerably more costly
  - Advantages may be justified, especially for deep-sub-micron

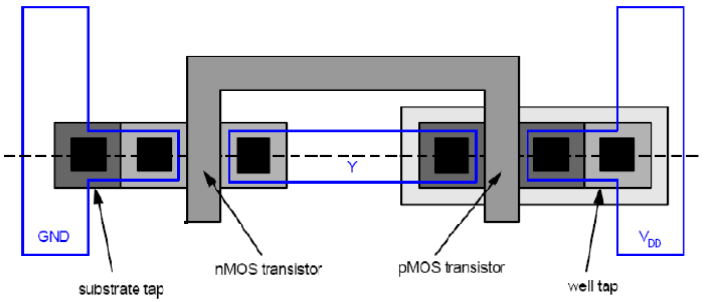


Today's Topics

- Review of semiconductor physics and devices
- Basic fabrication process
- CMOS fabrication
- Layout design rules
- Process variation and yield
- Manufacturing cost
- Summary

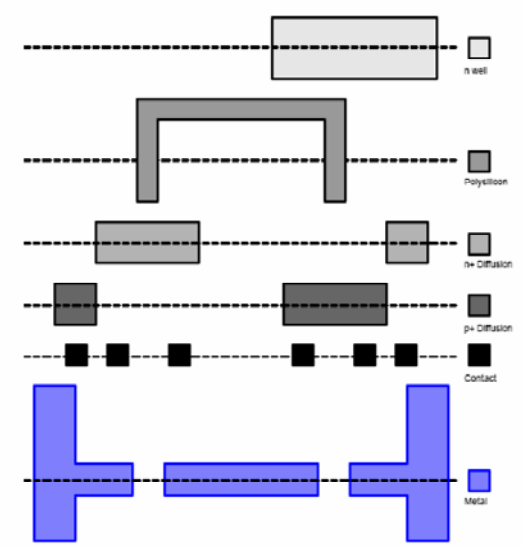
Summary of Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Detailed Mask View

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal



Layout

- Chips are specified with set of masks
  - This will be your design outcome: delivered to fab; so when an IC design is done, we say “tape out” (because we used to deliver the info via tape drive. Now we use FTP!)
- Feature size *f* = distance between source and drain
  - Set by minimum width of polysilicon
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size decreases 30% every 3 years or so
- Currently 180nm, 130nm dominating, industry-wise moving to 90nm, Intel and other leading 65nm

Design Rules

- Contract between you and foundry
  - Obey the design rules -> circuit will be fabbed properly
- Compromise
  - designer - tighter, smaller
  - fabricator - controllable, reproducible
- Rules defined in generally in terms of
  - Widths
  - separations (spacing)
  - overlaps

Design Rules: The Reality

- Manufacturing processes have inherent limitations in accuracy and repeatability
- Design rules specify geometry of masks that provide reasonable yield
- Prevents shorting, opens, contacts from slipping out of area to be contacted
- Design rules are determined by experience
- Estimation of parametric yield is useful for circuit designers because it helps identify the limits of the manufacturing process and facilitate and encourage design for manufacturability

Design Rules: Categories

- Well Rules
- Transistor Rules
- Contact Rules
- Metal Rules
- Via Rules
- Other Rules

- Use of Design Rules
  - For Design Rule Check (DRC)
  - For Extraction of Transistor Circuit from Layout
- Both are automated by EDA Tools

Lambda based design rules

- Design rules based on single parameter, λ
- Normalize for feature size. Rules expressed in terms of λ = *f*/2
  - E.g. l = 0.3 μm in 0.6 μm process
- Simple for the designer and wide acceptance
- Portable to different foundries
- Instantly scale design to new process by changing lambda definition
- See Mosis web site http://www.mosis.com/Technical/Designrules/scmos/scmos-main.html

Lambda based design rules: DSM

- Original lambda rules – "Scaleable CMOS" or SCMOS
  - Valid for 1.0μm – 3.0μm
- Sub-micron processes – SCMOS-SUBM rules
  - Increases lambda size for some rules (those that didn't scale as fast as feature size)
  - Allows a smaller value of lambda and tighter layout
- Deep sub-micron processes – SCMOS-DEEP rules
  - At 0.25μm and below

Examples of Lambda

Table 2a: MOSIS SCMOS-Compatible Mappings

Foundry	Process	Lambda (micro- meters)	Options
AMI	ABN (1.5 micron *n*-well)	0.80	SCNA, SCNE
AMI	C3O (0.35 micron *n*-well)	0.25	SCN4M, SCN4ME
AMI	C5F/N (0.5 micron *n*-well)	0.35	SCN3M, SCN3ME
Agilent/HP	AMOS14TB (0.5 micron *n*-well)	0.35	SCN3M, SCN3MLC
TSMC	0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V)	0.25	SCN4ME
TSMC	0.35 micron 1P4M (4 Metal Silicided, 3.3 V/5 V)	0.25	SCN4M

Table 2b: MOSIS SCMOS_SUBM-Compatible Mappings

Foundry	Process	Lambda (micro- meters)	Options
AMI	C3O (0.35 micron *n*-well)	0.20	SCN4M_SUBM, SCN4ME_SUBM
AMI	C5F/N (0.5 micron *n*-well)	0.30	SCN3M_SUBM, SCN3ME_SUBM
Agilent/HP	AMOS14TB (0.5 micron *n*-well)	0.30	SCN3M_SUBM, SCN3MLC_SUBM
TSMC	0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V)	0.20	SCN4ME_SUBM
TSMC	0.35 micron 1P4M (4 Metal Silicided, 3.3 V/5 V)	0.20	SCN4M_SUBM
TSMC	0.25 micron 5 Metal 1 Poly (2.5 V/3.3 V)	0.15	SCN5M_SUBM
TSMC	0.18 micron 6 Metal 1 Poly (1.8 V/3.3 V)	0.10	SCN6M_SUBM

Table 2c: MOSIS SCMOS_DEEP-Compatible Mappings

Foundry	Process	Lambda (micro- meters)	Options
TSMC	0.25 micron 5 Metal 1 Poly (2.5 V/3.3 V)	0.12	SCN5M_DEEP
TSMC	0.18 micron 6 Metal 1 Poly (1.8 V/3.3 V)	0.09	SCN6M_DEEP

SCMOS Design Rules

Layer	Rule	Description	SCMOS	SUBM	DEEP
Well	1.1	Width	10	12	12
	1.2	Spacing to well at different potential	9	18	18
	1.3	Spacing to well at same potential	6	6	6
Active (diffusion)	2.1	Width	3	3	3
	2.2	Spacing to active	3	3	3
	2.3	Source/drain surrounded by well	5	6	6
	2.4	Substrate/well contact surrounded by well	3	3	3
	2.5	Spacing to active of opposite type	4	4	4
Poly	3.1	Width	2	2	2
	3.2	Spacing to poly over field oxide	2	3	3
	3.2a	Spacing to poly over active	2	3	4
	3.3	Gate extension beyond active	2	2	2.5
	3.4	Active extension beyond poly	3	3	4
	3.5	Spacing of poly to active	1	1	1
Select	4.1	Spacing from substrate well contact to gate	3	3	3
	4.2	Overlap of active	2	2	2
	4.3	Overlap of substrate/well contact	1	1	1.5
	4.4	Spacing to select	2	2	4

SCMOS Design Rules

Layer	Rule	Description	SCMOS	SUBM	DEEP
Contact	5.1,6.1	Width (exact)	2x2	2x2	2x2
	5.2b, 6.2b	Overlap by poly or active	1	1	1
	5.3, 6.3	Spacing to contact	2	3	4
	5.4, 6.4	Spacing to gate	2	2	2
	5.5b	Spacing of poly contact to other poly	4	5	5
	5.7b, 6.7b	Spacing of active/poly for multiple poly/active contacts	3	3	3
	6.6b	Spacing of active contact to poly contact	4	4	4
Metal1	7.1	Width	3	3	3
	7.2	Spacing to Metal1	2	3	3
	7.3, 8.3	Overlap of contact or via	1	1	1
	7.4	Spacing to metal for lines wider than 10 λ	6	6	6
Via1	8.1	Width (exact)	2x2	2x2	2x2
	8.2	Spacing to via on same layer	3	3	3
	8.4	Spacing to contact (if no stacked via)	2	2	(n/a)
	8.5	Spacing of via1 to poly or active edge	2	2	(n/a)
	14.4	Spacing of via2 to via1 (if no stacked via)	2	2	(n/a)

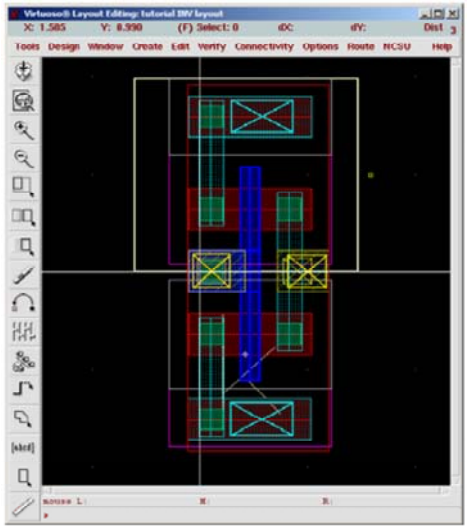
Lambda design rules: Examples

- Often illustrated by diagrams (specified by ASIC design rule files or text)
- See http://www.mosis.com/Technical/Layermaps/lmscmos_scn5m.html

Micron Rules

- Lambda rules are conservative
  - Worst-case set of rules across many processes
  - Leads to larger layout
- Industry mostly uses “Micron rules”
  - Each dimension is given in absolute microns
  - Tighter design
  - Less portable than lambda rules
- This class uses Micron rules
- Sill good to know lambda rules!
  - allows you to do fairly accurate estimations for layout in any process

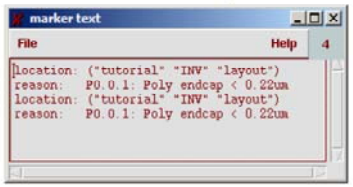
Minimum Size Inverter Layout



Design Rule Checker (DRC)

- Design rules automatically checked by Cadence

- After running DRC, error markers appear
- "Explain" command gives rule and dimensions



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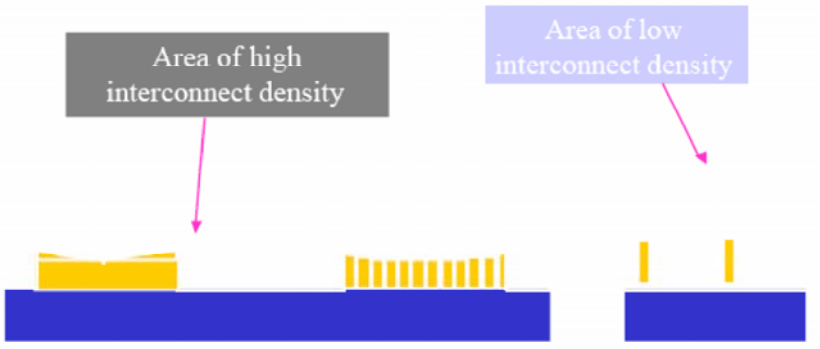
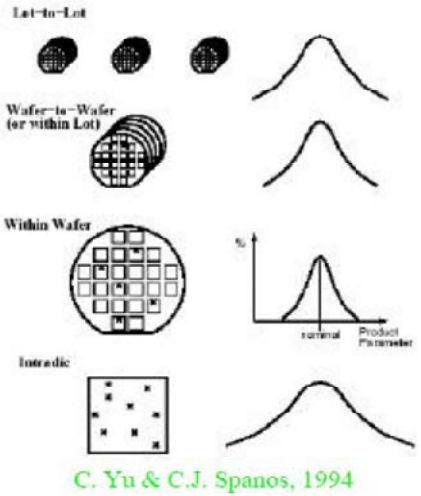
Interconnect Variation Sources

- Pattern density effect during Chemical Mechanical Planarization (CMP), which results in systematic wire height variation



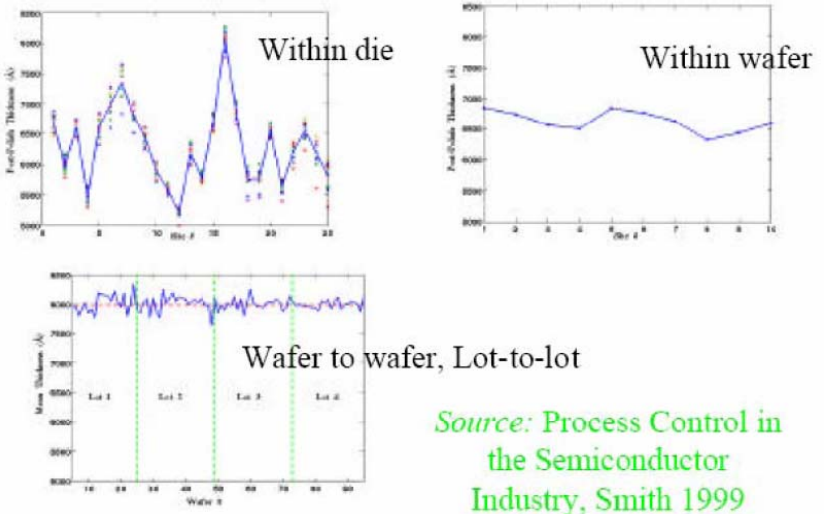
Sources of Process Variation



C. Yu & C.J. Spanos, 1994

- Variations in impurity concentration densities, oxide thickness, and diffusion depths caused by non-uniform conditions during the deposition and/or the diffusion of the impurity
- Variations in the device dimensions, mainly resulting from the limited resolution of the photolithographic process
- Variation in interconnect caused by CMP

Metal Width Variation Comparision



Source: Process Control in the Semiconductor Industry, Smith 1999

What to do as a Designer

- Worst-Case Consideration:
  - PVT (Process-Voltage-Temperature) Corner Simulation
    - supply voltage 2.1, 2.0, 1.9, 1.8
    - temperature 200, 220, 230
    - process: fast-npn, slow-pnp, (SPICE model files provided by the foundry)
- Monte Carlo Simulation
  - Given statistical process parameters, perform Monte Carlo (supported by most circuit simulators such as SPICE)
- Be aware of miss-matching for analog circuits

Yield

- Variability in IC manufacturing processes can lead to deformations or non-conformities in finished products
- Yield is defined as the percentage of devices or circuits that meet a nominal performance specification
- Commonly for digital ICs, we define
  - Functional (Hard) Yield - (opens, shorts, particles,..)
  - Parametric (Soft)Yield – (speed, noise immunity, power consumption)

Functional Yield

- Affected by the presence of defects
- Defects result from a number of random sources:
  - Contamination from equipment
  - Contamination from processes and handling
  - Mask imperfections
  - Airborne particles

Parametric Yield

- A measure of ‘quality’ of functioning systems
- Even in a defect free manufacturing environment, random process variations can lead to varying levels of system performance
- line widths, film thickness, relative humidity

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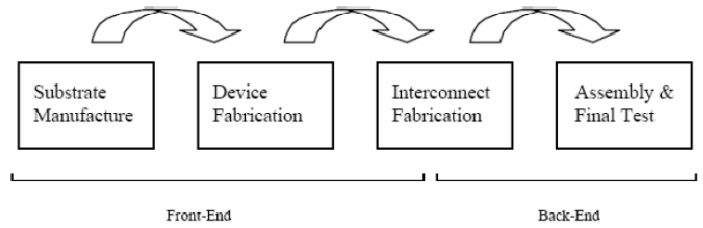
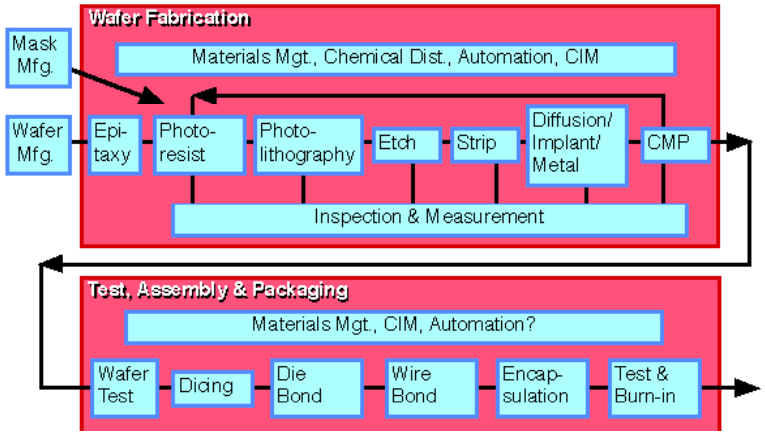
Fabrication Sequence

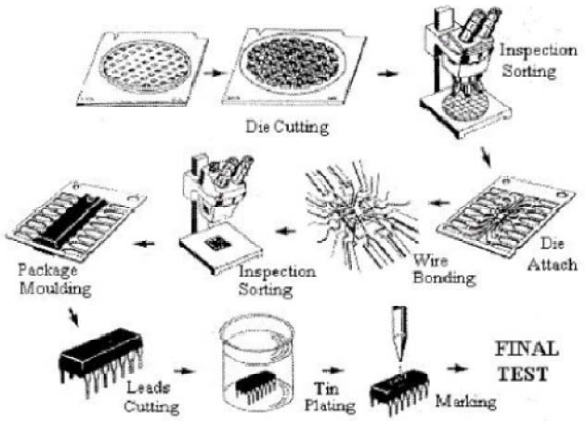


- Two manufacturing phases
- Front-end
  - Wafer fabrication – what you have already seen today
- Back-end – assembly
  - wafer probing
  - packaging the die
  - final test

Chip-Making Process



Final Assembly Process



The Cost of Fabrication

- Building the Fab
  - Current cost $2 - 3 billion
  - Typical fab line occupies 1 city block, employees a few hundred employees
  - Most profitable period is first 18 months to 2 years
- For large volume IC's packaging and testing is largest cost
- For low volume IC's, design costs may swamp manufacturing costs

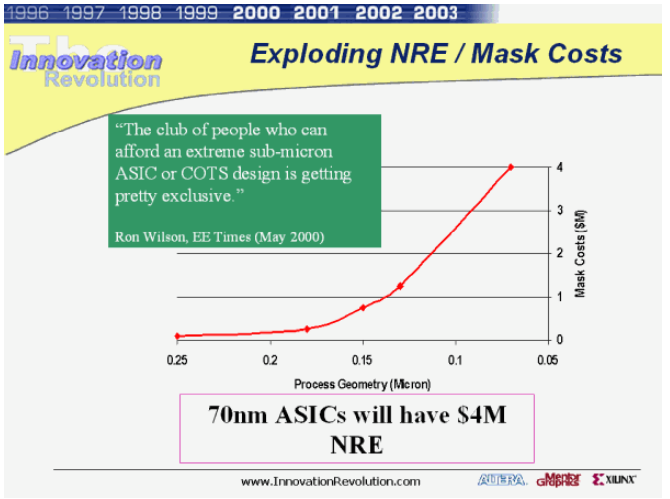
Manufacturing Costs

- Manufacturing involves many processing steps – each step adds to cost of wafer
- Wafer costs depend on:
  - number of masks used
  - the complexity of the devices
  - clean room requirements
- Costs increase with number of layers in a non-linear fashion - more defects introduced
- Cost per chip increases with smaller feature size – due to stringent requirements of lithography and process control
- Semiconductor fabrication process is highly toxic

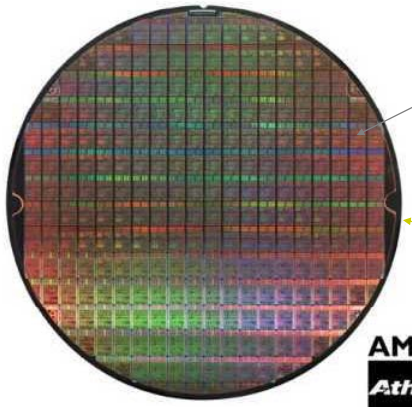
Cost of Integrated Circuits

- NRE (non-recurrent engineering) costs
  - design time and effort, mask generation
  - one-time cost factor
- Recurrent costs
  - silicon processing, packaging, test
  - proportional to volume
  - proportional to chip area

NRE Cost is Increasing



Die Cost



Single die

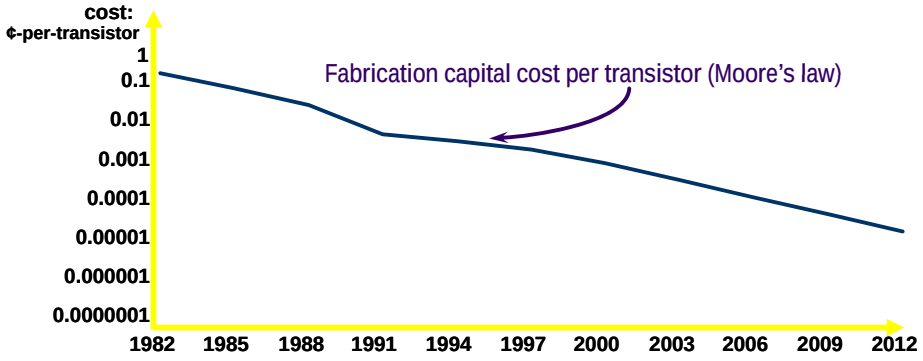
Wafer

AMD Athlon

Going up to 12″ (30cm)

From http://www.amd.com

Cost per Transistor

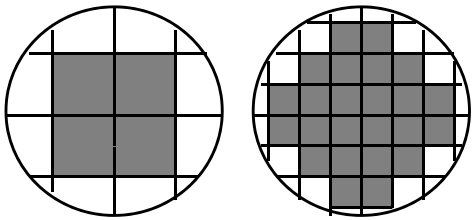


Yield

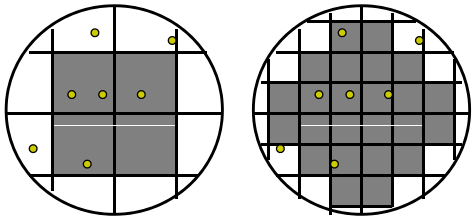
$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$



Defects



$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$

α is approximately 3

$$\text{die cost} = f(\text{die area})^4$$

Some Examples (1994)

Chip	Metal layers	Line width	Wafer cost	Def./ cm^2	Area mm^2	Dies/ wafer	Yield	Die cost
386DX	2	0.90	$900	1.0	43	360	71%	$4
486 DX2	3	0.80	$1200	1.0	81	181	54%	$12
Power PC 601	4	0.80	$1700	1.3	121	115	28%	$53
HP PA 7100	3	0.80	$1300	1.0	196	66	27%	$73
DEC Alpha	3	0.70	$1500	1.2	234	53	19%	$149
Super Sparc	3	0.70	$1700	1.6	256	48	13%	$272
Pentium	3	0.80	$1500	1.5	296	40	9%	$417

Summary

- Semiconductor fabrication process
  - photolithography and masking
- Design rules
  - Rules on spacing, width and overlap
  - Used for DRC and extraction
- Process variations are inherent
  - PVT Corners
  - Monte Carlo
- Think transistors, think mask geometry patterns, vice versa