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NASA MSFC
Astrionics Laboratory
Technology Division
Marshall Space Flight Center, Alabama

FINAL REPORT

"FEASIBILITY STUDY AND ANALYSIS OF THE USE OF COMPUTERS TO PREPARE MONOLITHIC INTEGRATED CIRCUITS FOR GSE"

Prepared by:

Approved by:

M&S Computing, Inc.
Huntsville, Alabama

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ABSTRACT

At the request of NASA MSFC, M&S Computing, Inc. has conducted a study on a conceptual approach for performing computer assisted MOS FET Circuit Design; the objective of the study being to develop the functional design of a baseline package which will provide for the computer assisted design of the photographic masks necessary for circuit fabrication. This report presents the software functional design and the system configuration required to implement this software. Both the software and system configuration are evaluated in terms of performance capabilities and future growth potential.

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PART I

PROBLEM DEFINITION

1.1 INTRODUCTION

M&S Computing, Inc. has been conducting a study for the NASA MSFC Astrionics Laboratory, Technology Division, on a conceptual approach for performing computer assisted MOS FET Circuit Design. The study effort was conducted to satisfy the following primary objectives:

(1) To confirm the feasibility of performing computer assisted MOS FET Circuit Design on a system available to NASA MSFC, and

(2) To develop the functional design of a baseline package which will provide for the computer assisted design of the photographic masks necessary for circuit fabrication.

To meet these objectives it was necessary to develop, during the course of this study, the standardization groundrules and the man/computer communication interface applicable to this application. Realistic system constraints were established by orienting the baseline approach towards the SDS 930 computer, which NASA MSFC had indicated was a potential small system candidate for performing this task.

The study effort was broken into the following three logically sequential study phases.

1.2 COMPUTER TASK STUDY

The first phase consisted of a definition and evaluation of the explicit functions that the computer would be required to perform during the circuit design task. This phase was relatively machine independent and consisted primarily of a determination of the desired man/computer interface, a functional definition of the application software, and a formalization of the necessary output requirements.

Since NASA MSFC had expressed an explicit interest in a system oriented about a graphics terminal which would provide the designer/engineer with a real time circuit design tool, M&S Computing placed special emphasis on defining a concept which provided for a graphics terminal to establish efficient two-way communication between the designer and the system.

To effectively estimate the graphics software requirements, a study was made of the current design and manufacturing procedure employed by NASA MSFC to produce MOS FET circuits. Particular attention was payed to the average chip device densities. Since the complexity of the graphics problem is directly related to the circuit complexity, it was necessary to define a "worst case" circuit in order to realistically bound the graphics requirement. A standard "worst case" or most complex circuit was defined by NASA MSFC which consisted of the following elements:

30 standard cells with up to 100 devices total
18 bonding pads
100 contact nodes
210 normal nodes

The computer task study resulted in the functional definition of a baseline software system, oriented around a graphics terminal, and designed to provide computer assisted MOS FET circuit design on a small dedicated system. The conclusions arrived at during this phase of the study are presented in detail in the attached Appendix, "A Design Concept for Computer Controlled MOS FET Circuit Artwork Generation." This Appendix should serve as a valuable reference and guidance document if such a system is implemented.

In particular, the Appendix presents a detailed discussion of:

1. The current NASA MSFC operations.

2. The standardized placement and interconnect groundrules established during the study phase.

3. The designer/computer communication interface both with and without a graphics terminal.

4. The functional design of the baseline software, including flowcharts, and

5. The processor requirements which include initial storage estimates and input/output requirements.

All of the storage estimates contained within the Appendix have been based on the "worst case" circuit described above.

1.3 INDUSTRIAL SURVEY

The second phase of the study effort consisted of a limited industrial survey which was conducted in order to evaluate the work that has been done in the field of computer aided circuit design and analysis. As a result of an expressed NASA MSFC interest, the survey was concentrated in two distinct areas. First, a review was conducted of a selected set of industrial packages which utilize a graphics terminal to support various phases of the automated circuit design and analysis process. Secondly, the BANNING Program, which is available from the National Security Agency, was evaluated in relation to NASA MSFC requirements.

The results of the Industrial Survey are discussed in Section II of this report.

1.4 SYSTEM CONFIGURATION STUDY

The third and final phase of this study effort consisted of the development of a recommended system hardware configuration and an analysis of the operational efficiency and limitation of the baseline software, presented in the Appendix, on the designated system. The UNIVAC 1108 Computer was evaluated to provide a comparison between the simple baseline approach used in defining the SDS 930 System configuration and the typical large scale approach used in industry. The UNIVAC 1108 is a large scale general purpose system which is currently being utilized by the NASA MSFC Computation Laboratory. Since this system is available to the Astrionics Laboratory Technology Division, it is a logical candidate for this task.

The results of the System Configuration Study are presented in Section III of this document.

Section IV of this document contains a concise summation of the conclusions arrived at during the course of this study effort and the recommendations being made by M&S Computing, Inc.

PART II

INDUSTRIAL SURVEY

2.1 INTRODUCTION

In order to determine the "state-of-the-art" and to be able to isolate trends within the field of computer aided circuit design and analysis, M&S Computing conducted a limited survey of industrial software systems. Some of the system reviewed required more than 200K of on-line storage in which to operate. These software packages may seem unduly large and complex, but as the engineer begins working with more complex circuits, he requires all the support capability available to solve interconnection problems and perform detailed circuit analysis.

Since NASA is considering implementing the BANNING Program developed by the National Security Agency, special emphasis was placed on developing a functional knowledge of this program in order to be able to evaluate the program in terms of applicability to current NASA requirements.

Due to the increased interest in real time circuit design capabilities and the additional program control provided by interactive graphics, the graphics terminal is playing an important role in industrial applications. During this survey special emphasis was placed on reviewing large industrial applications that provide graphics capabilities in order to determine the present and future role of graphics within the field of integrated circuits.

2.2 GRAPHICS ORIENTED SYSTEMS

The primary advantage of an on-line graphic display is that the user is able to quickly and easily interact with the program. It is apparent that there is a definite trend toward providing interactive graphics to facilitate circuit design, improve circuit development time, and optimize circuit performance. The software systems listed below have been developed by industry due to user demands for increased use of computer graphics to enhance the man-machine inter face.

CIRCAL: On-Line Circuit Design (Massachusetts Institute of Technology)

CADIC: Computer Aided Design of Integrated Circuits (United Aircraft Corporation)

EACP: Electronic Circuit Analysis Program (International Business Machines Corporation)

MICROMOSAIC (Fairchild Semiconductor)

Each of these programs was investigated during the course of this study effort because of their use of computer graphics to provide a real time graphics capability. Since detailed information on each of these systems is readily available to the reader, they have not been described in detail.

As software systems grow in size and complexity to provide the utmost capabilities in circuit design, analysis, routing, and artwork generation, they require larger computer resources than can be economically and realistically provided by a dedicated computer. However, large computer facilities must maintain a relatively free general computing capability and must remain available to many users for various applications. The graphics terminal which interfaces with a time-shared computer system allows the man-machine communication demanded by the designer/engineer without restricting the computer's capability of servicing other user requests.

The amount of software required to support interactive graphics depends on the complexity of the circuits being developed. As the circuits grow in complexity, the circuit schematic and mask graphic data may increase to such an extent that the display hardware is unable to present the entire circuit effectively. When this situation occurs, errors begin to increase due to free-hand handling of the light pen when specifying component locations and interconnections. This problem is common among users utilizing computer graphics as a circuit design tool, and software capabilities have been developed to correct the problem by using a "window", "zoom", or "scroll" concept for displaying only the section of the circuit in which the designer is interested. While the actual technique of implementation is different for each of these three concepts, they each effectively scale the graphic image on an imaginary surface far larger than that provided by the terminal screen.

The software required to provide a preliminary graphic design capability and a basic user oriented design language needed for effective designer/machine communication are presented in the Appendix of this report. This software was functionally defined as part of a baseline system designed to solve the immediate requirements of the NASA MSFC Astrionics Laboratory Technology Division, but is capable of being expanded to serve as the basic software requirement for a large scale system accessed from a remote graphics terminal.

2.3 BANNING

The Banning Design Automation System consists of five major programs and a standardized cell pattern library which provides for the design of MOS-FET circuits using standardized thick-oxide P-MOS building blocks or "cells." The five major Banning Programs are briefly described below.

2.3.1 Functional Description

The first two of the five programs are required to translate the detailed logic design into the precision MOS-FET photographic masks required to manufacture the desired circuits. The remaining three programs provide the analytical capability necessary to evaluate the performance of basic circuit and logic nets.

2.3.1.1 Placement-Routing-Folding (PRF) Program

The PRF Program is responsible for performing final cell placement on the chips and component signal interconnection routing. The final placement of the individual cells on the chips is governed by the computer which is responsible for establishing a placement which results in suitable minimum total wire lengths for interconnecting the array. Once cell placement has been completed, the signal interconnections are routed using both metal pathways and P-region tunnels.

The input data cards for the PRF Program are in the same format as those utilized by the logic block simulator. The PRF Program pre-processes the input data and converts it for its own needs. The common input format reduces the possibility of errors being introduced when proceeding from the circuit analysis phase to the placement, routing, and artwork generation phase. The PRF Program capability

is a function of the computer's memory size. For example, the GE 625 System appears to be able to handle arrays of more than 150 cells. (A bonding pad is counted as a cell.)

The output available from the PRF Program consists of the following four items:

(1) Two types of capacitance loading data (before and after routing).

(2) A folded array printout showing chip size, cell locations, cell orientation, and type.

(3) A printout of the predicted speed performance of the array as determined by the Signal-Trace Program.

(4) A listing of the PRF Program output specifications, cell locations, orientations, signal interconnects, and parallel bus and bonding pad locations.

2.3.1.2 Artwork Program

The Artwork Program generates the commands required by the Gerber Plotter to draw the desired artwork. The program output is a magnetic tape which contains the light aperture and motion commands which control the operation of the plotter. The topology data for the standard cells required by the program are available from the Banning cell pattern library.

The Artwork Program also performs certain housekeeping functions such as updating the library tape and formulating Gerber instructions for drawing standard cell composites from digitized cell data.

2.3.1.3 MOS Logic Block Simulator

The Logic Block Simulator is a self-contained program designed to simulate the binary logic system of interconnected MOS-FET standard cells. The program is driven from card inputs which describe the cell types comprising the circuit along with cell characteristics and interconnection information.

The primary output consists of columnized 0's and 1's which represent the outputs of specific cells as they exist at the end of Phase I or Phase II clock times. The run limitation is a function of the number of output columns available on the line printer.

2.3.1.4 Signal Trace and Transient Analysis Programs

The Signal Trace Program operates as a subroutine of the PRF Program and provides a highly accurate time analysis prediction for the desired array.

The Transient Analysis Program is used to evaluate the response times of the basic Banning cells.

Since this report is not concerned with circuit analysis, the above descriptions are deliberately sketchy. If additional information on these programs is desired, the reader is directed to the detailed Banning Software Documentation.

2.3.2 Advantages and Disadvantages

The Banning package is a sophisticated, large scale, batch processing oriented, design automation system which contains extensive capabilities for performing automated circuit design, analysis, and artwork generation. The capabilities are ideally suited for the design engineer who wishes to develop large scale MOS FET arrays with an emphasis on circuit analysis. A large pattern library of standardized cells simplified the design task, and a set of well standardized operating definitions allow the computer to relieve the designer of much of the tedium associated with the design process. In particular, the computer will perform for the designer automatic component placement, signal interconnection routing, and array interconnection. In addition, Banning supplies a number of analytical tools which allow the engineer to effectively analyze the predicted performance of his design.

In spite of the extensive capabilities of the Banning System, a number of limitations do exist which restrict the usefulness of the system in the highly R&D oriented atmosphere of the NASA MSFC Astrionics Laboratory, Technology Division operation.

The major limitation is the lack of a graphics terminal capability which would allow the designer to control, on line, the design and

analysis processes, and to actively participate in the design, placement, and routing operations with the computer. As stated earlier, the current trend in industry is to develop real time design automation systems in which the man and the computer complete the design process during an interactive on-line dialogue. The use of such graphics terminal systems allows the engineer to monitor his design through the entire development cycle and to make modifications or corrections as desired.

Two other limitations exist which are only minor in nature and could be easily corrected:

(1) No punched tape output currently exists from the Artwork Generation Program. Such a tape must be generated in order to drive the NASA Gerber Plotter.

(2) No preliminary plotter output of the circuit masks is provided prior to using the Gerber. Such an output on an inexpensive plotting device, such as one of the smaller Cal Comp machines, would prove valuable in verifying the mask design prior to actual generation, and could considerably reduce wasted Gerber operation.

PART III

SYSTEM CONFIGURATION STUDY

3.1 INTRODUCTION

The System Configuration Study was designed to identify the minimum realistic definition of the system hardware configuration required to perform the designated task while allowing for a reasonable growth potential. In defining a system configuration for computer aided circuit design, all systems from the large multi-processor time sharing system to the small "in house" dedicated computer must be considered.

The final system configuration must be chosen on the basis of the task requirements, the desired level of growth potential, and the user's availability requirements. There are advantages in developing an "in house" system that is closely monitored by the engineer responsible for its application; however, if the future expectations of the system require extensive circuit design and analysis capabilities, care must be taken to provide a system configuration that will permit the necessary growth required. If such growth is to be extensive, a large scale system may be necessary from the start.

3.2 DEDICATED SYSTEM (SDS 930)

The baseline software requirements presented in the Appendix of this report are developed around a small "in house" system configuration. However, care has been taken to insure that a large scale development could be implemented as a logical extension of this baseline package.

The small dedicated system can provide many advantages to both the programmer and user. Some of the more obvious advantages are listed below:

- Implementation is easier.
- Closer programmer/engineer communication.
- Engineers work directly with the computer.

- Immediate turnaround time.

Fast turnaround time, on-line debugging, and fewer system constraints facilitate and accelerate the development of software packages for a small dedicated computer. Such a system will establish and enhance a close communication between the engineers and programmers, resulting in a better system performance and confidence. Since turnaround time has been identified as a major problem with the current operation, the availability of a small system is a key advantage of a computer dedicated to the support of one project.

The basic system configuration presented in this section is small enough to be readily available as a design tool, and is also capable of significant expansion in order to handle the future requirements of the designer/engineer.

The minimum SDS 930 hardware configuration needed to effectively provide a real time circuit design tool should consist of the following elements:

- SDS 930 Central Processing Unit
- 16,000 Word Memory
- Graphic Display Terminal
- Disc
- Card Reader
- Magnetic Tape Unit

The SDS 930 is a high speed, low cost, general purpose digital computer, ideally suitable for use in a system dedicated to the support of one project. The computer is fast enough to provide the necessary response time needed to drive a real time circuit design system, and large enough to support significant growth potential. With an extensive overlay structure, the baseline software system could be implemented in an 8K memory; however, this would considerably complicate software implementation and would severely restrict the system growth potential and versatility. A 16K storage capability will result in the best overall systems performance and will simplify implementation.

The high speed direct access capabilities of the disc are necessary due to the fast response time demanded by the display terminal. The entire task of computer aided circuit design is primarily concerned with data manipulation and organization. The major percentage of the off-line storage provided by a disc will be devoted to the data tables needed for circuit schematics and mask definition. As the circuit development passes from the real time design phase into the mask creation phase, I/O response time becomes less important permitting the use of magnetic tape as both intermediate storage and as the final output medium for the circuit masks.

The card reader provides the necessary input device to communicate with the system assembler and to handle the large amount of data required to create and update the data tables on disk. If the system does not contain an interactive graphics display, the circuit design commands may also be entered by cards.

The basic design language developed in the Appendix of this report is compatible with both standard batch type job input and control, as well as with an interactive graphics capability. The developed system should be highly user oriented and should provide efficient designer/computer communication. A graphics capability simplifies the communication between the engineer and the computer, and places the designer in direct control of the development of his circuit. Without the graphics capability, the designer loses a powerful design tool and the system reverts to batch oriented operation.

3.3 LARGE SCALE SYSTEM (UNIVAC 1108)

The software available today that can be used for automated circuit design, analysis, routing, and artwork generation exceeds by far the capability of a small computer. These capabilities are natural extensions of a small scale circuit design system and should be carefully considered as possible future applications before committing to the development of a less sophisticated system.

The UNIVAC 1108 System presently in use at Marshall's NASA Computational Laboratory is capable of supporting the most sophisticated circuit design software currently available in industry for the preparation of monolithic integrated circuits. The UNIVAC 1108 System is a large-scale data processing system that features multiprogramming and multi-processing capabilities for high performance.

The cost, performance, and availability of the 1108 system prohibits its use as a dedicated computer to a project of this size. However, by incorporating a remote graphics terminal capability within the system, the designer/engineer would have both the capabilities of a large scale system and the availability of a dedicated computer. This arrangement would provide an unquestionable "best system" as future growth potential would be practically unlimited and turnaround time would be near optimum.

The cost of both the hardware and software required to provide graphic terminals has previously prohibited the large scale use of interactive graphics as the solution to the man/machine communication problem. A graphics terminal which provides sufficient capability for permitting computer assisted MOS FET circuit design and system software of the magnitude needed to support such terminals in a time shared environment is costly and would have to be developed in a general package to support many terminal users. Large scale systems which service many users invariably operate in a multiprogramming environment in order to effectively use central processor time during the delays inherent in servicing I/O requests. If the same system is to support terminals, additional software must be developed to provide a "demand" (priority) processing mode to establish productive "conversation" between the terminal and the computer.

The UNIVAC 1108 System currently in use at the NASA MSFC Computational Laboratory provides a graphics terminal capability. Several UNIVAC 1558/1557 Graphics Terminals have been placed in various locations within the NASA MSFC Facility, and are presently supported for on-line user applications. The UNIVAC 1108 system software is oriented toward maximizing the throughput of batch operations, while providing the capability for handling useful amounts of real time and demand processing. The system software, however, is of a general nature and must be supplemented by user software to be able to interpret the operator action and determine the required response. As explained in Section II of this report, the user-oriented graphic software required to provide an interactive graphics capability is proportional to the complexity of the circuits being designed. The generation of the additional application software required to utilize the existing graphics terminal will not be a minor problem. Graphics packages

can become extremely complex, especially if extensive operator flexibility and control must be provided. However, the advantages of such a graphics package, when considered in the light of the benefits provided by terminal operations, make it essential that such a system be seriously considered. Without the remote graphics terminal, the UNIVAC 1108 becomes unavailable for on-line, real-time circuit design, but retains the capability of employing the most up-to-date developments in the preparation of integrated circuit masks.

PART IV

STUDY CONCLUSIONS

The final system configuration must be chosen on the basis of the task requirements, the desired level of growth potential, and the user's availability requirements. The baseline software developed during this study is well suited for the SDS 930 system configuration presented in Part III. If a small dedicated system is desired, the SDS 930 configuration is large enough to perform the specified task and to provide a reasonable growth potential. However, if a graphics terminal is available for the 1108, it is unquestionably the more desirable system for performing automated artwork generation. This is especially true if future plans for the system require an extensive circuit design and analysis capability.

4.1 NASA OPERATION

4.1.1 Current Intentions

NASA MSFC is currently actively engaged with the evaluation and preliminary implementation of the Banning System. Tentative plans call for initially implementing the Artwork Program in order to establish a minimum production oriented capability to be followed later by the addition of the other Banning System components in a building block sequence. The overall objective appears to be to provide the full capabilities of the Banning System to NASA MSFC but in a sequence which allows the artwork generation capability to be available for use as quickly as possible.

Preliminary estimates indicate that approximately 1 - 3 months of effort will be required to make the Artwork Program operational at the Huntsville Facility if no serious complications are encountered. Inputs for the initial artwork system will probably have to be hand generated since the PRF Program will not be operational initially.

4.1.2 Potential Problem Areas

A number of potential problems exist with the current NASA proposal for the implementation of the Banning System. In presenting these points, it is not M&S Computing's intention to discourage the use

of the Banning System. The system is basically sound and contains extensive desirable capabilities. However, it is imperative that potential problem areas be quickly identified so that the responsible NASA personnel can assess their impact and develop appropriate corrections.

(1) The original NASA intention was to develop a system to support the designer/engineer during the placement and routine operations of MOS FET circuit design and to eliminate the tedious and time consuming manual operations involved in generating chip artwork. The current operation and its inherent problems are described in Section A. 2 of the Appendix. The current proposal to make the Banning Artwork Program operational will require 1 - 3 months of effort and will not substantially alleviate the problems associated with the current operation for the following reasons:

(a) Placement and routing will still have to be done by hand without the PRF Program. In order to digitize the necessary input data for the Artwork Program, the designer will still have to provide a scaled mask drawing which a programmer must then convert to the proper input format. While the full drafting steps of the current operation should not be necessary, significant manual preparation will still be required.

(b) The Artwork Program cannot directly provide the control paper tape needed to drive the Gerber Plotter. The magnetic tape output of the Artwork Program must be processed by essentially the same program currently used to punch the Gerber paper tape.

(c) It is unclear yet that the output from the Artwork Program is fully compatible with the Gerber Plotter at MSFC. As long as the deviations are not major, this problem should not be critical.

(2) Since the Banning System does not support a graphics terminal, the system is unavailable for on-line, real time circuit/mask design. Efficient two-way communication between the engineer and the system during the design phase will not be realized.

4.2 IMPORTANCE OF GRAPHICS

The NASA MSFC Computational Laboratory and many industrial computer facilities have realized the growing demand to supplement batch processing abilities with the remote terminal capability to provide effective man/machine communication. To allow the computer to completely replace the circuit designer, a multitude of design rules for the design of individual devices and for their interconnection into complete circuits must be established to generalize circuit designing and present the problem in terms applicable to the computer. Experience and subjective reasoning of the experienced designer is lost, freedom of design is greatly restricted, and considerable circuit design efficiency is eliminated in order to restrict designer interaction requirements. If the experienced circuit designer, whose primary interest is experimental design with a maximum emphasis on optimization, is to be provided computer assistance, an interactive graphics capability is highly desirable.

Interactive graphics provides a real time circuit design tool and allows the designer/engineer to specify components and control placement and interconnection modifications. The designer/engineer is able to "review" completed circuits and incorporate late design changes or modifications prior to generating the final artwork.

M&S Computing feels that interactive graphics is essential to the type of research and development work that is performed at the NASA MSFC Facility. Since both the hardware and software are available to provide graphic terminal support on the UNIVAC 1108 system, the amount of effort and expense required to provide the circuit designer with an interactive graphics capability is well worth while in light of the advantages of such a system.

4.3 RECOMMENDATIONS

In particular, M&S Computing feels that there are a number of distinct recommendations to be made as a result of this study effort:

(1) A UNIVAC 1558/1557 Graphics Terminal is located in the B Wing of the Astrionics Laboratory. If this system can be made available for this application, the UNIVAC 1108 will provide an unquestionable "best system" for this task since future growth potential would be practically unlimited and turn-around time would be near optimum.

(2) Immediate emphasis should be placed on developing the complete design of an application, user oriented graphic design language for this task. This language should be capable of supporting both job control and circuit design, analysis, routing, and artwork generation.

(3) The required graphics application software should be developed in parallel with the implementation of the Banning Artwork Program.

(4) The Banning Artwork Program will, if coupled to a display terminal, provide a significant improvement in the design and generation of circuit masks. However, the desirability of implementing the full Banning Program should be seriously reviewed. It is not at all clear that the benefits provided by the total Banning System are worth the cost of implementation to the NASA MSFC Facility.

APPENDIX

A DESIGN CONCEPT FOR COMPUTER CONTROLLED MOS FET CIRCUIT ARTWORK GENERATION

A.1 INTRODUCTION

The Computer Task Study was dedicated to developing a logically consistent and realistic software approach for performing computer assisted MOS FET circuit design. It was conducted with a systems approach in that all aspects of the design sequence were scrutinized and modified if necessary to form an overall approach with mutually compatible components. A considerable amount of effort was spent developing standardization groundrules for:

(a) Component Designation

(b) Cell Architecture

(c) Circuit Architecture, and

(d) Circuit Component Interconnection

A basic design language was developed which is compatible with both standard batch type job input and control, as well as with an interactive graphics capability. The man/computer communication interface is discussed in detail in Section A.4.

The software package which was designed as a result of this study effort has been functionally flowcharted and is presented in Section A.5.7. The output capabilities of the proposed system are presented in Section A.6, along with a discussion of desirable documentation and hard copy requirements.

A. 2 CURRENT OPERATION

The following discussion of current MOS FET design fundamentals is provided to establish a common baseline knowledge and to eliminate any possible confusion caused by the terminology utilized during the subsequent sections of this report. Those individuals fully versed in MOS FET design techniques need not concern themselves with this section.

The MOS FET (Metal-Oxide-Silicon Field Effect Transistor) is a solid state device which differs from the ordinary transistor in that it is a voltage amplifier with a very high input impedance and a transfer characteristic similar to that of a pentode vacuum tube. The simplest form of this device is shown in Figure A1, however, the actual layout may vary considerably, depending upon desired device characteristics and the circuit configuration into which the device is designed.

The device considered during this study was a P channel enhancement mode device and consists of a block of N type silicon called the Substrate into which P^+ impurities are diffused in two parallel strips called "the source" and "the drain". The area of N type silicon between the two P area strips is called the channel and becomes an induced P region during operation. The entire surface of the chip is covered by silicon dioxide which is etched down over the P regions and the channel area. A metal gate is deposited over the channel area, separated from it by the oxide. Metal supply lines contact the source and drain through contact cutouts in the oxide.

For a MOS FET circuit in which all devices are made by the same process, the characteristics of each transistor will be controlled primarily by the gate length and width. This feature is of the utmost importance in designing MOS FET devices.

As a first step in actual device fabrication, a thin layer of silicon dioxide is grown on the surface of the silicon wafer. This is followed by four photographic etch steps intermixed with other steps such as impurity diffusion, vacuum metalization, and intermediate layerings with silicon dioxide. The masks for these photographic operations are prepared by the same large scale layout and photo reduction techniques common to the integrated circuit industry.

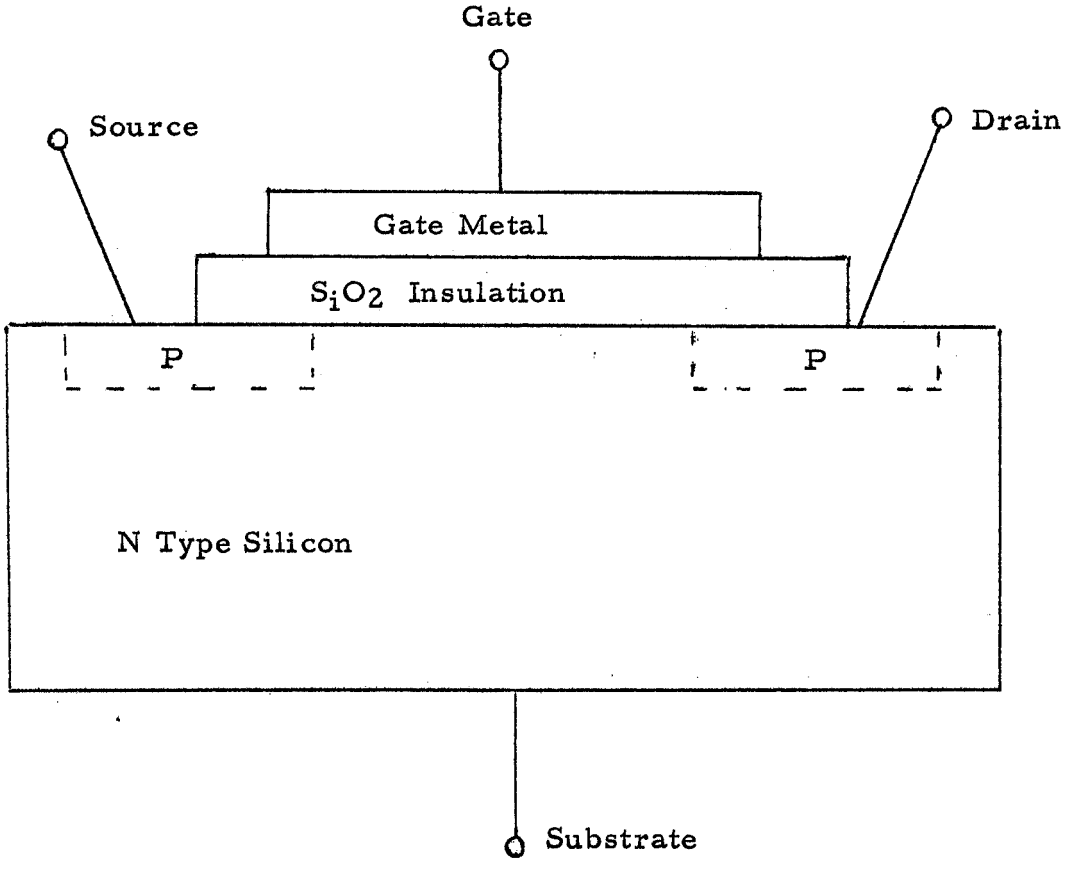

Gate
Source
Drain
Gate Metal
S_iO_2 Insulation
P
P
N Type Silicon
Substrate

Figure A1

In the MOS FET circuit (CHIP) fabrication operations used by NASA MSFC, the process of generating the four masks from a given input circuit schematic is a tedious and time consuming manual task. The individual steps in this procedure are listed below:

(1) A final circuit schematic is defined based on design requirements and breadboard results.

(2) From the schematic a topological layout is developed. This shows the location and approximate sizes of each device in the circuit along with the interconnections, crossover points, and metal to P-region contacts.

(3) Next a complete set of scaled mask layouts is developed by a draftsman.

(4) The scaled mask layouts are used to either manually cut the rubylith which is then photographically reduced to create the actual mask, or to generate an input tape for a gerber plotter which draws the mask to be photographically reduced.

The entire sequence of events listed above, including repetitions required to correct or modify the original design, can take months to complete. It is this design and mask development sequence which can be considerably improved and speeded up by utilizing a general purpose digital computer, preferably with interactive graphics capability, to support the circuit designer and to eliminate the need for an extensive drafting step.

A. 3 MOS DESIGN FUNDAMENTALS

During the course of this study effort, M&S Computing studied two distinct MOS FET design techniques.

The General Instrument's MOS LSI Design Manual describes a free form technique in which a multitude of design rules are established for the design of individual devices and for their interconnection into complete circuits. The rules, in effect, allow the design engineer to custom tailor each device and circuit component to optimize the desired circuit parameters. The GI approach allows a complete freedom of design and is ideally suited for the individual, experienced circuit designer whose primary interest is experimental design with a maximum

emphasis on optimization. However, the GI method, because of its total free form approach, is extremely difficult to implement on a computer. Far too many of the design steps in this method are based on intuition, experience, and subjective reasoning.

The second method investigated was a method described by Philco-Ford which allows for the design of large scale arrays with standardized cells. The procedure is similar to breadboarding conventional integrated circuits. The complete circuit is laid out using the standard circuit cells and well defined rules govern component interconnection and circuit geometry. The major concern of the designer with this approach is on optimizing cell interconnects. A functioning circuit can be laid out without considering the order in which blocks feed into each other. However, the number of crossovers and often the chip area as well can be minimized by grouping together, insofar as possible, cells that interconnect. The method described by Philco-Ford is ideally suited to computer assistance.

The primary disadvantage of this technique is that the circuit designer must work with standardized cells, the arrangement and interconnection of which is governed by rigid and formalized rules. This, of course, prevents the designer from completely optimizing all circuit devices and forces him to work with a circuit format somewhat less convenient than his normal schematic.

A.3.1 MOS Cell Specification

As stated previously, the Philco-Ford concept of utilizing "building blocks" or standardized cells as circuit components defines a circuit design technique which lends itself well to automation. The techniques presented in this study are based on that concept in an expanded form which liberalizes some of the design rules.

The cell, as defined for this study, is a circuit device or group of devices, including component interconnects which has been established as a standardized circuit element. Examples of cells are inverters, NOR gates, output buffers, one bit shift registers, etc. From the designers viewpoint, a cell consists only of a circuit component with well defined inputs and outputs, operating characteristics, and a symbolic representation. To the computer a cell is considerably different. This can best be demonstrated by an illustration.

Figure A2 shows the schematic and logical representation of a MOS FET inverter cell constructed of two devices where V_{DD} is the drain voltage, V_{GG} is the gate voltage, V_G is ground, and A and B are respectively the logical input and output for the cell. Three symbolic layouts for the inverter cell are shown in Figure A3. The primary difference between the various forms is their acceptability for computer representation and the number of data words required to construct each graphically. The particular symbolic layout most compatible with efficient computer storage techniques is shown in Figure A3(c) and will be discussed in detail later.

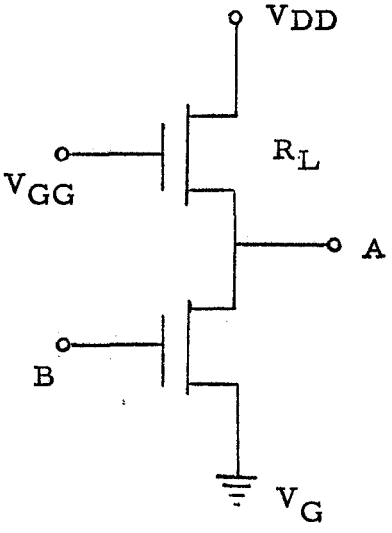
To construct circuits the designer only needs to know the symbolic representation of the available cells and the rules for component interconnection and circuit geometry. The computer needs to know considerably more.

Since the primary objective of the computer is to construct the output tapes required for manufacturing the four fabrication masks, the definition of a cell to the computer consists not only of the cell's symbolic representation but also of its mask representations. A complete cell representation for the basic inverter is presented in Figures A4 through A6. On the topological layout of Figure A4, dashed lines are used to represent metal circuit paths, solid lines represent diffused P-regions except for the cell border, solid dots show connections of metal to P-regions, and small circles indicate cell contact nodes for circuit interconnection. As can be seen by examining Figures A5 and A6, there is an almost direct correspondence between the solid lines on the topological layout and the diffusion mask, the dashed lines and the metalization mask, and the solid dots and the contact mask.

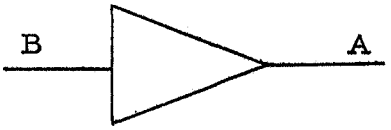
The cell representation is maintained in the computer storage area as a data set of points and vectors. Each of the four masks and the symbolic representation of the cell is stored independently and computer cell definition is synonymous with the five data tables that make up the cell's data set. A detailed description of these data tables and their use is presented in Section A. 5.

Two symbolic representations of an arbitrary cell are shown in Figure A7 and certain standardization rules have been established concerning its organization:

INVERTER



Schematic



Logic

Figure A2

TYPICAL STANDARD CELL REPRESENTATION

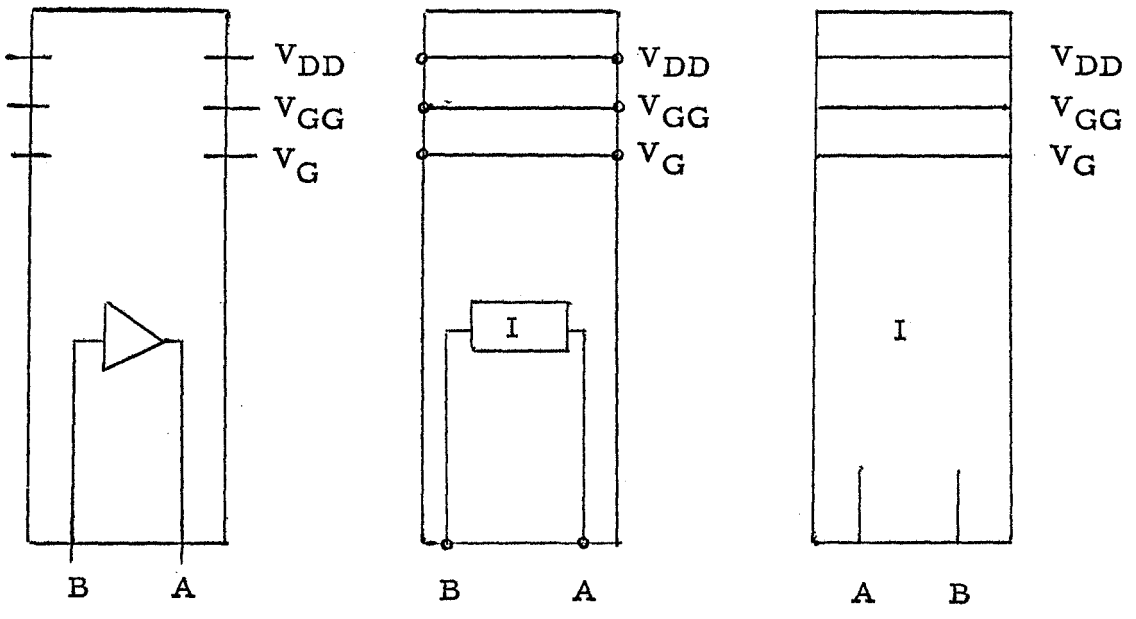
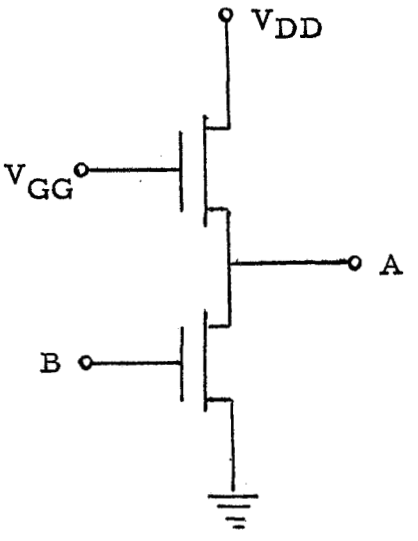
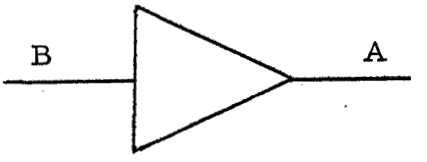


Figure A3

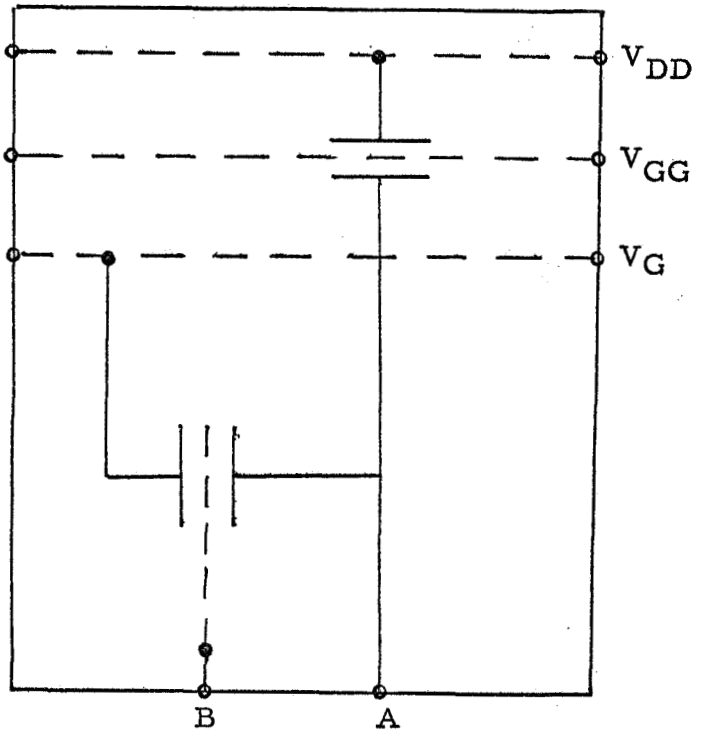
INVERTER CELL



Schematic Layout



Logic Layout



Topological Layout

Figure A4

Diffusion Mask

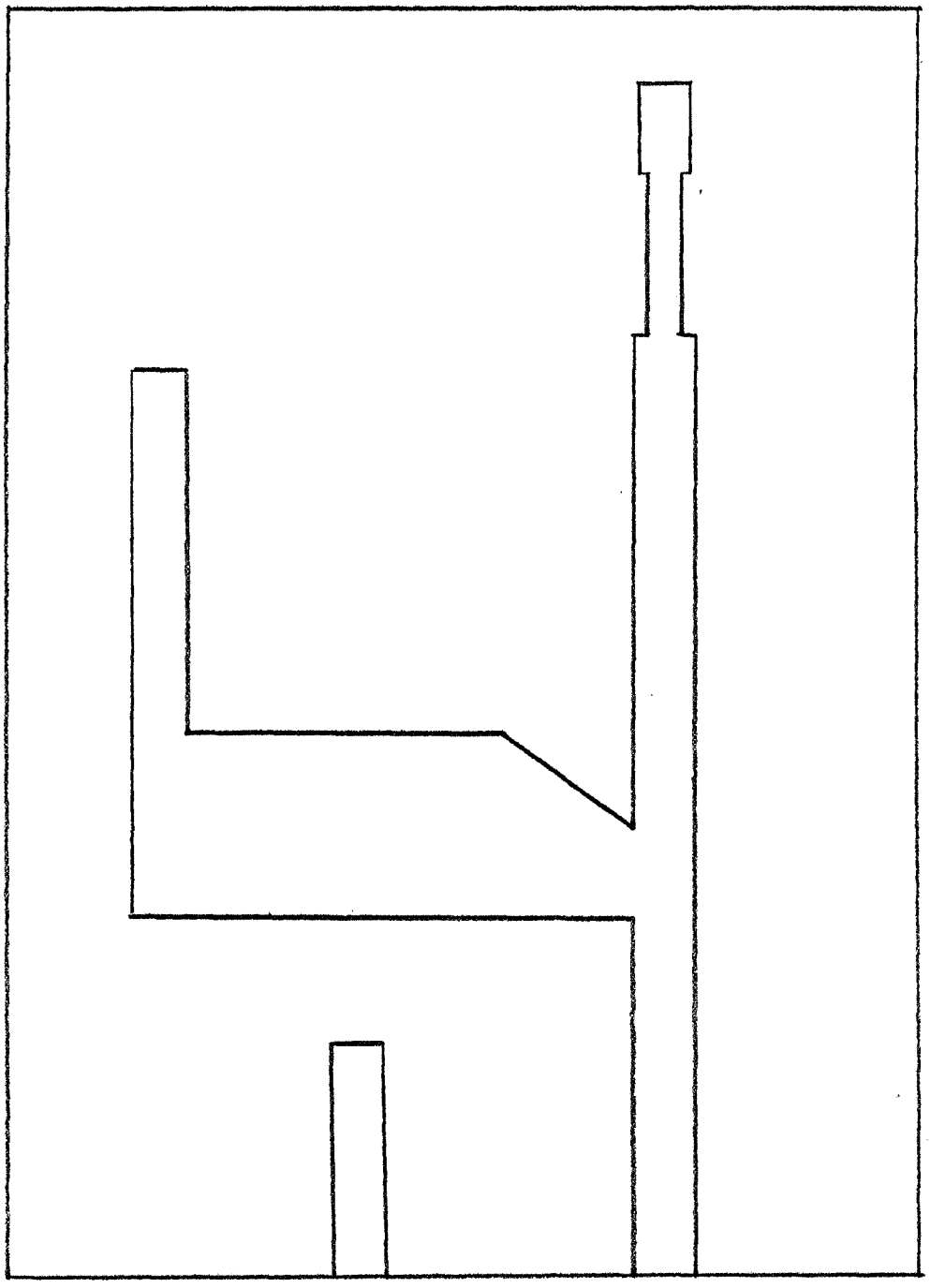


Figure A5(a)

Gate Mask

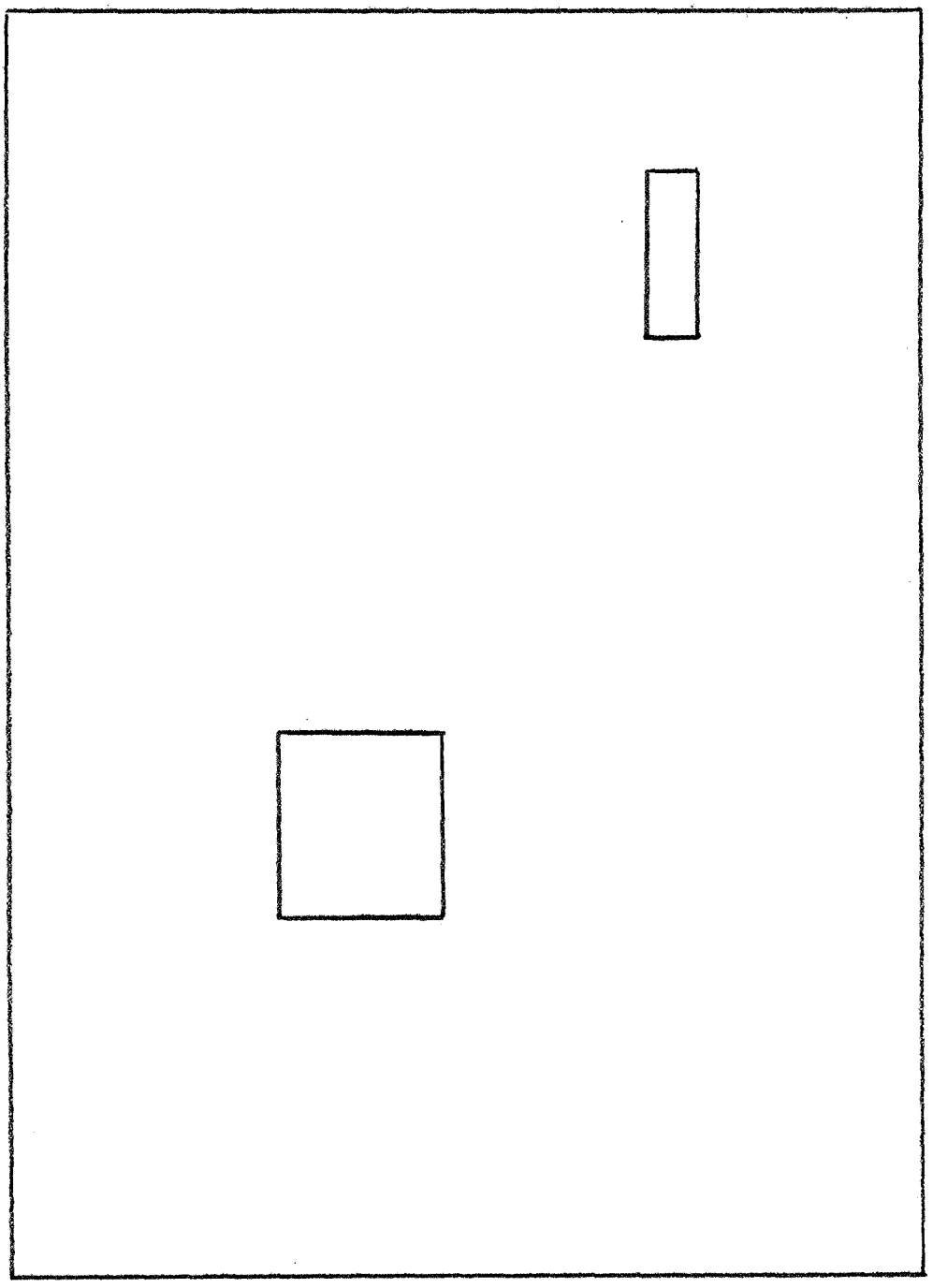


Figure A5(b)

Contact Mask

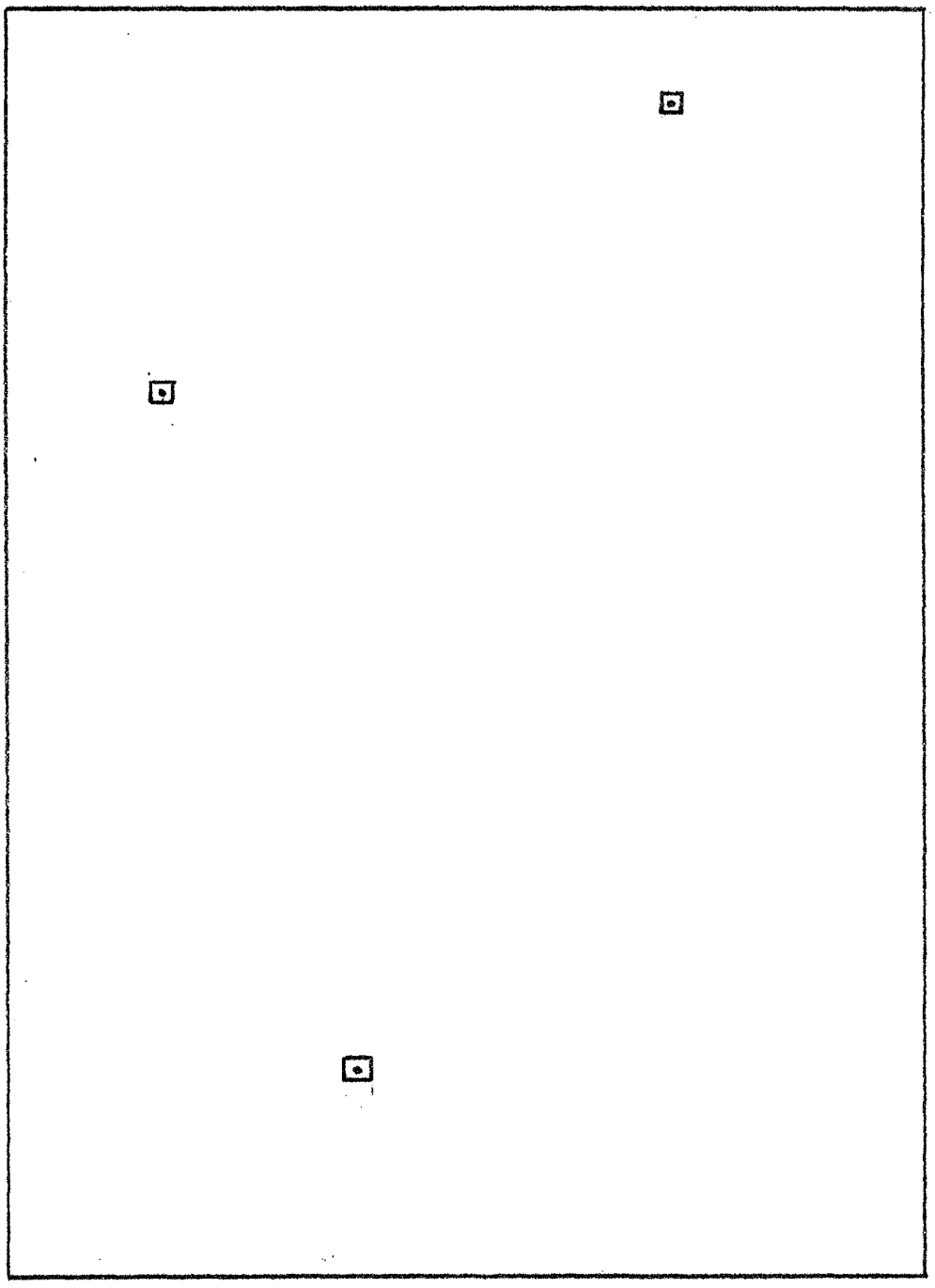


Figure A6(a)

Metalization Mask

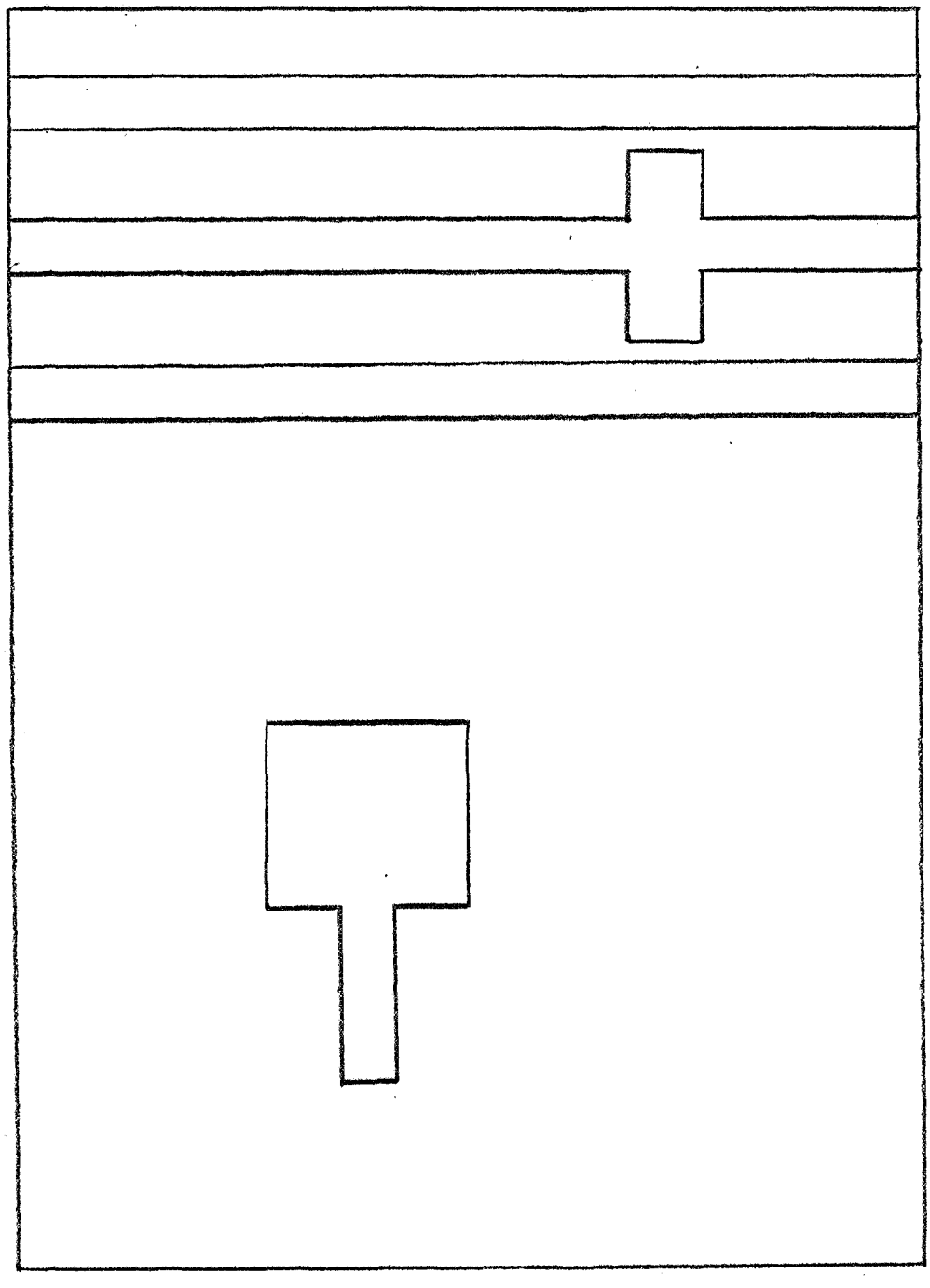
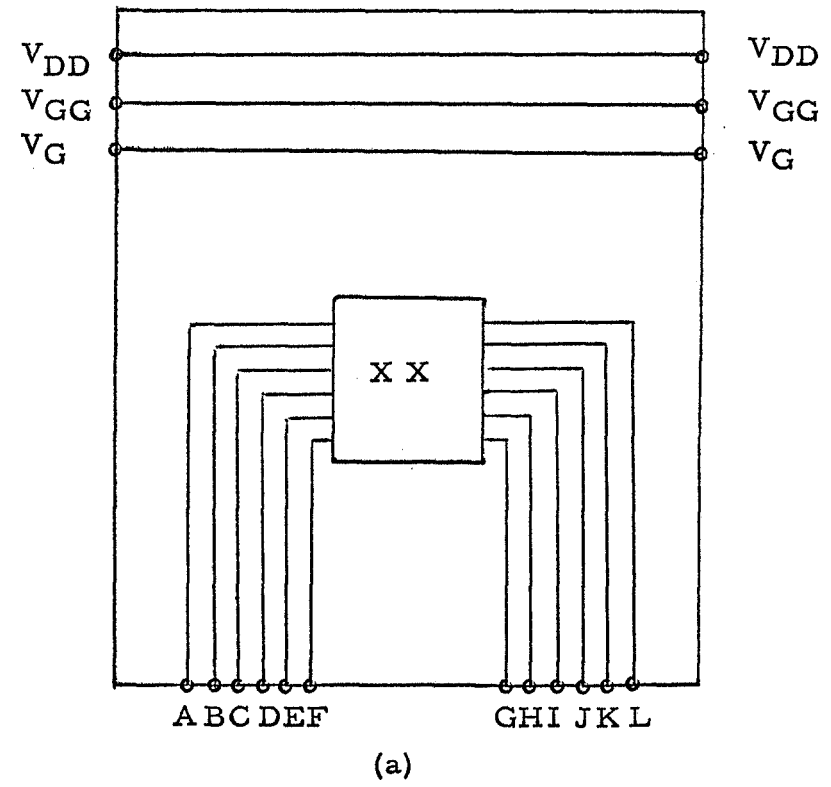
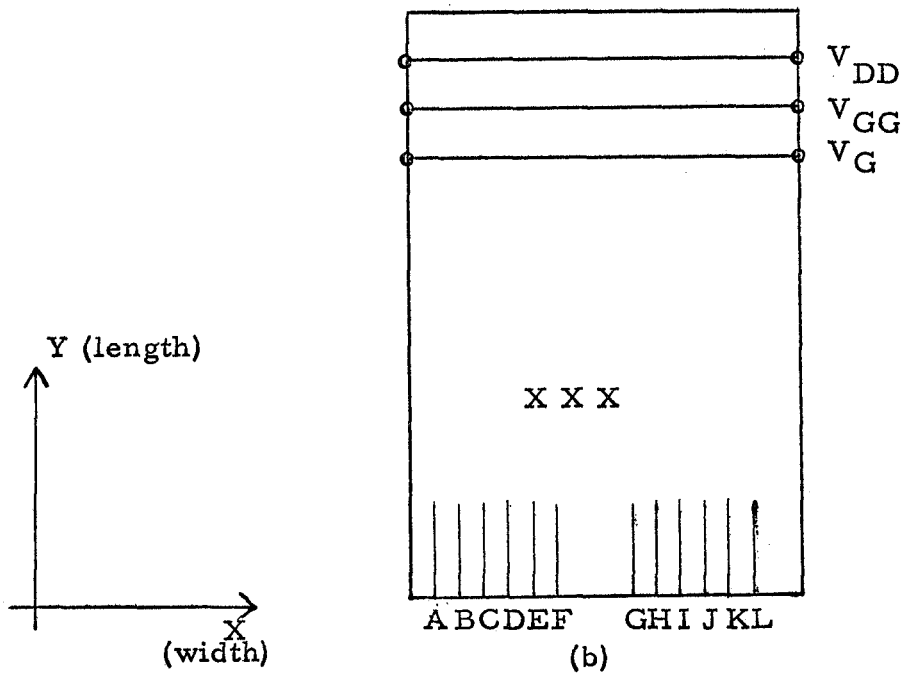


Figure A6(b)

BASIC CELL



(a)



(b)

Figure A7

(1) Power supply lines (V_{DD}, V_{GG}, and V_G) run through each cell horizontally at fixed locations and are metal.

(2) All cells have a standard length (Y-dimension) and a variable width (X-dimension) dependent upon cell function.

(3) All cell logical inputs and outputs enter or leave the cell from the bottom. In rare instances a logical I/O line may be routed to the top of a cell but never to the side.

(4) In general, all cell logical inputs and outputs will be P-region signal lines. (In the future it may be necessary to define a metal I/O but such a need will complicate computer cell definition and should be avoided if at all possible.)

A.3.2 Chip Circuit Specification

The term circuit in this study report refers to a collection of cells, cell interconnections, and bonding pads all located on a single silicon chip. With the building block approach, the circuit designer is primarily concerned with cell and bonding pad alignment, component interconnection, and circuit geometry.

Figure A8 shows the symbolic representation of a typical MOS FET circuit constructed with standardized cells of the type described in Section A.3.1. The boxes around the perimeter of the figure represent circuit bonding pads. The other symbolic conventions used are identical to those described in Section A.3.1 for the topological layout.

As stated earlier, to construct circuits the designer only needs to know the symbolic representation of the available cells and the rules for establishing component interconnection. The circuit information needed by the computer is analogous to the information that is required to define a cell.

The definition of a circuit to the computer consists of the symbolic representation of the components used to represent the circuit. This includes cells, bonding pads, nodes, contacts, and contact nodes. A node differs from a contact node in that it only allows two or more straight line interconnection paths of the same material to join. A contact node joins two or more interconnections of mixed materials (metal and P-region).

Typical Circuit

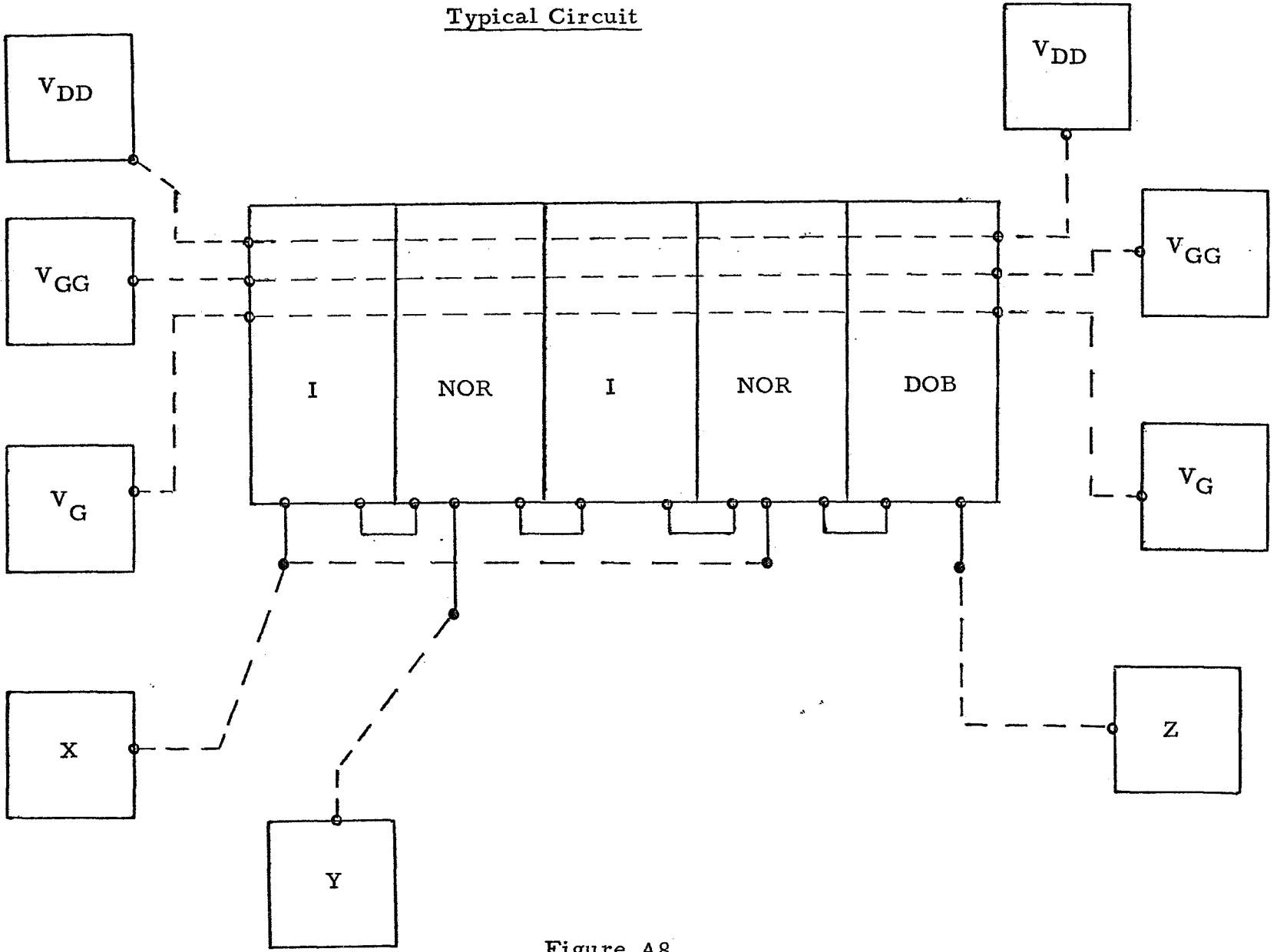


Figure A8

As with the individual cell, the computer is responsible for maintaining the circuit symbolic representation as well as the four mask layouts. In this case, the mask layouts are an overlapped composite consisting of the individual cell masks for those cells specified for this circuit and the individual masks for each specified bonding pad, metal or P-region interconnect, and contact.

The circuit representation is maintained in the computer storage area as a data set similar to those necessary to represent cells. The only difference is that the circuit data set's component coordinates are oriented to a chip grid system whereas individual cell definition data sets use a relocatable grid coordinate system with the origin located at the cell's lower left hand corner.

Circuit definition and construction is also governed by the following standardization rules necessary to permit computer participation in the design steps:

(1) Cells will be arranged in a horizontal fashion with vertical boundaries aligned.

(2) Multiple rows of cells may be employed if proper care is taken to protect against crossover shorts.

(3) In general, metal lines will run horizontally and P-region lines will run vertically to reduce the possibility of crossover problems.

(4) Metal lines should be used whenever possible to minimize line resistance and capacitance.

(5) Metal lines must be used for V_{DD}, V_{GG}, and V_G; and for all bonding pad connections.

(6) Each pin on a block will have only a single path attached to it. Multiple connects will be through an external node.

(7) Each bonding pad will have only a single path attached to it. Multiple connects will be through external nodes.

The above rules constitute a baseline set and may be revised if appropriate care is taken in analyzing the impact on computer operation.

Both the Philco-Ford manual and the GI manual list a voluminous number of specific design rules which have not been discussed in this section. One of the primary advantages of computer assisted design is that the computer will assume responsibility for properly implementing the detailed device design procedures if the circuit is constructed from defined cells properly linked. The designer's primary responsibility will be for establishing the desired circuit geometry.

A.4 MAN/COMPUTER INTERFACE

Since the primary user of this system will be a designer/engineer rather than a computer specialist, it is extremely important that the man/computer interface be user rather than programmer oriented. The ideal system would provide a graphics terminal to establish efficient two-way communication between the designer and the system, and a communication language which allows the designer to define his inputs in a familiar terminology suited to his particular problem.

Many of the problems encountered in the creation of a proper support system in which interactive graphics systems may operate are not unique to graphics applications. Rather, these problems are common to all interactive (conversational) systems. They are, however, accentuated by the graphic display console which, because of its ability to display much information rapidly, causes the user to become impatient with any system that cannot provide a response commensurate with its speed.

For this reason the man/computer interface was developed in two phases. The first phase assumed the existence of a graphics terminal and defines the basic conversational interface with the terminal as an essential component.

The second phase extrapolated the basic man/computer interface defined in phase one to a system which does not contain a graphics terminal. The primary objective was to establish an interface which, while not initially requiring a graphics display, could be easily expanded to include one with no major design modifications.

The minimum graphics terminal configuration required for this task would consist of a CRT display unit, a typewriter keyboard, and a light pen or gun. The typewriter keyboard will allow the user to transmit alphanumeric characters and special symbols to the system and to the graphic display. The light gun allows the user to identify particular display (X, Y) coordinates of which he wishes the system to be aware.

The system which has been developed for this application should be readily applicable to any display terminal which has a control light pen or gun and is capable of displaying vectors and alphanumeric characters.

Figure A9 presents a representation of the CRT screen layout for this application. It should be noted that the screen has been partitioned into four distinct areas.

The working area represents the silicon chip area upon which the desired circuit will be constructed. As the design task proceeds, this area will contain the symbolic representation of the circuit under consideration.

The element area portion of the CRT is used to provide an immediate response to the operation action of specifying a circuit element. Legitimate circuit elements are: defined circuit cells, bonding pads, contact nodes, and nodes. When an element is specified, its symbolic representation is immediately displayed in the element display area. It may be rotated, if necessary, and then transferred to the working area of the screen by either the "translate" or the "align" instructions.

The message area provides a display area on the screen which the system may use to communicate with the user. Possible uses are error messages to notify the user of illegal operations, system status messages, etc.

The command keyboard is a portion of the display which is sensitive to light gun activity. It is further subdivided as shown in Figure A10. Each small block, when touched by the light gun, will implement the command specified by that block. Blank blocks are current spares. Table A1 presents a detailed definition of the current instruction list and relates the instructions to the symbols used on Figure A10.

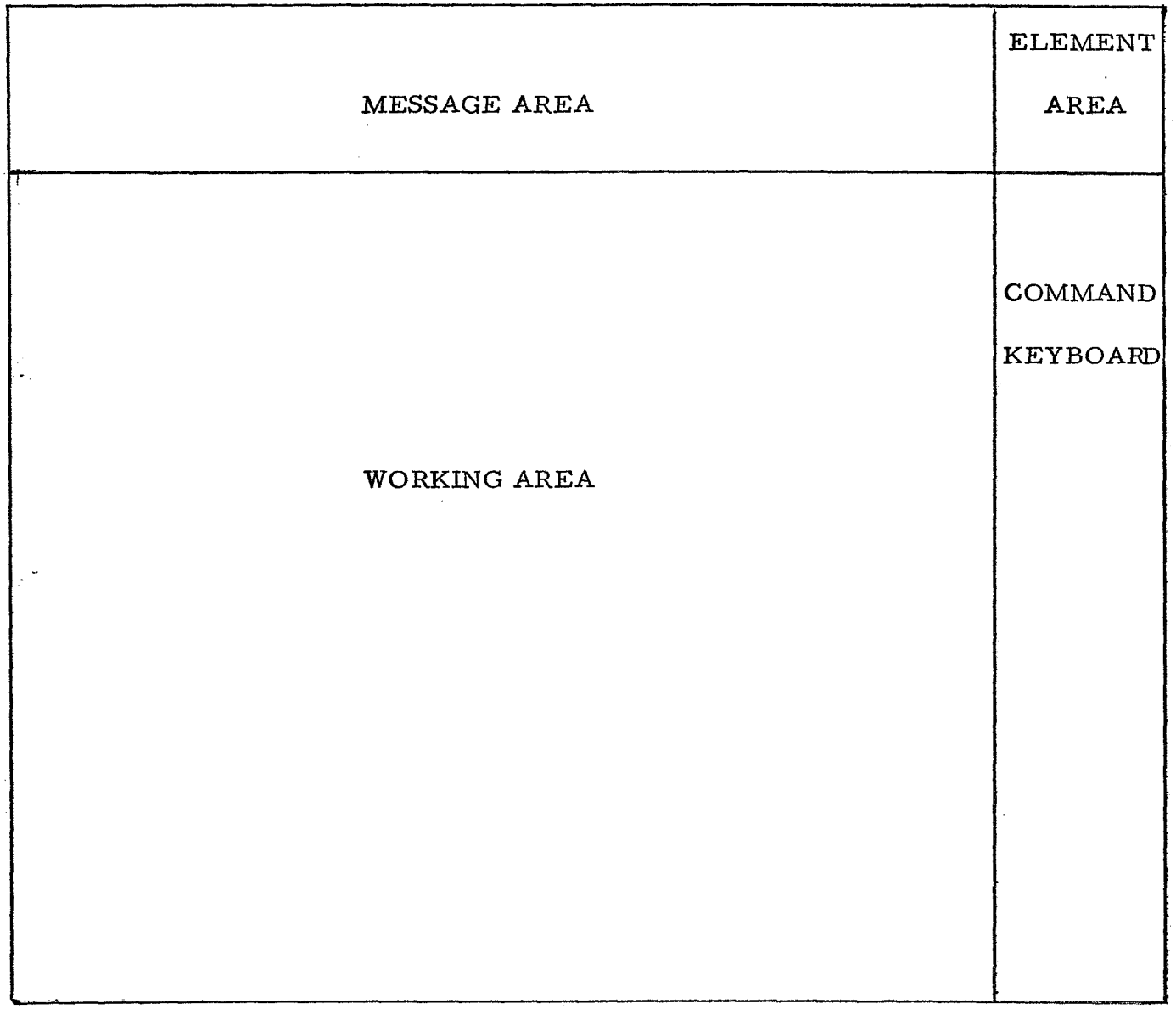


Figure A9

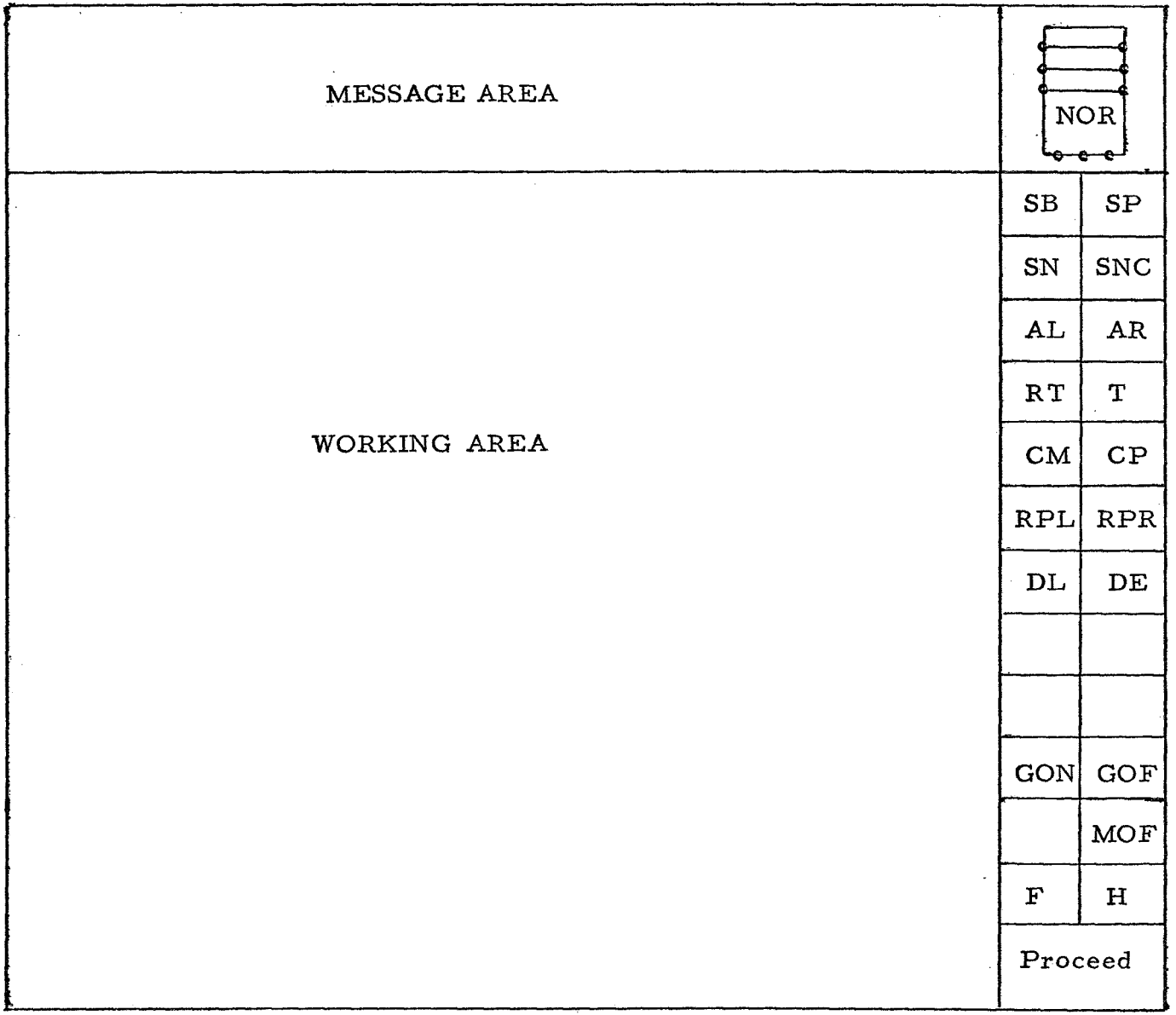

MESSAGE AREA
NOR
WORKING AREA
SB
SP
SN
SNC
AL
AR
RT
T
CM
CP
RPL
RPR
DL
DE
GON
GOF
MOF
F
H
Proceed

Figure A10

OPERATION CODES

Symbol	Definition	
SB	Specify a Circuit Block (defined cell)	As a result of any specify operation, the specified element appears in the element area of the display.
SPC	Specify a Corner Pad	
SP	Specify a Side Pad	
SN	Specify a Node	
SCN	Specify a Contact Node	
AL	Align Block Left - This instruction will align the block specified by the previous operation and currently in the element area with the left hand boundary of a currently existing chain of cells in the working area. The user must indicate with the light gun the left hand border of the desired chain.	
AR	Align Block Right - Same as AL except system will align on the right boundary of an existing chain.	
RT	Reset - This instruction will reset the screen and allow the designer to restart his circuit.	
CM	Connect Metal - If the user next indicates two nodes (or contact nodes) in the working area, the system will connect them with a metal path (dashed line).	
CP	Connect P-Region - Same as CM above except that the system will connect the indicated nodes with a P-region path (solid line).	
T	Translate - This instruction will allow the operator to move an element area to the working area by touching the desired (X, Y) coordinates in the working area with the light gun.	
RPL	Rotate Pad Left - Every time this instruction is touched, the pad in the element area will be rotated counter-clockwise 90°.	

Table A1

Symbol	Definition
DL	Delete Line - Allows the operator to eliminate the interconnection line touched by the light gun.
DE	Delete Element - Allows the operator to eliminate the element touched by the light gun and all of its interconnections.
GON	Grid On - This instruction allows the operator to grid the working area.
GOF	Grid Off - Allows the operator to turn the grid off.
F	File - This instruction allows the operator to record in a library for later reference the data sets describing the circuit currently in the working area.
H	Hardcopy - This instruction allows the operator to obtain a hard copy of the working area.
MOF	Message Off - This command will blank the message area of the display.
Proceed	Proceed - Indicates to the system that the design in the working area is complete and that the system should begin deriving the required output to generate the four masks.

Table A1. (continued)

To illustrate how this system is to be used, the circuit of Figure A8 will be constructed in the working area using the defined instructions. Figure A11 is identical to Figure A8 except that nodes, blocks, and pads are numbered to simplify the illustration. Pads are numbered from 1 to 9 starting at V_{DD} in the upper left and proceeding in a counter-clockwise manner. Cells are identified by their symbol and a repetition number which is assigned by the computer as the cell is specified. The repetition number is indicative of the number of times the same standard cell has been used in the circuit. In order to uniquely identify a particular cell or pad in a circuit, both its code number and repetition number must be known.

Nodes have been arbitrarily numbered as specified. The number and letters in parenthesis would not be visible on the screen but are analogous to the numbering scheme used by the system to keep track of circuit elements.

A detailed instruction list for the circuit of Figure A11 has been developed in Table A2. The nomenclature used is oriented about the numbering convention utilized in Figure A11. For the sake of simplicity, the following conventions have been used in Table A2:

(1) "SB-I(1)" - This is the specification of Block I, Repetition Number (1).

(2) "N(4)" is Node # 4.

(3) "CM-(P1)(N1)" is read "Connect Metal from Pad 1 to Node #1".

(4) "CP-(N9)(NOR2, 2)" is read "Connect P-Region from Node #9 to NOR Cell Repetition #2, Pin #2."

(5) Cell logic pins are numbered from 1 to n starting at the lower left hand corner.

(6) Cell chain power supply nodes are labeled A, B, C (Left) and A, B, C (Right); for example, BR is node B right.

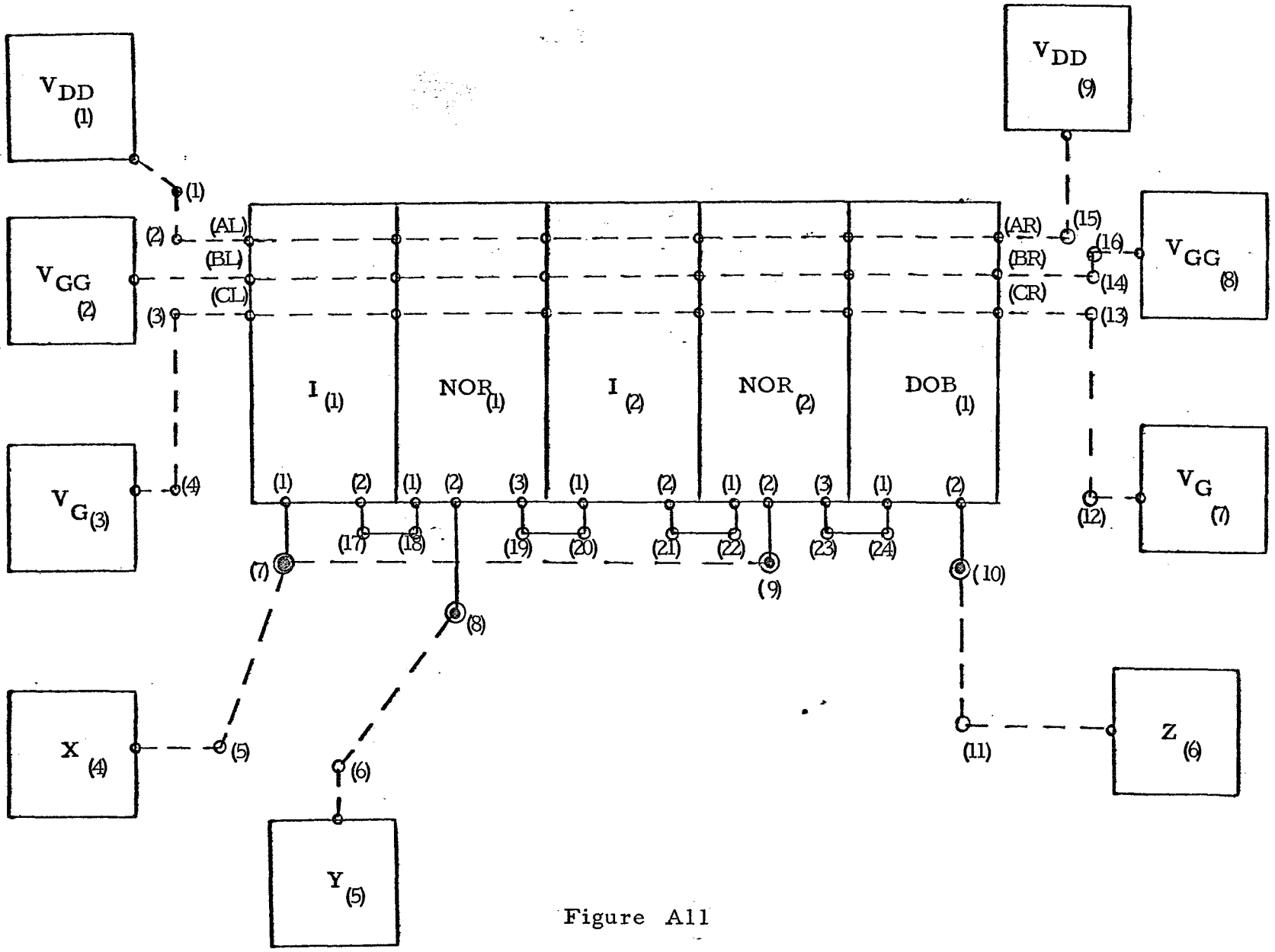

V_{DD} (1)
V_{GG} (2)
V_G (3)
X (4)
Y (5)
V_{DD} (9)
V_{GG} (8)
V_G (7)
Z (6)
(AL)
(BL)
(CL)
(AR)
(BR)
(CR)
$I_{(1)}$
$NOR_{(1)}$
$I_{(2)}$
$NOR_{(2)}$
$DOB_{(1)}$

Figure A11

CIRCUIT INSTRUCTION LIST

1	SB-I(1)	23	RPR	45	SN-N(5)
2	T-(X, Y)	24	T-(X, Y)	46	T-(X Y)
3	SB-NOR(1)	25	SP-V_{GG}(8)	47	SN-N(6)
4	AR-I(1)	26	RPR	48	T-(X, Y)
5	SB-I(2)	27	RPR	49	SCN-N(7)
6	AR-NOR(1)	28	T-(X, Y)	50	T-(X, Y)
7	SB-NOR(2)	29	SP-V_G(7)	51	SCN-N(8)
8	AR-I(2)	30	RPR	52	T-(X, Y)
9	SB-DOB(1)	31	RPR	53	SCN-N(9)
10	AR-NOR(2)	32	T-(X, Y)	54	T-(X, Y)
11	SPC-V_{DD}(1)	33	SP-Z(6)	55	SCN-N(10)
12	T-(X, Y)	34	RPR	56	T-(X, Y)
13	SP-V_{GG}(2)	35	RPR	57	SN-N(11)
14	T-(X, Y)	36	T-(X, Y)	58	T-(X, Y)
15	SP-V_G(2)	37	SN-N(1)	59	SN-N(12)
16	T-(X Y)	38	T-(X, Y)	60	T-(X, Y)
17	SP-X(4)	39	SN-N(2)	61	SN-N(13)
18	T-(X, Y)	40	T-(X, Y)	62	T-(X, Y)
19	SP-Y(5)	41	SN-N(3)	63	SN-N(14)
20	RPL	42	T-(X, Y)	64	T-(X, Y)
21	T-(X, Y)	43	SN-N(4)	65	SN-N(15)
22	SP-V_{DD}(9)	44	T-(X, Y)	66	T-(X, Y)

Table A2

67	SN-N(16)	90	CM-(N4)(N3)	113	CP-(N18)(NOR1, 1)
68	T-(X, Y)	91	CM-(N3)CL)	114	CP-(NOR1, 3)(N19)
69	SN-N(17)	92	CM-(P4)(N5)	115	CP-(N19)(N20)
70	T-(X, Y)	93	CM-(N5)(N7)	116	CP-(N20)(I2, 1)
71	SN-N(18)	94	CP-(N7)(I1, 1)	117	CP-(I2, 2)(N21)
72	T-(X, Y)	95	CM-(N7)(N9)	118	CP-(N21)(N22)
73	SN-N(19)	96	CP-(N9)(NOR2, 2)	119	CP-(N22)(NOR2, 1)
74	T-(X, Y)	97	CM-(P5)(N6)	120	CP-(NOR2, 3)(N23)
75	SN-N(2	98	CM-(N6)(N8)	121	CP-(N23)(N24)
76	T-(X, Y)	99	CP-(N8)(NOR1, 2)	122	CP-(N24)(DOB1, 1)
77	SN-N(21)	100	CM-(P6)(N11)	123	Proceed
78	T-(X, Y)	101	CM-(N11)(N10)		
79	SN-N(22)	102	CP-(N10)(DOB1, 2)		
80	T-(X, Y)	103	CM-(P7)(N12)		
81	SN-N(23)	104	CM-(N12)(N13)		
82	T-(X Y)	105	CM-(N13)(CR)		
83	SN-N(24)	106	CM-(P8)(N16)		
84	T-(X, Y)	107	CM-(N16)(N14)		
85	CM-(P1)(N1)	108	CM-(N14)(BR)		
86	CM-(N1)(N2)	109	CM-(P9)(N15)		
87	CM-(N2)(AL)	110	CM-(N15)(AR)		
88	CM-(P2)(BL)	111	CP-(I1, 2)(N17)		
89	CM-(P3)(N4)	112	CP-(N17)(N18)		

Table A2 (continued)

The following steps summarize the operator's responsibilities and describe the results to be observed in response to particular operator actions. The operations of Table A2 which perform each step have been identified in order to clarify the operation.

(1) Cell I(1) is specified by touching the SB instruction and keying an I on the typewriter keyboard. The symbol for this block will appear in the element area. The cell is then translated to the working area by touching the desired (X, Y) coordinates with the light gun. (Operations (1) and (2))

(2) Cell NOR (1) is then specified and aligned with Cell I(1) by first specifying the NOR Cell and by then touching the AR instruction and the right hand border of Cell I(1). (Operations (3) and (4))

(3) The remaining cells are specified and aligned in a similar manner. (Operations (5) through (10))

(4) Pads are specified like cells and first appear in the element area. They can then be rotated if desired using the RPR and RPL instructions. They are then translated to the desired portion of the working area in the normal manner. (Operations (11) through (36))

(5) Nodes and contact nodes are specified and positioned just as the pads and cells were above. (Operations (37) through (84))

(6) Signal and power paths of either metal or P-region are established by first commanding either the "CM" or the "CP" instruction and then touching with the light gun the two nodes between which the contact is to be made. (Operations (85) through (122))

(7) Once the circuit has been fully wired, the system is commanded to "proceed" which terminates the design phase. At this point the system will perform a final error analysis to insure that all nodes have been accounted for and properly connected. (Operation 123)

The above described technique is, of course, ideally suited to operation on a graphics terminal equipped with a light gun or pen. It has been estimated that the circuit of Figure A11 could be constructed in the work area of the display by an experienced designer in about three and one-half minutes.

A close examination of Table A2 will show that the data needed by the computer to represent this circuit could have been supplied on cards using exactly the same instruction set as used in the graphics mode. In the case of card inputs, the information previously supplied to the system by pointing the light gun, (X, Y) coordinates, and signal path interconnect end points, could be provided as instruction operands.

A systematic design approach without a display would be for the designer to sketch, not draft, onto graph paper a schematic of the desired circuit. The grid used should be equivalent to that used for the display working area. Such a sketch would be equivalent to that shown in Figure A8. He would then number all pads, nodes, and pin numbers and assign repetition numbers to the cells. The results would be similar to the drawing in Figure A11. From such a drawing the designer can code directly the instructions needed by the computer to represent the circuit. The cards would then contain statements of the form shown in Table A2.

As can be seen from Table A2, 123 instructions or operations are required to define the circuit of Figure A11. In the card input mode, the number of discrete operations can be significantly reduced and simplified if a statement format such as that of Table A3 is used.

The statement format operation set is very similar to the original graphics operation set. The primary difference being that specifications and translation are done in one step. Signal paths of a single material are also constructed by one statement regardless of the number of nodes contained in the path. In the case of the example, the circuit can be defined with 51 operations in statement format. This is a net saving of 72 operations over the discrete format nomenclature.

The primary disadvantage of the format statement is that it requires additional software to decode the statements. For this application the advantages of the format statement for non-graphic communication far outweighs the penalty incurred as a result of requiring the additional software.

STATEMENT FORMAT

1	SB-I(1), (X, Y)	
2	ALIGN R-I(1) (NOR(1), I(2), NOR(2), DOB(1))	*
3	SPC - V_{dd} (1), (X, Y)	
4	SP - V_{gg} (2), (X, Y)	
5	SP - V_{g} (3), (X, Y)	
6	SP - X(4), (X, Y)	
7	SP - Y(5), (X, Y), RPR	
8	SP - Z(6), (X, Y), RPR, RPR	
9	SP - V_{g}(7), (X, Y), RPR, RPR	
10	SP - V_{gg}(8), (X, Y), RPR, RPR	
11	SP - V_{dd}(9), (X, Y), RPL	
12	SN - N1, (X, Y)	
13	SN - N2, (X, Y)	
14	SN - N3, (X, Y)	
15	SN - N4, (X, Y)	
16	SN - N5, (X, Y)	
17	SN - N6, (X, Y)	
18	SCN - N7, (X, Y)	
19	SCN - N8, (X, Y)	
20	SCN - N9, (X, Y)	
21	SCN - N10, (X, Y)	
22	SN - N11, (X, Y)	

TABLE A3

23	SN - N12, (X, Y)
24	SN - N13, (X, Y)
25	SN - N14, (X, Y)
26	SN - N15, (X, Y)
27	SN - N16, (X, Y)
28	SN - N17, (X, Y)
29	SN - N18, (X, Y)
30	SN - N19, (X, Y)
31	SN - N20, (X, Y)
32	SN - N21, (X, Y)
33	SN - N22, (X, Y)
34	SN - N23, (X, Y)
35	SN - N24, (X, Y)
36	CM - P1, N1, N2, AL
37	CM - P2, BL
38	CM - P3, N4, N3, CL
39	CM - P4, N5, N7, N9
40	CP - N7, I(1) 1
41	CP - N9, NOR (2) 2
42	CM - P5, N6, N8
43	CP - N8, NOR (1) 2
44	CM - P6, N11, N10
45	CP - N10, DOB (1) 2

TABLE A3 (continued)

46	CM - P7, N12, N13, CR
47	CM - P8, N16, N14, BR
48	CM - P9, N15, AR
49	CP - I(1) 2, N17, N18, NOR (1) 1
50	CP - NOR (1) 3, N19, N20, I(2) 1
51	CP - NOR (2) 3, N23, N24, DOB(1) 1

* This statement is read "Align right on Block I(1) sequentially the following cells: NOR(1), I(2), NOR(2), DOB(1)."

TABLE A3 (continued)

The primary disadvantage of the non-graphic communication mode of operation is that it severely limits the amount of real time circuit design that the user can perform with the system. Such a mode is entirely satisfactory if the computer is used simply to produce the output required to manufacture the masks but is of little use for allowing the computer to aid or support the designer during the design phase.

A.5 PROCESSOR REQUIREMENTS

A.5.1 Introduction

The application software needed to perform computer assisted design can be divided into three sections: circuit design software, mask design software and support software. Since the entire task is highly data dependent, the software is primarily concerned with data manipulation and organization. A major percentage of memory and off-line storage is dedicated to maintaining the data tables needed to define a circuit schematic and its masks.

The circuit design software is responsible for conducting two-way communication with the user during the circuit design phase, performing display control, and constructing the circuit data set which defines circuit geometry.

The mask design phase is initiated by executing a "proceed" instruction. The software of this phase is responsible for performing final circuit schematic error checking and for constructing the mask data set files which define the circuit mask geometry.

The support software consists of the element dictionary, the element library and the circuit library. Since these are reference data sets rather than working tables, they do not have to be maintained in main memory. They are referenced by software in both the other phases and are discussed in detail below.

Chart A1 presents the data set organization and structure required to support the defined application. The overall task data organization is shown in Chart A1(a). It should be noted that each program phase requires its own main storage data set. Since the data requirements are substantial, this implies the possible need for an overlay software structure. Such an overlay structure is logically feasible since the program phases are relatively independent of each

TASK DATA ORGANIZATION

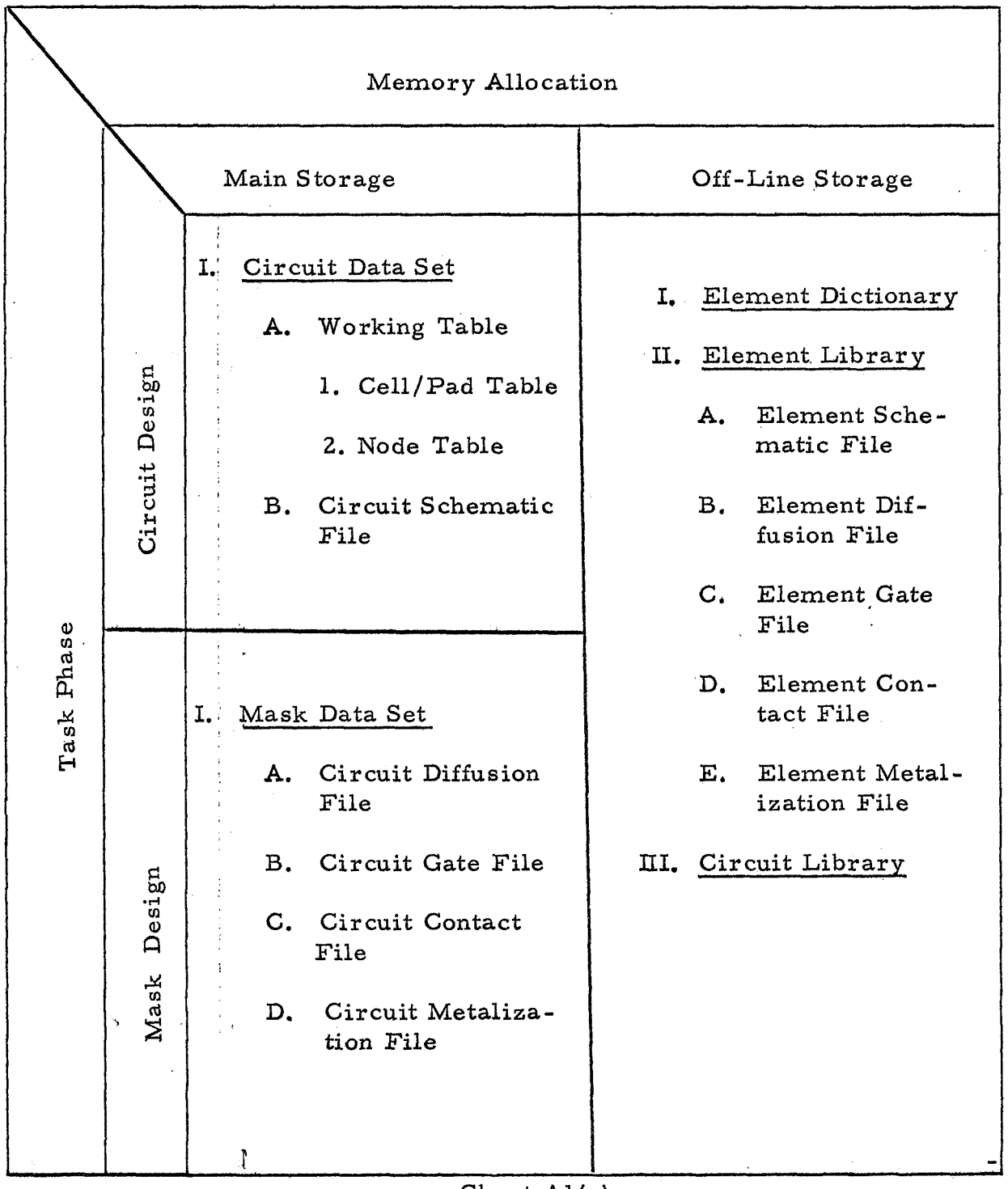


Chart A1(a)

CIRCUIT AND MASK DATA SETS ORGANIZATION

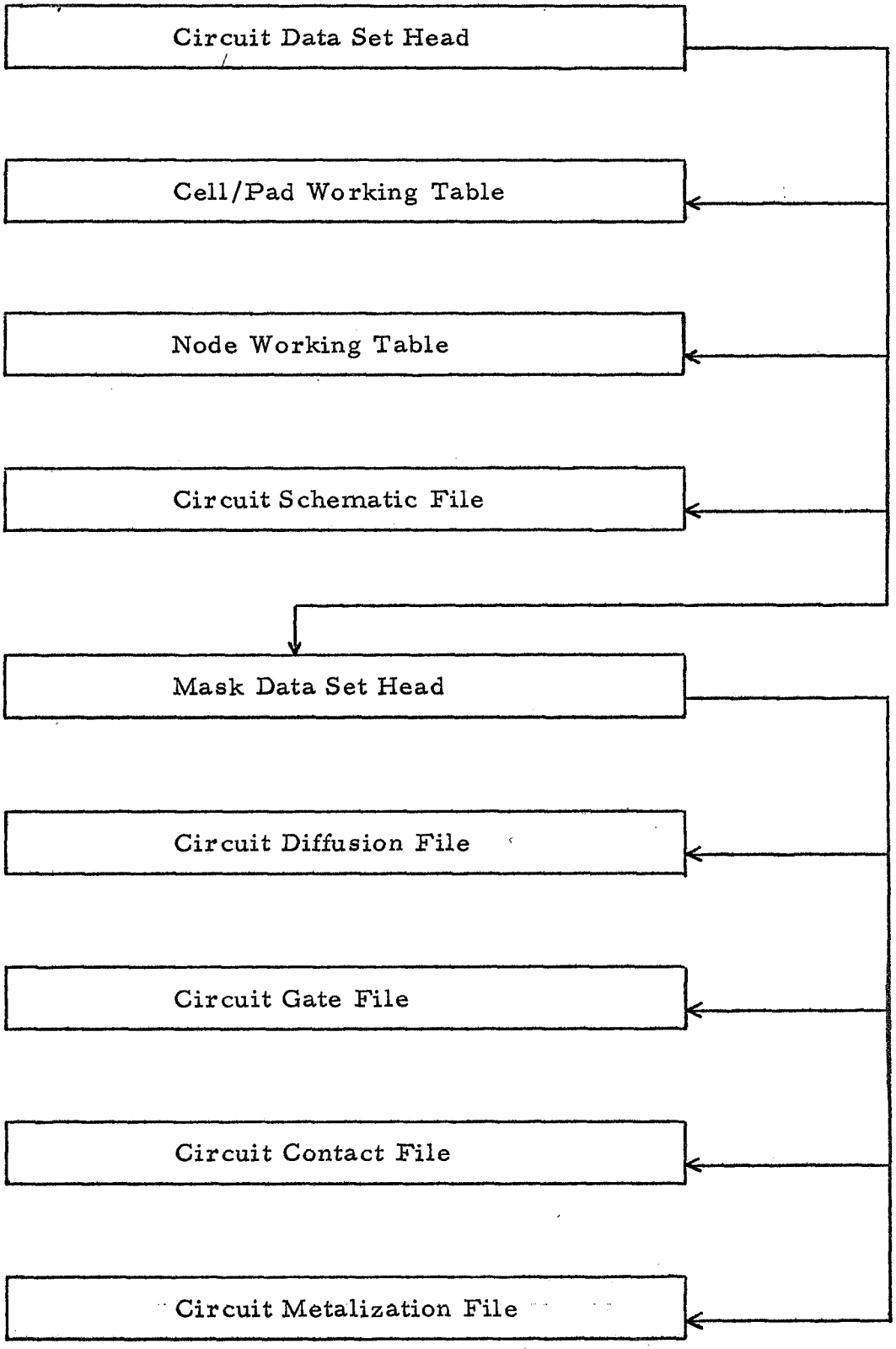


Chart A1(b)

CIRCUIT DATA SET HEAD

STRUCTURE

Circuit ID
Spare
Pointer to Cell/Pad Working Table
Pointer to Node Working Table
Pointer to Circuit Schematic File
Pointer to Mask Data Set

Chart A1(c)

other. If the computer chosen for this task has less than 25K 24 bit words of main storage memory, an overlay structure will be an absolute necessity.

A.5.2 Circuit Data Set

The circuit data set is used by the design phase software to compile the definition of the circuit elements and its schematic geometry. It is composed of two working tables (the cell/pad and node tables), and of the circuit schematic file.

The organization of the data set is presented in Chart A1(b). The data set head provides pointer information not only to the working tables and schematic file, but also to the head of the mask data set. This is necessary since the circuit data set head will act as the basic linkage between any necessary software overlays. The exact structure of the data set head is shown in Chart A1(c).

A.5.2.1 The Cell/Pad Table

The Cell/Pad Table is established when the first cell or pad is specified by the user. The table contains an entry for each circuit cell or pad and contains such information as:

(1) The element number - an eight bit identifying code which defines the type of cell or pad being specified.

(2) A repetition number - assigned by the computer on a sequential basis which represents the number of times this type of cell or pad has been used by this circuit. To locate a distinct cell or pad in a circuit requires knowledge of both its element and repetition numbers.

(3) The (X, Y) coordinates of the cell in the working area of the display which is analogous to circuit chip coordinates. All cells have been origined at their lower left hand corner. Pads have been origined at their geometric center.

(4) A six-bit indicator specifying the number of pins (cell nodes) associated with the cell - For example an inverter cell has eight pins (V_{GG} in, V_{GG} out, V_{DD} in, V_{DD} out, V_G in, V_G out, A & B). This information is obtained from the element dictionary and is used to block the number of computer words necessary for the cell record. A cell record requires a number of words calculated as follows:

Record Length = 3 + 2 (number of pins)

(5) Pin connect and Coordinate Data - Each pin of the cell or pad requires a two word entry in the record which gives the following information:

(a) The absolute pin coordinates in the working area or on the circuit chip.

(b) Interconnect information specifying the interconnect material and the other node or pin to which it connects.

(6) A pointer to the next element record in the cell/pad working table.

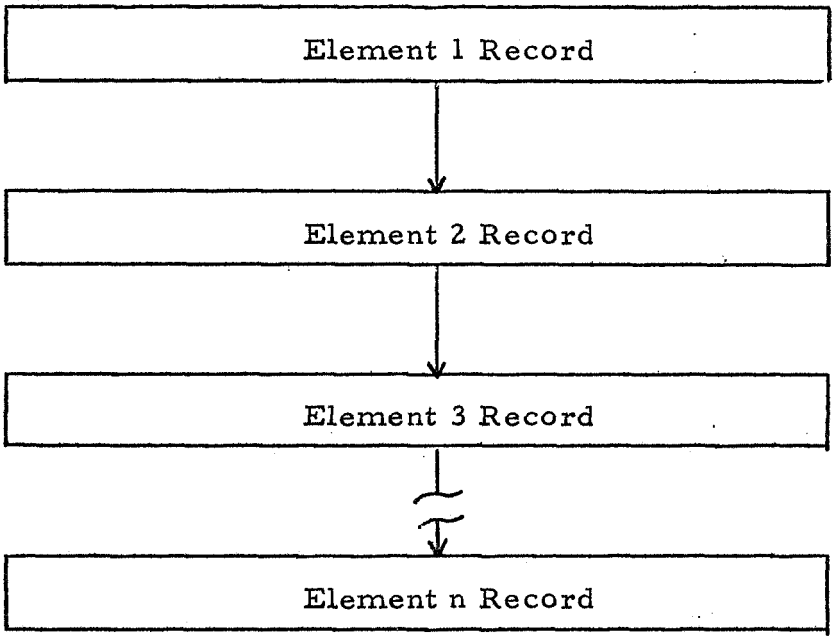
The cell/pad working table structure is presented in Chart A1(d) and the record organization is defined in Chart A1(e). Numbers in parenthesis define the number of bits required for each record entry. For definition purposes, the computer word length was assumed to be 24 bits long.

The overall record length, element identification, and the next record pointer are established during an element "specify" operation. Coordinate information and interconnect data are established through such operations as "Translate", "Align", "Connect Metal", and "Connect P-Region".

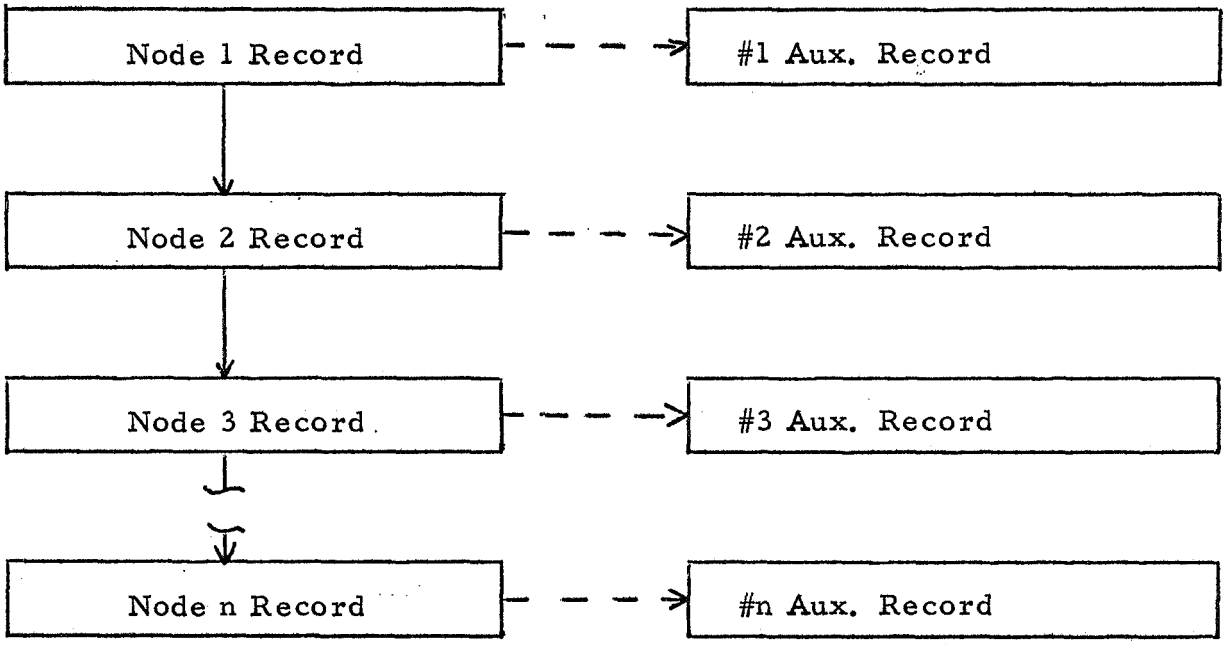
A.5.2.2 The Node Working Table

The Node Table is similar to the CELL/PAD Table and contains essentially the same type of information. The need for a separate table arises out of the requirement for a slightly different format since the overall node record length cannot be determined during the "specify" operation. The length is a function of the number of interconnects specified by "Connect" operations. A legal node must have a minimum of two interconnects but no maximum limitation currently exists. The node record length can be calculated as:

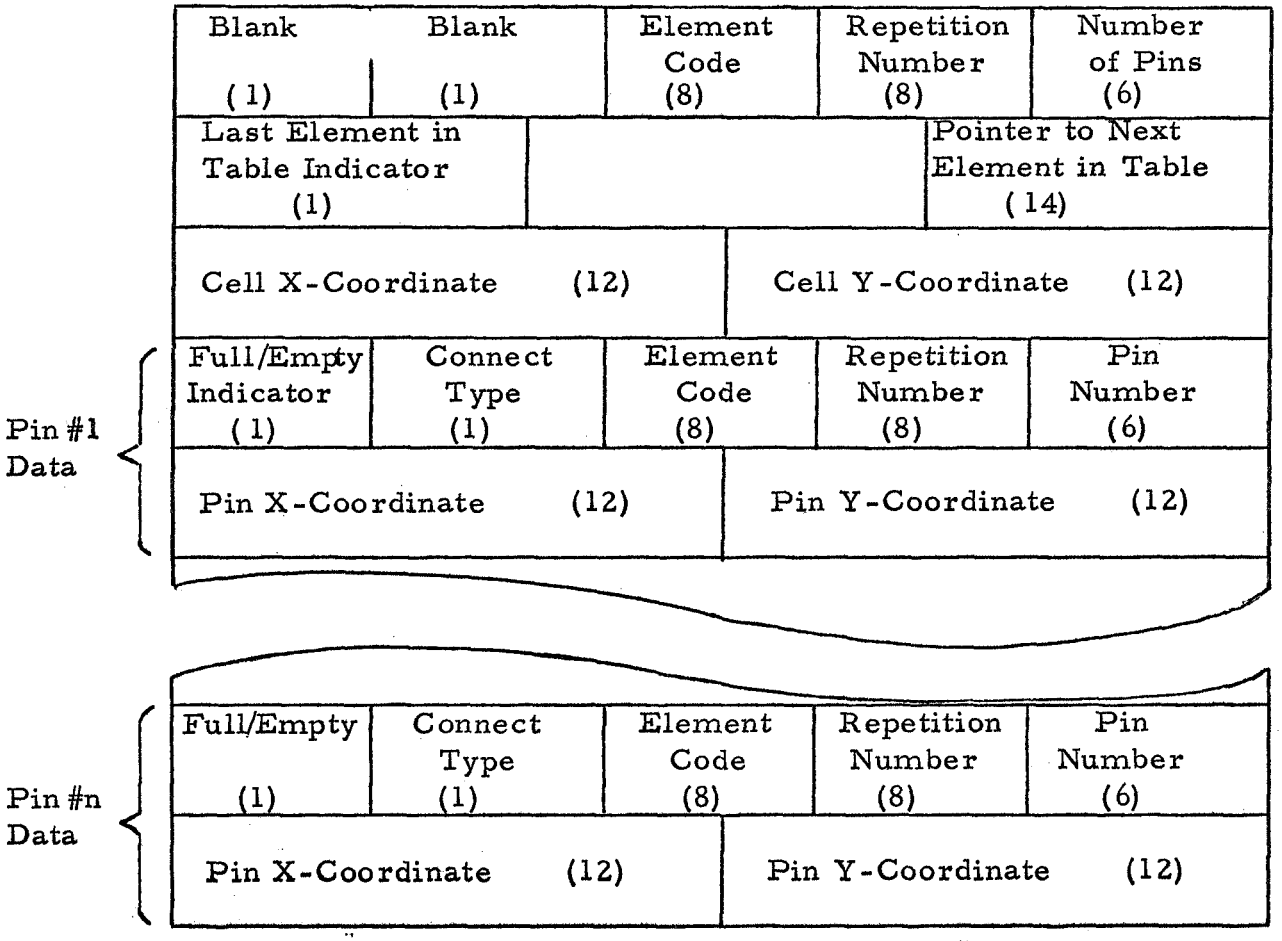
CELL/PAD WORKING TABLE STRUCTURE



NODE WORKING TABLE (STRUCTURE)



CELL/PAD WORKING TABLE
(CELL RECORD)



(PAD RECORD)

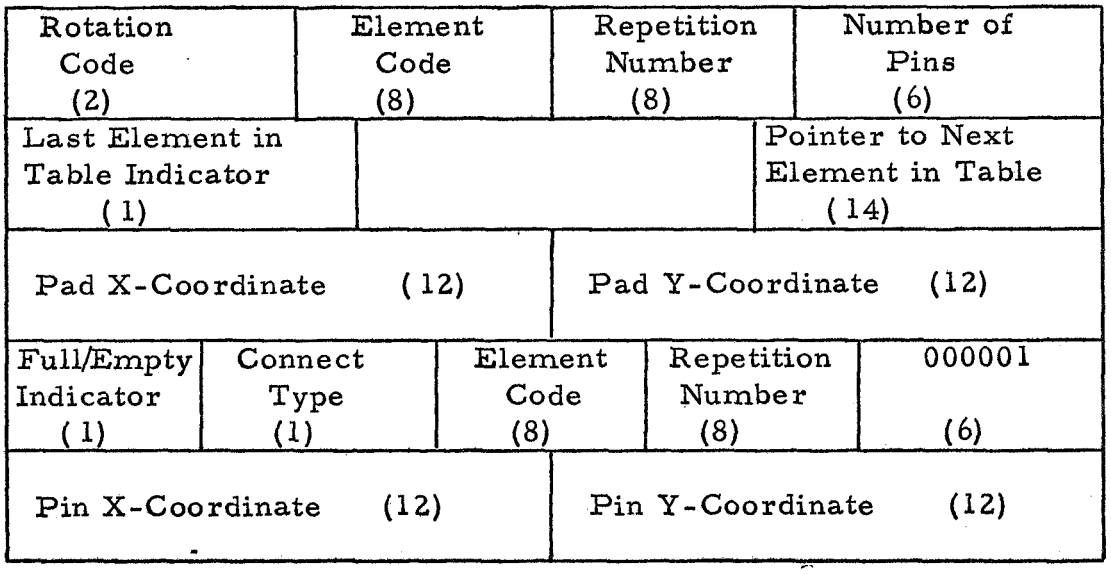


Chart A1(e)

NODE WORKING TABLE
(RECORD STRUCTURE)

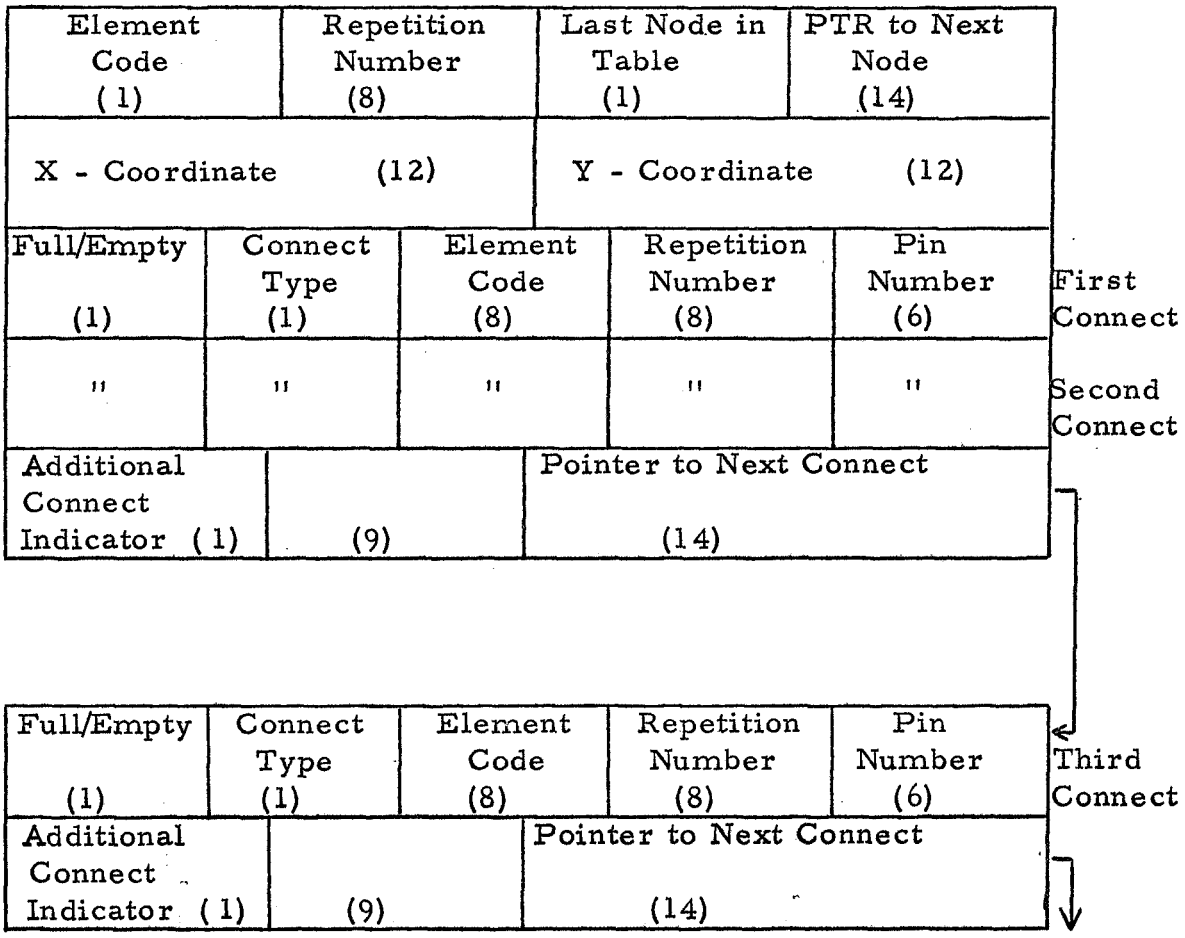


Chart A1(f)

Record Length = 5 + 2 [(number of interconnects) + 2]

The node element code field has been restricted to one bit since only two types of nodes (contact and normal) exist. However, to maintain compatibility with total element nomenclature, element numbers 000_8 and 001_8 will be utilized to specify the two node types. The node working table structure is presented in Chart A1(d) and the record format is detailed in Chart A1(f).

A.5.2.3 Circuit Schematic File

The Circuit Schematic File contains the explicit graphic orders necessary to control the graphic display terminal. It contains not only the orders necessary to produce the circuit schematic in the display work area, but also the orders necessary to partition the display and to present the keyboard image. The schematic file also contains buffer areas for the display message and element areas. The file structure is presented in Chart A1(g).

Since the exact format for file entries is a function of the computer and graphics terminal utilized for this application, no attempt has been made to explicitly specify the individual file tables. However, the file has been structured so that each table can be individually controlled by the display control software. In order to size the table requirements, the SDS CRT Display System for the SDS 930 Computer was used as a basis.

A.5.3 Mask Data Set

The mask data set contains four files, one for each of the required fabrication masks. These files will be utilized to define explicit mask geometry for the circuit. They are constructed during the mask design phase and use as input data information from the working tables, the element dictionary and the element library. The mask files will be developed one at a time and maintained until the output phase in temporary off-line storage. The circuit masks consist of the individual element masks, the arrangement of which is controlled by coordinate information from the working tables. The circuit interconnect and contact components of the masks are developed by standardized design rules and controlled by the interconnection and node information in the working tables.

Since the exact format for the mask data set files is directly dependent upon the exact output format requirements, the detailed file structure cannot be defined until the exact system configuration and output requirements are specified.

CIRCUIT SCHEMATIC FILE
(STRUCTURE)

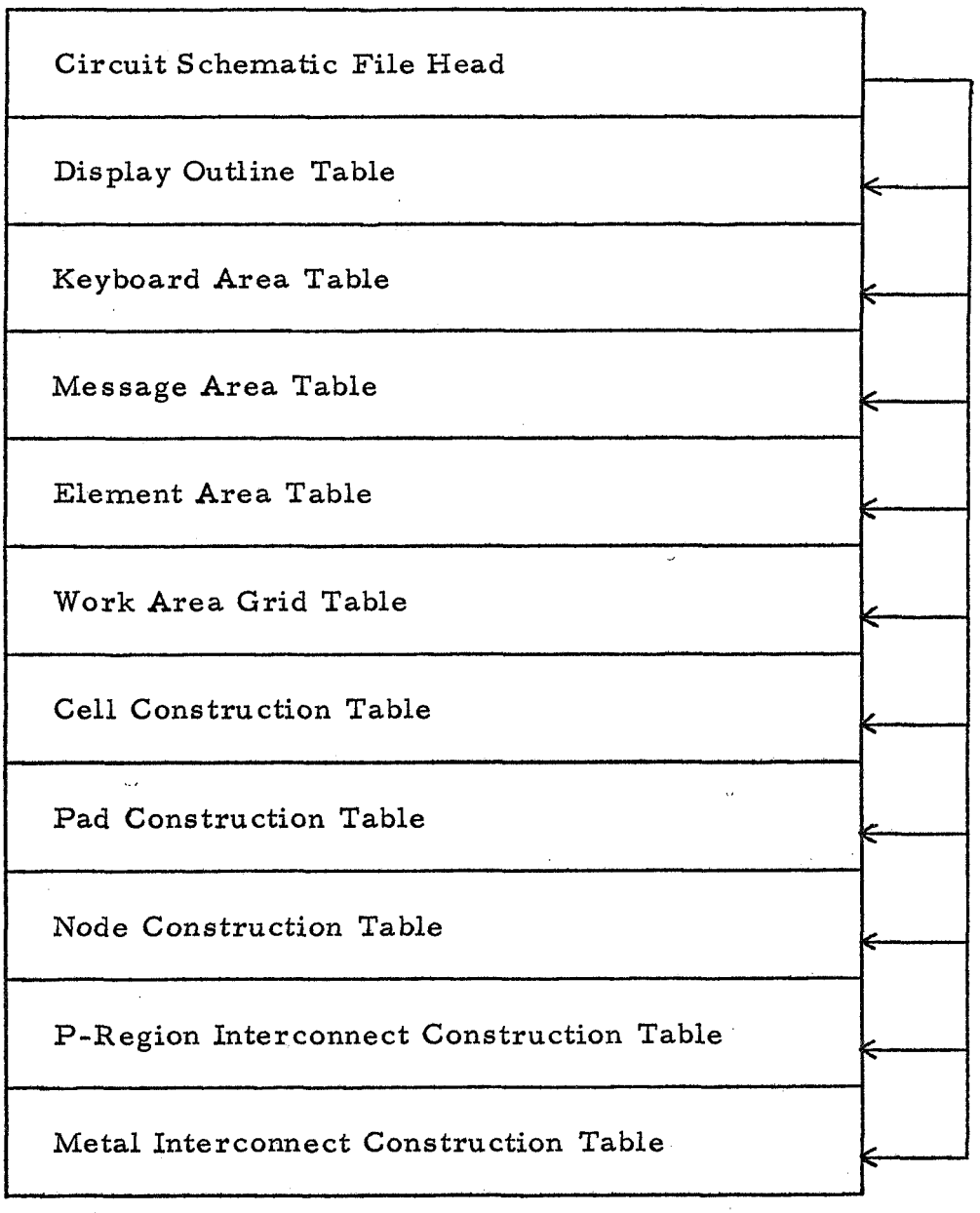


Chart A1(g)

A.5.4 Element Dictionary

The element dictionary lists all defined circuit elements, specifies the number of pins for each cell or pad, and provides the relative pin coordinates for any specified element. For both cell and pad, relative pin coordinates are measured from the element origin. For cells this is from the lower left hand corner and for pads from the geometric center.

Chart A1(h) presents the dictionary structure and record format. Only ten bits have been provided for pointing to the next record element whereas fourteen have been used previously. This has been justified on the assumption that: (a) the element dictionary will reside in contiguous storage locations, and (b) no element record will be smaller than four words. The second assumption is justified in that the vast majority of elements are cells which can have a minimum of six pins [(V_{GG}, V_{DD}, V_G) in and out]. The other element nodes and pads will be defined in the dictionary with four word blocks even though they can be adequately defined in less. The pointer word will be shifted left two locations when used to give the normal fourteen bit address. By starting the dictionary at an address which is a multiple of four, low order zeros in the shifted address will be valid.

A.5.5 Element Library

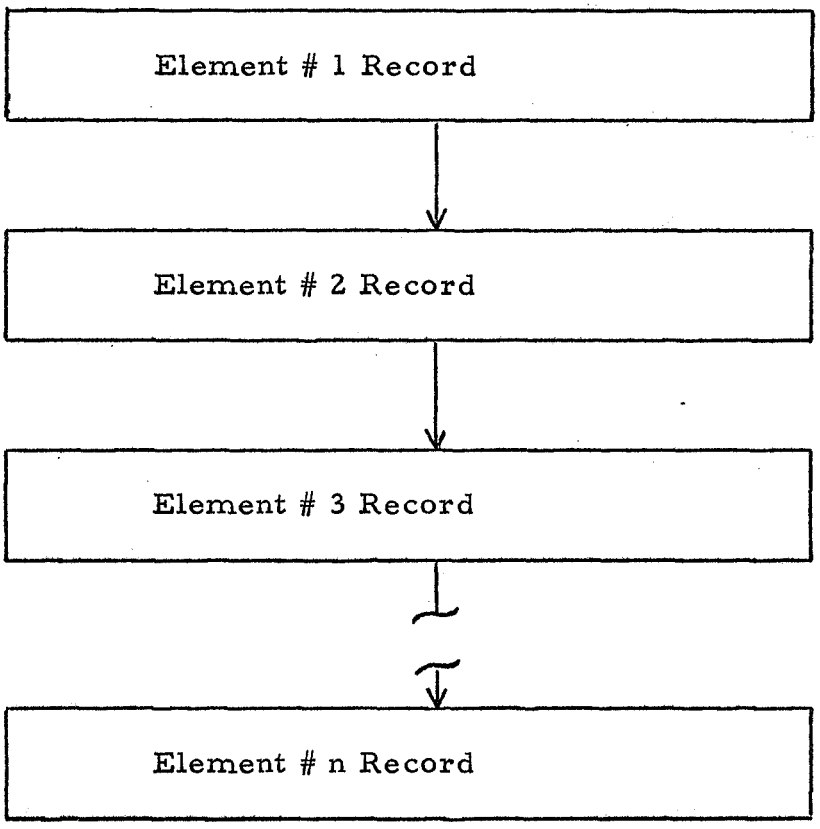
The element library consists of five files, one for each element mask and one for the element schematic. As described in Section A.3.1, a total cell definition consists of not only its schematic representation but also of its mask geometry. The element library file records are used in an overlap manner to construct the display circuit's schematic and the mask data set circuit files. Because of this all coordinate information in the element library is stored in a relocatable format relative to the element origin.

The actual library structure and file record format are highly dependent upon system configuration and have not been defined at this time. Element schematic file records will be stored as near to true graphic order format as is possible. The element mask files will utilize a format compatible with that of the circuit mask files.

A.5.6 Circuit Library

The circuit library provides a capability to store completed circuits on the system which can then be retrieved for reproduction or

ELEMENT DICTIONARY
(Structure)



(TABLE RECORD)

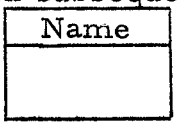
Element Number (8)	Number of Pins (6)	Pointer to Next Record (10)	
X - Coordinate (12)	Y - Coordinate (12)		Pin #1 Coordinates
X - Coordinate (12)	Y - Coordinate (12)		Pin #2 Coordinates
X - Coordinate (12)	Y - Coordinate (Y)		Pin #n Coordinates

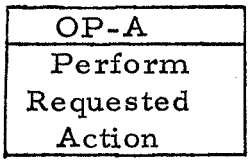
Chart A1(h)

used as the baseline for further design work. Entries will be made in the library by card or by using the "file" instruction.

Very little effort has been expended to define the circuit library requirements, structure, or format. It may not be feasible to provide such a library if a small computer is dedicated to this application and it is not of a high enough priority to warrant inclusion in the initial system developed. However, it is an attractive feature and should be seriously considered as a logical addition to the system.

A.5.7 Functional Flow Charts

Functional flow charts of the application software for both the circuit design and mask design phases have been prepared and are presented in Figure A12. The "Picture on a Page" technique has been utilized which allows the reader to study the flows to the depth he desires. Each page is a complete representation of the area presented. Those functions which are expanded in more depth on subsequent sheets are identified with subroutine nomenclature blocks 

. For example on Figure A12(a), the block 

indicates that the activity defined by the block is discussed in more detail on a separate sheet with the entry [OP-A]. (See Figure A12(c).)

The flow charts are self-explanatory and deliberately sketchy in those areas which either require additional definition or are dependent upon exact system configuration definition.

A.5.8 Software Statistics

The application software statistics are presented in Tables A2 through A7.

Table A2 provides an overall summary of core utilization and storage requirements. The derivation of the data requirement estimates is detailed on the subsequent tables.

The total main storage requirement is presented in Table A2. However, the maximum single phase requirement never exceeds 15, 610 words. If a machine with less than 16K of memory is selected for this task, additional overlays will be necessary. Current software requirements and definition indicate that at least 8K of memory is a requirement for performing this task.

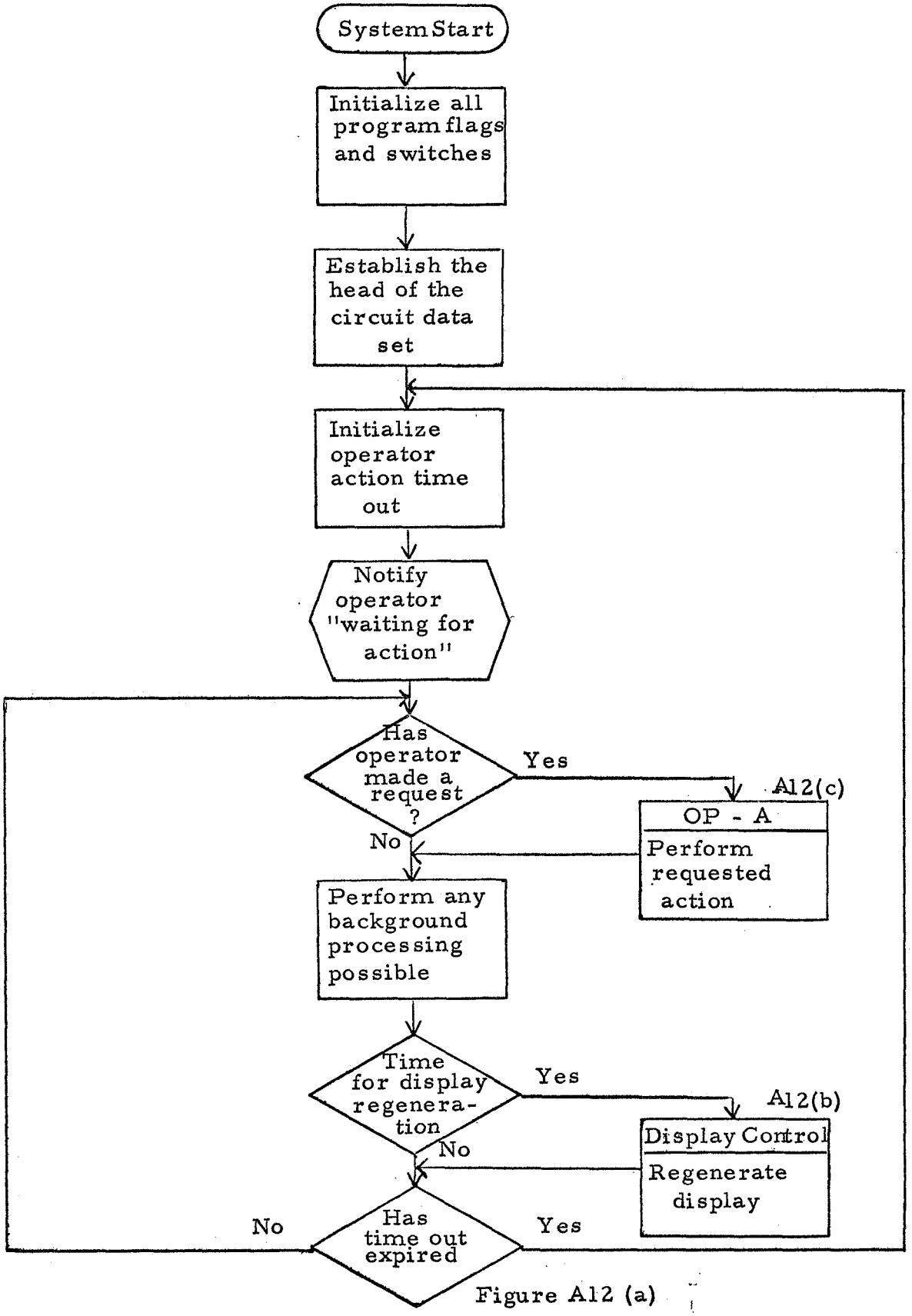

System Start
Initialize all program flags and switches
Establish the head of the circuit data set
Initialize operator action time out
Notify operator "waiting for action"
Has operator made a request ?
Yes
A12(c)
OP - A
Perform requested action
No
Perform any background processing possible
Time for display regenera-tion
Yes
A12(b)
Display Control
Regenerate display
No
Has time out expired
No
Yes

Figure A12 (a)

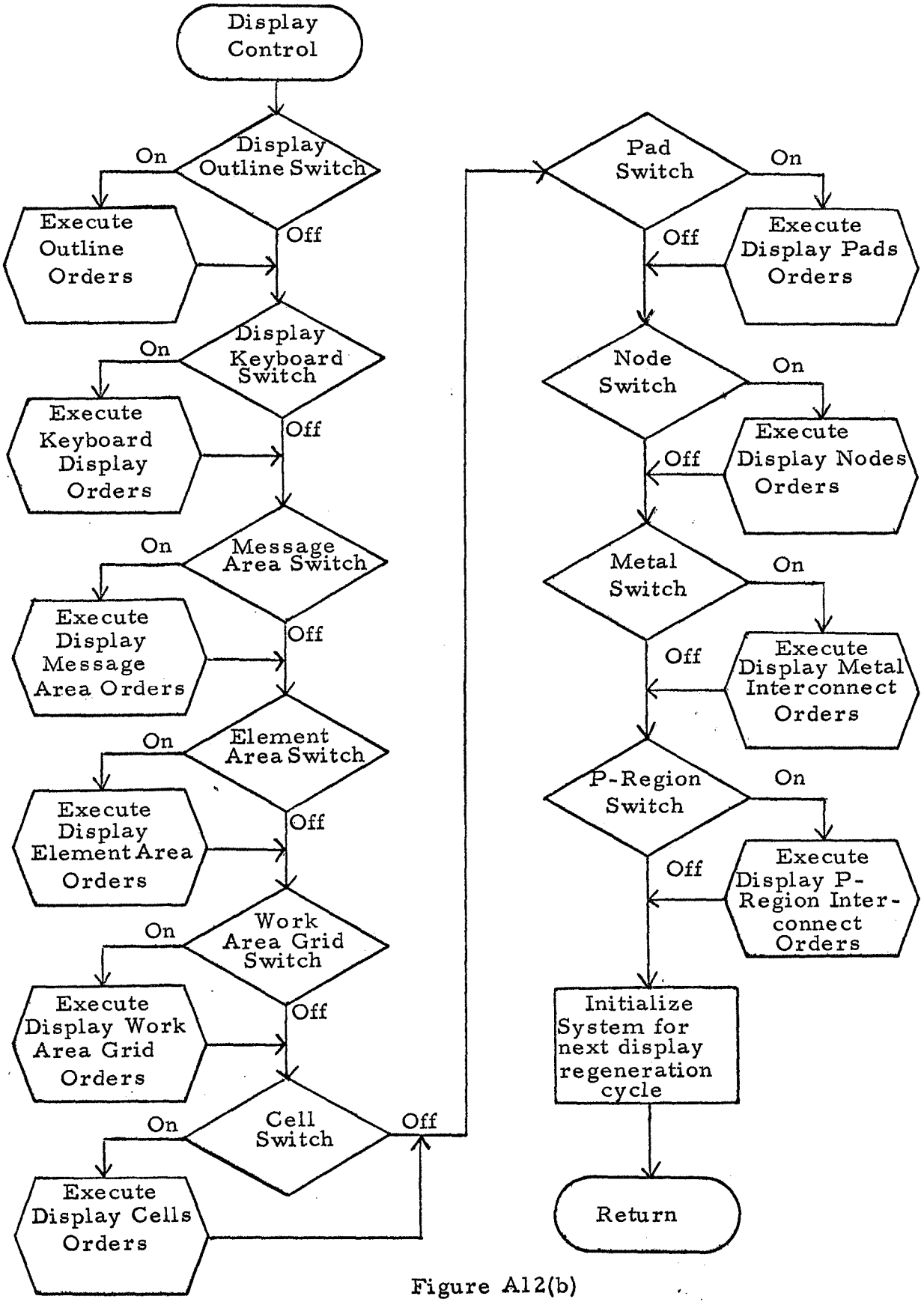

Display Control
Display Outline Switch
On
Execute Outline Orders
Off
Display Keyboard Switch
On
Execute Keyboard Display Orders
Off
Message Area Switch
On
Execute Display Message Area Orders
Off
Element Area Switch
On
Execute Display Element Area Orders
Off
Work Area Grid Switch
On
Execute Display Work Area Grid Orders
Off
Cell Switch
On
Execute Display Cells Orders
Off
Pad Switch
On
Execute Display Pads Orders
Off
Node Switch
On
Execute Display Nodes Orders
Off
Metal Switch
On
Execute Display Metal Interconnect Orders
Off
P-Region Switch
On
Execute Display P-Region Interconnect Orders
Off
Initialize System for next display regeneration cycle
Return

Figure A12(b)

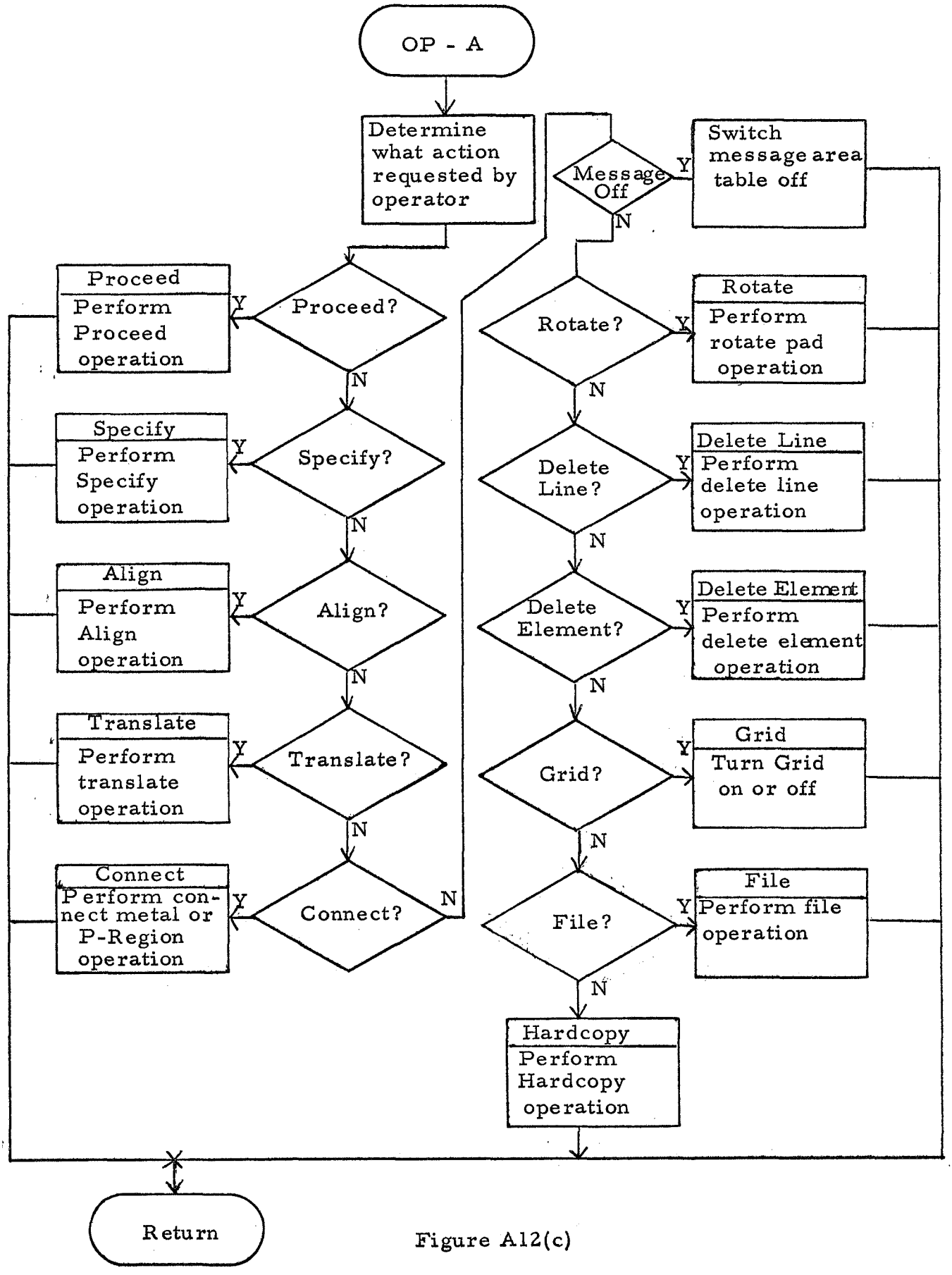

OP - A
Determine what action requested by operator
Message Off
Y
Switch message area table off
N
Proceed?
Y
Proceed
Perform Proceed operation
N
Rotate?
Y
Rotate
Perform rotate pad operation
N
Specify?
Y
Specify
Perform Specify operation
N
Delete Line?
Y
Delete Line
Perform delete line operation
N
Align?
Y
Align
Perform Align operation
N
Delete Element?
Y
Delete Element
Perform delete element operation
N
Translate?
Y
Translate
Perform translate operation
N
Grid?
Y
Grid
Turn Grid on or off
N
Connect?
Y
N
Connect
Perform connect metal or P-Region operation
File?
Y
File
Perform file operation
N
Hardcopy
Perform Hardcopy operation
Return

Figure A12(c)

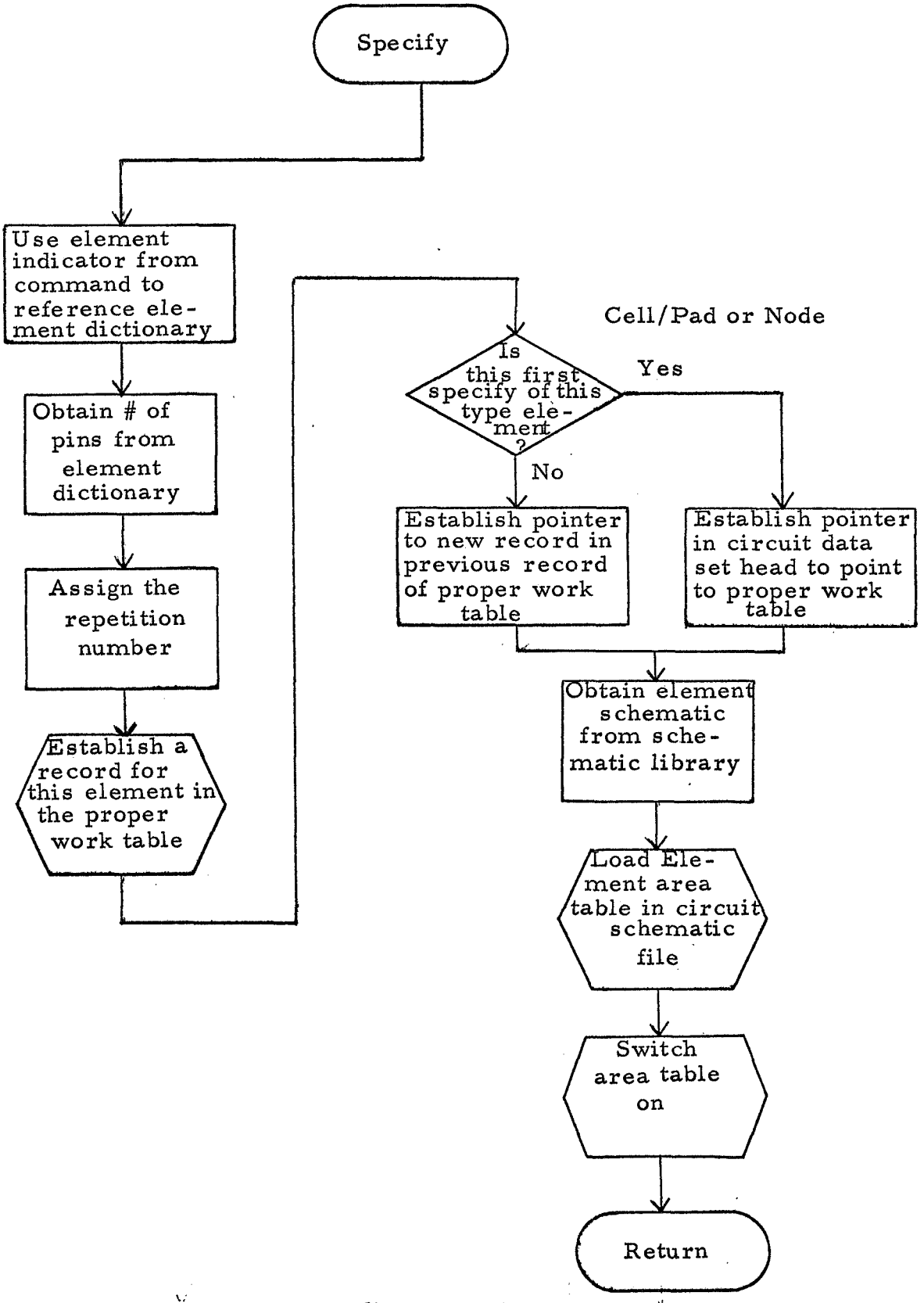

Specify
Use element indicator from command to reference element dictionary
Obtain # of pins from element dictionary
Assign the repetition number
Establish a record for this element in the proper work table
Cell/Pad or Node
Is this first specify of this type element ?
Yes
No
Establish pointer to new record in previous record of proper work table
Establish pointer in circuit data set head to point to proper work table
Obtain element schematic from schematic library
Load Element area table in circuit schematic file
Switch area table on
Return

Figure A12(d)

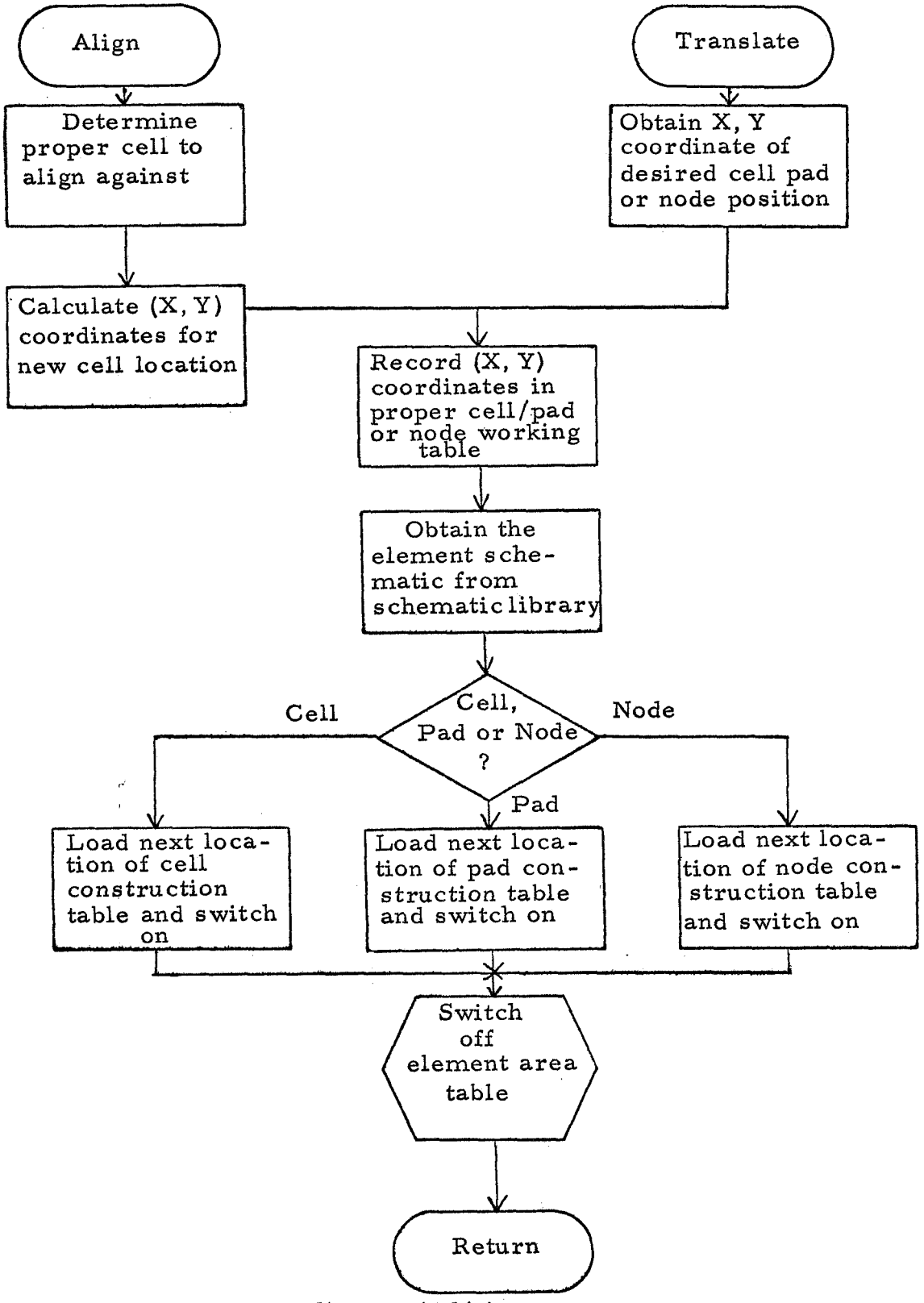

Align
Translate
Determine proper cell to align against
Obtain X, Y coordinate of desired cell pad or node position
Calculate (X, Y) coordinates for new cell location
Record (X, Y) coordinates in proper cell/pad or node working table
Obtain the element schematic from schematic library
Cell, Pad or Node ?
Cell
Pad
Node
Load next location of cell construction table and switch on
Load next location of pad construction table and switch on
Load next location of node construction table and switch on
Switch off element area table
Return

Figure A12(e)

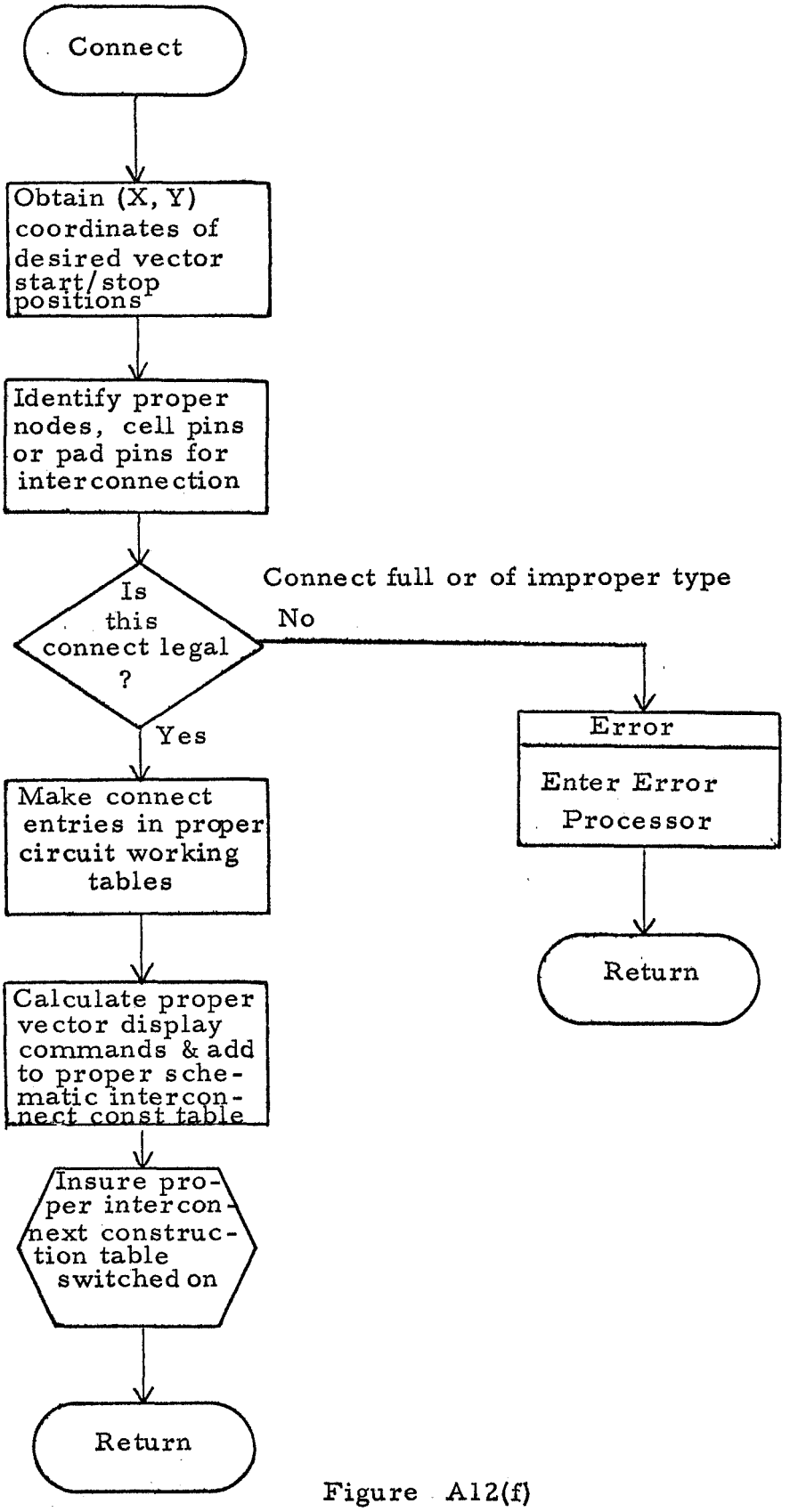

Connect
Obtain (X, Y) coordinates of desired vector start/stop positions
Identify proper nodes, cell pins or pad pins for interconnection
Is this connect legal ?
Connect full or of improper type
No
Yes
Error
Enter Error Processor
Return
Make connect entries in proper circuit working tables
Calculate proper vector display commands & add to proper schematic interconnect const table
Insure proper interconnect construction table switched on
Return

Figure A12(f)

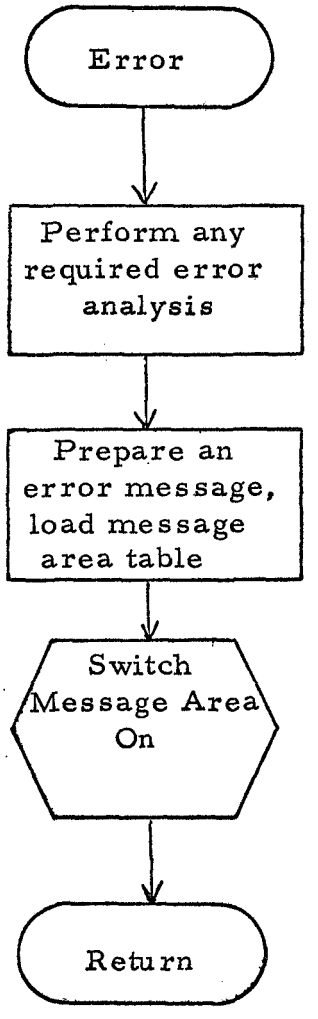

Error
Perform any required error analysis
Prepare an error message, load message area table
Switch Message Area On
Return

Figure A12(g)

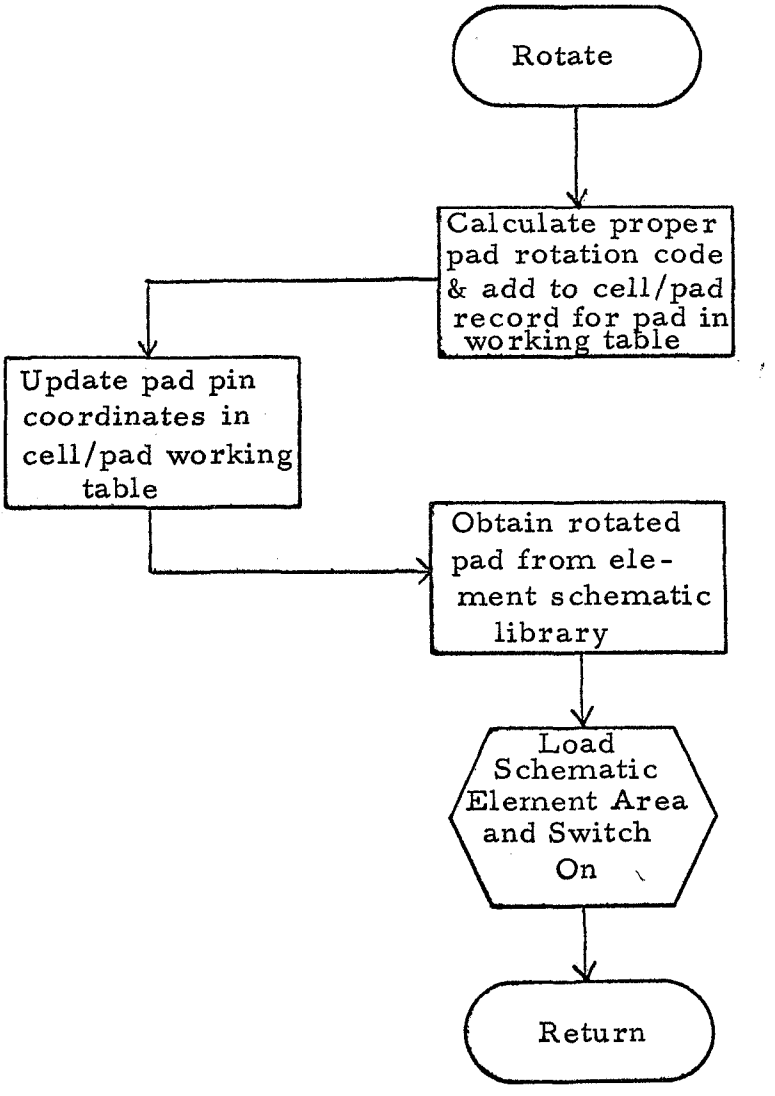

Rotate
Calculate proper pad rotation code & add to cell/pad record for pad in working table
Update pad pin coordinates in cell/pad working table
Obtain rotated pad from element schematic library
Load Schematic Element Area and Switch On
Return

Figure A12(h)

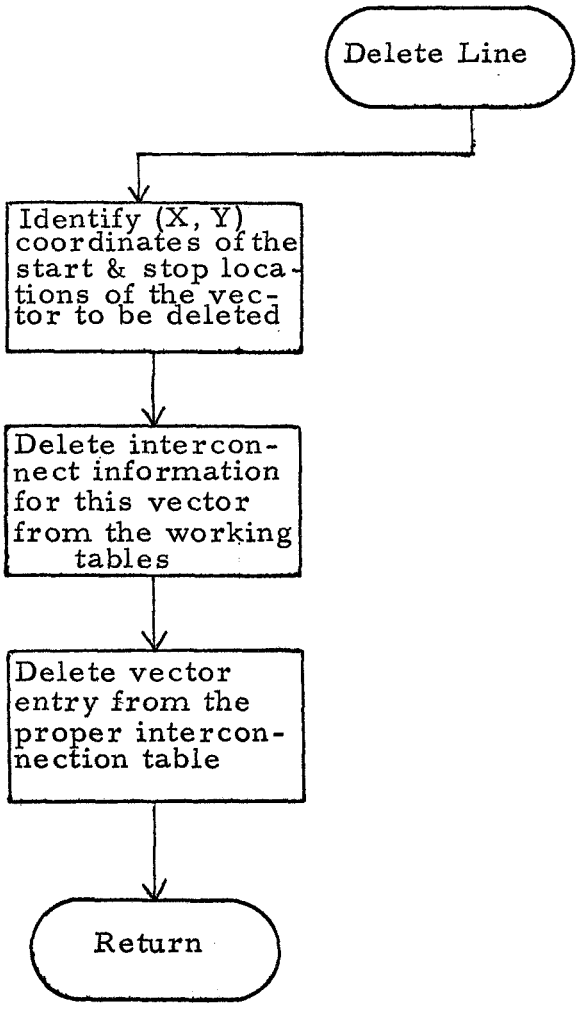

Delete Line
Identify (X, Y) coordinates of the start & stop locations of the vector to be deleted
Delete interconnect information for this vector from the working tables
Delete vector entry from the proper interconnection table
Return

Figure A12(i)

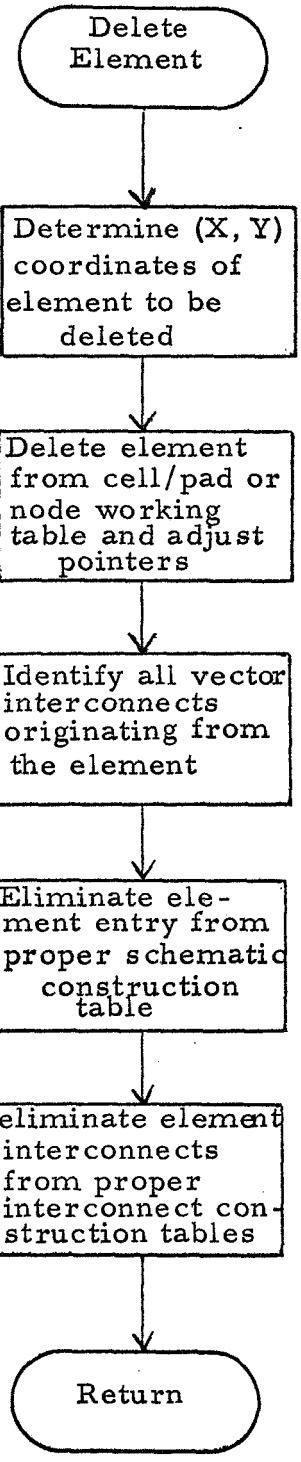

Delete Element
Determine (X, Y) coordinates of element to be deleted
Delete element from cell/pad or node working table and adjust pointers
Identify all vector interconnects originating from the element
Eliminate element entry from proper schematic construction table
eliminate element interconnects from proper interconnect construction tables
Return

Figure A12(j)

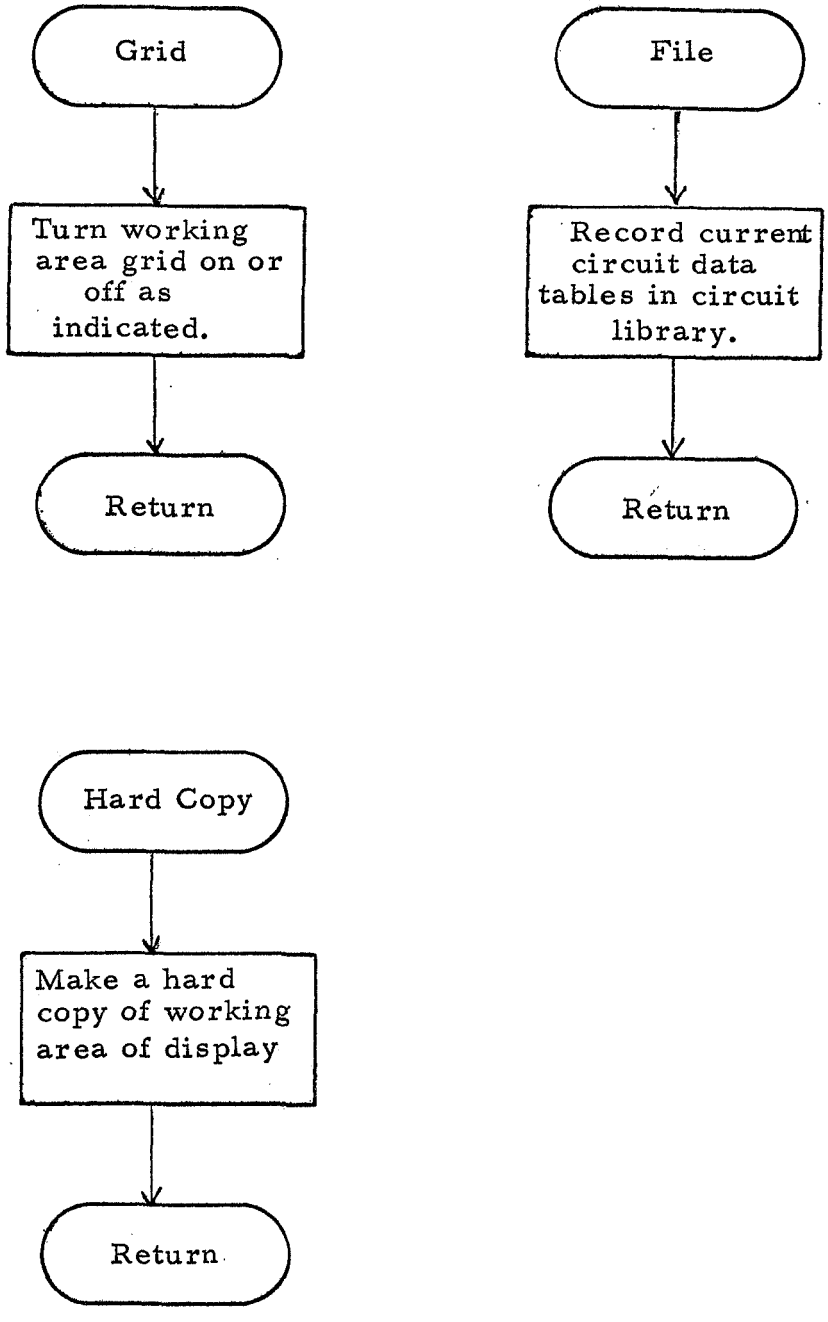

Grid
Turn working area grid on or off as indicated.
Return
File
Record current circuit data tables in circuit library.
Return
Hard Copy
Make a hard copy of working area of display
Return

Figure A12(k)

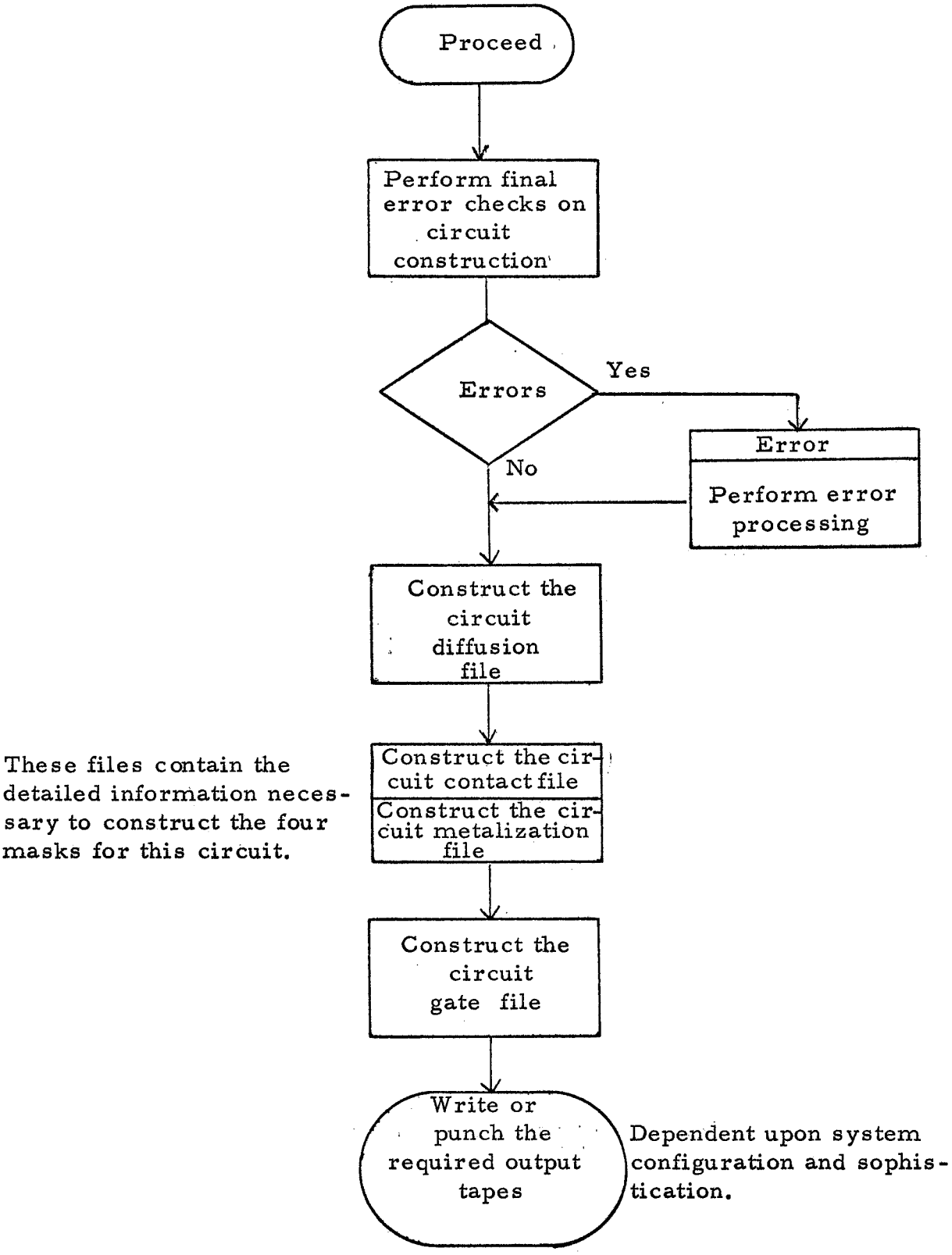

Proceed
Perform final error checks on circuit construction
Errors
Yes
No
Error
Perform error processing
Construct the circuit diffusion file
Construct the circuit contact file
Construct the circuit metalization file
Construct the circuit gate file
Write or punch the required output tapes
These files contain the detailed information necessary to construct the four masks for this circuit.
Dependent upon system configuration and sophistication.

Figure A12(1)

SOFTWARE COMPONENTS

		SDS 930 Core Estimates	
I.	Instructions		
1.	Executive & Initialization	500	
2.	Display Control	500	
3.	Card Input Processor	1000	
4.	Circuit Design Software	2000	
5.	Mask Design Processor	3000	
6.	Output Processor	1000	
		8000	
II.	Data		Reference Table
1.	Circuit Data Set	6810	A3
2.	Mask Data Set	6000	A4
3.	Element Dictionary	2200	A7
4.	Element Library	34060	A7
5.	Circuit Library	open ended	
6.	Miscellaneous Data (10% inst)	800	
		49870	
III.	Main Storage Components		
1.	Instructions	9000	
2.	Circuit Data Set (Both not in Core Simultaneously)	6810	
3.	Mask Data Set (Both not in Core Simultaneously)	6000	
4.	Miscellaneous Data	800	
		21610	

Table A2

CIRCUIT DATA SET

		Subtotal	Totals	Reference
A.	Data Set Head	6 words	6 words	Chart A1(c)
B.	Working Tables			
	1. Cell/Pad Table		840 words	
	a. 30 cells (11 pins ea)	750 words		Table A3(a)
	b. 18 pads	90 words		Table A3(a)
	2. Node Table		1750 words	
	a. 100 contact nodes	500 words		Table A3(b)
	b. 210 normal nodes	1250 words		Table A3(b)
C.	Circuit Schematic File		3079 words	
	1. File Head (estim.)	11 words		Table A3(c)
	2. Display Outline Table	30 words		"
	3. Keyboard Area Table	65 words		"
	4. Message Area Table	202 words		"
	5. Element Area Table	33 words		"
	6. Work Area Grid Table	400 words		"
	7. Cell Construction Table	990 words		"
	8. Pad Construction Table	198 words		"
	9. Node Construction Table	100 words		"
	10. P-Region Interconnect Construction Table	1050 words		"
	11. Metal Interconnect Construction Table			

Circuit Data Set (raw estimate)	5675 words
Margin 20%	1135 words
Circuit Data Set (Estimate)	6810 words

Table A3

CELL/PAD TABLE
(Calculations)

Cells

11 Cell Pins used as Pin Average/Cell

5 Logical Pins

6 Power Pins

Cell Record Length = 3 + 2 (number of Pins)

Standard Cell = 3 + 2 (11) = 25 words

30 Cells = 750 Words

Pads

Pad Record Length = 5 Words

18 Pads = 90 Words

Table A3(a)

NODE TABLE
(Calculations)

Assumptions:

1) The number of normal nodes estimated is approximately equal to the number of paths.

2) The worst case circuit number of contact nodes estimated at approximately 100 nodes.

3) Derive calculations based on 2 interconnects/node.

Node Record Length = 5 + 2 [(Number of Interconnects)-2]

Contact Nodes

100 Nodes = 500 Words

Normal Nodes *

210 Nodes [(7)(30)] = 1250 Words

* See Circuit Path Survey, Table A5(b).

Table A3(b)

CIRCUIT SCHEMATIC FILE
CALCULATION TABLES

1.	Display Outline Table		
	15 vectors -		30 words
2.	Display Keyboard Area		
	46 characters	46 words	
	19 coordinate positions	19 words	65 words
3.	Message Area Table		
	200 characters	200 words	
	2 lines	2 words	202 words
4.	Element Area Table		
	Typical Element (Five Logic Pins)		
	Box Outline	5 words	
	Pin Vectors (8)	16 words	
	Characters (3)	4 words	25 words
	Worst Case Element (Nine Logic Pins)		
	Box Outline	5 words	
	Pin Vectors (12)	24 words	
	Characters (3)	4 words	33 words
5.	Work Area Grid Table		
	400 Points (20 X 20)	400 words	400 words
6.	Cell Construction Table		
	30 Cells (worst case)		
	(33) (30)	990 words	990 words
7.	Pad Construction Table - 18 pads		
	Outline Vector	5 words	
	Pin Vector	2 words	
	Characters (3)	4 words	
	Times (18)	11	198 words

Table A 3(c)

8.	Node Construction Table	
	Contact (100)	100 words
9.	P-Region Interconnect Construction Table and Metal Interconnect Construction Table	
	Estimate based on 7 Paths/Cell 4 Vectors/Path	
	(30) (7) (5)	1050 words

Table A3(c) (continued)

MASK DATA SET

STANDARD WORST CASE CIRCUIT

Components	Data Words	Reference
100 Devices	3300	Table A5
Paths (30 cells)	630	Table A5(b)
Pads (18)	36	Table A6
Contact Nodes (100 est)	200	Table A6
Nodes (210)	420	Table A6
	4586	
Format Margin 30%	1375	
	5961	
Rounded	6000 words	

MASK FILE DISTRIBUTION (see Table A5)

A.	Circuit Diffusion File (25%)	1500 words
B.	Circuit Gate File (11.5%)	700 words
C.	Circuit Contact File (3.5%)	200 words
D.	Circuit Metalization File (60%)	3600 words
		6000 words

Table A4

COMPONENT SURVEY

Three types of typical circuit cells were analyzed and had the following characteristics:

I. Inverter

Definition Requires:

a)	Paths (18)	54 words
b)	Interconnect Lines (2)	6 words
c)	Contact Nodes (3)	6 words
		66 words

II. Double Output Buffer

Definition Requires:

a)	Paths (32)	96 words
b)	Interconnect Lines (4)	12 words
c)	Contact Nodes (4)	8 words
		116 words

III. NOR Unit

Definition Requires:

a)	Paths (21)	63 words
b)	Interconnect Lines (4)	12 words
c)	Contact Nodes (4)	8 words
		83 words

Table A5

COMPONENT SURVEY SUMMARY

Cell Type	Devices per Cell	Words per Definition	Words Scaled for 100 Devices
Inverter	2	66 words	3300 words
DOB	4	116 words	2900 words
NOR	3	83 words	2767 words

3300 chosen as standard estimate for 100 devices

Data Words/Mask (Ratio)

a)	Diffusion	25%
b)	Gate	11.5%
c)	Contact	3.5%
d)	Metalization	60%

Table A5(a)

CIRCUIT PATH SURVEY

Two typical circuits were analyzed:

1) The 5 cell circuit of Figure 3-10 of this document, and

2) The 24 cell circuit of the Ford/Philco Design Manual, Figure 5.8, Page 5-9.

Conclusions

a) 5 Cell Circuit - 35 Paths

b) 24 Cell Circuit - 150 Paths

7 Paths/Cell Chosen as Standard Estimate

Mask Path Estimate

(30 Cells) (7) = 210 Paths

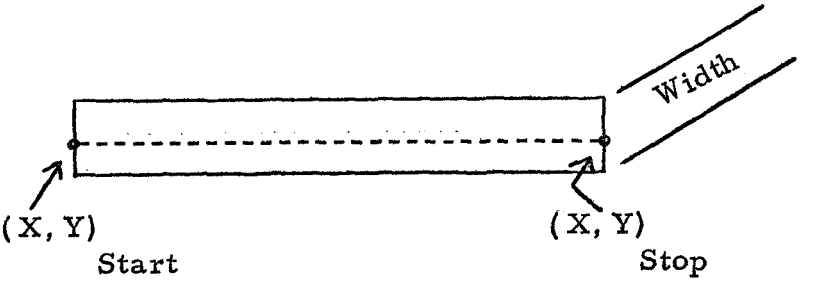
210 Paths (3) = 630 Words *

*See Table A6

Table A5(b)

CIRCUIT MASK COMPONENTS

I. Path



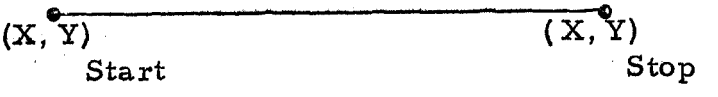
Identification of a path requires three words:

1) Identification, width

2) (X, Y) Start

3) (X, Y) Stop

II. Interconnect Line (Vector)



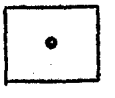
Requires 3 words:

1) Identification

2) (X, Y) Start

3) (X, Y) Stop

III. Bonding Pad



Requires two words:

1) Identification

2) (X, Y) Coordinates

IV. Node

Requires two words:

1) Identification

2) (X, Y) Coordinates

Table A6

ELEMENT DICTIONARY

200 Elements

Basic Element = Cell (11 Pins)	2200 words

ELEMENT LIBRARY

A. Mask Files — 100 words Standard/Element

200 Elements	20,000 words
Margin 30%	6,000 words
Total Estimate	26,000 words

File Breakdown

1)	Element Diffusion File (25%)	6,500 words
2)	Element Gate File (11.5%)	2,990 words
3)	Element Contact File (3.5%)	910 words
4)	Element Metalization File (60%)	15,600 words
		26,000 words

B. Element Schematic File

31 words/Element (200 elements)	6,200 words
Margin 30%	8,060 words
Total Element Library	34,060 words

Table A7

The statistic tables should be self-explanatory. However, some further clarification is necessary with respect to element symbolic representation.

The most complex element is the cell. A detailed analysis of the Philco-Ford building blocks indicates that the worst case cell required nine logical pins (the four/four - input or - NAND). On the average, a cell has five pins. Since a cell's symbolic representation is made up of vectors, pins, and characters, it is possible to develop cell symbol representation requirements. In order to simplify the representation, the cell format of Figure A7(b) has been adopted. This format allows a cell to be defined with vectors and characters alone. Table A3(a) provides the core estimates for describing both the worst case and typical cells.

A.6 OUTPUT REQUIREMENTS

The primary output of this system is the input tape for the Gerber plotter which will produce the artwork for the desired circuit masks. This data should be in the necessary format to provide direct input to the Gerber plotter. However, since the final masks may require more than four hours of plotter time to produce, it is worthwhile to provide additional output data describing and evaluating the mask design. The designer would use this output to determine if the circuit requires further design or is ready for final artwork generation. Some of the more useful outputs which should be provided are described below.

COMPONENT LISTING: A listing of all cells, nodes, pads, and interconnects should be provided for analysis and future reference.

ERROR MESSAGES: All program detectable errors or warnings should be brought to the attention of the designer.

PACKING INDEX NUMBER: A number giving the percentage of the total chip area required by the circuit could be useful in determining the possibility of future circuit modifications.

EFFICIENCY NUMBER: A number based on circuit geometry and the number of crossovers could be provided to evaluate the overall circuit design.

PLOTS: Rough plots of the circuit's schematic and masks may be drawn by an inexpensive CALCOMP plotter. Several of the mask geometries may be superimposed to improve readability.

A.7 COMPUTER TASK STUDY CONCLUSIONS

This section has developed the functional design of a baseline package which will provide for the computer assisted design of the photographic masks necessary for circuit fabrication. Since special interest was expressed in interactive graphics, the designed software package was developed to support such circuit design activities. Although the design was done under the constraint of a small system configuration dedicated to speedy "in house" mask creation, additional capability can be developed as a logical extension using the same design concepts.