M. Tech (Full Time) – VLSI DESIGN (FULL TIME)

Curriculum and Syllabus

(2018-19 and onwards)

FACULTY OF ENGINEERING AND TECHNOLOGY
SRM Institute of Science and Technology
SRM Nagar, Kattankulathur – 603 203

M. Tech. VLSI DESIGN (FULL TIME)
Curriculum and Syllabus
Batch 2018-19 and onwards

S. No.	Category	No. of Credits			
		I Semester	II Semester	III Semester	IV Semester
1	Core Courses	12	12	-	-
2	Program Elective Courses	3	6	9	-
3	Supportive Courses	3	-	-	-
4	Interdisciplinary	-	3	-	-
5	Career Advancement Courses	1	1	1	-
6	Seminar	-	-	1	-
7	Project Work	-	-	6*	16**
	Credits per semester	19	22	17	16
	Total Credits				**74**

* Main Project-Phase I ** Main Project-Phase II

Core courses

Course code	Course Title	L	T	P	C
VL2001	Digital Systems Design using Verilog	3	0	2	4
VL2002	MOS Device Modeling	4	0	0	4
VL2003	Digital Signal processing structures for VLSI	3	1	0	4
VL2004	CMOS Analog VLSI	3	0	2	4
VL2005	VLSI Design Automation	3	1	0	4
	OR				
VL2006	VLSI Technology	4	0	0	4
VL2007	Testing of VLSI Circuits	3	1	0	4
	OR				
VL2008	Reconfigurable Architectures for VLSI	4	0	0	4

Program Electives

Course code	Course Title	L	T	P	C
VL2101	Digital System Synthesis and Verification	3	0	0	3
VL2102	Nano Electronics	3	0	0	3
VL2103	Low Power VLSI Design	3	0	0	3
VL2104	Neural Networks for VLSI	3	0	0	3
VL2105	VLSI Digital Signal Processing systems	3	0	0	3
VL2106	ASIC Design	3	0	0	3
VL2107	CMOS Mixed signal Circuit Design	3	0	0	3
VL2108	DSP Architectures and Applications	3	0	0	3
VL2109	Design of Semiconductor Memories	3	0	0	3
VL2110	System-on-Chip design	3	0	0	3
VL2111	Genetic Algorithms and their Applications in VLSI	3	0	0	3

Course code	Course Title	L	T	P	C
VL2112	Reliability Engineering	3	0	0	3
VL2113	Fundamentals and Applications of MEMS	3	0	0	3
VL2114	RF VLSI Design	3	0	0	3
VL2115	High Speed VLSI	3	0	0	3
VL2116	Magneto-electronics	3	0	0	3
VL2117	VLSI interconnects and its design techniques	3	0	0	3
VL2118	Digital HDL Design and Verification	3	0	0	3
VL2119*	Computational Aspects of VLSI	3	0	0	3
VL2120*	Computational Intelligence	3	0	0	3
VL2121*	Chromatic Graph Theory	3	0	0	3
VL2122*	Solar Cells and Thin Film Technologies	3	0	0	3
VL2123*	Next Generation Photovoltaics	3	0	0	3
VL2124*	Quantum Computation and Information	3	0	0	3
VL2125*	Superconductivity: Theory and its Effects	3	0	0	3
VL2126*	Multicore Processors and Scheduling Algorithms	3	0	0	3

* Ph.D coursework subjects

Supportive Courses

Course code	Course Title	L	T	P	C
MA2010	Graph theory and optimization techniques	3	0	0	3
EM2101	Computer Architecture	3	0	0	3
CO2105	Electromagnetic Interference and Compatibility in System Design	3	0	0	3

Other Courses

Course code	Course Title	L	T	P	C
CAC2001	Career Advancement Course for Engineers –I	1	0	1	1
CAC2002	Career Advancement Course for Engineers –II	1	0	1	1
CAC2003	Career Advancement Course for Engineers –III	1	0	1	1
VL2047	Seminar	0	0	1	1
VL2049	Project Work – Phase - I	0	0	12	6
VL2050	Project Work – Phase – II	0	0	32	16

VL2001		L	T	P	C
	DIGITAL SYSTEMS DESIGN USING VERILOG	**3**	**0**	**2**	**4**
	Total Contact Hours - 75				
	Prerequisites : Nil				

PURPOSE	
HDL programming being fundamental for VLSI design this course concentrates on delivering the necessary concepts and features.	
INSTRUCTIONAL OBJECTIVES	
1.	The student will learn the different abstract levels in Verilog for modeling digital circuits.
2.	The student will learn the basic CMOS circuit, characteristics and performance.
3.	The student will learn the designing of combinational and sequential circuits in CMOS

UNIT I - BASIC CONCEPTS - VERILOG (15 hours)
Operators, Basic concepts, Identifiers, System task and functions, Value set, Data types, Parameters, Operands, Operators, Modules and ports, Gate-level Modeling, Dataflow Modeling, Behavioral Modeling, Switch level modeling, Tri state gates, MOS Switches, Bidirectional switches, User defined primitives, Combinational UDP, Sequential UDP. Introduction to synthesis, Verilog HDL synthesis-Synthesis Design flow Test bench-lab exercise.

UNIT II – BASICS OF MOS TRANISTORS (15 hours)
MOS transistors- Threshold voltage- characteristics of MOS transistor-channel length modulation- short channel effects- Design of Logic gates using NMOS, PMOS and CMOS, Stick diagrams- Transfer characteristics of CMOS inverter- Power dissipation – Delay and sizing of inverters- Lab exercise.

UNIT III - CMOS – COMBINATIONAL CIRCUITS (15 hours)
Static CMOS design-complementary CMOS - static properties- complementary CMOS design-Power consumption in CMOS logic gates-dynamic or glitching transitions - Design techniques to reduce switching activity - Radioed logic-DC VSL - pass transistor logic - Differential pass transistor logic -Sizing of level restorer-Sizing in pass transistor-Dynamic CMOS design-Basic principles - Domino logic-optimization of Domino logic-NPCMOS-logic style selection - Designing logic for reduced supply voltages.
Lab exercise in Switch level modeling.

UNIT IV - CMOS – SEQUENTIAL CIRCUITS (15 hours)
Timing metrics for sequential circuit - latches Vs registers -static latches and registers - Bistability principle - multiplexer based latches-master slave edge triggered registers- non-ideal clock signals-low voltage static latches-static SR flip flop - Dynamic latches and registers- C^2MOS register - Dual edge registers-True single phase clocked registers-pipelining to optimize sequential circuit latch Vs register based pipelines-non-Bistable sequential circuit-Schmitt trigger-mono stable -Astable -sequential circuit - choosing a clocking strategy.. Lab exercise in Switch level modeling

UNIT V – SUB-SYSTEM DESIGN/ SYSTEM VERILOG (15 hours)
Addition/Subtraction - Comparators- Zero/One Detectors- Binary Counters- ALUs Multiplication- Shifters- Memory elements- control: Finite-State Machines. Lab exercise.

REFERENCES

1. Samir palnitkar, ”*Verilog HDL*”, Pearson education, Second Edition,20O3.
2. J. Bhasker, “*A Verilog HDL Primer*”, Second Edition, Star Galaxy, 2005.
3. J. Bhasker, “*A Verilog Synthesis: A Practical Primer*”, Star Galaxy, 1998
4. Jan.M.Rabaey., Anitha Chandrakasan Borivoje Nikolic, "*Digital Integrated Circuits*", Second Edition
5. Neil H.E Weste and Kamran Eshraghian, "*Principles of CMOS VLSI Design*", 2nd Edition, Addition ,Wesley, 1998.

<table>
<tr><td rowspan="4">VL2002</td><td></td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>MOS DEVICE MODELING</td><td>4</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td colspan="5">Total Contact Hours - 60</td></tr>
<tr><td colspan="5">Prerequisites : Nil</td></tr>
<tr><td colspan="6">PURPOSE</td></tr>
<tr><td colspan="6">This course deals with the modeling of MOS devices and their fundamental working concepts.</td></tr>
<tr><td colspan="6">INSTRUCTIONAL OBJECTIVES</td></tr>
<tr><td>1.</td><td colspan="5">To make the student understand how MOSFET and other semiconductor devices are modeled</td></tr>
<tr><td>2.</td><td colspan="5">To impart knowledge to simulate MOSFET for various operational requirements.</td></tr>
<tr><td>3.</td><td colspan="5">To impart a knowledge on advanced structures of MOSFETs like SOIFET, FinFET</td></tr>
</table>

UNIT I - ELECTRON AND HOLE DENSITIES IN EQUILIBRIUM (12 hours)

Fermi – Dirac Statistics, Carrier concentration, Fermi level at equilibrium, recombination, Mobility of carriers, charge transport in semiconductors.

UNIT II - PN JUNCTION (12 hours)

PN Junction under thermal equilibrium under applied bias, Transient Analysis, Injection and Transport model, Diode small signal and large signal model.

UNIT III – MOSFET (12 hours)

Operation of Ideal MOS diode, Effects of mobile Ionic charges, Oxide charges and Interface states, C-V Characteristics, Threshold voltage of MOSFET, Bulk charge model, square law method (Level 1 is SPICE), Level 3 model in SPICE, BSIM Models.

UNIT IV - SECOND ORDER EFFECTS IN MOSFET (12 hours)

Effect of Gate voltage on carrier mobility, Effect of Drain voltage on carrier mobility, Channel length modulation, Breakdown and punch through, Subthreshold current, Short channel effects., Meyer’s model, Small signal model.

UNIT V - ADVANCED TOPICS (12 hours)

MOSFET scaling, Non-uniform doping in channel, SOI MOSFET, Buried channel MOSFET, Fin FET.

REFERENCES

1. Nandita Das Gupta, Amitava Das Gupta, "*Semiconductor devices, modeling and Technology*", Prentice Hall of Indis, 2004.
2. Philip.E.Allen Douglas, R. Hoberg, "*CMOS Analog circuit Design*", second edition, Oxford Press, 2002.
3. S.M. Sze, "*Semiconductor Devices-Physics and Technology*", John Wiley and Sons, 1985.
4. Kiat Seng Yeo, Samir R.Rofail, Wang-Ling Gob, "*CMOS/BiCMOS VLSI-Low Voltage, Low Power*", Pearson Education, Low price edition, 2003.

		L	T	P	C
VL2003	**DIGITAL SIGNAL PROCESSING STRUCTURES FOR VLSI**	**3**	**1**	**0**	**4**
	Total Contact Hours - 60				
	Prerequisite : Nil				
PURPOSE					
DSPs are used in many application areas and hence has become an essential part of VLSIs. Hence to introduce the student about DSP structures, this subject is included.					
INSTRUCTIONAL OBJECTIVES					
1.	To understand the fundamentals of DSP				
2.	To learn various DSP structures and their implementation.				
3.	To know designing constraints of various filters.				

UNIT I - INTRODUCTION TO DIGITAL SIGNAL PROCESSING (12 hours)

Linear System Theory- Convolution- Correlation - DFT- FFT- Basic concepts in FIR Filters and IIR Filters- Filter Realizations. Representation of DSP Algorithms-Block diagram-SFG-DFG.

UNIT II - ITERATION BOUND, PIPELINING AND PARALLEL PROCESSING OF FIR FILTER (12 hours)

Data-Flow Graph Representations- Loop Bound and Iteration Bound- Algorithms for Computing Iteration Bound-LPM Algorithm. Pipelining and Parallel Processing: Pipelining of FIR Digital Filters- Parallel Processing- Pipelining and Parallel Processing for Low Power. Retiming: Definitions-Properties and problems- Solving Systems of Inequalities.

UNIT III - FAST CONVOLUTION AND ARITHMETIC STRENGTH REDUCTION IN FILTERS (12 hours)

Cook-Toom Algorithm- Modified Cook-Toom Algorithm.Design of Fast Convolution Algorithm by Inspection. Parallel FIR filters-Fast FIR algorithms-Two parallel and three parallel. Parallel architectures for Rank Order filters-Odd Even Merge sort architecture-Rank Order filter architecture-Parallel Rank Order filters-Running Order Merge Order Sorter-Low power Rank Order filter.

UNIT IV - PIPELINED AND PARALLEL RECURSIVE FILTERS (12 hours)

Pipeline Interleaving in Digital Filters- Pipelining in 1st Order IIR Digital Filters- Pipelining in Higher- Order IIR Filters-Clustered Look ahead and Stable Clustered Look ahead- Parallel Processing for IIR Filters and Problems.

UNIT V - SCALING AND ROUNDOFF NOISE: (12 hours)

Introduction to Scaling and Roundoff Noise- State Variable Description of Digital Filters- Scaling and Roundoff Noise Computation-Round Off Noise Computation Using State Variable Description- Slow-Down- Retiming and Pipelining.

REFERENCES

1. K.K Parhi: *"VLSI Digital Signal processing"*, John-wiley, 2nd Edition Reprint, 2008.
2. John G.Proakis, Dimitris G.Manolakis, *"Digital Signal Processing"*, Prentice Hall of India, 1st Edition, 2009.

<table>
<tr><td rowspan="4">VL2004</td><td></td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>CMOS ANALOG VLSI</td><td>3</td><td>0</td><td>2</td><td>4</td></tr>
<tr><td colspan="5">Total Contact Hours - 75</td></tr>
<tr><td colspan="5">Prerequisites : Nil</td></tr>
<tr><td colspan="6">PURPOSE</td></tr>
<tr><td colspan="6">Analog circuits are essential in interfacing and building amplifiers and low pass filters. This course introduces design methods for CMOS analog circuit.</td></tr>
<tr><td colspan="6">INSTRUCTIONAL OBJECTIVES</td></tr>
<tr><td>1.</td><td colspan="5">To understand CMOS analog circuits design</td></tr>
<tr><td>2.</td><td colspan="5">To simulate Analog circuits using H SPICE.</td></tr>
<tr><td>3.</td><td colspan="5">To learn noise modeling of CMOS analog circuits</td></tr>
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UNIT I - ANALOG CMOS SUB-CIRCUITS (12 hours)

Introduction to analog design, Passive and active current mirrors, band-gap references, Switched Capacitor circuits - basic principles, sampling switches, switched capacitor integrator, switched capacitor amplifier, simulation of CMOS sub circuits using SPICE.

UNIT II - CMOS SINGLE STAGE AMPLIFIERS (17 hours)

Common-Source stage (with resistive load, diode connected load, current-source load, triode load, source degeneration), source follower, common-gate stage, cascode stage, folded cascode stage. Frequency responses of CS stage, CD stage, CG stage, cascode stage, simulation of CMOS amplifiers using SPICE.

UNIT III - DIFFERENTIAL AMPLIFIER and OPERATIONAL AMPLIFIERS (16 hours)

Single-ended and differential operation, basic differential pair – qualitative and quantitative analyses, common-mode response, differential pair with MOS loads, Performance parameters of op-amp, one stage op-amp, two-stage CMOS op-amp, Gain boosting, slew rate, power supply rejection, Simulation of differential amplifiers using SPICE.

UNIT IV - OSCILLATORS **(15 hours)**

General considerations, Ring oscillators, LC oscillators – cross-coupled oscillators, Colpitts oscillator, One-port oscillator, and voltage controlled oscillators. Simulation of oscillators using SPICE.

UNIT V - NOISE CHARACTERISTICS **(15 hours)**

Statistical characteristics of noise, Types of noise - thermal noise, flicker noise, Representation of noise in circuits, noise in single-stage amplifiers (CS, CD and CG stages), noise bandwidth.

REFERENCES

1. Razavi, *"Design of analog CMOS integrated circuits"*, McGraw Hill, Edition 2002.
2. Gray, Meyer, Lewis, Hurst, *"Analysis and design of Analog Integrated Circuits"*, Willey International, 4th Edition, 2002.
3. Allen, Holberg, *"CMOS analog circuit design"*, Oxford University Press, 2nd Edition, 2012.

		L	T	P	C
VL2005	**VLSI DESIGN AUTOMATION**	**3**	**1**	**0**	**4**
	Total Contact Hours - 60				
	Prerequisite				
	MA2010				

PURPOSE
There is a great need for methods to automate VLSI design methods. This course introduces the automation techniques.

INSTRUCTIONAL OBJECTIVES	
1.	To impart knowledge on implementation of graph theory in VLSI
2.	To impart knowledge on automation methods for VLSI physical design
3.	To impart knowledge on automation methods on VLSI interconnects.

UNIT I - DATA STRUCTURES AND BASIC ALGORITHMS **(12 hours)**

Basic terminology – Complexity Issues and NP-Hardness: algorithms for NP-hard problems- Basic algorithms: Graph algorithms, computational Geometry algorithms- Basic data structures- Graph algorithms for physical design: classes of graphs in physical design, relationship between graph classes, graph problems in physical design, algorithms for Interval graphs, permutation graphs and circle graphs.

UNIT II - PARTITIONING AND CLUSTERING **(12 hours)**

Partitioning and Clustering Metrics -Move-Based Partitioning Methods -Mathematical Partitioning Formulations -Clustering :Hierarchical Clustering ,Agglomerative Clustering - Multilevel Partitioning.

UNIT III - FLOORPLANNING AND PLACEMENT **(12 hours)**

Floorplanning: Early research-Silicing floorplan - Floorplan representation-Packaging floorplan representation-Recent advances in floorplanning.

Placement-Introduction- Problem formulation- Simulation based placement algorithms-Partitioning based placement algorithms-cluster growth-Quadratic assignment-resistive network optimization.

UNIT IV – ROUTING and COMPACTION (12 hours)
Global Routing- Detailed routing- Over the cell routing and via minimization- clock and power routing. Problem Formulation - Classification of Compaction algorithms- 3/2 dimensional compaction-2D compaction- Hierarchical compaction- Recent trends in Compaction.

UNIT V - ISSUES ON INTERCONNECTS (12 hours)
Timing driven Interconnect synthesis-Buffer insertion basics-Generalised buffer insertion-Buffering in layout environment-Global interconnect planning. Introduction to physical design for 3D circuits.

REFERENCES

1. N.A. Sherwani, *"Algorithms for VLSI Physical Design Automation"*, Kluwar Academic Publishers, 2002.
2. S.H. Gerez, *"Algorithms for VLSI Design Automation"*, John Wiley and Sons, 2008.
3. Sung Kyu Lim, *"Practice Problems in VLSI physical design Automation"*, Springer, 2008.
4. charles J . Alpert, Dinesh P. Mehta, Sachin S. Sapatnekar ,*"Hand book of algorithms of Physical design Automation "*, CRC press, 2009.
5. Jeffrey D Ullman*"Computational aspects of VLSI"*,Computer Science Press, 1984.
6. Sadiq M .Sait, Habib Youssef,*"VLSI Physical design automation theory and Practice"*,World Scientific Publishing,1999.

VL2006		**L**	**T**	**P**	**C**
	VLSI TECHNOLOGY	**4**	**0**	**0**	**4**
	Total Contact Hours – 60				
	Prerequisite : Nil				

PURPOSE	
It will focus on micro-fabrication process such as lithography, thermal oxidation, Si/SiO2 interface, dopant diffusion, ion implantation, thin film deposition, etching, and back-end technology. His paper deals with manufacturing of VLSI devices.	
INSTRUCTIONAL OBJECTIVES	
After going through this course student will know about various technologies used for fabricating VLSI devices.	
1.	To understand the impact of the physical and chemical processes of integrated circuit fabrication technology on the design of integrated circuits.
2.	To understand physics of the Crystal growth, wafer fabrication and basic properties of silicon wafers
3.	To learn the various lithography techniques and concepts of wafer exposure system

4.	To understand Concepts of thermal oxidation and Si/SiO2 interface.
5.	To learn concepts of dopant solid solubility, diffusion macroscopic point, different solutions to diffusion equation. Design and evaluation of diffused layers and its measurement methods.
6.	To learn concepts of ion implantation, role of the crystals structures, high-energy implants, ultralow energy implants and ion beam heating methods.

UNIT I - CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION (12 hours)

Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor Phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism And kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopant At interface, Oxidation of Poly Silicon, Oxidation inducted Defects.

UNIT II - LITHOGRAPHY AND RELATIVE PLASMA ETCHING (12 hours)

Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments,

UNIT III - DEPOSITION, DIFFUSION, ION IMPLEMENTATION AND METALLIZATION (12 hours)

Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Flick’s one Dimensional Diffusion Equation – Atomic Diffusion Mechanism – Measurement techniques – Range Theory- Implant equipment. Annealing Shallow junction – High energy implantation – Physical vapors Deposition – Patterning.

UNIT IV - PROCESS SIMULATION AND VLSI PROCESS INTEGRATION (12 hours)

Ion implantation – Diffusion and oxidation – Epitaxy – Lithography – Etching and Deposition- NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology - Bipolar IC Technology – IC Fabrication.

UNIT V - ANALYTICAL, ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES (12 hours)

Analytical Beams – Beams Specimen interactions - Chemical methods – Package types – banking design consideration – VLSI assembly technology – Package fabrication technology.

REFERENCES

1. S.M.Sze, “*VLSI Technology*”, McGraw Hill, 2nd Edition. 2008.
2. James D Plummer, Michael D. Deal, Peter B.Griffin, “*Silicon VLSI Technology: fundamentals practice and Modeling*”, Prentice Hall India, 2009.
3. Wai Kai Chen, “*VLSI Technology*” CRC press, 2003.

VL2007		L	T	P	C
	TESTING OF VLSI CIRCUITS	**3**	**1**	**0**	**4**
	Total Contact Hours - 60				
	Prerequisite : Nil				
PURPOSE					
The purpose of testing a design is twofold: 1. To ensure that, before fabrication, the circuit behavior satisfies the intent of the designer.2. To detect faulty devices, after fabrication					
INSTRUCTIONAL OBJECTIVES					
1.	To gain knowledge on digital testing as applied to VLSI design.				
2.	To acquire knowledge on testing of algorithms for digital circuits				
3.	To learn various testing methods for digital circuits.				

UNIT I - BASICS OF TESTING AND FAULT MODELING (12 hours)
Introduction- Principle of testing - types of testing - DC and AC parametric tests - fault modeling - Stuck-at fault - fault equivalence - fault collapsing - fault dominance - fault simulation

UNIT II - TESTING AND TESTABILITY OF COMBINATIONAL CIRCUITS (12 hours)
Test generation basics - test generation algorithms - path sensitization - Boolean difference – D-algorithm – PODEM - Testable combinational logic circuit design.

UNIT III - TESTING AND TESTABILITY OF SEQUENTIAL CIRCUITS (12 hours)
Testing of sequential circuits as iterative combinational circuits - state table verification - test generation based on circuit structure - Design of testable sequential circuits - Ad Hoc design rules - scan path technique (scan design) - partial scan - Boundary scan

UNIT IV - MEMORY, DELAY FAULT AND I_{DDQ} TESTING (12 hours)
Testable memory design - RAM fault models - test algorithms for RAMs – Delay faults - Delay test- I_{DDQ} testing - testing methods - limitations of I_{DDQ} testing

UNIT V - BUILT-IN SELF-TEST (12 hours)
Test pattern generation of Built-in Self-Test (BIST) - Output response analysis - BIST architectures.

REFERENCES

1. P. K. Lala, “*Digital Circuit Testing and Testability*”, Academic Press, 2002.
2. M.L. Bushnell and V.D. Agrawal, *“Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”*, Kluwar Academic Publishers, 2004.
3. N.K. Jha and S.G. Gupta, “*Testing of Digital Systems*”, Cambridge University Press, 2003.
4. Zainalabe Navabi, “*Digital System Test and Testable Design:* Using HDL Models and Architectures”, Springer, 2010.

<table>
<tr><td rowspan="4">VL2008</td><td></td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>RECONFIGURABLE ARCHITECTURES FOR VLSI</td><td>4</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td colspan="5">Total Contact Hours – 60</td></tr>
<tr><td colspan="5">Prerequisite : Nil</td></tr>
<tr><td colspan="6">PURPOSE</td></tr>
<tr><td colspan="6">The purpose of reconfigurable architectures for VLSI ensures to understand the different configuration patterns, high speed computing and the usage of optical and run time configuration.</td></tr>
<tr><td colspan="6">INSTRUCTIONAL OBJECTIVES</td></tr>
<tr><td>1.</td><td colspan="5">To gain knowledge on run time computing and its applications to VLSI.</td></tr>
<tr><td>2.</td><td colspan="5">To learn optical reconfigurable models.</td></tr>
<tr><td>3.</td><td colspan="5">To know the knowhow of various multi core architectures.</td></tr>
</table>

UNIT I - RECONFIGURABLE COMPUTING HARDWARE (12 hours)

Logic- computational fabric, Array and interconnect-Extended logic- Configuration-Reconfigurable processing fabric architectures-RPF integration into traditional computing systems- operating system support for reconfigurable computing- Evolvable FPGA

UNIT II - MAPPING DESIGNS INTO RECONFIGURABLE PLATFORMS (12 hours)

Structural mapping- integrated mapping- mapping for heterogeneous resources-Placement problem – clustering- simulated annealing – partition based placement – analytical placement-partitioning for granularity- partitioning of parallel programs- instance specific design

UNIT III - COMPUTATIONAL ARCHITECTURES FOR FPGA (12 hours)

Precision analysis for fixed point computation- Distributed arithmetic for FPGA – CORDIC architectures for FPGA- Boolean satisfiability – SAT solvers

UNIT IV - OPTICAL RECONFIGURATION MODELS (12 hours)

Simulation and scalability- Models, Basic algorithmic techniques- optical models – complexities of optical models- run time reconfigurability- Design and implementation

UNIT V - MULTI CORE ARCHITECTURES (12 hours)

Multi core and many core architectures-state of the art multi core operating systems-parallelism and performance analysis

REFERENCES

1. Scott Hauck, André Dehon ,*“Reconfigurable computing: the theory and practice of FPGA-based computation”*, Morgan Kaufmann publishers, 2008.
2. Ramachandran Vaidhyanathan and Jerry. L. Trahan *“Dynamic Reconfiguration: Architectures and Algorithms”*, Kluwer Academic publishers, 2003.
3. Andras Vajda, *“Programming many core chips”*, Springer, 2011.

<table>
<tr><td rowspan="4">VL2101</td><td></td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>DIGITAL SYSTEM SYNTHESIS AND VERIFICATION</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td colspan="5">Total Contact Hours – 45</td></tr>
<tr><td colspan="5">Prerequisite : Nil</td></tr>
<tr><td colspan="6">PURPOSE</td></tr>
<tr><td colspan="6">HDL programming is fundamental for VLSI design and hence this course is given.</td></tr>
<tr><td colspan="6">INSTRUCTIONAL OBJECTIVES</td></tr>
<tr><td>1.</td><td colspan="5">To gain knowledge on Verilog HDL language</td></tr>
<tr><td>2</td><td colspan="5">To get an insight on system C</td></tr>
<tr><td>3</td><td colspan="5">To understand the object oriented features on Verilog</td></tr>
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UNIT –I VERILOG - BASIC CONCEPTS (9 hours)

Operators, Basic concepts, Identifiers, System task and functions, Value set, Data types, Parameters ,Operands, Operators, Modules and ports, Gate-level Modeling, Dataflow Modeling, Behavioral Modeling, Test bench-lab exercise.

UNIT-II VERILOG - ADVANCED FEATURES (9 hours)

Tasks and Functions, Timing and delays, Switch level modeling, Tri state gates, MOS Switches, Bidirectional switches, User defined primitives, Combinational UDP, Sequential UDP, lab exercise. Introduction to synthesis,Verilog HDL synthesis-Synthesis Design flow –lab exercise.

UNIT-III SYSTEM VERILOG - INTRODUCTION (9 hours)

Introduction to System Verilog – Literal values-data Types, Arrays, Data Declarations-attributes-operators, expressions, procedural statements and control flow. Processes in System Verilog – Task and functions.

UNIT-IV OBJECT ORIENTED ANALYSIS IN SYSTEM VERILOG (9 hours)

Introduction to objects, its properties, methods, constructors- casting – chaining - Data hiding and encapsulation – polymorphism. Random constraints – randomization method. Inline constraints, Disabling random variables , controlling constraint, In-line random variable control-randomization of scope variable.

UNIT- V SYSTEM VERILOG – ADVANCED FEATURES (9 hours)

Interprocessor synchronization - communication- scheduling semantics-clocking blocks-assertions- Hierarchy-Interfaces- System Tasks and functions – system Verilog assertion API and coverage API.

REFERENCES

1. Samir palnitkar, ”Verilog HDL”, Pearson education, Second Edition,20O3.
2. J. Bhasker, A Verilog HDL Primer, Second Edition, Star Galaxy, 1999.
3. J. Bhasker, A Verilog Synthesis: A Practical Primer, Star Galaxy, 1998.
4. System Verilog 3.1a –Language Reference Manual (Accellera Extensions to Verilog 2001), 2004.

		L	T	P	C
VL2102	**NANO ELECTRONICS**	**3**	**0**	**0**	**3**
	Total Contact Hours - 45				
	Prerequisite : Nil				

PURPOSE	
As a new and expanding field, with many implications, nanotechnology and nano electronics is going to pave way for new technologies. Hence this course introduced.	
INSTRUCTIONAL OBJECTIVES	
1	To learn the various limitation on MOSFETS and the alternates.
2	To gain knowledge on SET and Carbon nano tubes in the design of transistors
3	To learn the basics of molecular electronics and spintronics.

UNIT I - LIMITATION OF MOSFETS (9 hours)

Classical mechanics and its drawbacks, Quantum mechanics, 1D problem - particle in a box, electron tunneling., MOSFET scaling, Non-uniform doping in channel, high K dielectrics, SOI MOSFET, Buried channel MOSFET, Fin FET.

UNIT II - SINGLE ELECTRONICS (9 hours)

Coulomb blockade, Electron tunnelling devices, Single electron transistors , Resonant Tunneling Diodes- principle and applications, Quantum computing, Quantum cellular automata

UNIT III- CARBON NANO TUBES (9 hours)

Carbon nano tubes – Basic structures, CNTFETs, Applications.

UNIT IV - MOLECULAR ELECTRONICS (9 hours)

Molecular wire conductance - Theories of Coherent Electron Transport in molecular junctions, Evaluation of the conductance for coherent transport, Incoherent transport and vibronic coupling, Molecular circuit elements, Circuits.

UNIT V - SPINTRONICS (9 hours)

Spin Vs charge, AMR, GMR, TMR, Spin devices- Spin valves, Magnetic tunnel junctions, Applications – memories (MRAM, STRAM), Logic device, and microwave oscillators.

REFERENCES

1. Rainer Waser, *"Nano Electronics and Information Technology: Advanced Electronic Materials and Novel Devices"*, 2nd Edition, Wiley-VCH, 2012.
2. Chonles P.Poole Jr., Frank. J. Owens, *"Introduction to Nano technology"*, John Wiley and Sons, 2009.
3. T. Pradeep, *"Nano: The essentials"*, Tata McGraw Hill, 2007.
4. Mark A. Ratner, Danill Ratner, *"Nano Technology: A Gentle Introduction to the Next Big Idea"*, Prentice Hall, 2003.

		L	T	P	C
VL2103	**LOW POWER VLSI DESIGN**	**3**	**0**	**0**	**3**
	Total Contact Hours – 45				
	Prerequisite				
	VL2001				

PURPOSE	
As there is always a need for power efficient circuits and devices, this course explain the methods for low power VLSI design.	
INSTRUCTIONAL OBJECTIVES	
1.	To design Low power CMOS designs, for digital circuits.
2.	To gain knowledge on low power circuit design styles for VLSI circuits.
3.	To understand software power estimation and optimization methods for VLSI circuits.

UNIT I - INTRODUCTION TO LOW POWER VLSI DESIGN and ANALYSIS (9hours)

Introduction to low power VLSI design-Need for low power-CMOS leakage current-static current- Basic principles of low power design-probabilistic power analysis-random logic signal-probability and frequency-power analysis techniques-signal entropy.

UNIT II - CIRCUIT LEVEL AND LOGIC LEVEL DESIGN TECHNIQUES (9hours)

Circuit - transistor and gate sizing - pin ordering - network restructuring and reorganization - adjustable threshold voltages - logic-signal gating - logic encoding. Pre-computation logic.

UNIT III - SPECIAL LOW POWER VLSI DESIGN TECHNICQUES (9 hours)

Power reduction in clock networks - CMOS floating node - low power bus - delay balancing Switching activity reduction - parallel voltage reduction - operator reduction -Adiabatic computation - pass transistor logic

UNIT IV - LOW VOLTAGE LOW POWER MEMORIES (9 hours)

Basics of SRAM- Memory cell –Pre-charge and equalization circuit decoder-ATD Sense amplifier-Output latch-Low power SRAM technologies-types of DRAM –Basics of DRAM-Cell refresh circuit-HVG-BBG-BVG-RVG-VDC

UNIT V - SOFTWARE DESIGN AND POWER ESTIMATION (9 hours)

Low power circuit design style - Software power estimation - co design, for low power.

REFERENCES

1. Gary Yeap *"Practical Low Power Digital VLSI Design"*, Springer US, Kluwer Academic Publishers, 2002.
2. Kaushik Roy, Sharat C. Prasad, "*Low power CMOS VLSI circuit design*", Wiley Inter science Publications",1987.
3. Kiat-Seng Yeo, Kaushik Roy, *"Low Voltage Low Power VLSI Subsystems"*, Tata Mc-Graw Hill, 2009.

VL2104	NEURAL NETWORKS FOR VLSI	L	T	P	C
		3	0	0	3
	Total Contact Hours - 45				
	Prerequisite - VL2002				

PURPOSE	
The purpose of this course is	
1.	To introduce neural network concepts to the student
2.	To apply artificial neural network concepts in VLSI
INSTRUCTIONAL OBJECTIVES	
1.	To gain knowledge on neural networks, its theory and various types.
2.	To acquire knowledge on implementation of neural networks for VLSI problems.
3	To learn Pulse stream technique in neural networks.

UNIT I - INTRODUCTION AND BASIC CONCEPTS (9 hours)

Introduction- Humans and Computers, the structure of the brain, learning in machines, the differences. The basic neuron- Introduction, modeling the single neuron, learning in simple neurons, the perception: a vectorial perspective, the perception learning rule, proof, limitations of perceptrons.

UNIT II - MULTILAYER NETWORKS (9 hours)

The multi layer perceptron: Introduction, altering the perception model, the new model, the new learning rule, multi layer perception algorithm, XOR problem.

Multi layer feed forward networks, error back propagation training algorithm: problems with back propagation, Boltzman training, Cauchy training, combined back propagation, Cauchy training.

UNIT III - NEURAL VLSI (9 hours)

Hopfield memories – the first generation of neural network VLSI, Pattern classification using neural networks, Computational requirement, MOSFET equations – a crash course, Digital accelerators, Op-amps and resistors, Superthreshold circuits for neural networks, Analogue/Digital combinations, MOS transconductance multiplier, MOSFET analogue multiplier, Imprecise low-area multiplier, Analogue , programmable – Intel Electronically Trainable Artificial Neural Network (ETANN) chip, Analogue synaptic weight storage – Dynamic weight storage, Metal Nitride Oxide Silicon(MNOS) networks, Floating-gate technology, Amorphous silicon synapses

UNIT IV - PULSE STREAM TECHNIQUE (9 hours)

Pulse encoding of information, Pulse stream arithmetic – addition and multiplication, Pulse stream communication, Pulse stream case studies – Edinburg SADMANN/ EPSILON work, The EPSILON chip, Process invariant summation and multiplication – the synapse, Pulse frequency modulation neuron, Pulse width modulation neuron, Switched-capacitor design, Per-pulse computation, EPSILON – The chosen neuron/synapse cells and results

UNIT V - APPLICATIONS OF NEURAL VLSI (9 hours)

Real time speech recognition, Applications of neural VLSI – dedicated systems, Hardware co-processors, Embedded neural systems, The future - Hardware learning with multi-layer perceptrons, The top-down approach: Virtual Targets, The bottom-up approach : weight perturbation, Test problem, Weight perturbation for hardware learning, Noisy synaptic arithmetic – an analysis, Noise in training , On-chip learning.

REFERENCES

1. R Beale and T Jackson, *"Neural Computing, An Introduction"*, Adam Hilger, 1990.
2. Freeman J.A. and Skapura B.M, *"Neural Networks, Algorithms Applications and Programming Techniques"*, Addison Wesely, 1991.
3. Alan Murray and Lionel Tarassenko , *"Analogue Neural VLSI"*, ChapmanandHall, 1994.

<table>
<tr><td rowspan="5">VL2105</td><td></td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>VLSI DIGITAL SIGNAL PROCESSING SYSTEMS</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td colspan="5">Total Contact Hours - 45</td></tr>
<tr><td colspan="5">Prerequisites</td></tr>
<tr><td colspan="5">VL2003</td></tr>
<tr><td colspan="6">PURPOSE</td></tr>
<tr><td colspan="6">As DSP has become an essential component of VLSI applications, this Course discusses implementation methods and problems in optimization algorithm of VLSI DSP Systems.</td></tr>
<tr><td colspan="6">INSTRUCTIONAL OBJECTIVES</td></tr>
<tr><td>1.</td><td colspan="5">To know the various methods for implementation of DSP systems.</td></tr>
<tr><td>2</td><td colspan="5">To understand the various implementations of VLSI DSP architectures for Arithmetic operations</td></tr>
<tr><td>3</td><td colspan="5">To gain knowledge on low power DSP architectures.</td></tr>
</table>

UNIT I - UNFOLDING (9 hours)

Algorithm for Unfolding- Properties of Unfolding- Critical Path- Unfolding and Retiming- Applications of Unfolding. Folding: Folding Transformation- Register Minimization Techniques- Lifetime analysis-Data Allocation using forward-Backward register Allocation- Register Minimization in Folded Architectures- Folding of Multirate Systems.

UNIT II - DIGITAL MULTIPLIER ARCHITECTURES (8 hours)

Parallel Multipliers- Interleaved Floor-plan and Bit-Plane-Based Digital Filters- Bit-Serial Multipliers- Bit-serial Filter Design and Implementation- Canonic Signed Digit Arithmetic- Distributed Arithmetic.

UNIT III - REDUNDANT ARITHMETIC (11 hours)

Redundant Number Representations- Carry-Free Radix-2 Addition and Subtraction- Hybrid Radix-4 Addition- Radix-2 Hybrid Redundant Multiplication Architectures- Data Format Conversion- Redundant to Non redundant Converter . Numerical Strength Reduction: Sub expression Elimination- Multiple Constant Multiplication- Sub expression sharing in Digital Filters- Additive and Multiplicative Number Splitting.

UNIT IV - SYNCHRONOUS AND ASYNCHRONOUS PIPELINING (9 hours)

Synchronous Pipelining and Clocking Styles- Clock Skew and Clock Distribution in Bit-Level Pipelined VLSI Designs- Wave Pipelining- Constraint Space Diagram and Degree of Wave Pipelining- Implementation of Wave-Pipelined Systems- Asynchronous Pipelining- Signal Transition Graphs- Use of STG to Design Interconnection Circuits- - Implementation of Computational Units.

UNIT V - LOW POWER VLSI DSP SYSTEMS (8 hours)

Theoretical Background- Scaling Versus Power Consumption- Power Analysis- Power Reduction Techniques- Power Estimation Approaches.-Simulation Based Approach.

REFERENCES

1. K.K Parhi, *"VLSI Digital Signal processing"*, John-Wiley 2008.
2. Behrooz Parhami, *"Computer Arithmetic : Algorithms and Hardware Designs"*, Oxford University Press, 2^{nd} Edition, 2010.

<table>
<tr><td rowspan="4">VL2106</td><td></td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>ASIC DESIGN</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td colspan="5">Total Contact Hours - 45</td></tr>
<tr><td colspan="5">Prerequisite : Nil</td></tr>
<tr><td colspan="6">PURPOSE</td></tr>
<tr><td colspan="6">As VLSI implementation is largely in ASIC this subject is introduced here.</td></tr>
<tr><td colspan="6">INSTRUCTIONAL OBJECTIVES</td></tr>
<tr><td>1</td><td colspan="5">To learn the fundamentals of ASIC and its design methods</td></tr>
<tr><td>2.</td><td colspan="5">To gain knowledge on programmable architectures for ASICs</td></tr>
<tr><td>3.</td><td colspan="5">To understand the physical design of ASIC.</td></tr>
</table>

UNIT I - INTRODUCTION TO ASIC'S (7 hours)

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell - Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort -Library cell design - Library architecture .

UNIT II - PROGRAMMABLE ASIC'S (9 hours)

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA -Altera FLEX - Altera MAX DC and AC inputs and outputs - Clock and Power inputs - Xilinx I/O blocks.

UNIT III - PROGRAMMABLE ASIC LOGIC CELLS (9 hours)

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX -Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV - ASIC FLOOR PLANNING, PLACEMENT AND ROUTING (11 hours)
ASIC Construction: Physical Design- System Partitioning- FPGA Partitioning- Partitioning Methods. Floorplanning and Placement: Floorplanning- Placement- Physical Design Flow. Routing: Global Routing - Detailed Routing- Special Routing. Design checks

UNIT V - OPTIMIZATION ALGORITHMS (9 hours)
Planar subset problem(PSP) -single layer global routing single layer detailed routing wire length and bend minimization technique-over the cell(OTC) Routing-multichip modules(MCM)-Programmable logic arrays-Transistor chaining-Weinberger Arrays-Gate Matrix Layout-1D compaction-2D compaction

REFERENCES

1. M. J. S. Smith, *"Application Specific Integrated Circuits"*, Addison -Wesley Longman Inc., 1997.
2. Farzad Nekoogar and Faranak Nekoogar, *"From ASICs to SOCs: A Practical Approach"*, Prentice Hall PTR, 2003.

		L	T	P	C
VL2107	**CMOS MIXED SIGNAL CIRCUIT DESIGN**	**3**	**0**	**0**	**3**
	Total Contact Hours – 45				
	Prerequisite - VL2002,VL2004				
PURPOSE					
As many real life applications involve both analog and digital circuits, this course aims to introduce the problems in implementing Analog and Digital Circuits in a single silicon wafer.					
INSTRUCTIONAL OBJECTIVES					
1.	To know mixed signal circuits like DAC, ADC, PLL etc.				
2.	To gain knowledge on filter design in mixed signal mode.				
3.	To acquire knowledge on design different architectures in mixed signal mode.				

UNIT I - PHASE LOCKED LOOP (9 hours)
Characterization of a comparator, basic CMOS comparator design, analog multiplier design, PLL - simple PLL, charge-pump PLL, applications of PLL.

UNIT II - SAMPLING CIRCUITS (9 hours)
Basic sampling circuits for analog signal sampling, performance metrics of sampling circuits, different types of sampling switches. Sample-and-Hold Architectures- Open-loop and closed-loop architectures, open-loop architecture with miller capacitance, multiplexed-input architectures, recycling architecture, switched capacitor architecture, current-mode architecture.

UNIT III - D/A CONVERTER ARCHITECTURES (9 hours)
Input/output characteristics of an ideal D/A converter, , performance metrics of D/A converter, D/A converter in terms of voltage, current, and charge division or multiplication, switching functions to generate an analog output corresponding to a digital input. Resistor-Ladder architectures, current-steering architectures.

UNIT IV - A/D CONVERTER ARCHITECTURES (9 hours)

Input/output characteristics and quantization error of an A/D converter, performance metrics of pipelined architectures, Successive approximation architectures, interleaved architectures.

UNIT V - INTEGRATOR BASED FILTERS (9 hours)

Low Pass filters, active RC integrators, MOSFET-C integrators, transconductance-c integrator, discrete time integrators. Filtering topologies - bilinear transfer function and biquadratic transferfunction.

REFERENCES

1. Razavi, *"Design of analog CMOS integrated circuits"*, McGraw Hill, Edition 2002.
2. Razavi, *"Principles of data conversion system design"*, Wiley IEEE Press, 1st Edition, 1994.
3. Jacob Baker, *"CMOS Mixed-Signal circuit design"*, IEEE Press, 2009.
4. Gregorian, Temes, *"Analog MOS Integrated Circuit for signal processing"*, John Wiley and Sons, 1986.
5. Baker, Li, Boyce, *"CMOS : Circuit Design, layout and Simulation"*, PHI, 2000.

<table>
<tr><td rowspan="4">VL2108</td><td></td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>DSP ARCHITECTURE AND APPLICATIONS</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td colspan="5">Total Contact Hours – 45</td></tr>
<tr><td colspan="5">Prerequisite - VL2003</td></tr>
<tr><td colspan="6">PURPOSE</td></tr>
<tr><td colspan="6">This course introduces Digital Signal processors.</td></tr>
<tr><td colspan="6">INSTRUCTIONAL OBJECTIVES</td></tr>
<tr><td>1.</td><td colspan="5">To know various DSP architectures and their applications.</td></tr>
<tr><td>2.</td><td colspan="5">To gain technical knowhow of various DSP processors</td></tr>
</table>

UNIT I - OVERVIEW OF DIGITAL SIGNAL PROCESSING (9 hours)

Advantages of DSP over analog systems, salient features and characteristics of DSP systems, applications of DSP systems. Common features of DSP processors, numeric representations in DSP processor, data path of a DSP processor, memory structures in DSP processors, VLIW architecture, special addressing modes in DSP processors, pipelining concepts, on-chip peripherals found in DSP processors.

UNIT II - TMS320C5X PROCESSORS (9 hours)

Architecture of TMS320C5X Processors- Assembly Instructions- Addressing Modes- Pipelining and Peripherals-Lab exercises

UNIT III - TMS320C3X PROCESSORS (9 hours)

Architecture of TMS320C3X- Instruction Set- Addressing Modes- Data Formats- Floating Point Operation- Pipelining and Peripherals- Lab exercises

UNIT IV - BLACK FIN PROCESSOR **(9 hours)**
Introduction to Black fin processor- Architecture overview-processor core-addressing modes-instruction sets-Targeted applications - Lab exercises.

UNIT V - SHARC PROCESSOR **(9 hours)**
VLIW Architecture- SHARC- SIMD- MIMD Architectures- Application: Adaptive filters-DSP based biometry receiver-speech processing-position control system for hard disk drive-DSP based power meter.

REFERENCES

1. B.Venkatramani and M.Baskar, *"Digital Signal Processor"*, Tata McGraw Hill, 4th Edition, 2008.
2. Avatar Singh and S.Srinivasan, *"Digital signal processing"*, Thomson books, 2004.
3. K.K Parhi, *"VLSI DSP Systems"*, John Wiley, 2008.

		L	T	P	C
VL2109	**DESIGN OF SEMICONDUCTOR MEMORIES**	**3**	**0**	**0**	**3**
	Total Contact Hours - 45				
	Prerequisites - VL2002				

PURPOSE	
Memory is an important part in many digital circuits and microcontrollers. This course discusses implementation methods and problems in designing and making semiconductor memories.	
INSTRUCTIONAL OBJECTIVES	
1.	To know the design of MOS memories and the various precautionary methods to be used in their design.
2.	To gain knowledge on various testing methods of semiconductor memories.
3.	To get an overview on reliability of semiconductors.

UNIT I - RAM **(9 hours)**
SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOl) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs.
DRAM Technology Development-CMOS DRAMs - DRAMs Cell Theory and Advanced Cell Strucutures - BiCMOS, DRAMs - Soft Error Failures in DRAMs - Advanced DRAM Designs and Architecture-Application Specific DRAMs.

UNIT II - NONVOLATILE MEMORIES **(9 hours)**
Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-BipolarPROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) Eproms-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-AdvancedFlash Memory Architecture.

UNIT III- MEMORY FAULT MODELING AND TESTING (9 hours)

RAM Fault Modelling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing-Non-volatile Memory Modelling and Testing-IDDQ Fault Modelling and Testing-Application Specific Memory Testing

UNIT IV - SEMICONDUCTOR MEMORY RELIABILITY (9 hours)

General Reliability Issues-RAM Failure Modes and Mechanism-Non-volatile Memory Reliability-Reliability Modelling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification.

UNIT V- ADVANCED MEMORY TECHNOLOGIES (9 hours)

Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs - Analog Memories-Magneto-resistive Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

REFERENCES

1. Ashok K. Sharma, *"Semiconductor Memories", Two-Volume Set,* Wiley-IEEE Press, 2003.
2. Brent Keeth, R. Jacob Baker, Brian Johnson, Freng Lin, *"DRAM Circuit Design : Fundamental and High Speed Topics",* Wiley-IEEE Press, 2nd Edition, 2008.
3. Betty Prince, *"High Performance Memories: New Architecture DRAMs and SRAMs - Evolution and Function",* Wiley, Revised Edition, 1999.

		L	T	P	C
VL2110	**SYSTEM-ON-CHIP DESIGN**	**3**	**0**	**0**	**3**
	Total Contact Hours – 45				
	Prerequisite : Nil				
PURPOSE					
IP cores and application specific design is becoming the order of the day. Because of usefulness of this for both VLSI and embedded students this subject is provided.					
INSTRUCTIONAL OBJECTIVES					
1.	To learn System on chip fundamentals, their applications.				
2.	To gain knowledge on NOC design.				
3.	To learn the various computation models of SOCs				

UNIT I - INTRODUCTION (9 hours)

Introduction to SoC Design., Platform-Based SoC Design., Multiprocessor SoC and Network on Chip, Low-Power SoC Design

UNIT II - SYSTEM DESIGN WITH MODEL OF COMPUTATION AND CO-DESIGN (9 hours)

System Models, Validation and Verification, Hardware/Software Codesign Application Analysis, Synthesis.

UNIT III - COMPUTATION–COMMUNICATION PARTITIONING AND NETWORK ON CHIP-BASED SOC (9 hours)

Communication System: Current Trend, Separation of Communication and Computation. Communication-Centric SoC Design, Communication Synthesis, Network-Based Design, Network on Chip, Architecture of NoC

UNIT IV - NOC DESIGN (9 hours)

Practical Design of NoC, NoC Topology-Analysis Methodology, Energy Exploration, NoC Protocol Design, Low-Power Design for NoC: Low-Power Signaling, On-Chip Serialization, Low-Power Clocking, Low-Power Channel Coding, Low-Power Switch, Low-Power Network on Chip Protocol

UNIT V - NOC /SOC CASE STUDIES (9 hours)

Real Chip Implementation-BONE Series-,BONE 1-4, Industrial Implementations-,Intel's Tera-FLOP 80-Core NoC, Intel's Scalable Communication Architecture, Academic Implementations-FAUST, RAW; design case study of SoC –digital camera

REFERENCES

1. Hoi-jun yoo, Kangmin Lee, Jun Kyoung kim, *"Low power NoC for high performance SoC desing"*,CRC press, 2008.
2. Vijay K. Madisetti Chonlameth Arpikanondt, *"A Platform-Centric Approach to System-on-Chip (SOC) Design"*, Springer, 2005.

		L	T	P	C
VL2111	**GENETIC ALGORITHMS AND APPLICATIONS IN VLSI**	**3**	**0**	**0**	**3**
	Total Contact Hours - 45				
	Prerequisite: VL2005, VL2007				

PURPOSE	
Optimization methods are necessary for making circuits and making device layouts. This course deals with Genetic Algorithm as an optimization application for VLSI design.	
INSTRUCTIONAL OBJECTIVES	
1.	To gain knowledge on Genetic algorithms
2.	To learn implementation of genetic algorithms for VLSI physical design problems
3	To understand implementation of genetic algorithms for testing of VLSI circuits and technology mapping.

UNIT I - FUNDAMENTALS OF GENETIC ALGORITHM (9 hours)

Terminologies – Simple Genetic algorithms – steady state algorithm – Genetic operators-types of GA-Genetic algorithms vs. Conventional algorithms – GA example – GA for VLSI design, layout and test automation.

UNIT II - PARTITIONING (9 hours)

Problem description – Circuit partitioning by genetic algorithms – hybrid genetic algorithms for ratio-cut partitioning.

UNIT III - PLACEMENT AND ROUTING (9 hours)

Placement: Standard cell placement – Macro cell placement – Standard cell placement on a network of workstations

Routing: Steiner problem in graph – macro cell global routing

UNIT IV - GENETIC ALGORITHMS IN VLSI TESTING (9 hours)

Problem description – test generation frame work – test generation for test applications time reduction – deterministic/genetic test generators sequences-dynamic test sequence compaction – parallel algorithms for ATPG

UNIT V - FPGA TECHNOLOGY MAPPING and PEAK POWER ESTIMATION (9 hours)

FPGA technology mapping: Circuit segmentation and FPGA mapping-circuit segmentation for Pseudo-Exhaustive testing. Peak power estimation: Problem description – application of GA – Estimation of peak single cycle and n-cycle powers-peak sustainable power estimation.

REFERENCES

1. Pinaki mazumder and Elizabeth M Rudnick,"*Genetic algorithms for VLSI design layout and test automation*", Pearson Edition, 2011.
2. David E Goldberg, "*Genetic algorithms in search, optimization and machine learning*", Addison-Wesley, Longman Publishing Co., Inc. Boston, MA, USA, 2009.

<table>
<tr><td rowspan="4">VL2112</td><td></td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>RELIABILITY ENGINEERING</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td colspan="5">Total Contact Hours - 45</td></tr>
<tr><td colspan="5">Prerequisites : Nil</td></tr>
<tr><td colspan="6">PURPOSE</td></tr>
<tr><td colspan="6">For any system reliability is an essential parameter. For evaluating reliability of designs, it is necessary to know reliability analysis methods.</td></tr>
<tr><td colspan="6">INSTRUCTIONAL OBJECTIVES</td></tr>
<tr><td>1.</td><td colspan="5">To learn basics of reliability evaluation methods</td></tr>
<tr><td>2.</td><td colspan="5">To understand its application to electronic circuit.</td></tr>
<tr><td>3.</td><td colspan="5">To understand the various Failure modes of many electronic components.</td></tr>
</table>

UNIT I - RELIABILITY AND RATES OF FAILURE (9 hours)

Statistical distribution , statistical confidence and hypothesis testing ,probability plotting techniques - Weibull, extreme value ,hazard, binomial data; Analysis of load - strength interference , Safety margin and loading roughness on reliability.

UNIT II - STATISTICAL EXPERIMENTS (9 hours)

Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis ,petric Nets, State space Analysis, Monte Carlo simulation, Design analysis methods - quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III - ELECTRONIC SYSTEMS AND SOFTWARE RELIABILITY (9 hours)

Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV - RELIABILITY TESTING (9 hours)

Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V - RELIABILITY IN MANUFACTURE AND MAINTENANCE (9 hours)

Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programmes , reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

REFERENCES

1. Lewis, "*Introduction to Reliability Engineering*", Wiley International,2nd Edition, 1996.
2. Patrick D.T. O'Commer, David Newton and Richard Bromley, "*Practical Reliability Engineering*", John Wiley and Sons, 4th Edition, 2002.

<table>
<tr><td rowspan="4">VL2113</td><td></td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>FUNDAMENTALS AND APPLICATIONS OF MEMS</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td colspan="5">Total Contact Hours - 45</td></tr>
<tr><td colspan="5">Prerequisites : Nil</td></tr>
<tr><td colspan="6">PURPOSE</td></tr>
<tr><td colspan="6">MEMS technology offers many exciting opportunities in miniaturization of elements in a wide range of applications. MEMS based sensors and actuators are constantly introduced into new products and new markets are expected to become affected by MEMS technology in the near future. The diversity and complexity of this technology demands a wide knowledge base from a prospect researcher. The goal of this course is to provide the student the needed background to comprehend existing technology, the tools to execute MEMS fabrication and the expertise to approach the development of new MEMS tools.</td></tr>
<tr><td colspan="6">INSTRUCTIONAL OBJECTIVES</td></tr>
<tr><td>1.</td><td colspan="5">To familiarize with MEMS Materials and Scaling Laws in Miniaturation.</td></tr>
<tr><td>2.</td><td colspan="5">To revive various concepts of Engineering Mechanics and Thermo fluid Engineering for Microsystems Design.</td></tr>
<tr><td>3.</td><td colspan="5">To study Microsystems Fabrication Process.</td></tr>
<tr><td>4.</td><td colspan="5">To familiarize with Microsystems Design, Assembly and Packaging.</td></tr>
<tr><td>5.</td><td colspan="5">To explore on various Case Study of MEMS Devices.</td></tr>
</table>

UNIT I - OVERVIEW OF MEMS AND MICROSYSTEMS, MEMS MATERIALS AND SCALING LAWS IN MINIATURATION (9 hours)

MEMS and Microsystems - Microsystems and microelectronics, Microsystems and miniaturization, Working principle of micro system - Micro sensors, Micro actuators, MEMS with Micro actuators.

Materials For MEMS - Substrate & wafer, Si as a substrate material, Si compound, Si Piezo-resistors, Gallium Arsenide, quartz, Piezoelectric crystals, polymers packaging Materials.

Scaling Laws in Miniaturization-Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling in Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer

UNIT II - ENGINEERING MECHANICS AND THERMOFLUID ENGINEERING FOR MICROSYSTEMS DESIGN (9 hours)

Atomic structure of matter, Ions and ionization, Molecular theory of matter and intermolecular forces, Doping of semiconductors, Diffusion process, Plasma physics, Electrochemistry, Static bending of thin plates, Mechanical vibration analysis, Thermo mechanical analysis, Overview of finite element analysis.

Thermo fluid Engineering-Characteristics of Moving Fluids, The Continuity Equation, The Momentum Equation, Incompressible Fluid Flow in Microconduits, Overview of Heat Conduction in Micro Structures.

UNIT III - MICROSYSTEMS FABRICATION PROCESS (9 hours)

Fabrication Process - Photolithography, Ion implantation, Oxidation, Chemical vapor deposition (CVD), Physical vapor deposition, Deposition by Epitaxy, Etching. Manufacturing Process - Bulk Micromachining, Surface Micromachining and LIGA Process.

UNIT IV - MICROSYSTEMS DESIGN, ASSEMBLY AND PACKAGING (9 hours)

Micro system Design - Design consideration, process design, Mechanical design, Mechanical design using MEMS. Mechanical packaging of Microsystems, Microsystems packaging, interfacings in Microsystems packaging, packaging technology, selection of packaging materials, signal mapping and transduction.

UNIT V - CASE STUDY OF MEMS DEVICES (9 hours)

Case study on strain sensors, Temperature sensors, Pressure sensors, Humidity sensors, Accelerometers, Gyroscopes , RF MEMS Switch, phase shifter, and smart sensors. Case study of MEMS pressure sensor Packaging.

REFERENCES

1. *“MEMS and Microsystems: design , manufacture, and nanoscale Engineering,”* 2nd Edition, by Tai-Ran Hsu, John Wiley and Sons, Inc., Hoboken, New Jersey, 2008.
2. Chang Liu, *“Foundations of MEMS*”, Pearson Indian Print, 1st Edition, 2012.
3. Gabriel M Rebeiz, *"RF MEMS - Theory Design and Technology",* John Wiley & Sons, 2004.
4. Julian W Gardner, *"Microsensors MEMS and smart devices"*, John Wiley and sons Ltd, 2001.

<table>
<tr><td rowspan="4">VL2114</td><td></td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>RF VLSI DESIGN</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td colspan="5">Total Contact Hours - 45</td></tr>
<tr><td colspan="5">Prerequisites - VL2004</td></tr>
<tr><td colspan="6">PURPOSE</td></tr>
<tr><td colspan="6">The explosive growth in wireless telecommunications, expects the design of RF circuits with low power consumption and Low noise. This course aims to introduce the design of CMOS RF circuits suitable for transmitter and receiver architectures.</td></tr>
<tr><td colspan="6">INTRUCTIONAL OBJECTIVES</td></tr>
<tr><td>1.</td><td colspan="5">To explore the various performance measures of RF circuits.</td></tr>
<tr><td>2.</td><td colspan="5">To acquire knowledge on the design of RF filters, amplifiers and oscillators</td></tr>
</table>

UNIT I - PERFORMANCE PARAMETERS OF RF CIRCUITS (9 hours)

Gain Parameters, Non-linearity parameters, Noise figure, Phase Noise, Dynamic range, RF front end performance parameters, performance trade offs in an RF circuit.

UNIT II - FILTER DESIGN (9 hours)

Modern filter design, Frequency and impedance scaling, High Pass filter design, Band pass filter design, Band reject filter design, the effects of finite Q.

UNIT III - HIGH FREQUENCY AMPLIFIER DESIGN (9 hours)

Zeros as Bandwidth enhances, Shunt-series Amplifier, Bandwidth enhancement with frequency Doublers, Tuned amplifiers, Neutralization and unilateralization, cascaded Amplifiers, LNA Topologies.

UNIT IV - MIXERS AND OSCILLATORS (9 hours)

Mixer fundamentals, Non linear systems as Linear mixers, multiplier based mixers, Subsampling mixers.

Problems with purely linear oscillators, Tuned oscillator, Negative Resistance oscillators, frequency synthesis.

UNIT V - RF POWER AMPLIFIERS (9 hours)

General considerations, Class A, AB, B and C Power amplifier, Class D, E and F amplifiers, modulation of power amplifiers, RF Power amplifier design examples.

REFERENCES

1. Aleksandar Tasic, Wouter.A.Serdijn, John.R.Long, *"Adaptive Low Power Circuits for Wireless Communication (Analog Circuits and Signal Processing)"*, Springer, 1st Edition, 2006.
2. Chris Bowick, *"RF Circuit design"*, Newnes (An imprint of Elesvier Science), 1st Edition, 1997.
3. Thomas.H. Lee, *"The design of CMOS Radio-Frequency Integrated Circuits"*, Cambridge University Press, 2nd Edition, 2004.

<table>
<tr><td rowspan="4">VL2115</td><td></td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>HIGH SPEED VLSI</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td colspan="5">Total Contact Hours - 45</td></tr>
<tr><td colspan="5">Prerequisites - VL2001</td></tr>
<tr><td colspan="6">PURPOSE</td></tr>
<tr><td colspan="6">This course is aimed at providing high speed design techniques for use in VLSI design</td></tr>
<tr><td colspan="6">INSTRUCTIONAL OBJECTIVES</td></tr>
<tr><td>1.</td><td colspan="5">To gain knowledge on circuits and techniques involved in high speed VLSI circuits.</td></tr>
<tr><td>2.</td><td colspan="5">To explore various design strategies to be followed for designing a high speed VLSI circuits.</td></tr>
<tr><td>3.</td><td colspan="5">To understand the logic styles for designing a high speed VLSI circuit.</td></tr>
</table>

UNIT I - CLOCKED LOGIC STYLES (9 hours)
Clocked Logic Styles, Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clocked pass Gate Logic Non Clocked Logic Styles, Static CMOS, DCVS Logic, Non-Clocked pass Gate Families.

UNIT II - CIRCUIT DESIGN MARGINING AND DESIGN VARIABILITY (9 hours)
Circuit Design Margining, Design Induced Variations, Process Induced Variations, Application Induced Variations, Noise.

UNIT III - LATCHING STRATEGIES (9 hours)
Latching Strategies, Basic Latch Design, Latching Differential Logic, Race Free Latches for Pre-charged Logic, Asynchronous Latch Techniques.

UNIT IV - INTERFACE TECHNIQUES (9 hours)
Signaling Standards, Chip-to-Chip Communication Networks, ESD Protection, Skew Tolerant Design

UNIT V - CLOCKING STYLES (9 hours)
Clocking Styles, Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques.

REFERENCES

1. Kerry Bernstein, Keith M. Carrig, “*High Speed CMOS Design Styles*”, Kluwer Academic Publishers, 2002.
2. Evan Sutherland, Bob Stroll, David Harris,” *Logical Efforts, Designing Fast CMOS Circuits*”, Kluwer Academic Publishers, 1999
3. David Harris, “*Skew Tolerant Domino Design*”, IEEE Journal of Solid State Circuits, 2001.

VL2116		L	T	P	C
	MAGNETO-ELECTRONICS	**3**	**0**	**0**	**3**
	Total Contact Hours - 45				
	Prerequisite : Nil				
PURPOSE					
To impart the applications of magnetism in the filed of electronics					
INSTRUCTIONAL OBJECTIVES					
1.	To gain knowledge on nanomagnetics				
2.	To obtain skill of nanomagnetism in various applications like Memory, Digital Logic, etc.				
3.	To acquire knowledge on software skills in n-mag simulation tool for micro magnetics.				

UNIT I - INTRODUCTION TO MAGNETOELECTRONICS (9 hours)

Introduction – What is magnetoelectronics –Key Engineering Issues Magnetoelectronics must solve –Spin vs Charge – Transport in Semiconductors, Metals- Spin-Polarized Current – Spin-Dependent Tunneling in Magnetic Tunnel Junction

UNIT II - SPIN VALVES (9 hours)

Introduction – Giant magneto resistance –Semi classical theory of CIP Giant Magnetoresistance – Current Perpendicular to Plane Giant Magnetoresistance – Spin Valve – Magnetic Properties - Spin Valves in Magnetoresistive Read Heads – Current Distribution and Magnetic Field due to Sense Current Acting on the Free Layer – SNR in Spin-Valve element -GMR MRAM.

UNIT III - MAGNETIC TUNNEL JUNCTION (9 hours)

Introduction – Superconductive Tunneling – Spin Effects is Superconductors – Superconductor-ferromagnet Tunneling – Spin-Filter Effect =Ferromagnetic-Ferromagnetic Tunneling – Early Experiments by Julliere and others – Recent Experiments and Basic Properties – Bias Voltage Dependence – Exchange Biasing of Tunnel Junctions – Temperature Effects – Barrier Dopant Effects - Observation of Resonant Effect in MTJs - Tunneling and the role of the Interface .

UNIT IV - MAGNETORESISTIVE RANDOM ACCESS MEMORY (9 hours)

Intro. to MRAM – Pseudo-Spin valve MRAM – Magnetic Tunnel Junction MRAM - MRAM Development-– Programming – MRAM Bit Cell Architecture – Improving Write Select Margins – Extending Density/Reducing Write Currents - Savtchenko Switching – Toggle MRAM.

UNIT V - MICROMAGNETIC SIMULATION (9 hours)

Nmag – Over view of Nmag – Command Line Launching– The 2D Micromagnetic Solver - Command Line Utilities – Nmag for simulation of MTJs.

REFERENCES

1. Mark Johnson, “*Magnetoelectronics*”, Academic Press (An Imprint of Elsevier), 2005.
2. Sadamichi Maekawa and Teruya Shinjo, “*Spin Dependent Transport in Magnetic Nanostructure*”, Taylor and Francis Inc, CRC Press, 2010.
3. John C. Mallinson, “*Magneto-Resistive and Spin Valve Heads Fundamentals and Application*”, Academic Press, 2002.
4. J. St¨ohr H.C. Siegmann, “*Magnetism From Fundamentals to Nanoscale Dynamics*”, Springer, 2006.

<table>
<tr><td rowspan="4">VL2117</td><td></td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>VLSI INTERCONNECTS AND ITS DESIGN TECHNIQUES</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td colspan="5">Total Contact Hours – 45</td></tr>
<tr><td colspan="5">Prerequisites : Nil</td></tr>
<tr><td colspan="6">PURPOSE</td></tr>
<tr><td colspan="6">VLSI interconnects modeling is playing vital role in the IC design.</td></tr>
<tr><td colspan="6">INSTRUCTIONAL OBJECTIVES</td></tr>
<tr><td>1.</td><td colspan="5">To gain knowledge on VLSI Interconnects</td></tr>
<tr><td>2</td><td colspan="5">To get an insight on Transmission line parameters of VLSI interconnects</td></tr>
<tr><td>3</td><td colspan="5">To understand the novel solutions on interconnects.</td></tr>
</table>

UNIT –I PRELIMINARY CONCEPTS OF VLSI INTERCONNECTS (9hours)

Interconnects for VLSI applications-copper interconnections –method of images- method of moments- even and odd capacitances- transmission line equations- miller's theorem- Resistive interconnects as ladder network- Propagation modes in micro strip interconnects- slow wave propagations- Propagation delay.

UNIT-II PARASITIC RESISTANCES, CAPACITANCE & INDUCTANCE (9 hours)

Parasitic resistances, capacitances and inductances- approximate formulas for inductances- green's function method: using method of images and Fourier integral approach- network Analog method- Inductance extraction using fast Henry- copper interconnections for resistance modelling .

UNIT- II INTERCONNECTION DELAYS (9 hours)

Metal insulator semiconductor micro strip line- transmission line analysis for single level interconnections- transmission line analysis for parallel multilevel interconnections- analysis of crossing interconnections- parallel interconnection models for micro strip line- modelling of lossy parallel and crossing interconnects- high frequency losses in micro strip line- Expressions for interconnection delays- Active interconnects.

UNIT-IV CROSS TALK ANALYSIS (9 hours)

Lumped capacitance approximation- coupled multi conductor MIS micro strip line model for single level interconnects- frequency domain level for single level interconnects- transmission line level analysis of parallel multi level interconnections.

UNIT-V NOVEL SOLUTIONS FOR PROBLEMS IN INTER (9 hours)

Optical interconnects – carbon Nano tubes / Graphenes vs. Copper wires.

REFERENCES

1. H B Bakog Lu, Circuits, "*Interconnections and packaging for VLSI*", Addison Wesley publishing company.
2. J A Davis, J D Meindl, "*Interconnect technology and design for Gigascale integration*", Kluwer academic publishers.

3. Nurmi J, Tenhumen H, Isoaho J, Jantsch A, “*Interconnect Centric deisgn for advanced SOC and NOC*”, Springer.
4. C K Cheng, J Lillis, S Lin, N Chang, “*Interconnect analysis and synthesis*”, Wiley inter-science.
5. Hall S H, G W Hall and J McCall, High speed digital system design, Wiley inter-science
6. Askok K Goel, “*High speed VLSI interconnections*”, Wiley inter-science, second edition, 2007.

<table>
<tr><td rowspan="4">VL2118</td><td></td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>DIGITAL HDL DESIGN AND VERIFICATION</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td colspan="5">Total Contact Hours – 45</td></tr>
<tr><td colspan="5">Pre-requisites - VL2001</td></tr>
<tr><td colspan="6">PURPOSE</td></tr>
<tr><td colspan="6">HDL programming is fundamental for VLSI design and hence this course is given.</td></tr>
<tr><td colspan="6">INSTRUCTIONAL OBJECTIVES</td></tr>
<tr><td>1.</td><td colspan="5">To gain knowledge on VHDL</td></tr>
<tr><td>2</td><td colspan="5">To get an insight on Advanced VHDL</td></tr>
<tr><td>3</td><td colspan="5">To understand the System C</td></tr>
</table>

UNIT-I VHDL- BASIC CONCEPTS (9 hours)

Operators, Basic concepts, Entity and Architecture design, System task and functions, Value set, Data types,Operands, Operators, Entity and ports, Gate-level Modeling, Dataflow Modeling, Behavioral Modeling, Test Bench- lab exercise.

UNIT-II VHDL- ADVANCED FEATURES (9 hours)

Packages and Functions, Sub-Program, User Defined Attributes, Specifications and Configurations, Delay modeling- pin-to-pin delay and distributed delay modeling- Timing delay analysis- FSM design and Synthesis-UART –lab exercise.

UNIT- III SYSTEM C – INTRODUCTION (9 hours)

Introduction to System C- Design methodology – Data Types – Bit, Logic, Integer , Precision signed type and resolved types, user defined data type- Data operators – Logical, arithmetic , relational operators, vectors and ranges- sequential statements – IF, LOOP,SWITCH statements- methods – structures .

UNIT-IV COMBINATIONAL and SYNCHRONOUS LOGIC DESIGN IN SYSTEM C (9 hours)

SC_module – File Structure, Reading and writing port signals. Miscellaneous logic – modeling basic combinational logic circuits (Multiplexer, Decoder, encoder, memory model, modeling an FSM- Moore’s and Mealy FSM – Universal Shift Register.

UNIT-V SYSTEM C – ADVANCED FEATURES **(9 hours)**

SC_THREAD process, dynamic sensitivity- constructors – arguments, Filter design - ports, interfaces and channels. Advanced Topics – shared data members, fixed point types – Module-simulation algorithm –Runtime Environment.

REFERENCES

1. Ben Cohen, "*VHDL: Coding Styles and Methodologies*", Kluwer Academic Publisher (1999), Reprint 2004
2. J. Bhaskar, "*A System C Primer*", Galaxy Publications, 2004.
3. Z. Navabi , "*VHDL: Modular Design and synthesis of cores and systems*", McGraw Hill Publications, Reprint 2005 .

		L	T	P	C
VL2119	**COMPUTATIONAL ASPECTS OF VLSI**	**3**	**0**	**0**	**3**
	Total Contact Hours - 45				
	Prerequisites : Nil				

PURPOSE	
The purpose of this course is to make the student understand the algorithms used for the VLSI design tools.	
INSTRUCTIONAL OBJECTIVES	
1.	To understand the concept of design and analysis of algorithms
2.	To learn the different models in VLSI
3.	To know the design languages in VLSI design tools
4.	To understand the algorithms for VLSI Design tools

UNIT I - ANALYSIS AND DESIGN OF ALGORITHMS **(9 hours)**

Abstract Data Types - Time and Space Analysis of Algorithms - Big Oh and Theta Notations - Average, best and worst case analysis - Simple recurrence relations and use in algorithms **–** Mappings. **Algorithms Analysis** - Sorting - Searching - Design Techniques- Greedy Methods - Dynamic Programming - Divide and Conquer - Back Tracking –Applications**.**

UNIT II - VLSI MODELS **(9 hours)**

Integrated circuits and the mead Conway rules-VLSI implementation of logic-Abstraction of VLSI circuits. **Lower bounds on area and time:** Introduction to lower bound arguments-information and crossing sequence- probabilistic circuits and algorithms – circuits with repetitive inputs.

UNIT III - ALGORITHM FOR VLSI Design **(9 hours)**

Algorithms for layout –organization with high area- Compilation and optimization algorithms.

UNIT IV - OVERVIEW OF VLSI DESIGN SYSTEMS **(9 hours)**

Design languages- CIF –CHISEL –ESIM –LGEN- LAVA- SLIM- A regular expression language.

UNIT V - ALGORITHMS FOR VLSI DESIGN TOOLS (9 hours)
Reporting Intersections of Rectangles-Circuit Extraction Algorithms-Design Rule Checking-An Algorithm for Simulation of Switch Circuits-The PI Placement and Routing System-Optimal Routing.

REFERENCES

1. Jeffrey D. Ullman, "*Computational aspects of VLSI*", Computer Science Press (1984).
2. Alfred .V. Aho, John .E. Hop croft, Jeffrey .D. Ullman, "*Data Structures and Algorithms*", Addison-Wesley Publications.,1985

		L	T	P	C
VL2120	**COMPUTATIONAL INTELLIGENCE**	**3**	**0**	**0**	**3**
	Total Contact Hours - 45				
	Prerequisites : Nil				

PURPOSE

The purpose of this course is to make the student understand the various optimization techniques and the evolutionary algorithms.

INSTRUCTIONAL OBJECTIVES

1.	To understand the concept of computational intelligence
2.	To explore genetic and evolutionary algorithms
3.	To learn the knowhow of differential evolution
4.	To understand the concept of Particle swarm optimization and ant colony algorithms

UNIT I - INTRODUCTION TO COMPUTATIONAL INTELLIGENCE (9 hours)
Computational intelligence paradigms: Artificial Neural networks, evolutionary Computation, swam intelligence, artificial immune systems and fuzzy systems. **Introduction to Evolutionary computation**: Genetic evolutionary algorithms, Representation, Initial population, fitness function, selection, reproduction of operators, stopping conditions and evolutionary computation versus classical optimization.

UNIT II - GENETIC ALGORITHMS AND PROGRAMMING (9 hours)
Genetic algorithms: Canonical GA, crossover, mutation, control parameters, GA variants, applications **Genetic programming:** Tree based representation, initial population, fitness function, cross over operators, mutation operators, building block in Genetic programming.

UNIT III - EVOLUTIONARY PROGRAMMING AND ITS STRATEGIES (9 hours)
Basic of Evolutionary programming- operators- strategy parameters- implementations- Genetic evolutionary strategy algorithms-strategy parameters and self adoption- evolution strategy variants.

UNIT IV - DIFFERENTIAL EVOLUTION (9 hours)
Basic differential evolution-Variations to basic DE- DE for discrete valued problems. **Coevolution:** Coevolution types- competitive Coevolution – co-operative Coevolution.

UNIT V - COMPUTATIONAL SWAM INTELLIGENCE **(9 hours)**

Particle swarm optimization: Basics- social network structures- Basic variations- PSO parameters- single solution PSO- applications

Ant algorithms: ant colony optimization Meta-Heuristic- Cemetery organization and brood care- division of labor-Applications

REFERENCES

1. Andries P Engel Brecht, "*Computational intelligence an introduction*", Wiley publications, 2nd Edition, 2007.
2. Goldberg," *Genetic algorithms in search, optimization and machine learning*" Pearson Education India, 2007 Edition.

		L	T	P	C
VL2121	**CHROMATIC GRAPH THEORY**	**3**	**0**	**0**	**3**
	Total Contact Hours - 45				
	Prerequisites - MA2010				
PURPOSE					
The purpose of this course is to make the student understand the basic concepts of graph theory and the coloring of graphs and role of it in VLSI CAD.					
INSTRUCTIONAL OBJECTIVES					
1.	To understand the concept of vertex coloring and edge coloring				
2.	To understand the concept of coloring on surfaces				

UNIT I - INTRODUCTION TO GRAPHS **(9 hours)**

Trees and connectivity, Eulerian and Hamiltonian Graphs- Matching and factorization.

UNIT II - INTRODUCTION TO VERTEX COLORING **(9 hours)**

Chromatic number of a graph, applications of coloring, perfect graphs- restricted vertex coloring: uniquely colorable graphs, list coloring, pre-coloring extensions of graphs.

Case studies: VLSI Partitioning as vertex coloring problem, a chaotic neural network for the graph coloring problem in VLSI channel routing and on rectangle intersection and overlap graphs for VLSI floor planning

UNIT III - BOUNDS OF CHROMATIC NUMBERING **(9 hours)**

Bounds for the chromatic number: color-critical graphs, upper bounds and greedy coloring, upper bounds and oriented graphs, the chromatic number of Cartesian product.

Coloring graphs on surfaces: four color problem, conjecture of Hajos and Hadwiger, chromatic polynomials, Heawood map-coloring.

UNIT IV - EDGE COLORING OF GRAPH **(9 hours)**

Edge coloring of graphs- monochromatic and rainbow colorings-complete coloring–distinguish coloring.

Case study: Fast approximation algorithms on max cut, k-coloring, and k-color ordering for VLSI applications and interval graph algorithms for 2D multiple folding of array based VLSI circuits

UNIT V - SPECIAL TYPES ON COLORING (9 hours)

Coloring, distance and domination: T-coloring, Radio coloring, Hamiltonian coloring, domination coloring.

Case study: A new graph coloring algorithm for constrained via minimization in VLSI circuits and Hybrid symbolic-explicit techniques for the graph coloring problem

REFERENCES

1. Gary chartrand, Ping Zhang, "*Chromatic Graph theory*", CRC Press, Edition 2009.
2. Narsingh Deo, "*Graph theory with applications to engineering and computer science*", PHI Learning Pvt. Ltd., 2004.

		L	T	P	C
VL2122	**SOLAR CELLS AND THIN FILM TECHNOLOGIES**	**3**	**0**	**0**	**3**
	Total Contact Hours - 45				
	Prerequisites				
	Nil				
PURPOSE					
Generation of electricity through solar energy is among the top priority issues in today's world. Photovoltaic cells convert solar energy in to electrical energy by separating the photo-generated electron and holes. Over the last decade, the field has emerged as an application of recognized potential and has attracted the interest of students and researchers. Newer materials and structures are being studied and new solar cell industries are coming up. In view of this there is a need to offer a dedicated **elective** course on this subject to the students at undergraduate/post graduate level.					
INSTRUCTIONAL OBJECTIVES					
The course objectives are to make sure each student:					
1.	understands the basics of light and solar irradiance				
2.	understands the basics of PN junction				
3.	understands solar cell designs				
4.	understands solar cell operation				
5.	acquires knowledge of the various solar cells technologies				

UNIT-I: SOLAR IRRADIANCE (9 hours)

Basics of light: properties of light, energy of photon, photon flux, spectral irradiance, radiant power density, black body radiation, sun radiation.

Solar Radiation: The Sun,solar radiation in space, solar radiation outside the earth's atmosphere, terrestrial solar radiation, solar radiation at the earth's surface, atmospheric effects, air mass, motion of the sun, solar time, declination angle, elevation angle, azimuth angle, the sun's position, solar radiation on a tilted surface, arbitrary orientation and tilt, calculation of solar insulation, measurement of solar radiation.

UNIT-II: PN JUNCTION (9 hours)

Basics: Semiconductor materials, semiconductor structure, conduction in semiconductor, band gap, intrinsic carrier concentration, doping, and equilibrium carrier concentration.

Generation: Absorption of light, absorption coefficient, absorption depth, generation rate.

Recombination: Types of recombination, life time, diffusion length, surface recombination.

Carrier Transport: movement of carriers in semiconductor, diffusion, drift.

PN Junction: Formation of a PN junction, PN junction diode, bias of PN junctions, diode equations, diode equation for PV, ideal diode equation derivation, basic equations, applying basic equations to a PN junction, solving for depletion region and quasi-neutral regions, finding total current.

UNIT-III: SOLAR CELLS (9 hours)

Principles of solar cell operation: Electrical characteristics, optical properties, typical solar cell structures, ideal efficiencies.

Crystalline silicon solar cells: Manufacturing and properties of Crystalline silicon, high-efficiency laboratory cells, screen-printed cells, laser-processed cells, HIT cell, rear-contacted cells, thin silicon solar cells – light trapping, voltage enhancements, silicon deposition and crystal growth.

UNIT-IV: THIN-FILM SILICON SOLAR CELLS (9 hours)

Hydrogenated amorphous silicon (a-Si:H) layers, hydrogenated microcrystalline silicon (µSi:H) layers, p-i-n and n-i-p structures, tandem and multi-junction solar cells.

UNIT-V: RECENT ADVANCES IN THIN-FILM SOLAR CELLS 9

CdTe based thin film solar cells, $CuInSe_2$ (CIS) based thin-film solar cells, thin-film GaAs solar cells, Chalcopyrite Based Solar Cells, concentrator silicon solar cells, dye-sensitized thin-film solar cells, organic solar cells

REFERENCES

1. Adrian Kitai, “Principles of Solar Cells, LEDs and Diodes: The role of the PN junction”, John Wiley and Sons, 2011.
2. AugustinMcEvoy, L. Castaner, Tom Markvart, “Solar Cells: Materials, Manufacture and Operation”, 2nd edition, Newnes, 2012.
3. Arvind Shah, “Thin-Film Silicon Solar Cells”, Illustrated edition, EPFL Press, 2010.
4. I. M. Dharmadasa, “Advances in Thin-Film Solar Cells”, Illustrated edition, CRC Press, 2012.

<table>
<tr><td rowspan="5">VL2123</td><td></td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>NEXT GENERATION PHOTOVOLTAICS</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td colspan="5">Total Contact Hours - 45</td></tr>
<tr><td colspan="5">Prerequisites - Nil</td></tr>
<tr><td colspan="5"></td></tr>
<tr><td colspan="6">PURPOSE</td></tr>
<tr><td colspan="6">Photovoltaics are regarded by many as the most likely candidate for long-term sustainable energy production. This course discusses about the new novel concepts to produce a new generation of low-cost, high performance photovoltaics that make improved use of the solar spectrum. The topics in this course include discussions on high efficiency III-V multi-junction solar cells, and new concept design solar cells including quantum well, quantum dots, intermediate-band solar cells, thermophotovoltaic cells, and other nanostructured devices. ‘Next Generation Photovoltaics’ will be an essential course for graduate students and researchers working with solar cell technology.</td></tr>
<tr><td colspan="6">INSTRUCTIONAL OBJECTIVES</td></tr>
<tr><td colspan="6">The course objectives are to:</td></tr>
<tr><td>1.</td><td colspan="5">review multijunction solar cells and the use of concentrated light</td></tr>
<tr><td>2.</td><td colspan="5">understand the potential of plasma polaritons and to master the light management</td></tr>
<tr><td>3.</td><td colspan="5">give an overview of new novel concepts and trends to produce low-cost, high performance photovoltaics</td></tr>
</table>

UNIT-I: TRENDS IN THE DEVELOPMENT OF PHOTOVOLTAICS (9 hours)

Simple structures and simple technologies, nanostructures and ‘high technologies’, multi-junction solar cells, concentration of solar radiation, concentrators in space, non-solar photovoltaics, concepts of solar cells with ultra-high frequencies – thermophotovoltaic conversion, hot carrier cells, tandem cells, intermediate level cells, photon up- and down-conversion.

UNIT-II: HIGH EFFICIENCY SOLAR DEVICES (9 hours)

III-V Multi-junction solar cells: Basic principles of multi-junction solar cells, triple-junction, four-junction, five- and six-junction solar cells, prospects of multi-junction solar cells
High concentration PV technology (HCPV): Classification, merits and status of CPV, overview of HCPV modules, RandD,

UNIT-III: THERMOPHOTOVOLTAIC (TPV) CONVERTERS (9 hours)

Progress in thermophotovoltaic converters: TPV based on III/V low-bandgap photocells, TPV in residential heating systems, progress in TPV with silicon photocells, design of a novel thin-film TPV system.
Solar cells for TPV converters: Predicted efficiency of TPV cells, Ge-based TPV cells, Si-based TPV cells, TPV cells based on InAs- and GaSb- related materials, TPV cells based on InGaAs/InPheterostructures.

UNIT-IV: NEW CONCEPTS BASED SOLAR CELLS (9 hours)

Quantum Well Cells: QW cells, strain compensation, QWs in tandem cells, QWCs with light trapping, QWCs for thermophotovoltaics

Quantum Dot solar cells: Silicon-QD solar cell, III-V multi-junction QD solar cells

Intermediate-Band Solar Cells: Preliminary concepts and definitions, IBSC model, QD IBSC

Nanowire (NW) solar cells: Silicon NW solar cells, compound semiconductor NW solar cells

NW-polymer hybrid solar cells: InP nanowire-polymer (P3HT) hybrid solar cell, microcrystalline silicon nanorods / P3HT hybrid solar cells, TiO_2 nanotube arrays in DSCs

UNIT-V: OTHER CONCEPTS (9 hours)

Light management in thin-film solar cell, Hot carrier solar cells, plasmonics photovoltaics, nanostructured materials for thin film solar cells, crystalline silicon on glass (CSG) solar cells.

REFERENCES

1. P. Jayarama Reddy, “Solar Power Generation: Technology, New Concepts and Policy”, Illustrated edition, CRC Press, 2012.
2. A. Martí, A. Luque, “Next Generation Photovoltaics: High Efficiency through Full Spectrum Utilization”, Illustrated edition, CRC Press, 2010.
3. Ana BelénCristóbalLópez, Antonio Martí Vega, Antonio LuqueLópez, “Next Generation of Photovoltaics: New Concepts”, Illustrated edition, Springer, 2012.
4. M. A. Green, “Third Generation Photovoltaics: Advanced Solar Energy Conversion”, Springer, 2006.

		L	T	P	C
VL2124	**QUANTUM COMPUTATION AND INFORMATION**	**3**	**0**	**0**	**3**
	Total Contact Hours - 45				
	Pre-requisites: Nil				
PURPOSE					
The purpose of this course is to make the student understand the computational aspects and information for designing.					
INSTRUCTIONAL OBJECTIVES					
1.	To understand the Quantum computing and Quantum information				
2.	To learn Quantum search algorithm.				
3.	To understand Quantum information theory and cryptography				

UNIT-I: INTRODUCTION (9 hours)

Quantum States - Density Operators - Generalized Measurements - Quantum Operations/Channels - No-Cloning Theorem.

UNIT-II: QUANTUM CORRELATIONS (9 hours)

Bell Inequalities And Entanglement - Schmidt Decomposition - Super-Dense Coding - Teleportation - PPT Criterion.

UNIT-III: QUANTUM GATES AND ALGORITHMS (9 hours)

Universal Set Of Gates - Quantum Circuits - Solovay-Kitaev Theorem - Deutsch-Jozsa Algorithm - Period-Finding - Factoring - Shor's Algorithm - Quantum Search - Abelian Quantum Hidden Subgroup Problem.

UNIT-IV: QUANTUM INFORMATION THEORY (9 hours)

Shannon Entropy - Noiseless Coding Theorem - Von Neumann Entropy and Properties - Schumacher Compression - Noisy-Coding Theorem.

UNIT-V: QUANTUM CRYPTOGRAPHY (9 hours)

Private Key Cryptography - Quantum Key Distribution - Entropic Uncertainty Relations – The Security of Quantum Key Distribution

TEXT-BOOKS

1. Quantum Computation and Quantum Information, M. A. Nielsen and I.Chuang, Cambridge University Press (2000).
2. A Short Introduction to Quantum Information and Quantum Computation, M. Le Bellac (Cambridge University Press, 2006)
3. Lecture notes by Prof. John Preskill, California Institute of Technology

REFERENCES

1. The mathematical language of quantum theory: from uncertainty to entanglement, T. Hienosaari and M. Ziman, Cambridge University Press (2011).
2. Quantum systems, channels, information, A.S. Holevo, de Gruyter Studies in Mathematical Physics (2012).
3. Quantum information Theory, Mark M. Wilde, Cambridge University Press (2012).
4. Quantum error correction, D. A. Lidar and T. A. Brun, Cambridge University Press (2013).

<table>
<tr><td rowspan="4">VL2125</td><td></td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>SUPERCONDUCTIVITY: THEORY & ITS EFFECTS</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td colspan="5">Total Contact Hours - 45</td></tr>
<tr><td colspan="5">Pre-requisites: Nil</td></tr>
<tr><td colspan="6">PURPOSE</td></tr>
<tr><td colspan="6">The purpose of this course is to make the student understand the basics in superconductivity</td></tr>
<tr><td colspan="6">INSTRUCTIONAL OBJECTIVES</td></tr>
<tr><td>1.</td><td colspan="5">To learn different types of superconductor types</td></tr>
<tr><td>2.</td><td colspan="5">To understand superconductor theory</td></tr>
<tr><td>3.</td><td colspan="5">To understand superconductor Effects</td></tr>
</table>

UNIT-I: INTRODUCTION (9 hours)

Basic Phenomena - Perfect Conductivity - Perfect Diamagnetism - Critical Temperature – Fields and Currents - Type-I and Type-II - High-Temperature Superconductors.

UNIT-II: BCS THEORY **(9 hours)**
Cooper Pairs – BCS Ground State – Finite Temperatures – Electron Tunneling – Electrodynamics – Penetration Depth.

UNIT-III: GINZBURG-LANDAU THEORY **(9 hours)**
GL Free Energy – GL Differential Equation – Critical Current of Thin Wire or Film – Linearized GL Equation

UNIT-IV: JOSEPHSON EFFECT-I **(9 hours)**
Josephson Critical Current – BCSJ Model – SQUID Devices: DC SQUID, RF SQUID and its Application – S-I-S Detector – S-I-S Mixer.

UNIT-V: JOSEPHSON EFFECT-II: PHENOMENA UNIQUE TO SMALL JUNCTION **(9 hours)**
Damping Effect of Lead Impedance – Quantum Consequences of small Capacitance – Single Electron Tunneling – Energy and Charging Relations in Quasi-Equilibrium – Double-Junction Circuit with Finite Bias Voltage.

TEXT-BOOKS

1. M. Tinkham, Introduction to Superconductivity, Second Edition, McGraw-Hill. This book is currently out of print, but will be republished by Dover in May, 2004.
2. Terry P. Orlando and Kevin A. Delin, Foundations of Applied Superconductivity, Addison-Wesley, Reading MA, 1991.

REFERENCES

1. T. Van Duzer, T. Van, and C. W. Turner, *Principles of Superconductive Devices and Circuits*, 2nd ed. Upper Saddle River, NJ: Prentice Hall, 1999.
2. Buckel, W., and R. Kleiner, *Superconductivity: Fundamentals and Applications*, 2nd ed. New York, NY: John Wiley and Sons, 2004.
3. Kadin, Alan M, *Introduction to Superconducting Circuits.* New York, NY: John Wiley and Sons, 1999.

		L	T	P	C
VL2126	**MULTICORE PROCESSORS AND SCHEDULING ALGORITHMS**	**3**	**0**	**0**	**3**
	Total Contact Hours-45				
	Prerequisites: NIL				
PURPOSE					
Recent Trends in developing embedded systems are multi core processors. This course gives you knowledge about real time embedded systems					
INSTRUCTIONAL OBJECTIVES					
1.	To gain knowledge in embedded multi core architecture				
2.	To learn real time scheduling Algorithm				
3.	To know details about multi core applications				

UNIT-I MULTI CORE PROCESSORS (9 hours)
Introduction-Basic Processor Architecture-Multi core embedded processors-Intel Architecture-Scalar Optimization-Usability-Parallel Optimization Using Threads.

UNIT-II-REAL TIME SCHEDULING ALGORITHM (9 hours)
Real Time Scheduling-Material Architectures-Operating Systems-Scheduling Algorithms-Real Time Application-Scheduler Classification-Properties of schedulers-Partitioned Schedulers-Global scheduling.

UNIT-III-EXECUTION TIME AND ENERGY ESTIMATION (9 hours)
Worst Case Execution Time Analysis-Multi Core and Complex Architecture-State of the art-Modelling consumptions-Low consumption scheduling-Experimental results.

UNIT-IV-DESIGN OF EMBEDDED COMPONENTS (9 hours)
Hardware Components-Firmware Components-RTOS Systems-Software Mechanisms-Software Application Components-Debugging Components-Performance Tuning-High Reliability Design.

UNIV-V-CASE STUDIES (9 hours)
System Life Cycle Application-Media Application-Robotic Application-Computer Vision Applications.

REFERENCES

1. Max Domeiko “**Software Development for embedded multi core systems**” Intel@Architecture Guide Elsevier 2008.
2. Maryline Chetto ”**Real Time system scheduling**” ISTE Wiley and John Sons, Oxford University, 1st edition 2014.
3. Sam Siewert “ **Real Time Embedded System**” ISBN,1st edition, 2007 and published by Charles River Media, Boston, Massachusetts. www.abebooks.co.uk/book-search/author/sam-siewert/
4. Arrems Hua, Shih-Liang Chang “**Algorithms and Architectures for parallel processing**” 9th International Conference Proceeedings, ICA3PP 2009 in Springer.

		L	T	P	C
	ADVANCED SEMICONDUCTOR PHYSICS	**3**	**0**	**0**	**3**
	Total Contact Hours: 45				
	Prerequisite: Nil				
PURPOSE					
This course helps to review the fundamentals of semiconductor physics and focuses on the advanced physical principles and operational characteristics of modern semiconductor electronic devices such as metal-oxide systems, bipolar, high-electron mobility, and field-effect transistors.					
INSTRUCTIONAL OBJECTIVES					
1.	To understand the advance physics of semiconductor material and electronic devices.				
2.	To be familiar with the parameters of electronic devices that governs their performance and limitation.				
3.	To understand the tendency in contemporary microelectronics and principles of the nano-scale electronic devices.				

UNIT I - BASICS OF SEMICONDUCTOR DEVICES (9 hours)

Importance of semiconductor devices and their diverse applications. Introduction to semiconductors, concept of energy bands and how bands form. Effective mass of electrons, E-k diagram. Concept of holes. Concept of Fermi level, Fermi-Dirac distribution. Doping (extrinsic and intrinsic semiconductor), density of states. Equilibrium electron-hole concentration, temperature-dependence. Carrier scattering and mobility, velocity saturation, Drift-diffusion transport.

UNIT II - QUANTITATIVE THEORY OF P-N JUNCTIONS (9 hours)

Excess carrier decay and recombination, charge injection, continuity equation, quasi-Fermi level p-n junction: static behavior (depletion width, field profile), p-n junction under forward and reverse bias, current equations, generation-recombination current and reference to typical devices.

UNIT III - OXIDE LAYERS (9 hours)

Zener and avalanche breakdown, Capacitance-voltage profiling, metal/semiconductor junction – Ohmic and Schottky contacts, reference to device applications. MOS capacitor, charge/field/energy bands, accumulation, inversion, C-V (high and low frequencies), deep depletion, Real MOS cap: Flat-band & threshold voltage, Si/SiO2 system.

UNIT IV - MOSFET AND HEMT (9 hours)

MOSFET: structure and operating principle, derivation of I-V, gradual channel approximation, substrate bias effects, sub-threshold current and gate oxide breakdown. Control of threshold voltage, short channel effects. Moore’s Law and CMOS scaling Introduction to compound semiconductors & alloys, commonly used compound semiconductors, heterostructure band diagrams and basics of MODFET and HEMT, introduction to quantum well, applications of heterostructure device technologies.

UNIT V - BJT AND HBT **(9 hours)**

BJT: working principle, DC parameters and current components, base transport factor, Early Effect, charge control equation & current gain, need for HBT. Applications of BJTs/HBTs in real-life. (Basics of) - transistors for high-speed logic, transistors for high frequency (RF), transistors for high power switching, transistors for memories, transistors for low noise, transistors for the future.

REFERENCES

1. Solid State Electronic Devices, Ben Streetman and Sanjay Banerjee, Pearson; 7 edition, 2014.
2. Introduction to Semiconductor Materials and Devices, by M. S. Tyagi, Wiley Publications, 2008.
3. Physics of Semiconductor devices; S.M.Sze, Third edition, Wiley Publications, 2008.
4. Fundamental of Semiconductor Devices; K.N.Bhat and M.K.Achuthan, McGraw Hill Education, 1st edition, 2017.

<table>
<tr><td rowspan="4">MA2010</td><td></td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>GRAPH THEORY AND OPTIMIZATION TECHNIQUES</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td colspan="5">Total Contact Hours - 45</td></tr>
<tr><td colspan="5">Prerequisite : Nil</td></tr>
<tr><td colspan="6">PURPOSE</td></tr>
<tr><td colspan="6">This course is aimed at providing graph theory and optimization techniques for use in VLSI design.</td></tr>
<tr><td colspan="6">INSTRUCTIONAL OBJECTIVES</td></tr>
<tr><td>1.</td><td colspan="5">To impart a knowledge on basics of graph theory and its algorithms</td></tr>
<tr><td>2</td><td colspan="5">To impart a knowledge on basic optimization techniques.</td></tr>
<tr><td>3</td><td colspan="5">To impart a knowledge on various statistical methods in analyzing a sample.</td></tr>
</table>

UNIT–I: BASICS OF GRAPH THEORY **(9 hours)**

graphs –data structures for graphs-sub graphs – operations on graph connectivity- networks and the maximum flow- minimum cut theorem- trees- spanning trees- Rooted trees- matrix representation of graphs.

UNIT–II: CLASSES OF GRAPH **(9 hours)**

Eulerian graphs and Hamiltonian graphs - standard theorems- planar graphs- Euler's formula – five color problem- coloring of graphs- chromatic number (vertex and edge) properties and examples- directed graphs

UNIT–III: GRAPH ALGORITHMS **(9 hours)**

Computer representation of graphs-Basic graph algorithms- minimal spanning tree algorithm - Kruskal and prim's algorithm- shortest path algorithms- Dijsktra's algorithm- DFS and BFS algorithms.

UNIT–IV: OPTIMIZATION TECHNIQUES **(9 hours)**

Linear programming- graphical methods- simplex method (Artificial variables not included) - transportation and assignment problems.

UNIT-V: STATISTICS **(9hours)**

Tchebyshev's inequality – Maximum likelihood estimation- correlation- partial correlation- multiple correlations- regression- Multiple regressions.

REFERENCES

1. S C Gupta, V K Kapoor," *Fundamentals of Mathematical statistics*", Sultan Chand and sons, 2002.
2. Narsngh Dev, "*Graph theory with applications to engineering and computer science*", Prentice Hall of IndiaLtd, 1998.
3. Hoffmann and Kunze," *Linear algebra*", PHI, 1994.
4. Rao S.S , "*Engineering optimization : Theory and practice*", New age International Pvt. Ltd, 4th edition, 2009.

		L	T	P	C
EM2101	**COMPUTER ARCHITECTURE**	**3**	**0**	**0**	**3**
	Total Contact Hours – 45				
	Prerequisite				
	NIL				
PURPOSE					
To introduce students with general concepts of computer architecture basics to enable them to use the processors effectively.					
INSTRUCTIONAL OBJECTIVES					
1.	To familiarize with fundamentals of computer design.				
2.	To learn parallel and pipeline architectures.				
3.	To learn principles of parallel programming.				

UNIT I - PROCESSOR AND MEMORY HIERARCHY **(9 hours)**

Multiprocessors and Multicomputer – Multivector and SIMD computers – Architectural Development Tracks – Processors and Memory Hierarchy – Advanced Processor Technology – Superscalar and vector Processor – Memory Hierarchy technology-Virtual memory technology.

UNIT II - FUNDAMENTALS OF COMPUTER DESIGN **(9 hours)**

Elements of modern computers-System attributes to performance-Bus, Cache and Shared memory-Bus Systems – Cache Memory Organizations – Shared memory Organization – Sequential and weak consistency models.

UNIT III - PARALLEL AND SCALABLE ARCHITECTURES **(9 hours)**

Multiprocessor System Interconnects – Cache Coherence and Synchronization Mechanisms – Message-Passing Mechanisms – Vector Processing Principles – Multivector Multiprocessors – Performance-Directed Design Rules – Fujitsu VP2000 and VPP500 – SIMD Computer Organizations – Implementation models – The MasPar MP-1 Architecture-Latency - Hiding

Techniques – Principles of Multithreading – Scalable and Multithreaded Architectures - The Tera Multiprocessor System.

UNIT IV - PIPELINING AND SUPER SCALAR TECHNIQUES (9 hours)
Introduction – Basics of a RISC Instruction set – Implementation of five stage Pipeline for a RISC processor – Performance issues – hurdle of pipelining – simple implementation of MIPS – extending the MIPS pipeline to handle multicycle operations – cross cutting issues.

UNIT V - SOFTWARE FOR PARALLEL PROGRAMMING (9 hours)
Parallel programming models – parallel languages and compliers – code optimization and scheduling – scalar optimization with basic blocks – code generation and scheduling – trace scheduling compilation – parallelization and wave fronting – software pipelining – parallel programming environments – Y-MP, Paragon and CM-5 environments – synchronization and multiprocessing modes – principles of synchronization - multiprocessor execution modes – shared-variable program structures – locks for protected access – semaphores and applications – message-passing program development.

REFERENCES

1. Kai Hwang and Naresh Jotwani, "*Advanced Computer Architecture*", McGraw –Hill, Inc. 2011.
2. John L. Hennessey and David A. Patterson, "*Computer Architecture: A Quantitative Approach*", 3rd Edition, Morgan Kaufmann, 2003.

		L	T	P	C
CO2105	**ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN**	**3**	**0**	**0**	**3**
	Total Contact Hours – 45				
	Prerequisites : Nil				
PURPOSE					
The purpose of this course is to expose the students to the basics and fundamentals of Electromagnetic Interference and Compatibility in System Design.					
INSTRUCTIONAL OBJECTIVES					
At the end of the course, student should be able to know:					
1.	EMI Environment				
2.	EMI Coupling Principles				
3.	EMI Specification, Standards and Limits				
4.	EMI Measurements and Control Techniques				
5.	EMC Design of PCBs				

UNIT I - INTRODUCTION AND SOURCES OF EMI (9 hours)
EMI/ EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD.

UNIT II - TYPES OF ELECTROMAGNETIC COUPLING **(9 hours)**
Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near78 Field Cable to Cable Coupling, Power Mains and Power Supply coupling.

UNIT III - EMI MEASUREMENTS **(9 hours)**
EMI Shielded Chamber, Open Area Test Site, TEM Cell, GTEM cell Sensors/ Injectors/ Couplers, LISN, voltage probe, Current probeTest beds for ESD and EFT.

UNIT IV - EMI MITIGATION TECHNIQUES **(9 hours)**
Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting.

UNIT V - EMC SYSTEM DESIGN **(9 hours)**
PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models.

REFERENCES

1. W. Prasad Kodali, *"Engineering Electromagnetic Compatibility: Principles, Measurements and Technologies and Computer Models"*, Wiley, IEEE Press, 2nd Edition, 2001.
2. Henry W. Ott, *" Electromagnetic Compatibility Engineering"*, John Wiley and Sons, 2009.
3. Clayton. R. Paul, *"Introduction to Electromagnetic Compatibility"*, John Wiley and Sons, 2nd Edition, 2006.
4. Bernhard Keiser, *"Principles of Electromagnetic Compatibility"*, Artech house, 3rd Ed, 1998.

		L	T	P	C
CAC2001	**Career Advancement Course for Engineers -I**	**1**	**0**	**1**	**1**
	Total Contact Hours - 30				
	Prerequisite: Nil				
PURPOSE					
To enhance holistic development of students and improve their employability skills					
INSTRUCTIONAL OBJECTIVES					
1.	To improve aptitude, problem solving skills and reasoning ability of the student.				
2.	To collectively solve problems in teams and group.				
3.	Understand the importance of verbal and written communication in the workplace				
4.	Understand the significance of oral presentations, and when they may be used				
5.	Practice verbal communication by making a technical presentation to the class				
6.	Develop time management Skills				

UNIT I–BASIC NUMERACY: Types and Properties of Numbers, LCM, GCD, Fractions and decimals, Surds
UNIT II-ARITHMETIC – I: Percentages, Profit and Loss, Equations
UNIT III-REASONING – I: Logical Reasoning

UNIT IV-SOFT SKILLS – I: Presentation skills, E-mail Etiquette
UNIT V-SOFT SKILLS – II: Goal Setting and Prioritizing

ASSESSMENT

Soft Skills (Internal)

Assessment of presentation and writing skills.

Quantitative Aptitude (External)

- Objective Questions- 60 marks
- Descriptive case lets- 40 marks*
- Duration: 3 hours

***Engineering problems will be given as descriptive case lets.

REFERENCES

1. Quantitative Aptitude by Dinesh Khattar – Pearsons Publicaitons
2. Quantitative Aptitude and Reasoning by RV Praveen – EEE Publications
3. Quantitative Aptitude by Abijith Guha – TATA Mc GRAW Hill Publications
4. Soft Skills for Everyone by Jeff Butterfield – Cengage Learning India Private Limited
5. Six Thinking Hats is a book by Edward de Bono - Little Brown and Company
6. IBPS PO - CWE Success Master by Arihant - Arihant Publications(I) Pvt.Ltd - Meerut

<table>
<tr><td rowspan="4">CAC2002</td><td></td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>Career Advancement Course for Engineers -II</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td colspan="5">Total Contact Hours - 30</td></tr>
<tr><td colspan="5">Prerequisite: CAC2001</td></tr>
<tr><td colspan="6">PURPOSE</td></tr>
<tr><td colspan="6">To enhance holistic development of students and improve their employability skills</td></tr>
<tr><td colspan="6">INSTRUCTIONAL OBJECTIVES</td></tr>
<tr><td>1.</td><td colspan="5">To improve aptitude, problem solving skills and reasoning ability of the student</td></tr>
<tr><td>2.</td><td colspan="5">To collectively solve problems in teams and group</td></tr>
<tr><td>3.</td><td colspan="5">Understand the importance of verbal communication in the workplace</td></tr>
<tr><td>4.</td><td colspan="5">Understand the significance of oral presentations, and when they may be used</td></tr>
<tr><td>5.</td><td colspan="5">Understand the fundamentals of listening and how one can present in a group discussion</td></tr>
<tr><td>6.</td><td colspan="5">Prepare or update resume according to the tips presented in class</td></tr>
</table>

UNIT-I: ARITHMETIC – II: Ratios and Proportions, Mixtures and Solutions
UNIT-II: MODERN MATHEMATICS: Sets and Functions, Data Interpretation, Data Sufficiency
UNIT-III: REASONING – II: Analytical Reasoning
UNIT-IV: COMMUNICATION – I: Group discussion, Personal interview
UNIT-V: COMMUNICATION – II: Verbal Reasoning test papers

ASSESSMENT

1. **Communication (Internal)**
   - Individuals are put through formal GD and personal interviews.
   - Comprehensive assessment of individuals' performance in GD and PI will be carried out.

2. **Quantitative Aptitude (External)**
   Objective Questions- 60 marks (30 Verbal +30 Quants)
   Descriptive case lets- 40 marks*
   Duration: 3 hours
   *Engineering problems will be given as descriptive case lets.

REFERENCES

1. Quantitative Aptitude by Dinesh Khattar – Pearsons Publicaitons
2. Quantitative Aptitude and Reasoning by RV Praveen – EEE Publications
3. Quantitative Aptitude by Abijith Guha – TATA Mc GRAW Hill Publications
4. General English for Competitive Examination by A.P. Bharadwaj – Pearson Educaiton
5. English for Competitive Examination by Showick Thorpe - Pearson Educaiton
6. IBPS PO - CWE Success Master by Arihant - Arihant Publications(I) Pvt.Ltd - Meerut
7. Verbal Ability for CAT by Sujith Kumar - Pearson India
8. Verbal Ability and Reading Comprehension by Arun Sharma - Tata McGraw - Hill Education

		L	T	P	C
CAC2003	**Career Advancement Course For Engineers - III**	**1**	**0**	**1**	**1**
	Total Contact Hours - 30				
	Prerequisite: Nil				

PURPOSE	
To develop professional skills abreast with contemporary teaching learning methodologies	
INSTRUCTIONAL OBJECTIVES At the end of the course the student will be able to	
1.	acquire knowledge on planning, preparing and designing a learning program
2.	prepare effective learning resources for active practice sessions
3.	facilitate active learning with new methodologies and approaches
4.	create balanced assessment tools
5.	hone teaching skills for further enrichment

UNIT-I: DESIGN **(2 hrs)**
Planning and Preparing a learning program, Planning and Preparing a learning session

UNIT-II: PRACTICE **(2 hrs)**
Facilitating active learning , Engaging learners

UNIT-III: ASSESSMENT **(2 hrs)**
Assessing learner's progress**,** Assessing learner's achievement

UNIT-IV: HANDS ON TRAINING **(10 hrs)**
Group activities – designing learning session, Designing teaching learning resources, Designing

assessment tools, Mock teaching session

UNIT-V: TEACHING IN ACTION **(14 hrs)**
Live teaching sessions, Assessments

ASSESSMENT (Internal)

Weightage:

Design - 40%
Practice – 40%
Quiz – 10%
Assessment – 10%

REFERENCES

1. Cambridge International Diploma for Teachers and Trainers Text book by Ian Barker - Foundation books
2. Whitehead, Creating a Living Educational Theory from Questions of the kind: How do I improve my Practice? Cambridge J. of Education

#

VL2047	**SEMINAR**	**L**	**T**	**P**	**C**
		0	**0**	**1**	**1**

Every student will be required to present a seminar talk on a topic approved by the Department. The Committee constituted by the Head of the Department will evaluate the presentation and will award the marks based on

- Comprehensible arguments and organization.
- Accessible delivery
- Accessible visuals in support of arguments.
- Question and Answers.

VL2049	**PROJECT WORK – PHASE - I**	**L**	**T**	**P**	**C**
	Total Contact Hours - 12	**0**	**0**	**12**	**6**

Student has to identify the faculty supervisor (Guide), topic, objectives, deliverables and work plan. The topic should be of advanced standing requiring use of knowledge from program core and be preferably hardware oriented. Students are evaluated on monthly basis, by conducting reviews by the department throughout the project period. Student has to submit a report describing his/her project work. End semester examination/ Viva-voce will be conducted by the Department.

		L	T	P	C
VL2050	**PROJECT WORK – PHASE – II**	**L**	**T**	**P**	**C**
	Total Contact hours - 32	**0**	**0**	**32**	**16**

Student has to continue the project work he/she was doing in phase –I. The Student will be evaluated with monthly reviews and an end semester examination / viva-voce. The students are encouraged to submit his/her project work in Conference/Journal and due weightage will be given in their evaluation.