

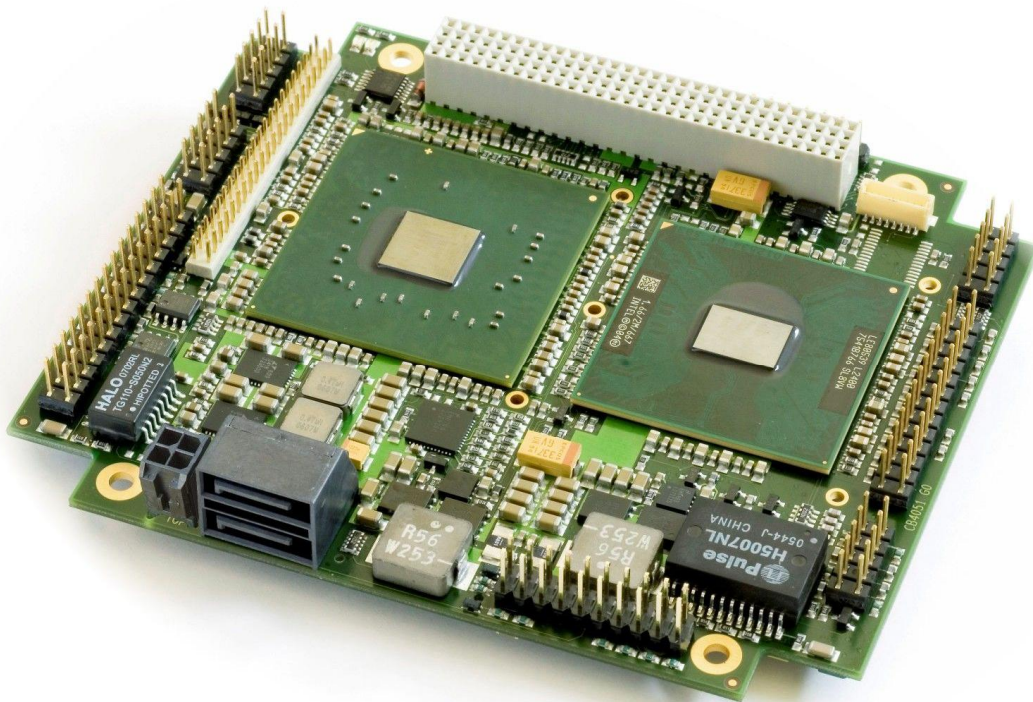
embedded-logic

DESIGN & MORE

PB945+

Manual

rev 0.2 (preliminary)



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0 History

Version	Changes
0.1	first preliminary release
0.2	adopted new name for form factor: "PCI-104" from www.pc104.org , updated block diagram

1 Introduction

1.1 Important Notes

Please read this manual carefully before you start with the installation of this hardware device. Also, make sure that you adhere to the following rules at any time:

- You must discharge your body from electric power before touching this board.
- Tools you use must be discharged from electric power as well.
- Please make sure that neither the board you want to install, nor the unit you want to install this board on, is energized before installation is completed.
- Please do not touch any devices or components on the board.

1.2 Technical Support

Technical support for this product can be obtained in the following ways:

- By describing the problem directly, using the support sheet on our homepage.
www.embedded-logic.de
- By downloading the support sheet from our homepage, filling it out and sending it in via email (support@embedded-logic.de) or fax (+49 8071 595857).

Please keep in mind that for the solution of the problem it is necessary to give us a detailed description as well as revision, BIOS version and serial number of the product.

1.3 Warranty

Embedded-logic GmbH issues a warranty of 24 months on the hardware. The warranty period starts on the issuing date of the invoice ex works. Pieces, which were damaged demonstrably as a result of manufacturing or material defects, will be substituted or repaired according to the estimation of embedded-logic GmbH. Thus an extension of the warranty period will not arise. Substitution-pieces will pass into embedded-logic GmbH properties. Any further claims against embedded-logic GmbH, especially claims for redhibitory actions, decrease in value or indemnification, are not constituted through this warranty. In such cases any material will be delivered free of charges. If the unit needs to be transported for repair, this will occur at sender's risk and expense.

Excluded from warranty services are:

- Damages resulting from the interference of people not authorised by embedded-logic GmbH.
- Units with destroyed or removed serial number.
- Damages which result from the non-observance of instructions, such as the connection of a wrong voltage or electric current, careless treatment or misemployment of defect or out-of-date batteries as well as mistakes in the reverse poling of cables.
- Wear parts, for example damaged connectors.
- Improper packing and improper additional packing.

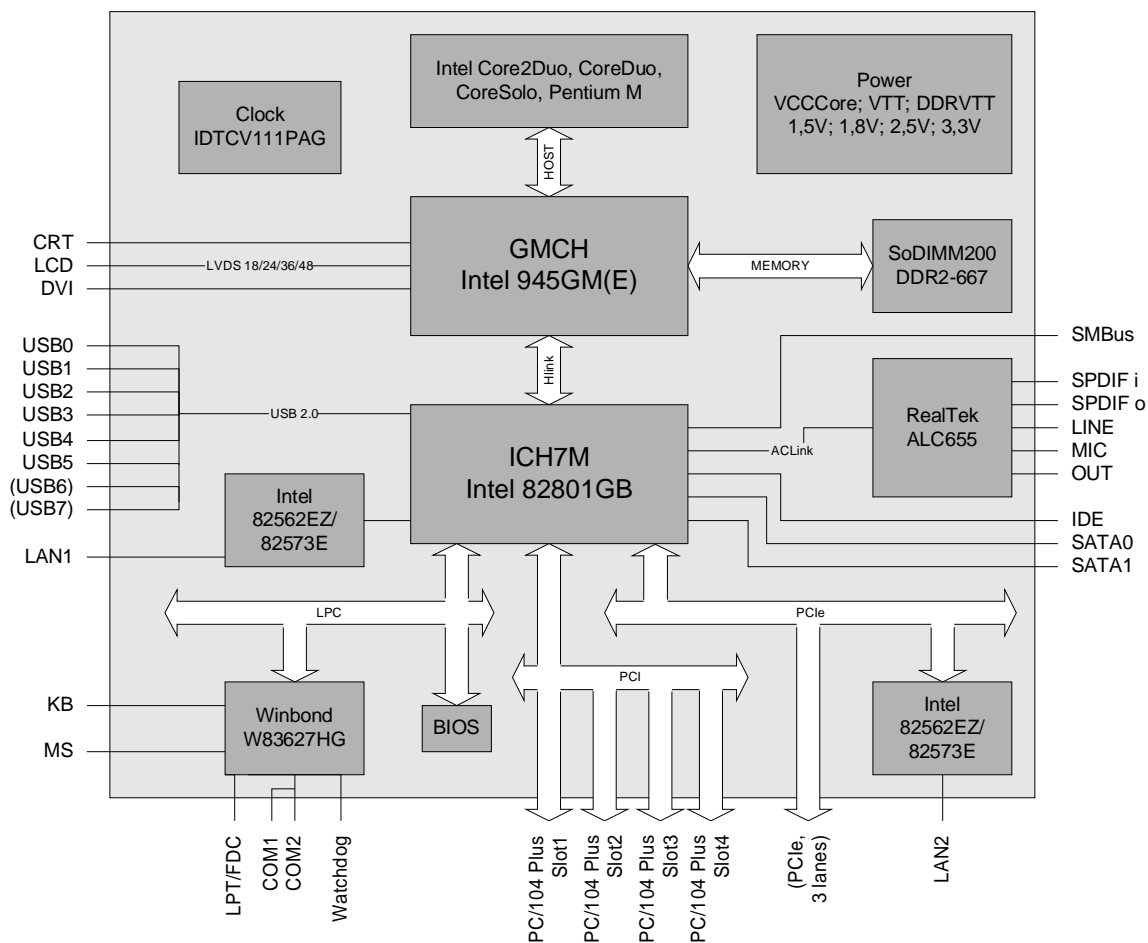
The warranty refers to the first buyer and it is not transferable.

Before the unit is sent back for repair, a RMA number must be requested at embedded-logic GmbH to register the process.

2 Overview

2.1 Features

The PB945+ is a highly complex PCI-104-board with the functionalities of a motherboard. Equipped with an Intel Celeron M, an Intel Core Duo, or an Intel Core 2 Duo processor, it can accommodate up to 2 GByte of DDR2-RAM (667 MHz) via SoDIMM200. It also provides a PCI bus (via PC/104-plus) and additional peripheral devices such as two serial interfaces, Gigabit-LAN, one IDE and two SATA interfaces, audio in and out, eight USB channels and CRT and TFT support. As an option a PCIe connector can be provided.



- o Processor Intel Celeron M, Intel CoreDuo/CoreSolo, Intel Core2Duo
- o Chipset Intel 945GM(E) and Intel ICH7
- o SoDIMM200-socket for one DDR2-667 module of up to 2GByte
- o Two serial interfaces COM1 and COM2
- o LAN-interface Ethernet 10/100 (Base-T)
- o LAN-interface Ethernet 10/100/1000 (Base-T)
- o IDE-interface
- o Two SATA-interfaces
- o PS2 keyboard / mouse interface
- o LPT interface
- o Eight USB 2.0 interfaces

- AWARD BIOS 6.10
- CRT connection
- TFT connection, LVDS 18/24/36/48 Bit
- AC97 compatible sound controller with SPDIF in and out
- RTC with external CMOS battery
- 5V single supply voltage
- PCI bus via PC/104+
- PCIe connector (option), 3 lanes
- Size: 96 mm x 90 (115,5) mm

Preliminary

2.2 Specifications und Documents

In making this manual and for further reading of technical documentation the following documents, specifications and web-pages were used and are recommended:

- PC/104 specification
Version 2.5
www.pc104.org
- PC/104-Plus specification
Version 2.0
www.pc104.org
- PCI specification
Version 2.3 resp. 3.0
www.pcisig.com
- PCI-Express specification
Version 1.1
www.pcisig.com
- ACPI specification
Version 3.0
www.acpi.info
- ATA/ATAPI specification
Version 7 Rev. 1
www.t13.org
- USB specifications
www.usb.org
- SM-Bus specification
Version 2.0
www.smbus.org
- Intel chip set description
Mobile Intel 945 Express Chipset Family Datasheet
www.intel.com
- Intel chip descriptions
Celeron M, Core Duo/Solo, Core2 Duo
www.intel.com
- Winbond chip description
W83627HG Datasheet
www.winbond-usa.com or www.winbond.com.tw
- Intel chip description
82562GZ Datasheet
www.intel.com
- Intel chip description
82573E Datasheet
www.intel.com
- IDT chip description
IDTCV111i Datasheet
www.idt.com

2.3 Trade Marks

All trade marks belong to their respective owners and are accepted.

Preliminary

3 Detailed Description

3.1 Power Supply

The power supply of the hardware module is effected via the power connector. The board only requires an operating voltage of 5 volt \pm 5%.

3.2 CPU

The board can be ordered with one of the following processors employed: Intel Celeron M, Intel Core Duo, and Intel Core 2 Duo. The package type allows a maximum die temperature of 100 degrees Celsius and accords highest possible security even in rough environment.

The processor includes a second level cache of up to 4 MByte, depending on which model is used. Furthermore the processors offer many features known from the desktop range such as MMX2, serial number, loadable microcode etc.

3.3 Memory

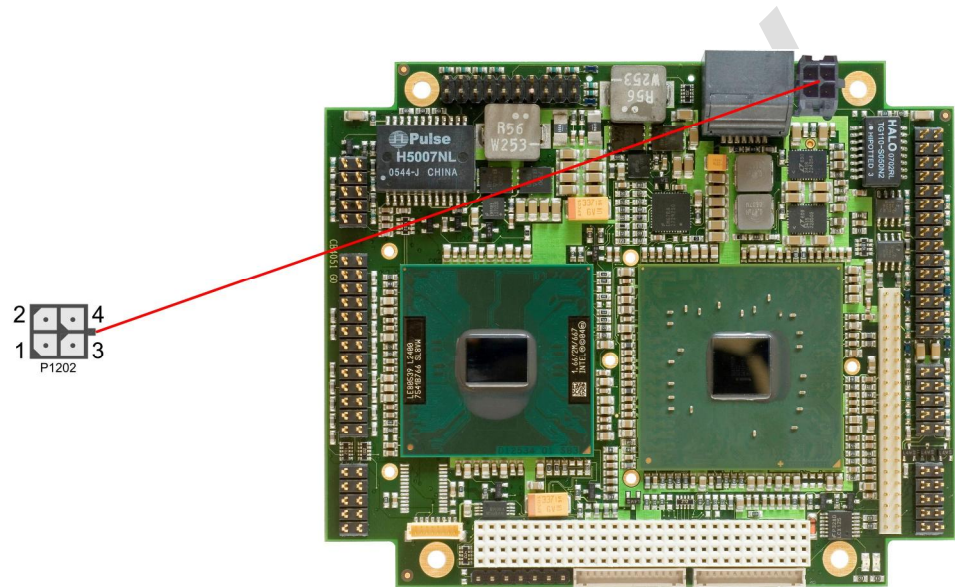
There is one conventional SoDIMM200 socket available to equip the board with memory. For mechanical reasons it is possible that particular memory modules cannot be employed. Please ask your distributor for recommended memory modules.

With currently available SoDIMM modules a memory extension up to 2 GByte is possible (DDR2-667).

4 Connectors

4.1 Power Supply

The connector for the power supply is a standard IDC socket connector with a spacing of 2.54 mm. The board only requires an operating voltage of 5 volt \pm 5%, it is not necessary to connect all indicated voltages. Additional voltages may only be necessary for PC/104-Plus expansion cards. For safety reasons it is recommended to connect all power pins of the PC/104-Plus connector to the power supply as well.

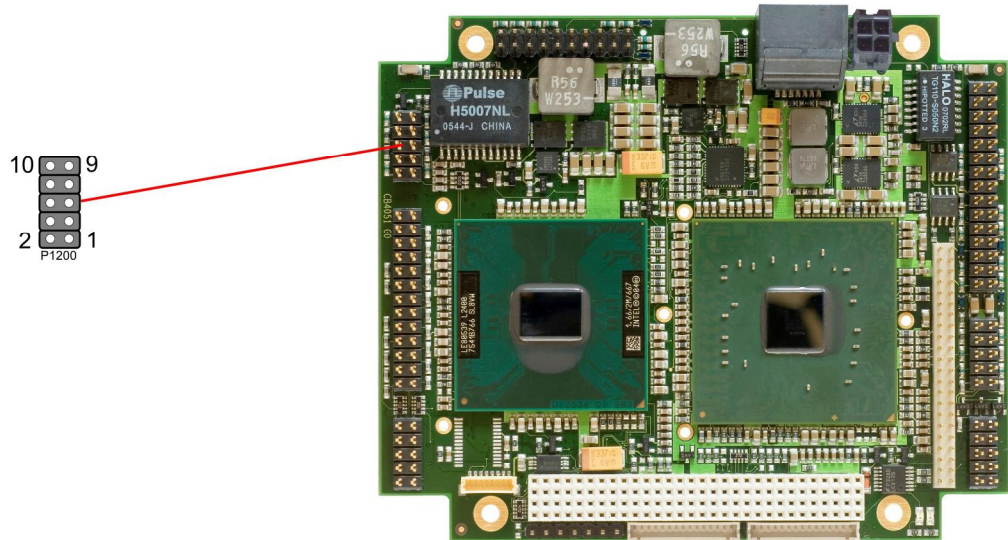


Description	Name	Pin	Name	Description	
5 volt supply	VCC	1	2	VCC	5 volt supply
ground	GND	3	4	GND	ground

4.2 System

The system connector, which has the main functions that are necessary to start the board, is provided via a standard IDC socket connector with a spacing of 2.54 mm.

This connector supports the following interfaces: PS/2 keyboard, PS/2 mouse, speaker, external RTC-battery, hard disk LED and reset of the board.

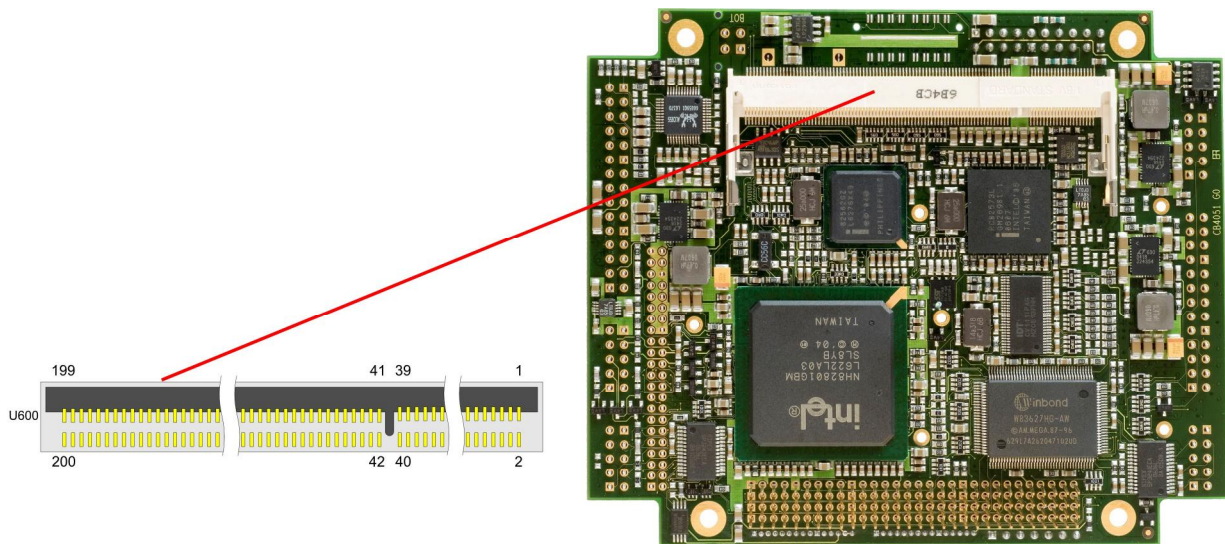


Description	Name	Pin	Pin	Name	Description
speaker to 5 volt	SPEAKER	1	2	GND	ground
reset to ground	RESET#	3	4	KLOCK#	keyboard lock
keyboard Data	KDAT	5	6	KCLK	keyboard clock
mouse data	MDAT	7	8	MCLK	mouse clock
CMOS battery ≥ 3 volt	VBAT	9	10	VCC	5 volt supply

4.3 Memory

There is one conventional SoDIMM200 socket available to equip the board with memory (DDR2-667). It is located on the bottom side of the board. For mechanical reasons it is possible that particular memory modules cannot be employed. Please ask your distributor for recommended memory modules.

With currently available SoDIMM modules a memory extension up to 2 GByte is possible. The timing parameters for different memory modules are automatically set by BIOS.



Description	Name	Pin	Name	Description
memory reference current	REF	1	2	GND
ground	GND	3	4	DQ4
data 0	DQ0	5	6	DQ5
data 1	DQ1	7	8	GND
ground	GND	9	10	DQM0
data strobe 0 -	DQS0#	11	12	GND
data strobe 0 +	DQS0	13	14	DQ6
ground	GND	15	16	DQ7
data 2	DQ2	17	18	GND
data 3	DQ3	19	20	DQ12
ground	GND	21	22	DQ13
data 8	DQ8	23	24	GND
data 9	DQ9	25	26	DQM1
ground	GND	27	28	GND
data strobe 1 -	DQS1#	29	30	CK0
data strobe 1 +	DQS1	31	32	CK0#
ground	GND	33	34	GND
data 10	DQ10	35	36	DQ14
data 11	DQ11	37	38	DQ15
ground	GND	39	40	GND
ground	GND	41	42	GND
data 16	DQ16	43	44	DQ20
data 17	DQ17	45	46	DQ21
ground	GND	47	48	GND
data strobe 2 -	DQS2#	49	50	N/C

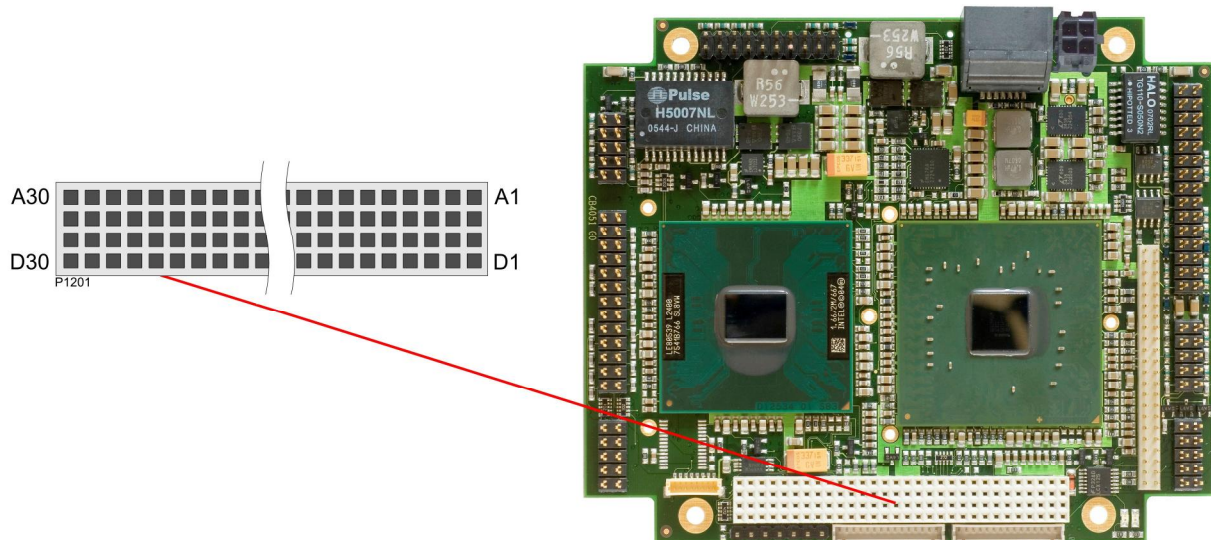
Description	Name	Pin		Name	Description
data strobe 2 +	DQS2	51	52	DQM2	data mask 2
ground	GND	53	54	GND	ground
data 18	DQ18	55	56	DQ22	data 22
data 19	DQ19	57	58	DQ23	data 23
ground	GND	59	60	GND	ground
data 24	DQ24	61	62	DQ28	data 28
data 25	DQ25	63	64	DQ29	data 29
ground	GND	65	66	GND	ground
data mask 3	DQM3	67	68	DQS3#	data strobe 3 -
reserved	N/C	69	70	DQS3	data strobe 3 +
ground	GND	71	72	GND	ground
data 26	DQ26	73	74	DQ30	data 30
data 27	DQ27	75	76	DQ31	data 31
ground	GND	77	78	GND	ground
clock enables 0	CKE0	79	80	CKE1	clock enables 1
1.8 volt supply	1.8V	81	82	1.8V	1.8 volt supply
reserved	N/C	83	84	N/C	reserved
SDRAM bank 2	BA2	85	86	N/C	reserved
1.8 volt supply	1.8V	87	88	1.8V	1.8 volt supply
address 12	A12	89	90	A11	address 11
address 9	A9	91	92	A7	address 7
address 8	A8	93	94	A6	address 6
1.8 volt supply	1.8V	95	96	1.8V	1.8 volt supply
address 5	A5	97	98	A4	address 4
address 3	A3	99	100	A12	address 2
address 1	A1	101	102	A0	address 0
1.8 volt supply	1.8V	103	104	1.8V	1.8 volt supply
address 10	A10	105	106	BA1	SDRAM bank 1
SDRAM bank 0	BA0	107	108	RAS#	row address strobe
write enable	WE#	109	110	S0#	chip select 0
1.8 volt supply	1.8V	111	112	1.8V	1.8 volt supply
column address strobe	CAS#	113	114	ODT0	on die termination 0
chip select 1	S1#	115	116	A13	address 13
1.8 volt supply	1.8V	117	118	1.8V	1.8 volt supply
on die termination 1	ODT1	119	120	N/C	reserved
ground	GND	121	122	GND	ground
data 32	DQ32	123	124	DQ36	data 36
data 33	DQ33	125	126	DQ37	data 37
ground	GND	127	128	GND	ground
data strobe 4 -	DQS4#	129	130	DQM4	data mask 4
data strobe 4 +	DQS4	131	132	GND	ground
ground	GND	133	134	DQ38	data 38
data 34	DQ34	135	136	DQ39	data 39
data 35	DQ35	137	138	GND	ground
ground	GND	139	140	DQ44	data 44
data 40	DQ40	141	142	DQ45	data 45
data 41	DQ41	143	144	GND	ground
ground	GND	145	146	DQS5#	data strobe 5 -
data mask 5	DQM5	147	148	DQS5	data strobe 5 +
ground	GND	149	150	GND	ground
data 42	DQ42	151	152	DQ46	data 46
data 43	DQ43	153	154	DQ47	data 47
ground	GND	155	156	GND	ground
data 48	DQ48	157	158	DQ52	data 52

Description	Name	Pin		Name	Description
data 49	DQ49	159	160	DQ53	data 53
ground	GND	161	162	GND	ground
Test	TEST	163	164	CK1	clock 1 +
ground	GND	165	166	CK1#	clock 1 -
data strobe 6 -	DQS6#	167	168	GND	ground
data strobe 6	DQS6	169	170	DQM6	data mask 6
ground	GND	171	172	GND	ground
data 50	DQ50	173	174	DQ54	data 54
data 51	DQ51	175	176	DQ55	data 55
ground	GND	177	178	GND	ground
data 56	DQ56	179	180	DQ60	data 60
data 57	DQ57	181	182	DQ61	data 61
ground	GND	183	184	GND	ground
data mask 7	DQM7	185	186	DQS7#	data strobe 7 #
ground	GND	187	188	DQS7	data strobe 7 +
data 58	DQ58	189	190	GND	ground
data 59	DQ59	191	192	DQ62	data 62
ground	GND	193	194	DQ63	data 63
SMBus data	SDA	195	196	GND	ground
SMBus clock	SCL	197	198	SA0	SPD address
3.3 volt	3.3V	199	200	SA1	SPD address

4.4 PC/104-Plus Bus

Expansion cards can be connected to the board using the PC/104-Plus connector. A maximum of four PC/104-Plus cards are supported.

The interrupt routing and the IDSEL signals for the expansion cards are specified in the PC/104-Plus specification.

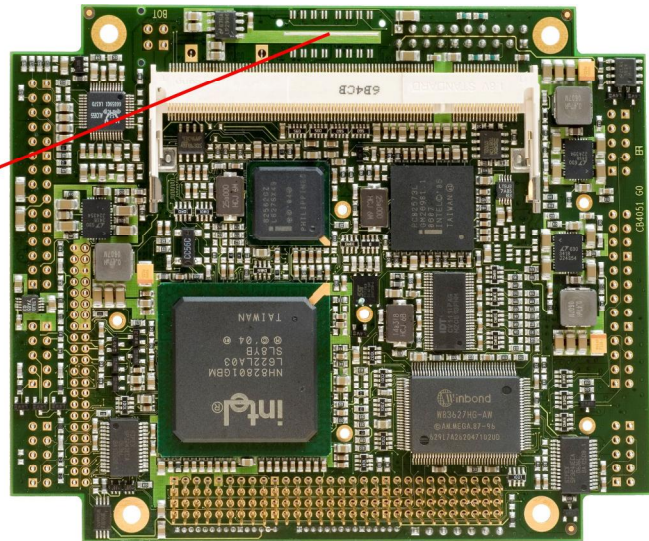


Description	Name	Pin	Name	Description
ground	GND	A1 B1	N/C	reserved
5 volt - IO buffer power	VCCIO	A2 B2	AD2	PCI - address/data 2
PCI - address/data 5	AD5	A3 B3	GND	ground
PCI - com/byte enable 0	CBE0#	A4 B4	AD7	PCI - address/data 7
ground	GND	A5 B5	AD9	PCI - address/data 9
PCI - address/data 11	AD11	A6 B6	VCCIO	5 volt - IO buffer power
PCI - address/data 14	AD14	A7 B7	AD13	PCI - address/data 13
3.3 volt supply	3.3V	A8 B8	CBE1#	PCI - com/byte enable 1
PCI - system error	SERR#	A9 B9	GND	ground
ground	GND	A10 B10	PERR#	PCI - parity error
PCI - stop	stop#	A11 B11	3.3V	3.3 volt supply
3.3 volt supply	3.3V	A12 B12	TRDY#	PCI - target ready
PCI - frame	FRAME#	A13 B13	GND	ground
ground	GND	A14 B14	AD16	PCI - address/data 16
PCI - address/data 18	AD18	A15 B15	3.3V	3.3 volt supply
PCI - address/data 21	AD21	A16 B16	AD20	PCI - address/data 20
3.3 volt supply	3.3V	A17 B17	AD23	PCI - address/data 23
PCI - ID select slot 1	IDSEL0	A18 B18	GND	ground
PCI - address/data 24	AD24	A19 B19	CBE3#	PCI - com/byte enable 3
ground	GND	A20 B20	AD26	PCI - address/data 26
PCI - address/data 29	AD29	A21 B21	VCC	5 volt supply
5 volt supply	VCC	A22 B22	AD30	PCI - address/data 30
PCI - bus request slot 1	REQ0#	A23 B23	GND	ground
ground	GND	A24 B24	REQ2#	PCI - bus request slot 3
PCI - bus grant slot 4	GNT1#	A25 B25	VCCIO	5 volt - IO buffer power
5 volt supply	VCC	A26 B26	CLK0	PCI - clock slot 1

Description	Name	Pin		Name	Description
PCI – clock slot 3	CLK2	A27	B27	VCC	5 volt supply
ground	GND	A28	B28	INTD#	PCI – interrupt D
12V supply	12V	A29	B29	INTA#	PCI – interrupt A
-12V supply	-12V	A30	B30	REQ3#	PCI – bus request slot 4
5 volt supply	VCC	C1	D1	AD0	PCI – address/data 0
PCI – address/data 1	AD1	C2	D2	VCC	5 volt supply
PCI – address/data 4	AD4	C3	D3	AD3	PCI – address/data 3
ground	GND	C4	D4	AD6	PCI – address/data 6
PCI – address/data 8	AD8	C5	D5	GND	ground
PCI – address/data 10	AD10	C6	D6	M66EN	PCI – 66MHz enable
ground	GND	C7	D7	AD12	PCI – address/data 12
PCI – address/data 15	AD15	C8	D8	3.3V	3.3 volt supply
reserved	N/C	C9	D9	PAR	PCI – parity bit
3.3 volt supply	3.3V	C10	D10	N/C	reserved
PCI – lock	LOCK#	C11	D11	GND	ground
ground	GND	C12	D12	DEVSEL#	PCI – device select
PCI – initiator ready	IRDY#	C13	D13	3.3V	3.3 volt supply
3.3 volt supply	3.3V	C14	D14	CBE2#	PCI – com/byte enable 2
PCI – address/data 17	AD17	C15	D15	GND	ground
ground	GND	C16	D16	AD19	PCI – address/data 19
PCI – address/data 22	AD22	C17	D17	3.3V	3.3 volt supply
PCI – ID select slot 2	IDSEL1	C18	D18	IDSEL2	PCI – ID select slot 3
5 volt - IO buffer power	VCCIO	C19	D19	IDSEL3	PCI – ID select slot 4
PCI – address/data 25	AD25	C20	D20	GND	ground
PCI – address/data 28	AD28	C21	D21	AD27	PCI – address/data 27
ground	GND	C22	D22	AD31	PCI – address/data 31
PCI – bus request slot 2	REQ1#	C23	D23	VCCIO	5 volt - IO buffer power
5 volt supply	VCC	C24	D24	GNT0#	PCI – bus grant slot 1
PCI – bus grant slot 3	GNT2#	C25	D25	GND	ground
ground	GND	C26	D26	CLK1	PCI – clock slot 2
PCI – clock slot 4	CLK3	C27	D27	GND	ground
5 volt supply	VCC	C28	D28	RST#	PCI – reset
PCI – interrupt B	INTB#	C29	D29	INTC#	PCI – interrupt C
PCI – bus grant slot 4	GNT3#	C30	D30	GND	ground

4.5 PCIe Interface

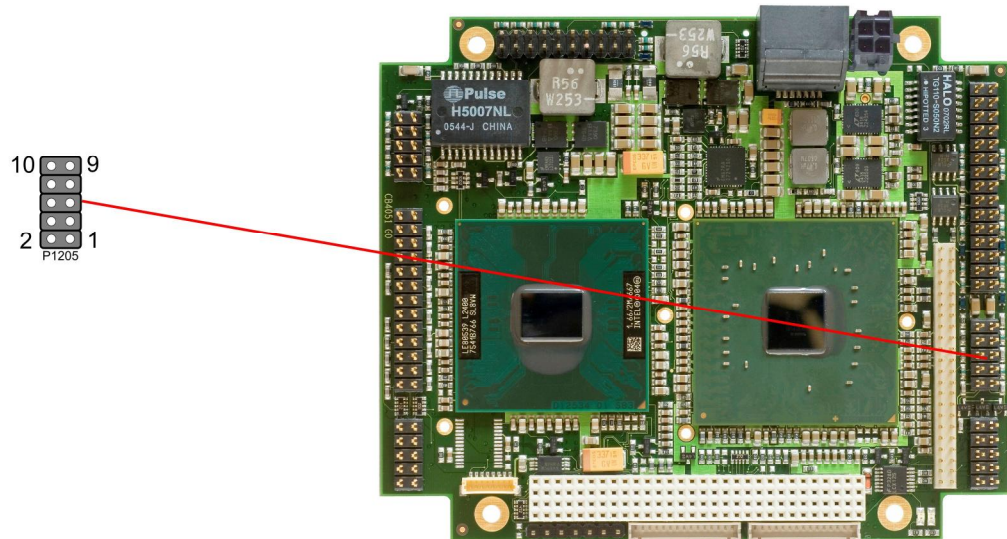
As an option, the PB945+ board can be equipped with a 32 pin PCIe connector (Samtec QMS...). USB channels 7 and 8 are also provided through this connector.



Description	Name	Pin	Name	Description	
PCIe slot 0 clock +	PECLK0	1	17	SMCLK	SMBus clock
PCIe slot 0 clock -	PECLK0#	2	18	SMDAT	SMBus data
PCIe 0 receive data +	PER0	3	19	PET0	PCIe 0 transmit data +
PCIe 0 receive data -	PER0#	4	20	PET0#	PCIe 0 transmit data -
PCIe slot 1 clock +	PECLK1	5	21	WAKE#	PCIe wake
PCIe slot 1 clock -	PECLK1#	6	22	PERST#	PCIe reset
PCIe 1 receive data +	PER1	7	23	PET1	PCIe 1 transmit data +
PCIe 1 receive data -	PER1#	8	24	PET1#	PCIe 1 transmit data -
PCIe slot 2 clock +	PECLK2	9	25	PE0CEN#	PCIe 0 clock enable
PCIe slot 2 clock -	PECLK2#	10	26	PE1CEN#	PCIe 1 clock enable
PCIe 2 receive data +	PER2	11	27	PET2	PCIe 2 transmit data +
PCIe 2 receive data -	PER2#	12	28	PET2#	PCIe 2 transmit data -
USB overcurrent 6	OC6#	13	29	PE2CEN#	PCIe 2 clock enable
USB overcurrent 7	OC7#	14	30	SMALERT#	SMBus alert
USB + channel 7	USB6	15	31	USB7	USB + channel 8
USB - channel 7	USB6#	16	32	USB7#	USB - channel 8

4.6 VGA

The CRT-VGA signals are provided by a standard IDC socket connector with a spacing of 2.54 mm. This interface allows the connection of a standard VGA-monitor.



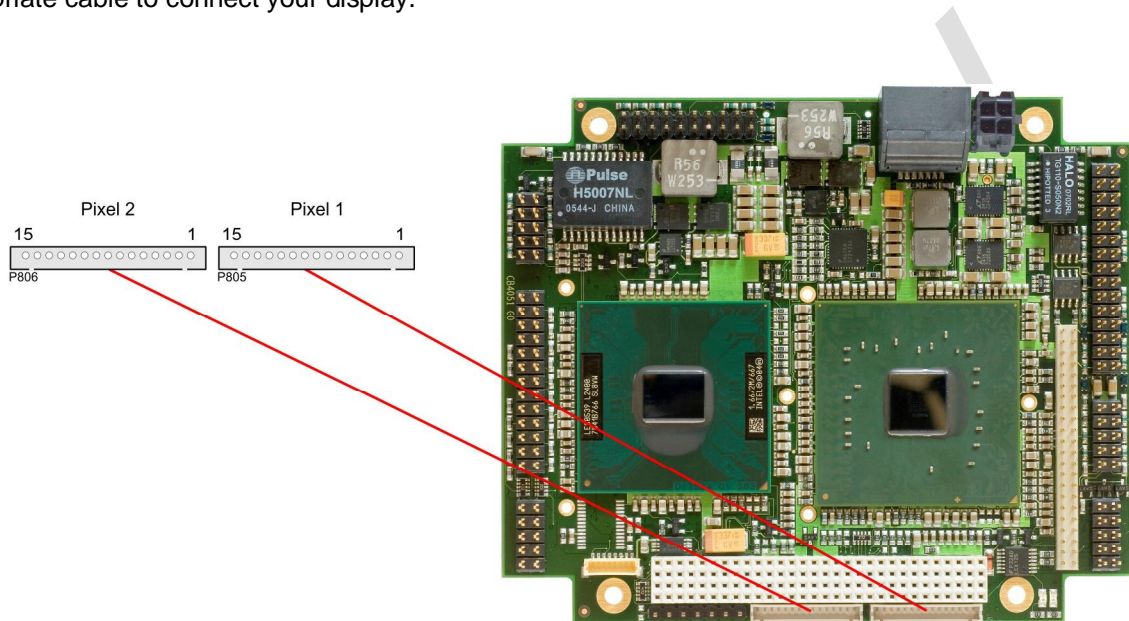
Description	Name	Pin	Name	Description	
analog red	RED	1	2	GND	ground
analog green	GREEN	3	4	DDDA	DD data
analog blue	BLUE	5	6	DDCK	DD clock
vertikal sync	VSYNC	7	8	GND	ground
horizontal sync	HSYNC	9	10	GND	ground

4.7 LCD

The LCD is connected via two 15 pin connectors (Hirose DF13-15P-DAS, mating connector: DF13-15S-xxx). The power supply for the display is also provided through these connectors. The PB945+ board only supports displays with LVDS interface. For displays with digital interface an extra receiver board is available. There is no support for DSTN displays.

With the LVDS interface it is possible to trigger LVDS displays with a maximum of 24Bit colour depth and one or two pixels per clock. For single pixel displays only one connector is necessary.

The display type can be chosen over the BIOS setup. Please contact your sales representative regarding an appropriate cable to connect your display.



The following table shows the pin description for the first bit ("even" pixel).

Pin	Name	Description
1	GND	ground
2	GND	ground
3	TXO00#	LVDS even data 0 -
4	TXO00	LVDS even data 0 +
5	TXO01#	LVDS even data 1 -
6	TXO01	LVDS even data 1 +
7	TXO02#	LVDS even data 2 -
8	TXO02	LVDS even data 2 +
9	TXO0C#	LVDS even clock -
10	TXO0C	LVDS even clock +
11	TXO03#	LVDS even data 3 -
12	TXO03	LVDS even data 3 +
13	BL_VCC	switched 5 volt for backlight
14	FP_3.3V	switched 3.3 volt for display
15	FP_3.3V	switched 3.3 volt for display

The following table shows the pin description for the second bit ("odd" pixel). This connector will only be used if a display with two pixels per clockcycle is to be connected.

Pin	Name	Description
1	GND	ground

Pin	Name	Description
2	GND	ground
3	TXO10#	LVDS odd data 0 -
4	TXO10	LVDS odd data 0 +
5	TXO11#	LVDS odd data 1 -
6	TXO11	LVDS odd data 1 +
7	TXO12#	LVDS odd data 2 -
8	TXO12	LVDS odd data 2 +
9	TXO1C#	LVDS odd clock -
10	TXO1C	LVDS odd clock +
11	TXO13#	LVDS odd data 3 -
12	TXO13	LVDS odd data 3 +
13	LCD-CLK	I2C-Bus clock für LCD
14	LCD-DAT	I2C-Bus data für LCD
15	VCC	5 volt supply

4.8 USB 1 to 4, LAN, Sound

USB 1-4, LAN and sound are provided via a standard IDC socket connector with a spacing of 2.54 mm. Necessary settings can be accomplished in BIOS setup.

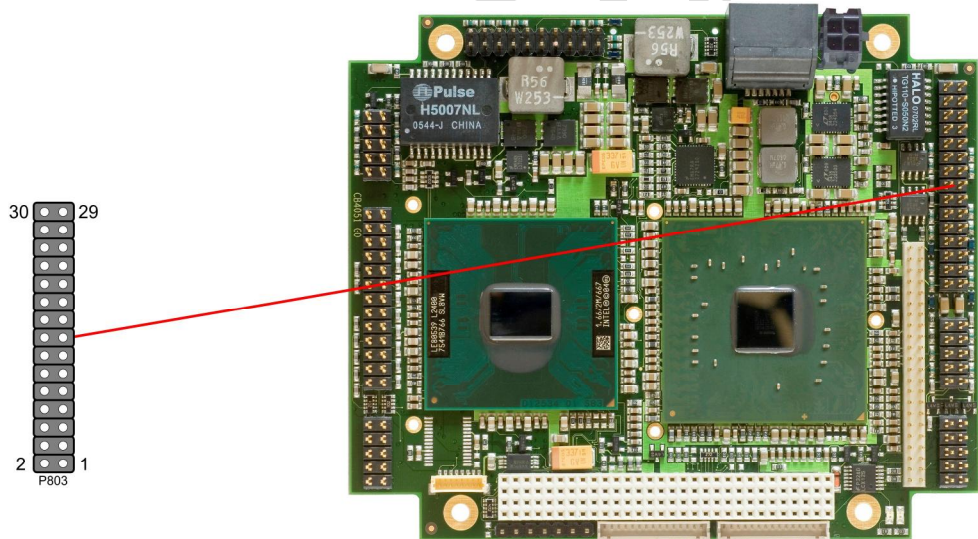
All USB-channels support USB 2.0. You may note that the setting of USB keyboard or USB mouse support in the BIOS-setup is only necessary and advisable, if the OS offers no USB-support. BIOS-setup can be changed with an USB keyboard without enabling USB keyboard support. Running Windows with these features enabled may lead to significant performance or functionality limitations.

Every USB interface provides up to 500 mA current and is protected by an electrical fuse.

The LAN-interface on this connector supports 10BaseT and 100BaseT compatible net components with automatic bandwidth selection. Additional signals are provided for status LEDs. Auto-negate and auto-cross functionality is available, PXE and RPL are available on request.

Additionally on this plug one can also find signals for audio input and output. There are two ways to use these signals. Default functionality is the familiar audio in, audio out, and microphone. OS dependent device drivers can switch these signals to support an 5.1 output; thus in this mode no audio input signals are available.

Signals "SPDIFI" and "SPDIFO" provide digital input and output. If a transformation to a coaxial or optical connector is necessary this must be performed externally.

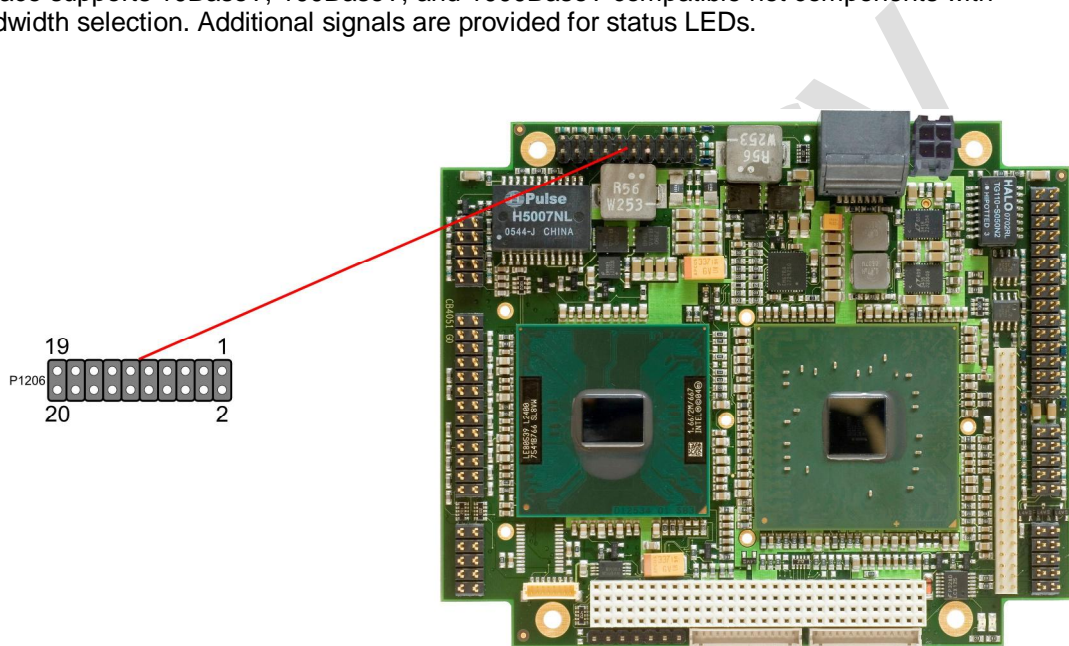


Description	Name	Pin	Name	Description
5 volt for USB1	USB1 VCC	1	2	USB2 VCC
USB- channel 1	USB1#	3	4	USB2#
USB+ channel 1	USB1	5	6	USB2
ground	GND	7	8	GND
USB+ channel 3	USB3	9	10	USB4
USB- channel 3	USB3#	11	12	USB4#
5 volt for USB3	USB3 VCC	13	14	USB4 VCC
LAN activity	ACTLED	15	16	SPEEDLED
LAN RX+	LANRX	17	18	LANTX
LAN RX-	LANRX#	19	20	LANTX#
digital output SPDIF	SPDIFO	21	22	3.3V
digital input SPDIF	SPDIFI	23	24	S_AGND
sound output right / frond output right	LOUT_R / FRONT_R	25	26	LOUT_L / FRONT_L
				sound output left / frond output left

Description	Name	Pin		Name	Description
AUX input right / rear output right	AUXA_R / REAR_R	27	28	AUXA_L / REAR_L	AUX input left / rear output left
microphone input 1 / center output	MIC1 / CENTER	29	30	MIC2 / LFE	microphone input 2 / LFE output

4.9 USB 5 and 6, LAN2

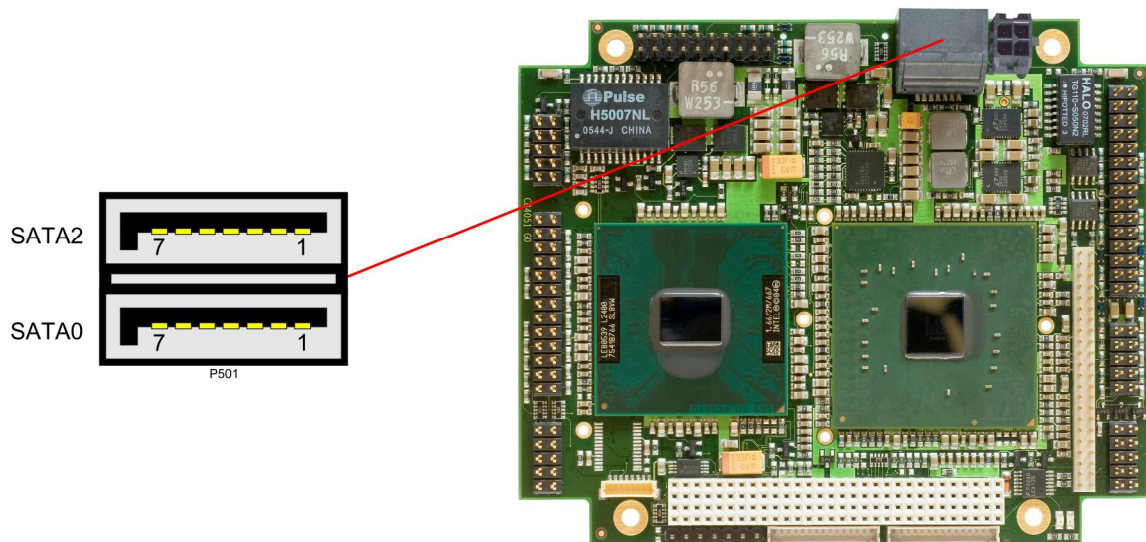
USB channels 5 and 6 are combined with LAN2 into one standard IDC socket connector with a spacing of 2.54 mm. All required settings can be accomplished in BIOS setup. The USB channels support USB 2.0. You may note that the setting of USB keyboard or USB mouse support in the BIOS-setup is only necessary and advisable, if the OS offers no USB-support. BIOS-setup can be changed with an USB keyboard without enabling USB keyboard support. Running Windows with these features enabled may lead to significant performance or functionality limitations. Every USB interface provides up to 500 mA current and is protected by an electrical fuse. The LAN-interface supports 10BaseT, 100BaseT, and 1000BaseT compatible net components with automatic bandwidth selection. Additional signals are provided for status LEDs.



Description	Name	Pin	Name	Description
5V for USB5	USB5 VCC	1	2	USB6 VCC
USB- channel 5	USB4#	3	4	USB5#
USB+ channel 5	USB4	5	6	USB5
ground	GND	7	8	GND
LAN active LED	ACTLED2	9	10	LILED2
LAN 1 +	LAN1	11	12	LAN0
LAN 1 -	LAN1#	13	14	LAN0#
LAN 3 +	LAN3	15	16	LAN2
LAN 3 -	LAN3#	17	18	LAN2#
link 100 LED	SPEED100	19	20	3.3V
				3.3 volt supply

4.10 SATA Interfaces

The PB945+ provides two SATA interfaces allowing transfer rates of up to 3 GBit per second. These interfaces are made available via two 7 pin connectors. The required settings are made in the BIOS setup.

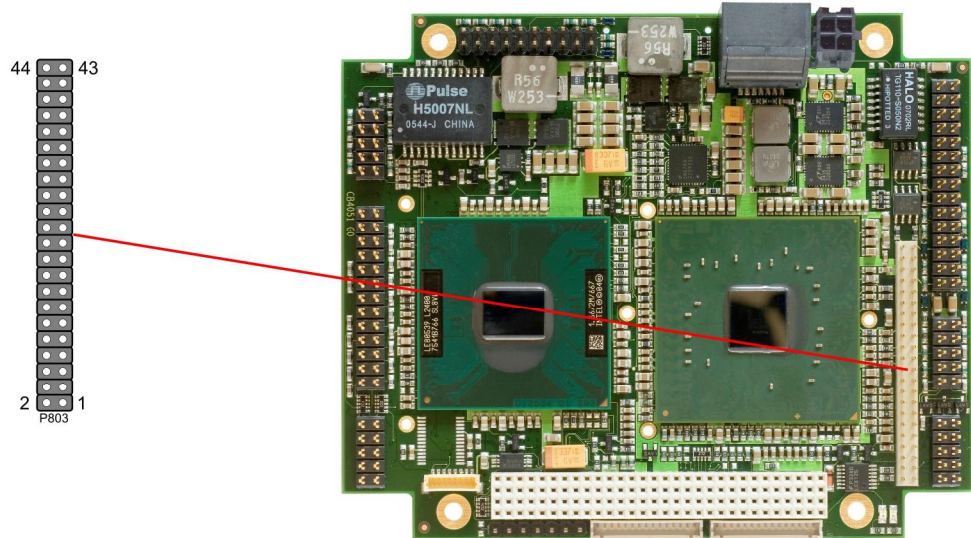


Pin	Name	Description
1	GND	ground
2	SATA1TX	SATA1 transmit +
3	SATA1TX#	SATA1 transmit -
4	GND	ground
5	SATA1RX	SATA1 receive +
6	SATA1RX#	SATA1 receive -
7	GND	ground

Pin	Name	Description
1	GND	ground
2	SATA2TX	SATA2 transmit +
3	SATA2TX#	SATA2 transmit -
4	GND	ground
5	SATA2RX	SATA2 receive +
6	SATA2RX#	SATA2 receive -
7	GND	ground

4.11 IDE Interface

The primary IDE interface is a standard IDC socket connector with a spacing of 2 mm. All commercial IDE devices are supported but an adapter to connect may be necessary. The required settings are made in the BIOS setup.

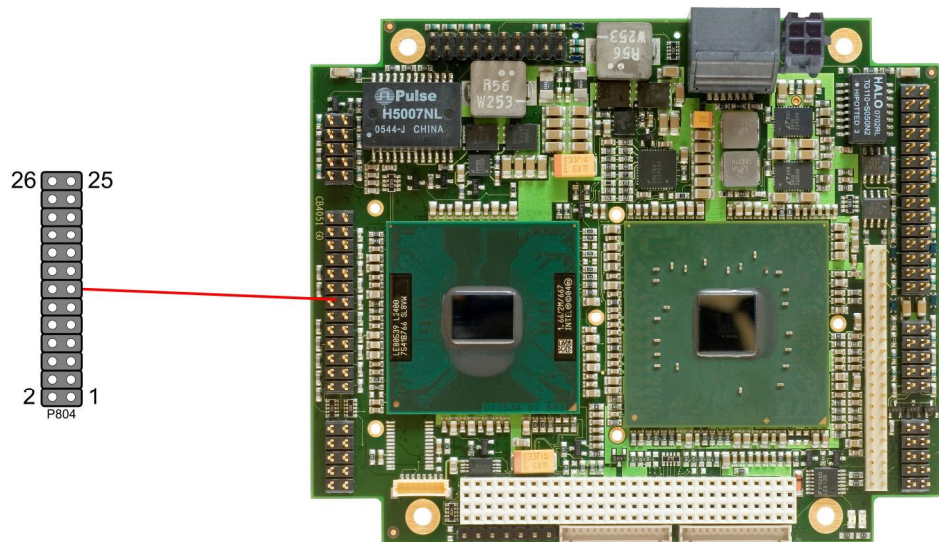


Pinout for primary IDE

Description	Name	Pin	Pin	Name	Description
reset	PRST#	1	2	GND	ground
data bit 7	PDD7	3	4	PDD8	data bit 8
data bit 6	PDD6	5	6	PDD9	data bit 9
data bit 5	PDD5	7	8	PDD10	data bit 10
data bit 4	PDD4	9	10	PDD11	data bit 11
data bit 3	PDD3	11	12	PDD12	data bit 12
data bit 2	PDD2	13	14	PDD13	data bit 13
data bit 1	PDD1	15	16	PDD14	data bit 14
data bit 0	PDD0	17	18	PDD15	data bit 15
ground	GND	19	20	N/C	reserved
DMA request signal	PDDREQ	21	22	GND	ground
write signal	PDIOW#	23	24	GND	ground
read signal	PDIOR#	25	26	GND	ground
ready signal	PDRDY	27	28	N/C	reserved
DMA acknowledge signal	PDDACK#	29	30	GND	ground
interrupt signal	PDIRQ	31	32	N/C	reserved
address bit 1	PDA1	33	34	PDMA66EN	enable UDMA66
address bit 2	PDA0	35	36	PDA2	address bit 2
chip select signal 0	PDSC0#	37	38	PDCS1#	chip select signal 1
reserved	N/C	39	40	GND	ground
supply HDD 5V	VCC	41	42	VCC	supply HDD 5V
ground	GND	43	44	N/C	reserved

4.12 Parallel Interface LPT

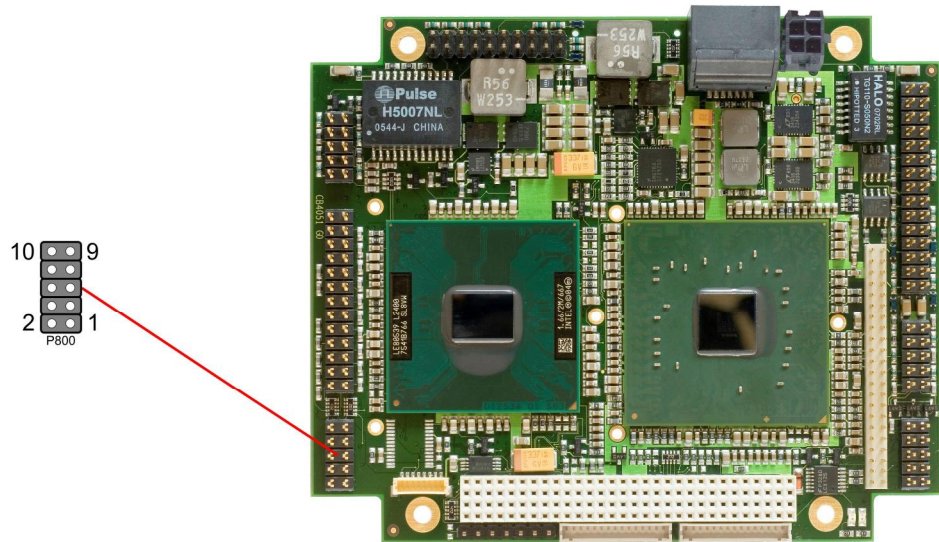
The parallel interface is a standard IDC socket connector with a spacing of 2.54 mm. The port address and the interrupt are set via the BIOS setup. Floppy drives can be connected to this interface as well. For that purpose this function is enabled via BIOS setup. A floppy drive is connected with a special cable. Please contact your sales representative for such a cable.



Description	Name	Pin	Name	Description	
strobe	STB#	1	2	AFD#	automatic line feed
LPT data 0	PD0	3	4	ERR#	error
LPT data 1	PD1	5	6	INIT#	init
LPT data 2	PD2	7	8	SLIN#	select input
LPT data 3	PD3	9	10	GND	ground
LPT data 4	PD4	11	12	GND	ground
LPT data 5	PD5	13	14	GND	ground
LPT data 6	PD6	15	16	GND	ground
LPT data 7	PD7	17	18	GND	ground
acknowledge	ACK#	19	20	GND	ground
busy	BUSY	21	22	GND	ground
paper end	PE	23	24	GND	ground
select printer	SLCT	25	26	VCC	5 volt supply

4.13 Serial Interface COM1

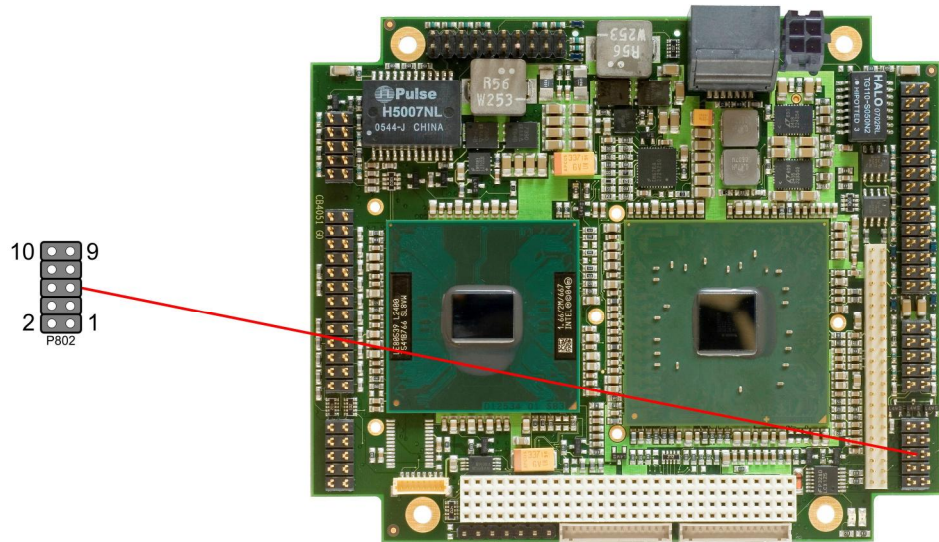
The serial interface is a standard IDC socket connector with a spacing of 2.54 mm. According to the product order, TTL level signals or RS232 standard signals are provided. The port address and the interrupt are set via the BIOS setup.



Description	Name	Pin	Name	Description	
data carrier detect	DCD	1	2	DSR	data set ready
receive data	RXD	3	4	RTS	request to send
transmit data	TXD	5	6	CTS	clear to send
data terminal ready	DTR	7	8	RI	ring indicator
ground	GND	9	10	VCC	5 volt supply

4.14 Serial Interface COM2

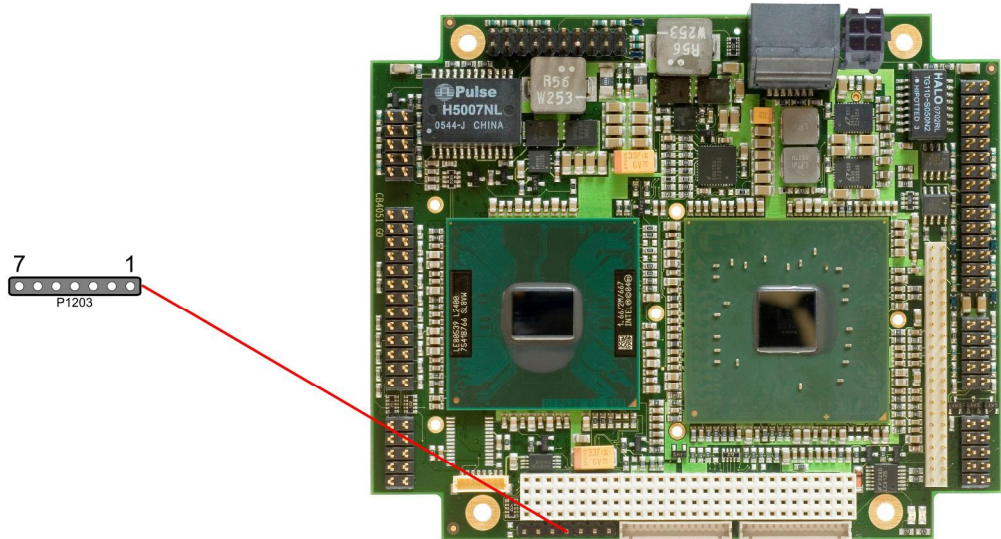
The serial interface is a standard IDC socket connector with a spacing of 2.54 mm. According to the product order, TTL level signals or RS232 standard signals are provided. The port address and the interrupt are set via the BIOS setup.



Description	Name	Pin	Name	Description	
data carrier detect	DCD	1	2	DSR	data set ready
receive data	RXD	3	4	RTS	request to send
transmit data	TXD	5	6	CTS	clear to send
data terminal ready	DTR	7	8	RI	ring indicator
ground	GND	9	10	VCC	5 volt supply

4.15 SMBus

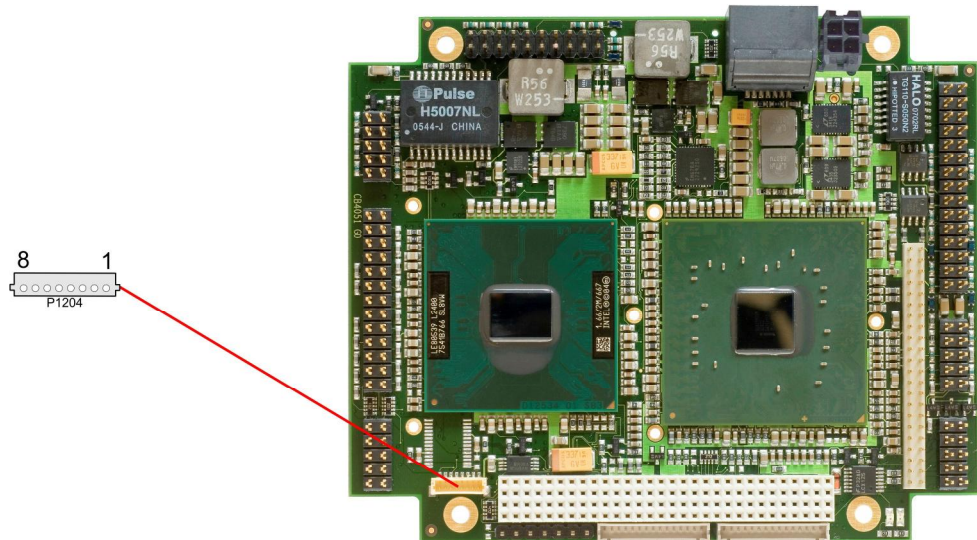
The PB945+ can communicate with external devices via the SMBus protocol. The signals for these protocol are available through a standard IDC socket connector with a spacing of 2.54 mm.



Pin	Name	Description
1	3.3V	3.3 volt supply
2	CS-SMB-CLK	SMBus clock
3	CS-SMB-DAT	SMBus data
4	SMB-ALERT	SMBus alert
5	PWRBTN#	power button
6	PS_ON#	power save on
7	GND	ground

4.16 Monitoring Functions

Some more monitoring functions, e. g. concerning the status of the fan or of other devices connected over SMBus (e. g. temperature sensor), are accessible via an 8 pin connector (JST BM08B-SRSS-TB, mating connector: SHR-08V-S(-B)).



Pin	Name	Description
1	3.3V	3.3 volt supply
2	CS-SMB-CLK	SMBus clock
3	CS-SMB-DAT	SMBus data
4	GND	ground
5	FANON1	fan 1 on
6	FANCTRL1	fan 1 monitor
7	VCC	5 volt supply
8	FANCTRL3	fan 3 monitor

5 BIOS Settings

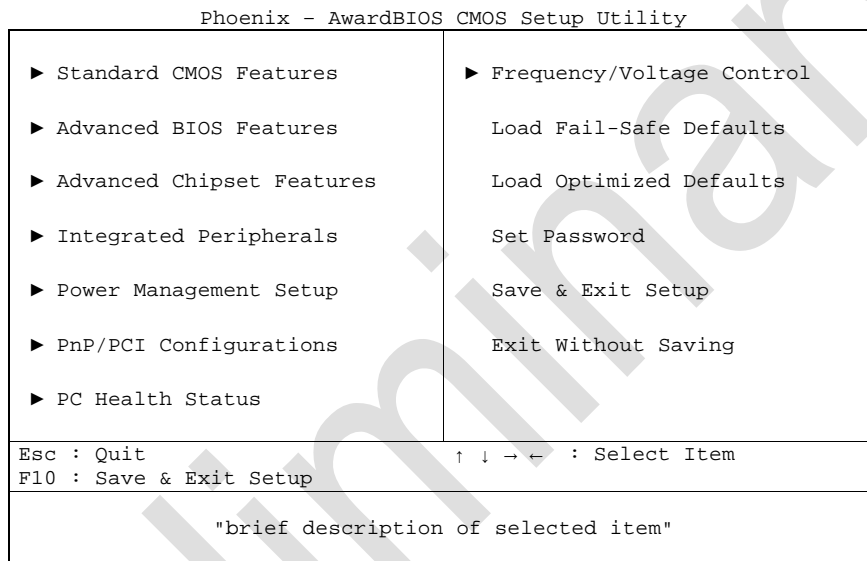
5.1 Remarks for Setup Use

In a setup page, standard values for its setup entries can be loaded. Fail-safe defaults are loaded with F6 and optimized defaults are loaded with F7. These standard values are independent of the fact that a board has successfully booted with a setup setting before.

This is different if these defaults are called from the Top Menu. Once a setup setting was saved, which subsequently leads to a successful boot process, those values are loaded as default for all setup items afterwards.

See also the chapters "Load Fail-Safe Defaults" (5.10) and "Load Optimized Defaults" (5.11).

5.2 Top Level Menu



The sign „▶“ in front of an item means that there is a sub menu.

The „x“ sign in front of an item means, that the item is disabled but can be enabled by changing or selecting some other item (usually somewhere above the disabled item on the same screen).

Use the arrow buttons to navigate from one item to another. For selecting an item press Enter which will open either a sub menu or a dialog screen.

5.3 Standard CMOS-Features

Phoenix - AwardBIOS CMOS Setup Utility
Standard CMOS Features

Date (mm:dd:yy)	Thu, Jan 25 2007	Item Help
Time (hh:mm:ss)	11 : 13 : 35	
▶ IDE Channel 0 Master	[None]	
▶ IDE Channel 0 Slave	[None]	
Drive A	[None]	
Halt On	[No Errors]	
Base Memory	640K	
Extended Memory	2086912K	
Total Memory	2087936K	

↑↓←→:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü Date (mm:dd:yy)

Options: mm: Monat
dd: Tag
yy: Jahr

ü Time (hh:mm:ss)

Options: hh: Stunden
mm: Minuten
ss: Sekunden

ü IDE Channel 0 Master

Sub menu: see "IDE Channel 0 Master/Slave" (p. 36)

ü IDE Channel 0 Slave

Sub menu: see "IDE Channel 0 Master/Slave" (p. 36)

ü Drive A

Options: None / 360K, 5.25 in. / 1.2M, 5.25 in. / 720K, 3.5 in. / 1.44M, 3.5 in. / 2.88M, 3.5 in.

ü Halt On

Options: All Errors / No Errors / All, But Keyboard / All, But Diskette / All, But Disk/Key

ü Base Memory

Options: none

ü Extended Memory

Options: none

ü Total Memory

Options: none

5.3.1 IDE Channel 0 Master/Slave

Phoenix - AwardBIOS CMOS Setup Utility
IDE Channel 0 Master

IDE HDD Auto-Detection	[Press Enter]	Item Help
IDE Channel 0 Master	[Auto]	
Access Mode	[Auto]	
Capacity	0 MB	
Cylinder	0	
Head	0	
Precomp	0	
Landing Zone	0	
Sector	0	

↑↓←→:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü IDE HDD Auto-Detection

Options: none

ü IDE Channel 0 Master

Options: None / Auto / Manual

ü Access Mode

Options: CHS / LBA / Large / Auto

ü Capacity

Options: none

ü Cylinder

Options: none

ü Head

Options: none

ü Precomp

Options: none

ü Landing Zone

Options: none

ü Sector

Options: none

5.4 Advanced BIOS Features

Phoenix - AwardBIOS CMOS Setup Utility
Advanced BIOS Features

		Item Help
▶ CPU Feature	[Press Enter]	
▶ Hard Disk Boot Priority	[Press Enter]	
Virus Warning	[Disabled]	
CPU L1 & L2 Cache	[Enabled]	
CPU L3 Cache	[Enabled]	
Quick Power On Self Test	[Enabled]	
First Boot Device	[Hard Disk]	
Second Boot Device	[Hard Disk]	
Third Boot Device	[Disabled]	
Boot Other Device	[Enabled]	
Boot Up Floppy Seek	[Disabled]	
Boot Up NumLock Status	[On]	
Gate A20 Option	[Fast]	
Typematic Rate Setting	[Disabled]	
x Typematic Rate (Chars/Sec)	6	
x Typematic Delay (Msec)	250	
Security Option	[Setup]	
APIC Mode	[Enabled]	
MPS Version Control For OS	[1.4]	
OS Select For DRAM > 64MB	[Non OS2]	
HDD S.M.A.R.T. Capability	[Enabled]	
Full Screen LOGO Show	[Disabled]	

↑↓←→:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü **CPU Feature**

Sub menu: see "CPU Feature" (p. 39)

ü **Hard Disk Boot Priority**

Sub menu: see "Hard Disk Boot Priority" (p. 40)

ü **Virus Warning**

Options: Enabled / Disabled

ü **CPU L1 & L2 Cache**

Options: Enabled / Disabled

ü **CPU L3 Cache**

Options: Enabled / Disabled

ü **Quick Power On Self Test**

Options: Enabled / Disabled

ü **First Boot Device**

Options: Floppy / LS120 / Hard Disk / CDROM / ZIP100 / USB-FDD / USB-ZIP / USB-CDROM / LAN / Disabled

ü **Second Boot Device**

Options: Floppy / LS120 / Hard Disk / CDROM / ZIP100 / USB-FDD / USB-ZIP / USB-CDROM / LAN / Disabled

ü **Third Boot Device**

Options: Floppy / LS120 / Hard Disk / CDROM / ZIP100 / USB-FDD / USB-ZIP / USB-CDROM / LAN / Disabled

ü **Boot Other Device**

Options: Enabled / Disabled

- ü **Boot Up Floppy Seek**
Options: Enabled / Disabled
- ü **Boot Up NumLock Status**
Options: Off / On
- ü **Gate A20 Option**
Options: Normal / Fast
- ü **Typematic Rate Setting**
Options: Enabled / Disabled
- ü **Typematic Rate (Chars/Sec)**
Options: 6 / 8 / 10 / 12 / 15 / 20 / 24 / 30
- ü **Typematic Delay (Msec)**
Options: 250 / 500 / 750 / 1000
- ü **Security Option**
Options: Setup / System
- ü **APIC Mode**
Options: Enabled / Disabled
- ü **MPS Version Control For OS**
Options: 1.1 / 1.4
- ü **OS Select For DRAM > 64MB**
Options: Non-OS2 / OS2
- ü **HDD S.M.A.R.T. Capability**
Options: Enabled / Disabled
- ü **Full Screen LOGO Show**
Options: Enabled / Disabled

5.4.1 CPU Feature

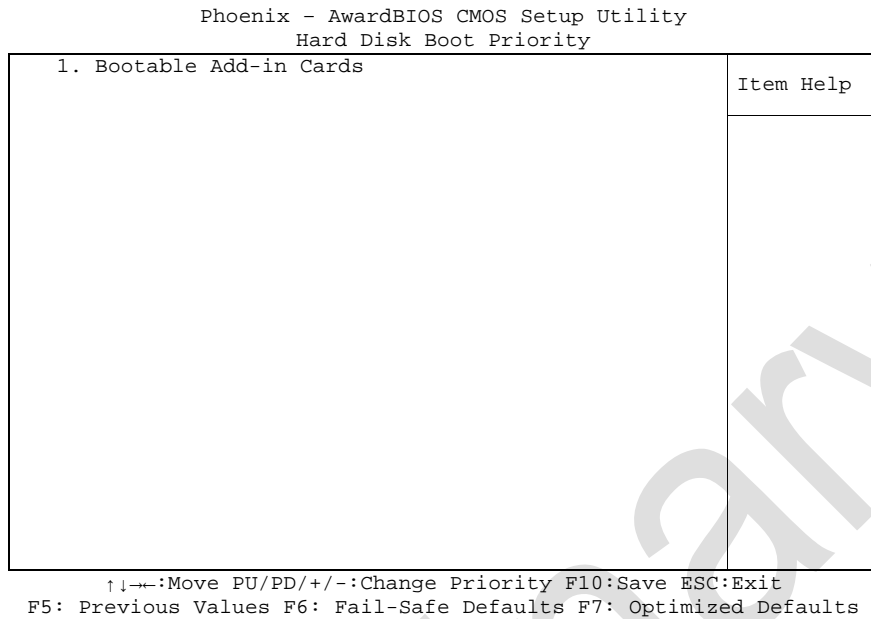
Phoenix - AwardBIOS CMOS Setup Utility
CPU Feature

Delay Prior to Thermal [TM disable] ClE Function [Auto] Execute Disable Bit [Enabled] Virtualization Technology [Enabled]	Item Help
--	-----------

↑↓←→:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

- ü **Delay Prior to Thermal**
Options: 4 Min / 8 Min / 16 Min / 32 Min / TM disable
- ü **Thermal Management**
Options: Auto / Disabled
- ü **Execute Disable Bit**
Options: Enabled / Disabled
- ü **Virtualization Technology**
Options: Enabled / Disabled

5.4.2 Hard Disk Boot Priority



ü [list of available devices]

Options: this dialog allows you to set the order in which the available bootable devices shall be accessed for an attempt to boot.

ü Attention!

in this sub menu the buttons <Page Up>, <Page Down>, <+> and <-> have a different function than in the rest of the setup: They serve to move the items of the list up or down.

5.5 Advanced Chipset Features

Phoenix - AwardBIOS CMOS Setup Utility
Advanced Chipset Features

		Item Help
DRAM Timing Selectable	[By SPD]	
x CAS Latency Time	Auto	
x DRAM RAS# to CAS# Delay	Auto	
x DRAM RAS# Precharge	Auto	
x Precharge delay (tRAS)	Auto	
x System Memory Frequency	Auto	
SLP_S4# Assertion Width	[4 to 5 Sec.]	
System BIOS Cacheable	[Enabled]	
Video BIOS Cacheable	[Disabled]	
Memory Hole At 15M-16M	[Disabled]	
▶ PCI Express Root Port Func	[Press Enter]	
** VGA Setting **		
PEG/Onchip VGA Control	[Auto]	
On-Chip Frame Buffer Size	[8MB]	
DVMT Mode	[DVMT]	
DVMT/FIXED Memory Size	[128MB]	
Boot Display	[Auto]	
Panel Scaling	[Auto]	
Panel Number	[640x480]	

↑←→:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü **DRAM Timing Selectable**

Options: By SPD / Manual

ü **CAS Latency Time**

Options: 5 / 4 / 3 / 6 / Auto

ü **DRAM RAS# to CAS# Delay**

Options: 2 / 3 / 4 / 5 / 6 / Auto

ü **DRAM RAS# Precharge**

Options: 2 / 3 / 4 / 5 / 6 / Auto

ü **Precharge delay (tRAS)**

Options: Auto / 4 / 5 / 6 / 7 / 8 / 10 / 11 / 12 / 13 / 14 / 15

ü **System Memory Frequency**

Options: Auto / 533MHz / 667MHz

ü **SLP_S4# Assertion Width**

Options: 4 to 5 Sec. / 3 to 4 Sec. / 2 to 3 Sec. / 1 to 2 Sec.

ü **System BIOS Cacheable**

Options: Enabled / Disabled

ü **Video BIOS Cacheable**

Options: Enabled / Disabled

ü **Memory Hole At 15M-16M**

Options: Enabled / Disabled

ü **PCI Express Root Port Func**

Sub menu: see "PCI Express Root Port Func" (p. 43)

ü PEG/Onchip VGA Control

Options: Onchip VGA / PEG Port / Auto

ü On-Chip Frame Buffer Size

Options: 1MB / 8MB

ü DVMT Mode

Options: FIXED / DVMT / BOTH

ü DVMT/FIXED Memory Size

Options: 64MB / 128MB / 224MB

ü Boot Display

Options: Auto / CRT / TV / EFP / LFP

ü Panel Scaling

Options: Auto / On / Off

ü Panel Number

Options: 640x480 / 800x600 / 1024x768 / 1280x1024 / 1400x1050 / 1600x1200 / 1280x768 / 1600x1050 / 1920x1200 / 1280x800 / 1440x900

5.5.1 PCI Express Root Port Func

Phoenix - AwardBIOS CMOS Setup Utility
PCI Express Root Port Func

PCI Express Port 1	[Auto]	Item Help
PCI Express Port 2	[Auto]	
PCI Express Port 3	[Auto]	
PCI Express Port 4	[Auto]	
PCI-E Compliancy Mode	[v1.0a]	

↑↓←→:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü PCI Express Port 1

Options: Auto / Enabled / Disabled

ü PCI Express Port 2

Options: Auto / Enabled / Disabled

ü PCI Express Port 3

Options: Auto / Enabled / Disabled

ü PCI Express Port 4

Options: Auto / Enabled / Disabled

ü PCI-E Compliancy Mode

Options: v1.0a / v1.0

5.6 Integrated Peripherals

Phoenix - AwardBIOS CMOS Setup Utility
Integrated Peripherals

▶ OnChip IDE Device	[Press Enter]	Item Help
▶ Onboard Device	[Press Enter]	
▶ SuperIO Device	[Press Enter]	

↑↓←→:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü OnChip IDE Device

Sub menu: see "OnChip IDE Devices" (p. 45)

ü Onboard Device

Sub menu: see "Onboard Devices" (p. 47)

ü SuperIO Device

Sub menu: see "SuperIO Devices" (p. 48)

5.6.1 OnChip IDE Devices

Phoenix - AwardBIOS CMOS Setup Utility
OnChip IDE Device

	Item Help
IDE HDD Block Mode	[Enabled]
IDE DMA transfer access	[Enabled]
On-Chip Primary PCI IDE	[Enabled]
IDE Primary Master PIO	[Auto]
IDE Primary Slave PIO	[Auto]
IDE Primary Master UDMA	[Auto]
IDE Primary Slave UDMA	[Auto]
*** On-Chip Serial ATA Setting ***	
SATA Mode	[IDE]
On-Chip Serial ATA	[Disabled]
SATA PORT Speed Settings	[Disabled]
PATA IDE Mode	[Primary]
SATA Port	P1,P3 is Secondary

↑↓←→:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

- ü **IDE HDD Block Mode**
Options: Enabled / Disabled
- ü **IDE DMA transfer access**
Options: Enabled / Disabled
- ü **On-Chip Primary PCI IDE**
Options: Enabled / Disabled
- ü **IDE Primary Master PIO**
Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4
- ü **IDE Primary Slave PIO**
Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4
- ü **IDE Primary Master UDMA**
Options: Disabled / Auto
- ü **IDE Primary Slave UDMA**
Options: Disabled / Auto
- ü **SATA Mode**
Options: IDE / RAID / AHCI
- ü **On-Chip Serial ATA**
Options: Disabled / Auto / Combined Mode / Enhanced Mode / SATA Only
- ü **SATA PORT Speed Settings**
Options: Disabled / Force GEN I / Force GEN II
- ü **PATA IDE Mode**
Options: none

ü **SATA Port**

Options: none

Preliminary

5.6.2 Onboard Devices

Phoenix - AwardBIOS CMOS Setup Utility
Onboard Device

USB Controller	[Enabled]	Item Help
USB 2.0 Controller	[Enabled]	
USB Keyboard Support	[Disabled]	
Azalia/AC97 Audio	[Auto]	

↑↓←→:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü **USB Controller**

Options: Enabled / Disabled

ü **USB 2.0 Controller**

Options: Enabled / Disabled

ü **USB Keyboard Support**

Options: Enabled / Disabled

ü **Azalia/AC97 Audio Select**

Options: Auto / Azalia / AC97 Audio and Modem / AC97 Audio only / AC97 Modem only / All Disabled

5.6.3 SuperIO Devices

Phoenix - AwardBIOS CMOS Setup Utility
SuperIO Device

Onboard FDC Controller	[Enabled]	Item Help
Onboard Serial Port 1	[3F8/IRQ4]	
Onboard Serial Port 2	[2F8/IRQ3]	
UART Mode Select	[Normal]	
x RxD , TxD Active	Hi,Lo	
x IR Transmission Delay	Enabled	
x UR2 Duplex Mode	Half	
x Use IR Pins	RxD2,TxD2	
Onboard Parallel Port	[378/IRQ7]	
Parallel Port Mode	[SPP]	
EPP Mode Select	[EPP1.7]	
ECP Mode Use DMA	[3]	

↑↓←→:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü Onboard FDC Controller

Options: Enabled / Disabled

ü Onboard Serial Port 1

Options: Disabled / 3F8/IRQ4 / 2F8/IRQ3 / 3E8/IRQ4 / 2E8/IRQ3 / Auto

ü Onboard Serial Port 2

Options: Disabled / 3F8/IRQ4 / 2F8/IRQ3 / 3E8/IRQ4 / 2E8/IRQ3 / Auto

ü UART Mode Select

Options: IrDA / ASKIR / Normal

ü RxD , TxD Active

Options: Hi,Hi / Hi,Lo / Lo,Hi / Lo,Lo

ü IR Transmission Delay

Options: Enabled / Disabled

ü UR2 Duplex Mode

Options: Full / Half

ü Use IR Pins

Options: RxD2,TxD2 / IR-Rx2Tx2

ü Onboard Parallel Port

Options: Disabled / 378/IRQ7 / 278/IRQ5 / 3BC/IRQ7

ü Parallel Port Mode

Options: SPP / EPP / ECP / ECP+EPP / Normal

ü EPP Mode Select

Options: EPP1.9 / EPP1.7

ü **ECP Mode Use DMA**
Options: 1 / 3

Preliminary

5.7 Power Management Setup

Phoenix - AwardBIOS CMOS Setup Utility
Power Management Setup

		Item Help
ACPI Function	[Enabled]	
ACPI Suspend Type	[S1(POS)]	
Run VGABIOS if S3 Resume	Yes	
Power Management	[User Define]	
Video Off Method	[DPMS]	
Video Off in Suspend	[Yes]	
Suspend Type	[Stop Grant]	
Modem Use IRQ	[3]	
Suspend Mode	[Disabled]	
HDD Power Down	[Disabled]	
Soft-Off by PWR-BTTN	[Instant-Off]	
PWRON After PWR-Fail	[On]	
Wake-Up by PCI card	[Disabled]	
Power On by Ring	[Disabled]	
x USB KB Wake-Up From S3	Disabled	
Resume by Alarm	[Disabled]	
x Date(of Month) Alarm	0	
x Time(hh:mm:ss)	0 : 0 : 0	

↑↓←→:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü ACPI function

Options: Enabled / Disabled

ü ACPI Suspend Type

Options: S1(POS) / S3(STR) / S1&S3

ü Run VGABIOS if S3 Resume

Options: Auto / Yes / No

ü Power Management

Options: User Define / Min Saving / Max Saving

ü Video Off Method

Options: Blank Screen / V/H SYNC+Blank / DPMS

ü Video Off In Suspend

Options: No / Yes

ü Suspend Type

Options: Stop Grant / PwrOn Suspend

ü MODEM Use IRQ

Options: NA / 3 / 4 / 5 / 7 / 9 / 10 / 11

ü Suspend Mode

Options: Disabled / 1 Min / 2 Min / 4 Min / 8 Min / 12Min / 20 Min / 30 Min / 40 Min / 1 Hour

ü HDD Power Down

Options: Disabled / 1 Min ... 15 Min

ü Soft-Off by PWR-BTTN

Options: Instant-Off / Delay 4 Sec

ü PWRON After PWR-Fail

Options: Former Sts / On / Off

- ü **Wake Up by PCI Card**
Options: Enabled / Disabled
- ü **Power-On by Ring**
Options: Enabled / Disabled
- ü **USB KB Wake Up From S3**
Options: Enabled / Disabled
- ü **Resume by Alarm**
Options: Enabled / Disabled
- ü **Date(of Month) Alarm**
Options: 1 / ... / 31
- ü **Time (hh:mm:ss) Alarm**
Options: [hh], [mm] und [ss] eintragen
- ü **Primary IDE 0**
Options: Enabled / Disabled
- ü **Primary IDE 1**
Options: Enabled / Disabled
- ü **Secondary IDE 0**
Options: Enabled / Disabled
- ü **Secondary IDE 1**
Options: Enabled / Disabled
- ü **FDD,COM,LPT Port**
Options: Enabled / Disabled
- ü **PCI PIRQ[A-D]#**
Options: Enabled / Disabled
- ü **HPET Support**
Options: Enabled / Disabled
- ü **HPET Mode**
Options: 32-bit mode / 64-bit mode

5.8 PnP/PCI Configuration

Phoenix - AwardBIOS CMOS Setup Utility
PNP/PCI Configurations

Init Display First	[PCI Slot]	Item Help
Reset Configuration Data	[Disabled]	
Resources Controlled By	[Manual]	
▶ IRQ Resources	[Press Enter]	
PCI/VGA Palette Snoop	[Disabled]	
INT Pin 1 Assignment	[Auto]	
INT Pin 2 Assignment	[Auto]	
INT Pin 3 Assignment	[Auto]	
INT Pin 4 Assignment	[Auto]	
INT Pin 5 Assignment	[Auto]	
INT Pin 6 Assignment	[Auto]	
INT Pin 7 Assignment	[Auto]	
INT Pin 8 Assignment	[Auto]	
** PCI Express relative Maximum Payload Size	items ** [128]	

↑↓←→:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü Init Display First

Options: PCI Slot / Onboard

ü Reset Configuration Data

Options: Enabled / Disabled

ü Resources Controlled By

Options: Auto(ESCD) / Manual

ü IRQ Resources

Sub menu: see "IRQ Resources" (p. 54)

ü PCI/VGA Palette Snoop

Options: Enabled / Disabled

ü INT Pin 1 Assignment

Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

ü INT Pin 2 Assignment

Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

ü INT Pin 3 Assignment

Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

ü INT Pin 4 Assignment

Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

ü INT Pin 5 Assignment

Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

ü INT Pin 6 Assignment

Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

ü INT Pin 7 Assignment

Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

ü INT Pin 8 Assignment

Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

ü Maximum Payload Size

Options: 128 / 256 / 512 / 1024 / 2048 / 4096

5.8.1 IRQ Resources

Phoenix - AwardBIOS CMOS Setup Utility
IRQ Resources

IRQ-3	assigned to	[PCI Device]	Item Help
IRQ-4	assigned to	[PCI Device]	
IRQ-5	assigned to	[PCI Device]	
IRQ-7	assigned to	[PCI Device]	
IRQ-9	assigned to	[PCI Device]	
IRQ-10	assigned to	[PCI Device]	
IRQ-11	assigned to	[PCI Device]	
IRQ-12	assigned to	[PCI Device]	
IRQ-14	assigned to	[PCI Device]	
IRQ-15	assigned to	[PCI Device]	

↑↓←→:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü IRQ-3 assigned to

Options: PCI Device / Reserved

ü IRQ-4 assigned to

Options: PCI Device / Reserved

ü IRQ-5 assigned to

Options: PCI Device / Reserved

ü IRQ-7 assigned to

Options: PCI Device / Reserved

ü IRQ-9 assigned to

Options: PCI Device / Reserved

ü IRQ-10 assigned to

Options: PCI Device / Reserved

ü IRQ-11 assigned to

Options: PCI Device / Reserved

ü IRQ-12 assigned to

Options: PCI Device / Reserved

ü IRQ-14 assigned to

Options: PCI Device / Reserved

ü IRQ-15 assigned to

Options: PCI Device / Reserved

5.9 PC Health Status

Phoenix - AwardBIOS CMOS Setup Utility
PC Health Status

Shutdown Temperature	[Disabled]	Item Help
On Die Digital Temp.	54°C	
Temp. Board	46°C	
CPU Core	1.12V	
GMCH Core	1.05V	
CPU VTT	1.07V	
Memory 1.8V	1.84V	
+3.3 V	3.29V	
+5.0 V	4.99V	
VBatt	2.65V	
Fan1 Speed	12500 RPM	
Fan2 Speed	0 RPM	
Fan3 Speed	0 RPM	
Board Revision	0	

↑↓←→:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

- ü **Shutdown Temperature**
Options: 60°C/140°F / 65°C/149°F / 70°C/158°C / Disabled
- ü **On Die Digital Temp.**
Options: none
- ü **Temp. Board**
Options: none
- ü **CPU Core**
Options: none
- ü **GMCH Core**
Options: none
- ü **CPU VTT**
Options: none
- ü **Memory 1.8 V**
Options: none
- ü **+3.3 V**
Options: none
- ü **+5.0 V**
Options: none
- ü **VBatt**
Options: none
- ü **Fan1 Speed**
Options: none
- ü **Fan2 Speed**
Options: none

ü **Fan3 Speed**

Options: none

ü **Board Revision**

Options: none

Preliminary

5.10 Frequency/Voltage Control

Phoenix - AwardBIOS CMOS Setup Utility
Frequency / Voltage Control

Auto Detect PCI Clk	[Enabled]	Item	Help
Spread Spectrum	[-0.25%]		

↑↓←→:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü **Auto Detect PCI Clk**

Options: Enabled / Disabled

ü **Spread Spectrum**

Options: -0.25% / -0.5% / -0.75% / -1% / +-0.125% / +-0.25% / +-0.375% / +-0.5%

5.11 Load Fail-Safe Defaults

If this option is chosen, the last working setup is loaded from flash. Working means that the setup setting has already led to a successful boot process.

At the first setting of the BIOS setup, safe values are loaded which lets the board boot. This status is reached again, if the board is reprogrammed with the corresponding flash-program and the required parameters.

5.12 Load Optimized Defaults

This option applies like described under "Remarks for Setup Use" (5.1).

At first start of the BIOS, optimized values are loaded from the setup, which are supposed to make the board boot. This status is achieved again, if the board is reprogrammed using the flash program with the required parameters.

5.13 Set Password

Here you can enter a password to protect the BIOS settings against unauthorized changes. Use this option with care! Forgotten or lost passwords are a frequent problem.

5.14 Save & Exit Setup

Settings are saved and the board is restarted.

5.15 Exit Without Saving

This option leaves the setup without saving any changes.

6 Software and Drivers

6.1 Drivers

The following table gives an overview of required and available drivers for some operating systems. If a required operating system is not listed and the installation of the operating system failed, please ask your distributor for a driver or another solution.

Attention

Please note, that you should install the latest service pack for the OS prior to driver installation.

Operating System	Chipset	VGA	USB	IDE	AC97	LAN
Windows 98/SE	CD	CD	CD	CD	CD	CD
Windows ME	CD	CD	CD	CD	CD	CD
Windows NT4	CD	CD	CD	CD	CD	CD
Windows 2000	CD	CD	CD	CD	CD	OS/CD
Windows XP	CD	CD	CD	CD	CD	OS/CD
Linux	OS	CD	OS	OS	CD	OS

OS Included in the operating system or no driver required.
 CD A driver will be delivered on a CD.

6.2 BIOS update

The program "AWDFLASH.EXE" of the company Phoenix is used to update the BIOS. It is important, that the program is started from a DOS environment without a virtual memory manager such as for example "EMM386.EXE". In case such a memory manager is loaded, the program will stop with an error message. The system must not be interrupted during the flash process, otherwise the update is stopped and the BIOS is destroyed afterwards.

The program should be started as follows:

```
awdflash [biosfilename] /sn /cc /cd /cp
```

/sn Do not save the current BIOS
 /cc Clear the CMOS
 /cd Clear the DMI information
 /cp Clear the PnP information

The erasure of CMOS, DMI and PnP is strongly recommended. This ensures, that the new BIOS works correctly and that all chipset registers, which were saved in the setup, are reinitialized through the BIOS. A complete description of all valid parameters is shown with the parameter "/?".

In order to make the BIOS run automatically, the parameter "/py" must be added. This parameter bypasses all security checks within the programming.

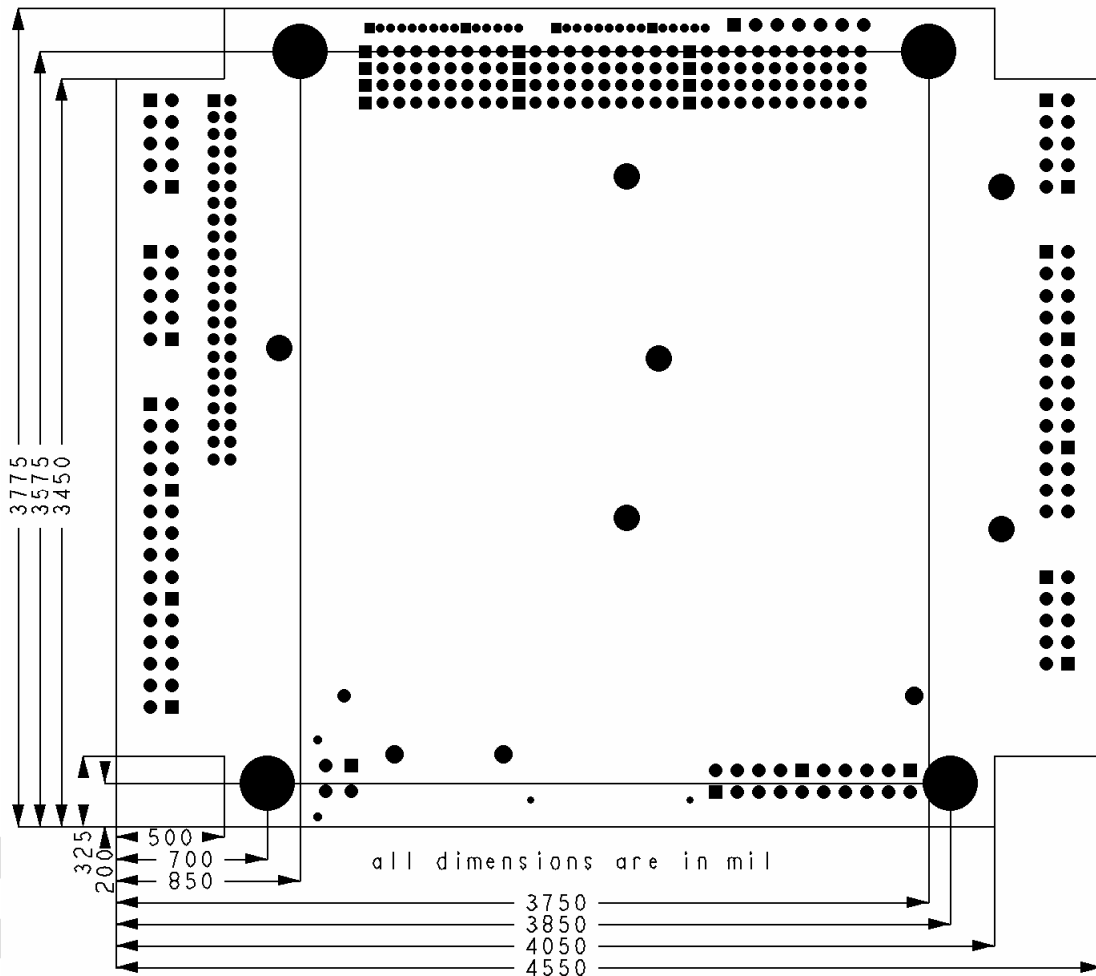
7 Mechanical Drawing

7.1 PCB: Mounting Holes

A true dimensioned drawing can be found in the PC/104 specification.

! Attention

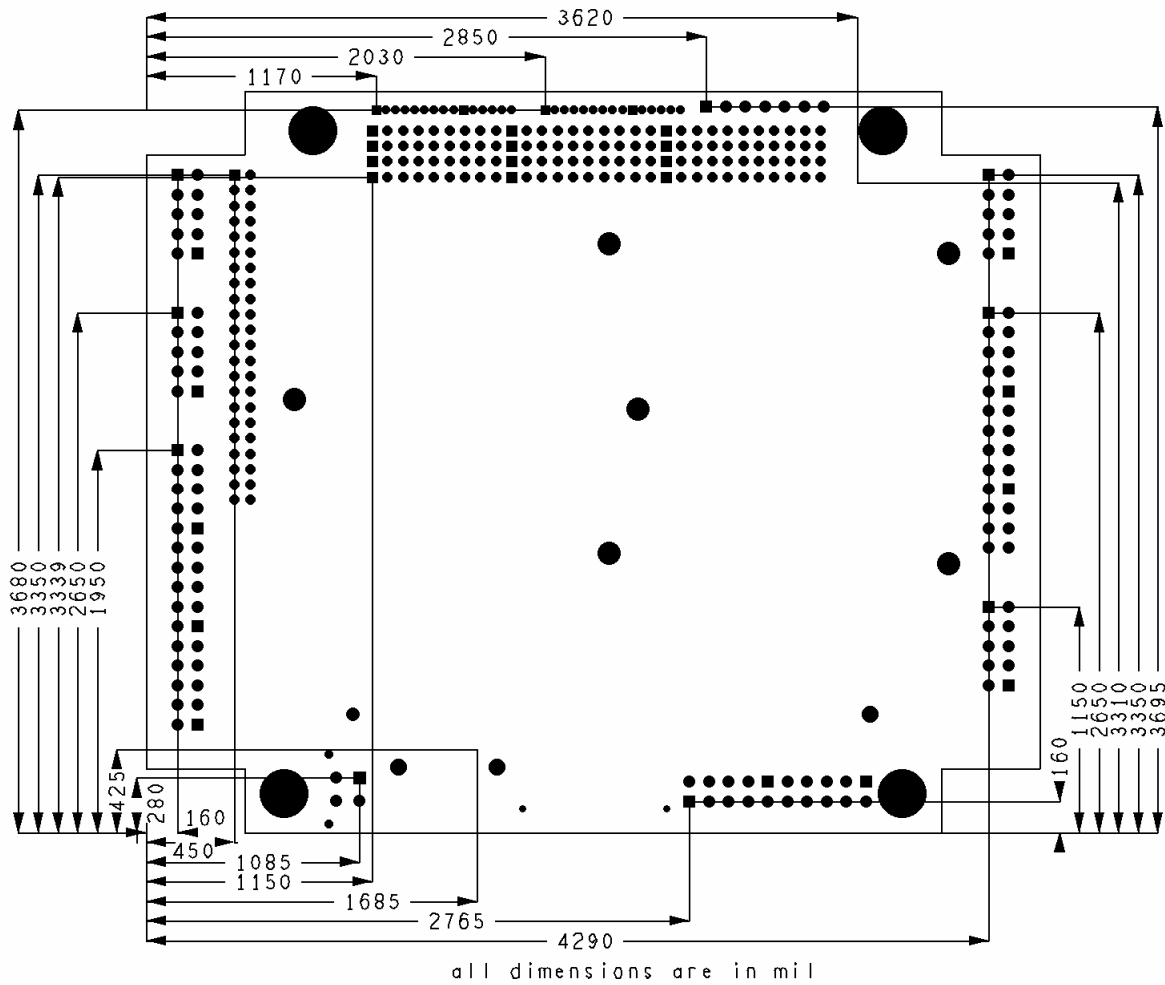
All dimensions are in mil (1 mil = 0,0254 mm)



7.2 PCB: Pin 1 Dimensions

! *Attention*

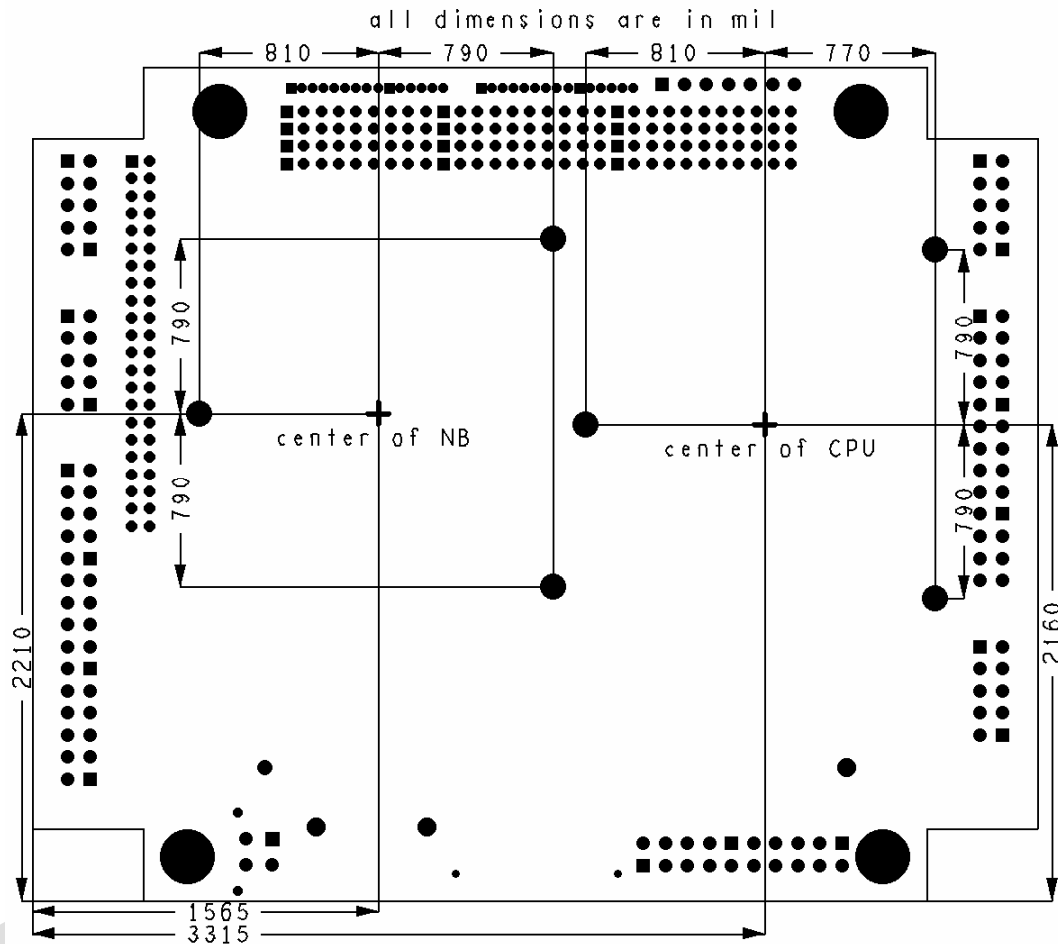
All dimensions are in mil (1 mil = 0,0254 mm)



7.3 PCB: Heat Sink

! *Attention*

All dimensions are in mil (1 mil = 0,0254 mm)



8 Thermal Specifications

The environmental temperature range is from -25°C to 60°C .

It has to be ensured that the DIE temperature of the processor does not exceed 100°C . The typical and the maximum power consumption must be considered. The maximum power consumption may be twice as much and should be used as a basis for the cooling concept.

Additional controllers may also affect the cooling concept. The power consumption of such components may be comparable to the consumption of the processor.

Attention

The end customer has the responsibility to ensure that the DIE temperature of the processor does not exceed 100°C . Permanent overheating may destroy the board!

In case the temperature exceeds 100°C the environmental temperature must be reduced. Under certain circumstances sufficient air circulation must be provided.

I Annex: Post-Codes

Code	Description
01h	The Xgroup-program code is written in the random access memory from address 1000:0 onwards.
03h	Initialise Variable/Routine "Superio_Early_Init".
05h	1. Cancel display 2. Cancel CMOS error flag
07h	1. Cancel 8042 (keyboard controller) Interface Register 2. Initialising and self testing of 8042 (keyboard controller)
08h	1. Test of special keyboard controllers (Winbond 977 super I/O Chip-series). 2. Enabling of the keyboard-interface register
0Ah	1. Disabling of the PS/2 mouse interface (optional). 2. Auto-detection of the connectors for Keyboard and mouse, optional: swap of PS/2 mouse ports and PS/2 interfaces.
0Eh	Test of the F000h-memory segment (Read/Write ability). In case of an error a signal will come out of the loud speakers.
10h	Auto-detection of the flash-rom-type and loading of the suitable Read/Write program into the run time memory segment F000 (it is required for ESCD-data & the DMI-pool-support).
12h	Interface-test of the CMOS RAM-logic (walking 1's"-algorithm). Setting of the power status of the real-time-clock (RTC), afterwards test of register overflow.
14h	Initialising of the chip-set with default values. They can be modified through a software (MODBIN) by the OEM-customer.
16h	Initialise Variable/Routine "Early_Init_Onboard_Generator".
18h	CPU auto-detection (manufacturer, SMI type (Cyrrix or Intel), CPU-class (586 or 686).
1Bh	Initialising if the interrupt pointer table. If nothing else is pretended, the hardware interrupts will point on "SPURIOUS_INT_HDLR and the software interrupts will point on SPURIOUS_soft_HDLR.
1Dh	Initialise Variable/Routine EARLY_PM_INIT.
1Fh	Load the keyboard table (Notebooks)
21h	Initialising of the hardware power management (HPM) (Notebooks)
23h	1. Test the validity of the RTC-values (Example: "5Ah" is an invalid value for an RTC-minute). 2. Load the CMOS-values into the BIOS Stack. Default-values are loaded if CMOS-checksum errors occur. 3. Preparing of the BIOS 'resource map' for the PCI & plug and play configuration. If ESCD is valid, take into consideration the ESCD's legacy information. 4. Initialise the onboard clock generator. Clock circuit at non-used PCI- and DIMM slots. 5. First initialising of PCI-devices: assign PCI-bus numbers - alot memory- & I/O resources - search for functional VGA-controllers and VGA-BIOS and copy the latter into memory segment C000:0 (Video ROM Shadow).
27h	Initialise cache memory for INT 09
29h	1. Program the CPU (internal MTRR at P6 and PII) for the first memory address range (0-640K). 2. Initialising of the APIC at CPUs of the Pentium-class. 3. Program the chip-set according to the settings of the CMOS-set-up (Example: Onboard IDE-controller). 4. Measuring of the CPU clock speed. 5. Initialise the video BIOS.
2Dh	1. Initialise the "Multi-Language"-function of the BIOS 2. Soft copy, e.g. Award-Logo, CPU-type and CPU clock speed...
33h	Keyboard-reset (except super I/O chips of the Winbond 977 series)
3Ch	Test the 8254 (timer device)
3Eh	Test the interrupt Mask bits of IRQ-channel 1 of the interrupt controller 8259.
40h	Test the interrupt Mask bits of IRQ-channel 2 of the interrupt controller 8259
43h	Testing the function of the interrupt controller (8259).
47h	Initialise EISA slot (if existent).

Code	Description
49h	1. Determination of the entire memory size by revising the last 32-Bit double word of each 64k memory segment. 2. Program "write allocation" at AMD K5-CPU's.
4Eh	1. Program MTRR at M1 CPU's 2. Initialise level 2-cache at CPU's of the class P6 and set the "cacheable range" of the random access memory. 3. Initialise APIC at CPU's of the class P6. 4. Only for multiprocessor systems (MP platform): Setting of the "cacheable range" on the respective smallest value (for the case of non-identical values).
50h	Initialise USB interface
52h	Testing of the entire random access memory and deleting of the extended memory (put on "0")
55h	Only for multi processor systems (MP platform): Indicate the number of CPU's.
57h	1. Indicate the plug and play logo 2. First ISA plug and play initialising – CSN-assignment for each identified ISA plug and play device.
59h	Initialise TrendMicro anti virus program code.
5Bh	(Optional:) Indication of the possibility to start AWDFLASH.EXE (Flash ROM programming) from the hard disk.
5Dh	1. Initialise Variable/Routine Init_Onboard_Super_IO. 2. Initialise Variable/Routine Init_Onboard_AUDIO.
60h	Release for starting the CMOS set-up (this means that before this step of POST, users are not able to access the BIOS set-up).
65h	Initialising of the PS/2 mouse.
67h	Information concerning the size of random access memory for function call (INT 15h with AX-Reg. = E820h).
69h	Enable level 2 cache
6Bh	Programming of the chip set register according to the BIOS set-up and auto-detection table.
6Dh	1. Assignment of resources for all ISA plug and play devices. 2. Assignment of the port address for onboard COM-ports (only if an automatic junction has been defined in the setup).
6Fh	1. Initialising of the floppy controller 2. Programming of all relevant registers and variables (floppy and floppy controller).
73h	Optional feature: Call of AWDFLASH.EXE if: - the AWDFLASH program was found on a disk in the floppy drive. - the shortcut ALT+F2 was pressed.
75h	Detection and installation of the IDE drives: HDD, LS120, ZIP, CDROM...
77h	Detection of parallel and serial ports.
7Ah	Co-processor is detected and enabled.
7Fh	1. Switch over to the text mode, the logo output is supported. - Indication of possibly emerged errors. Waiting for keyboard entry. - No errors emerged, respective F1 key was pressed (continue): Deleting of the EPA- or own logo.
82h	1. Call the pointer to the "chip set power management". 2. Load the text font of the EPA-logo (not if a complete picture is displayed) 3. If a password is set, it is asked here.
83h	Saving of the data in the stack, back to CMOS.
84h	Initialising of ISA plug and play boot drives (also Boot-ROMs)
85h	1. Final initialising of the USB-host. 2. At network PC's (Boot-ROM): Construction of a SYSID structure table 3. Backspace the scope presentation into the text mode 4. Initialise the ACPI table (top of memory). 5. Initialise and link ROMs on ISA cards 6. Assignment of PCI-IRQs 7. Initialising of the advanced power management (APM) 8. Set back the IRQ-register.

Code	Description
93h	Reading in of the hard disk boot sector for the inspection through the internal anti virus program (trend anti virus code)
94h	<ol style="list-style-type: none"> 1. Enabling of level 2 cache 2. Setting of the clock speed during the boot process 3. Final initialising of the chip set. 4. Final initialising of the power management. 5. Erase the onscreen and display the overview table (rectangular box). 6. Program "write allocation" at K6 CPUs (AMD) 7. Program "write combining" at P6 CPUs (INTEL)
95h	<ol style="list-style-type: none"> 1. Program the changeover of summer-and winter-time 2. Update settings of keyboard-LED and keyboard repeat rates
96h	<ol style="list-style-type: none"> 1. Multi processor system: generate MP-table 2. Generate and update ESCD-table 3. Correct century settings in the CMOS (20xx or 19xx) 4. Synchronise the DOS-system timer with CMOS-time 5. Generate an MSIRQ-Routing table..
C0h	Chip set initialising: <ul style="list-style-type: none"> - Cut off shadow RAM - Cut off L2 cache (apron 7 or older) - Initialise chip set register
C1h	Memory detection: <ul style="list-style-type: none"> Auto detection of DRAM size, type and error correction (ECC or none) Auto detection of L2 cache size (apron 7 or older)
C3h	Unpacking of the packed BIOS program codes into the random access memory.
C5h	Copying of the BIOS program code into the shadow RAM (segments E000 & F000) via chipset hook.
CFh	Testing of the CMOS read/write functionality
FFh	Boot trial over boot-loader-routine (software-interrupt INT 19h)