Materials inside the Semiconductor Chips

Santosh K Kurinec
Fellow IEEE
Electrical & Microelectronic Engineering
Kate Gleason College of Engineering
Rochester Institute of Technology, Rochester, NY

The Advanced Materials Show USA & The Nanotechnology Show USA, October 13-14, 2021

Broad Spectrum of Semiconductor Chips Applications

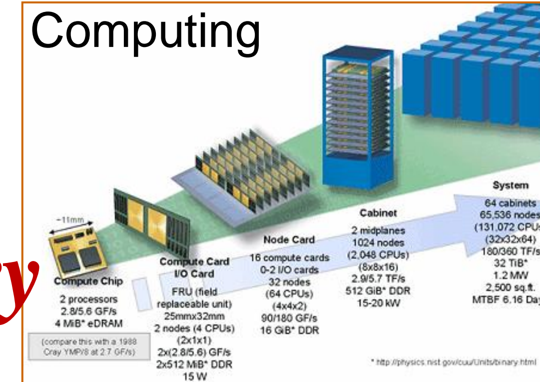
Communications

The World of Semiconductors

The Amazing Revolutionary Microchip (or Nanochip!)

Manufacturing

Entertainment



Computing

Transportation

Display

Space and Earth Sciences

Agriculture and Environment

National Defense

Medical Advances

Energy & Power

Electrical Conductivity Spans ~ > 25 Orders of Magnitude

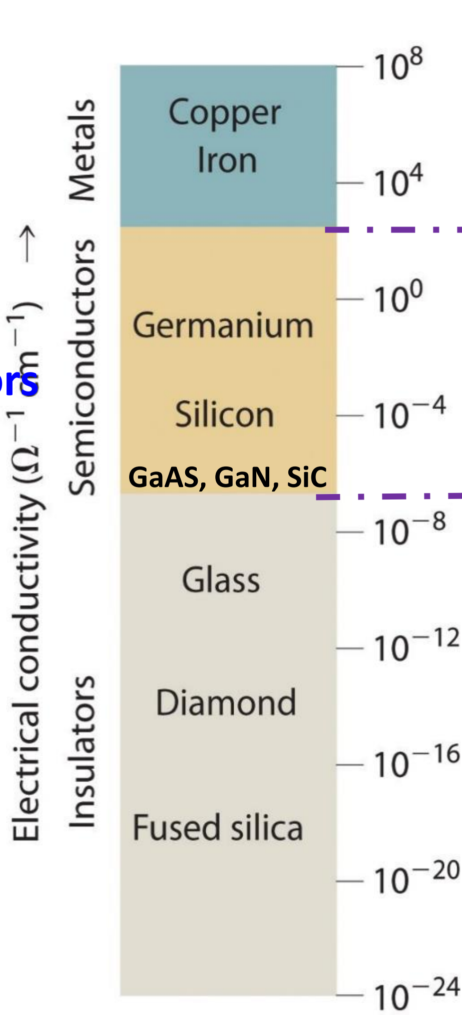
THE Advanced Materials SHOW | USA
THE NANOTECHNOLOGY SHOW

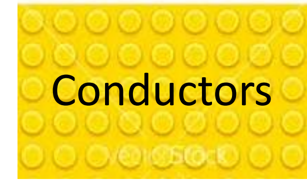
Largest varying physical property

Metals
Conductors

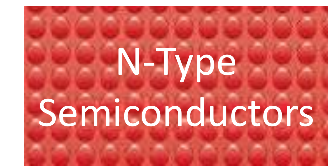
Semiconductors

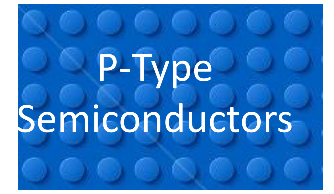
Insulators

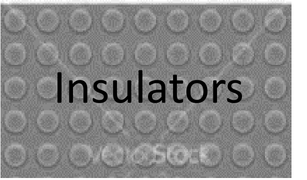




Can make them
N type
or
P type
by doping







Building blocks
of electronic circuits

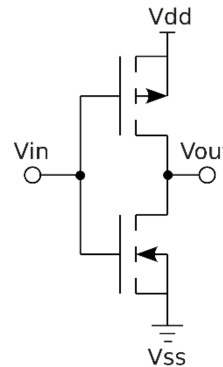
Schottky diodes/Ohmic contacts

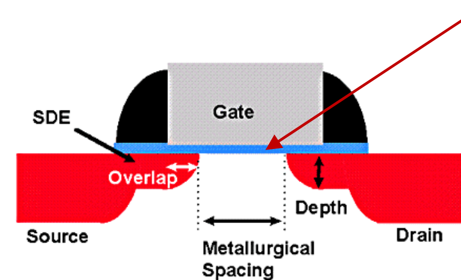
PN Diodes

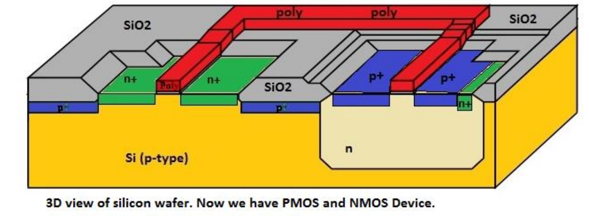
Heterojunctions

MOS Capacitors

The MOS transistor is the foundation of digital logic





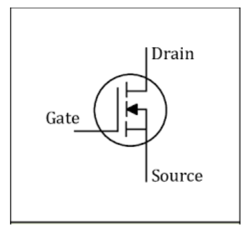


3D view of silicon wafer. Now we have PMOS and NMOS Device.

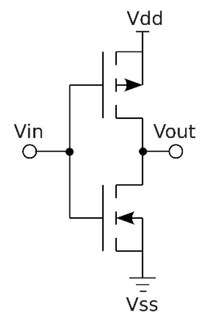
MOS Switch to Logic Gates to Processors

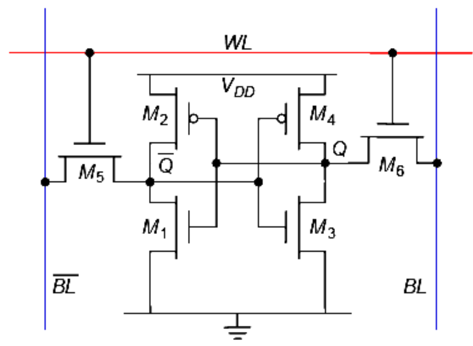
THE Advanced Materials SHOW | USA   THE NANOTECHNOLOGY SHOW

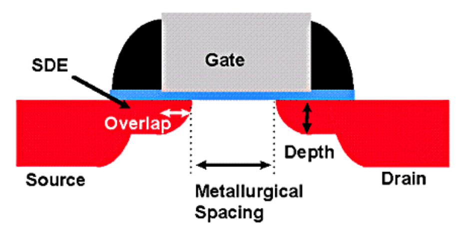
Switch: Metal Oxide Semiconductor Field Effect Transistor

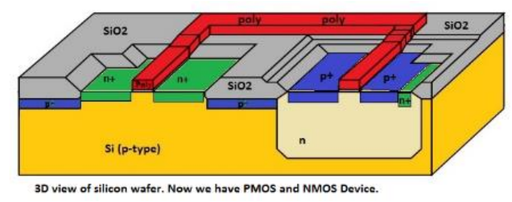


Logic Gates

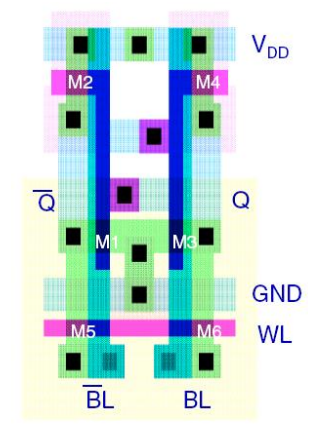




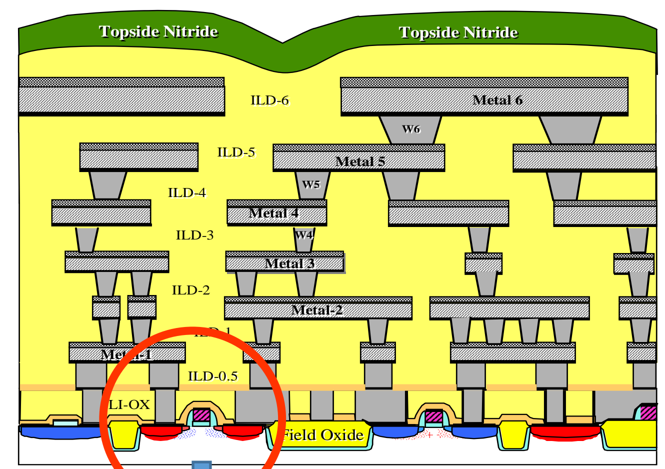




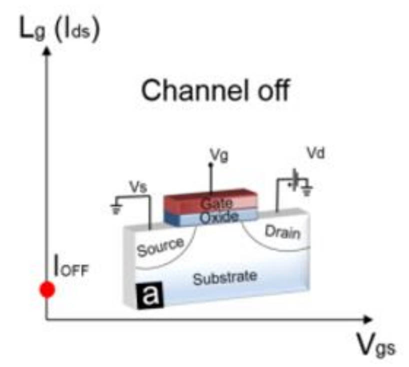
Cross-Sectional Schematic

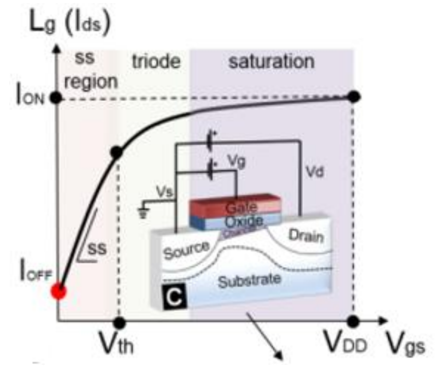


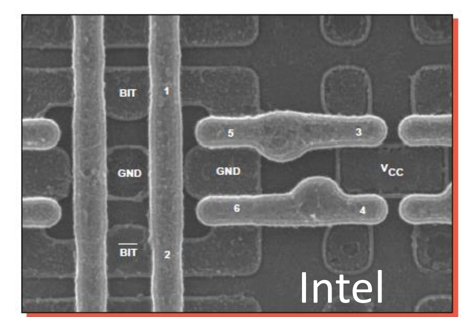
Functional Chip



Smallest unit: A MOS switch







Requirements: High Ion/Ioff ratio; Steeper subthreshold slope

How Chips are Made?

Sand

300mm

Ingot

Silicon crystal
sliced into wafers

Processing
Completed

etching, deposition,
implant, oxidation

MIRROR
LENS
MASK
LENS
WAFER
TABLE

Dice the
wafers into
small die

Packaging

silicon
chip
5 mm
notch
small
dot
plastic
case

Mounted on
circuit board

Moore’s Law: Stages of Scaling

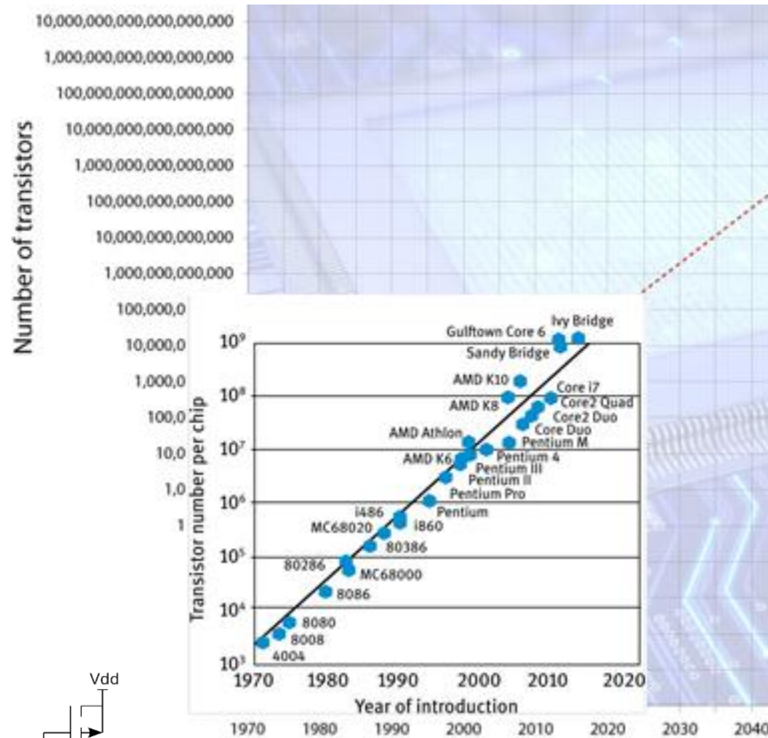
THE Advanced Materials SHOW | USA   THE NANOTECHNOLOGY SHOW

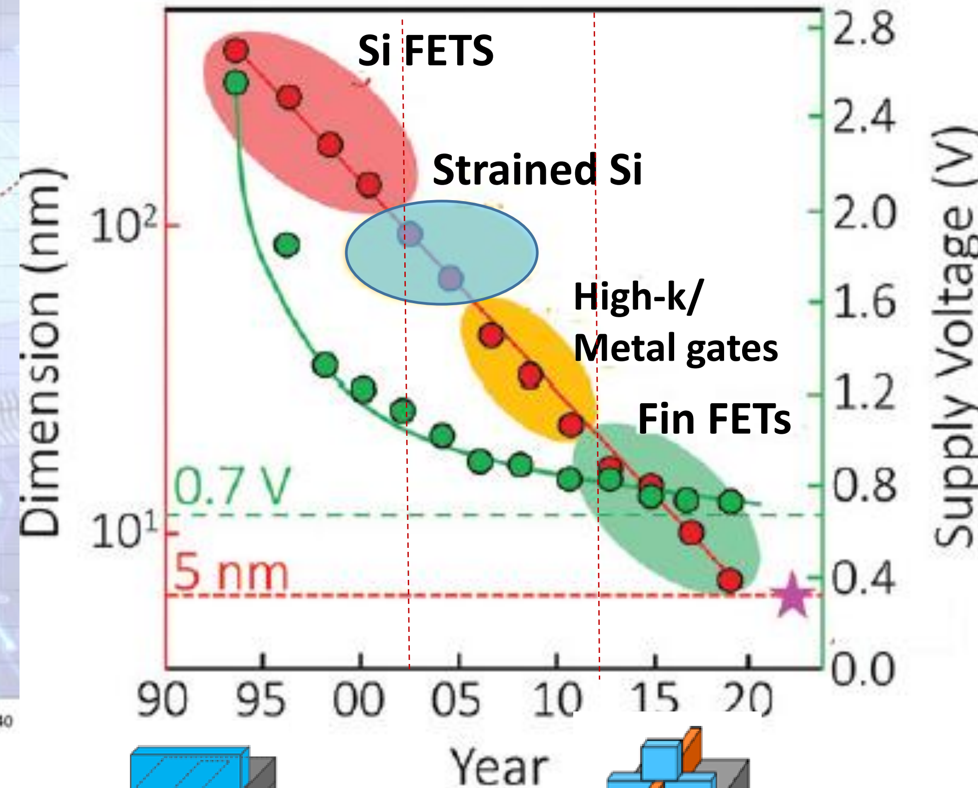
Each new generation of silicon provided a profusion of value: chips captured more functionality at higher performance, with lower power per function, and at lower cost per circuit.

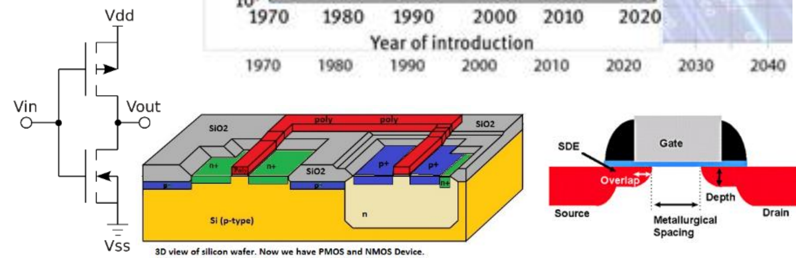
Cramming more components onto integrated circuits

Moores’ Law” was predicted by the co-founder of Intel®, Gordon Moore, in 1965

Scalings Geometrical, Equivalent, FinFET







Enablers:

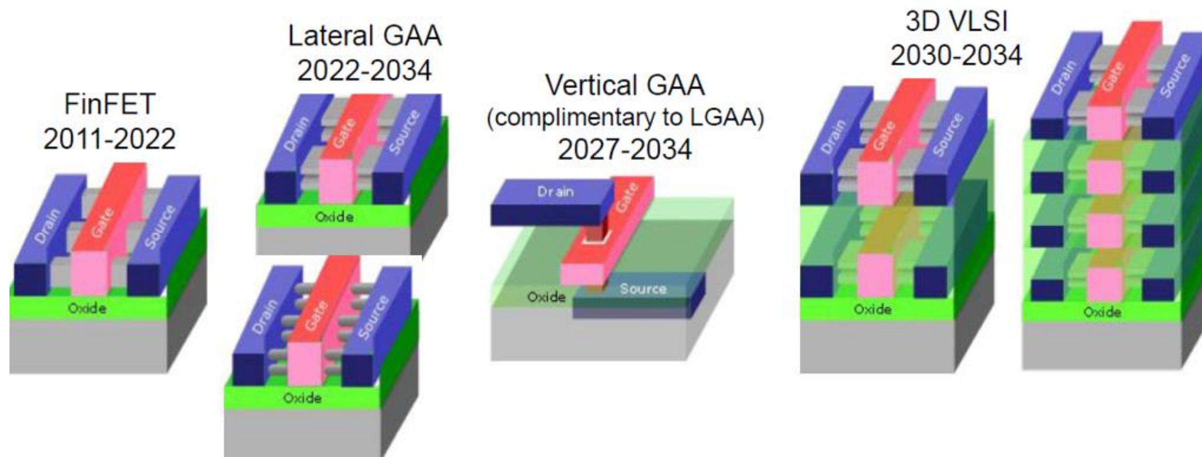
- **Remarkable innovations in photolithography**
- **Materials and Processes**
- **Designs**

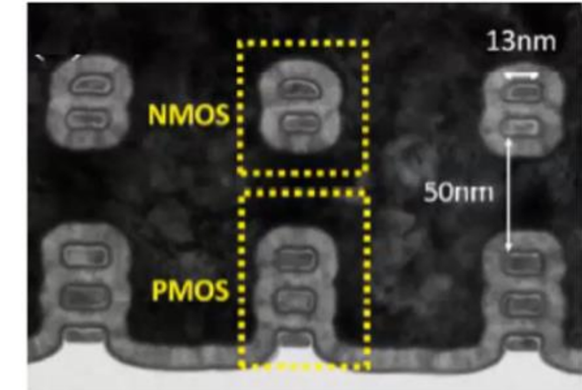
Accelerated Density Scaling –Push for more Complex Device Structures

FinFET Scaling

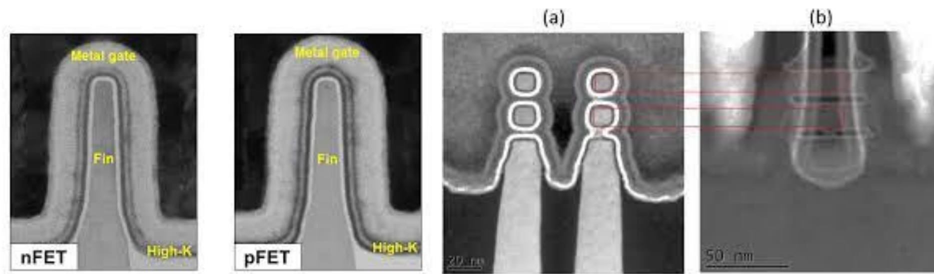
THE Advanced Materials SHOW | USA
THE NANOTECHNOLOGY SHOW

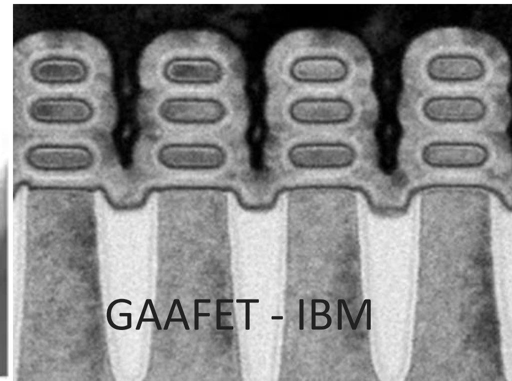
FinFET to Gate All Around to Nanowire and Nanosheets

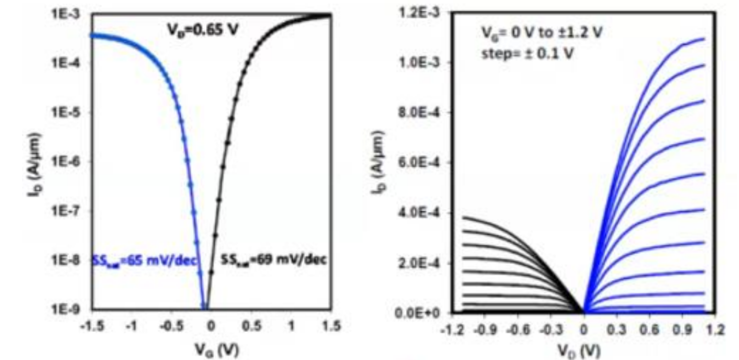




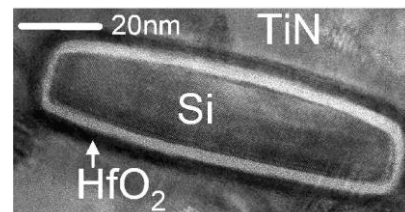
Ref: IDRS, 2020







TEM images of Fins, nanowire and nanoshhets.

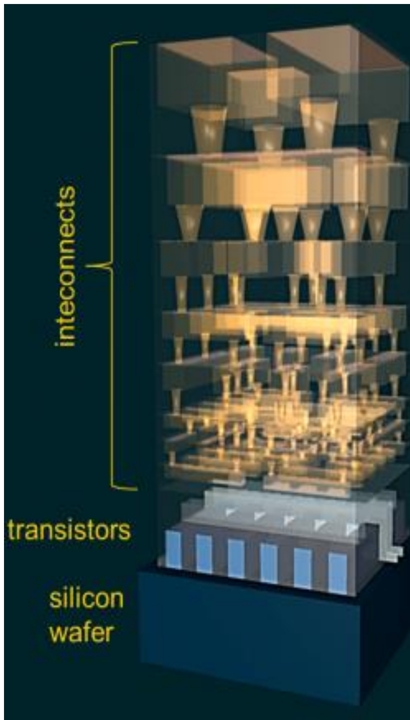


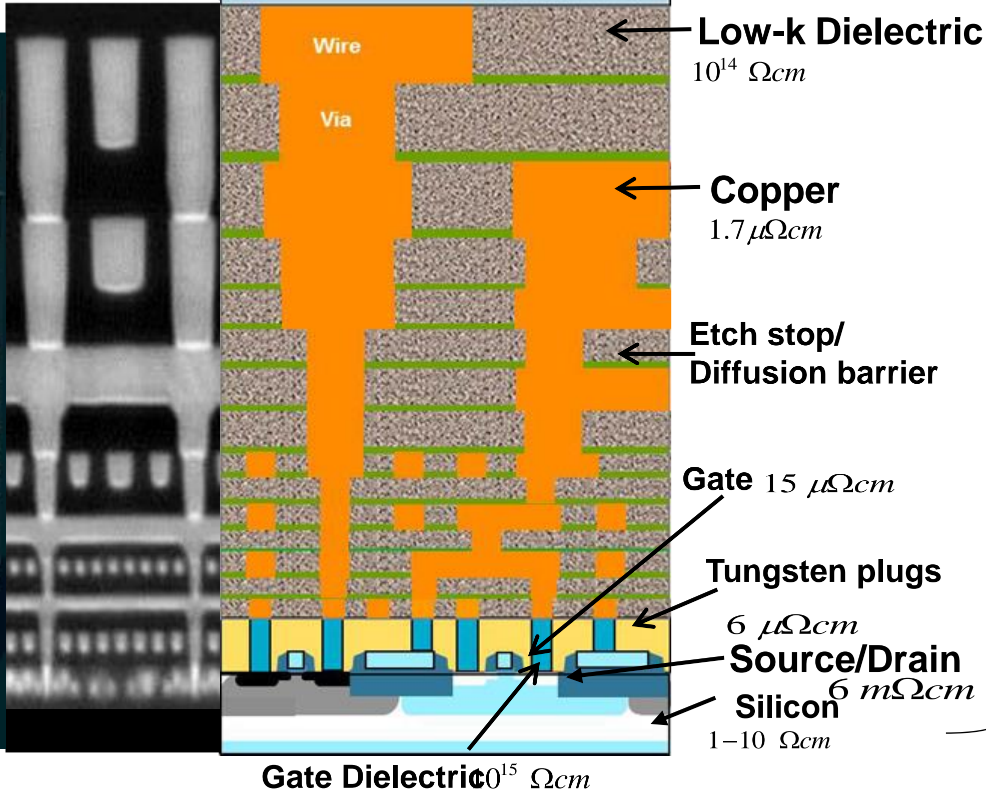
Transfer and output characteristics of 75 nm gate stacked channel MOSFETs

Huang et al, Tech. Dig. IEDM, 425-28 (2019)

Back End of the Line:

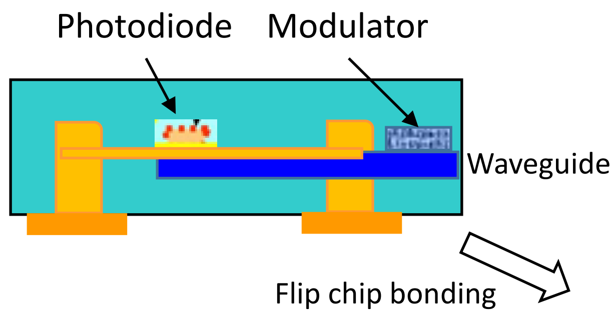
- Aluminum to Copper
- Electroplating
- Chemical Mechanical Planarization (CMP)
- Liners
- Low-k Dielectrics
- Optical Interconnests
- Cu to Co



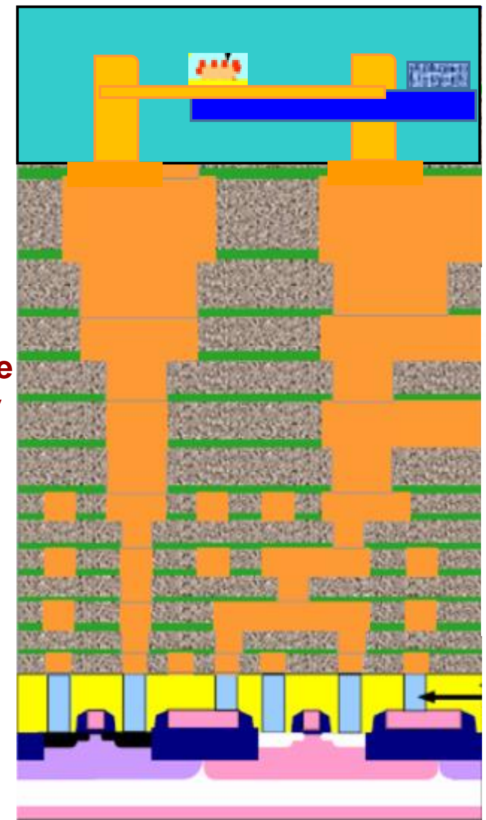


21 orders of change in magnitude of resistivity

Optical layer

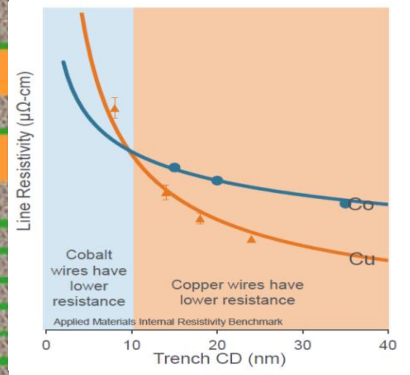


Optical Interconnects

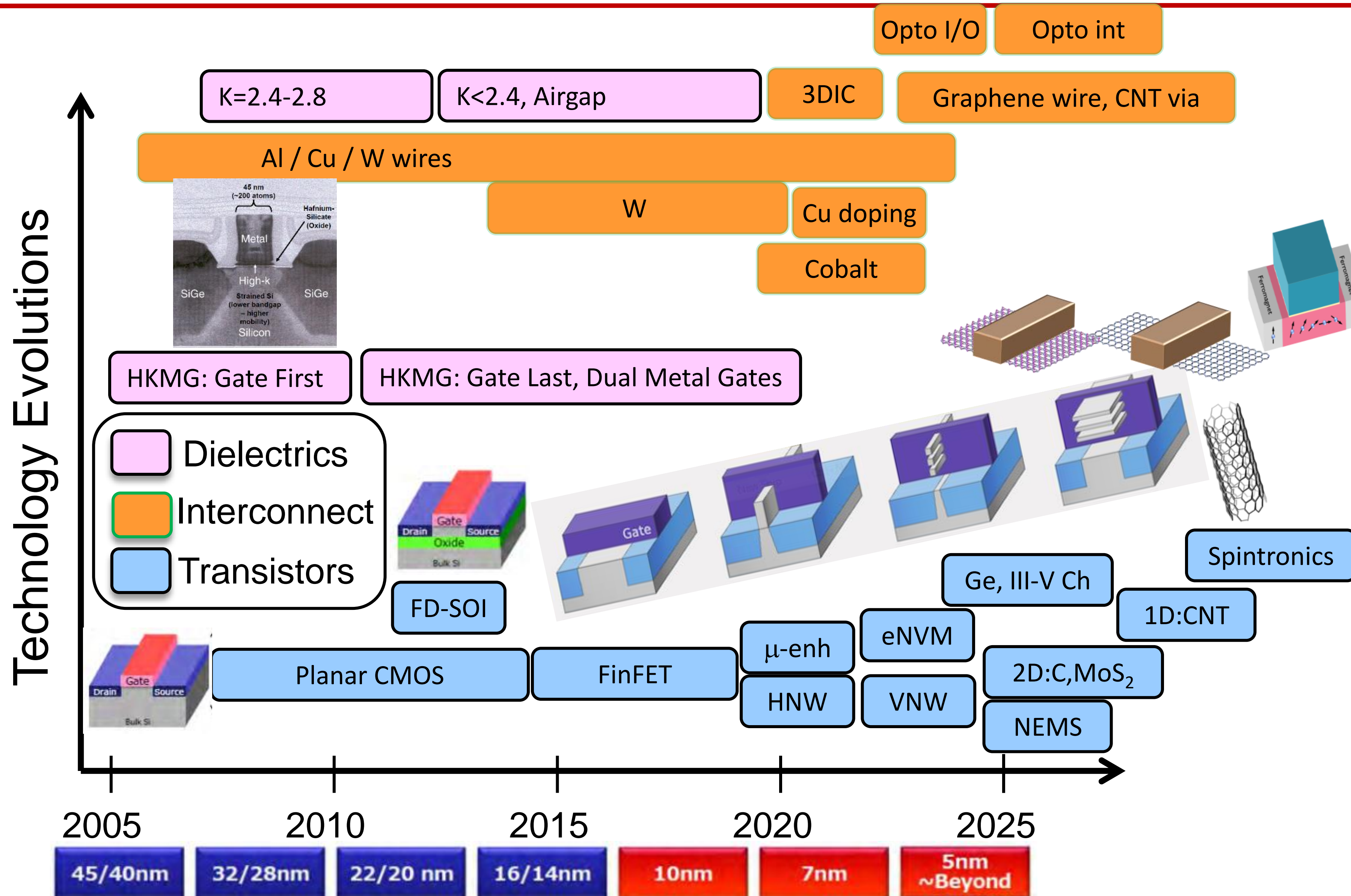


Light Source

Cobalt for < 10nm lines?



Technology Evolutions with Scaling in the CMOS Transistors



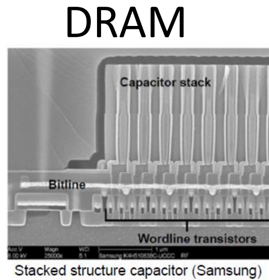
Different Memory Devices

Memory Devices

Volatile Memory

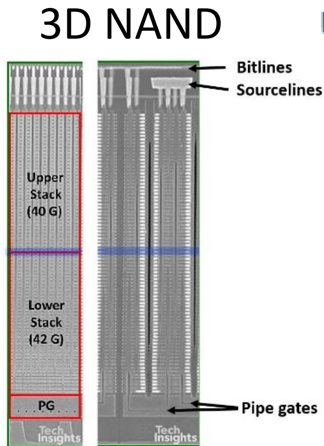
Non-Volatile Memory

DRAM



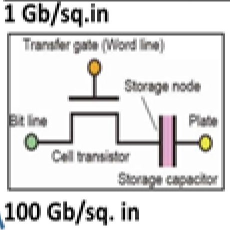
Stacked structure capacitor (Samsung)

3D NAND

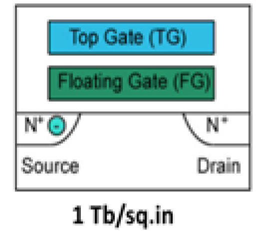


SRAM

DRAM



1 Gb/sq.in



100 Gb/sq. in

Charge Trap

FLASH

SONOS

Top Gate (TG)

Floating Gate (FG)

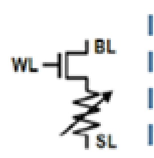
Source

Drain

1 Tb/sq.in

Polarization change

FRAM



Resistance Change

PRAM

MRAM

RRAM

FTJ

Phase change causes resistance change

Magneto-resistance change

Interface or bulk resistance change

Tunelling electroresistance change

Atom Movement

Electron Spin Movement

Ion Movement

Ferroelectric Polarization Change

Chemical Change

DNA

Storage structure physically changes

Charge based Programming & Reading

Current based Programming & Reading

Storage class

Magnetic Recording

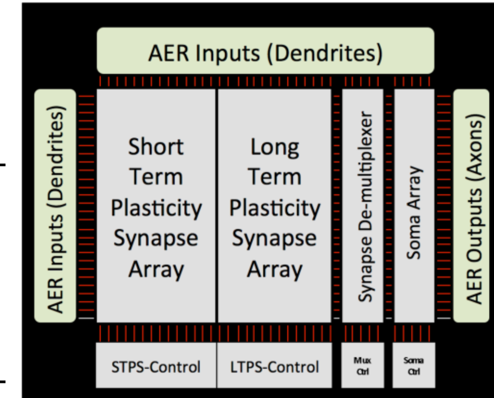
PMR→HAMR →HDMR

10Tb/in^2

Perpendicular, heated dot assisted, heated dot magnetic recording

Emerging Neuromorphic Devices

Devices	Schematic	Mechanism	Materials	Switching Energy	On/Off	# of states
PCM		Phase change	Chalcogenides GST	>100 fJ	$<10^3$	~20
RRAM		Resistance change: filamentary, ion, vacancy movement	Metal oxides 2D materials Perovskites	>20 fJ	10-100	64-500
MRAM		Magnetization switching	CoFeB, MgO	>10 fJ	2-3	~2
ECRAM		Electrochemically driven ion movement	Metal oxides Graphene PEDOT:PSS	>10 fJ	2-40	50-1000
Mott Memristor		Metal to insulator phase transition	NbO2, VO2	> 1 pJ	> 500	~2
FETs/FTJ		Polarization switching	Doped HfO2, HZO	> 100 fJ	45-300	32-100



Ferroelectricity in Doped HfO2

THE Advanced Materials SHOW | USA

THE NANOTECHNOLOGY SHOW

P, P_R, P_S, E_C, E_C, E, $-P_R$

HfO$_2$	HfO$_2$-ZrO$_2$	ZrO$_2$
monoclinic	orthorhombic	tetragonal

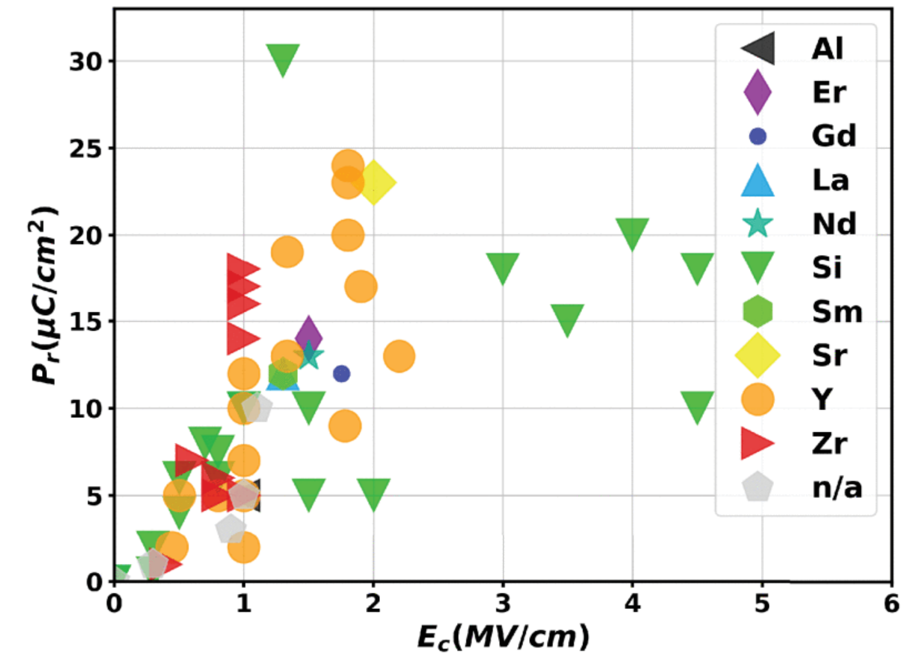
log counts, 2Θ, P, E

$V_G > 0$ Gate, Ferroelectric, n+, n+, p-Substrate

I_D, ON, OFF, MW, V_G

$V_G < 0$ Gate, n+, n+, p-Substrate

Ferroelectricity demonstrated in doped HfO2



Muller, 2011
Boscke, 2011
Boescke, 2011
Yurchuk, 2012
Olsen, 2012
Zhou, 2012
Mueller, 2012
Lomenzo, 2014
Schroeder, 2014
Starschich, 2014
Park, 2015
Polakowski, 2015

Johannes Müller et al, Nano Lett., 2012, 12 (8), pp 4318–4323
DOI: 10.1021/nl302049k

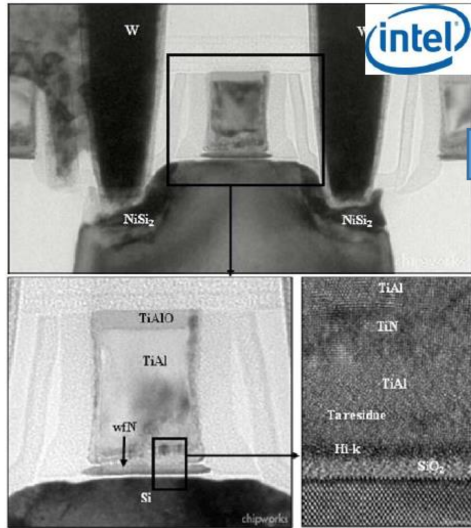
J. D. Anderson, J. Merkel, D. MacMahon, and S. K. Kurinec, "Evaluation of Si:HfO2 Ferroelectric Properties in MFM and MFIS Structures," *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 525–534, 2018, doi: 10.1109/JEDS.2018.2826978.

HfO2 - From High-k to Ferroelectric Gate Oxide

THE Advanced Materials SHOW | USA   THE NANOTECHNOLOGY SHOW

Introduction of HfO_2 as Gate- Oxide Replacement

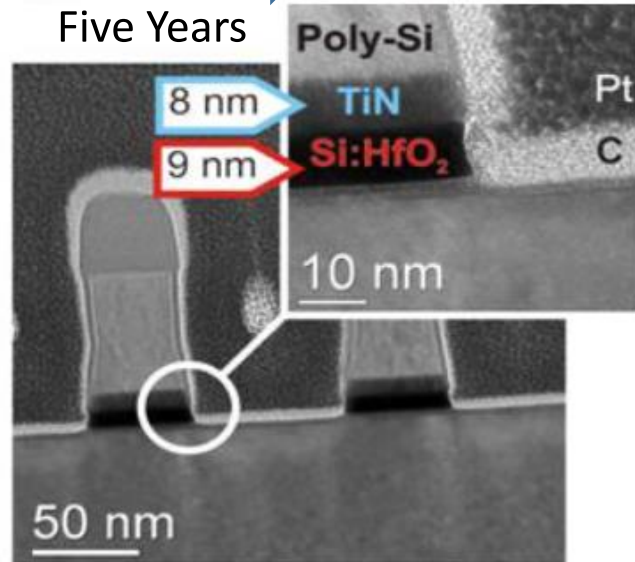
Intel 45 nm node (2007):



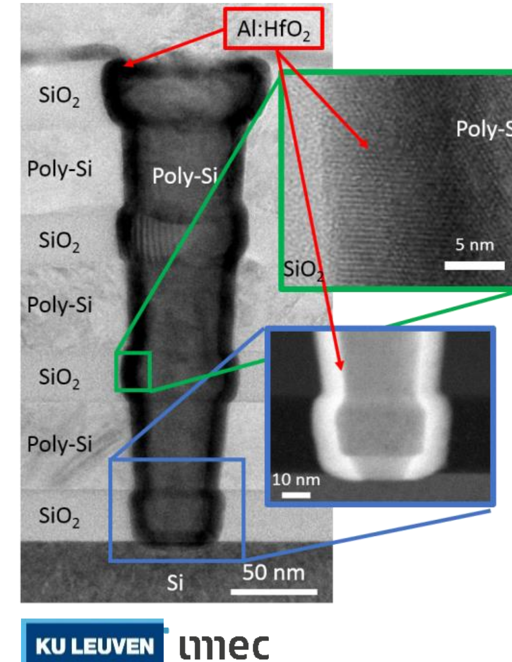
World's first 28 nm Si:HfO_2 FeFET

Globalfoundries 28 nm node (2012):

Five Years

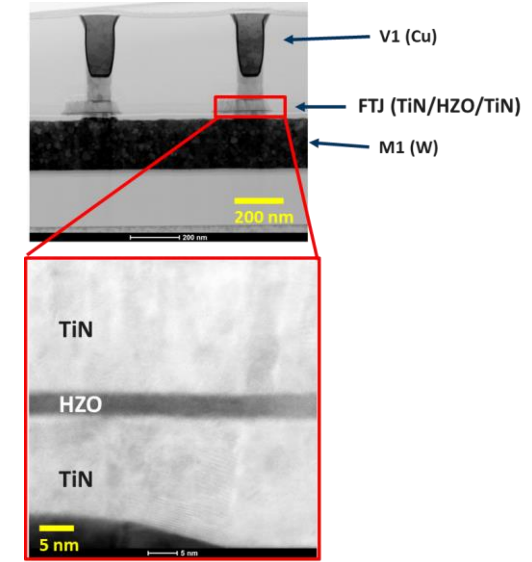


First demonstration of vertically stacked FE HfO_2 capacitors

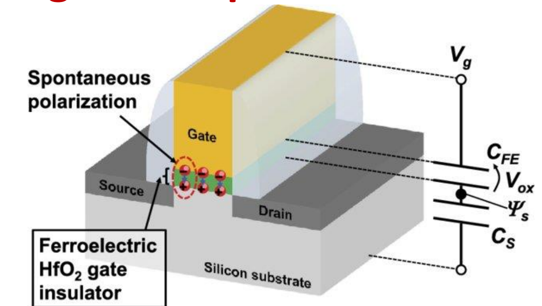


Emereging Devices

Ferroelectric Tunnel Junction



Negative Capacitance FeFET



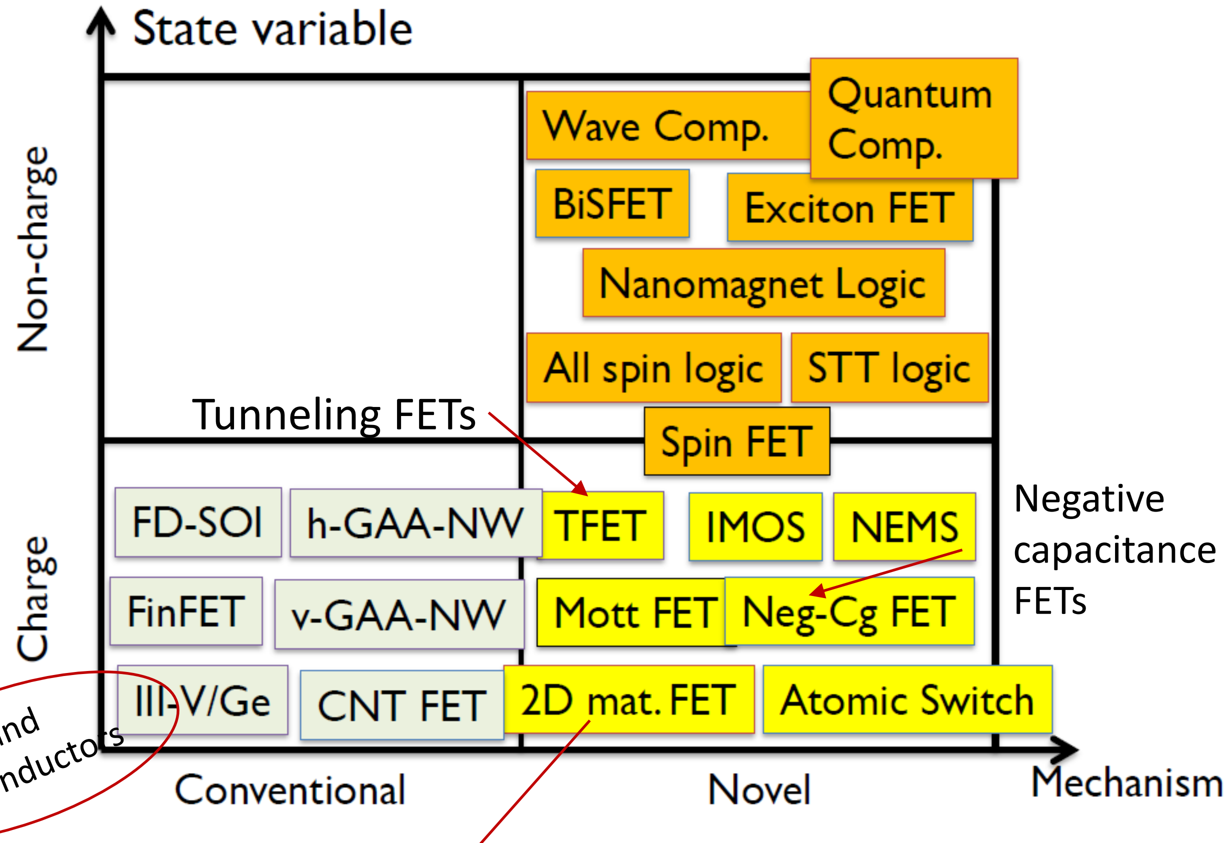
Source: J J. Müller et al., "Ferroelectricity in HfO_2 Enables Nonvolatile Data Storage in 28 nm HKMG", 2012 IEEE Symposia on VLSI Technology and Circuits, submitted for publication.

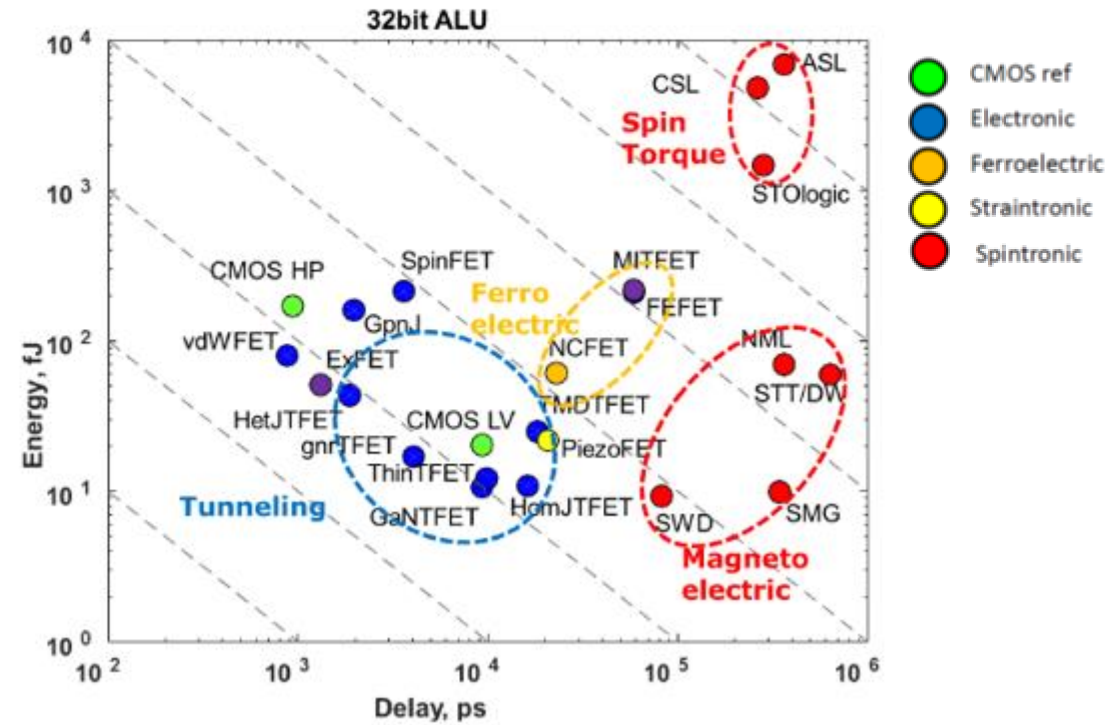
K. Florent et al., IEEE IEDM, pp. 2.5.1-2.5.4, 2018.

Silicon & Beyond

THE Advanced Materials SHOW | USA
THE NANOTECHNOLOGY SHOW

Conventional MOS switching speed limited by change in entropy
Landauer limit: 60mV/decade
Explore other switching mechanisms/ materials





Switching energy vs delay for 32bit Arithmatic Logic Unit

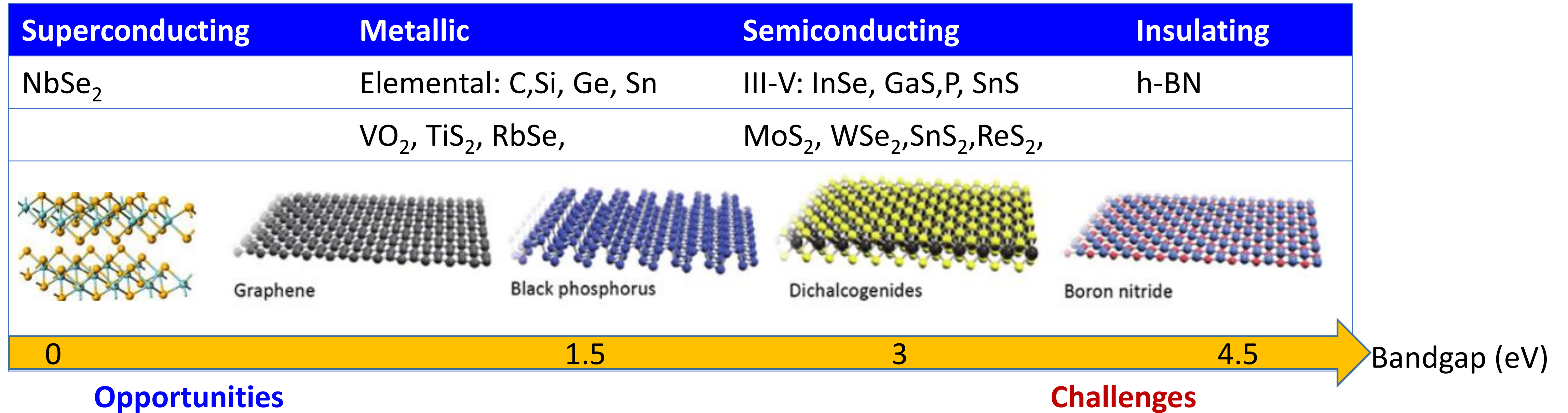
They include graphene, black phosphorus, transition metal dichalcogenides, and boron nitride nanosheets.

Chang et. al. (Intel, Ian Young), "Clocked Domain Wall Logic using MagnetoelectricEffects," IEEE Journal on Exploratory Solid-State Computational Devices and Circuits , Year: 2016, Volume: PP, Issue: 99

Prof. Aaron Thean, *Director, E6 Nanofabrication Center, HiFESResearch Program National University of Singapore*

imec

Bank of New 2D Mateials:



Superconducting	Metallic	Semiconducting	Insulating
$NbSe_2$	Elemental: C,Si, Ge, Sn	III-V: InSe, GaS,P, SnS	h-BN
	VO_2, TiS_2, RbSe,	MoS_2, WSe_2,SnS_2,ReS_2,	

Opportunities

2-D materials are ~ an atom or two thick, they can be either grown atop silicon or they can be grown separately, and then transferred on arbitrary substrates.

Some 2-D materials, especially graphene, dissipate heat well

2D semiconductors provide best electrostatic control for low power consumption concurrently with lateral channel scaling

Challenges

Considerable challenges exist in the scalable and damage-free fabrication of 2D transistors, including doping, contact and dielectric integration.

Growth of uniform high quality material at wafer scales and compatible temperatures is also a major challenge.

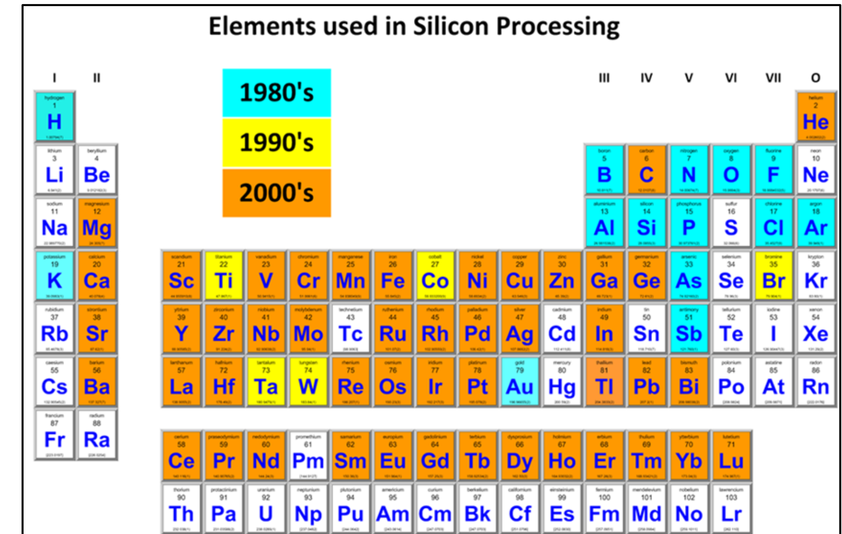
Deposition and patterning with high pitch density on 300nm remains very challenging, and must be explored to justify these materials as Si replacement.

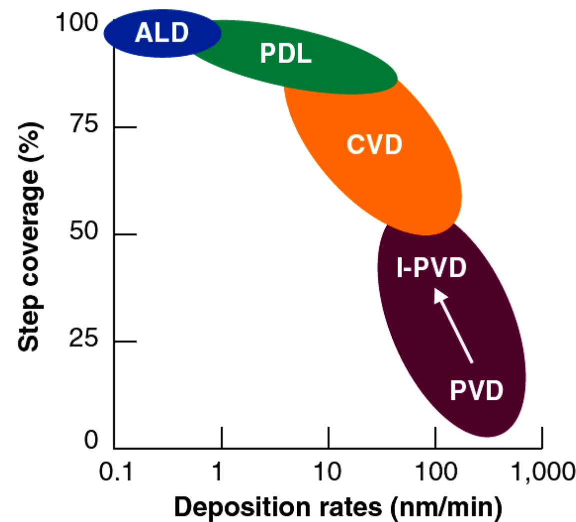
Published in IEEE Journal of the Electron Devices Society 2019
Ultimate Monolithic-3D Integration With 2D Materials: Rationale, Prospects, and ChallengesJunkai Jiang, K. Parto, W. Cao, K. Banerjee

Materials & Processes

- More and more materials are being incorporated
- New processes are being developed and implemented
- Selective patterning with high pitch density is desired

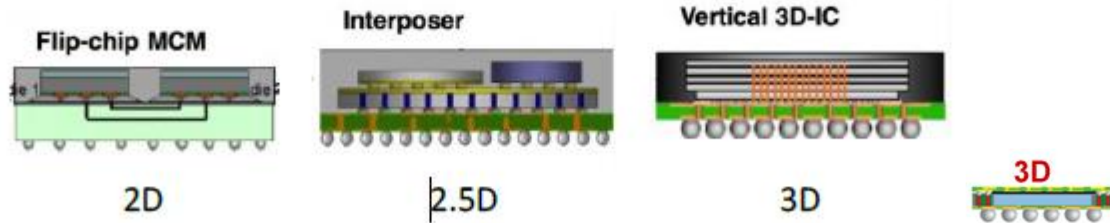
Deposition	Etching
Physical vapor deposition (PVD)	Wet etching
Chemical vapor deposition (CVD)	Dry etching
Thermal diffusion/growth	Ion milling
Atomic layer deposition(ALD)	Stripping
Electrochemical deposition	Chemical mechanical planarization
Spin coating	Atomic layer etching
Laser deposition	Lift-off

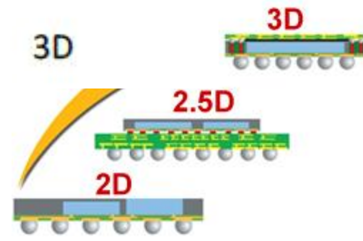


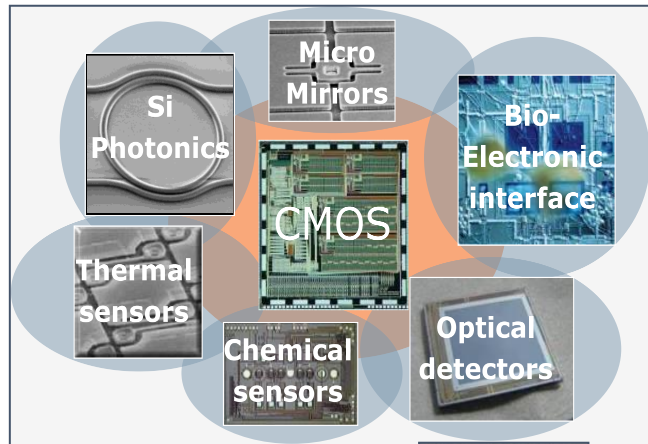


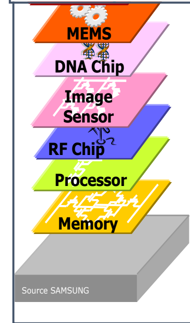
Sputtering Materials for VLSI and Thin Film Devices
By Jaydeep Sarkar

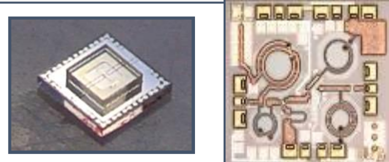
Heterogeneous Integration (HI)



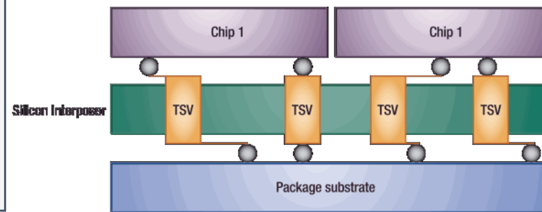


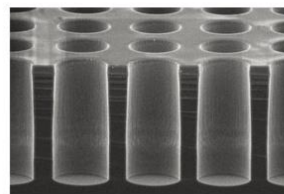


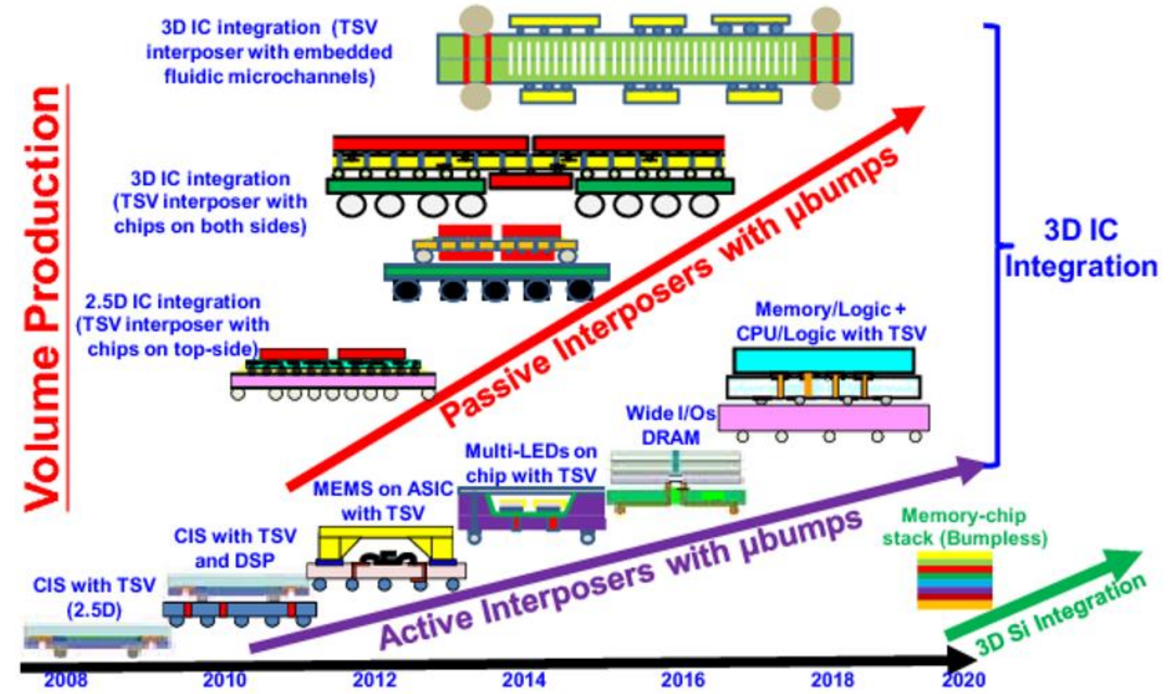


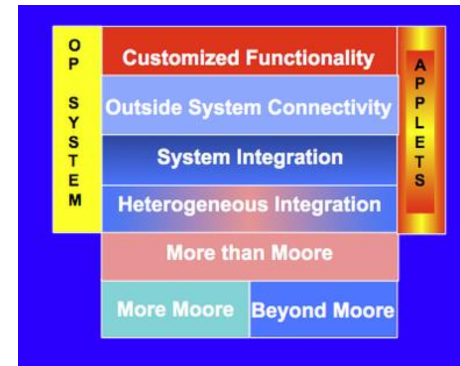


TSV: Through Si Via









Evolution, challenge, and outlook of TSV, 3D IC integration and 3d silicon integration
•J. Lau, Materials Science, 2011 International Symposium on Advanced Packaging Materials (APM)

Concluding Remarks

Si is the foundational material for semiconductor devices.

Its abudance, electronic & chemical properties are super and scalability to 7nm device technology in production and 3nm Demonstrated.

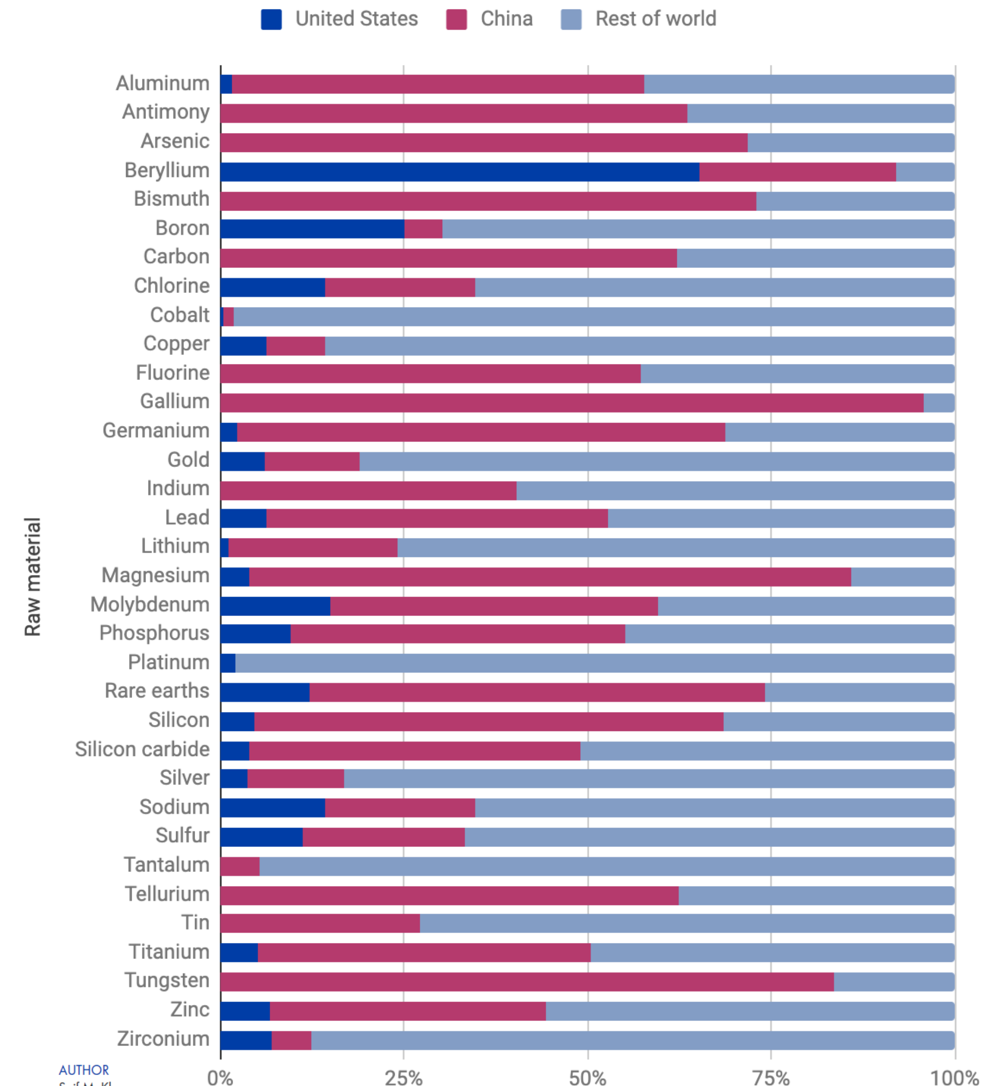
More and more materials are being introduced in microchips to continue trend towards high density & performance. About 2/3 of the periodic Table is in the chips.

Heterogeneous integration of new materials augmenting Si electronics is happening.

New materials/devices have to be capable of process integration with lab to fab realizations. High pitch patterned depositions on large area. Process compatibilty, defect free & resilience required.

Supply chain of materials/processes will be a critical issue.

2019 primary production of raw materials by country/region



AUTHOR
Saif M. Khan
Alexander Mann
Dahlia Peterson

Source: USGS

CSET
CENTER *for* SECURITY *and* EMERGING TECHNOLOGY

Q&A