Computer Organization and Architecture

Class: SEIT AY: 2018-19 (Sem-1)

MCQ's on Unit-1 Computer Evolution, Performance Measurement & Arithmetic

Subject Incharge: Ms. Y.K.Desai

* indicates questions for reference only & not included in syllabus

Sr.No.	Question	Option a	b	c	d
1	First electronic computer was constructed using_____	Vaccum tubes	Transistors	IC's	VLSI
2	the first computer constructed using vaccum tubes was	EDVAC	ENIAC	EDIAC	None of these
3	Weight of ENIAC is _____ tons	20	40	10	30
4	_____ contains more than _____ vaccum tubes	EDVAC, 17600	EDVAC, 18000	ENIAC,18000	ENIAC,17600
5	Which one was is the decimal machine	EDVAC	ENIAC	EDIAC	None of these
6	what is the capacity of addition of ENIAC machine	2000 additions/sec	3000 additions/sec	4000 additions/sec	5000 additions/sec
7	_____ stores program & data in separate memory	EDVAC	ENIAC	EDIAC	None of these
8	_____ stores program & data in same memory	EDVAC	ENIAC	EDIAC	None of these
9	Capacity of fast memory of EDVAC is _____	1000K	1012K	1024K	1042K
10	Capacity of slow memory of EDVAC is _____	10	20	30	40
11	Second generation of computers based on	Vaccum tubes	Transistors	IC's	VLSI
12	Third generation of computers based on	Vaccum tubes	Transistors	IC's	VLSI
13	the computers after third generation based on	Vaccum tubes	Transistors	IC's	VLSI
14	How many types of architectures are available, for designing a device that is able to work on its own?	3	2	1	4
15	Which architecture is followed by general purpose microprocessors?	Harvard architectur	umann archi	None of the	All of the above
16	Which architecture involves both the volatile and the n	Harvard architecture	umann archi	None of the mentioned	All of the above
17	Which architecture provides separate buses for progra	Harvard architecture	umann archi	None of the mentioned	All of the above

18	*Which microcontroller doesn't match with its architec	Microchip PIC- Harvard	MSP430- Harvard	ARM7- Von Neumann	ARM9- Harvard
19	Harvard architecture allows:	ogram and d	Piprlining	complex architectur e	all of the mentioned
20	*Which out of the following supports Harvard architecture?	ARM7	Pentium	SHARC	all of the mentioned
21	*Why most of the DSPs use Harvard architecture?	ide greater b	they provide more predictable bandwidth	they provide greater bandwidth & also more predictable bandwidth	none of the mentioned
22	Which of the architecture saves memory?	Harvard	Von Neumann	Harvard & Von Neumann	None of the mentioned
23	PC is madeto point _____ instruction of the program	first	second	next	all
24	CPU fetctes the instruction pointed by____	MR	MAR	MBR	PC
25	CPU interacts with memory through	MAR,MBR	MAR, DR	MBR, DR	All of these
26	MAR provides	address of memory location	data at memory location	address & data of memory location	none of these
27	DR acts as buffer storage between	cache & main memory	main memory & CPU	CPU & cache memory	none of these
28	Identify the interconnection structures	Linear	Mesh	Ring	All of these
29	Identify the interconnection structures	Star	Hypercube	Complete	All of these
30	the strcture with n nodes has _____ dedicated buses	n*(n-1)	n*(n+1)	n*(n-1)/2	n*(n+1)/2

31	Machine capability can be enhanced with	better hardware technology	Innovative architectural features	Efficient resource management	all of these
32	A program can be made efficient	with better algorithm	with better data structure	Language efficiency	all of these
33	A program can be made efficient	with better algorithm	with better data structure	Compiler technolgy	all of these
34	CPI (Cycles per instruction) depends on	machine	Program	both a & b	none of these
35	MIPS rate varies with respect to	Clock rate	Instruction count	CPI	All of the above
36	binary representation of -7 is	111	1001	1101	1011
37	Which of the following is used for binary multiplication	ring Multipli	Booth's Algorithm	Pascal's Rule	Digit-by-digit multiplication
38	One extra bit is added on the left of a binary number, in case of Binary Multiplication using Booth's Algorithm.	TRUE	FALSE		
39	Booth's Algorithm is applied on _____	decimal numbers	binary numbers	hexadecimal numbers	octal Numbers
40	If Booth's Multiplication is performed on the numbers 22*3, then what is 3 referred to as _____	accumulator	multiplicand	quotient	multiplier
41	What is the default value of accumulator in booth's multiplication of two 4-bit binary numbers?	0	1	0000	00000
42	What is the value of n in multiplication of 110* 1000?	2	3	4	0
43	What will be the value obtained after multiplication of (-2) * (-3) using Booth's Algorithm?	(-6)	6	(-2)	(-3)
44	in multiplication of -7 & -3 using booth's algorithm what is the value of accumulator after cycle 3	1110	0101	0010	0001
45	in multiplication of -7 & -3 using booth's algorithm what is the value of Q initially	0011	1101	1110	0111
46	in multiplication of -7 & -3 using booth's algorithm what is the value of Q after cycle 2	1110	0111	1011	0101

47	In Booth's algorithm when the value of Q_0Q_{-1} is 00 then	AC=AC+M	AC=AC-M	Arithmetic shift Right AC,Q,Q_{-1}	shift Right AC,Q,Q_{-1}
48	In Booth's algorithm when the value of Q_0Q_{-1} is 01then	AC=AC+M	AC=AC-M	Arithmetic shift Right AC,Q,Q_{-1}	shift Right AC,Q,Q_{-1}
49	In Booth's algorithm when the value of Q_0Q_{-1} is 10 then	AC=AC+M	AC=AC-M	Arithmetic shift Right AC,Q,Q_{-1}	shift Right AC,Q,Q_{-1}
50	*Which method/s of representation of numbers occupies a large amount of memory than others?	Sign-magnitude	1's complement	2's complement	1's & 2's complimen t
51	*Which representation is most efficient to perform arithmetic operations on the numbers?	Sign-magnitude	1's complement	2's complement	1's & 2's complimen t
52	Which method of representation has two representations for '0'?	Sign-magnitude	1's complement	2's complement	1's & 2's complimen t
53	*The processor keeps track of the results of its operations using a flags called _____	Conditional code flags	Test output flags	Type flags	None of the mentioned
54	Which architecture has higher speed?	Harvard	Von Neumann	both a & b	Noneof these
55	*What is the long form of IAS	Institute of Advance Studies	Institute of Advance Study	Institute of Automatic Studies	Noneof these
56	*Which kind of number system is used by IAS ?	Decimal	Binary	Hex	Octal
57	What is function of MAR ?	Read/write a word form memory	Specify an address of memory	Contains the 8 - bit op code	Store address of next instruction
58	What is function of MBR ?	Read/write a word form memory	Specify an address from me mory	Contains the 8 - bit op - code	Store address of next instruction
59	Which register pair holds the result of multiplication operation?	AC,MQ	MQ,AC	AC,PC	PC,AC

60	*What types of memories are used in second generation computers?	Magnetic core memories	Semiconductor memories	Optical memories	All of these
61	What types of memories are used in third generation computers?	Magnetic core memories	Semiconductor memories	Optical memories	All of these
62	Which is first microprocessor developed by Intel ?	4004	8008	8086	8080
63	Which is first general purpose microprocessor developed by Intel?	4004	8008	8086	8080
64	In Booth's algorithm, for Multiplier =1000 and Multiplicand =1100. How many number of cycles are required to get the correct multiplication result?	4	5	3	6
65	In Booth 's algorithm, for Multiplier =100 and Multiplicand =1100. How many number of cycles are required to get the correct multiplication result?	4	5	3	6
66	In Booth's algorithm, for Multiplier =10000 and Multiplicand =1100101. How much number of cycles are required to get the correct multiplication result?	4	5	3	6
67	In Booth's algorithm, for Multiplier=10000 and Multiplicand =1100101.What will be the size of A register?	4	5	3	6
68	In Booth's algorithm, for Multiplier=100 and Multiplicand=1100. What will be the size of A register?	4	5	3	6
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Answer Key

1	a	21	c	41	d
2	b	22	b	42	c
3	d	23	a	43	b
4	c	24	d	44	c
5	b	25	b	45	b
6	d	26	a	46	b
7	b	27	b	47	c
8	a	28	d	48	a
9	c	29	d	49	b
10	b	30	c	50	a (one bit used up to store the sign.)
11	b	31	d	51	c
12	c	32	d	52	a
13	d	33	d	53	a
14	b (Von neumann & harward)	34	c	54	b
15	b	35	d	55	a
16	a	36	b	56	b
17	a	37	b	57	b
18	b(MSP430 supports Von Neumann architecture.)	38	a	58	a
19	d	39	b	59	a
20	c	40	d	60	a

61	b	62	a	63	b
64	a	65	c	66	b
67	b	68	c	69	