Memory Interface

Introduction

- Simple or complex, every microprocessor-based system has a memory system.
- Almost all systems contain two main types of memory: **read-only memory** (ROM) and **random access memory** (RAM) or read/write memory.
- This chapter explains how to interface both memory types to the Intel family of microprocessors.

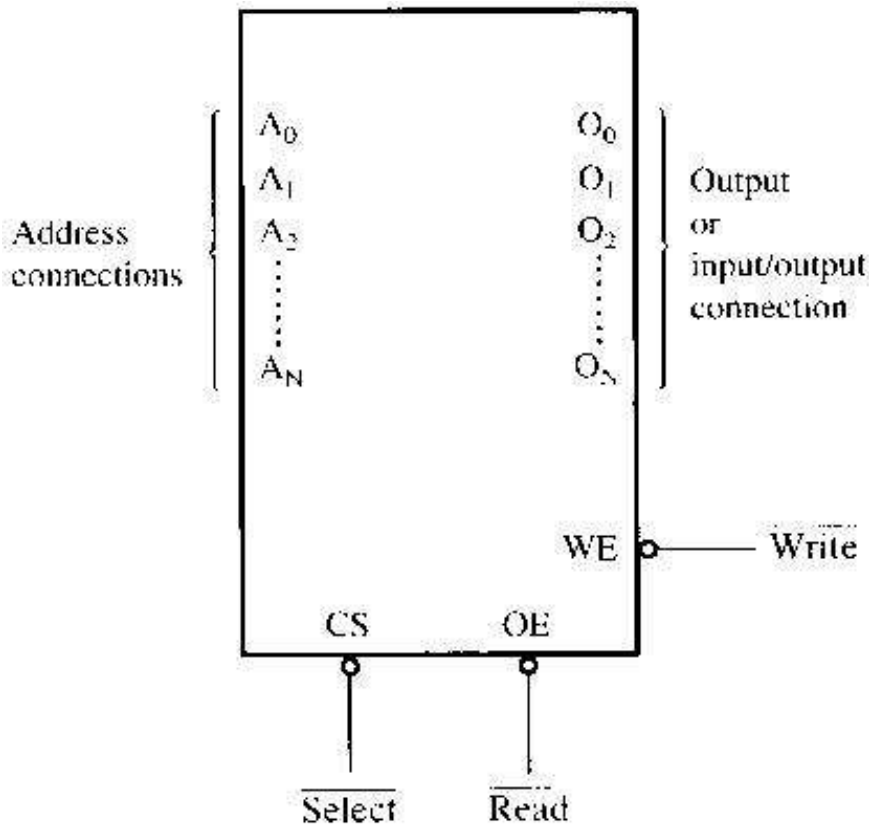
Objectives
Upon completion of this chapter, you will be able to:

- Decode the memory address and use the outputs of the decoder to select various memory components.
- Explain how to interface both RAM and ROM to a microprocessor.
- Interface memory to an 8-, 16-bit data bus.
- Interface dynamic RAM to the microprocessor.

MEMORY DEVICES

- Before attempting to interface memory to the microprocessor, it is essential to understand the operation of memory components.
- In this section, we explain functions of the four common types of memory:
  - read-only memory (ROM)
  - Static random access memory (SRAM)

Memory Pin Connections



- address inputs
- data outputs or input/outputs
- some type of selection input
- at least one control input to select a read or write operation

Figure A pseudomemory component illustrating the address, data, and control connections

Address Connections

- Memory devices have address inputs to select a memory location within the device.
- Almost always labeled from A_0, the least significant address input, to A_n
  - where subscript n can be any value
  - always labeled as one less than total number of address pins
- A memory device with 10 address pins has its address pins labeled from A_0 to A_9.
- The number of address pins on a memory device is determined by the number of memory locations found within it.
- Today, common memory devices have between 1K (1024) to 1G (1,073,741,824) memory locations.
  - with 4G and larger devices on the horizon
- A 1K memory device has ……. address pins.
  - therefore, 10 address inputs are required to select any of its 1024 memory locations
- It takes a 10-bit binary number to select any single location on a 1024-location device.
  - 1024 different combinations
  - if a device has ….. address connections, it has 2048 (2K) internal memory locations
- The number of memory locations can be extrapolated from the number of pins.

Data Connections

- All memory devices have a set of data outputs or input/outputs.
  - today, many devices have bidirectional common I/O pins
  - data connections are points at which data are entered for storage or extracted for reading
- Data pins on memory devices are labeled D_0 through D_7 for an 8-bit-wide memory device.
- An 8-bit-wide memory device is often called a **byte-wide** memory.
  - most devices are currently 8 bits wide,
  - some are 16 bits, 4 bits, or just 1 bit wide
- Catalog listings of memory devices often refer to memory locations times bits per location.
  - a memory device with 1K memory locations and 8 bits in each location is often listed as a 1K × 8 by the manufacturer
- Memory devices are often classified according to total bit capacity.

Selection Connections

- Each memory device has an input that selects or enables the memory device.
  - sometimes more than one
- This type of input is most often called a **chip select** (G2A) **chip enable** (CE) or simply **select** (S) input.
- RAM memory generally has at least one or input, and ROM has at least one
- If more than one CE connection is present, all must be activated to read or write data.

Control Connections

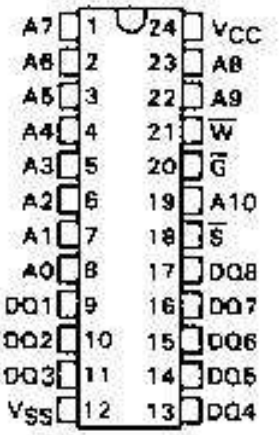
- All memory devices have some form of control input or inputs.
  - ROM usually has one control input, while RAM often has one or two control inputs
- Control input often found on ROM is the **output enable** or **gate** connection, which allows data flow from output data pins.
- The OE connection enables and disables a set of three-state buffers located in the device and must be active to read data.
- RAM has either one or two control inputs.
  - if one control input, it is often called R/W
- If the RAM has two control inputs, they are usually labeled WE (or W), and OE (or G).
  - **write enable** must be active to perform memory write, and OE active to perform a memory read
  - when the two controls are present, they must never both be active at the same time
- If both inputs are inactive, data are neither written nor read.
  - the connections are at their high-impedance state

ROM Memory

- **Read-only memory (ROM) permanently stores programs/data resident to the system.**
  - **and must not change when power disconnected**
- **Often called nonvolatile memory, because its contents *do not* change even if power is disconnected.**
- **A device we call a ROM is purchased in mass quantities from a manufacturer.**
  - **programmed during fabrication at the factory**
- **The EPROM (erasable programmable read-only memory) is commonly used when software must be changed often.**
  - **or when low demand makes ROM uneconomical**
  - **for ROM to be practical at least 10,000 devices must be sold to recoup factory charges**
- **An EPROM is programmed in the field on a device called an EPROM programmer.**
- **Also erasable if exposed to high-intensity ultraviolet light.**
  - **depending on the type of EPROM**
- **PROM memory devices are also available, although they are not as common today.**
- **The PROM (programmable read-only memory) is also programmed in the field by burning open tiny NI-chrome or silicon oxide fuses.**
- **Once it is programmed, it cannot be erased.**
- **A newer type of read-mostly memory (RMM) is called the flash memory.**
  - **also often called an EEPROM (electrically erasable programmable ROM)**
  - **EAROM (electrically alterable ROM)**
  - **or a NOVRAM (nonvolatile RAM)**
- **Electrically erasable in the system, but they require more time to erase than normal RAM.**
- **The flash memory device is used to store setup information for systems such as the video card in the computer.**

- **Flash has all but replaced the EPROM in most computer systems for the BIOS.**
  - **some systems contain a password stored in the flash memory device**
- **Flash memory has its biggest impact in memory cards for digital cameras and memory in MP3 audio players.**
- **Figure 10–2 illustrates the 2716 EPROM, which is representative of most common EPROMs.**

TMS4016 . . . NL PACKAGE
(TOP VIEW)



- One important piece of information provided by the timing diagram and data sheet is the memory access time
- that is the time it takes the memory to read information

PIN NOMENCLATURE	
A0 – A10	Addresses
DQ1 – DQ8	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{S}$	Chip Select
V_{CC}	+5 V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

Static RAM (SRAM) Devices

- Static RAM memory devices retain data for as long as DC power is applied.
- Because no special action is required to retain data, these devices are called **static memory**.
  - also called **volatile memory** because they will not retain data without power
- The main difference between ROM and RAM is that RAM is written under normal operation, whereas ROM is programmed outside the computer and normally is only read.

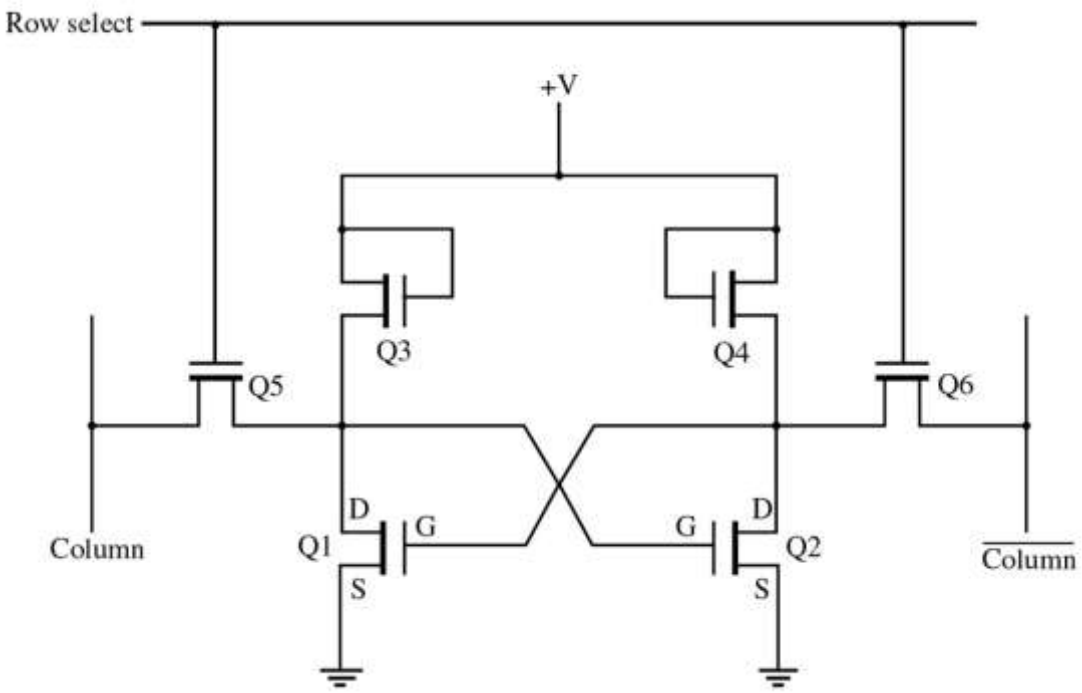
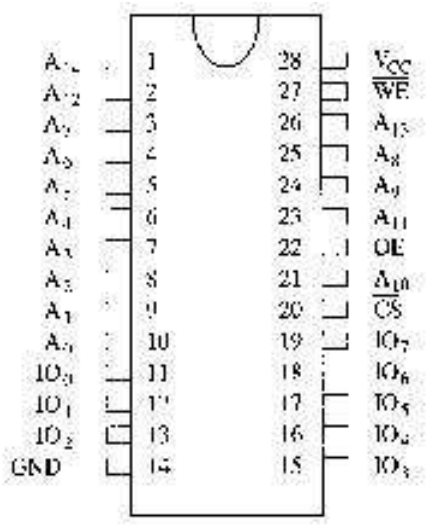
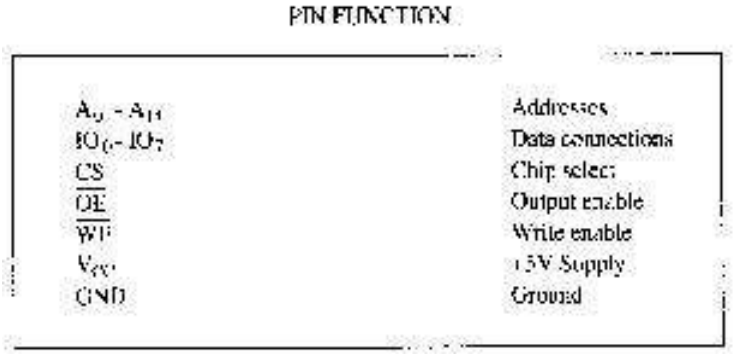


FIGURE 7-8 Basic six-transistor static memory cell. (From J. Uffenbeck, Microcomputers and Microprocessors: The 8080, 8085, and Z-80. Prentice Hall, Englewood Cliffs, NJ, 1991.)

- Fig 10–4 illustrates the 4016 SRAM,
  - a 2K × 8 read/write memory
- This device is representative of all SRAM devices.
  - except for the number of address and data connections.
- The control inputs of this RAM are slightly different from those presented earlier.
  - however the control pins function exactly the same as those outlined previously
- Found under part numbers 2016 and 6116.





- SRAM is used when the size of the read/write memory is relatively small
- today, a small memory is less than 1M byte

Figure 10–4 The pin-out of the TMS4016, 2K × 8 static RAM (SRAM). (Courtesy of Texas Instruments Incorporated.)

Dynamic RAM (DRAM) Memory

- Available up to 256M × 8 (2G bits).
- DRAM is essentially the same as SRAM, except that it retains data for only 2 or 4 ms on an integrated capacitor.

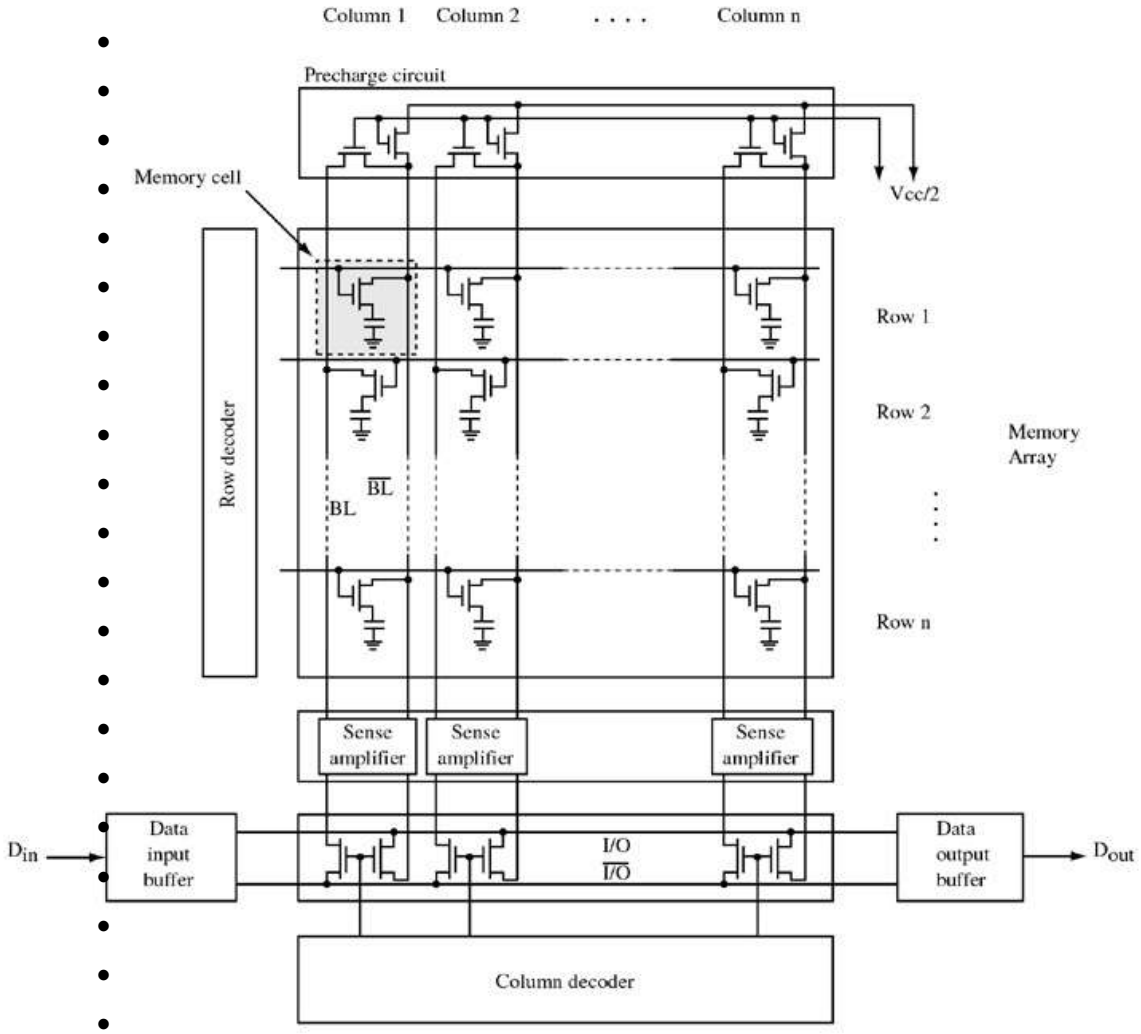


FIGURE 7-9 Dynamic RAMs use an MOS transistor and capacitor as the basic storage cell. Particular cells are selected via a row and column address.

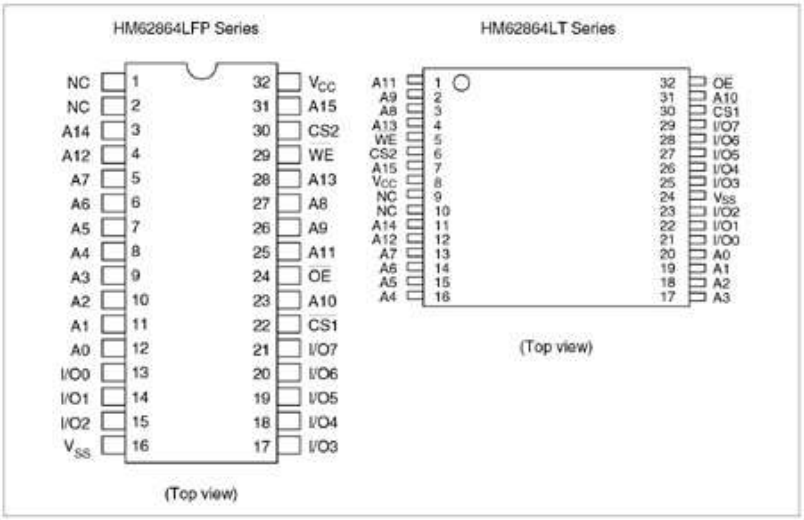
-
- After 2 or 4 ms, the contents of the DRAM must be completely rewritten *(refreshed)*.
  - because the capacitors, which store a logic 1 or logic 0, lose their charges
- In DRAM, the entire contents are refreshed with 256 reads in a 2- or 4-ms interval.
  - also occurs during a write, a read, or during a special refresh cycle
- DRAM requires so many address pins that manufacturers multiplexed address inputs.
- Figure 10–7 illustrates a 64K × 4 DRAM, the TMS4464, which stores 256K bits of data.
  - note it contains only eight address inputs where it should contain 16—the number required to address 64K memory locations

SRAM Interface Examples

To interface means to connect in a compatible manner. When interfacing memory, all the three system buses – the address, control and data buses – are involved.

Interfacing the HM62864

Pin Arrangement



Pin Description

Pin Name	Function
A0 to A15	Address
I/O0 to I/O7	Input/output
CS1	Chip select 1
CS2	Chip select 2
WE	Write enable
OE	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Function Table

CS1	CS2	OE	WE	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
X	L	X	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	H	H	Output disable	I_{CC}	High-Z	—
L	H	L	H	Read	I_{CC}	Dout	Read cycle (1) to (3)
L	H	H	L	Write	I_{CC}	Din	Write cycle (1)
L	H	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: X: High or Low

FIGURE Specifications for the HM62864 64K x 8 SRAM.

Interfacing the 8088 procesor

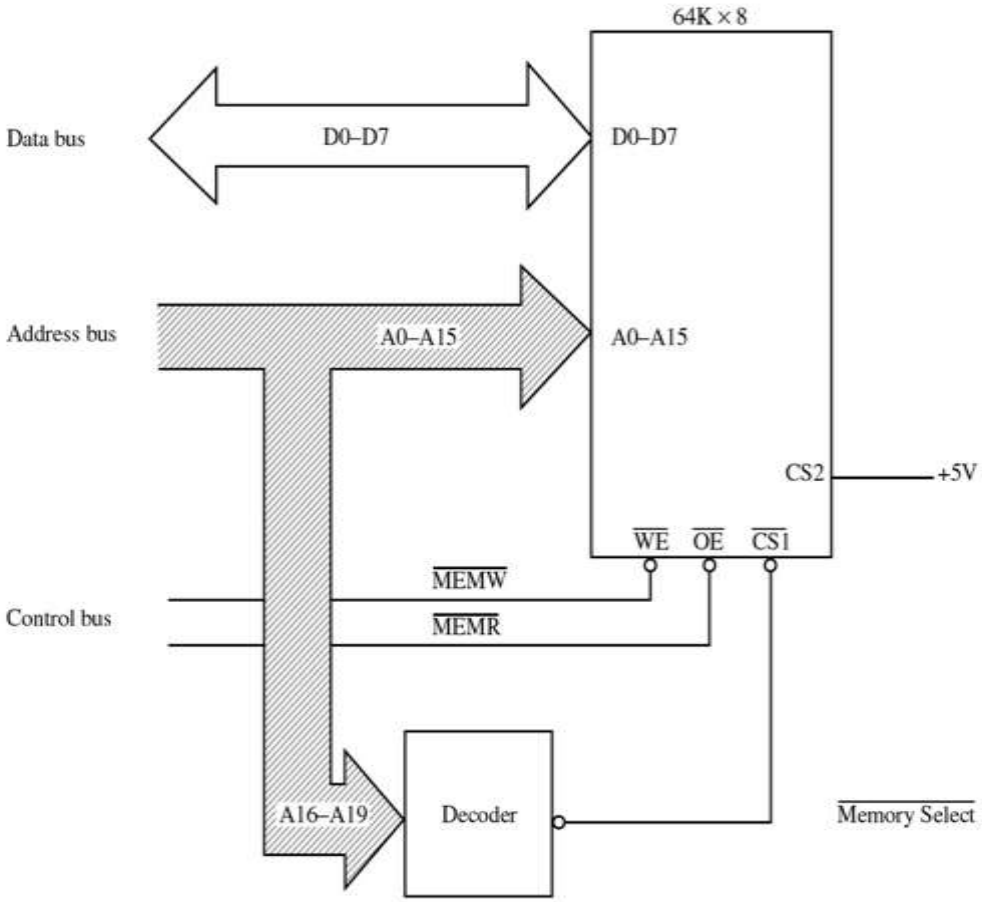


FIGURE 64K x 8 8088 SRAM interface. Only a single memory chip is required.

ADDRESS DECODING

- In order to attach a memory device to the microprocessor, it is necessary to decode the address sent from the microprocessor.
- Decoding makes the memory function at a unique section or partition of the memory map.
- Without an address decoder, only one memory device can be connected to a microprocessor, which would make it virtually useless.

Why Decode Memory?

- The 8088 has 20 address connections and the **HM62864** has 16 connections.
- The 8088 sends out a 20-bit memory address whenever it reads or writes data.
  - because the **HM62864** has only 16 address pins, there is a mismatch that must be corrected
- The decoder corrects the mismatch by decoding address pins that do not connect to the memory component.

Simple NAND Gate Decoder

- When the 64K × 8 SRAM is used, address connections A_{15}–A_0 of 8088 are connected to address inputs A_{15}–A_0 of the SRAM.
  - the remaining four address pins (A_{19}–A_{16}) are connected to a NAND gate decoder
- The decoder selects the SRAM from one of the 64K-byte sections of the 1M-byte memory system in the 8088 microprocessor.
- In this circuit a NAND gate decodes the memory address, as seen in the following figure.
- If the 20-bit binary address, decoded by the NAND gate, is written so that the leftmost nine bits are 1s and the rightmost 11 bits are don’t cares (X), the actual address range of the SRAM can be determined.

  - a *don't care* is a logic 1 or a logic 0, whichever is appropriate
- Because of the excessive cost of the NAND gate decoder and inverters often required, this option requires an alternate be found.

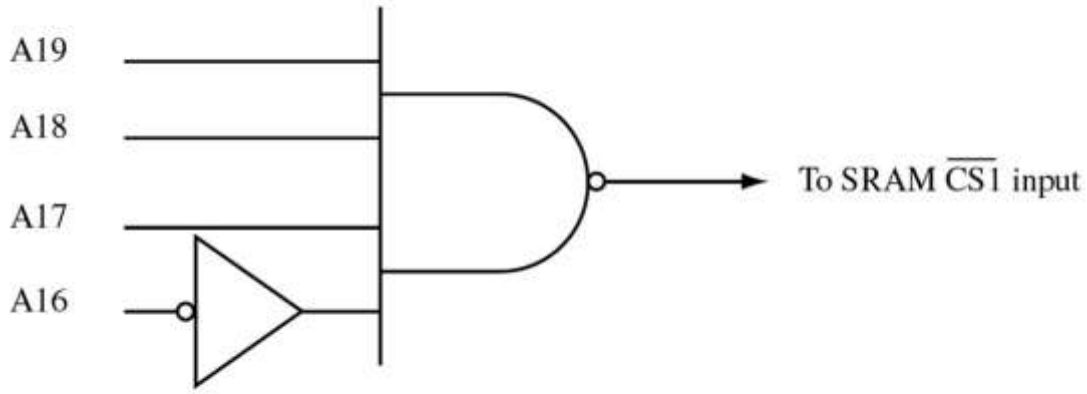


FIGURE Example of an address decoder for the 8088 memory interface in previous figure. The memory will be enabled only when A19-A16 = 1110.

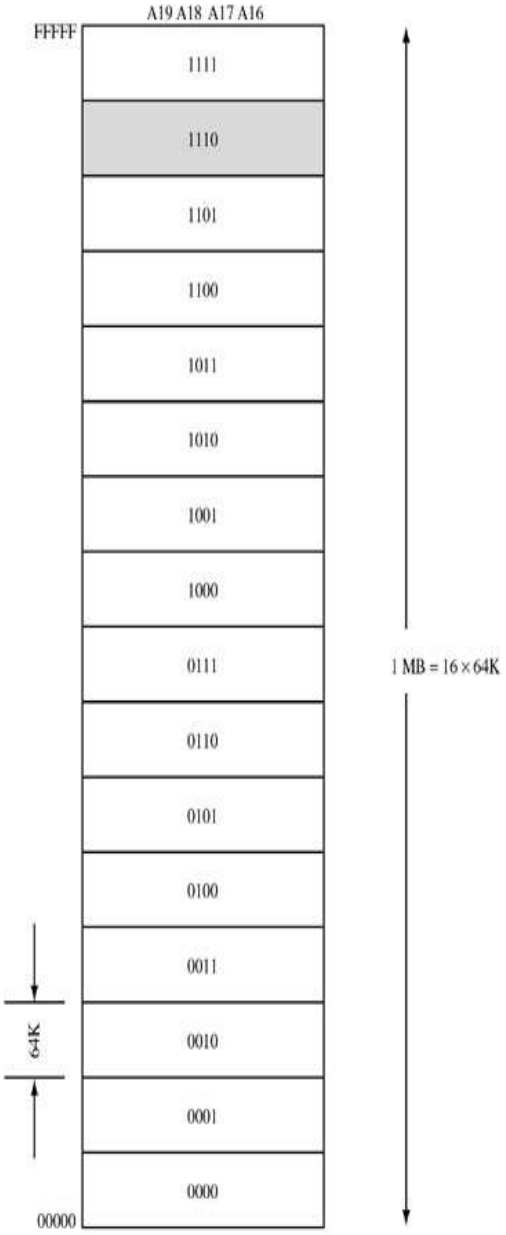


FIGURE Memory map for the 8088 interface and decoder. The 64K SRAM is mapped to the address range E0000H to EFFFFH.

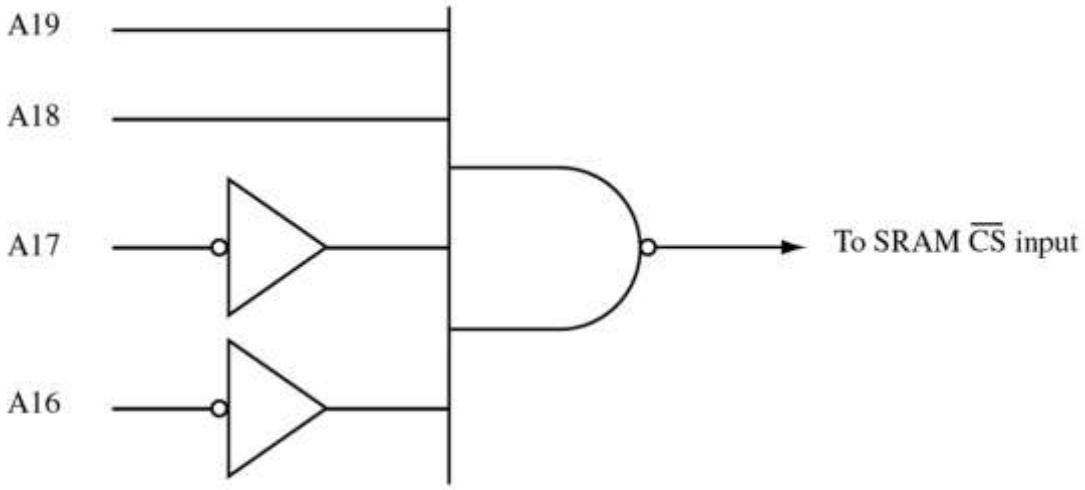


FIGURE Decoder to map the SRAM to the range C0000-CFFFFH.

Interface between memory and 8086

Even and Odd Memory Banks
Two SRAMs are needed. One stores the even bytes and connects to D_0-D_7, the other stores the odd bytes and connects to D_8-D_{15} .

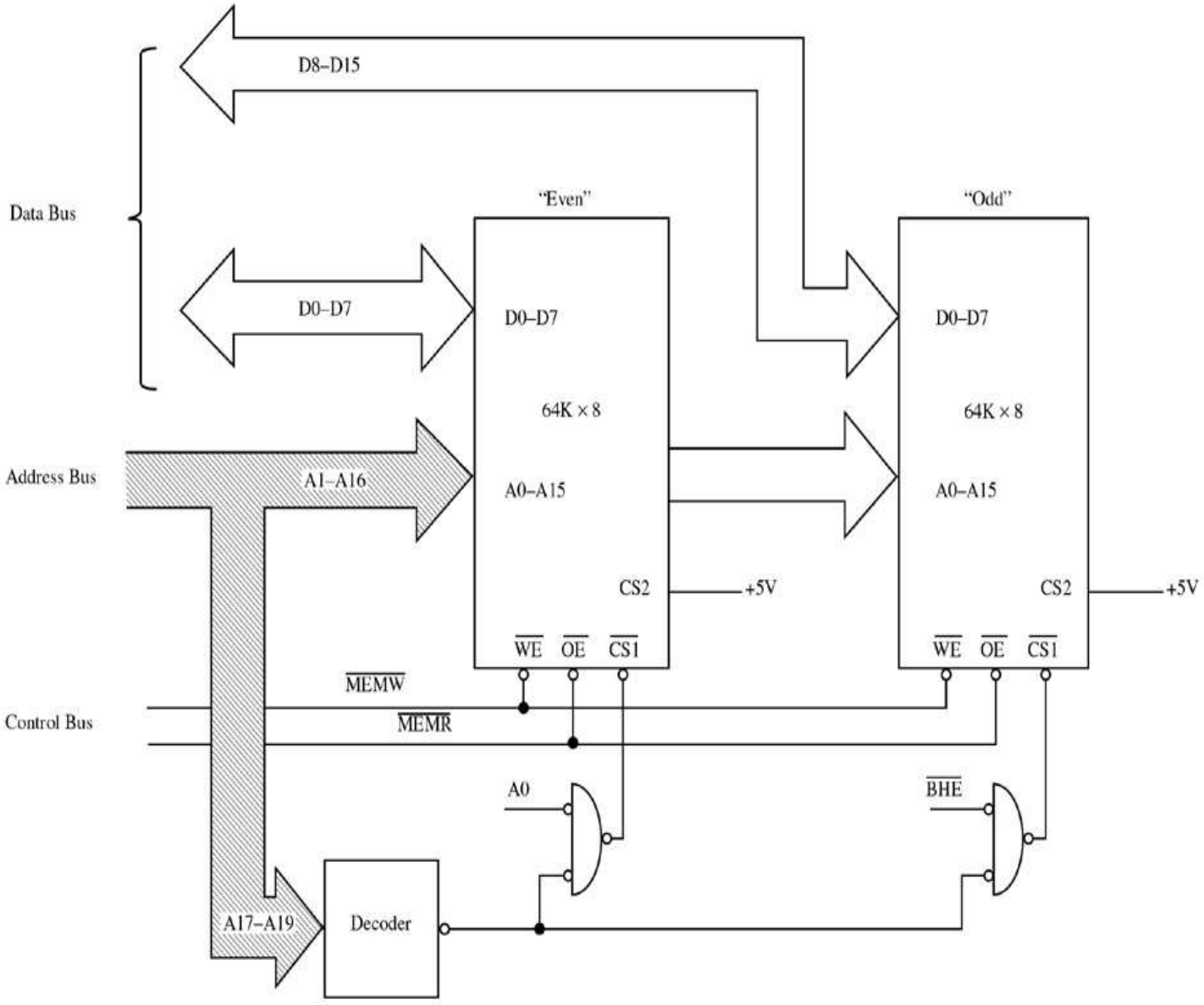


FIGURE 128K x 8 8086 SRAM interface.

The 3-to-8 Line Decoder (74LS138)

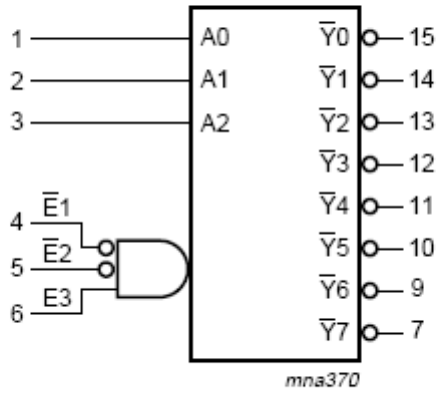


Fig 1. Logic symbol

Table 3. Function table [1]

Input						Output							
$\overline{E}1$	$\overline{E}2$	E3	A0	A1	A2	$\overline{Y}0$	$\overline{Y}1$	$\overline{Y}2$	$\overline{Y}3$	$\overline{Y}4$	$\overline{Y}5$	$\overline{Y}6$	$\overline{Y}7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

Figure The 74LS138 3-to-8 line decoder and function table.

Sample Decoder Circuit

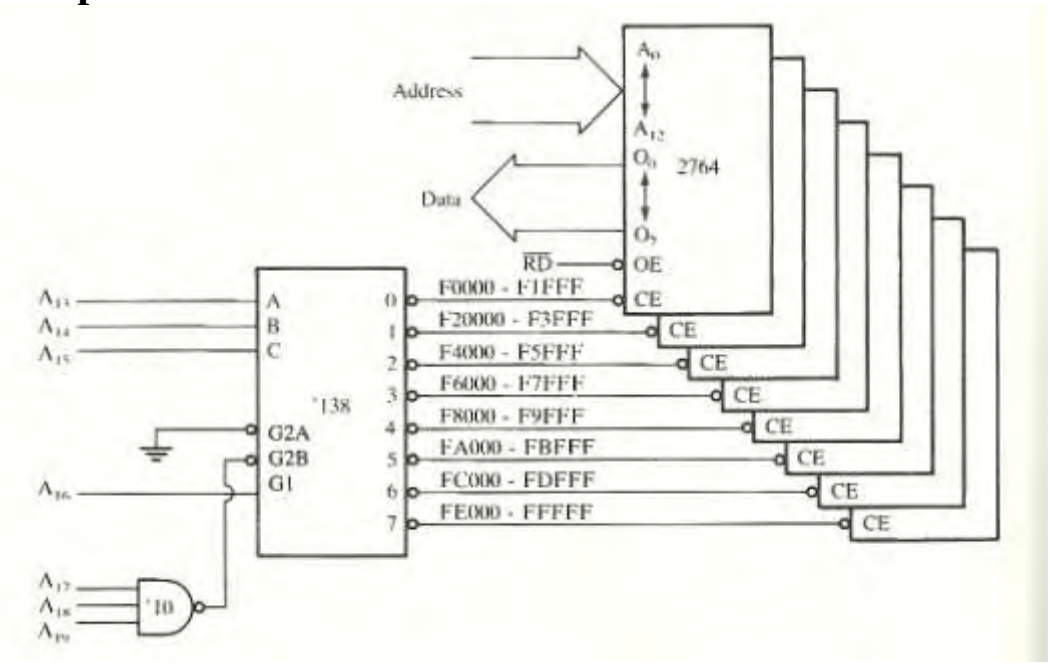
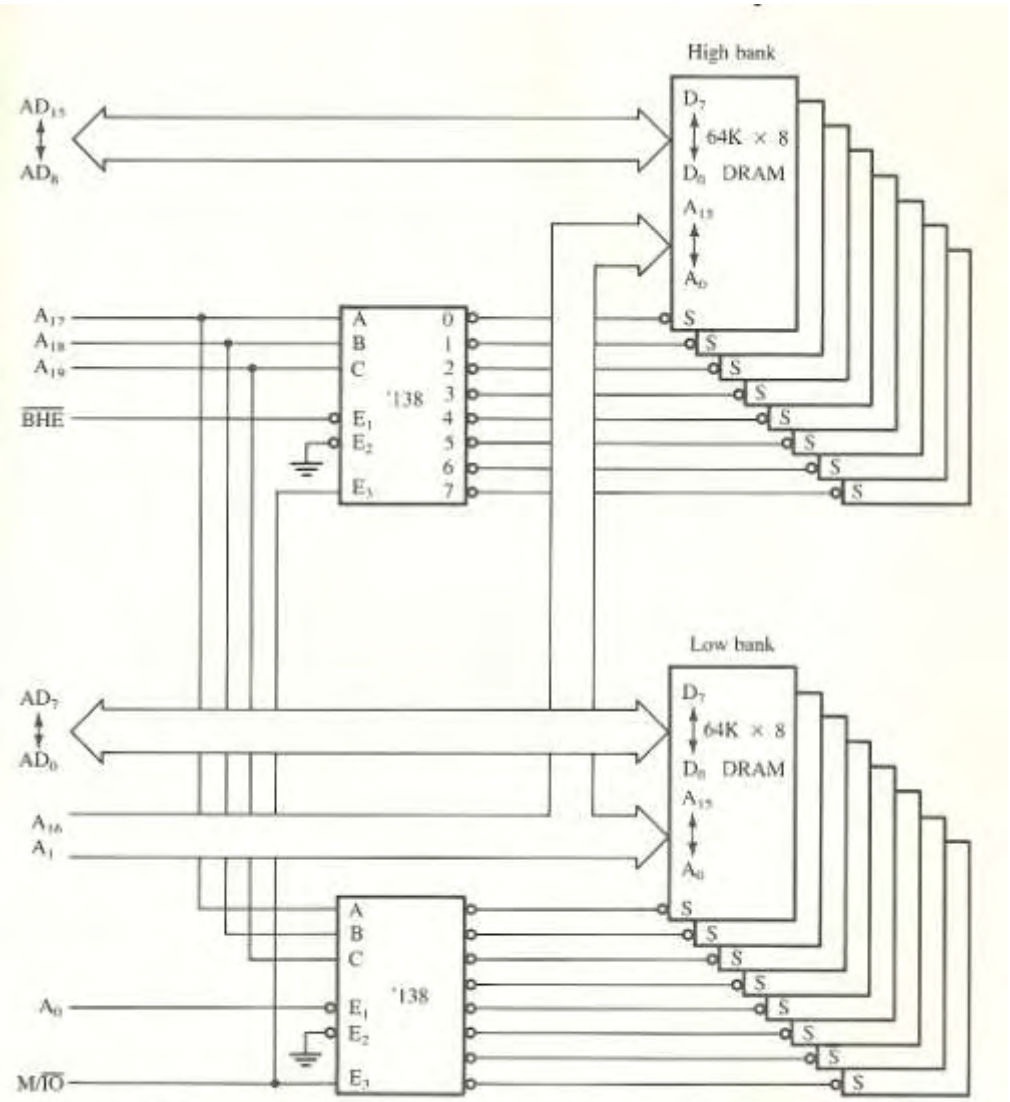


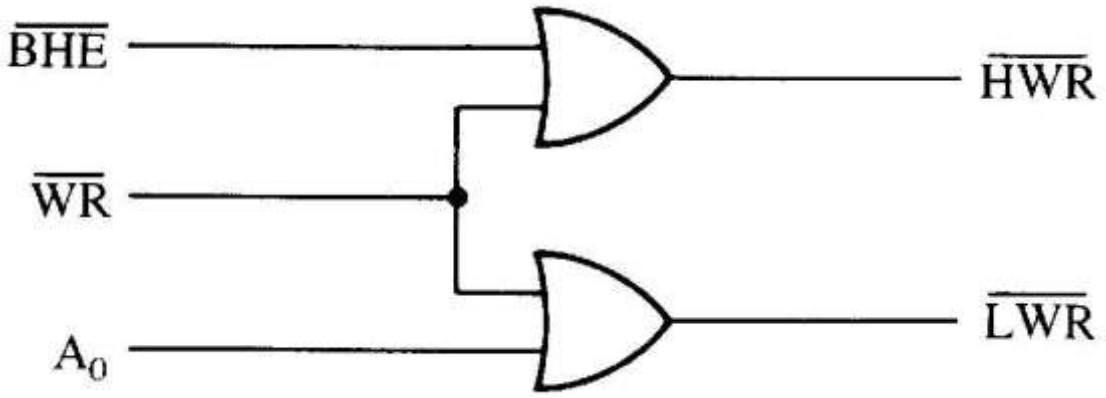
Figure A circuit that uses eight 2764 EPROMs for a 8K × 8 section of memory in an 8088 microprocessor-based system. The addresses selected in this circuit are F0000H–FFFFFH

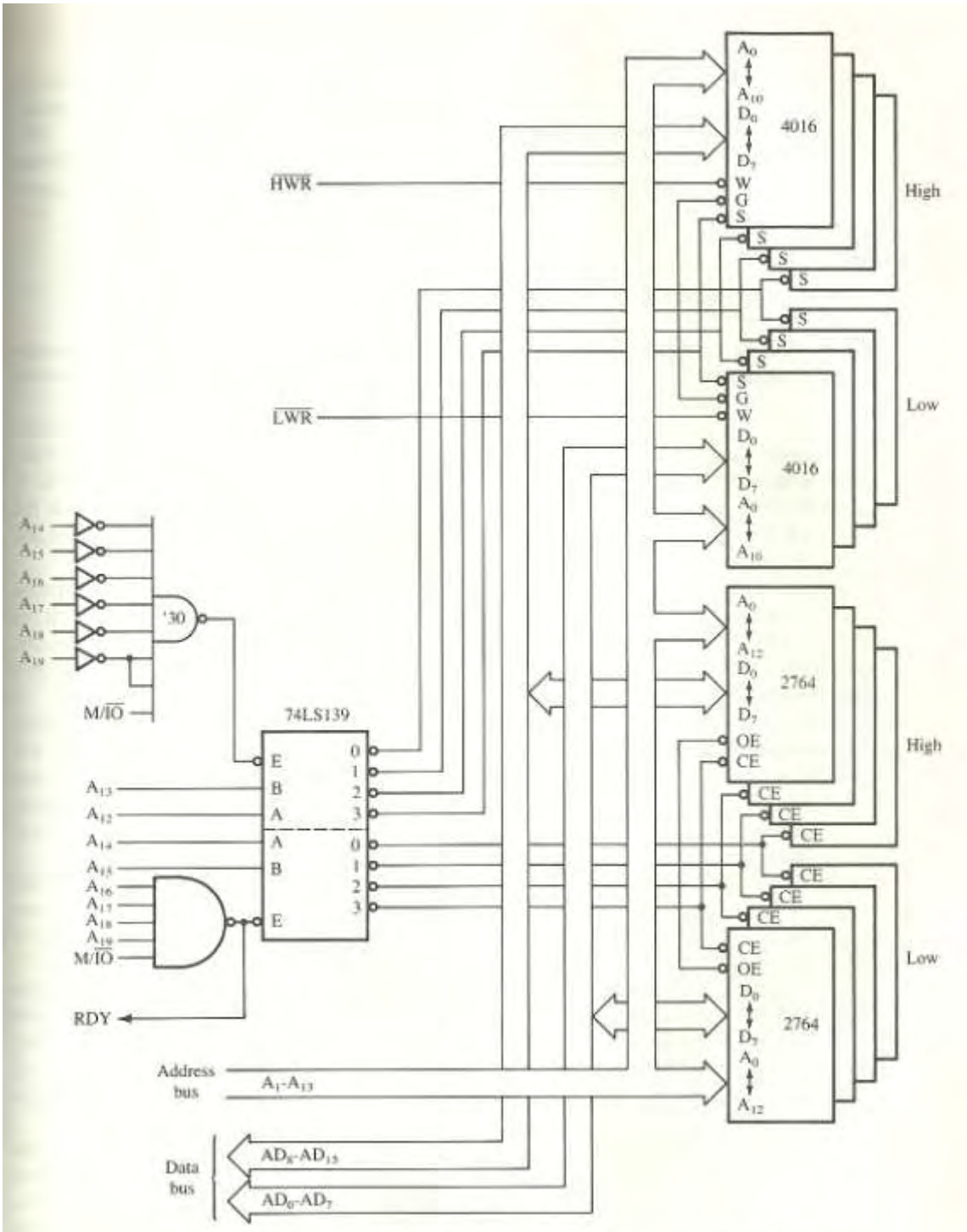
- The outputs of the decoder in the figure, are connected to eight different 2764 EPROM memory devices.
- The decoder selects eight 8K-byte blocks of memory for a total capacity of 64K bytes.
- This figure also illustrates the address range of each memory device and the common connections to the memory devices.
    - all address connections from the 8088 are connected to this circuit.
    - the decoder's outputs are connected to the CE inputs of the EPROMs,
    - the RD signal from the 8088 is connected to the OE inputs of the EPROMs
- In this circuit, a three-input NAND gate is connected to address bits A_{19}–A_{17}.
- When all three address inputs are high, the output of this NAND gate goes low and enables input G2B of the 74LS138.
- Input G1 is connected directly to A_{16}.
- In order to enable this decoder, the first four address connections (A_{19}–A_{16}) must all be high.
- Address inputs C, B, and A connect to microprocessor address pins A_{15}–A_{13}.
- These three address inputs determine which output pin goes low and which EPROM is selected whenever 8088 outputs a memory address within this range to the memory system.



An 8086 1 M byte memory interface. Note that no attempt is made to illustrate $\overline{RD}$, $\overline{WR}$, and the DRAM selection inputs.

Figure Separate bank decoders.





The 8086 interfaced to a 32 K × EPROM (F0000H–FFFFFH) and an 8 K × 16 SRAM (00000H–03FFFH).

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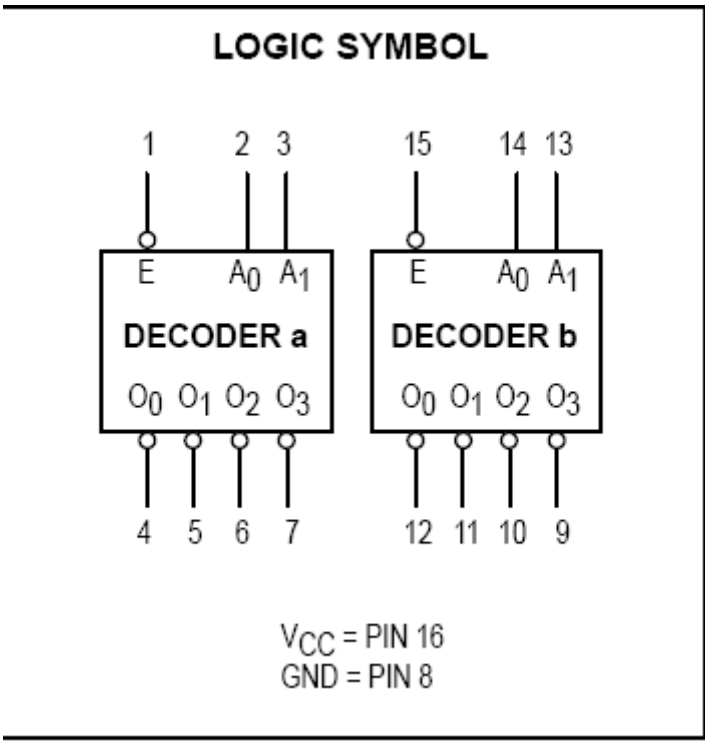
The Dual 2-to-4 Line Decoder (74LS139)

- Figure illustrates both the pin-out and the truth table for the 74LS139 dual 2-to-4 line decoder.
- 74LS139 contains two separate 2-to-4 line decoders—each with its own address, enable, and output connections.
- A more complicated decoder using the 74LS139 decoder appears in the figure.



TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O_0}$	$\overline{O_1}$	$\overline{O_2}$	$\overline{O_3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care