

矽晶源高科股份有限公司 SCS Hightech Inc.

MEMS Solution for Semiconductor Probing

South-Western Testing Workshop Presentation

Presented by Dr. Howard Hsu 06-06-2005

Presentation Overview

Introduction

- Device Geometry vs. IC Characteristics
- Device Geometry vs. Pad Layout Rule and Package Technology
- Classical Probing Technology is Insufficient at These Circumstances
- Mechanical Probing Has Shown Productivity Degradation in Volume Production
- MEMS VPC Solution

Probing Mechanism Comparison – Classical vs. MEMS

- Structural Differences
- Material Combination & Technology Development
- Mechanism Practices
- Performance Comparison

Development Challenges & Solutions for MEMS Probing

- Test, Assembly, and Operation
- Reliability
- IC Concerns

MEMS Probing Technology Roadmap

- Compliant Probing Structure
- Tighter Control of Electrical Connection

MEMS Solution for Semiconductor Probing

Introduction

Introduction Device Geometry vs. IC Characteristics

	2003-2005	Remarks 備註	
Process Technology	Copper Process	Low Resistance & Electronic migration High conductivity & Thermal Conductivity	
製程技術	SOI Capacitor	Low power consume & voltage, Energy storage	
	Low k – dielectric ~ 2.2	Low leakage, capacitor effects, thermal conductivity, power consumption, and higher integration ability.	
	Stepper / Photo down to 0.065 um	Smaller transistor, large quantity, faster speed.	
Components 元件	Power – Increase	Number of function, I/O, power, and Vdd & Vss are	
	Speed greater than 300 MHz	increasing. Speed faster than 300 MHz, package no wire bond.	
	Number of transistors – Increase	Number of I/Os increases too fast, therefore Array Design is the major trend.	
Package 封装Flip Chip PackageMaterials, Reliability, MCM COB BBULDuferfill DevelopmentBBUL	•		
	Unferfill Development		
	Pb-Free Solder Bump		
Testing	Vertical Probe Card	I/O pins over 1000	
測試	Wafer Level Burn In	High speed test	
	KGD	Burn-in and test before package	

Device Technology is going further...

Above 0.35um	0.35um ~ 0.18um	0.18um ~ 0.13um	0.13um below
~2000	2000~2002	2002~2004	2004~

IC Pad Layout Rule is getting more and more critical...

Pad Pitch over 200um		Pad Pitch over 200u	um Pad Pitch under 100um	
Linear Bump Design	Stag	ger Bump Design	Array Bump Design	

Package Technology has to be changed in order to fit the progress..

Wire Bonding Package	Flip chip package

Introduction

Classical Probing Technology is Insufficient at These Circumstances

Array Bump Probing

- Bump pitch will need to go lower than 150um
- Maintenance free probe card
- No burning tips
- Short lead-time for order delivery
- Consistent probing; no need to re-probe
- High frequency probing

Aluminum Pad Probing

- Multiple sites
- Small pad pitch ~ 50um

Introduction

Mechanical Probing Has Shown Productivity Degradation in Volume Production

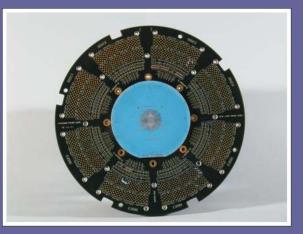


Introduction MEMS VPC Solution

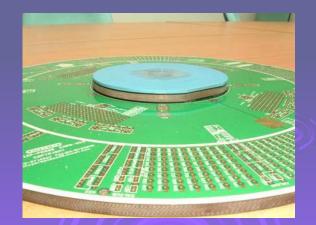
MEMS Prove Card Specifications

8 ~ 12 um
Up to 100um
0 ~ 4 inch
120um array, 35um LDI
1um
< 1.5um
1 A
100g / pin
Nickel, Copper, and Silver
2 ohm whole path
50 ohm plus minus 5 ohm
Smaller than 10nA at 5 volts
6~8 weeks (design related)
< 2 weeks

Here is the solution!!



Vertical Probe card for Aglient 93000

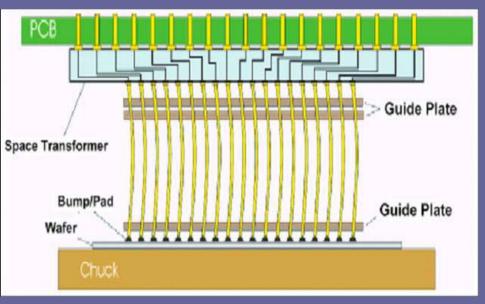


Vertical Probe Card for Cadence Type

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Probing Mechanism Comparison – Classical vs. MEMS

Probing Mechanism Comparison – Classical vs. MEMS Structure Differences

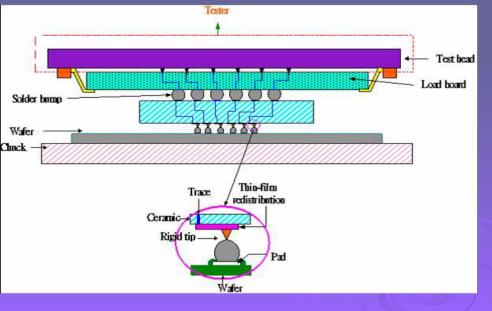


Classical Vertical Type Probe Card

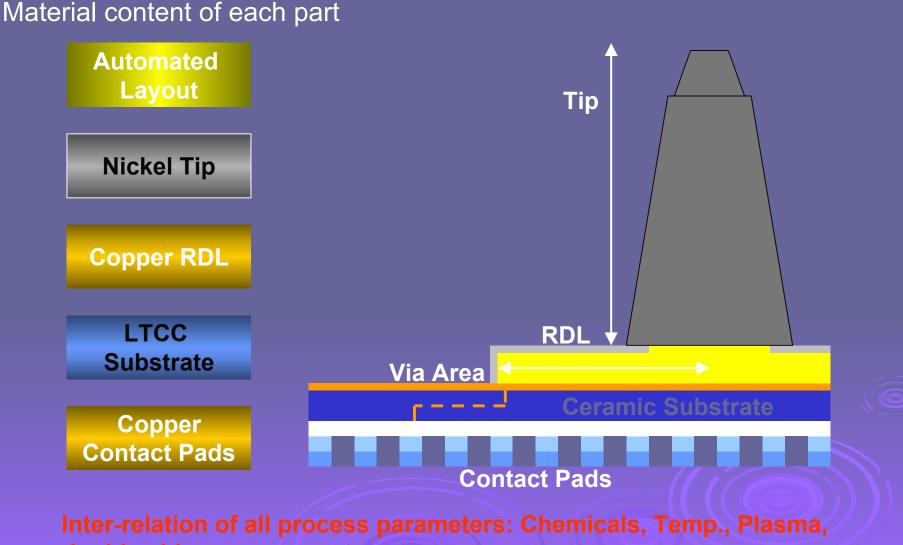
- Probing tip will deform cause open issue
- Use PCB substrate
- Need cleaning both online and offline



- Rigid tip will never deform
- Use ceramic substrate
- Excellent co-planarity w/o manual adjustment
- No cleaning, no re-probing, and no repairing



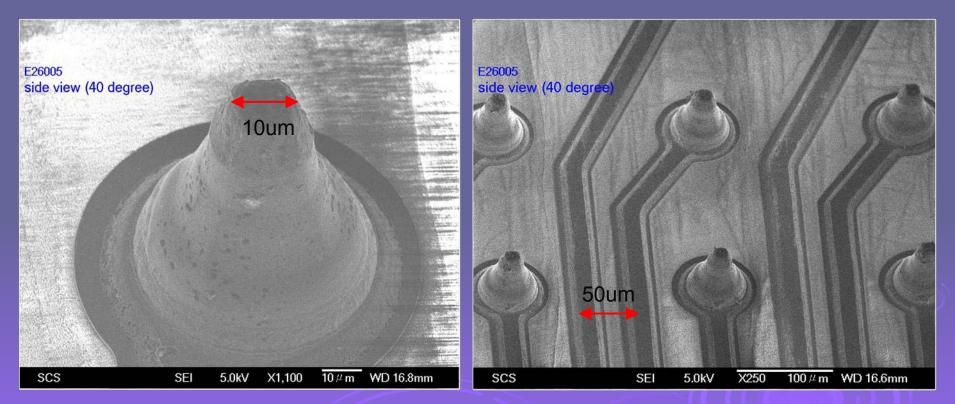
Probing Mechanism Comparison – Classical vs. MEMS Material Combination



double side process.... etc

Probing Mechanism Comparison – Classical vs. MEMS Technology Development

MEMS VPC: Use the same process to fabricate the sub-micron level rigid tips. Can be applied to small pitch ~35um multiple die sorting.

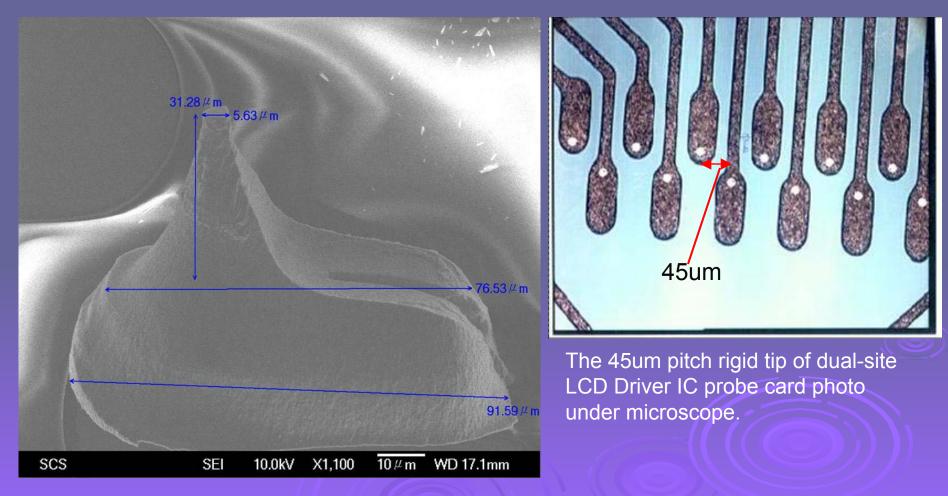


Classical VPC:

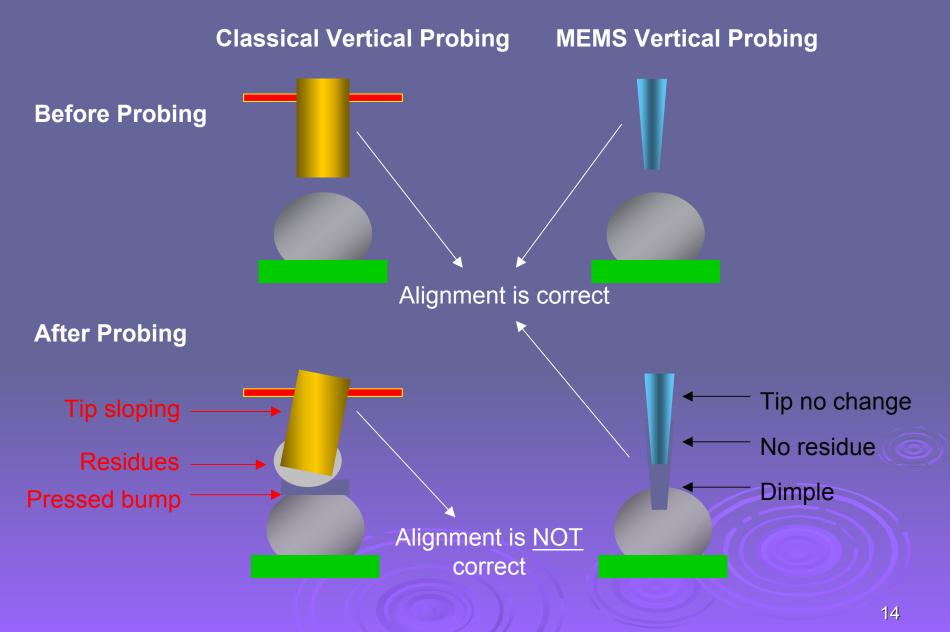
Use the mechanical technology – minimum pitch is ~150um for array VPC

Probing Mechanism Comparison – Classical vs. MEMS Technology Development

Use the same process technology to fabricate the sub-micron level rigid tips for LCD driver IC probing.



Probing Mechanism Comparison – Classical vs. MEMS Mechanism



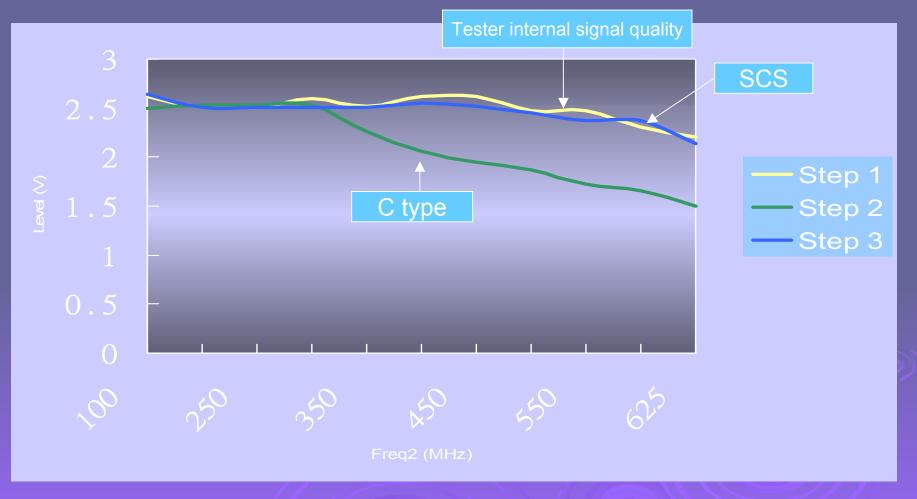
Probing Mechanism Comparison – Classical vs. MEMS Performance

	Classical C type Probe Card	SCS Diamond Vespa MEMS VPC
Pad Pitch	> 150 um	Under 120 um
Volume lead time First order	6 ~ 8 weeks	5 ~ 6 weeks
Volume lead time Repeat order	4 weeks	2 weeks
Multiple Site Probing	Depends on pad pitch	Bumped pad only for now
LDI probing	Not available (other types, such as cantilever)	Already in evaluation sample
Reprobing	Need	No need
Tip cleaning	Need, because residue	No need, nor online maintenance

Comparison Table for different probe card

Probing Mechanism Comparison – Classical vs. MEMS Performance

MEMS Vertical Probe Card : Has passed several qualifications in Taiwan. Electrical performance (up to 3GHz) is superior to classical manufactured probe cards.



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Development Challenges & Solutions For MEMS Probing

Development Challenges & Solutions For MEMS Probing

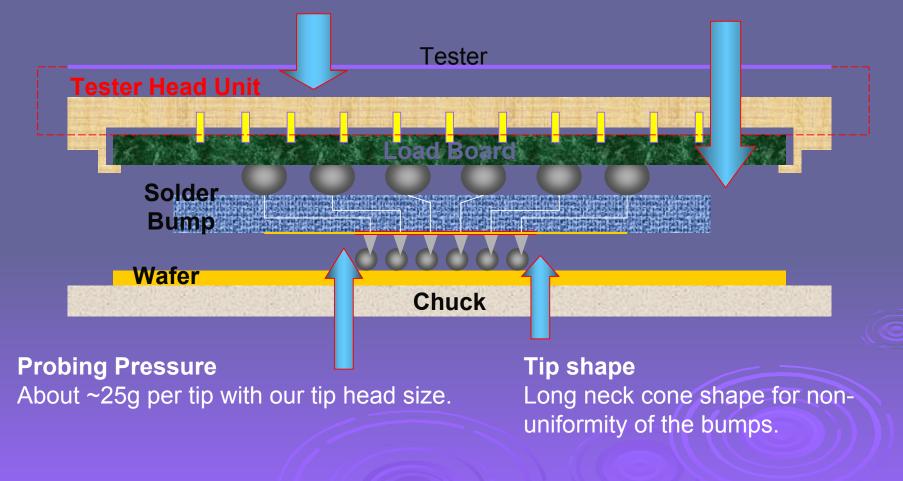
Test, Assembly, and Operation

Testing

Alignment focus issues – tip head is 10um SOP training for using MEMS probe card.

Load Board

Parallelism between PCB and LTCC Requires high stand-off.



Development Challenges & Solutions For MEMS Probing Reliability

Durability for Probing ICs

Excellent probing consistency (eliminate re-probing) Excellent probing life time – some model probed over 1.3M, other around 1M. Excellent maintenance – No need to repair anymore because lead time is short.

Subject: SCS MEMS VPC for 8" wafers(633 pins) Tester/Prober: Agilent 93000/P600, P12/TEL Clean sheet: Enhanced 3M type C (*type C + polish paper/pink type*) Tool: Olympus microscope with micro meter Reading: Check pin high twice(from ULTCC to tip) for average.



After 150K times

After 350K times







Result

- With clean process, the wear out rate is around 3~6 um after 12k ti

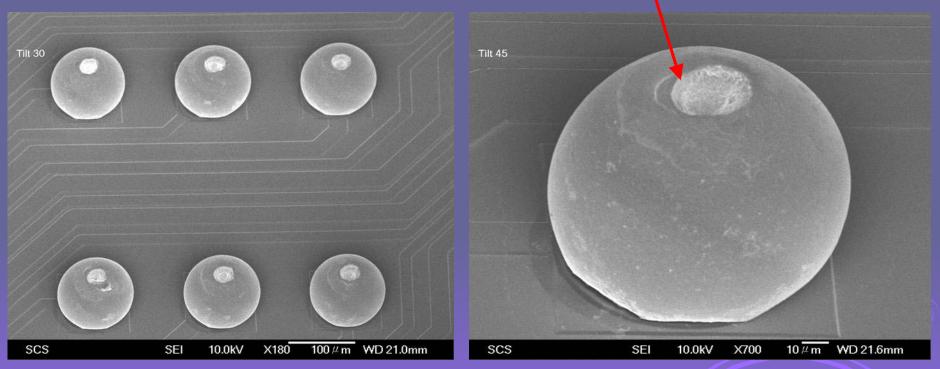
Development Challenges & Solutions For MEMS Probing IC Concerns

Rigid Tip

After the tip probes into the bump, it will produce a "dimple" that looks like a crater.

Dimple

This has been notified and IC has also been checked out with reliability qualification.



Dimple Reliability The reliability issue has been passed by a famous Taiwan foundries and packaging house.

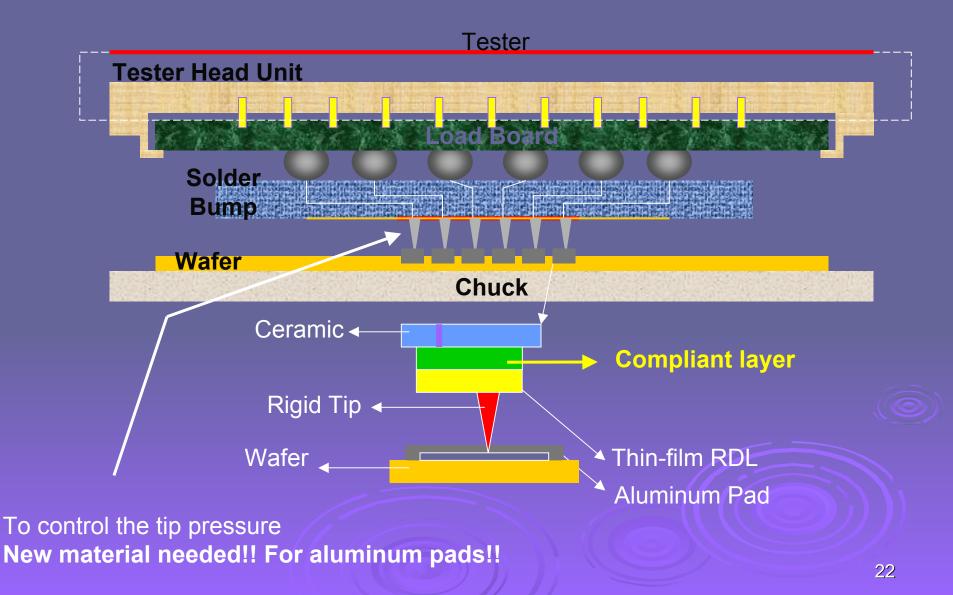
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MEMS Probing Technology Roadmap



MEMS Probing Technology Roadmap

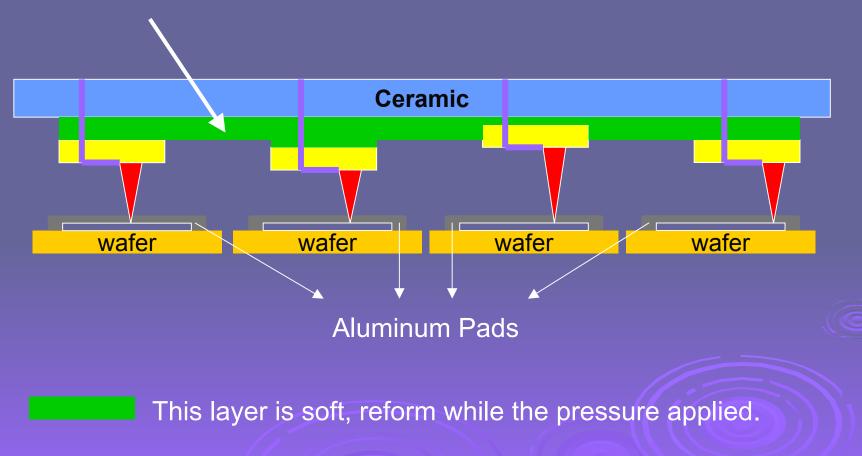
Compliant probing structure



MEMS Probing Technology Roadmap

Compliant probing structure

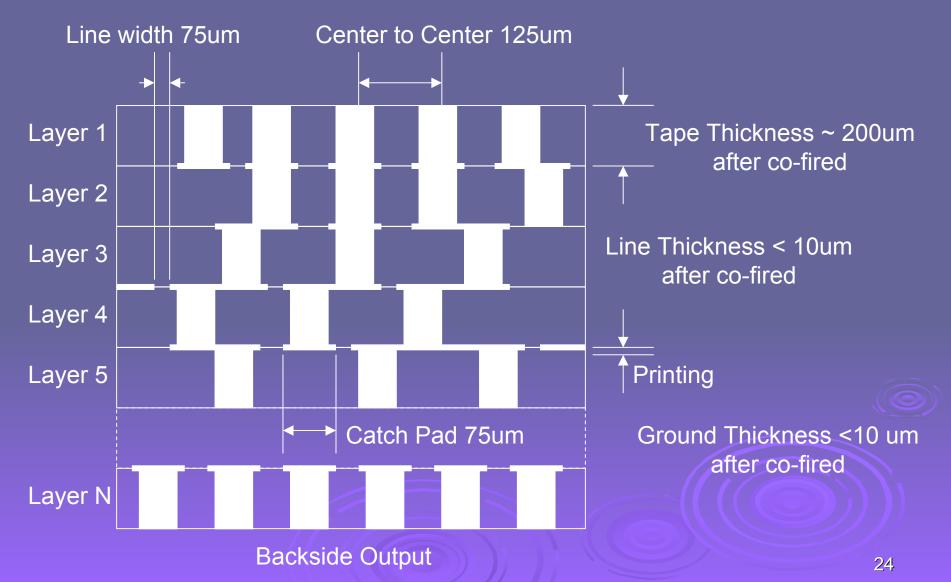
Compliant layer To provide adjustment for improving contact uniformity.



MEMS Product R&D Roadmap

Tighter Control of Electrical Connection – Ceramic Section

Improvement of the LTCC to improve the performance of the probe card



End of Presentation Q & A

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