Mentor Graphics Tools Tutorial

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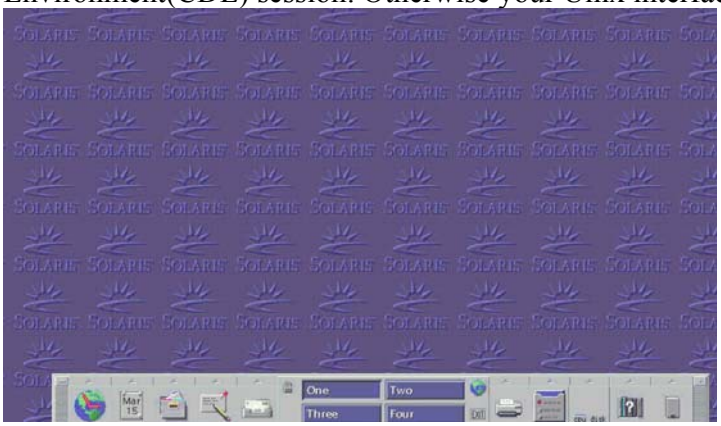
In this tutorial, we will use the following Mentor Graphics tools:
1. *Design Architect (DA)* for schematic design.
2. *Design Viewpoint Editor (DVE)* for creating design viewpoint for your circuit. You must use DVE tool to generate a viewpoint of your circuit generated in DA tool in order to be passed to the next tool (for example, Accusim simulation).
3. *ICStation* for layout design. After your layout is finished, you will use DRC check (design-rule-check) to check whether your layout has any design rule violation. You will also need to use LVS tool to verify the designed layout is consistent with your schematic design.
4. *Accusim* for analog simulation. You will need it to simulate the schematic of your circuit design.

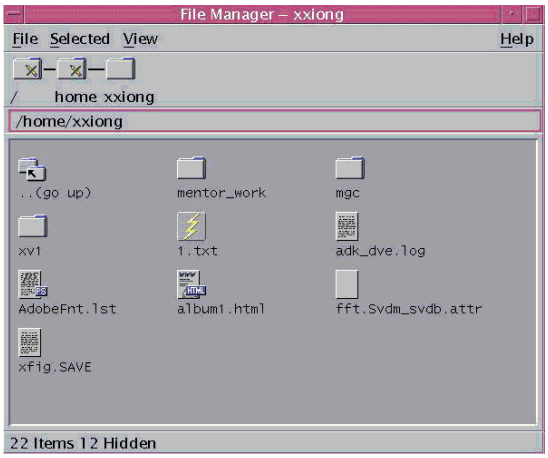
The silicon process we are going to use in all lab sessions is the C5N process by American Microsystems, Inc. (AMI). The AMI C5N is an N-Well sub-micron CMOS process. The process is for 5V VDD systems, and has 3 metal layers, 2 poly layers, and a high resistance layer. We will use only 2 metal layers (METAL1 and METAL2), and one poly. While using the process in the Mentor-Graphics tools, you will be using the Mosis Scalable-CMOS (SCMOS) design rules. The C5N process has a feature size of 0.60 micron, and uses a lambda (λ, or *L*) of 0.30 micron. In ICGraph, every minor grid is 0.5 lambda. All designs must fit into a Mosis TinyChip unit which is 1.5 mm×1.5 mm in size. Although there is no rule for a minimum channel width, Mosis and AMI recommend to use a minimum channel width of 1.8μm (which is 6 lambda for our process).

Section A. Preparing your account

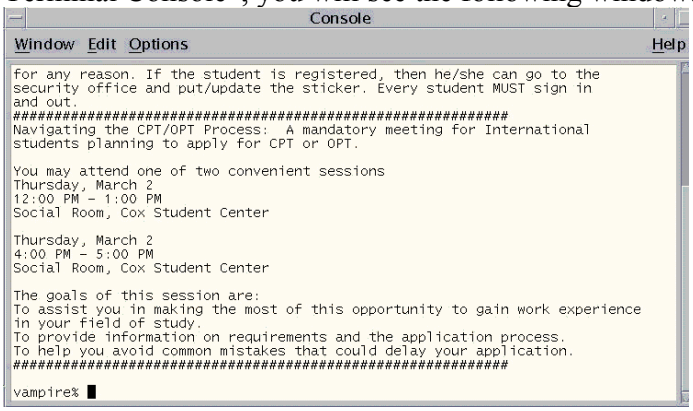
First please log into one Sun SPARC station use your UB email ID and password. In the login interface, please click "Options—Session—Common Desktop Environment(CDE)" to select Common Desktop Environment(CDE) session. Otherwise your Unix interface will be different from the following.



You need to know some basic unix commands and operations for this operation system. For example, you can right click your mouse on the desktop, in the popup menu, select "Folders—File Manager-Home", you will see the file manager window as below. It's just like Windows File Explorer. It's convenient to organize your files and folders.



Again, in the main desktop, if you right click mouse, in the popup window, click to select "Hosts—Terminal Console", you will see the following window.



This is the main prompt command input window. You can input unix commands to interact with the unix operation system. For example, you can input "ls" to display the files and subfolders in current directory, "pwd" command to display current directory, "cd *directory_name*" to enter a directory, etc.

If you are using Mentor Graphics tools the very first time, you will need to do some initial setup to use the software. In the terminal console window, please input the following command:

mentorprep

This will start a special script that will prepare your account to run Mentor-Graphics. The script should issue a "successful" message. If it didn't, ask for assistance from your Mentor TA. You should now log out and log in again to make the changes effective. After that, you would be able to use Mentor Graphics tools. Remember, you only need to do this initial setup for once. In the future, you needn't do this anymore.

Section B. Mentor Graphics Design Architect (DA) tutorial

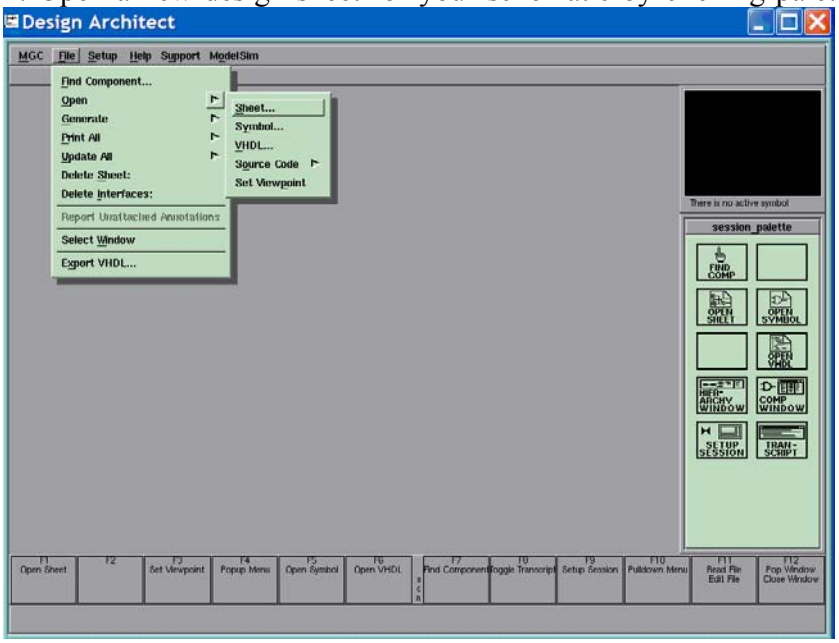
In this tutorial, we are going to use Mentor Graphics Design Architect (DA) tool to design a schematic circuit of 2-input NAND gate.

1. Log into a Mentor-capable machine. Open a terminal console window. Input the following command:

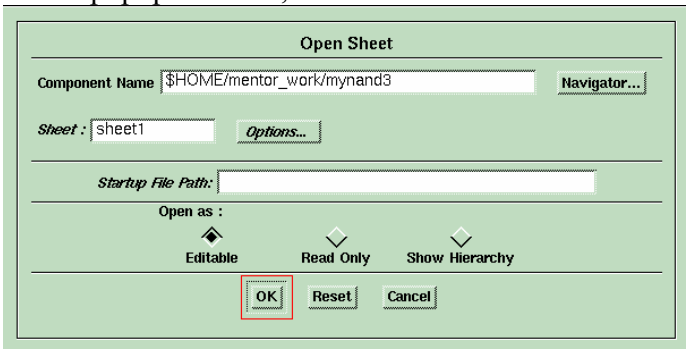
da

You will see the main interface of DA tool shows up. Resize the DA window so it will cover most of your screen.

2. Open a new design sheet for your schematic by clicking palette “session_palette—OPEN—SHEET”.



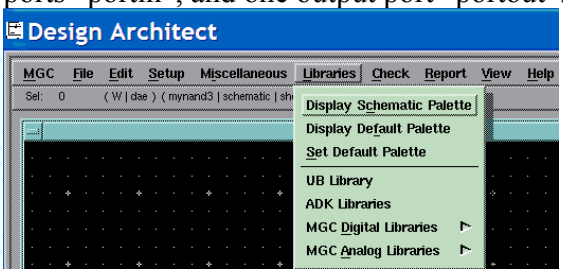
In the popup window, click at the end of the text in the “Component Name” box and type: /mynand3.



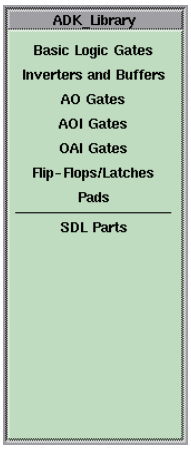
Then click on “OK”. You should get a clean schematic sheet. Maximize the sheet window so that you feel comfortable with it.

3. For our circuit schematic design, the procedures are described as follow: we will first place all the parts, then move or rotate/flip some devices if necessary, after that, we will make the wire connections among these parts, then we will name/label the nets, and finally we will set part properties (such as resistor values, transistor sizes, etc.), and check our design.

First we are going to place all the parts. In this circuit, we need the following parts: two “p-fet-4” (4-terminal PMOS transistors), two “n-fet-4” (4-terminal NMOS transistor), power Vdd and gnd, two input ports “portin”, and one output port “portout”. Click on menu “Libraries--ADK Libraries”.

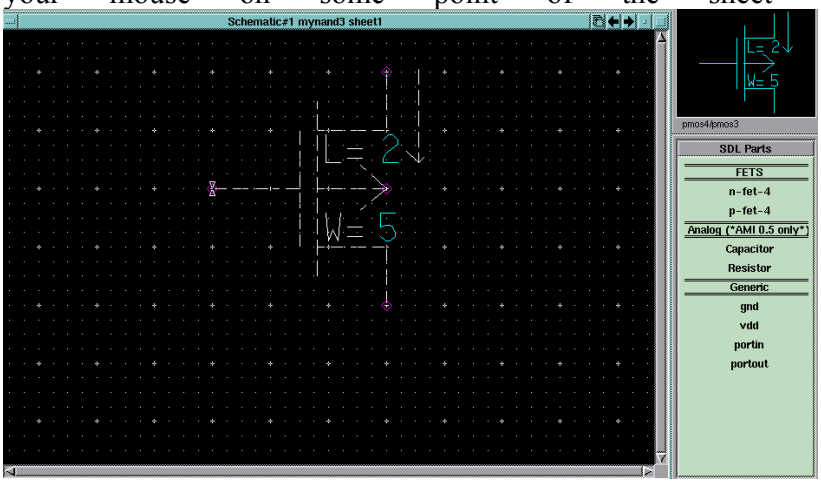


The ADK_Library palette shows up on the right side:



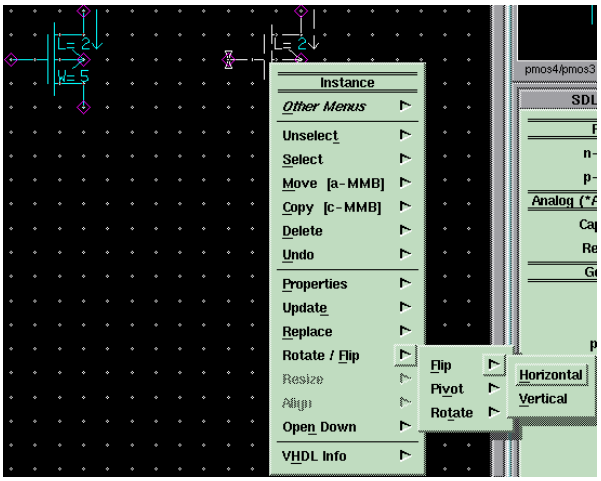
Click on palette “SDL Parts”, you will see the available parts in “SDL library”, such as n-fet-4 (4-terminal NMOS), p-fet-4 (4-terminal PMOS), capacitor, resistor, gnd (ground), Vdd (power source), portin (input port), portout (output port), etc. We can use these parts for our design.

4. Please click on the palette “SDL Parts—FETS—p-fet-4”, and move your cursor to the design sheet region, you will see a 4-terminal PMOS device shows up and move together with your cursor. Left click your mouse on some point of the sheet to drop it in your design.

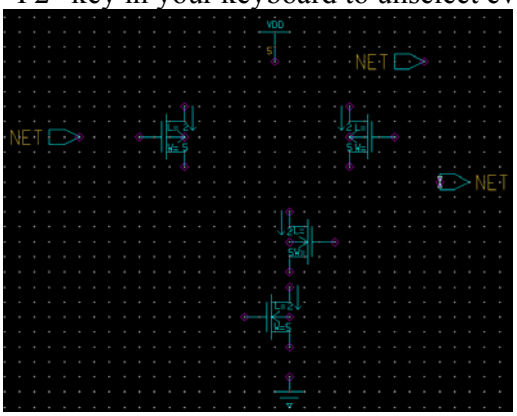


You will see that the PMOS transistor looks too large in your design. This doesn’t matter. Just click on menu “View—Zoom out—3.0”, you will see the device becomes smaller and you have more space for your design. You may also click on the “maximize” icon (the rectangle in top right corner) to maximize your design view. At this time, you will see the transistor size is defined as “W=5” and “L=2” (the unit is lambda). This doesn’t matter. We won’t worry about it now because we can adjust it later.

5. Now please repeat the similar procedure to place another instance of p-fet-4 into your design. Then click to select this p-fet-4, its color will be changed to blue to indicate it’s actively selected. (Note: If you want to unselect a device, press the “F2” key in your keyboard. This will unselect all the selected items.) Then right click your mouse on this device, and in the popup menu, select “Rotate/Flip—Flip—Horizontal”.

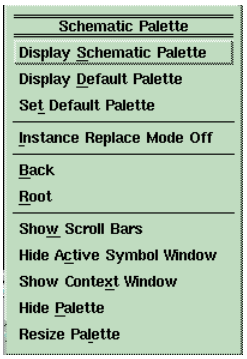


You will see the selected p-fet-4 device is flipped horizontally. Now continue the above similar procedures to place two "n-fet-4" devices (i.e. 4-terminal NMOS transistor), power Vdd and gnd, two input ports "portin", and one output port "portout" into your design. You may need to move or flip a part if it's necessary. If you want to move a part, please right click your mouse and select "Move—Selected:" to move it. Sometimes you selected more parts in your design, and you want to unselect it, then just press "F2" key in your keyboard to unselect everything. Now you will come to the following design.

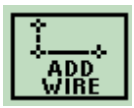


Also please find out the model name for your PMOS and NMOS devices. First press "F2" button to unselect all. Then click on any of your PMOS transistor to select it, right click mouse to get popup menu. In the popup menu, select "Properties—Modify", you will get a popup window about the transistor. Please scroll down to find out the line of "ASIM_MODEL=" to check the model name for your PMOS device. In our case, we use "p-fet-4", you should see the following line:
"ASIM_MODEL=p".
Please remember this name "p", because you may need it if you want to create your own spice parameter for NMOS/PMOS devices in Accusim simulation. Use the similar procedure for any NMOS transistor to check the model name of NMOS. In our case, you should see the line as "ASIM_MODEL=n".

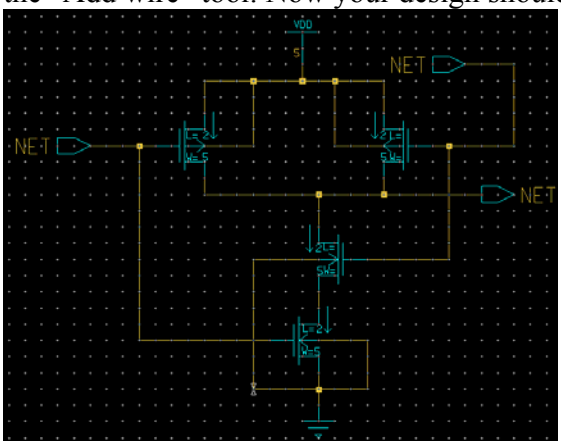
6. Now we are going to make the wire connections. Please right click your mouse on any point in the right palette, in the popup window, click "Display Schematic Palette".



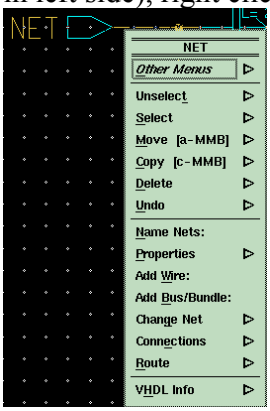
This will bring you back to the main Schematic palette. Please click on “Add wire” icon in the palette:



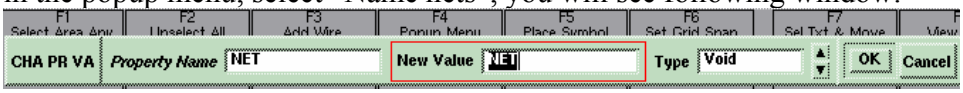
Now if you move your cursor into the design sheet, you will see your cursor changes into a cross. You can click on one point and move your mouse to another point and click it, you will see a wire connection is generated between these two points. You can continue to move and click to create multiple segments of the wire. When you don’t want any more wire segment, just click that point twice, and you will end the wire connection. If you made a mistake, you can right click your mouse to select “Undo”, or just click to select the unwanted wire segment and press the “delete” key in your keyboard to delete it. Now please make the wire connections for the circuit till you get following design. Please note that you need to connect the bulk of PMOS to Vdd, and the bulk of NMOS to Gnd. After you finish all the wire connections and you don’t need any more wire, you can press the “Esc” button on your keyboard to exit the “Add wire” tool. Now your design should look like follow.



7. Now we are going to name (label) the input and output ports. First please press “F2” key in your keyboard to unselect everything (this guarantees that you will only select the part you want). Then click to select the wire segment which is closest to the port you are going to label (here it’s the input port “portin” in left side), right click mouse, you will get a popup window:

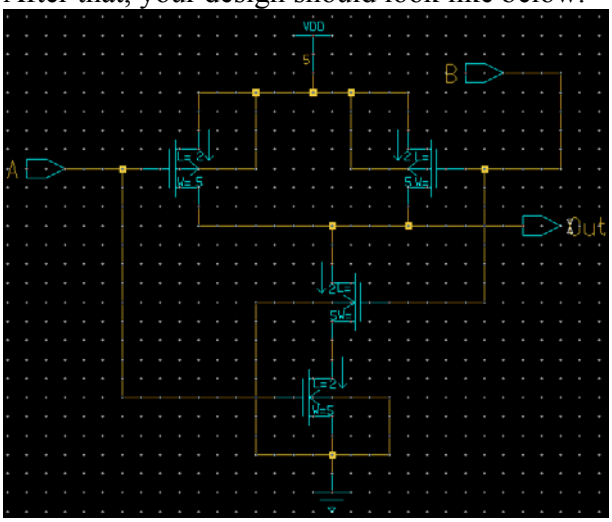


in the popup menu, select “Name nets”, you will see following window:

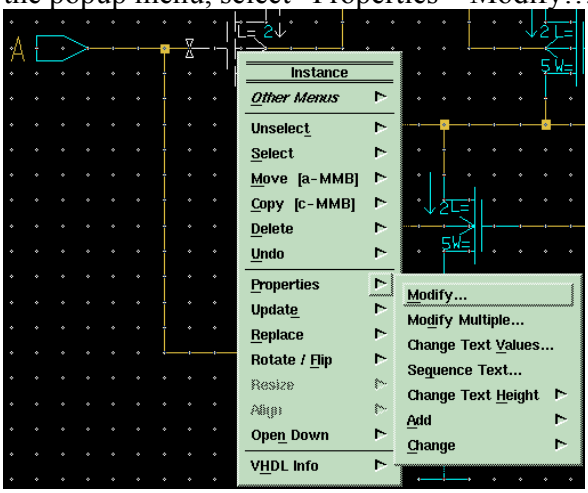


Click on the region of “New Value”, delete the text of “NET”, and type in new name as “A”. Then click OK. You will see that the input port has been renamed from “NET” to “A”.

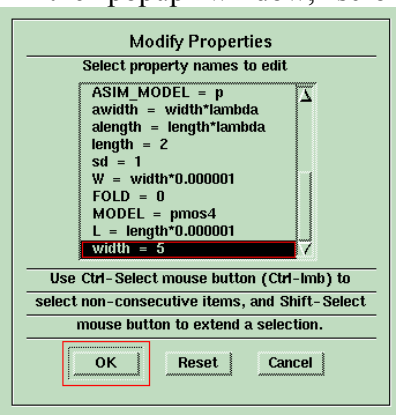
Repeat the similar procedure to rename the other input port as “B”, and the output port as “Out”. (Note that “VDD” and “GND” nodes are automatically assigned with the names, and you needn’t worry about it.) After that, your design should look like below.



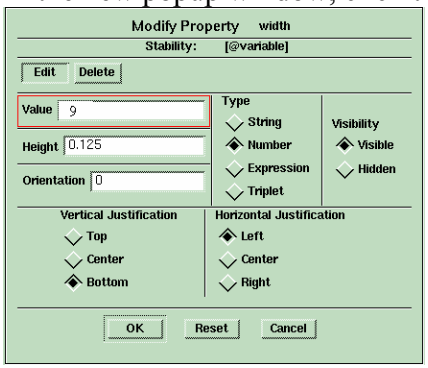
8. Now we are going to set the part properties, such as the sizes (width and length) of transistors, the value of resistors and capacitance, etc. First let’s change the size of top left PMOS transistor into W=9L (L is lambda). First press “F2” to unselect all, then click on top left PMOS transistor, and right click mouse. In the popup menu, select “Properties—Modify…”.



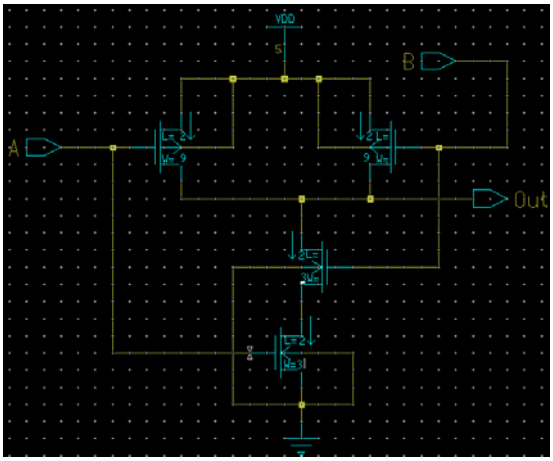
In the popup window, scroll down to click to select the line of “width=5”, then click OK.



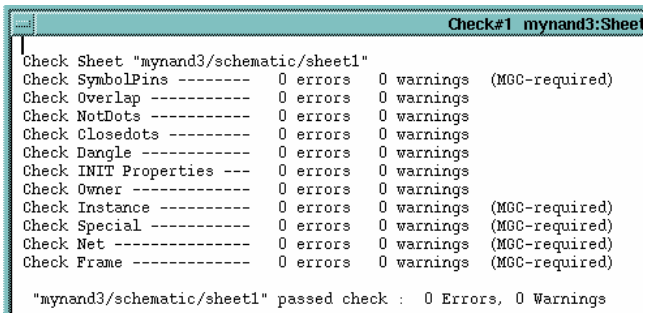
In the new popup window, click the line of “Value“, and change the value of “5” to “9”. Then click OK.



You will see the width of the transistor has been changed to “W=9”. Repeated the above procedures to change the width of top right PMOS transistor to be “W=9”, and change the widths of both NMOS transistors to be “W=3”. Sometimes you find that you cannot get the correct menu when you right click your mouse, then please check whether you have selected more than one part. Please make sure to press “F2” to unselect all before you select a transistor to edit its properties. Now your design should look like this.



9. Now we finished our schematic design. We will run a check to see whether there is any error in it. Please click menu “Check—Sheet”. You will get a check report as follow. Please check the report to see if there is any error. If there is any error, please find out the reason and go back to revise your design to solve the problem. The warning may be ignored. However, you must ensure there is zero error in it in order to proceed to next step.



10. Now click on the top left icon of the report window and select "Close" to close the report window. Click on menu "File—Save sheet" to save your schematic design, and then click on menu "MGC—Exit" to exit Design Architect.

Section C. Creating an ICGraph viewpoint

In order to simulate your design in Accusim, you will need to create a viewpoint for your design. This viewpoint file is just like a netlist of your circuit. It's necessary for other Mentor Graphics to perform analysis on your design.

1. After you exit "Design Architect", now you come back to "terminal console" command prompt window. First make sure you are in the same directory as your schematic design file. Your schematic design files should be kept in the directory of "/home/your_user_name/mentor_work". You must be in the same directory in order to use the "adk_dve" command to create the ICGraph viewpoint. Please type:

pwd

in terminal console prompt window and enter it. This command will display your current directory. If it's already in your "/home/your_user_name/mentor_work", then you needn't do anything and directly go to next step to create the viewpoint. However, in this example, I found that my current directory is my home directory "/home/xxiong".

```
india% pwd
/home/xxiong
india%
```

In this way, I type the "ls" command to see the current files and subdirectories in this directory. Please type "ls", and I see the following file/subdirectory display:

```
india% ls
1.txt               album1.html         mgc
AdobeFnt.lst        fft.Svdm_svdb.attr  xfig.SAVE
adk_dve.log         mentor_work         xv1
```

The "mentor_work" directory is there. Then use "cd" command to enter that directory. I enter the command of "cd mentor_work" as shown below:

```
india% cd mentor_work
```

Now I enter command "pwd" again to check my current directory, and find that I am already in the "/home/xxiong/mentor_work" directory.

```
india% pwd
/home/xxiong/mentor_work
india%
```

2. Now in the prompt window, input the following line:

adk_dve mynand3 –technology ami05

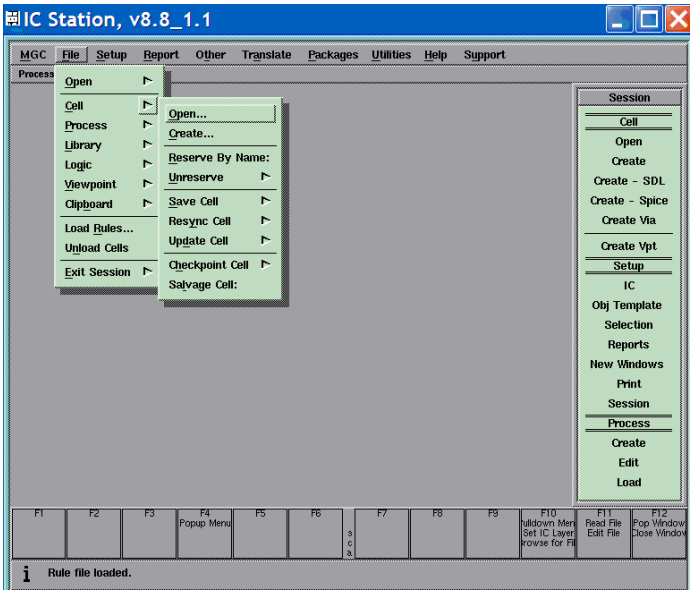
You will see a lot of text scrolling on the screen. Your viewpoint file for your design will be created. The format of "adk_dve" command is:

adk_dve *your_design_name* –technology technology_name

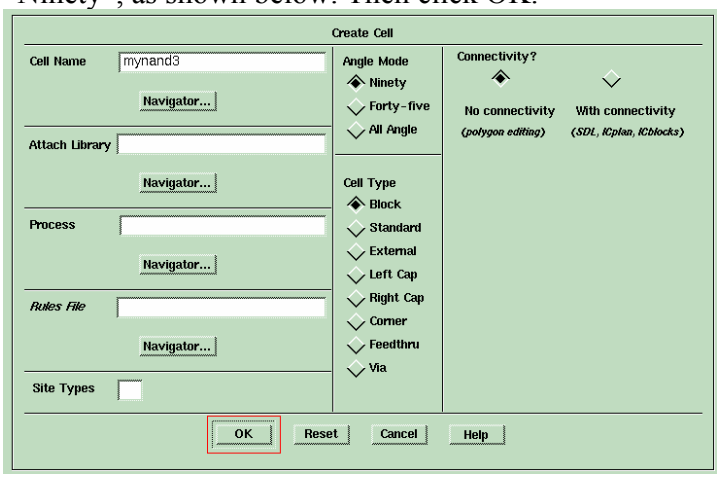
This will create the viewpoint for your design with the technology you want. Here we are using "ami05" technology, which means C5N process with a feature size of 0.6um. The lambda equals half of the feature size, which is 0.3um.

Section D. Layout Design with ICGraph

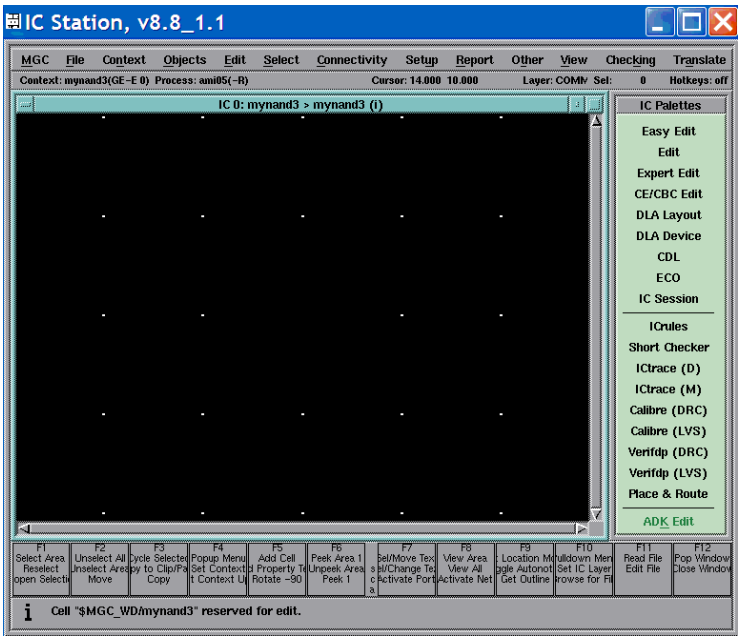
1. In the terminal console prompt window, please enter command “ic”. You will see the GUI interface of the Mentor Graphics ICStation for layout design as shown below. Please click on menu “File—Cell—Create…”.



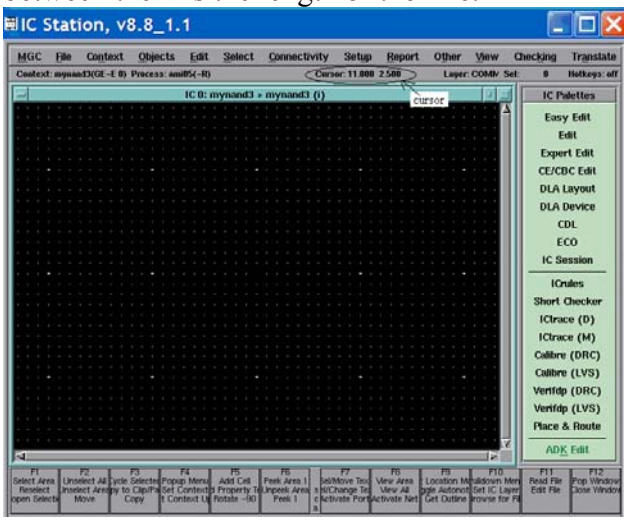
You will see a popup window as below. In the “Cell Name” row, please input “mynand3” as the name of the layout design. You can use any name you like. In the “Angle Mode” option, please click to select “Ninety”, as shown below. Then click OK.



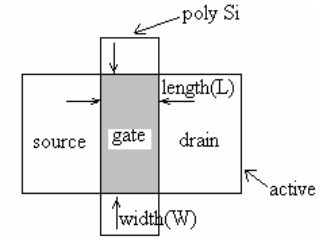
You will see a new layout sheet available for your layout design, as shown below.



2. Please click menu "View—Zoom—To grid", you will see the layout sheet is zoomed to grid. In the layout design, the grid system is helpful for you to find out the size of your layout pattern. By default, each minor grid will be 0.5 lambda. Your cursor will be snapped to the grid in your design. Also you can see that your cursor coordinates will be dynamically displayed on the top below the menu, as shown in the circle below. The cursor coordinates are in unit of lambda. This cursor display is very helpful for you to find out the size of your rectangular patterns. For example, you want to measure the length of a horizontal line, just place your cursor on both ends of the line and read the X coordinates of both ends, the difference between them is the length of the line.



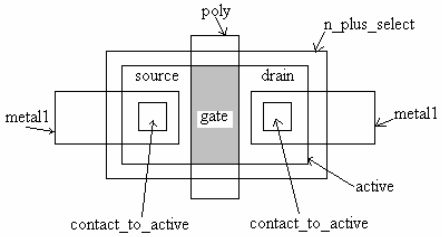
Before we start our layout design, we should have a rough sketch about the layout on paper. First let's know how a basic MOS transistor can be designed. The layout is actually the top view of your circuit. The basic MOS transistor can be formed by crossing a poly (poly-Si) layer on top of the active layer. As shown below, when a poly cross an active layer, the overlap area (shaded area) is the gate region (also the conductive channel) of the MOS transistor. The length (L) and width (W) of the transistor is marked in the figure. Whenever a poly cross an active layer, a MOS transistor is formed. Thus when you want to count how many transistors you have in a CMOS layout, you just need to count how many times a poly layer cross active layer. In the VLSI fabrication, the active layer only opens the doping window in the Si wafer. However, whether you will have p-type or n-type doping is decided by the layer of p-plus-select or n-plus-select. In order for the tolerance of photolithography misalignment, the p-plus-select or n-plus-select needs to be slightly larger than the active rectangle.



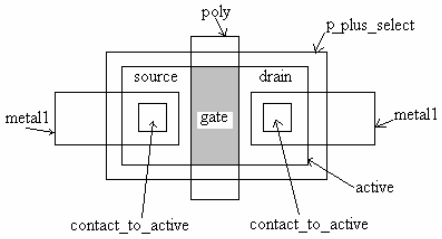
a MOS transistor

The rule to decide NMOS or PMOS transistor is:
1). If the active layer rectangle is inside the n_plus_select rectangle, then the doping of the source and drain will be n-type, and it will be a NMOS transistor, also it needs to be on top of p-substrate.
2). If the active layer rectangle is inside a p_plus_select rectangle, then the doping of the source and drain will be p-type. Hence it will be a PMOS transistor, and it must be on top of n-well.

In a circuit, source and drain of MOS transistors are connected with metal wires (metal1 layer). However, please note that there are insulations between different layers. Thus in order to connect the metal wires to source and drain, you need to design contacts (contact_to_active layer) for sources and drains. Please note that in order to tolerate process variation, we must follow certain design rules in our layout design. For example, the poly gate must extrude the active region for at least 2 lambda, p_plus_select (or n_plus_select) must be larger than active region by at least 2 lambda, the size of a contact_to_poly or contact_to_active must be exactly 2 labmda by 2 lambda, the minimum width of a poly gate is 2 lambda, etc. The full design of a NMOS and PMOS transistors are shown below.

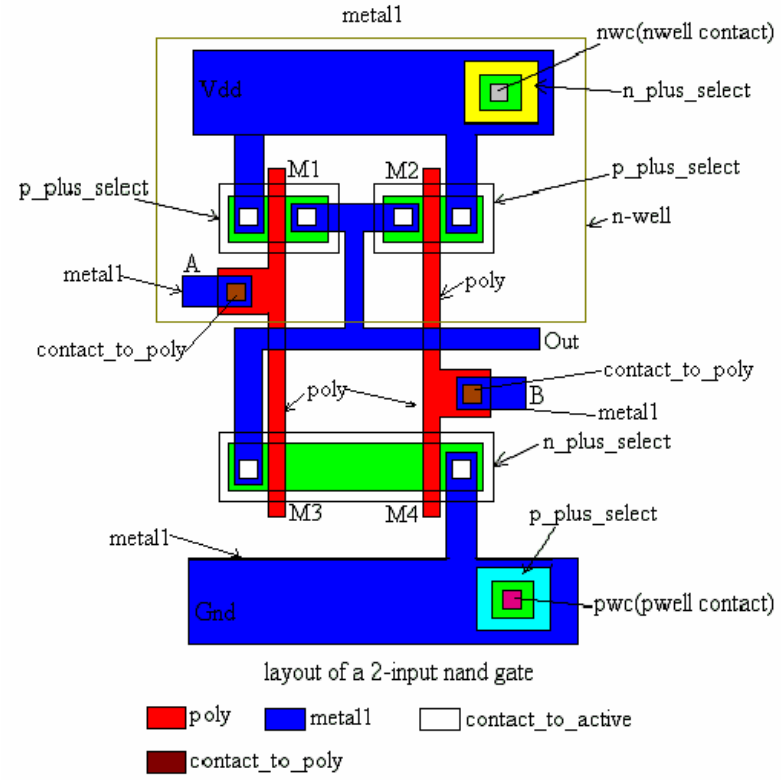


layout of a NMOS transistor

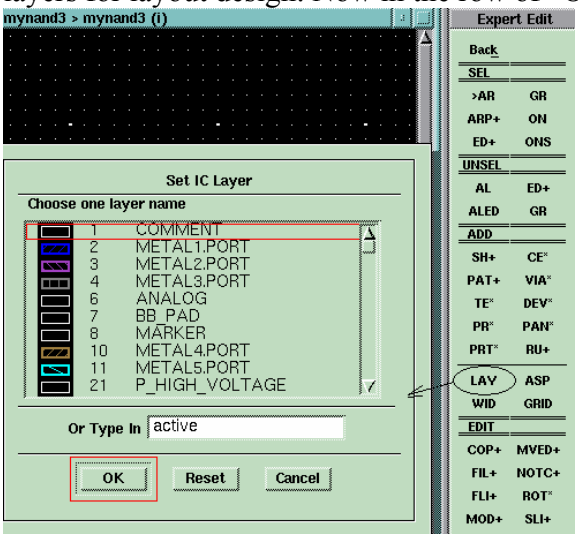


layout of a PMOS transistor

The basic layers for constructing VLSI layout include poly, active, p-plus-select, n-plus-select, n-well, contact_to_poly, contact_to_active, metal1, metal2, via, etc. We first sketch the layout of 2-input nand gate on paper as shown below. Generally transistors are formed by overlapping poly on active region, and metal1 is used for wire connection as well as power (Vdd and Gnd) rails. Poly is used for gate materials. For easy connection among transistors, generally we can add a metal1 to the poly gate, and put a contact_to_poly between them. Please note that we have 2 PMOS (M1 and M2), 2 NMOS (M3 and M4) transistors in the nand gate design. The sources of M1 and M2 are connected to VDD, the drains of M1 and M2 are connected together by metal1, and they are connected to "Out" port as well as the drain of M3. Since the source of M3 and the drain of M4 are connected together, they can share the common active region and no contact is necessary. The source of M4 is again connected to the Gnd. The gates of M1 and M3 are connected together, they are connected to portin "A" by a contact_to_poly and metal1. The gates of M2 and M4 are connected together, they are connected to portin "B" by a contact_to_poly and metal1. These connections are the same as our schematic design. Also note that MOS transistors are 4 terminal devices, and we need to connect the bulk of PMOS transistors to highest voltage level (VDD), and connect the bulk of NMOS transistors to lowest voltage level (Gnd). In order for this connection, the n-well (bulk of PMOS) is connected to metal1 of Vdd through n_plus_select, active, and nwc (nwell contact). Also the p-substrate (bulk of NMOS) is connected to metal1 of Gnd through p_plus_select, active, and pwc (pwell contact). The hand sketch of 2-input nand gate is shown below. Please note that this is just an example design. You can create your own custom design by rotating the transistors, arranging the wires to make it more compact.

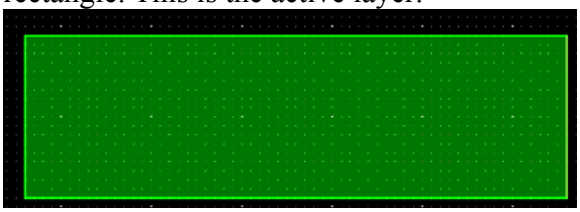


3. Now with this hand sketch, we can begin to design our layout. Please note that the size of M1 and M2 are: W/L=9L/2L, the size of M3 and M4 are 3L/2L. Let's click on the palette on the right side: "IC palette—Expert Edit", you will see the edit menu shows up as below. Let's click on the palette "LAY" to select the layer you want to create pattern with. You will see a popup window showing all the available layers for layout design. Now in the row of "Or type in" please input "active" and click OK.

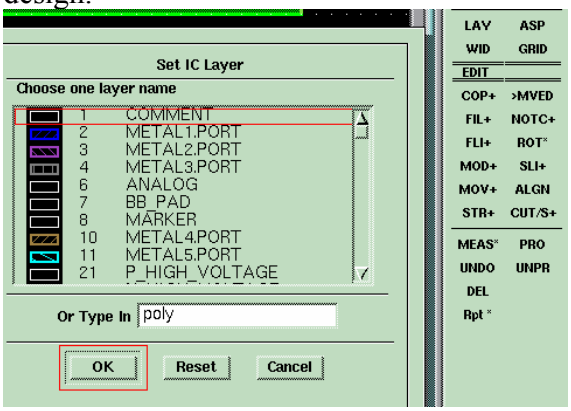


Now you are ready to create active layers in your design. Please click on the palette "ADD—SH+", as circled below.

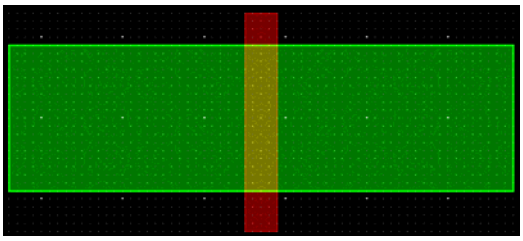
Now use your mouse to click and drag to create a rectangle with length of 30 lambda and width of 9 lamda. You can decide the length of the rectangle with the help of the displayed cursor. After you move the cursor to the desired location for the rectangle, click to release it. Now you see an empty rectangle because it's in selected mode. Please press "F2" button to unselect it. You will see it changes into a shaded green rectangle. This is the active layer.



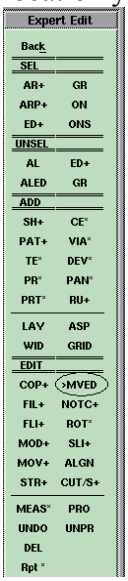
Now please click on the palette "LAY". In the row of "Or Type in" in the popup window, please input "poly". This will select "Poly" as the working layer and we are going to create poly-silicon layers in the design.



Please click on palette "Add—Sh", you can add shape now. Use your mouse to click and drag a poly-silicon shape with width of 2 lambda in about the middle of the active rectangle. After that, press "F2" key to unselect it, it will change from an empty red rectangle to a red-filled rectangle. This is the poly silicon pattern. Now you should have an overlap between poly and active region. That is, you already created a MOS transistor in your layout. Please make sure your poly gate actually extrudes the active region by at least 2 lambda. Now your design looks like follow.



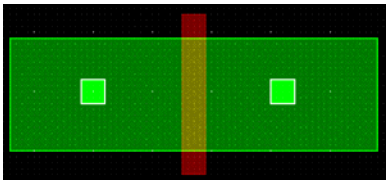
Please note that if you are not satisfied with the size of a rectangle, you can click palette “Edit—MvEd”, this is the “move-edge” command. You can click on any edge of a rectangle, and drag to move it to the location you want, and then click to release it. In this way, you can resize the size of a rectangle.



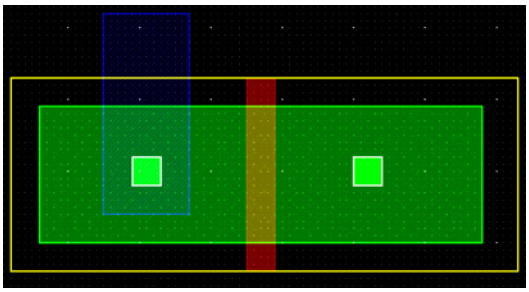
There are also other commands such as “copy+” (copy command), “mov+” (move command). Please play with them to get familiar with these commands. They can be very helpful in your design.

4. Now let’s add two contact_to_active on the source and drain. The contact_to_active must be exactly 2 lambda by 2 lambda according to DRC rule. First click on the palette “LAY”. In the row of “Or Type in” in the popup window, please input “contact_to_active”. This will select “contact_to_active” as the working layer and we are going to create contact_to_active in the design. Please click on palette “Add—Sh”. Use your mouse to click and drag a contact_to_active rectangle with width and length of 2 lambda at the center (needn’t to be exact) of the source region. After that, press “F2” key to unselect it. Please use the cursor display to help you decide the size of the rectangle you have draw to ensure it’s exactly 2 lambda by 2 lambda. When you draw the contact_to_active, if it’s not in the center, try to move it with “MOV+” menu. Now your design should look like below.

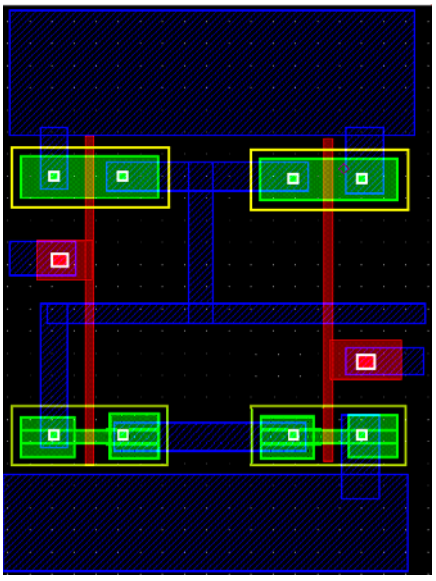
Hint: How to move a rectangle: First press “F2” to unselect all. Then click on palette “SEL—AR+” (select area), then click to select the rectangle you want to move. After that, click on the palette “Edit—Mov+”, then click on any point on your layout sheet, and you should be able to move your rectangle to that point.



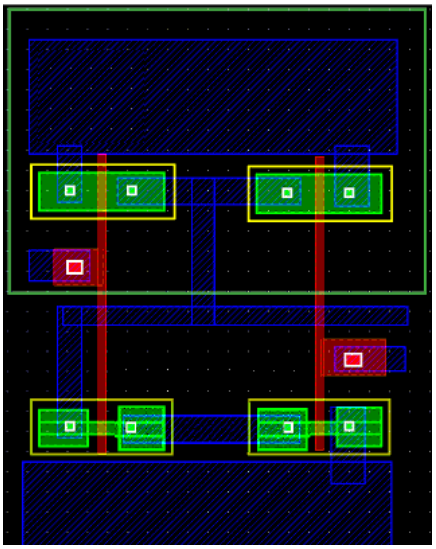
Now please use the similar procedures to add a p_plus_select rectangle which is at least 2 lambda larger than the active rectangle, this will define your transistor as PMOS. Also please add a metal1 wire to the source of the PMOS transistor. Now your transistor should look like this.



5. Now use the similar procedures to create other 3 transistors, and create power rails (metal1 for Vdd and Gnd), and the connections (contact_to_active, contact_to_poly, metal1, etc.). The names of the layers you need to type in when selecting working layer are: poly, active, p-plus-select, n-plus-select, n-well, contact_to_poly, contact_to_active, metal1, etc. During the design, if you want to delete a pattern, just click to select it, and press "Delete" key, you can delete it. Please note that for metal1 wire connection, we may need several segments to overlap each other for the connection. This is normal and it's not a problem. For the same material, if they are overlapping with each other, this means they are connected to each other and no contact is needed. However, for different materials, because they are in different layers and there is insulation layer between the layers, thus if you want to connect different materials, you need to overlap them and also add a contact for them. This is the reason that if we want to connect metal1 to active layer, we must overlap them and add a contact_to_active to them. Please note that you have the flexibility in deciding the shape and size of the components except the width and length of each transistor. For example, you can decide your metal1 wire width, the size of the nwell, etc. You can even rotate some transistors to make it either horizontal or vertical. Here in this example, we will just follow our sketched design for our layout. During the layout design, some operation may be very helpful. Now your design should look like below.



6. Now we need to add nwell for the PMOS portion. Please be aware that NMOS are directly built on p-substrate, but for PMOS devices, we must design a nwell for it. Please use the similar procedures as above to add a nwell rectangle to include all the PMOS transistors. Please click on the palette "LAY". In the row of "Or Type in" in the popup window, please input "nwell". Please click on palette "Add—Sh", you can add shape now. Use your mouse to click and drag a nwell rectangle to include all the PMOS devices. After that, press "F2" key to unselect it. Now your design looks like follow.



7. Now we need to connect the bulk of PMOS and NMOS transistors.

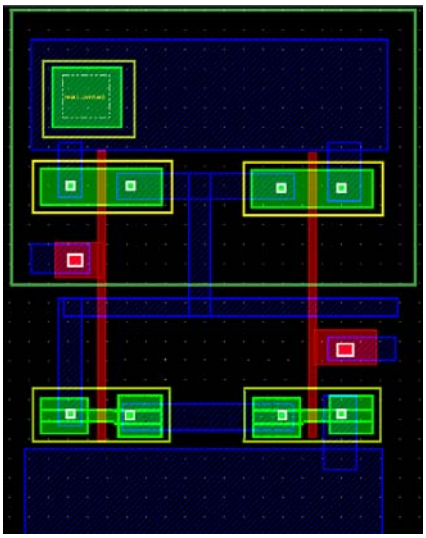
1). The bulk of PMOS is actually nwell, we need to connect it to Vdd. Thus we need to design a nwc (nwell contact) on the overlap region of nwell and Vdd metal1 rail to connect the nwell to Vdd. We also need to design "active" and "n_plus_select" rectangles to surround it to ensure good electrical connection.

2). The bulk of NMOS is actually p-substrate, we need to connect it to Gnd. Thus we need to design a pwc (pwell contact) on the overlap region of Gnd metal1 rail and p-substrate to connect the psubstrate to Gnd rail. We also need to design "active" and "p_plus_select" rectangles to surround it to ensure good electrical connection.

First let's create "nwc" (nwell contact) for the nwell. click on palette "SEL—AR+", then move your cursor to anywhere in the design sheet and type "nwc" from your keyboard. (Please make sure you move your cursor to the design sheet instead of other places. Otherwise you would not be able to get the "IC 0" input panel.) Now you will see the following input panel:

After you type "nwc" and enter, you will see a nwc nwell contact is moving with your cursor. Move your cursor and click on the metal1 Vdd power rail, you can place a nwc there. Then press "F2" to unselect it, you can put the nwc into your design, as shown below. You can see the size of the nwc is fixed as 12 lambda by 12 lambda.

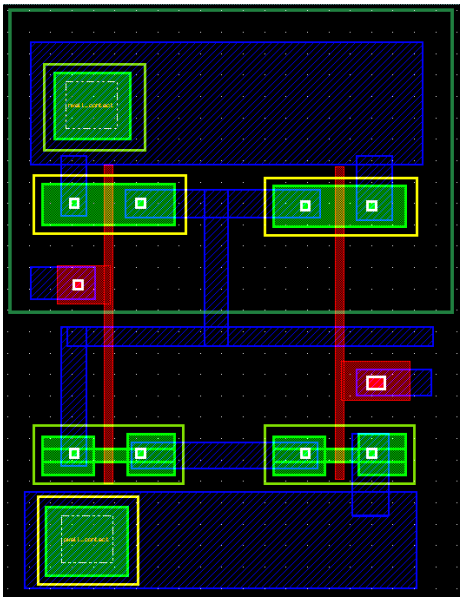
Now continue to add the "active" and "n_plus_select" rectangles. After that, your design should look as follow.



Now let's create the "pwc" (pwell contact). Please type "pwc" anywhere in the design sheet, you would be able to get the same "IC 0" input panel.

After you finish typing "pwc" and enter it, you can place a pwell contact (p-substrate contact) on your metal1 Gnd rail, and press "F2" key to unselect it. You can see the size of the nwc is fixed as 12 lambda by 12 lambda.

Now continue to add the "active" and "p_plus_select" rectangles. Now we finish all the layout design. Please click menu "View—All" to see the whole circuit layout design. Your design should look as follow.

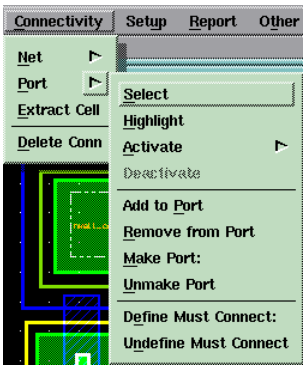


Up to now, we have finished the layout design of the nand gate. This is a standard cell layout design. You can see it's not very area efficient, there is some empty area in it. If you want to be area efficient, you can try to rotate the MOS transistors to achieve a fully customized compact design.

8. Now we are going to save our design. Please click on menu "File—Cell--Save cell". Whenever you save the cell to disk, Mentor Graphics makes the cell immediately available for others to use, and as a result, it changes the cell properties to read only. That is, it will not allow you to make any more change to the cell. Thus, if you wish to edit the cell (for example, to draw a rectangle, etc.), you will see that no action is allowed. If you want to continue to edit your cell, you must reserve the cell to yourself (and disable others from using it).

9. Now we need to assign the port names to our input/output/power lines, so that ICGraph can understand the connectivity between the schematic and the layout. This is very important for LVS verification. Since we just save the design, now it's not editable. We need to reserve the cell for editing. Please click on the menu "File—Cell—Reserve".

10. First click on palette "SEL—AR+", press "F2" key to unselect all, and click on the metal1 VDD rail to select it. Then click on menu "Connectivity—Port—Make port:". If you see that this menu is gray, please make sure whether you have reserved the cell. If you saved it and forget to reserve it, you won't be able to access this menu.



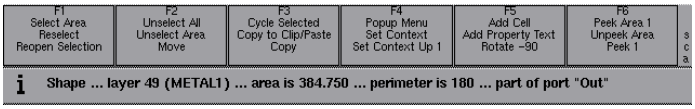
In the popup window, use the arrows to select the port type as "power", (In your circuit, only Vdd and Gnd are power, all the other nodes should be signals.), the direction as "in", and type the port name as "Vdd". (Please make sure here the port name should be exactly the same as you defined it in your schematic, otherwise it will cause problem in LVS.) By doing so, you can tell LVS tool to correctly map the nodes in your layout to the corresponding nodes in your schematic. Finally click OK.

You will not see any change in your layout. However, now the port name has been assigned to metal1 Vdd power line.

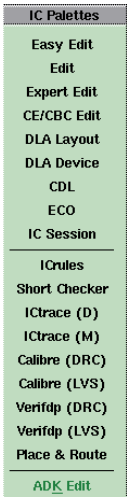
11. Similarly, select the metal1 Gnd rail and assign the port type, direction and name as shown follow.

12. Continue to select two input ports (poly), and assign the port type as "signal", direction as "in", port name as "A" and "B" separately.

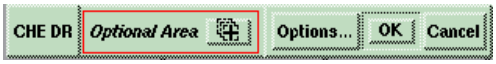
13. Select the output ports (metal1), and assign the port type as "signal", direction as "out", port name as "Out". Now we finished naming the ports. You won't see any port name displayed on your layout. However, these names do have been assigned to the ports. If you want to check the name of the port, just click to select it, the name of this port (if it has) will be displayed in the bottom of your layout sheet. For example, if you click to select the "Out" port metal1, you will see the following information in the bottom. This information clearly tells you that the port name of this port is "Out".



14. Now please click on menu “File—Cell—Save Cell” to save your design. Now let’s move to the verification stage of our layout design. We need to do two verifications for our layout desing: DRC (Design Rule Check) check and LVS (Layout Versus. Schematic) check. First let’s perform DRC check to see whether our design obeys “MOSIS/AMI TinyChip” design rules. If you are still inside the “Expert Edit” palette, please click on palette “Back” to go to the main “IC Palette” menu. In it, click on palette menu “ICrules”.

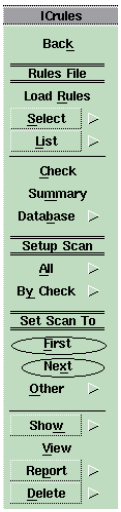


You will see following palette menu. Please click “ICrules”, you will see a popup menu bar as follow. Please click “OK”.



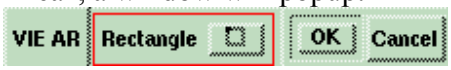
15. Now IC station will perform “DRC” check and give you the results in the bottom of you design sheet, as shown below.

Please note that “Total Results” tells you how many DRC errors you have in your layout design. If the “Total Results” is “0”, then congratulations, you have successfully passed DRC check. As an example, here we show one DRC error in this design. Your DRC report may contains different number of errors. Please go through each error step by step, and go back to the “Expert Edit” menu to revise your design accordingly, then redo the DRC check, till finally you have “0” error in your report. Since here we have one DRC error, now let’s find out what the error is. Please click on palette “Set Scan To—First”, it will show the first error in the message at the bottom of your design sheet, and the corresponding portion which contains the DRC error will blink for several time for you to easily locate your DRC error. After you finish reading the first DRC error, please continue to click on palette “Set Scan To—Next”, and read the following error message, till you reach the end of your error messages.

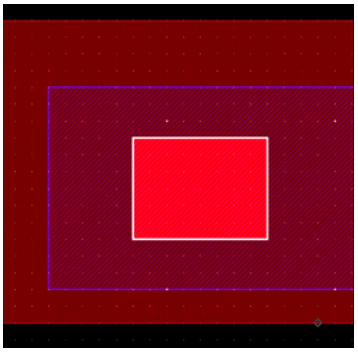


For example, if it shows the following DRC error message, and a contact_to_poly rectangle blinks for several times.

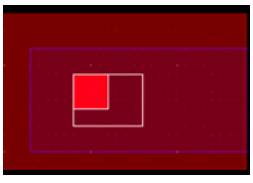
This tells you that the design rule requires the contact_to_poly size should be exactly 2L by 2L (lambda), but your contact_to_poly has a wrong size. Now let's go back to the "Expert Edit" palette to revise our contact_to_poly size to fix this DRC error. Please right click on palette "Back", and click on "Expert Edit" on the new palette to enter the "Expert Edit" mode. Now please click on menu "File—Cell—Reserve Cell" to reserve the cell for edit. Otherwise your design is not editable because you just saved it. Now let's try to zoom in the contact_to_poly rectangle which contains DRC error. Please click on menu "View—Area", a window will popup.



Please click and drag your mouse to define a window containing the contact_to_poly rectangle. This window will be zoomed in so that you can look at its details.



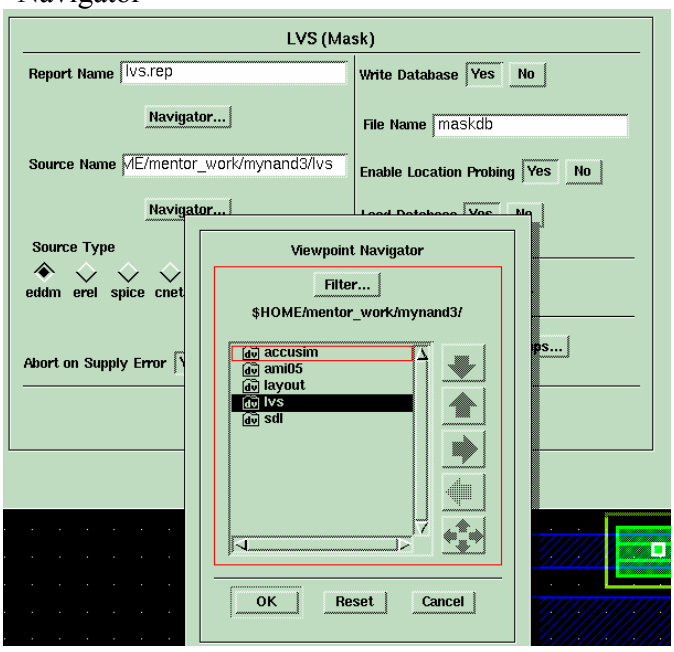
You can see that its size is really not 2L by 2L. Please click on palette "Edit—MVED" (move edge), and click to select one edge of the contact_to_poly, and move this edge to change the size of the contact_to_poly. Do this for the other edge so that you change the size of the contact_to_poly to 2L by 2L.



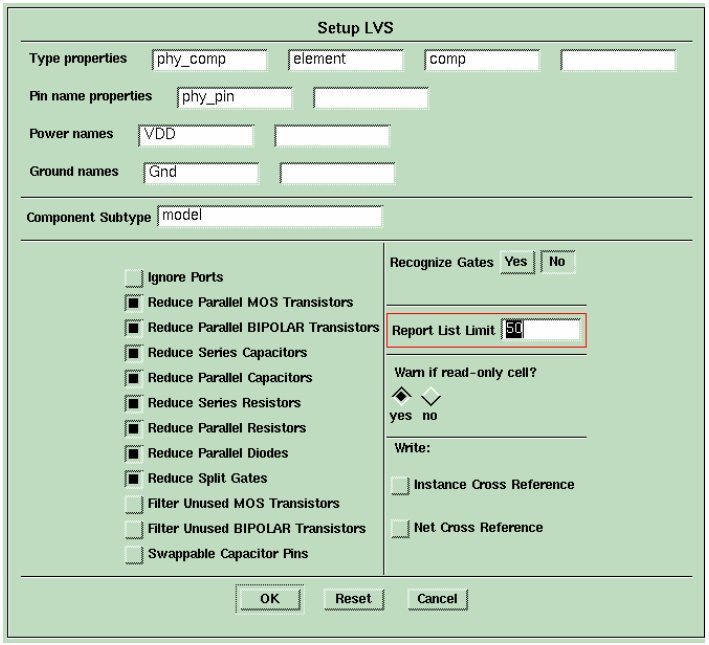
Now again save your design. After you correct all the errors in your layout design, now we will redo the DRC check to verify whether all the errors are corrected. Please click on palette “Back”. In “IC Palette” menu, click on palette menu “ICrules”, click “OK” on popup window to begin DRC rule checking. This time we see that the “Total Results” is 0. This means we already correct the DRC error in our design, and now our design successfully pass the DRC checking.

Please note that in above we showed one error as an example. However, in your design you may have different number of errors. Sometimes you need to go over and over again the process of “DRC check—go back to revise your design—redo DRC check—go back again to revise design” till finally your design get 0 errors in DRC report. You need to be very patient on it.

16. Now we are going to perform LVS check on our layout to compare it with our schematic design to see whether our layout is the same design as our schematic. Before this your design should already pass the DRC check without error. LVS checks every schematic net against the masks and reports any discrepancies, then it checks out the primitive properties (in our case, the dimensions). First we should setup LVS. Please click on palette “Back” until you are in the main “IC_Palettes”. In the “IC_Palette”, Click on “ICtrace(M)”, in the new palette, click on “LVS”. In the popup window, click on the “Navigator...” button under “Source Name” (this is the viewpoint that LVS is going to use as data source). You should see your "mynand3" folder in the Navigator box. Please double click on the “mynand3” folder to enter this folder. You will see an “lvs” viewpoint object in it. Click (don’t double click, just one click) on “lvs” object to select it (it’s marked with a small “dv” dv box beside it) and click on “OK” in the “Navigator” box.

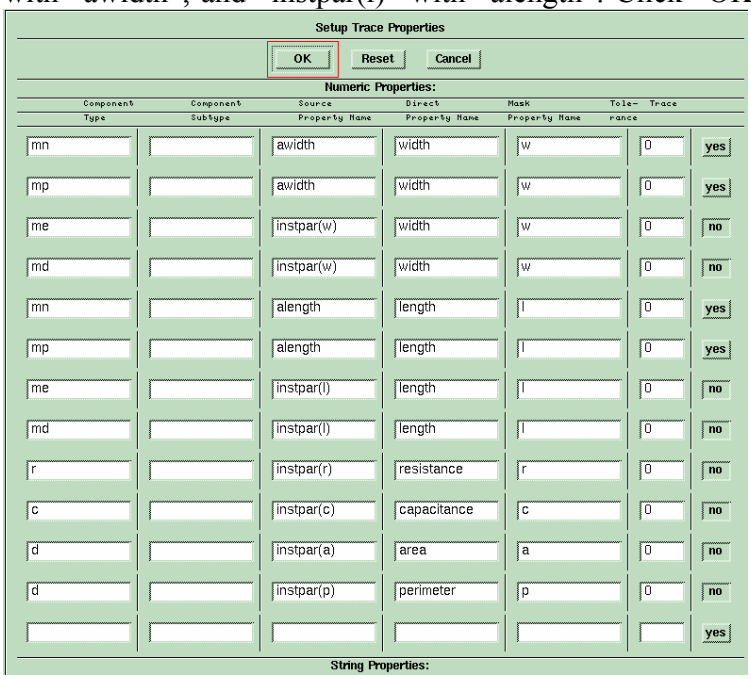


17. Now click on “Setup LVS...” in the popup window. In the new popup window, For “Recognize Gates” option please click on “No”. This will disable LVS from trying to analyze the masks at the logic gate level (it only works for standard cell designs). We also need to change the Ground name to be Gnd (not VSS). Move the cursor over the “VSS” in “Ground name” row, and type “Gnd” to replace it (this is because we use Gnd for the name of ground in our DA schematic design). Then click “OK” in the “Setup LVS” window to close it.

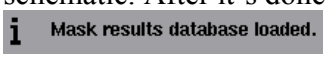


18. Click on “Setup Trace Props...”. The trace properties tell LVS which component properties to check against the mask database. As you probably see, the default setup is not to check any properties. We have entered the gate L/W properties and so we would like LVS to trace them. Each transistor in the schematic has an absolute length and absolute width properties. The absolute properties are the channel length and width, expressed in meters (this is derived by multiplying the length/width with lambda). We need to change the schematic property name to be the absolute values. The related components are mn (MOS N-type) and mp (MOS P-type), and for each we have an 'alength' property and a 'awidth' property that we need to set.

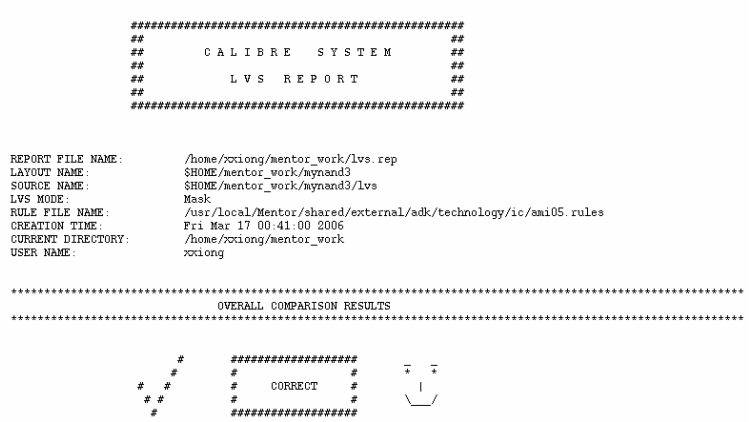
19. Click on the “no” button in the topmost line of the box (the “mn-w property” line), so it will turn to a “yes”. Change the 'instpar(w)' on the 'Source Property Name' Column to 'awidth'. Do the same for the second (mp-width), fifth (mn-length), and sixth (mp-length) lines, remembering to replace “instpar(w)” with “awidth”, and “instpar(l)” with “alength”. Click “OK” in the “Setup Trace Properties” dialog box.



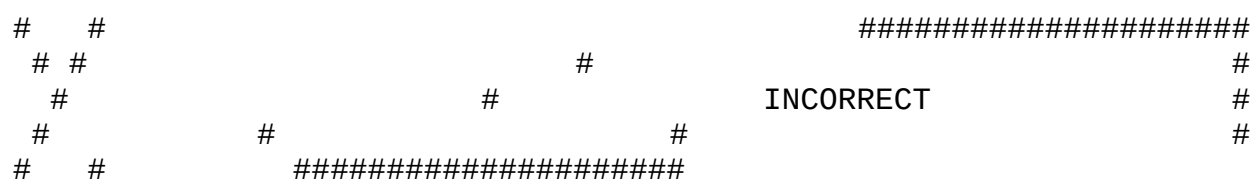
20. Click “OK” in the “LVS(Mask) dialog box” to close it. Now LVS starts to check your layout versus schematic. After it’s done, a message as below shows in the bottom of your design sheet.



21. Now we can now go to see LVS's report. Click (left mouse) on the arrow beside “Report” in the palette. Click (right mouse) on the palette “Report—LVS”. The report window will open up. If everything goes well, LVS prints at the top of the report a 'V' sign, a box with "CORRECT" in it, and a smiling face:



However, if it finds errors we will get in the report:



This means you have errors in LVS checking, your layout is not the same as the schematic you designed in DA. If this is the case, you should read the report carefully (maybe write some notes), go back to the mask window and to the Expert Edit palette, and correct your errors. then do LVS again (this time you do not need to setup anything in the LVS box - Just click LVS and OK). The report itself is very informative and contains valuable information that will help you in debugging your masks. Except of the report LVS has a handful of tools to locate the errors on the mask. We will not describe them here, but you should explore them by yourself (they will make your work much easier). They are all placed in the ICtrace(M) palette.

Section E. ACCUSIM Simulation

Now we are going to use Accusim to simulate our schematic to verify its function. The Accusim application is a graphic front end and a post processor for SPICE like kernels. Currently it is attached to the ELDO SPICE kernel which is included with the Mentor-Graphics Analog-Station package. Before you start the Accusim simulation, make sure you have previously created viewpoint file using *adk_dve* command as described in section C. You need the viewpoint file in order to load the technology parameter (λ) for the correct sizing of the transistors in Accusim simulation. If you make some changes in your design in DA (Design Architect), you need to rerun the *adk_dve* command to create a new viewpoint file. Otherwise, your change in DA may not be reflected in your Accusim simulation.

1. In terminal console prompt window, input following command:

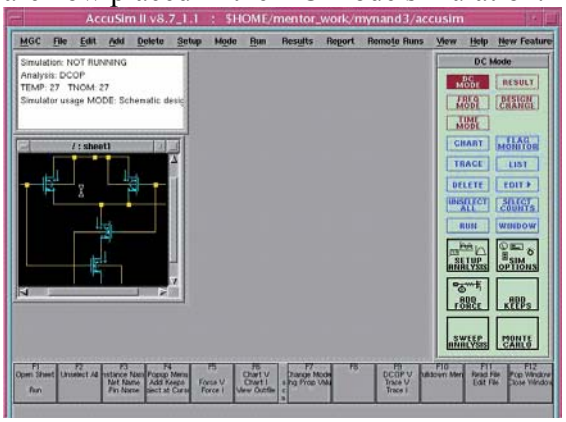
accusim mynand3/accusim

The general command syntax is:
accusim *your_schematic_design_name*/accusim

Please make sure you are not omitting "/accusim" part after your design name. If you omit the "/accusim" part and type the accusim command as follow:
accusim *your_schematic_design_name*

the viewpoint file created by *adk_dve* command will not be loaded in Accusim. In this way, you will not get correct sizing of the transistors in your netlist, and your simulation result will be wrong.

You should see your schematic design is already loaded in a window inside the simulator workspace. You are now placed in the DC mode simulation.



2. First, we have to load a model library for our parts. That is, we need to tell Accusim what model should be used for devices such as PMOS/NMOS transistors. Accusim allow you to input your own model file. If you want to use your own spice parameter for NMOS and PMOS, you can create a ".mod" file and save it into your mentor_work directory, then load it into accusim. In order to create your own model file, you need to know the model names for PMOS and NMOS which was used in Design Architect. For example, we already found in Design Architect before that the model names for NMOS and PMOS are "n" and "p" separately. Thus we may open a text editor and input following parameters into the file.

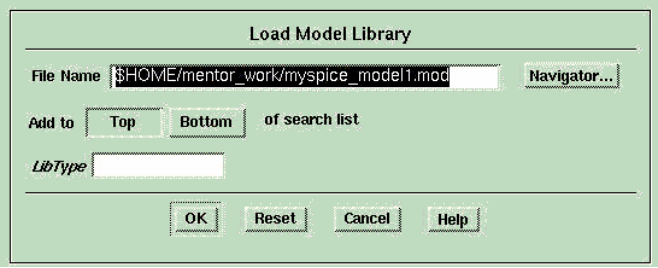
```
.MODEL n NMOS LEVEL  = 3
+ TOX    = 200E-10       NSUB   = 1E17          GAMMA  = 0.5
+ PHI    = 0.7           VTO    = 0.8           DELTA  = 3.0
+ UO     = 650           ETA    = 3.0E-6        THETA  = 0.1
+ KP     = 120E-6        VMAX   = 1E5           KAPPA  = 0.3
+ RSH    = 0             NFS    = 1E12          TPG    = 1
+ XJ     = 500E-9        LD     = 100E-9
+ CGDO   = 200E-12       CGSO   = 200E-12       CGBO   = 1E-10
+ CJ     = 400E-6        PB     = 1             MJ     = 0.5
+ CJSW   = 300E-12       MJSW   = 0.5

.MODEL p PMOS LEVEL  = 3
+ TOX    = 200E-10       NSUB   = 1E17          GAMMA  = 0.6
+ PHI    = 0.7           VTO    = -0.9          DELTA  = 0.1
+ UO     = 250           ETA    = 0             THETA  = 0.1
+ KP     = 40E-6         VMAX   = 5E4           KAPPA  = 1
```

+ RSH = 0 NFS = 1E12 TPG = -1
+ XJ = 500E-9 LD = 100E-9
+ CGDO = 200E-12 CGSO = 200E-12 CGBO = 1E-10
+ CJ = 400E-6 PB = 1 MJ = 0.5
+ CJSW = 300E-12 MJSW = 0.5

After you finish input the parameter into the text file, please save it as "myspice_model1.mod" in the "$HOME/mentor_work" directory. (Actually you can use any name you wish for this ".mod" file, just remember the name you used.)

3. Now we will load the model file we created. Click on menu "Files—Auxiliary Files—Load Model Library…", in the dialog box, click "Navigator" to find the "myspice_model1.mod" in the "$HOME/mentor_work" directory. Click to select it, and then hit "OK", your "myspice_model1.mod" model will be loaded for use.

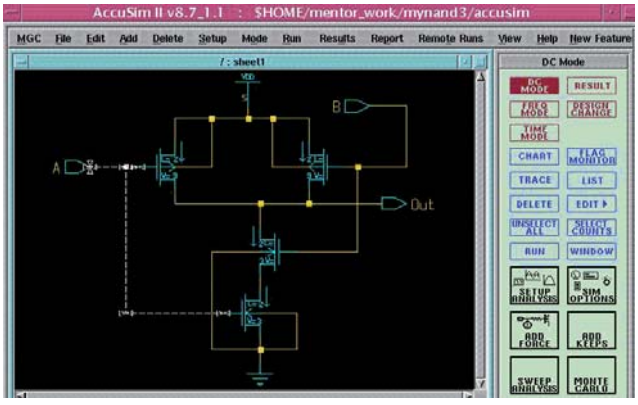


Note: If you don't want to input your own SPICE parameter, you can use the "ami05.mod" file (AMI05 SPICE model) of the system. Just click on menu "Files—Auxiliary Files—Load Model Library…", in the "File Name" row of dialog box, type

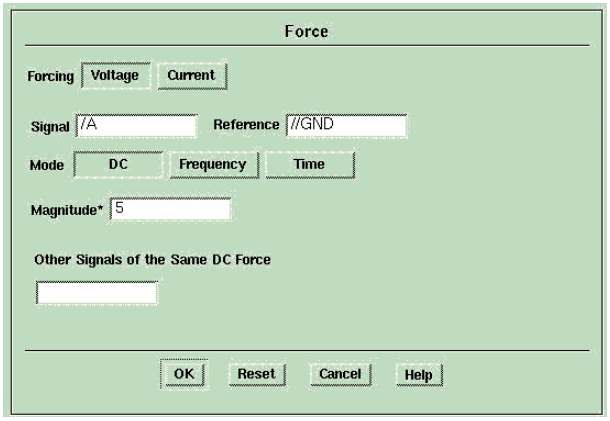
$UB_MODLIB/ami05.mod

Then hit "OK", the "ami05.mod" model will be loaded.

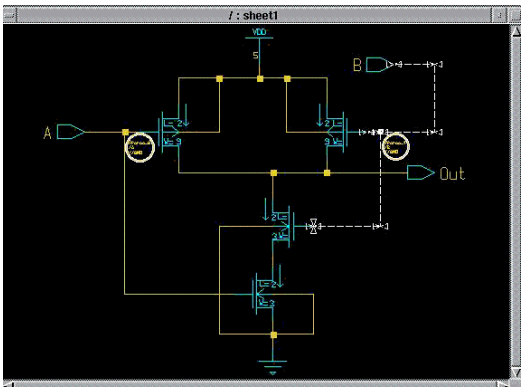
4. First we would like to perform a DC sweep analysis on input port "A" when input port "B" is kept at 5V. We now have to define a "force" on the input nodes, so we will be able to "force" them externally to any voltage we like. Select the "A" network by dragging a rectangle around the "A" port using your left mouse button.



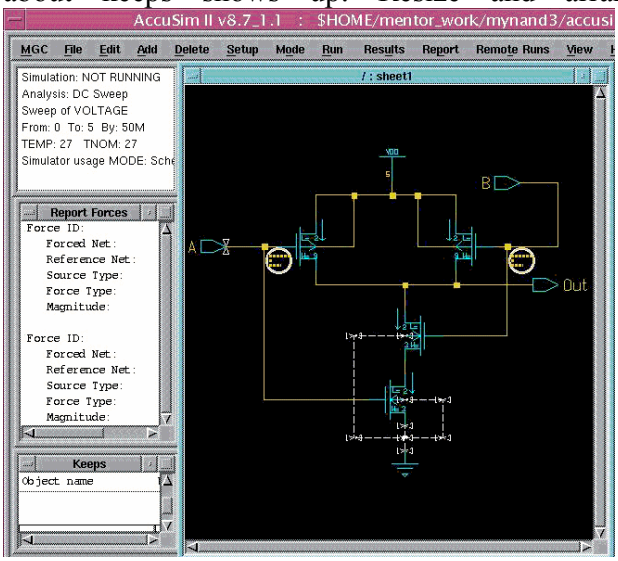
Then click palette "DC Mode--ADD FORCE". In the dialog box, set the "Magnitude" to 5, then press OK. This set a DC voltage of 5V on input port "A". You should see a force probe (a circle with data in it) appear beside the forced nets on the schematic.



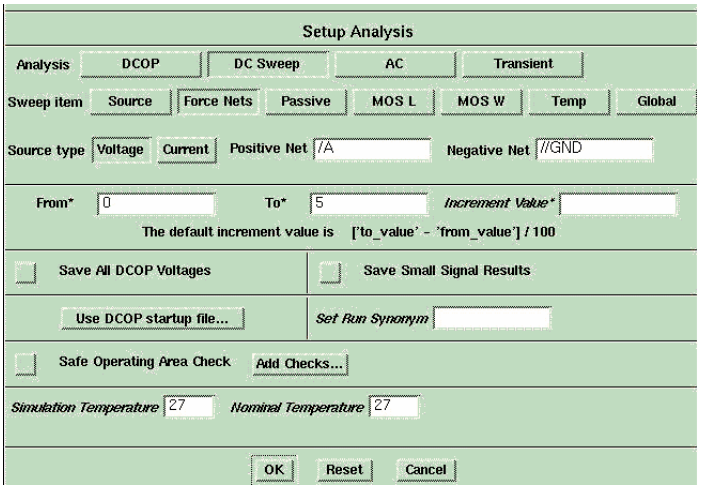
5. Do the same to the "B" network. After that, you should see the schematic as below.



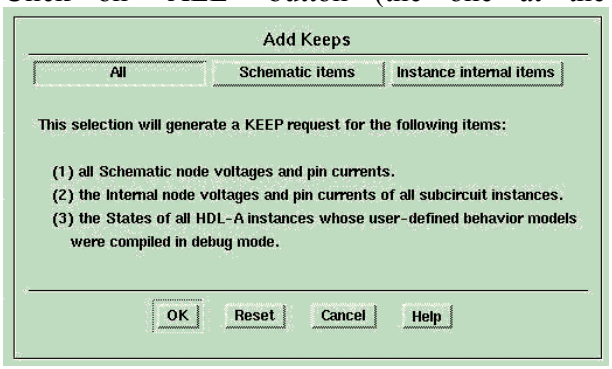
6. Let's have some report windows available. First click menu “Report--Forces on Schematic”, a report window about forces shows up. Then click menu “Report—Keeps--Schematic keeps”, a report window about keeps shows up. Resize and arrange the windows so that it looks like below.



7. Unselect all signals by pressing “F2” key, then select Net “A”. Click on palette “DC Mode--SETUP ANALYSIS”. In the popup window, click on “DC Sweep”, change the "from" value to 0, and the “to” value to "5". Notice that the net name is already set as “/A”, which is the net we would like to sweep between 0 and 5V. Now click “OK” to close the popup window.



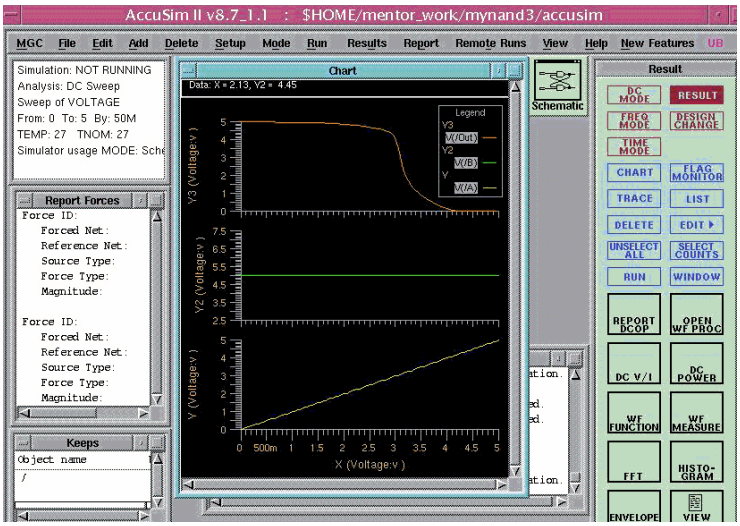
Notice that the simulation conditions have been updated in the simulation status window (upper left corner of the window). We now have to add keeps. Those are the circuit nodes whose signals will be recorded by the simulator, so that we can observe our simulation results on these nodes. Because our circuit is small we will keep all the nodes. Please click on palette “DC Mode--ADD KEEPS”, a popup window shows up. Click on “ALL” button (the one at the top) and on “OK” to exit the popup window.



You should see the Object "/" added to the Keeps report window (Accusim understands signal names as a hirarchy similar to a file system and so keeping "/" means keep everything from the signal tree root and down).

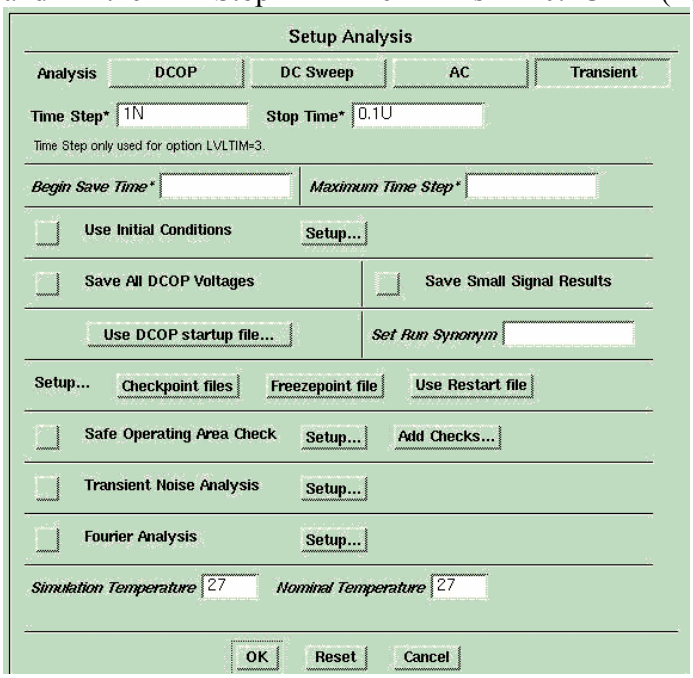
8. Now, let's run a simulation. Click on palette “DC Mode—RUN”. The status window will show "RUNNING" for a few moments. Wait for the "NOT RUNNI NG" message to appear. We now need to view the results.

9. Select the "A", "B" and "Out" nets, then click on palette “RESULT—CHART”, you should get the waveform chart for the “A”, “B” and “Out” nets in a new window. If you didn’t see this window, it may be hidden behind your schematic. Click to minimize your schematic window, you would be able to see the waveform window. Move the cursor over the plot. You will see the cursor values are displayed on the upper left window corner. This is very helpful for you to read the values of your signals. Does this plot agree with your knowledge of CMOS NAND gate?

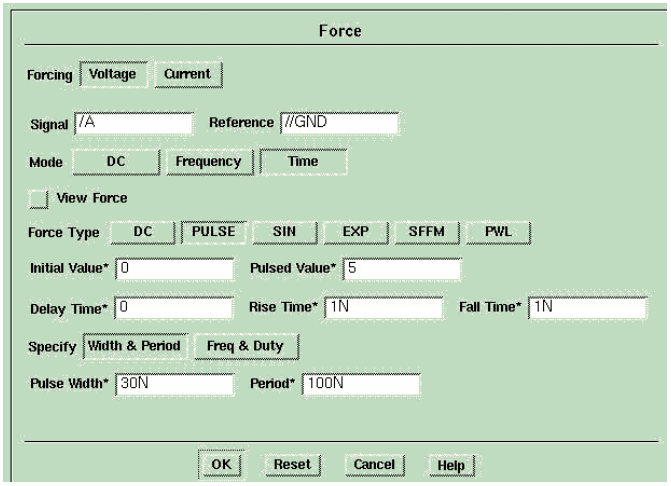


10. You may want to practice similar sweep simulation on net "B". Please note that you don't have to redefine any of the forces, just repeat the "Setup Analysis" with the "B" net selected. This will sweep net "B" instead of "A".
11. Now close the chart window by clicking on the icon on top left corner of your waveform window, and select “close” in the popup menu.

12. In the next steps, we will perform a transient (time domain) simulation on our circuit. First, click on palette “TIME MODE”. If this is the first time you launch a transient analysis you will get a setup window. In the popup window, check that the “Transient” button is pushed, the “Time Step” is 1N (1 nanosecond), and the “Stop Time” is 0.1U (100 Nanoseconds). Then click “OK”.

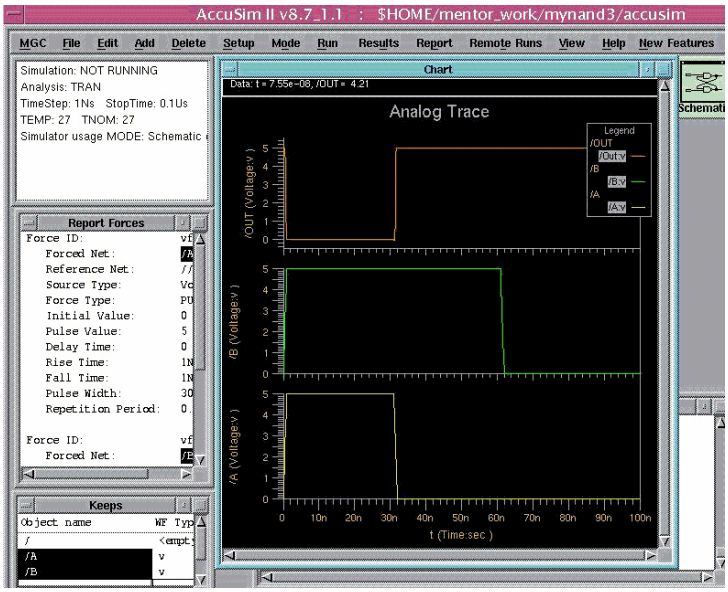


13. Delete all the previously defined forces by click on menu “Delete--Forces...--All signals—OK”.
10. Now we are going to add forces to inputs. Select the "A" network and click on palette “ADD FORCE”. In the popup window, click to choose a PULSE Force type. In the options, change the “Pulsed Value” to 5, “Pulse Width” to 30N, and the “Period” to 100N. Click on OK to close the window.
14. Repeat the above for net "B", with a Pulse Width of 60N (the rest should be the same). Click “OK”



15.Now click on palette “Time Mode—RUN”. The simulation will be started.

16.When the simulation is done, select "A", "B" and "Out" networks in your schematic, and click on palette “RESULT—TRACE”. You should have an analog trace waveform of the nodes “A”, “B” and “Out” you just selected. Does that output conform with your expectations from a NAND? If not, then what happened?



Congratulations, you have successfully finished Mentor Graphics tutorial. However, you still need to practice more on the Mentor Graphics tools to explore its functions. Please use the tools to design and simulate some other circuits. It will be very helpful for you to accumulate experience in it.

Reference

1. Matanya Elchanani, Mentor Graphics tutorial, http://www.bridgeport.edu/~matanya/vlsi/mentor.html.