METHODS AND TECHNIQUES FOR SEMICONDUCTOR CHARACTERIZATION

4200A–SCS PARAMATER ANALYZER APPLICATIONS GUIDE

KEITHLEY
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METHODS AND TECHNIQUES FOR SEMICONDUCTOR CHARACTERIZATION APPLICATIONS GUIDE

Tackle the challenges that can impede your measurements and introduce errors. The four application notes in this semiconductor characterization applications guide offer tips and techniques for insight and understanding of DC semiconductor device performance.

CONTENTS

Using the Model 4225-RPM Remote Amplifier/Switch to Automate Switching Between DC I-V, C-V, and Pulsed I-V Measurements

Characterizing a device, material, or process electrically often requires performing multiple types of measurements, including DC I-V, C-V, and pulsed I-V tests. The 4200A-SCS Parameter Analyzer can perform all of these measurements using a combination of 4200-SMU Source Measure Units, 4210-CVU C-V Module, and 4225-PMU Ultra-Fast I-V Module. Once, combining these diverse measurement capabilities into one system would have required re-cabling each module's output manually to the device under test (DUT) in between measurement types. The 4225-RPM Remote Amplifier/Switch solves this problem by acting as a multiplexer, making it possible to switch between precision DC SMUs, the CVU, or the Ultra-Fast I-V Modules automatically **(Figure 1.)**

Figure 1. 4200A-SCS with 4225-RPM Remote Amplifier/Switch accessories.

The 4225-RPM is an accessory for the 4225-PMU 2-Channel Ultra-Fast I-V Module. The 4225-RPM serves two purposes: to extend the 4225-PMU's current measurements down to the 100nA range and to allow switching between the 4200-SMU, 4210-CVU, and 4225-PMU without re-cabling. **The output terminals of each 4225-RPM in the system are connected to a single prober as shown in Figure 2**. The 4225-RPM can be mounted very close to the DUT, reducing cable capacitance effects. The input terminals of the 4225-RPM are connected to the modules in the 4200A-SCS.

This application note explains how to use the 4225-RPM to switch between the SMU, CVU, and PMU and make DC I-V, C-V, and pulsed I-V measurements on a single device. In particular, it describes hardware connections and how to use the system software, Clarius, to configure and execute tests.

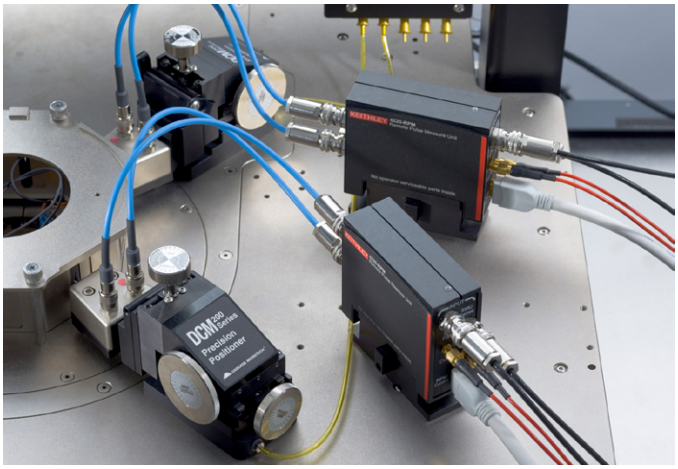

Figure 2. The output terminals of each 4225-RPM module connect to a single prober.

Making Connections

The SMUs, CVU, and PMU are connected to the input terminals of the RPM using the cables supplied with the instrument modules. The output terminals of the RPM are connected to the DUT. Either two or four-wire connections can be made. Each RPM comes with adaptors and one SMA cable for two-wire measurements. **Figure 3 shows the inputs and output connections of the 4225-RPM.**

Figure 3. Input and output connections of the 4225-RPM Remote Amplifier/Switch.

The schematic in Figure 4 illustrates the hardware connections from both the input and output terminals of the two 4225-RPMs. The DUT in this example is a diode.

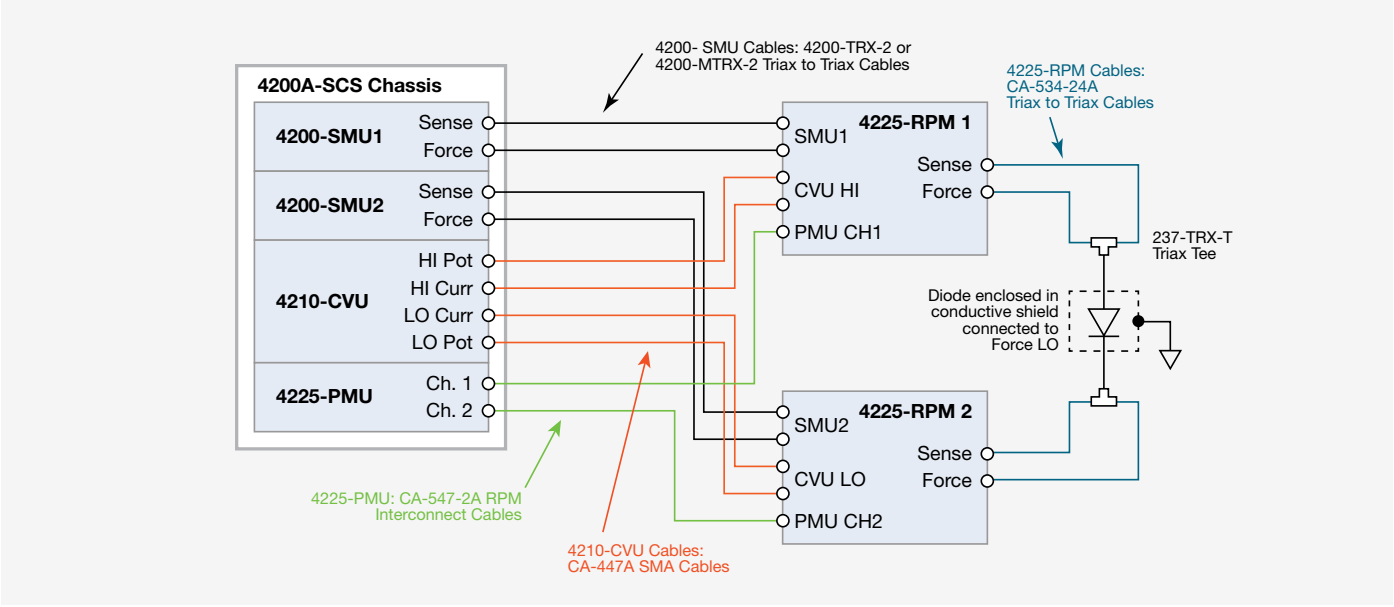

Figure 4. Connections from the 4200A-SCS and 4225-RPMs to the diode.

The output terminals of the two RPMs are connected to the diode in a four-wire configuration to provide the best measurement accuracy and eliminate the effects of the lead resistance on the I-V and C-V measurements. These connections are made using four 24-inch triax cables (Keithley part number CS-534-24A). These triax cables have the performance needed for both low current (I-V) and high frequency (C-V and pulsed I-V) measurements. The Force and Sense output terminals from 4225-RPM Ch1 are connected to the anode of the diode using two triax cables and a triax tee (237-TRX-T). The output terminals of 4225-RPM Ch2 are connected to the cathode of the diode. To prevent noisy measurements, the diode should be enclosed in a conductive shield that is connected to the Force LO terminal (the outside shield of the triax connector).

Updating the RPM Configuration in the KCON Application

The Keithley Configuration Utility (KCON) is used to manage and configure the 4200A-SCS, including the 4225-RPMs. Before using an RPM for automatic switching, it's essential to update the RPM configuration using the KCON application located on the 4200A-SCS desktop. This will properly associate the instruments connected to each RPM and will enable automatic switching between tests.

To update the configuration, follow these steps:

1. Make sure the device under test is disconnected from the outputs of the RPMs.
2. Close the Clarius application.
3. Open KCON (located on the desktop of the 4200A-SCS).
4. Select "Update Preamp, RPM and CVIV Configuration" **(see Figure 5.)**
5. Validate the configuration.
6. Save the configuration.
7. Close KCON application.

Figure 5. Update RPM configuration in KCON.

Setting Up the Measurements in the Clarius Application

Once the hardware connections are made and the RPMs are configured in KCON, open the Clarius application and create a project to switch automatically between DC I-V, C-V, and pulsed I-V measurements. Basically, just Select, Configure and Analyze the measurements. In the following paragraphs, these three easy steps are described for creating a project to characterize a diode; however, the same procedure can be followed for other devices and tests, depending upon the application.

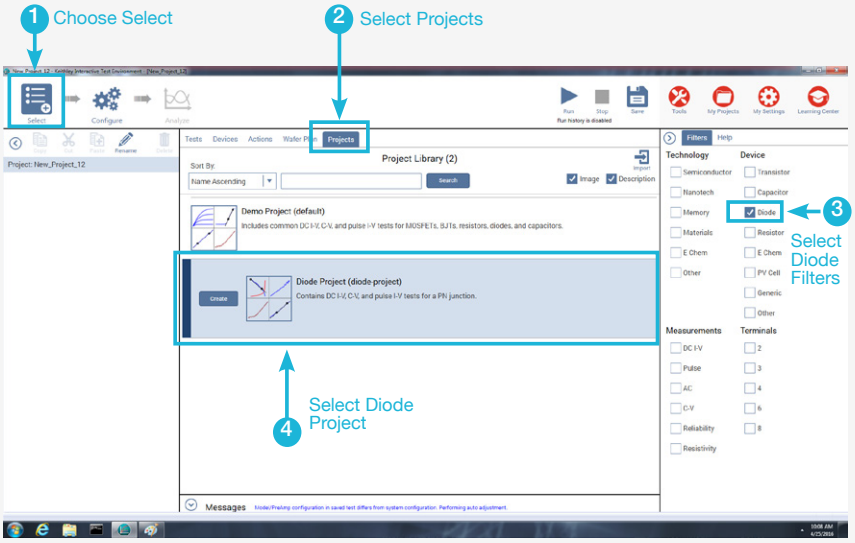

Figure 6. Select the diode project.

Select the Diode Project (Figure 6).

Choose Select in the top left corner of the screen. In the Library, select the Projects tab. Select the Diode in the Filters pane on the right-hand side of the screen. Select the Diode Project in the Project Library and create a new project when prompted.

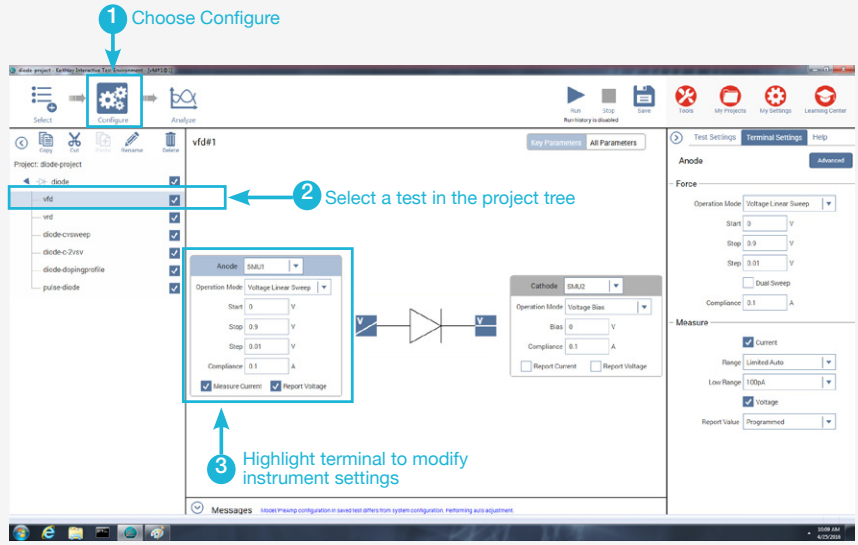

Figure 7. Configure tests in the diode project.

Configure the Tests (Figure 7).

The Diode Project has tests for measuring I-V, C-V, and pulsed I-V. Each test can be opened up and configured based upon the test requirements. To configure each test, choose Configure in the top left-hand corner of the screen. Highlight the test to be configured. Highlight the terminal to modify the instrument settings. More detailed settings can be found in the Test Settings and Terminal Settings tabs on the right-hand side of the screen.

Analyze the Results (Figure 8).

Once the tests are configured, the three tests can be executed consecutively. Start by selecting Analyze in the top left corner of the screen. This will bring up the Analyze pane in the center of the screen. To execute the tests sequentially, highlight the device in the project tree and then select Run at the top of the screen. The tests will begin to run sequentially from the top of the project tree. The RPMs will automatically switch the instrument outputs based on the test being executed.

The screen shown in Figure 8 allows viewing the data in tabular format at the top of the pane or graphically at the bottom. This screen can also be configured for viewing only the data or the graph. On the right-hand side of the screen, the Run History pane allows selecting and analyzing the data and graphs taken from any previous executions of the test.

Figure 8. Analyze the test results.

Conclusion

Fully characterizing a device often requires precision DC I-V, C-V, and pulsed I-V measurements. Re-cabling between measurements can be a time-consuming manual process. The 4225-RPM Remote Amplifier/Switch option for the 4225-PMU supports automatic switching between the PMU, CVU, and SMU modules installed in the 4200A-SCS chassis, saving valuable time and avoiding the potential for re-cabling errors.

An Ultra-Fast Single Pulse (UFSP) Technique for Channel Effective Mobility Measurement

Introduction

The channel effective mobility (μ_{eff}) influences the MOSFET performance through the carrier velocity and the driving current. It is one of the key parameters for complementary metal-oxide-semiconductor (CMOS) technologies. It is widely used for benchmarking different processes in technology development and material selection [1, 2]. It is also a fundamental parameter for device modelling [3]. With device scaling down to the nano-size regime and the introduction of new dielectric materials, the conventional measurement technique for mobility evaluation encountered a number of problems described in the following section, leading to significant measurement errors. As a result, a new mobility extraction technique is needed.

This application note describes a novel Ultra-Fast Single Pulse technique (UFSP) [4, 5] for accurate mobility evaluation, including the technique principle, how to connect the device, and how to use the Clarius software in the 4200A-SCS Parameter Analyzer.

Conventional Mobility Measurement and Challenges

We use a p-channel device of gate length L and width W as an example. When the channel charge is fairly uniform from source to drain in the linear region, the channel effective mobility (μ_{eff}) can be written as

$$\mu_{eff} = \frac{L}{W} \cdot \frac{I_{ch}}{Q_i \cdot V_d}$$

where V_d is a small bias applied on the drain terminal of the device, Q_i is the mobile channel charge density (C/cm^2), and I_{ch} is the conduction current flowing in the channel.

Traditionally, I_{ch} is measured at the drain terminal of the device with the configuration shown in **Figure 1(a)**. Q_i is extracted from integrating the measured gate-to-channel capacitance, C_{gc}, with respect to V_g, i.e.,

$$Q_i = \int_{+\infty}^{V_g} C_{gc} dV_g$$

by using the connection configuration shown in **Figure 1(b)**.

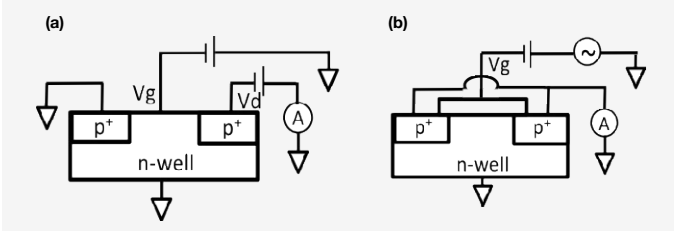

Figure 1. Configuration for (a) conduction current measurement and (b) gate-to-channel capacitance, C_{gc}, measurement.

The principle of conventional mobility measurement is deceptively simple. However, many challenges and pitfalls are associated with this testing. Several sources of error are often ignored in the past.

V_d-dependence: The conventional technique applies a non-zero V_d (usually 50mV–100mV) for I_{ch} measurement but a zero V_d for Q_i measurement. This difference in V_d used in two measurements can lead to significant errors in evaluating mobility for thin oxides, especially in the low electric field region. One example is given in **Figure 2**, where a higher $|V_d|$ results in a substantial reduction of mobility near its peak. This is because $|V_g–V_d|$ reduces for high $|V_d|$, so that the real charge carrier density for the I_{ch} is smaller than the Q_i measured at $V_d = 0$.

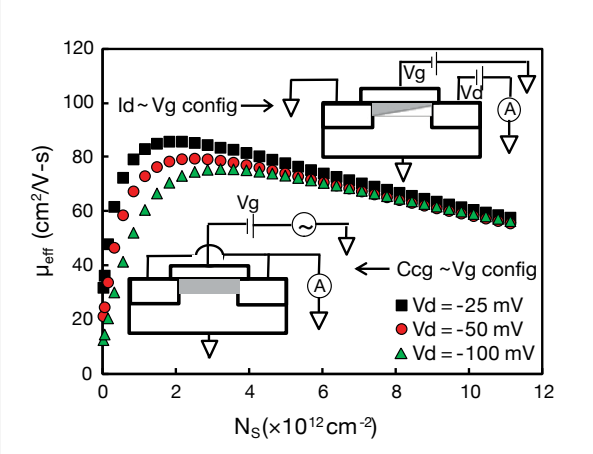

Figure 2. Effective channel mobility measured by conventional technique. I_{ch} was measured under various non-zero drain biases, V_{DS}, but Q_i was measured under $V_d = 0$. The extracted mobility clearly reduces for higher $|V_d|$. Insets illustrate the carrier distribution in the channel.

Charge Trapping: The conventional technique used slow measurement with typical measurement time in seconds. The fast charge trapping becomes significant for both thin SiON and high-k dielectric. For slow measurements, trapping can respond during the measurement and give rise to hysteresis and stretch-out of the C_{gc}–V_g curve and a reduction of I_{ch}. This results in an underestimation of mobility.

Leaky Dielectric: As gate oxide is downscaled, high gate leakage current becomes a main challenge for mobility extraction. It affects both I_{ch} and Q_i measurements and in turn the mobility. To minimize its impact on C_{gc} measurement, frequencies up to gigahertz have been used, which requires devices with an RF structure. The RF structure requires more processing and die space and is not always available.

Cable Switching: The conventional technique involves cable changing between I_{ch} and Q_i measurements. This slows down the measurement and can potentially cause breakdown of the device under test.

The Ultra-Fast Single Pulse Technique (UFSP Technique)

To overcome the challenges mentioned above, a novel technique called the Ultra-Fast Single Pulse technique (UFSP) has been developed and is described as follows.

A p-channel device is used here for illustrating the working principle of the UFSP technique as shown in **Figure 3**. The considerations for n-channel devices are similar. To perform the UFSP measurement, a single pulse with edge time of several microseconds is applied on the gate terminal of the device. The gate voltage sweeps toward negative during the falling edge of the pulse and turns the device on. The transient currents are recorded at both the source and the drain terminal of the device. The device is then switched off during the subsequent rising edge where the gate voltage sweeps toward positive. The corresponding transient currents are also to be recorded. Channel effective mobility can be extracted from these four transient currents measured within several microseconds.

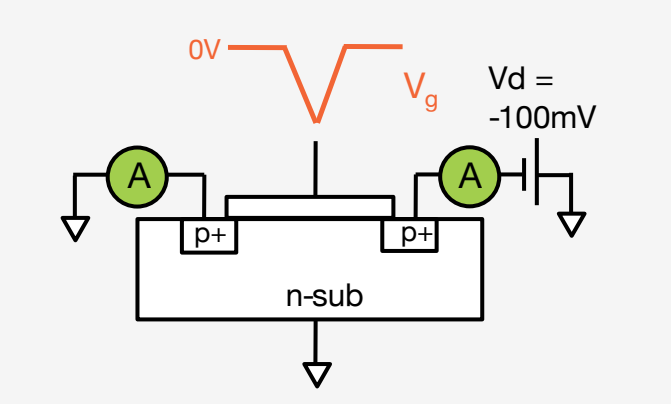

Figure 3. Illustration of the working principle of UFSP technique.

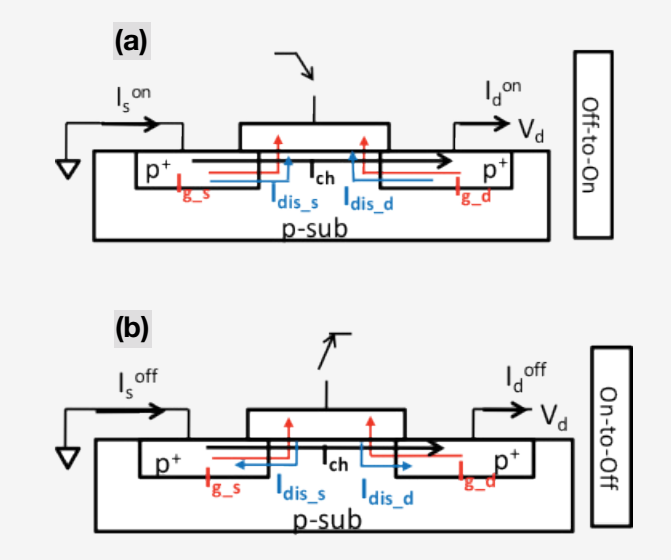

Figure 4. Schematic diagram of current flow during the transient measurement.

To facilitate the analysis, we define currents measured at drain and source terminal during switching on and off as I_d^{on}, I_s^{on}, I_d^{off}, and I_s^{off}. The current flow in the channel during the transient measurement is shown in **Figure 4 (a)** and **(b)**. Three types of current are present: channel conduction current, I_{ch}, displacement current between gate and source/drain, I_{dis_s} and I_{dis_d}, and the leakage current between gate and source/drain, I_{g_s} and I_{g_d}. When device is switched off-to-on, the direction of I_{dis_s} and I_{dis_d} is toward the channel center; I_{dis_s} has the same direction as I_{ch} at the source, but I_{dis_d} is in opposite direction to I_{ch} at the drain. When the device is switched on-to-off, I_{dis_s} and I_{dis_d} change direction, but I_{ch} does not. I_{g_s} and I_{g_d} are independent of the V_g sweep direction and always flow from the source and drain towards gate under negative V_g. Based on the above analysis, channel current, I_{ch}, gate current, I_g, and displacement current, I_{dis} can be separated by using Equations (2)–(4). C_{gc} can be calculated using (5).

$$I_{CH} = \frac{I_D^{ON} + I_D^{OFF} + I_S^{ON} + I_S^{OFF}}{4} \quad (2)$$

$$I_G = I_{G\_S} + I_{G\_D} = \frac{I_S^{ON} + I_S^{OFF} - I_D^{ON} - I_D^{OFF}}{2} \quad (3)$$

$$I_{DIS} = I_{DIS\_S} + I_{DIS\_D} = \frac{I_D^{OFF} - I_D^{ON} + I_S^{ON} - I_S^{OFF}}{2} \quad (4)$$

$$C_{GC} = \frac{I_{DIS}}{dV_G/dt} \quad (5)$$

To calibrate the UFSP technique, a p-channel MOSFET with thick oxide is used that has negligible I_G current. The measurement time (=edge time) is set at 3µs. The measured four currents are shown in **Figure 5**. The I_{ch}, I_g and C_{gc} extracted by using Equations (2) to (5) are shown in **Figure 6(a)**. Once C_{gc} and I_{ch} are evaluated accurately, Q_i can be obtained by integrating C_{gc} against V_g and channel effective mobility, μ_{eff}, is calculated through Equation (1) as shown in **Figure 6(b)**.

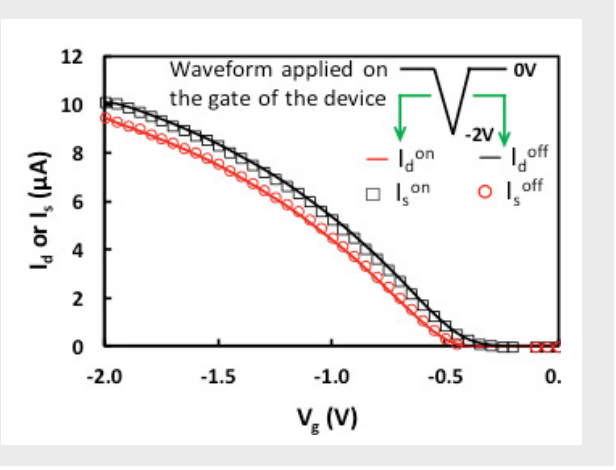

Figure 5. Four currents measured from source and drain corresponding to the off-to-on and on-to-off Vg sweep. Schematic Vg waveform is shown in inset.

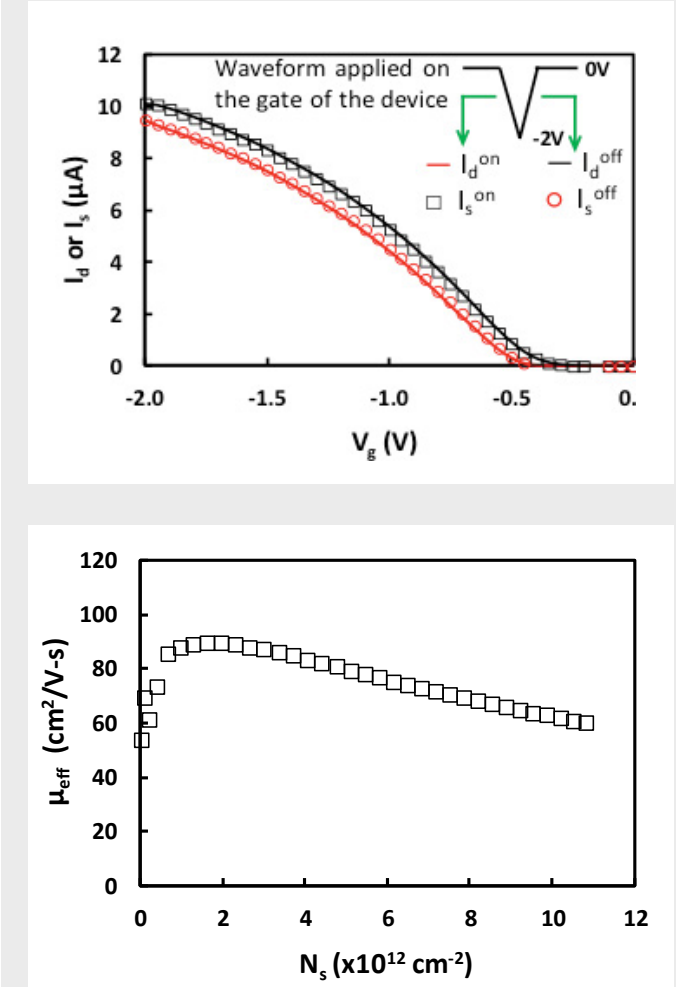

Figure 6. (a) I_{ch}, I_g, and C_{gc} extracted simultaneously from the currents in Figure 5 by using Equations (2)–(5). (b) Channel effective mobility extracted from I_{ch} and C_{gc} from (a).

Because the UFSP measured I_{ch} and C_{gc} under the same V_d, μ_{eff} should be independent of V_d. The μ_{eff} evaluated under three different V_d biases is compared in **Figure 7**. Good agreements are obtained confirming that the errors induced by V_d using the conventional techniques have been removed.

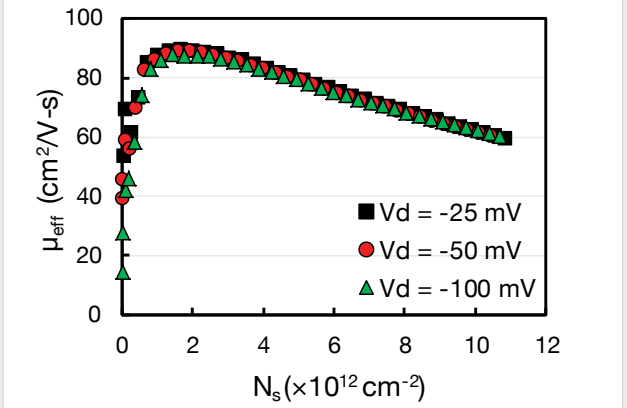

Figure 7. The effective channel mobility, μ_{eff}, extracted under three different V_d by using UFSP technique.

The UFSP also works well on leaky gate dielectric of standard structure. When it was applied on one 'leaky' n-channel MOSFET with an EOT of 1.28nm, the four currents measured from the source and drain terminals corresponding to the off-to-on and on-to-off V_G sweep are shown in **Figure 8 (a)**. By using Equations (2)–(5), I_{ch} ('□'), I_g ('o') and C_{gc} ('x') are extracted and plotted in **Figure 8 (b)**. I_g from DC measurement is also plotted for comparison in **Figure 8 (b)**. Good agreement is obtained. **Figure 8 (c)** shows that electron mobility can be reliably measured for this leaky device where Ig is as high as 45A/cm². Because the UFSP can tolerate high gate leakage, it does not require the use of the special RF structure for mobility evaluation.

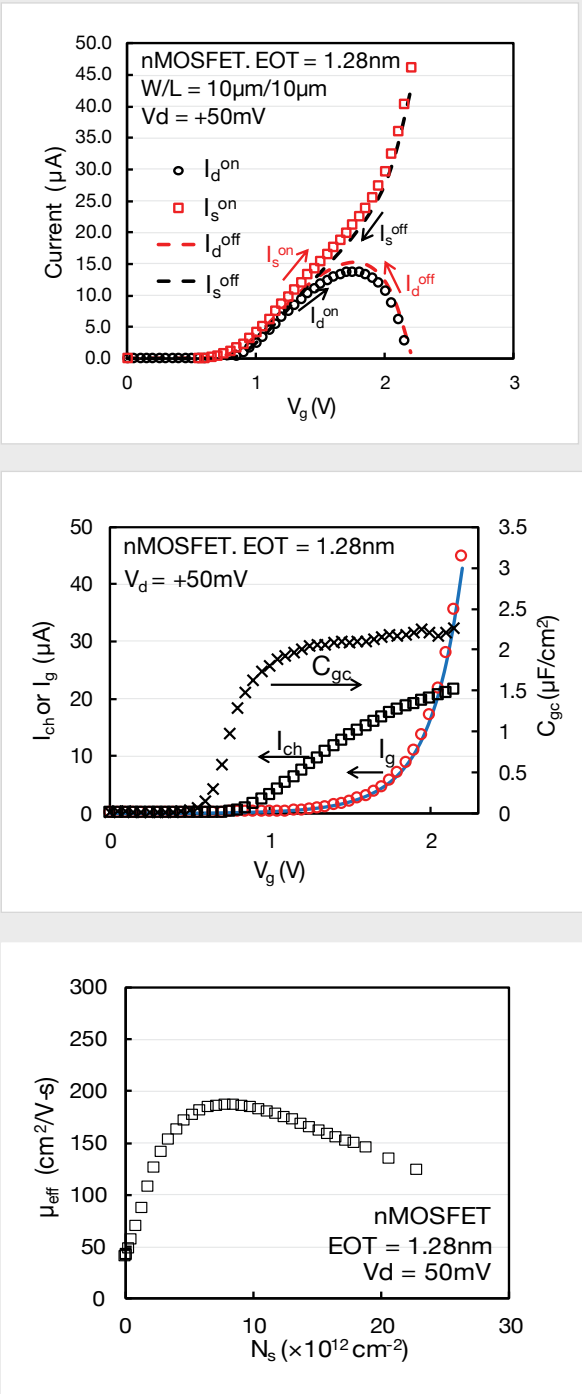

Figure 8. (a) Four currents measured from the source and drain corresponding to the off-to-on and on-to-off V_g sweeps by UFSP technique on an nMOSFET with EOT of 1.28nm.

(b) I_{ch} ('□'), I_g ('o') and C_{gc} ('x') are extracted from the currents in (a) with Equations (2)-(5). The blue line is the leakage current obtained by DC measurement.

(c) Channel effective mobility, μ_{eff}, is calculated by using the extracted I_{ch} and C_{gc} with Eqn (1).

To demonstrate the applicability of UFSP to devices with significant charge trapping, one pMOSFET with an HfO_2/SiO_2 stack was used. Large amount of traps locate close to the Si/SiO_2 interface in this dielectric stack and they can exchange charges with the substrate rapidly. The conventional technique takes seconds, making them indistinguishable from channel mobile charges. As a result, inversion charges will be overestimated and in turn the channel effective mobility will be underestimated. The UFSP technique only takes microseconds, minimizing charge trapping effect. **Figure 9** compares the mobility extracted by these two techniques. It clearly shows that after suppressing the trapping, the mobility extracted from the UFSP is considerably higher than that by the conventional technique.

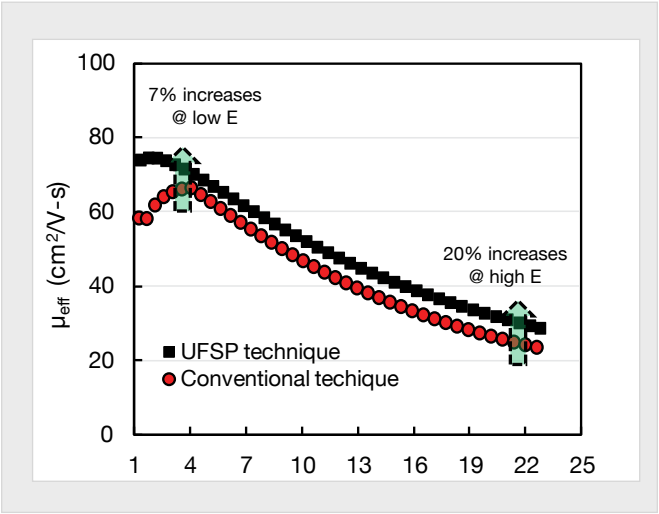

Figure 9. A comparison of mobility extracted by UFSP and conventional technique for a device with HfO_2/SiON dielectric of considerable fast trapping.

Required Hardware for UFSP Measurement

Selecting appropriate measurement equipment is critical to the successful implementation of theh ultra-fast single pulse method. The following hardware is required:

- One Model 4200A-SCS Parameter Analyzer, with
- Two Ultra-Fast I-V Modules (4225-PMU);
- Four Remote Amplifier/Switches (4225-RPM);
- 4 High Performance Triaxial Cable Kits (4210-MMPC-C).

A photo of the cabling configuration for the test is shown in **Figure 10.** The 4225-PMU is the latest addition to the growing range of instrumentation options for the 4200A-SCS Parameter Analyzer. The module integrates ultra-fast voltage waveform generation and signal observation capabilities into the 4200A-SCS's already powerful test environment to deliver unprecedented I-V testing performance. It makes ultra-fast I-V sourcing and measurement as easy as making DC measurements with a traditional high resolution source measure unit (SMU) instrument. Each plug-in 4225-PMU module provides two channels of integrated sourcing and measurement. Each channel of the 4225-PMU combines high speed voltage outputs (with pulse widths ranging from 60 nanoseconds to DC) with simultaneous current and voltage measurements. The 4225-RPM Remote Amplifier/Switch further expands the 4225-PMU's capabilities by providing ultra-low current measurement (below 100nA) and reducing cable capacitance effects.

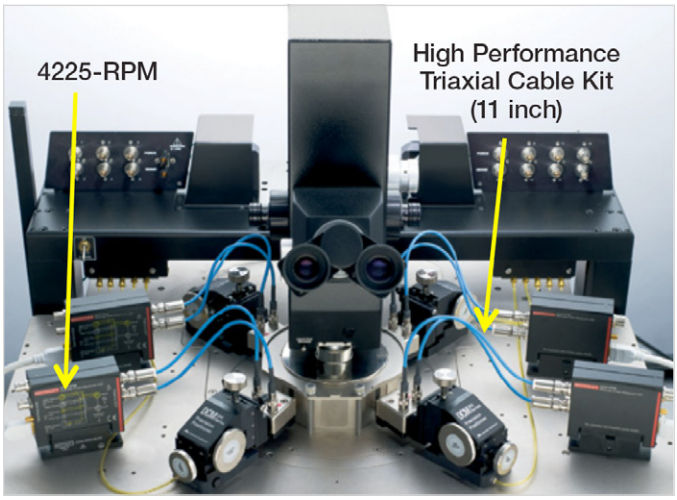

Figure 10. UFSP technique setup.

Connections to the Device

The connection for the UFSP measurement is shown in **Figure 11.** Each terminal of the device is connected to one 4225-RPM using two 11-inch triaxial cables (provided in the cable set 4210-MMPC-C). Then each 4225-RPM is connected to one channel of the PMU using two triaxial cables. All the measurements are controlled by the Clarius software.

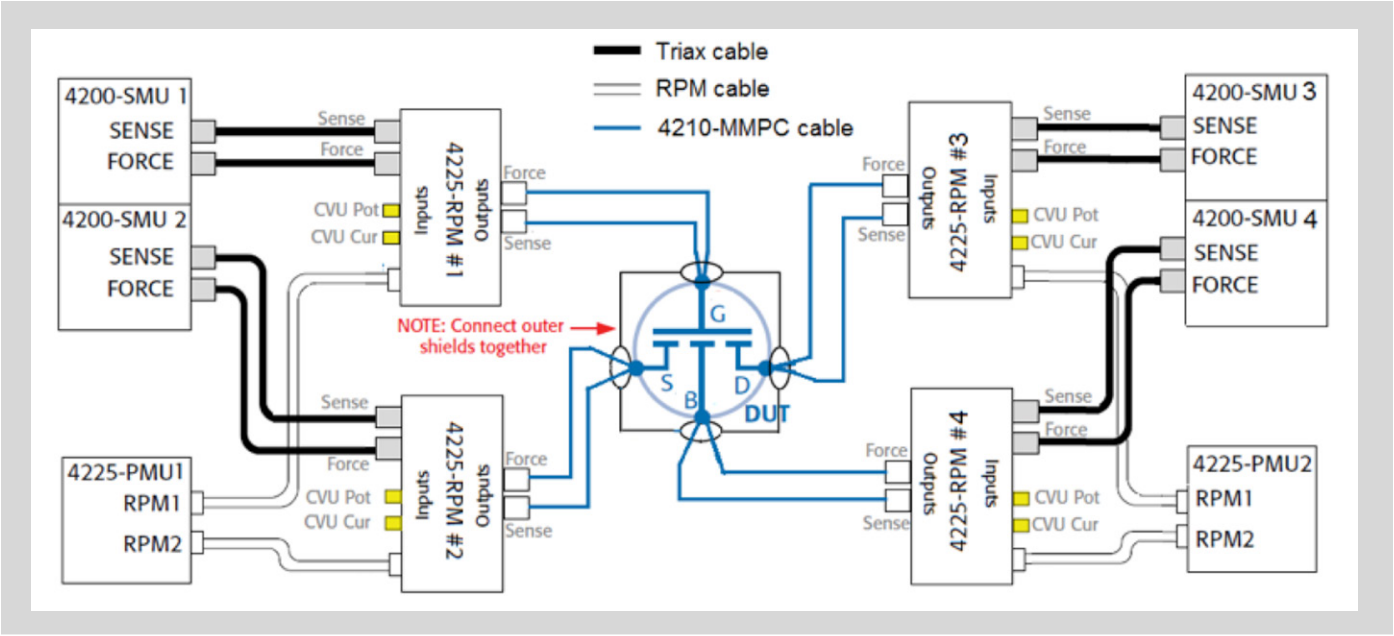

Figure 11. Experiment connection for the Ultra-fast Single Pulse (UFSP) technique. Two Keithley dual-channel 4225-PMUs are used for performing transient measurements. Four Keithley 4225-RPMs are used to reduce cable capacitance effect and achieve accurate measurement below 100nA.

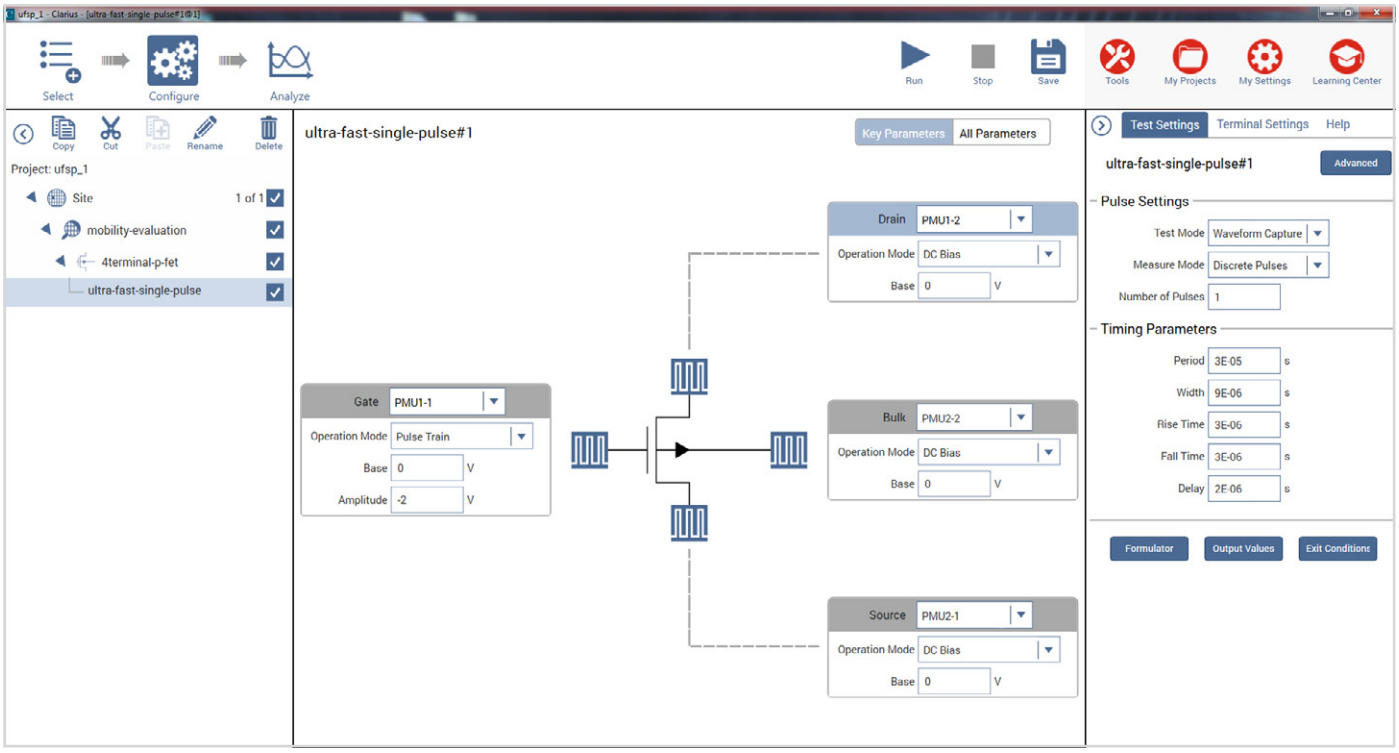

Figure 12. Example project in the Clarius software for UFSP measurement. Each of the four terminals of the device is connected to one channel of PMU respectively.

Using Clarius Software to Perform UFSP Measurements

Performing UFSP for channel effective mobility measurement using the 4200A-SCS system is quite simple. An example project is included with the system. As shown in **Figure 12**, each terminal of the device is connected to one channel of the PMU. Users can modify the parameters for each PMU channel in the definition tab. **Table 1** lists one set of user-defined parameters for a p-channel MOSFET.

In the Test Setings pane, users can input the desired measurement speed which is the edge time of the pulse. The recommended values are listed in **Table 2.**

Table 1. Recommended settings in the definition tab for each channel of the PM

PMU Setting for Gate Terminal			
Parameters		**Value**	**Description**
Pulse Train Settings	Forcing Function	Pulse Train	To generate a single pulse or a pulse train with same shape
	Voltage Amplitude	–2V	To define the Vg sweep range
	Voltage Base	0V	
Measurement Range	Vrange	10V	Maximum possible voltage applied on the gate
	Irange	10µA	Measurement range for current
Measurement Setting	Sample I waveform	untick	Do not record current at the gate
	Sample V waveform	tick	Record applied voltage at the gate
	Timestamp	tick	Record total time for the measurement

PMU Setting for Drain Terminal			
Parameters		**Value**	**Description**
Pulse Train Settings	Forcing Function	Pulse Train	To generate a single pulse or a pulse train with the same shape
	Pulse Train Settings	DC voltage	To apply a constant Vd bias used for mobility measurement
	Voltage base (V)	–0.1	
Measurement Range	Vrange	10V	Maximum possible voltage applied on the gate
	Irange	10µA	Measurement range for current
Measurement Setting	Sample I waveform	tick	Record current at the drain
	Sample V waveform	untick	Do not record applied voltage at the drain
	Timestamp	untick	Do not record total time for the measurement

PMU Setting for Source Terminal			
Parameters		**Value**	**Description**
	Forcing Function	Pulse Train	To generate a single pulse or a pulse train with the same shape
	Pulse Train Settings	DC voltage	To apply a zero Vs bias used for mobility measurement
	Voltage base (V)	0	
Measurement Range	Vrange	10V	Maximum possible voltage applied on the gate
	Irange	10µA	Measurement range for current
Measurement Setting	Sample I waveform	tick	Record current at the source
	Sample V waveform	untick	Do not record applied voltage at the source
	Timestamp	untick	Do not record total time for the measurement

PMU Setting for Bulk Terminal			
Parameters		**Value**	**Description**
	Forcing Function	Pulse Train	To generate a single pulse or a pulse train with the same shape
	Pulse Train Settings	DC voltage	To apply a zero Vbulk bias used for mobility measurement
	Voltage base (V)	0	
Measurement Setting	Sample I waveform	untick	Do not record current at the bulk
	Sample V waveform	untick	Do not record applied voltage at the bulk
	Timestamp	untick	Do not record total time for the measurement

Table 2. Recommended settings in the timing tab.

Parameters	Value	Description
Test Mode	Waveform capture	
Measurement Mode	Discrete Pulses	Discrete Pulse and Average pulses, then you need to input number of Pulses, 10 is enough.
Sweep parameter	None	No sweeping required
Period (s)	5.00E-05	Period of the pulse
Width (s)	6.00E-06	Pulse width
Rise Time (s)	3.00E-06	Pulse rise time
Fall Time (s)	3.00E-06	Pulse fall time, set to be the same as rise time
Pulse Delay (s)	2.00E-06	Pulse delay time, keep the same as rise time

Once the test is executed, transient currents during switching on and off at source and drain terminals will be recorded and stored in the sheet and can be saved as an .xls file. These currents can also be plotted on the graph tab. From these currents, the channel effective mobility can be extracted based on Equations (2) to (5).

Conclusion

Channel carrier mobility is a key parameter for material selection and process development. The conventional technique suffers from several shortcomings: slow speed and vulnerability to fast trapping, V_d-dependence, cable-changing, sensitivity to gate leakage, and a complex procedure. An ultra-fast single pulse technique (UFSP) has been proposed and developed to overcome these shortcomings. I_{CH} and Q_i can be simultaneously measured within several microseconds without cable switching. UFSP measurement can be easily performed using the 4200A-SCS Parameter Analyzer with two 4255-PMUs and four 4225-RPMs. It provides a complete solution for robust and accurate mobility evaluation in a convenient way and serves as a tool for process development, material selection, and device modelling for CMOS technologies.

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Acknowledgements

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C-V Characterization of MOS Capacitors Using the 4200A-SCS Parameter Analyzer

Introduction

Maintaining the quality and reliability of gate oxides of MOS structures is a critical task in a semiconductor fab. Capacitance-voltage (C-V) measurements are commonly used in studying gate-oxide quality in detail. These measurements are made on a two-terminal device called a MOS capacitor (MOS cap), which is basically a MOSFET without a source and drain. C-V test results offer a wealth of device and process information, including bulk and interface charges. Many MOS device parameters, such as oxide thickness, flatband voltage, threshold voltage, etc., can also be extracted from the C-V data.

Using a tool such as the Keithley 4200A-SCS equipped with the 4210-CVU Integrated C-V Option for making C-V measurements on MOS capacitors can simplify testing and analysis. The 4200A-SCS is an integrated measurement system that can include instruments for both I-V and C-V measurements, as well as software, graphics, and mathematical analysis capabilities. The software incorporates C-V tests, which include a variety of complex formulas for extracting common C-V parameters.

This application note discusses how to use a Keithley 4200A-SCS Parameter Analyzer equipped with the 4210-CVU Integrated C-V Option to make C-V measurements on MOS capacitors. It also addresses the basic principles of MOS caps, performing C-V measurements on MOS capacitors, extracting common C-V parameters, and measurement techniques. The Keithley Clarius software that controls the 4200A-SCS incorporates many tests and projects specific to C-V testing. Each project is paired with the formulas necessary to extract common C-V parameters, such as oxide capacitance, oxide thickness, doping density, depletion depth, Debye length, flatband capacitance, flatband voltage, bulk potential, threshold voltage, metal-semiconductor work function difference, and effective oxide charge. This completeness is in sharp contrast to other commercially available C-V solutions, which typically require the user to research and enter the correct formula for each parameter manually.

Overview of C-V Measurement Technique

By definition, capacitance is the change in charge (Q) in a device that occurs when it also has a change in voltage (V):

$$C \equiv \frac{\Delta Q}{\Delta V}$$

One general practical way to implement this is to apply a small AC voltage signal (millivolt range) to the device under test, and then measure the resulting current. Integrate the current over time to derive Q and then calculate C from Q and V.

C-V measurements in a semiconductor device are made using two simultaneous voltage sources: an applied AC voltage signal (dV_{ac}) and a DC voltage (V_{dc}) that is swept in time, as illustrated in **Figure 1**.

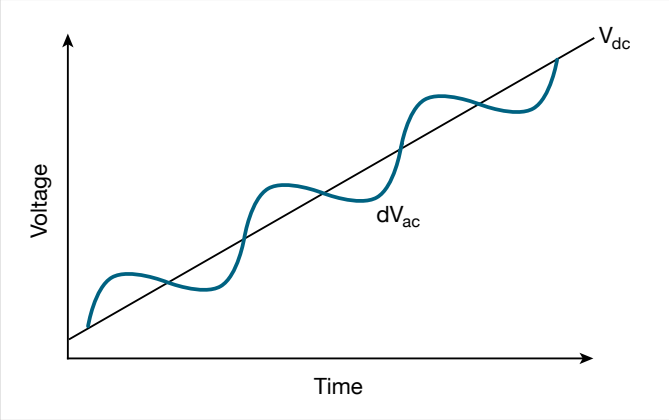

Figure 1. AC and DC voltage of C-V Sweep Measurement

The magnitude and frequency of the AC voltage are fixed; the magnitude of the DC voltage is swept in time. The purpose of the DC voltage bias is to allow sampling of the material at different depths in the device. The AC voltage bias provides the small-signal bias so the capacitance measurement can be performed at a given depth in the device.

Basic Principles of MOS Capacitors

Figure 2 illustrates the construction of a MOS capacitor. Essentially, the MOS capacitor is just an oxide placed between a semiconductor and a metal gate. The semiconductor and the metal gate are the two plates of the capacitor. The oxide functions as the dielectric. The area of the metal gate defines the area of the capacitor.

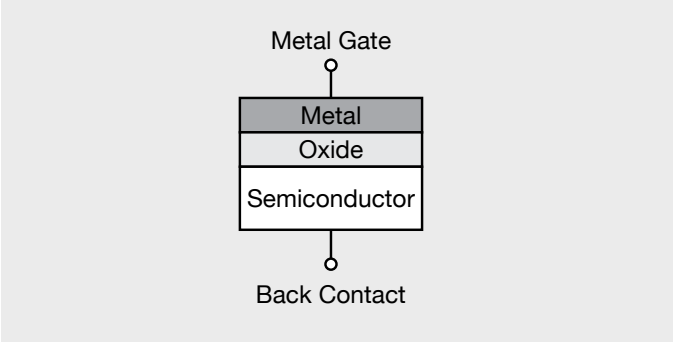

Figure 2. MOS capacitor

The most important property of the MOS capacitor is that its capacitance changes with an applied DC voltage. As a result, the modes of operation of the MOS capacitor change as a function of the applied voltage. **Figure 3** illustrates a high frequency C-V curve for a p-type semiconductor substrate. As a DC sweep voltage is applied to the gate, it causes the device to pass through accumulation, depletion, and inversion regions.

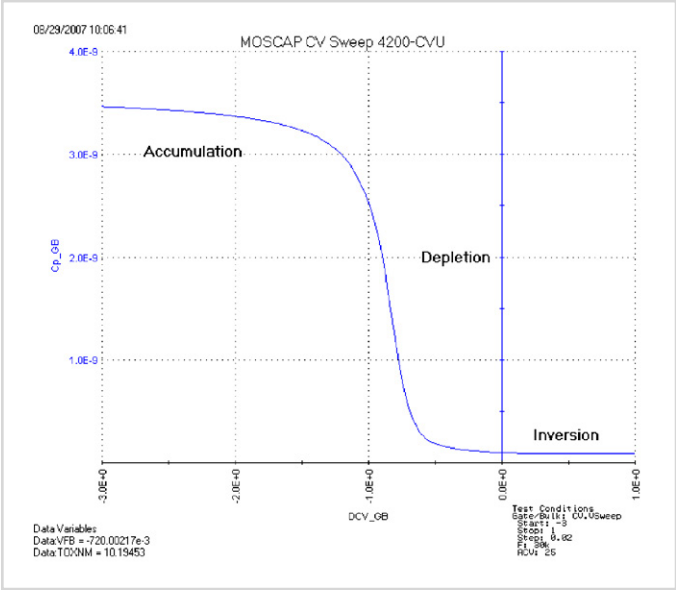

Figure 3. C-V curve of a p-type MOS capacitor measured with the 4210-CVU

The three modes of operation, accumulation, depletion and inversion, will now be discussed for the case of a p-type semiconductor, then briefly discussed for an n-type semiconductor at the end of this section.

Accumulation Region

With no voltage applied, a p-type semiconductor has holes, or majority carriers, in the valence band. When a negative voltage is applied between the metal gate and the semiconductor, more holes will appear in the valence band at the oxide-semiconductor interface. This is because the negative charge of the metal causes an equal net positive charge to accumulate at the interface between the semiconductor and the oxide. This state of the p-type semiconductor is called accumulation.

For a p-type MOS capacitor, the oxide capacitance is measured in the strong accumulation region. This is where the voltage is negative enough that the capacitance is essentially constant and the C-V curve is almost flat. This is where the oxide thickness can also be extracted from the oxide capacitance. However, for a very thin oxide, the slope of the C-V curve doesn't flatten in accumulation and the measured oxide capacitance differs from the actual oxide capacitance.

Depletion Region

When a positive voltage is applied between the gate and the semiconductor, the majority carriers are replaced from the semiconductor-oxide interface. This state of the semiconductor is called depletion because the surface of the semiconductor is depleted of majority carriers. This area of the semiconductor acts as a dielectric because it can no longer contain or conduct charge. In effect, it becomes an insulator.

The total measured capacitance now becomes the oxide capacitance and the depletion layer capacitance in series, and as a result, the measured capacitance decreases. This decrease in capacitance is illustrated in **Figure 3** in the depletion region. As a gate voltage increases, the depletion region moves away from the gate, increasing the effective thickness of the dielectric between the gate and the substrate, thereby reducing the capacitance.

Inversion Region

As the gate voltage of a p-type MOS-C increases beyond the threshold voltage, dynamic carrier generation and recombination move toward net carrier generation. The

positive gate voltage generates electron-hole pairs and attracts electrons (the minority carriers) toward the gate. Again, because the oxide is a good insulator, these minority carriers accumulate at the substrate-to-oxide/well-to-oxide interface. The accumulated minority-carrier layer is called the inversion layer because the carrier polarity is inverted. Above a certain positive gate voltage, most available minority carriers are in the inversion layer, and further gate-voltage increases do not further deplete the semiconductor. That is, the depletion region reaches a maximum depth.

Once the depletion region reaches a maximum depth, the capacitance that is measured by the high frequency capacitance meter is the oxide capacitance in series with the maximum depletion capacitance. This capacitance is often referred to as minimum capacitance. The C-V curve slope is almost flat.

NOTE: The measured inversion-region capacitance at the maximum depletion depth depends on the measurement frequency. Therefore, C-V curves measured at different frequencies may have different appearances. Generally, such differences are more significant at lower frequencies and less significant at higher frequencies.

n-type Substrate

The C-V curve for an n-type MOS capacitor is analogous to a p-type curve, except that (1) the majority carriers are electrons instead of holes; (2) the n-type C-V curve is essentially a mirror image of the p-type curve; (3) accumulation occurs by applying a positive voltage to the gate; and (4) the inversion region occurs at negative voltage.

Performing C-V Measurements with the 4210-CVU

To simplify testing, a project has been created for the 4200A-SCS that makes C-V measurements on a MOS capacitor and extracts common measurement parameters such as oxide thickness, flatband voltage, threshold voltage, etc. The *MOS Capacitor C-V Project* (*cvu-moscap*) is included with all 4200A-SCS systems in the Clarius application. **Figure 4** is a screen shot of the project, which has three tests that generate a C-V sweep *(moscap-cvsweep)*, a $1/C^2$ vs. Gate Voltage curve *(moscap-c-2vsv)*, and a doping profile *(moscap-dopingprofile)*. **Figure 4** also illustrates a C-V sweep generated with the *moscap-cvsweep* test. All of the extracted C-V parameters in these test modules are defined in the next section of this application note.

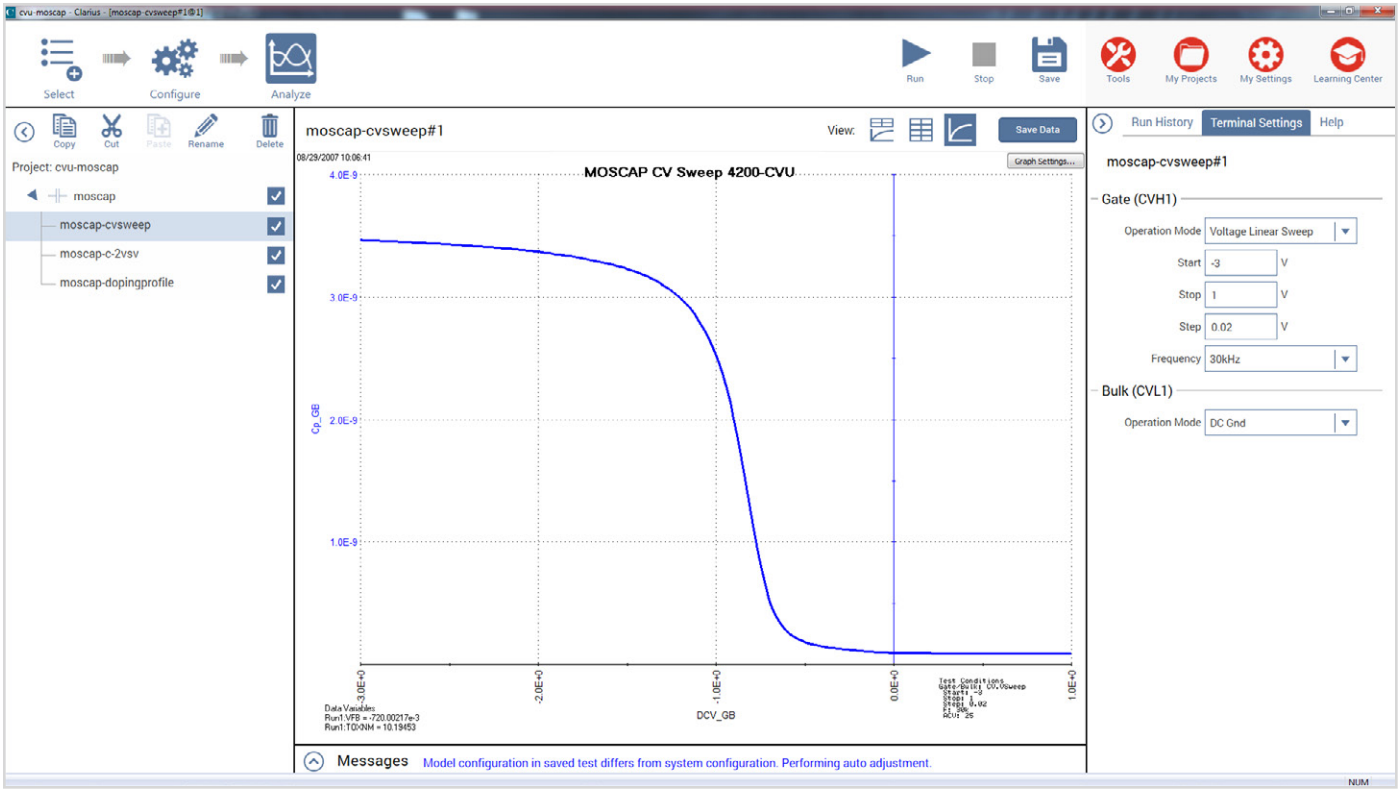

Figure 4. C-V sweep created with *moscap-cvsweep* test for the 4200A.

MOS Capacitor C-V Sweep (*moscap-cvsweep*) Test

This test performs a capacitance measurement at each step of a user-configured linear voltage sweep. A C-V graph is generated from the acquired data, and several device parameters are calculated using the Formulator, which is a tool in the 4200A-SCS's software that provides a variety of computational functions, common mathematical operators, and common constants. **Figure 5** shows the window of the Formulator. These derived parameters are listed in the Analyze view of the test.

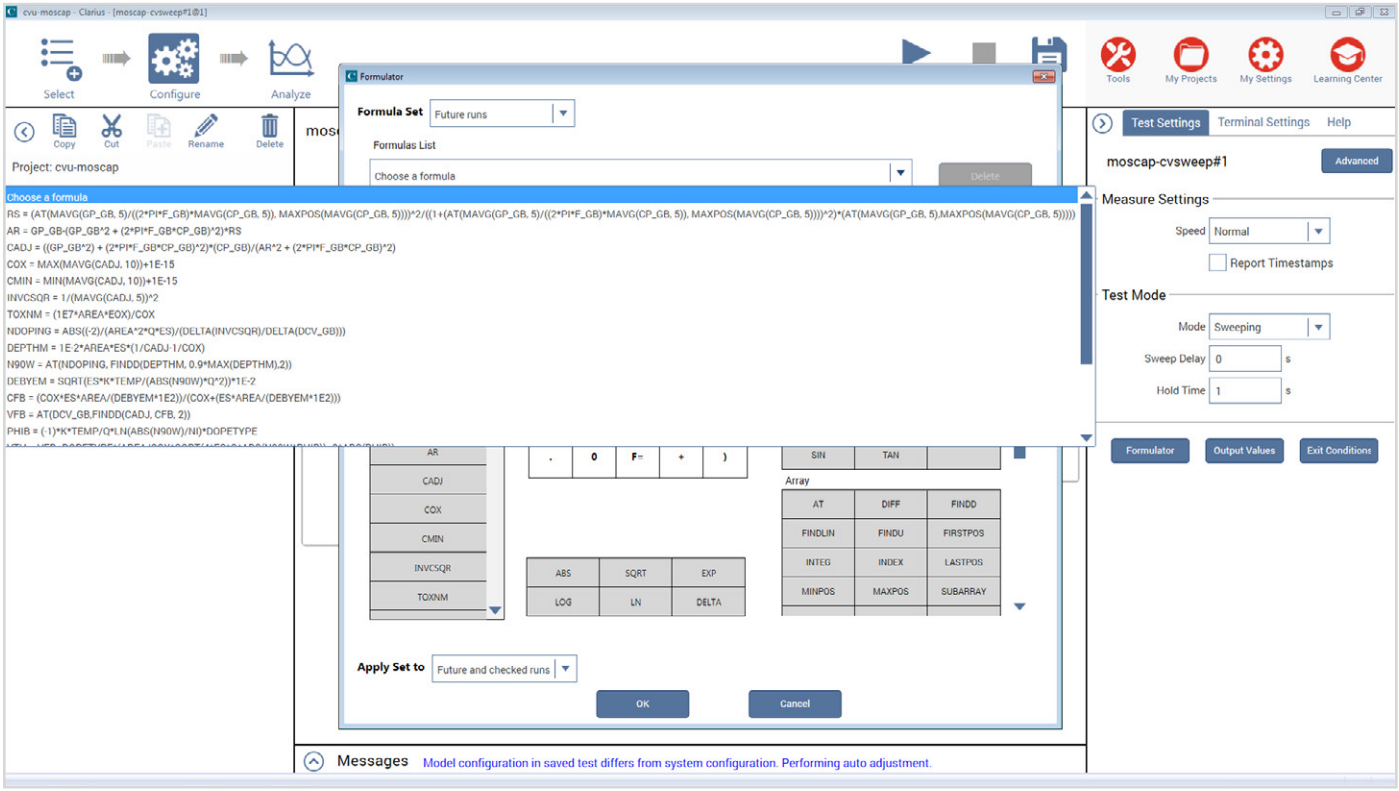

Figure 5. Formulator window with parameters derived

MOS Capacitor I/C² vs. Gate Voltage Sweep (*moscap-c-2vsv*) Test

This test performs a C-V sweep and displays the capacitance ($1/C^2$) as a function of the gate voltage (V_G). This sweep can yield important information about doping profile because the substrate doping concentration (N_{SUB}) is inversely related to the reciprocal of the slope of the $1/C^2$ vs. V_G curve. A positive slope indicates acceptors and a negative slope indicates donors. The substrate doping concentration is extracted from the slope of the $1/C^2$ curve and is displayed on the graph. **Figure 6** shows the results of executing this test module.

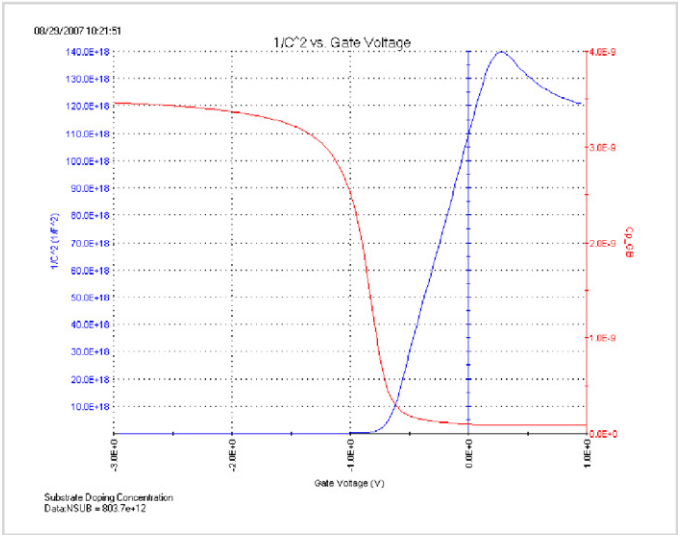

Figure 6. $1/C^2$ vs. gate voltage plot generated with 4210-CVU

MOS Capacitor Doping Profile (*moscap-dopingprofile*) Test

This test performs a doping profile, which is a plot of the doping concentration vs. depletion depth. The difference in capacitance at each step of the gate voltage is proportional to the doping concentration. The depletion depth is computed from the high frequency capacitance and oxide capacitance at each measured value of the gate voltage. The results are plotted on the graph as shown in **Figure 7.**

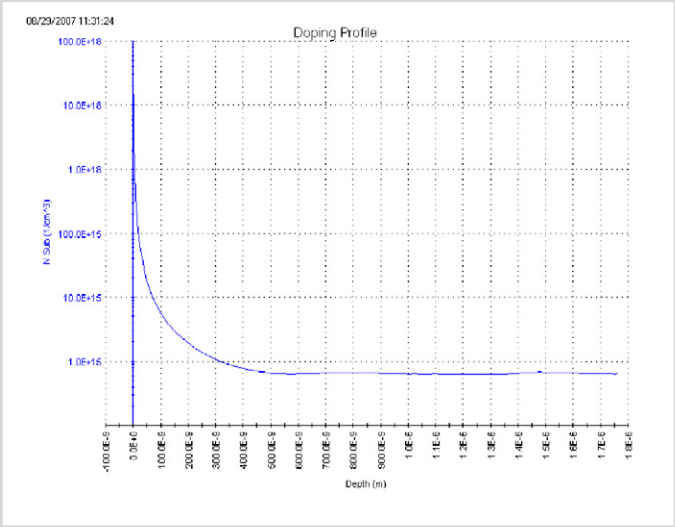

Figure 7. Doping profile extracted from C-V data taken with 4210-CVU

Connections to the 4210-CVU

To make a C-V measurement, a MOS cap is connected to the 4210-CVU as shown in **Figure 8**. In the test, both the 4210-CVU ammeter and the DC voltage appear at the HCUR/HPOT terminals. See the next section, "Measurement Optimization," for further information on connecting the CVU to the device on a wafer.

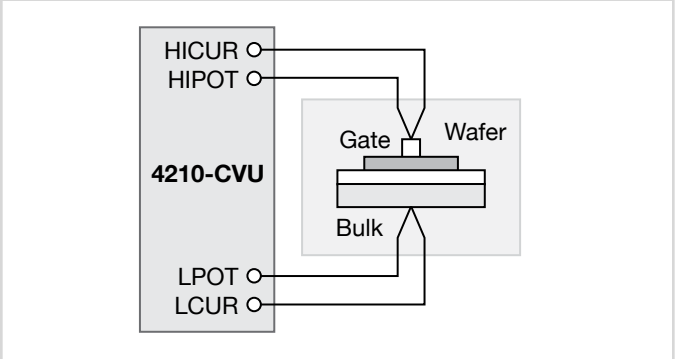

Figure 8. Basic configuration to test MOS capacitor with 4210-CVU

Measurement Optimization

Successful measurements require compensating for stray capacitance, measuring at equilibrium conditions, and compensating for series resistance.

Offset Correction for Stray Capacitance

C-V measurements on a MOS capacitor are typically performed on a wafer using a prober. The 4210-CVU is designed to be connected to the prober via interconnect cables and adaptors and may possibly be routed through a switch matrix. This cabling and switch matrix will add stray capacitance to the measurements.

To correct for stray capacitance, the Clarius software has a built-in tool for offset correction, which is a two-part process: the corrections for open and/or short are performed first, and then they can be enabled within a test.

To perform the corrections, select Tools and select CVU Connection Compensation. For an Open correction, select Measure Open. Probes must be up during the correction. Open is typically used for high impedance measurements (<10pF or >1MΩ).

For a Short correction, select Measure Short. Short the probe to the chuck. A short correction is generally performed for low impedance measurements (>10nF or <10Ω).

After the corrections are performed, they must be enabled in the test. To enable corrections, select the CVU Open and/or Short checkboxes in the Terminal Settings pane (**Figure 9**).

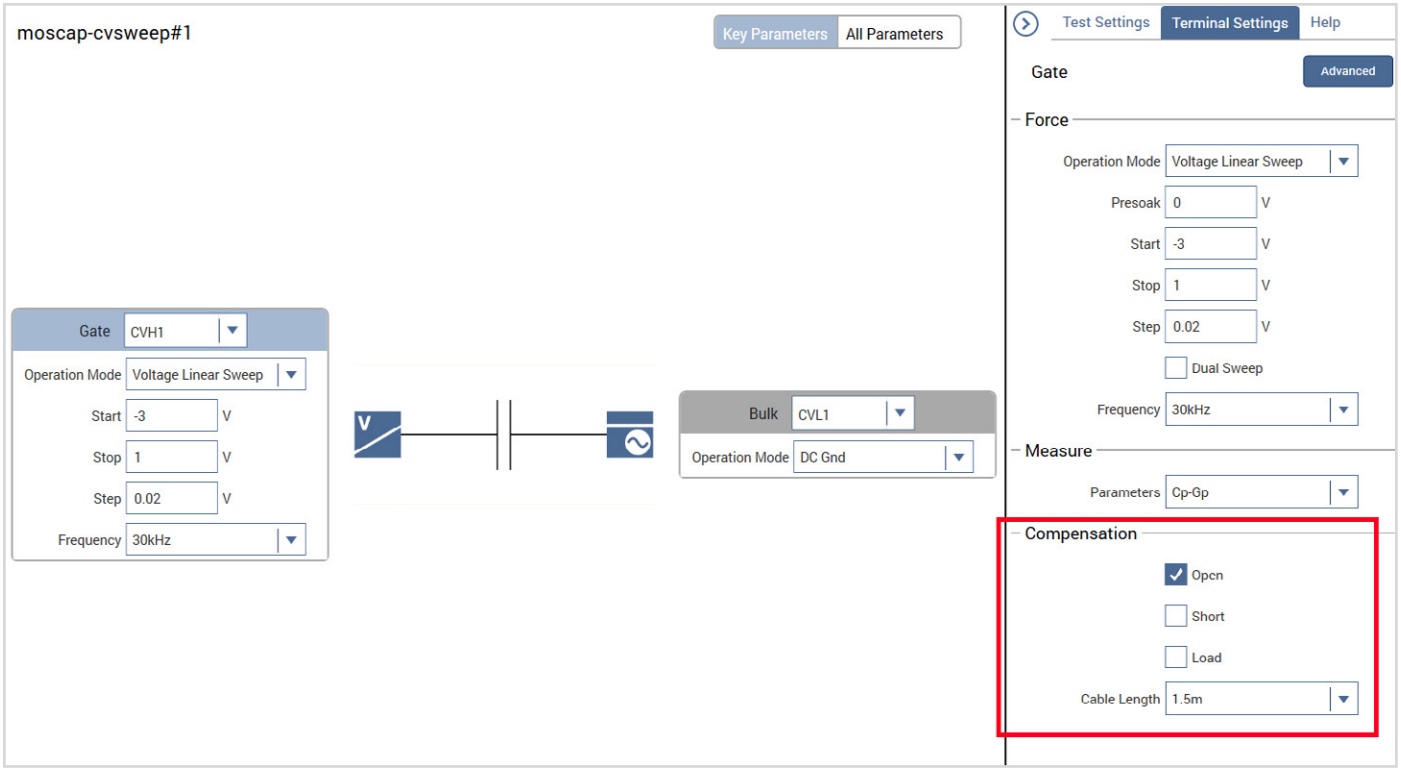

Figure 9. CVU compensation window

Measuring at Equilibrium Conditions

A MOS capacitor takes time to become fully charged after a voltage step is applied. C-V measurement data should only be recorded after the device is fully charged. This condition is called the equilibrium condition. Therefore, to allow the MOS capacitor to reach equilibrium: (1) allow a sufficient Hold Time in the Test Settings panel to enable the MOS capacitor to charge up while applying a "PreSoak" voltage, and (2) allow a sufficient Sweep Delay Time before recording the capacitance after each voltage step of a voltage sweep. The appropriate Hold and Delay Times are determined experimentally by generating capacitance vs. time plots and observing the time for the capacitance to settle.

Although C-V curves swept from different directions may look different, allowing adequate Hold and Delay Times minimizes such differences. One way to determine sufficient Hold and Delay Times is to generate a series of C-V curves in both directions. Change the Hold and Delay Times for each pair of inversion → accumulation and accumulation → inversion curves until the curves look essentially the same for both sweep directions.

Hold and Delay Times When Sweeping from Inversion Accumulation.

When the C-V sweep starts in the inversion region and the starting voltage is initially applied, a MOS capacitor is driven into deep depletion. Thereafter, if the starting voltage is maintained, the initial high frequency C-V curve climbs toward and ultimately stabilizes to the minimum capacitance at equilibrium. However, if the initial Hold Time is too short, the MOS capacitor cannot adequately recover from deep depletion, and the measured capacitance will be smaller than the minimum capacitance at equilibrium. Set the "PreSoak" voltage to the first voltage in the voltage sweep and allow a sufficient Hold Time for the MOS capacitor to reach equilibrium.
However, once the MOS capacitor has reached equilibrium after applying the "PreSoak" voltage, an inversion → accumulation C-V sweep may be performed with small delay times. This is possible because minority carriers recombine relatively quickly as the gate voltage is reduced. Nonetheless, if the Delay Time is too short, non-equilibrium occurs, and the capacitance in the inversion region is slightly higher than the equilibrium value. This is illustrated by the upper dotted line in **Figure 10.**

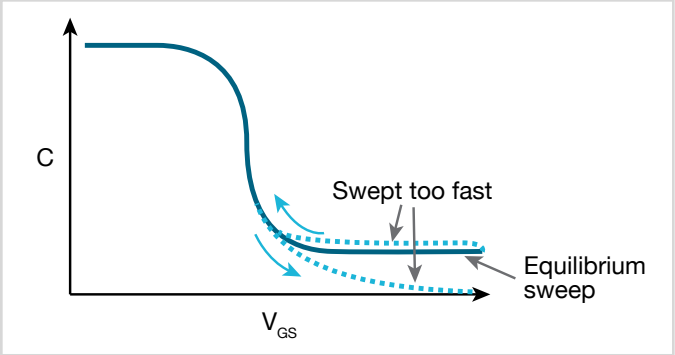

Figure 10. Effects of performing a C-V sweep too quickly

Hold and Delay Times When Sweeping from Accumulation → Inversion.

When the C-V sweep starts in the accumulation region, the effects of Hold and Delay Times in the accumulation and depletion regions are fairly subtle. However, in the inversion region, if the Delay Time is too small (i.e., the sweep time is too fast), there's not enough time for the MOS capacitor to generate minority carriers to form an inversion layer. On the high frequency C-V curve, the MOS capacitor never achieves equilibrium and eventually becomes deeply depleted. The measured capacitance values fall well below the equilibrium minimum value. The lower dotted line in **Figure 10** illustrates this phenomenon.

Using the preferred sequence. Generating a C-V curve by sweeping from inversion to accumulation is faster and more controllable than sweeping from accumulation to inversion. **Figure 11** illustrates a preferred measurement sequence.

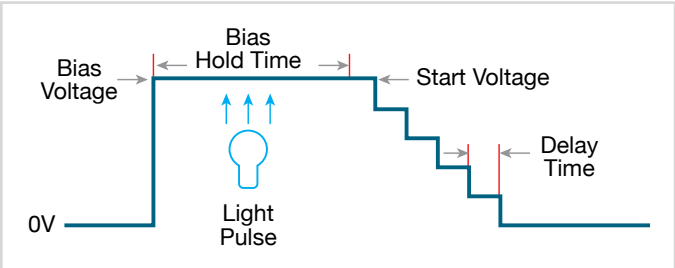

Figure 11. Preferred C-V measurement Sequence

The device is first biased at the "PreSoak" voltage for the specified Hold Time. The bias or "PreSoak" voltage should be the same as the sweep start voltage to avoid a sudden voltage change when the sweep starts. During biasing, if necessary, a short light pulse can be applied to the sample to help generate minority carriers. However, before the sweep starts, all lights should be turned off. All measurements should be performed in total darkness because the semiconductor material may be light sensitive. During the sweep, the Delay Time should be chosen to create the optimal balance between measurement speed and measurement integrity, which requires adequate equilibration time.

Compensating for Series Resistance

After generating a C-V curve, it may be necessary to compensate for series resistance in measurements. The series resistance (R_{SERIES}) can be attributed to either the substrate (well) or the backside of the wafer. For wafers typically produced in fabs, the substrate bulk resistance is fairly small (<10Ω) and has negligible impact on C-V measurements. However, if the backside of the wafer is used as an electrical contact, the series resistance due to oxides can significantly distort a measured C-V curve. Without series compensation, the measured capacitance can be lower than the expected capacitance, and C-V curves can be distorted. Tests for this project compensate for series resistance using the simplified three-element shown in **Figure 12**. In this model, C_{OX} is the oxide capacitance and C_A is the capacitance of the accumulation layer. The series resistance is represented by R_{SERIES}.

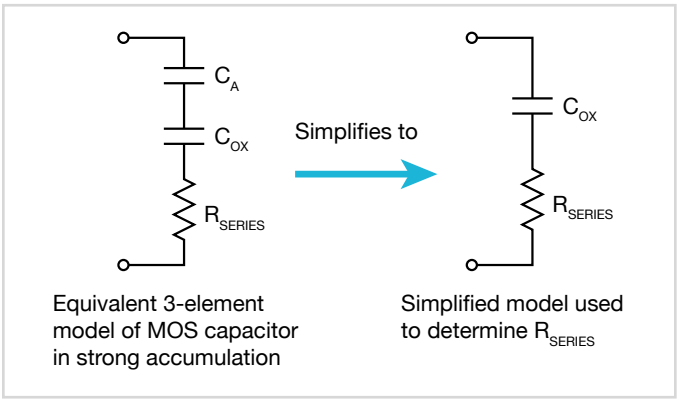

Figure 12. Simplified model to determine series resistance

The corrected capacitance (C_{ADJ}) and corrected conductance (G_{ADJ}) are calculated from the following formulas [1]:

$$C_{ADJ} = \frac{(G^2 + (2\pi fC)^2)C}{a_R^2 + (2\pi fC)^2}$$

$$G_{ADJ} = \frac{(G^2 + (2\pi fC)^2)a_R}{a_R^2 + (2\pi fC)^2}$$

where:

$a_R = G - (G^2 + (2\pi fC)^2)R_S$

C_{ADJ} = series resistance compensated parallel capacitance

C = measured parallel capacitance

G_{ADJ} = series resistance compensated conductance

G = measured conductance

f = test frequency

R_S = series resistance

The series resistance (R_S) may be calculated from the capacitance and conductance values that are measured while biasing the DUT (device under test) in the accumulation region as follows:

$$R_S = \frac{\left(\frac{G}{2\pi fC}\right)^2}{\left[1+\left(\frac{G}{2\pi fC}\right)^2\right]G}$$

where:

R_S = series resistance

G = measured conductance

C = measured parallel capacitance (in strong accumulation)

f = test frequency

NOTE: The preceding equations for compensating for series resistance require that the 4210-CVU be using the parallel model (Cp-Gp).

For this project, these formulas have been added into the Formulator so the capacitance and conductance can be automatically compensated for the series resistance.

Extracting MOS Device Parameters From C-V Measurements

This section describes the device parameters that are extracted from the C-V data taken in the three test modules in the *MOS Capacitor C-V Project*. The parameters are derived in the Formulator and the calculated values appear in the Sheet tab in the Analyze view of each test as shown in **Figure 13**.

moscap-cvsweep#1 View:

Run1 Formulas List RS= (AT(MAVG(GP_GB, 5)/((2*PI*F_GB)*MAVG(CP_GB, 5)), MAXPOS(MAVG(CP_GI Edit Save Data

	A	B	C	D	E	F	G	H	I	J	
1	Cp_GB	Gp_GB	DCV_GB	F_GB	RS	AR	CADJ	COX	CMIN	INVCSQR	TC
2	3.4645E-9	36.4846E-6	-3.0000E+0	30.0000E+3	85.3264E+0	-19.4742E-9	3.4754E-9	3.4698E-9	90.0692E-12	#REF	
3	3.4633E-9	36.4740E-6	-2.9800E+0	30.0000E+3		-4.7268E-9	3.4741E-9			#REF	
4	3.4621E-9	36.4524E-6	-2.9600E+0	30.0000E+3		158.2666E-12	3.4729E-9			82.9086E+15	
5	3.4609E-9	36.4374E-6	-2.9400E+0	30.0000E+3		10.4458E-9	3.4717E-9			82.9667E+15	
6	3.4597E-9	36.4159E-6	-2.9200E+0	30.0000E+3		13.5522E-9	3.4705E-9			83.0257E+15	
7	3.4585E-9	36.3938E-6	-2.9000E+0	30.0000E+3		17.2661E-9	3.4693E-9			83.0848E+15	
8	3.4572E-9	36.3689E-6	-2.8800E+0	30.0000E+3		19.1980E-9	3.4680E-9			83.1443E+15	
9	3.4559E-9	36.3514E-6	-2.8600E+0	30.0000E+3		28.4679E-9	3.4667E-9			83.2056E+15	
10	3.4547E-9	36.3206E-6	-2.8400E+0	30.0000E+3		23.3835E-9	3.4655E-9			83.2676E+15	
11	3.4534E-9	36.3083E-6	-2.8200E+0	30.0000E+3		39.6584E-9	3.4641E-9			83.3307E+15	
12	3.4521E-9	36.2819E-6	-2.8000E+0	30.0000E+3		40.3526E-9	3.4628E-9			83.3955E+15	
13	3.4507E-9	36.2581E-6	-2.7800E+0	30.0000E+3		45.5286E-9	3.4614E-9			83.4610E+15	
14	3.4493E-9	36.2374E-6	-2.7600E+0	30.0000E+3		55.0267E-9	3.4600E-9			83.5275E+15	
15	3.4480E-9	36.2034E-6	-2.7400E+0	30.0000E+3		48.0724E-9	3.4587E-9			83.5952E+15	
16	3.4465E-9	36.1833E-6	-2.7200E+0	30.0000E+3		58.5557E-9	3.4572E-9			83.6643E+15	
17	3.4451E-9	36.1589E-6	-2.7000E+0	30.0000E+3		63.6099E-9	3.4558E-9			83.7338E+15	
18	3.4436E-9	36.1332E-6	-2.6800E+0	30.0000E+3		69.5090E-9	3.4543E-9			83.8057E+15	
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20	3.4406E-9	36.0822E-6	-2.6400E+0	30.0000E+3		81.4972E-9	3.4513E-9			83.9541E+15	
21	3.4390E-9	36.0475E-6	-2.6200E+0	30.0000E+3		80.0865E-9	3.4497E-9			84.0308E+15	
22	3.4375E-9	36.0144E-6	-2.6000E+0	30.0000E+3		79.6444E-9	3.4481E-9			84.1090E+15	
23	3.4358E-9	35.9866E-6	-2.5800E+0	30.0000E+3		86.8085E-9	3.4464E-9			84.1885E+15	
24	3.4342E-9	35.9480E-6	-2.5600E+0	30.0000E+3		82.0969E-9	3.4448E-9			84.2691E+15	
25	3.4325E-9	35.9198E-6	-2.5400E+0	30.0000E+3		88.1696E-9	3.4431E-9			84.3510E+15	
26	3.4309E-9	35.8909E-6	-2.5200E+0	30.0000E+3		94.6727E-9	3.4414E-9			84.4342E+15	
27	3.4292E-9	35.8622E-6	-2.5000E+0	30.0000E+3		101.1837E-9	3.4397E-9			84.5191E+15	
28	3.4274E-9	35.8265E-6	-2.4800E+0	30.0000E+3		102.8557E-9	3.4379E-9			84.6060E+15	
29	3.4256E-9	35.7885E-6	-2.4600E+0	30.0000E+3		101.8689E-9	3.4361E-9			84.6951E+15	
30	3.4238E-9	35.7543E-6	-2.4400E+0	30.0000E+3		105.9497E-9	3.4343E-9			84.7873E+15	
31	3.4219E-9	35.7237E-6	-2.4200E+0	30.0000E+3		114.7982E-9	3.4324E-9			84.8822E+15	
32	3.4199E-9	35.6793E-6	-2.4000E+0	30.0000E+3		111.9680E-9	3.4304E-9			84.9795E+15	
33	3.4179E-9	35.6533E-6	-2.3800E+0	30.0000E+3		128.3570E-9	3.4283E-9			85.0793E+15	
34	3.4159E-9	35.6002E-6	-2.3600E+0	30.0000E+3		116.8718E-9	3.4263E-9			85.1827E+15	
35	3.4138E-9	35.5684E-6	-2.3400E+0	30.0000E+3		128.2407E-9	3.4242E-9			85.2879E+15	
36	3.4116E-9	35.5340E-6	-2.3200E+0	30.0000E+3		140.0366E-9	3.4220E-9			85.3942E+15	
37	3.4094E-9	35.4767E-6	-2.3000E+0	30.0000E+3		127.7582E-9	3.4198E-9			85.5035E+15	
38	3.4073E-9	35.4462E-6	-2.2800E+0	30.0000E+3		141.0168E-9	3.4177E-9			85.6165E+15	
39	3.4050E-9	35.3947E-6	-2.2600E+0	30.0000E+3		137.1490E-9	3.4154E-9			85.7313E+15	
40	3.4026E-9	35.3588E-6	-2.2400E+0	30.0000E+3		151.2832E-9	3.4129E-9			85.8492E+15	

Figure 13. Extracted C-V parameters shown in the Sheet

Oxide Thickness

For a relatively thick oxide (>50Å), extracting the oxide thickness is fairly simple. The oxide capacitance (C_{OX}) is the high frequency capacitance when the device is biased for strong accumulation. In the strong accumulation region, the MOS-C acts like a parallel-plate capacitor, and the oxide thickness (T_{OX}) may be calculated from C_{OX} and the gate area using the following equation:

$$T_{OX(nm)} = \frac{(10^7)A\varepsilon_{OX}}{C_{OX}}$$

where:

T_{OX} = oxide thickness (nm)

A = gate area (cm^2)

ε_{OX} = permittivity of the oxide material (F/cm)

C_{OX} = oxide capacitance (F)

10^7 = units conversion from cm to nm

Flatband Capacitance and Flatband Voltage

Application of a certain gate voltage, the flatband voltage (V_{FB}), results in the disappearance of band bending. At this point, known as the flatband condition, the semiconductor band is said to become flat. Because the band is flat, the surface potential is zero (with the reference potential being taken as the bulk potential deep in the semiconductor). Flatband voltage and its shift are widely used to extract other device parameters, such as oxide charges.

V_{FB} can be identified from the C-V curve. One way is to use the flatband capacitance method. For this method, the ideal value of the flatband capacitance (C_{FB}) is calculated from the oxide capacitance and the Debye length. The concept of Debye length is introduced later in this section. Once the value of C_{FB} is known, the value of V_{FB} can be obtained from the C-V curve data, by interpolating between the closest gate-to-substrate (V_{GS}) values [2].

The Debye length parameter (λ) must also be calculated to derive the flatband voltage and capacitance. Based on the doping profile, the λ calculation requires one of the following doping concentrations: N at 90% of W_{MAX} (refer to Nicollian and Brews), a user-supplied N_A (bulk doping concentration for a p-type, acceptor, material), or a user-supplied N_D (bulk doping concentration for an n-type, donor, material).

NOTE: The flatband capacitance method is invalid when the interface trap density (D_{IT}) becomes very large (10^{12}–10^{13} or greater). However, the method should give satisfactory results for most users. When dealing with high D_{IT} values, consult the appropriate literature for a more suitable method.

The flatband capacitance is calculated as follows:

$$C_{FB} = \frac{C_{OX}\,(\varepsilon_S A/\lambda)\,(10^2)}{C_{OX} + (\varepsilon_S A/\lambda)\,(10^2)}$$

where:

C_{FB} = flatband capacitance (F)

C_{OX} = oxide capacitance (F)

ε_S = permittivity of the substrate material (F/cm)

A = gate area (cm^2)

10^2 = units conversion from m to cm

λ = extrinsic Debye length, which is calculated as follows:

$$l = \left(\frac{\varepsilon_S kT}{q^2 N}\right)^{1/2} (10^{-2})$$

where:

λ = extrinsic Debye length

ε_S = permittivity of the substrate material (F/cm)

kT = thermal energy at room temperature (293K) (4.046×10^{-21}J)

q = electron charge (1.60219×10^{-19}C)

$N_X = N$ at 90% W_{MAX} or N90W (refer to Nicollian and Brews; see References) or, when input by the user, $N_X = N_A$ or $N_X = N_D$

10^{-2} = units conversion from cm to m

The extrinsic Debye length is an idea borrowed from plasma physics. In semiconductors, majority carriers can move freely. The motion is similar to a plasma. Any electrical interaction has a limited range. The Debye length is used to represent this interaction range. Essentially, the Debye length indicates how far an electrical event can be sensed within a semiconductor.

Threshold Voltage

The turn-on region for a MOSFET corresponds to the inversion region on its C-V plot. When a MOSFET is turned on, the channel formed corresponds to strong generation of inversion charges. It is these inversion charges that conduct current. When a source and drain are added to a MOS-C to form a MOSFET, a p-type MOS-C becomes an n-type MOSFET, also called an n-channel MOSFET. Conversely, an n-type MOS-C becomes a p-channel MOSFET.

The threshold voltage (V_{TH}) is the point on the C-V curve where the surface potential (ϕ_S) equals twice the bulk potential (ϕ_B). This curve point corresponds to the onset of strong inversion. For an enhancement-mode MOSFET, V_{TH} corresponds to the point where the device begins to conduct. The physical meaning of the threshold voltage is the same for both a MOS-C C-V curve and a MOSFET I-V curve. However, in practice, the numeric V_{TH} value for a MOSFET may be slightly different due to the particular method used to extract the threshold voltage.

The threshold voltage of a MOS capacitor can be calculated as follows:

$$V_{TH} = V_{FB} \pm \left[\frac{A}{C_{OX}} \sqrt{4\varepsilon_S q |N_{BULK}\, \phi_B|} + 2|\phi_B| \right]$$

where:

V_{TH} = threshold voltage (V)

V_{FB} = flatband potential (V)

A = gate area (cm^2)

C_{OX} = oxide capacitance (F)

ε_S = permittivity of the substrate material (F/cm)

q = electron charge (1.60219×10^{-19}C)

N_{BULK} = bulk doping (cm^{-3}) (Note: The Formulator name for N_{BULK} is N90W.)

ϕ_B = bulk potential (V) (Note: The Formulator name for ϕ_B is PHIB.)

The bulk potential is calculated as follows:

$$\phi_B = -\frac{kT}{q} \ln\left(\frac{N_{BULK}}{N_i}\right) (DopeType)$$

where:

ϕ_B = bulk potential (V)
(Note: The Formulator name for ϕ_B is PHIB.)

k = Boltzmann's constant (1.3807×10^{-23}J/K)

T = test temperature (K)

q = electron charge (1.60219×10^{-19}C)

N_{BULK} = Bulk doping (cm^{-3})
(Note: The Formulator name for N_{BULK} is called N90W.)

N_i = Intrinsic carrier concentration ($1.45 \times 10^{10} cm^{-3}$)

DopeType = +1 for p-type materials and –1 for n-type materials

Metal-semiconductor Work Function Difference

The metal-semiconductor work function difference (W_{MS}) is commonly referred to as the work function. It contributes to the shift in V_{FB} from the ideal zero value, along with the effective oxide charge [3][4]. The work function represents the difference in work necessary to remove an electron from the gate and from the substrate.

The work function is derived as follows:

$$W_{MS} = W_M - \left[W_S + \frac{E_{BG}}{2} - \phi_B \right]$$

where:

W_{MS} = work function

W_M = metal work function (V) *

W_S = substrate material work function, electron affinity (V) *

E_{BG} = substrate material bandgap (V) *

ϕ_B = bulk potential (V)
(Note: The Formulator name for ϕ_B is PHIB)

*The values for W_M, W_S, and E_{BG} are listed in the Formulator as constants. The user can change the values depending on the type of materials.

The following example calculates the work function for silicon, silicon dioxide, and aluminum:

$$W_{MS} = 4.1 - \left[4.15 + \frac{1.12}{2} - \phi_B \right]$$

Therefore,

$$W_{MS} = -0.61 + \phi_B$$

and

$$W_{MS} = -0.61 - \frac{kT}{q} \ln\left(\frac{N_{BULK}}{N_i}\right) (DopeType)$$

where:

W_{MS} = work function

k = Boltzmann's constant (1.3807×10^{-23}J/K)

T = test temperature (K)

q = electron charge (1.60219×10^{-19}C)

N_{BULK} = bulk doping (cm^{-3})

DopeType = +1 for p-type materials and –1 for n-type materials

For example, for an MOS capacitor with an aluminum gate and p-type silicon (N_{BULK} = $10^{16}cm^{-3}$), W_{MS} = –0.95V. Also, for the same gate and n-type silicon (N_{BULK} = $10^{16}cm^{-3}$), W_{MS} = –0.27V. Because the supply voltages of modern CMOS devices are lower than those of earlier devices and because aluminum reacts with silicon dioxide, heavily doped polysilicon is often used as the gate material. The goal is to achieve a minimal work-function difference between the gate and the semiconductor, while maintaining the conductive properties of the gate.

Effective and Total Bulk Oxide Charge

The effective oxide charge (Q_{EFF}) represents the sum of oxide fixed charge (Q_F), mobile ionic charge (Q_M), and oxide trapped charge (Q_{OT}):

$$Q_{EFF} = Q_F + Q_M + Q_{OT}$$

Q_{EFF} is distinguished from interface trapped charge (Q_{IT}), in that Q_{IT} varies with gate bias and Q_{EFF} does not [5] [6]. Simple measurements of oxide charge using C-V measurements do not distinguish the three components of Q_{EFF}. These three components can be distinguished from one another by temperature cycling [7]. Also, because the charge profile in the oxide is not known, the quantity (Q_{EFF}) should be used as a relative, not an absolute, measure of charge. It assumes that the charge is located in a sheet at the silicon–silicon dioxide interface.

From Nicollian and Brews, Eq. 10.10, we have:

$$V_{FB} - W_{MS} = -\frac{Q_{EFF}}{C_{OX}}$$

where:

V_{FB} = flatband potential (V)

W_{MS} = metal-semiconductor work function (V)

Q_{EFF} = effective oxide charge (C)

C_{OX} = oxide capacitance (F)

Note that C_{OX} here is per unit of area. So that:

$$Q_{EFF} = \frac{C_{OX}(W_{MS} - V_{FB})}{A}$$

where:

Q_{EFF} = effective oxide charge (C)

C_{OX} = oxide capacitance (F)

W_{MS} = metal–semiconductor work function (V)

V_{FB} = flatband potential (V)

A = gate area (cm^2)

For example, assume a $0.01cm^2$, 50pF, p-type MOS-C with a flatband voltage of –5.95V; its N_{BULK} of $10^{16}cm^{-3}$ corresponds to a W_{MS} of –0.95 V. For this example, Q_{EFF} can be calculated to be $2.5 \times 10^{-8}C/cm^2$, which in turn causes the threshold voltage to shift ~5V in the negative direction. Note that in most cases where the bulk charges are positive, there is a shift toward negative gate voltages. **The effective oxide charge concentration (N_{EFF}) is computed from effective oxide charge (Q_{EFF}) and the electron charge as follows:**

$$N_{EFF} = \frac{Q_{EFF}}{q}$$

where:

N_{EFF} = effective oxide charge density (cm^{-2})

Q_{EFF} = effective oxide charge (C)

q = electron charge ($1.60219 \times 10^{-19}C$)

Substrate Doping Concentration

The substrate doping concentration (N) is related to the reciprocal of the slope of the $1/C^2$ vs. V_G curve. **The doping concentration is calculated and displayed below the graph in the moscap-c-2vsv test as follows:**

$$N_{SUB} = \frac{2}{q\varepsilon_S A^2 \left(\frac{\Delta 1/C^2}{\Delta V_G}\right)}$$

where:

N_{SUB} = substrate doping concentration

q = electron charge ($1.60219 \times 10^{-19}C$)

A = gate area (cm^2)

ε_S = permittivity of the substrate material (F/cm)

V_G = gate voltage (V)

C = measured capacitance (F)

Doping Concentration vs. Depth (doping profile)

The doping profile of the device is derived from the C-V curve based on the definition of the differential capacitance as the differential change in depletion region charges produced by a differential change in gate voltage [8].

The standard doping concentration (N) vs. depth (w) analysis discussed here does not compensate for the onset of accumulation, and it is accurate only in depletion. This method becomes inaccurate when the depth is less than two Debye lengths. **The doping concentration used in the doping profile is calculated as:**

$$N = \left| \frac{-2}{q\varepsilon_s A^2 \frac{d(1/C^2)}{dV}} \right|$$

The *moscap-dopingprofile* test computes the depletion depth (w) from the high frequency capacitance and oxide capacitance at each measured value of the gate voltage (V_G) [9]. The Formulator computes each (w) element of the calculated data array as shown:

$$W = A\varepsilon_S \left(\frac{1}{C} - \frac{1}{C_{OX}} \right) (10^2)$$

where:

W = depth (m)

A = the gate area (cm^2)

C = the measured capacitance (F)

ε_S = the permittivity of the substrate material (F/cm)

C_{OX} = the oxide capacitance (F)

10^2 = units conversion from cm to m

Once the doping concentration and depletion depth are derived, a doping profile can be plotted. This is done in the Graph of the *MOS Capacitor Doping Profile* (*moscap-dopingprofile)* test.

Summary

When equipped with the 4210-CVU option, the 4200A-SCS is a very useful tool for making both C-V and I-V measurements on MOS capacitors and deriving many of the common MOS parameters. In addition to the *MOS Capacitor C-V Project*, the 4200A-SCS includes other projects specifically for testing MOS capacitors. The *MOS Capacitor Lifetime Test Project* is used for determining generation velocity and lifetime testing (Zerbst plot) of MOS capacitors. *The MOS Capacitor Mobile Ion Project* determines the mobile charge of a MOS cap using the bias-temperature stress method. In addition to making C-V measurements, the SMUs can make I-V measurements on MOS caps, including leakage current and breakdown testing.

References

1. E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (New York: Wiley, 1982), 224.
2. *Ibid.,* 487–488
3. Nicollian and Brews, 462–477.
4. S.M. Sze, *Physics of Semiconductor Devices*, 2nd edition. (New York: Wiley, 1985), 395–402.
5. Nicollian and Brews, 424–429.
6. Sze, 390–395.
7. Nicollian and Brews, 429 (Figure 10.2).
8. Nicollian and Brews, 380–389.
9. Nicollian and Brews, 386.

Additional Suggested Reading

D.K. Schroder, *Semiconductor Material and Device Characterization*, 2nd edition. (New York, Wiley, 1998).

Switching Between C-V and I-V Measurements Using the 4200A-CVIV Multi-Switch and 4200A-SCS Parameter Analyzer

Introduction

Full parametric characterization of a semiconductor device usually requires an array of tests to gather all of the device's important parameters. Current-voltage (I-V) tests are used to determine device parameters like transfer characteristics, leakages, and breakdown voltages. Capacitance-voltage (C-V) tests are used to determine device parameters like doping concentrations, interface charges, and threshold voltages. It is very common to perform both I-V and C-V tests on the same device, but the two test types require different test equipment and cabling. These differences make it difficult to perform I-V and C-V measurements on the same device quickly because changing test types typically requires recabling the entire system.

When configured with 4200-SMU or 4210-SMU Source Measure Units (SMUs) and the 4210-CVU Capacitance Voltage Unit, the 4200A-SCS Parameter Analyzer is capable of performing both I-V and C-V measurements. However, the SMUs use triaxial cables and the CVU uses SMA coaxial cables. Combining the 4200A-SCS Parameter Analyzer with the 4200A-CVIV Multi-Switch eliminates these difficulties because the 4200A-CVIV is capable of switching between I-V and C-V measurements with no need to change cables or lift probe tips. The 4200A-CVIV is shown in **Figure 1**. The Clarius software that runs on the 4200A-SCS makes it simple to control the Multi-Switch and creates a faster, more efficient device testing workflow for any application that requires making I-V and C-V measurements on the same device.

Figure 1. The 4200A-CVIV Multi-Switch.

4200A-CVIV Operation

The 4200A-CVIV Multi-Switch is a four-channel multiplexed switching accessory for the 4200A-SCS that allows users to switch seamlessly between I-V and C-V measurements. It accepts four SMUs, one for each channel, and one CVU as inputs. Changing the output mode for each of the four channels reconfigures the internal switches of the 4200A-CVIV to route the desired signals to the output terminals. **Figure 2** shows a simplified switching diagram of the 4200A-CVIV.

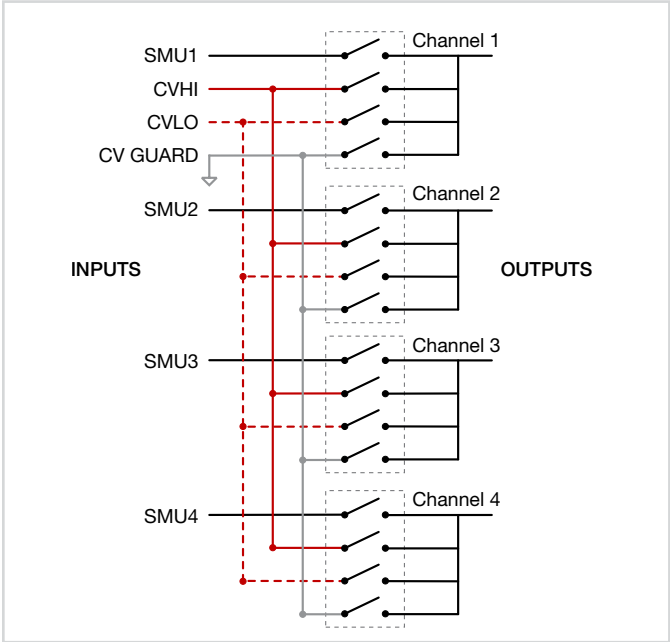

Figure 2. A simplified switching diagram for the 4200A-CVIV. All of the channels are shown in two-wire mode and in the OPEN position.

The 4200A-CVIV has five different output modes for each channel:

- **SMU** – The SMU signal paths in the 4200A-CVIV are not multiplexed and cannot be switched between channels. Each SMU channel is directly associated with the channel to which it is connected. For example, setting Channel 3 to **SMU** will pass the signal from the SMU connected to Channel 3 to the output terminals for Channel 3.
- **CV HI and CV LO** – The CVU signal path in the 4200A-CVIV is fully multiplexed and can be assigned to any of the output channels. **CV HI or CV LO** can be assigned to any channel or any combination of channels to perform the desired C-V measurement. For example,

setting Channel 1 to **CV HI** and Channels 2 and 3 to **CV LO** will configure the Multi-Switch to perform a C-V measurement on the device connected between Channel 1 and Channels 2/3.

- **CV GUARD** – This mode of the 4200A-CVIV can be used to remove undesired capacitances from C-V measurements. The CVU guard is the outside shield of the CVU coaxial cable. For example, setting Channel 4 to **CV GUARD** will configure the Multi-Switch to guard out capacitance from the device terminal connected to Channel 4.
- **OPEN** – Configuring any channel to **OPEN** will open all of the output relays connected to that channel.

The 4200A-CVIV is controlled using the Clarius software application that comes with the 4200A-SCS Parameter Analyzer. Switch configurations are controlled by placing the *cviv-configure* Action from the Action Library into the project tree.

The *cviv-configure* Action is used to switch the channel output configuration, two-wire/four-wire CVU setting, and the names of the test and channels to be shown on the 4200A-CVIV display. A *cviv-configure* Action must be used any time the configuration of the 4200A-CVIV needs to change. **Figure 3** shows an example of the *cviv-configure* Action populated with settings to switch the CVU output terminals to a MOSFET.

The *cvu-cviv-comp-collect* Action performs CVU connection compensation through a 4200A-CVIV on a user-defined configuration. Open, Short, and Load correction compensations can be acquired. Connection compensation corrects for offset and gain errors caused by the connections between the CVU and the device under test. The compensation for each particular switch configuration is automatically stored so that when a particular configuration is recalled using the *cviv-configure* Action, the compensation will automatically be applied if it is enabled within a C-V measurement test. **Figure 4** shows the *cvu-cviv-comp-collect* Action setup to perform an Open compensation.

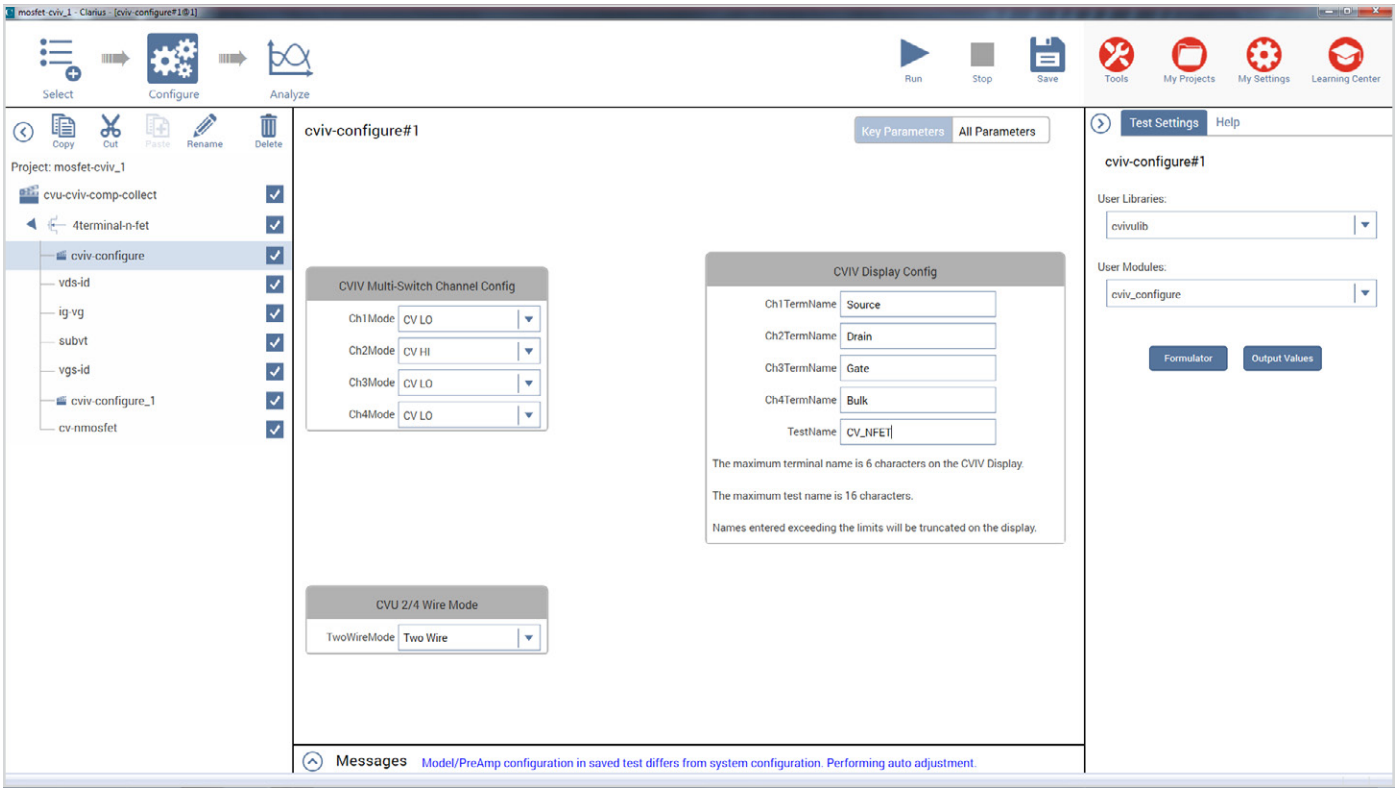

Figure 3. The *cviv-configure* Action options.

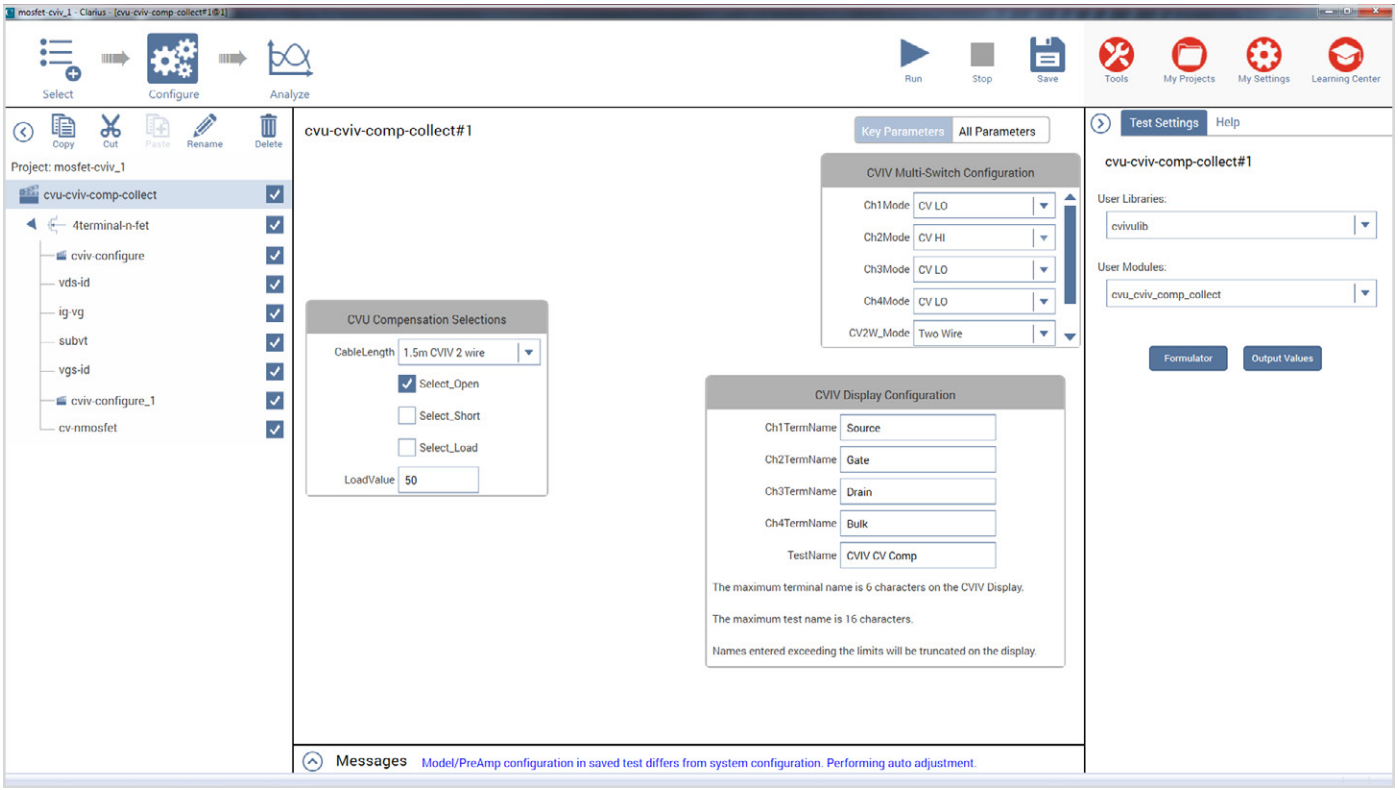

Figure 4. The *cvu-cviv-comp-collection* Action configured to perform an Open Compensation.

Figure 5 shows a screen capture of a project called *Diode Tests* that is used to make I-V and C-V measurements on a diode that is connected to the outputs of Channels 1 and 2. First, compensation is performed using the *cvu-cviv-comp-collect* Action. Then the *cviv-configure-iv* Action connects SMU1 and SMU2 to Channels 1 and 2 so that the forward and reverse I-V measurements can be made in the two tests that follow. When the *cviv-configure-cv* Action is executed, the SMUs are disconnected from the outputs and the CVU HI and LO terminals are connected to Channels 1 and 2. Finally, a C-V sweep is made on the diode.

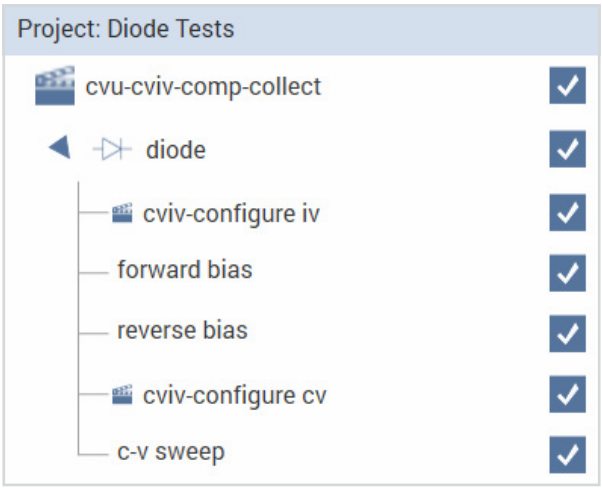

Figure 5. The project tree structure for a diode test that uses the 4200A-CVIV to switch between I-V and C-V measurements

C-V/I-V Switching for Device Characterization

Both I-V and C-V measurements play a role in the parametric characterization of semiconductor devices. Two-terminal devices require simple I-V sweeps to characterize their DC performance and C-V sweeps to determine the capacitance between their two terminals at different bias levels. For example, full characterization of a diode requires I-V measurements to acquire the forward I-V curve, reverse leakage curve, and reverse breakdown voltage. C-V measurements are used to acquire the diode's doping profile and charge density information.

Two-terminal Devices

Two channels of the 4200A-CVIV are used to connect to the diode for I-V and C-V measurements. Since diodes have very low impedance forward active characteristics, it's best practice to perform measurements in four-wire mode to prevent measurement inaccuracies due to losses in cabling. Four-wire mode, also called remote sense, forces a test current through one set of cables and measures a voltage directly at the device under test with another set of cables. This technique helps remove the effects of cable impedance from the measurements.

Figure 6 shows the device connections and 4200A-CVIV settings for an I-V test on a diode. All of the DC I-V characteristics of the diode are collected in this configuration. The connections to the diode are made with triaxial cables, Model 4200-TRX-.75 (75cm or approximately 30 inches). These shielded cables are used to ensure that both very low current I-V measurements and high frequency AC measurements can be made with high accuracy. The device can be a packaged part in a test fixture or located directly on a wafer in a probe station.

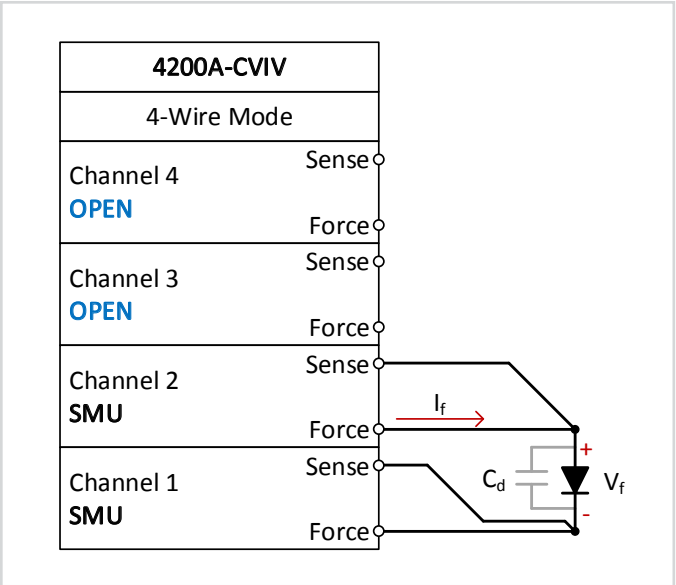

Figure 6. Configuration for I-V characterization of a diode using the 4200A-CVIV.

The gray capacitor in **Figure 6** (C_d) is the parasitic capacitance of the PN junction. The I-V test does not provide information about this parasitic capacitance. A C-V test is necessary to characterize the capacitance of the device. **Figure 7** shows the device connections and 4200A-CVIV settings for a C-V test on a diode. All of the connections are identical to the I-V test. When the *cviv-configure* Action is executed in the Clarius software, the output is switched from the SMUs to the CVU terminals.

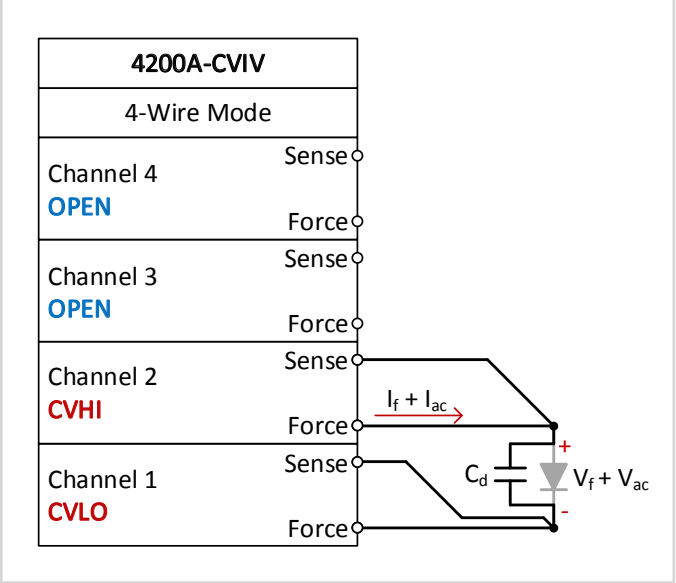

Figure 7. Configuration for C-V characterization of a diode using the 4200A-CVIV.

Three-terminal Devices

Three-terminal devices require more complicated I-V characterization and often capacitance measurements between multiple combinations of terminals. For example, bipolar junction transistors (BJTs) are three-terminal devices that require multiple SMUs to measure their transfer characteristics and produce useful data, such as Gummel plots. The 4200A-CVIV, when coupled with three 4200-SMUs or 4210-SMUs and the 4210-CVU in the 4200A-SCS, can make these measurements.

Figure 8 shows the device connections, and 4200A-CVIV settings, for an I-V test on a BJT. The configuration is shown in two-wire mode, also known as local sense, but remote sensing should be used for high current BJTs. All of the connections to the BJT are made with the 4200-TRX-.75 triaxial cables. The device can be a packaged part in a test fixture or located directly on a wafer in a probe station.

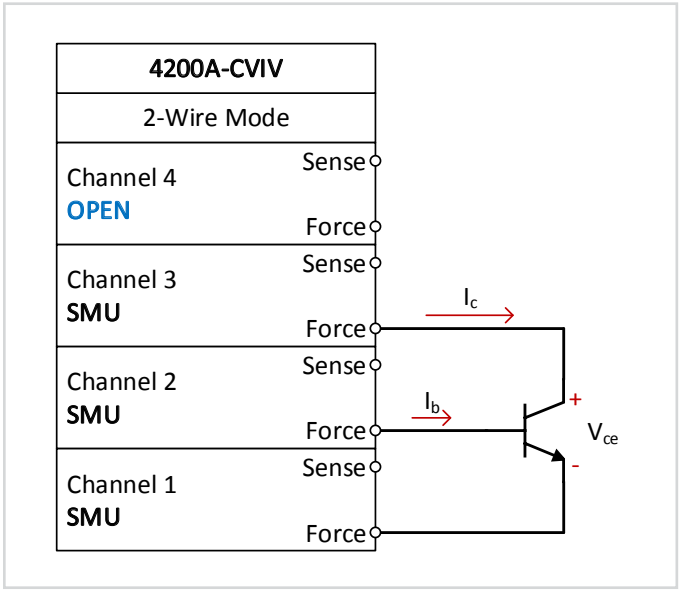

Figure 8. Configuration for I-V characterization of a BJT using the 4200A-CVIV.

Once the I-V measurements are complete, the 4200A-CVIV can be seamlessly switched to measure the parasitic capacitances of the BJT junctions without changing cables or removing connections to the device. **Figure 9** shows the parasitic capacitances between the BJT's terminals to be measured.

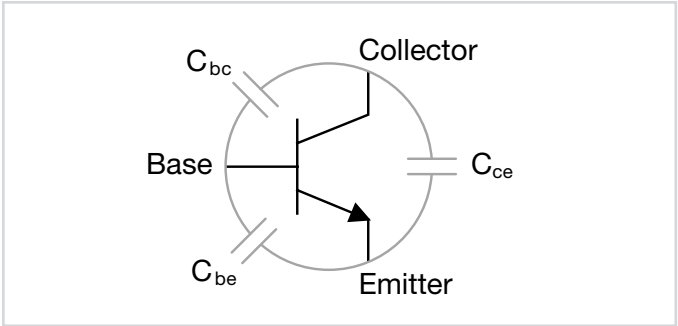

Figure 9. Parasitic capacitances of a bipolar junction transistor (BJT).

To measure the capacitance between two terminals, it is necessary to guard the third terminal to remove the effects of the additional parasitic capacitors. For example, to measure the base-emitter capacitance (C_{be}), the collector is connected to guard. The 4200A-CVIV provides this guard signal with the CV GUARD setting. **Figure 10** shows the *cviv-configure* settings that instruct the 4200A-CVIV to use the CV GUARD signal. In this example, the CV HI terminal is connected to base (b) through Channel 2, CV LO is connected to the emitter (e) through Channel 1, and CV GUARD is connected to the collector (c) through Channel 3.

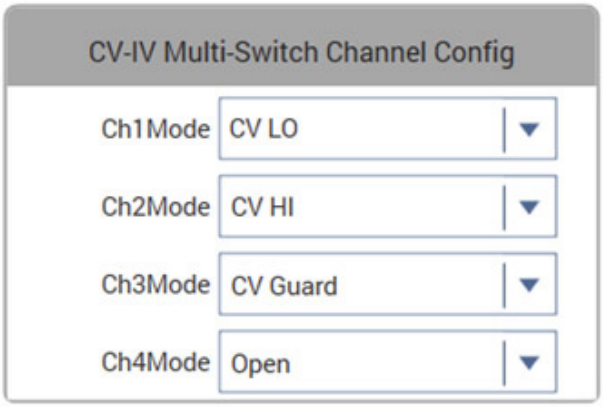

Figure 10. *cviv-configure* settings for a base-emitter capacitance measurement on a BJT.

Figure 11 shows the device connections, and 4200A-CVIV settings, for a guarded capacitance measurement on the C_{be} of a BJT.

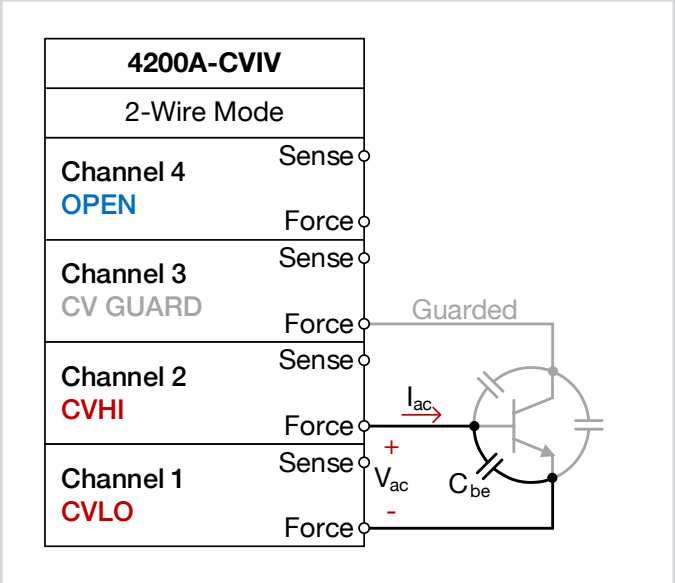

Figure 11. Base-emitter capacitance measurement on a BJT using the 4200A-CVIV.

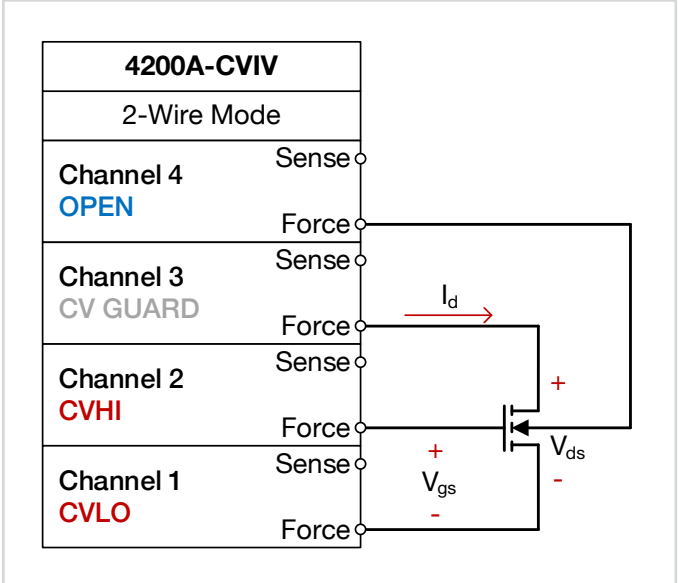

Figure 12. I-V characterization of a four-terminal MOSFET using the 4200A-CVIV.

The same technique is used to measure the base-collector capacitance or the collector-emitter capacitance of the BJT. The 4200A-CVIV can be controlled by the Clarius software to make all of these measurements automatically without moving cables between the terminals. The Clarius software includes a project (*cvu-bjt-cviv*) that is configured to measure these three parasitic capacitances present in a BJT using the 4210-CVU and the 4200A-CVIV to switch the CVU between terminals of the device.

Four-terminal Devices

Four-terminal devices, such as a MOSFET with a separate bulk connection, have more terminal-to-terminal parasitic capacitances, and more potential I-V and C-V measurement combinations than lower terminal count components. The 4200A-CVIV, when fully configured with four SMUs and one CVU, addresses these measurements with flexible configurability.

Figure 12 shows the device connections, and 4200A-CVIV settings, for an I-V test on a four-terminal MOSFET. The configuration is shown in two-wire mode, also known as local sense, but remote sensing should be used for high current MOSFETs. All of the connections to the MOSFET are made with 4200-TRX-.75 triaxial cables. The device can be a packaged part in a test fixture or located directly on a wafer in a probe station.

Capacitance measurements are often made on MOSFETs to explore their basic operation and various parameters. Given that the high frequency operation and switching speeds of a MOSFET are dependent on the capacitance of the device, capacitance measurements are often made on various parasitic capacitances of the device, as shown in **Figure 13**. For example, the capacitance between the gate and channel (C_{gd} and C_{gs}) is important because it creates the charges necessary for operating the devices. This gate-channel capacitance depends on the applied voltage and the operating region.

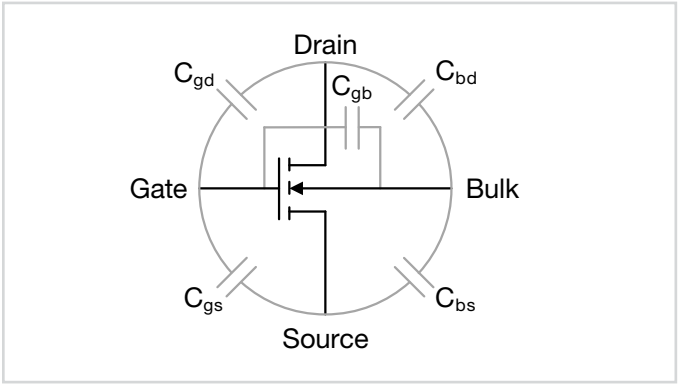

Figure 13. Parasitic capacitances of a MOSFET.

The C-V characteristics of the capacitor formed between the gate and the source, drain, and bulk of the MOSFET structure can be used to determine characteristics of the MOSFET like the threshold voltage, oxide thickness, oxide capacitance,

and doping density. **Figure 14** shows the most common way of configuring this measurement. The source, drain, and bulk terminals are physically tied together and a C-V sweep is performed between the gate and the other three terminals.

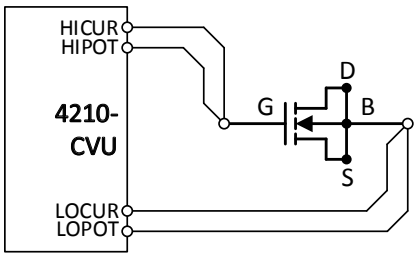

Figure 14. C-V test configuration for a MOSFET.

The CVHI, CVLO, and CV GUARD signals of the 4200A-CVIV can each be assigned to more than one pin at a time. This removes the need to tie the source, drain, and bulk together physically at the device to perform this measurement; instead, the connections are made internal to the 4200A-CVIV. **Figure 15** shows the device connections, and 4200A-CVIV settings, for this C-V test on a four-terminal MOSFET. Channels 1, 3, and 4 are all assigned to CVLO in this configuration. **Figure 16** shows the equivalent circuit of this 4200A-CVIV configuration.

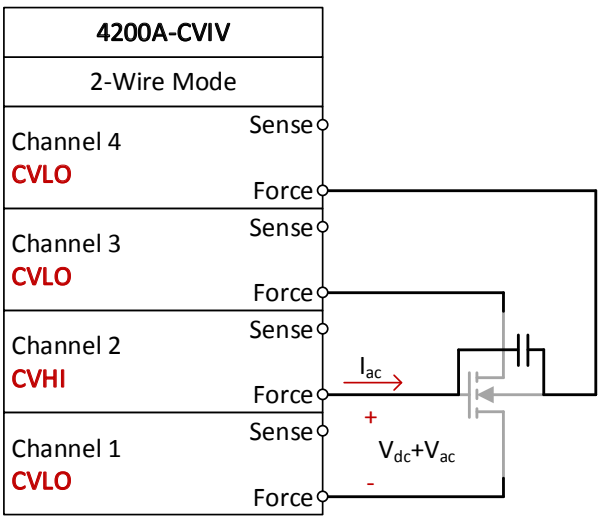

Figure 15. C-V characterization of a four-terminal MOSFET using the 4200A-CVIV.

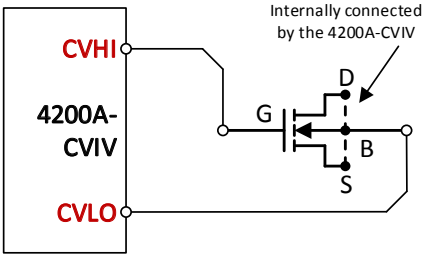

Figure 16. 4200A-CVIV two-terminal MOSFET C-V test equivalent circuit.

Conclusion

The 4200A-CVIV Multi-Switch makes it easy to perform I-V and C-V measurements on the same device without the need to change cables, which could potentially introduce errors or damage devices. The 4200A-SCS and Clarius software make it simple to control the 4200A-CVIV and integrate C-V and I-V testing together into a single project that executes seamlessly and continuously.

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