San Jose State University

Department of Electrical Engineering

ELECTRICAL ENGINEERING SENIOR PROJECT

Microwave Amplifier Design
(part 1)

by

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Objective

The goal of our senior design project was to design and build a prototype single stage Microwave power amplifier operated at 2.4 GHz with a linear region of operation up to our desired output of 1 watt or 30 dBm. This project was chosen because of its apparent complexity and the RF design experience that would be gained by the end of the project.

Project Specifications:

As a design team, we came to the conclusion that we wanted to design our amplifier to operate in the 2.4 GHz ISM (Industrial, Scientific, and Medical) Band. Typical 2.4 GHz Microwave amplifiers on the market were researched and comparable target specifications were proposed. The overall target specifications of the amplifier design are as follows:

- Operating frequency @ 2.4GHz
- Output power of 1 watt (30 dBm)
- Obtain a gain of +10 ~12db
- 1dB compression >= 30dbm
- Cost < $ 100

Application

The applications of our proposed device include many products in the field of microwave communications. One of the important applications of a Microwave power amplifier is in the output stage of a transmitter where a signal needs amplification before it is transmitted. A high power amplifier is needed for transmitting a signal through an antenna and a medium. The Microwave power amplifier amplifies the input signal after the signal has been modulated in the transmitter. The High power amplification step is necessary for every application of antenna transmission.
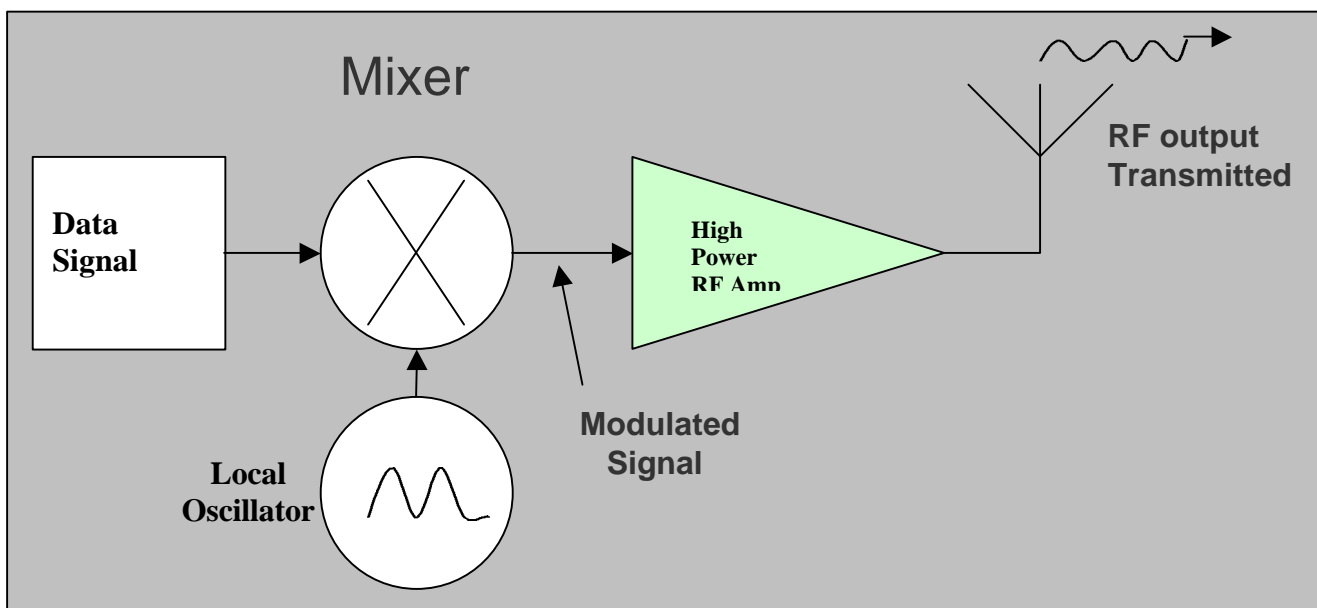

Figure 1: General Transmitter Output Stage

Design Methodology

A power amplifier is an amplifier that takes a low or intermediate level signal and significantly boosts its power level. At low frequencies this might be a trivial design which would only involve the careful choice of a DC bias circuit designed for maximum power output. But our chosen amplifier design is designed to operate at the microwave frequency of 2.4 GHz. When operating at this frequency, transmission line theory comes into the picture. The high frequency and short wavelength of microwave energy make for difficulties in analysis and design of microwave components and systems. Matching of the input and output of the transistor must be considered and designed around. A typical block diagram of a single-stage RF amplifier is shown below.
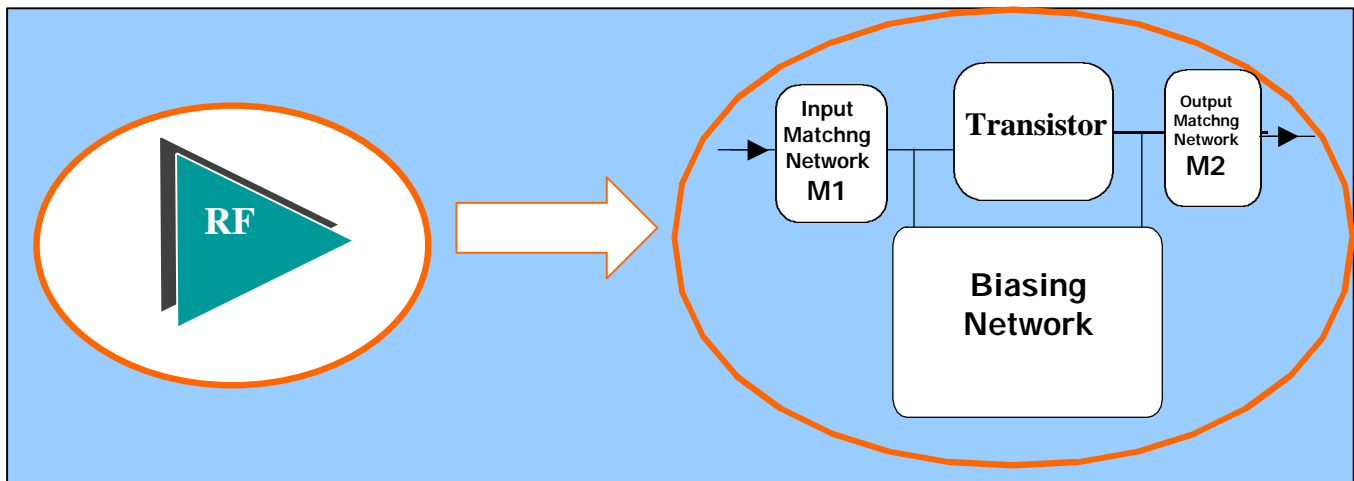

Figure 2: General Microwave Amplifier Topology

This was the basic topology that we adhered to through our design procedure. The basic design flow for this topology is as follows:

- Choose an Microwave Transistor based on design specifications
- Design a DC Biasing circuit for desired operation: Class A, Class B, Class C, or Class AB
- Design the Input and Output Matching Circuits based on the desired type of amplifier: Low-Noise Amp, High-Gain Amp, or High-Power Amp

Because our design is that of a high-power device, there is a more specific design flow to follow when designing a high-power microwave amplifier that is illustrated in the book, *Microwave Circuit Design Using Linear and Nonlinear Techniques* by Vendelin, Pavio, and Rohde. This design method is based strictly on using small-signal S-parameters for the design of M1 (the input matching circuit) and M2 (the output matching circuit). It also addresses the proper form of biasing for maximum output power. The design flow is as follows:

- Obtain transistor static IV curves
- Using IV curves, design the bias circuit for the transistor in order to achieve Class A operation
- Obtain the transistor S-parameters for the determined bias values
- Using IV curves, define the optimum load line for maximum output power and determine the resistance value, R_L, corresponding to this load line
- Design M2 for maximum output power using the value of R_L

- Determine S_{11}' with M2 at output and design input matching circuit, M1, for zero reflection.

The IV curve of the transistor is the starting point for the design. An example of one is shown below:
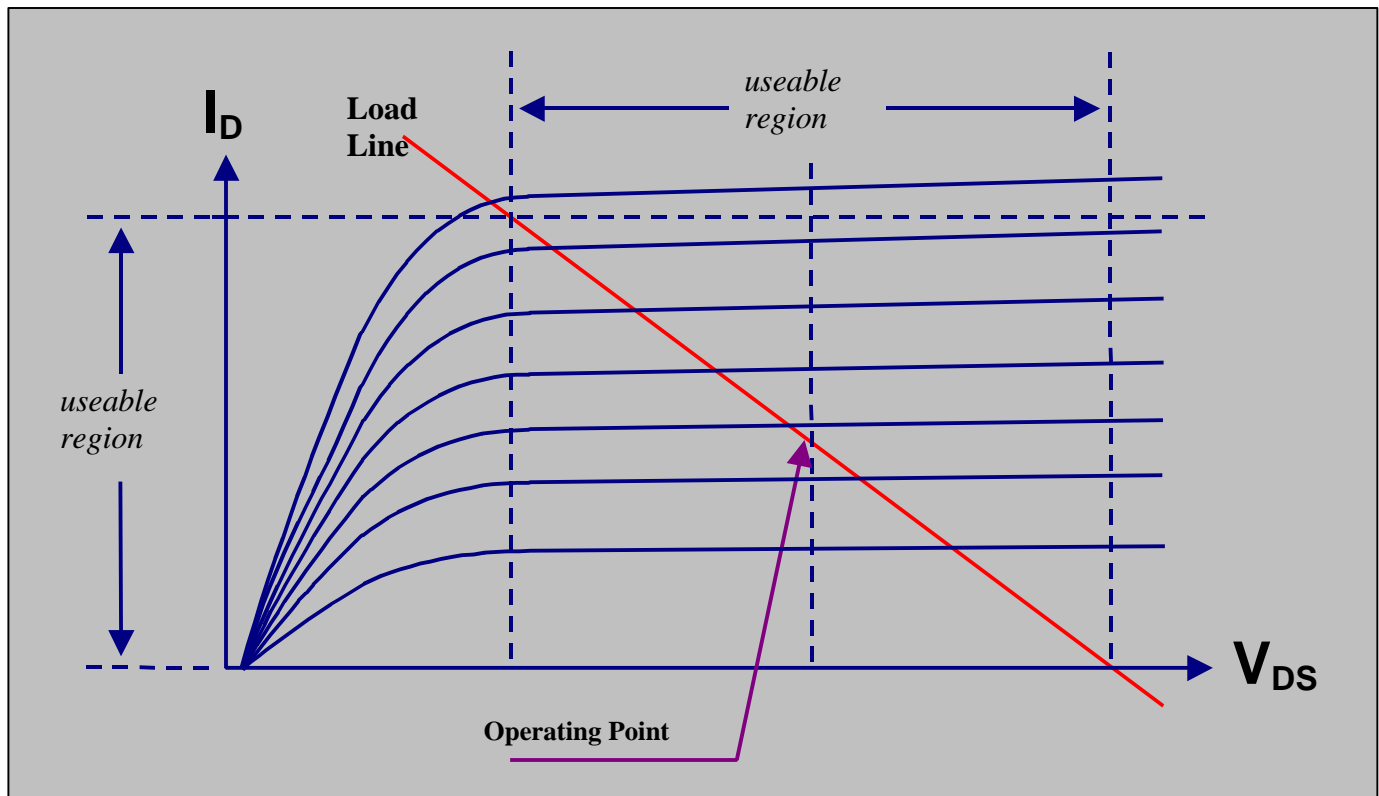

Figure 3: FET Transistor IV Curve

From the IV curve, the usable regions of I_D and V_{DS} can be determined. For Class A operation, the DC operating point should be centered in these usable regions. This determined operating point will define the V_{GS} and V_{DS} in the bias circuit design.

In order to obtain maximum power from this device, we must define a load line that fully spans these usable regions. The slope of this load line will determine the large-signal load impedance, R_L, for maximum transistor output power. In other words, R_L is used as the goal impedance to be presented to the device's drain terminal by the output circuit in order to achieve maximum RF power output. This value of R_L defines the output matching circuit, M2. The Smith chart is then used to define the lossless output circuit M2 by matching R_L to 50Ù at the design frequency.

With M2 designed, the input matching circuit, M1, can then be designed using S_{11}'. M1 should be designed for zero input reflection. To do this, the Smith chart is used by matching S_{11}' to 50Ù at the design frequency.

This design method should result in a high power amplifier with little input reflection, $\tilde{A}_{IN}$. It should be observed that the output match will be poor because it is intentionally mismatched in order to achieve maximum RF power generation. In other words, the output match is optimized on R_L rather than the device's S_{22}.

It should be noted that this design method for high power works even though small-signal S-parameters are used as a design basis. Ideally, large signal S-parameters should be used because power amplifiers are inherently large signal components. This is because they operate into the power saturation area of the IV curve which is, in most cases, a non-linear region. Ideally, a set of large-signal S-parameters would include these non-linearities and would characterize a transistor for high power applications but unfortunately device manufacturers do not provide them. This is because the measurement of large-signal S-parameters is difficult and is not properly defined. Fortunately, small-signal S-parameters are suitable for use in large-signal amplifier design when they are operating in Class A.

Although this design procedure may seem straight forward, the actual design process turned out to be much more involved.

Design Environment: Microwave Office

It was obvious from the start that our amplifier would need to be designed in the software environment if we actually wanted to build it. There are several software packages in the industry that are used for the design and simulation of RF circuits. The one that we chose to use was Applied Wave Research's Microwave Office. The primary reason for this choice was that we could obtain our own trial copy which gave us much more flexibility in the design process. Microwave Office is one of the top three industry standard RF design and simulation packages which also made it very attractive. Learning the use and capabilities of the software through the design process turned out to be very time consuming but the experience gained with the software will no doubt be invaluable in an RF career.
We also used Agilent Technology's Advance Design Software for parallel design and comparison in the early stages of design. This was done primarily to gain a little experience with comparable software.
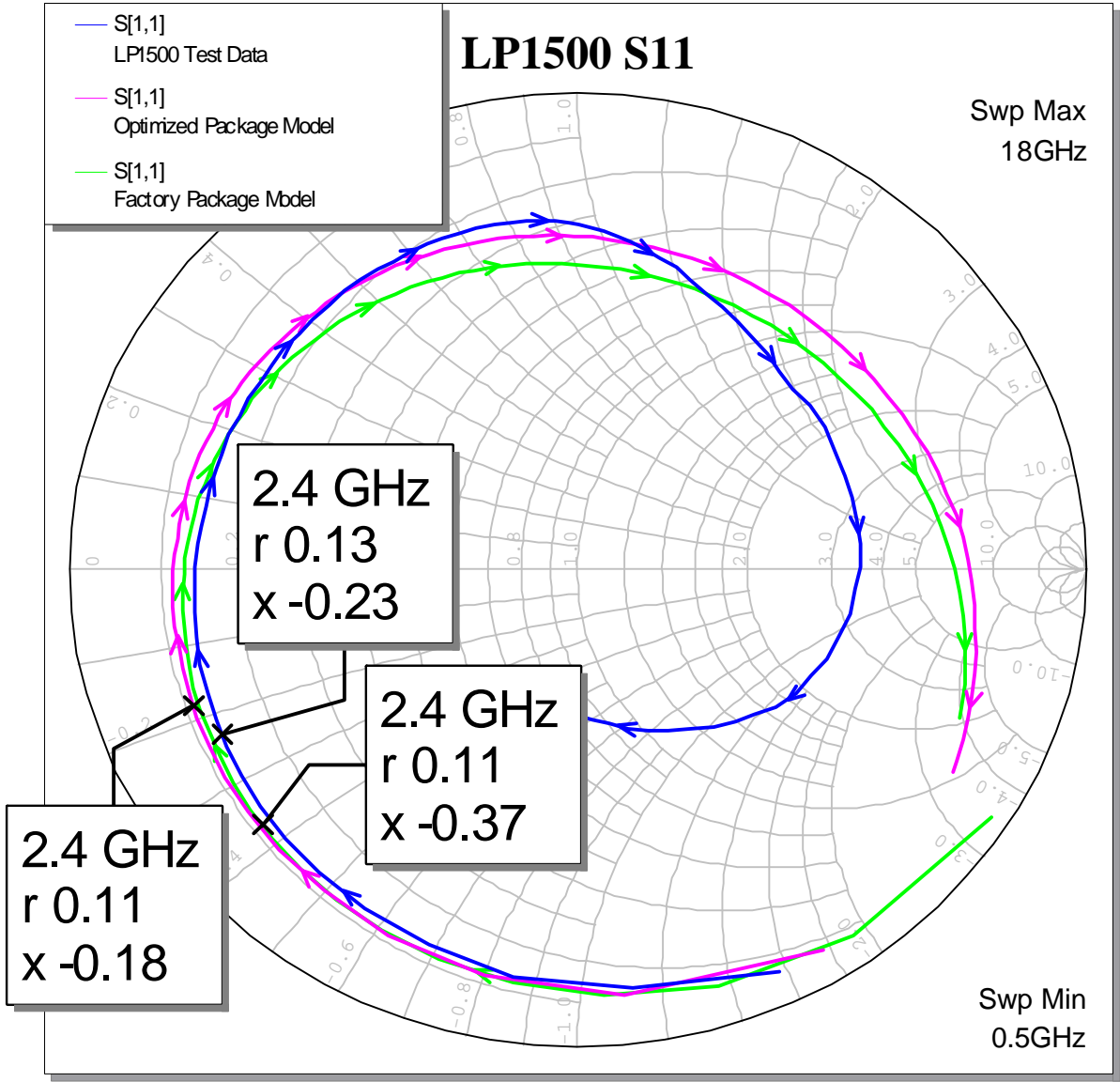
Design Phase I: Obtaining a Non-Linear Device Model

The first step in the whole design process was to choose a transistor. We chose the Filtronic LP1500 transistor in a P100 package which is a 1 Watt power PHEMT. The LP1500P100 is a packaged Aluminum Gallium Arsenide / Indium Gallium Arsenide (AlGaAs/InGaAs) pseudomorphic High Electron Mobility Transistor (pHEMT). This transistor was chosen because it met all of the requirements for our target specifications.
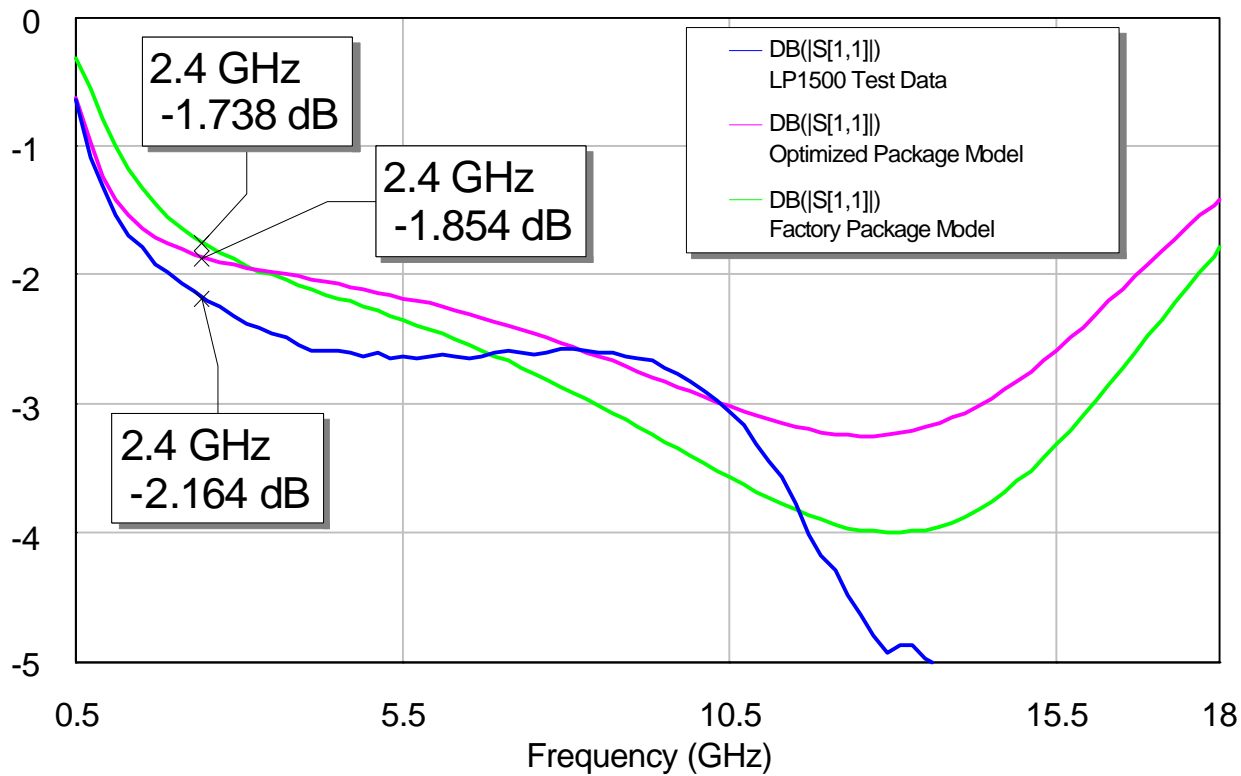
The most unexpected problems that we encountered when we started our design was that there are no perfect non-linear models for microwave transistors. The non-linear model given for the LP1500 does not generate the actual S-parameters of device test data that they also supply. Filtronics supplies, on their website, a Cutice-Cubic Non-Linear Device Model is given along with a set of actual S-parameters of a tested LP1500P100 device at a specific DC bias. But when we compared this test data with the S-parameters that are generated by the non-linear device model in Microwave Office simulation, the values did not match at our design frequency of 2.4 GHz. We found the solution to this problem by consulting a professional in the design field.   We were advised to optimize the non-linear device model for our design frequency by adjusting various parameter values in the non-linear model. The Curtice-Cubic non-linear device model that we obtained from Filtronics has a total of 36 parameters. The optimization procedure of the non-linear model involved changing arbitrary values one at a time, running S-parameter simulation,
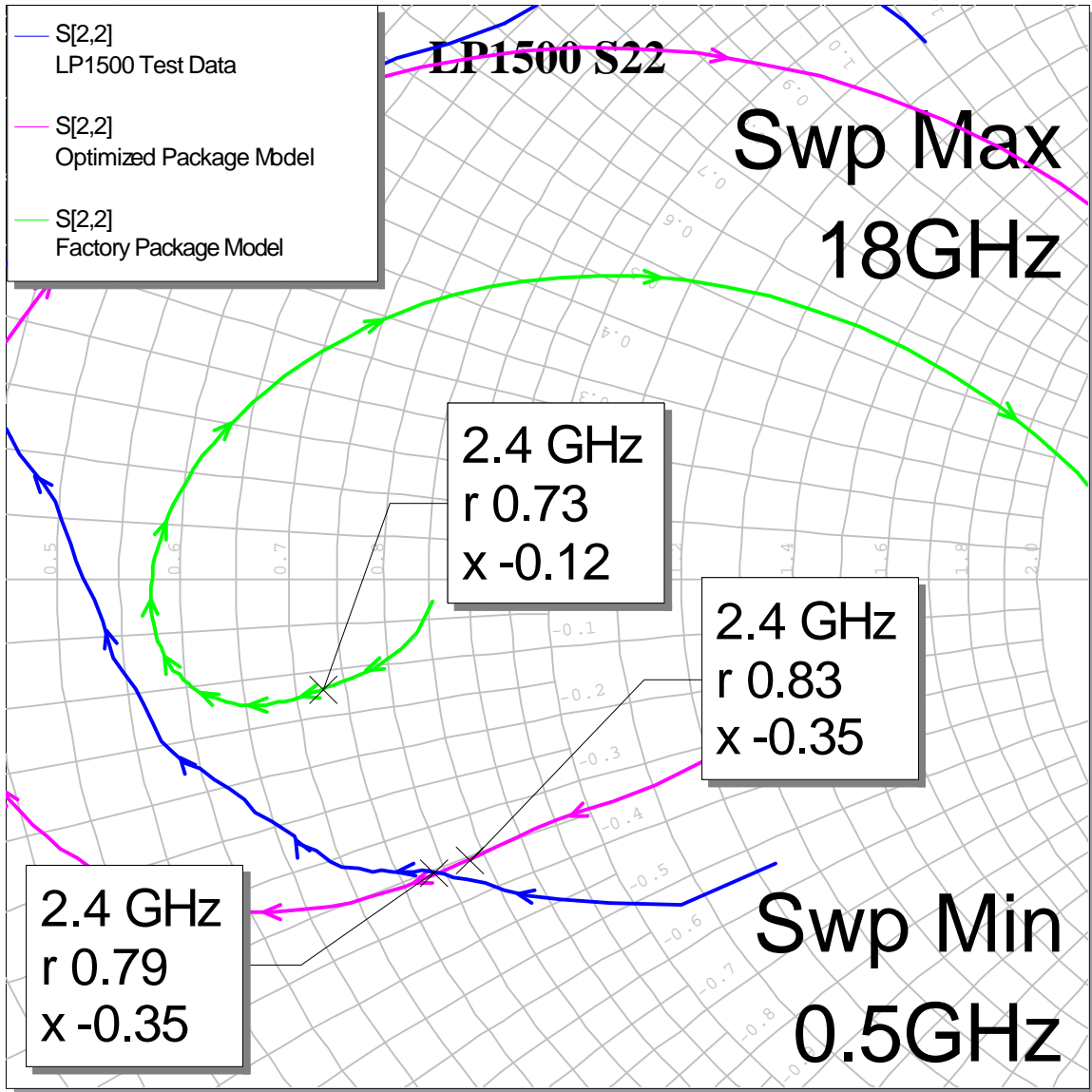
and comparing the results of simulation with that of the given device test data. This was an especially time consuming procedure because it is a hit-and-miss method. We first had to determine which of the 36 device model parameters made the most significant changes in the S-parameter simulation. Then we had to adjust them while watching all 4 S-parameters. This was quite frustrating because changing one parameter might bring one of the S-parameters values come with in the desired range but would, at the same time, make another S-parameter deviate further from the desired value. We realized how hard it was to bring every device model S-parameter close to that of the actual test data values, so we concentrated on optimizing the input and output matching S-parameters; S11 and S22 respectively, while allowing more error within the through parameters; S21 and S21. This decision was made because obtaining the right matching in the simulation environment would ensure good matching in the realized amplifier circuit. In other words, designing around a device model with S11 and S22 close to the actual device values should guarantee a properly matched circuit when it is actually built. It should be noticed that optimization would not necessarily be needed if the amplifier circuit were only to designed and tested in the software environment.

Below is a graphical representation of the actual device Test Data S-parameters (Blue Trace), the non-optimized model (Green Trace), and our final optimized device model (Pink Trace). Notice the optimization at our design frequency, 2.4 GHz of S11 and S22.
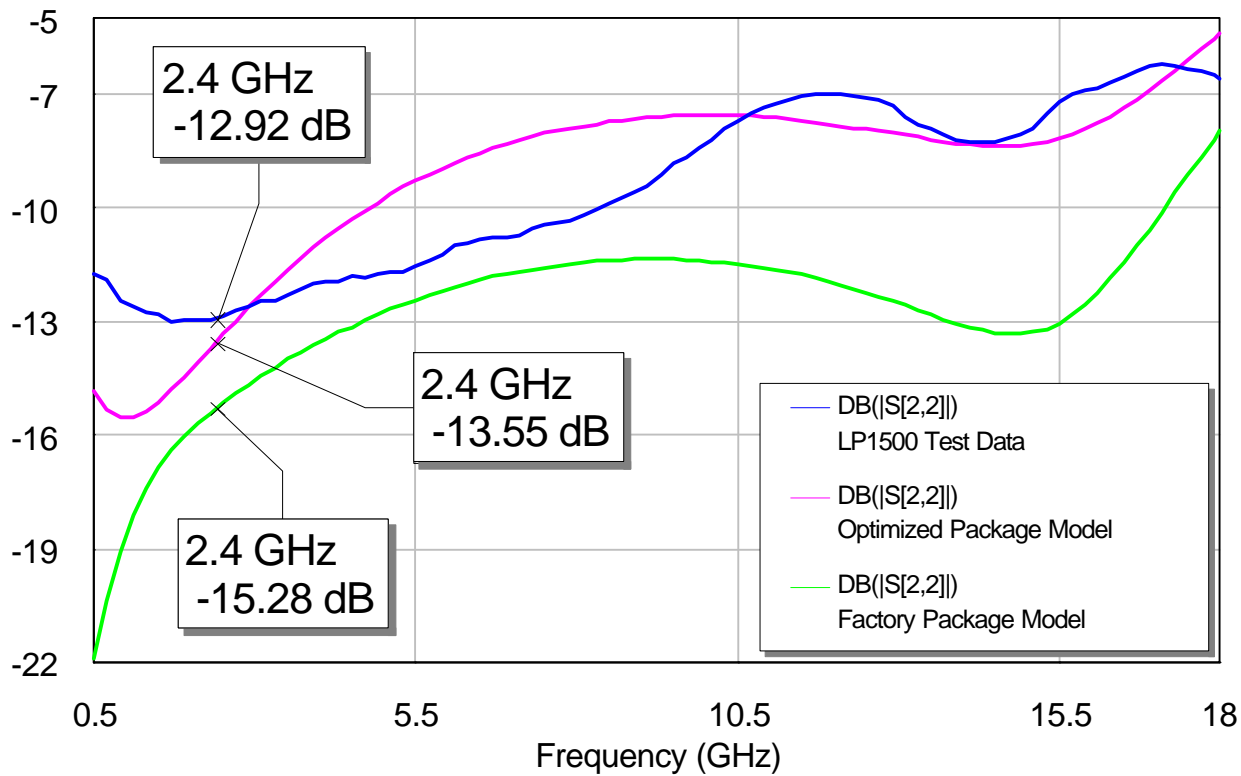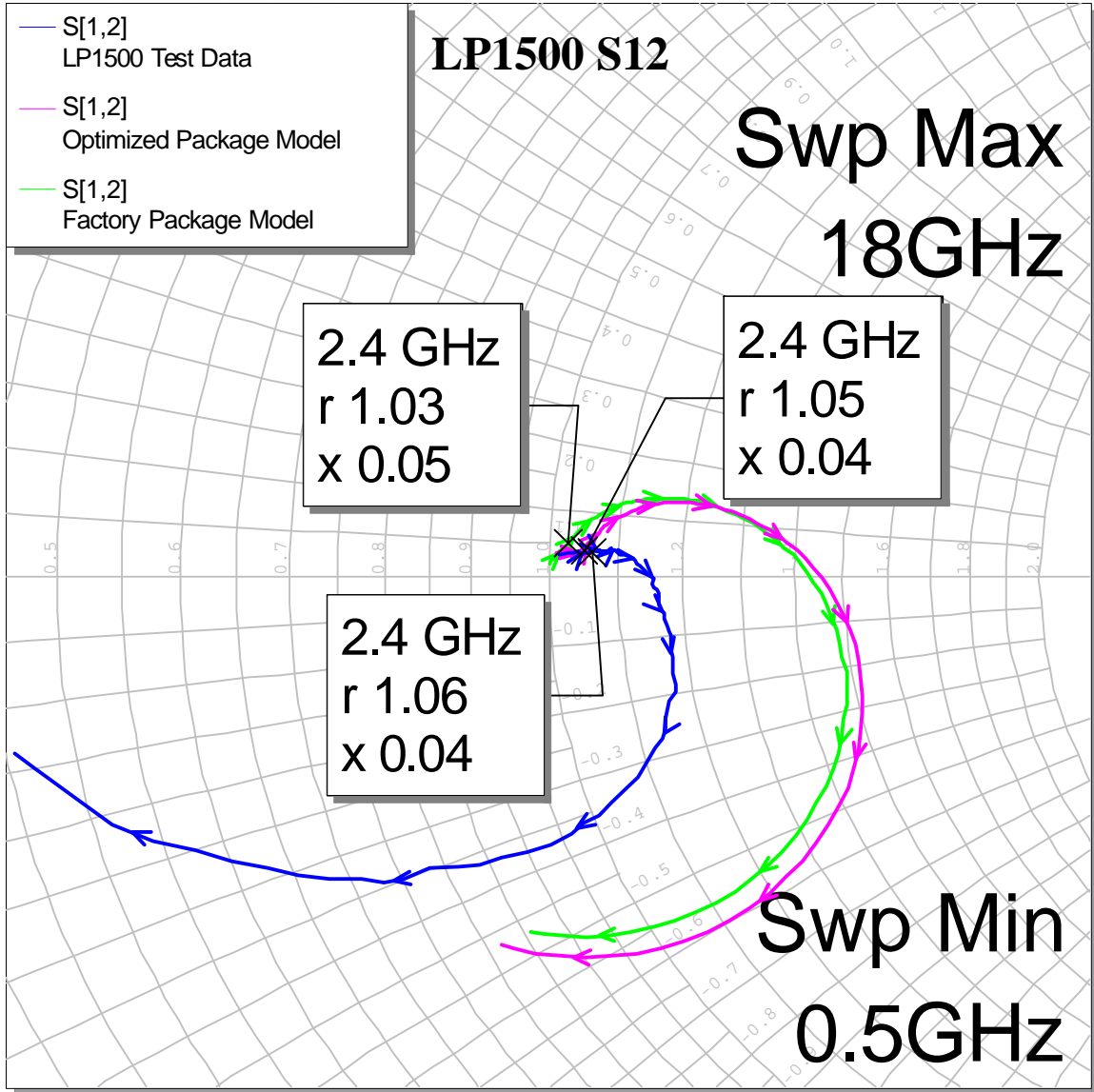
LP1500 S11

S[1,1]
LP1500 Test Data

S[1,1]
Optimized Package Model

S[1,1]
Factory Package Model

Swp Max
18GHz

2.4 GHz
r 0.13
x -0.23

2.4 GHz
r 0.11
x -0.37

2.4 GHz
r 0.11
x -0.18

Swp Min
0.5GHz

LP1500 S11

2.4 GHz
-1.738 dB

2.4 GHz
-1.854 dB

2.4 GHz
-2.164 dB

DB(|S[1,1]|)
LP1500 Test Data

DB(|S[1,1]|)
Optimized Package Model

DB(|S[1,1]|)
Factory Package Model

Frequency (GHz)

Legend:
- S[2,2] LP1500 Test Data
- S[2,2] Optimized Package Model
- S[2,2] Factory Package Model

LP1500 S22

Swp Max
18GHz

Swp Min
0.5GHz

2.4 GHz
r 0.73
x -0.12

2.4 GHz
r 0.83
x -0.35

2.4 GHz
r 0.79
x -0.35

LP1500 S22

2.4 GHz
-12.92 dB

2.4 GHz
-13.55 dB

2.4 GHz
-15.28 dB

DB(|S[2,2]|)
LP1500 Test Data

DB(|S[2,2]|)
Optimized Package Model

DB(|S[2,2]|)
Factory Package Model

Frequency (GHz)

LP1500 S12

Swp Max
18GHz

Swp Min
0.5GHz

S[1,2]
LP1500 Test Data

S[1,2]
Optimized Package Model

S[1,2]
Factory Package Model

2.4 GHz
r 1.03
x 0.05

2.4 GHz
r 1.05
x 0.04

2.4 GHz
r 1.06
x 0.04

LP1500 S12

2.4 GHz
-29.12 dB

2.4 GHz
-30.11 dB

2.4 GHz
-30.89 dB

DB(|S[1,2]|)
LP1500 Test Data

DB(|S[1,2]|)
Optimized Package Model

DB(|S[1,2]|)
Factory Package Model

Frequency (GHz)

LP1500 S21

Mag Max
20

Swp Max
18 GHz

2.4 GHz
Re 0.84
Im 4.24

2.4 GHz
Re 1.36
Im 6.79

2.4 GHz
Re -0.04
Im 5.07

—— S[2,1]
LP1500 Test Data

—— S[2,1]
Optimized Package Model

—— S[2,1]
Factory Package Model

5
Per Div

Swp Min
0.5 GHz

LP1500 S21

Legend:
- DB(|S[2,1]|) LP1500 Test Data
- DB(|S[2,1]|) Optimized Package Model
- DB(|S[2,1]|) Factory Package Model

Annotations:
- 2.4 GHz 16.81 dB
- 2.4 GHz 14.09 dB
- 2.4 GHz 12.72 dB

X-axis: Frequency (GHz)
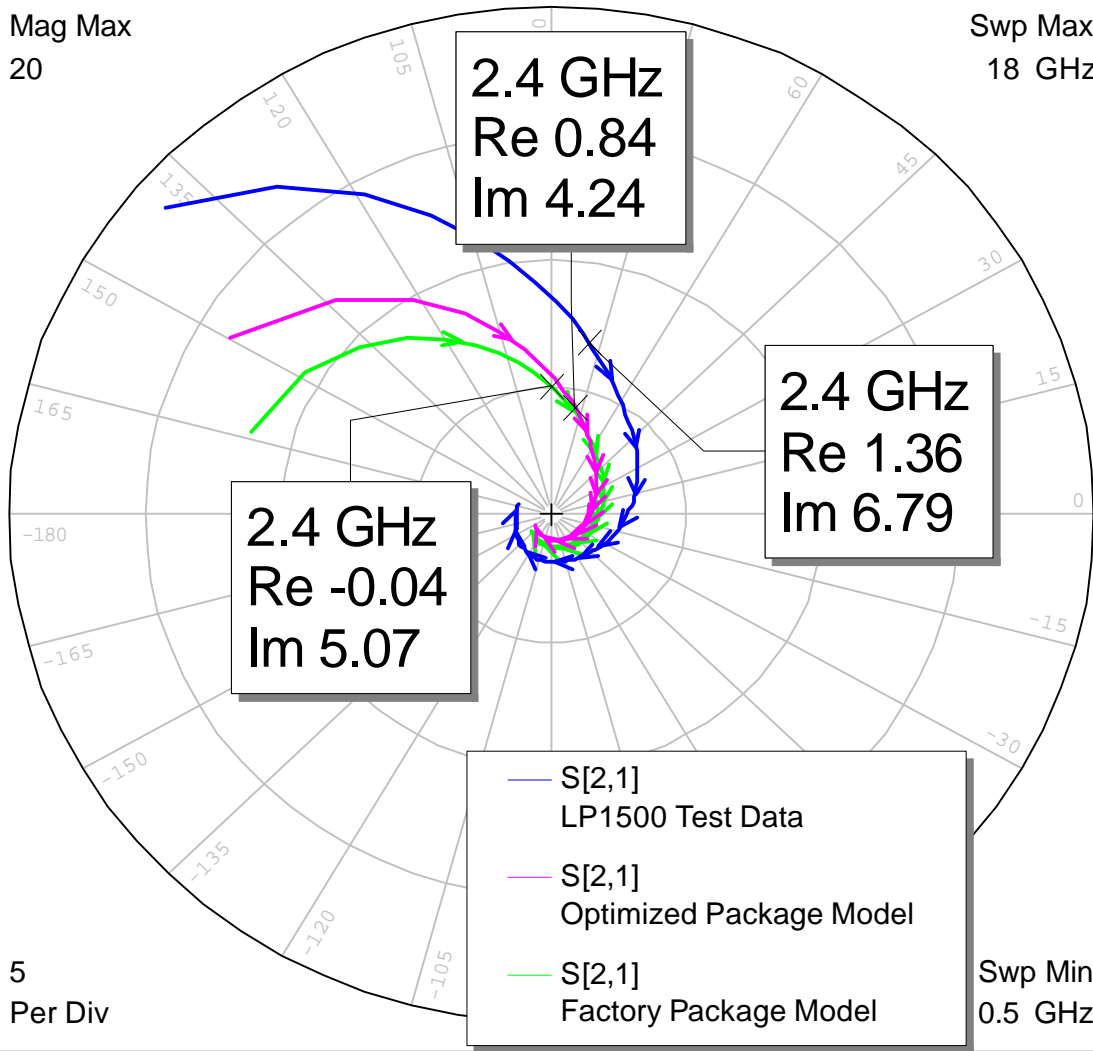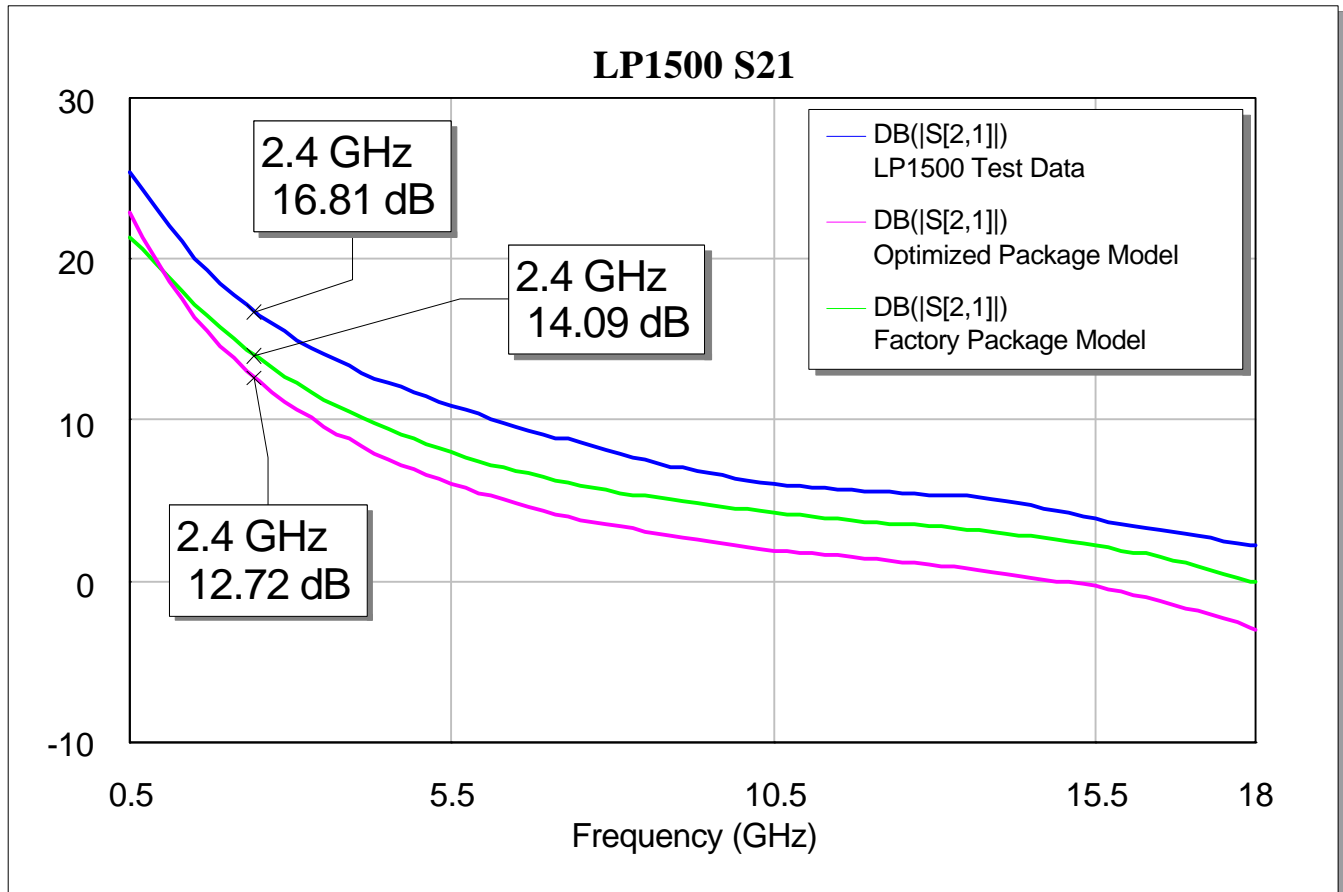
## Design Phase II: IV Curve

With an acceptable device model obtained, the actual design process could begin. The curvetracer in Microwave Office was used to generate the LP1500 IV curves from which an operating point and load line could be determined.
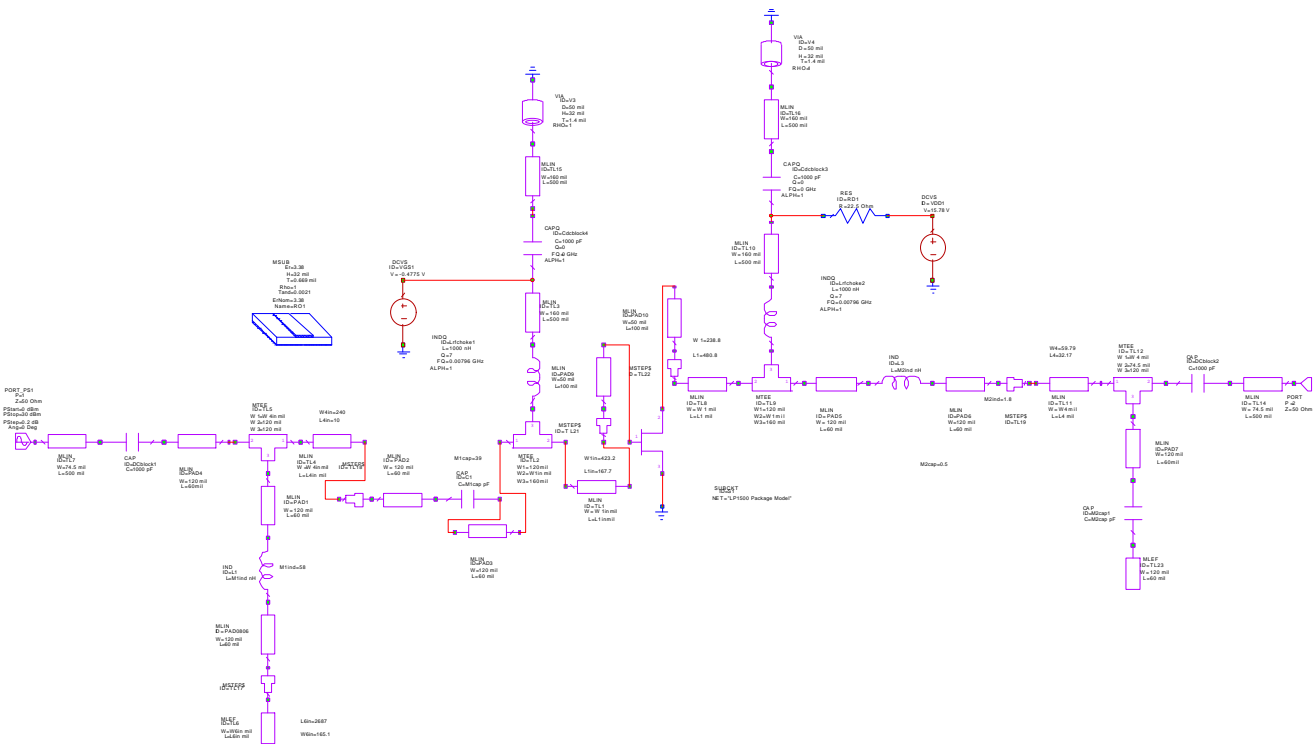
IV Curve of LP1500

Legend: IVCurve (mA), CurveTrace

X-axis: Voltage (V)
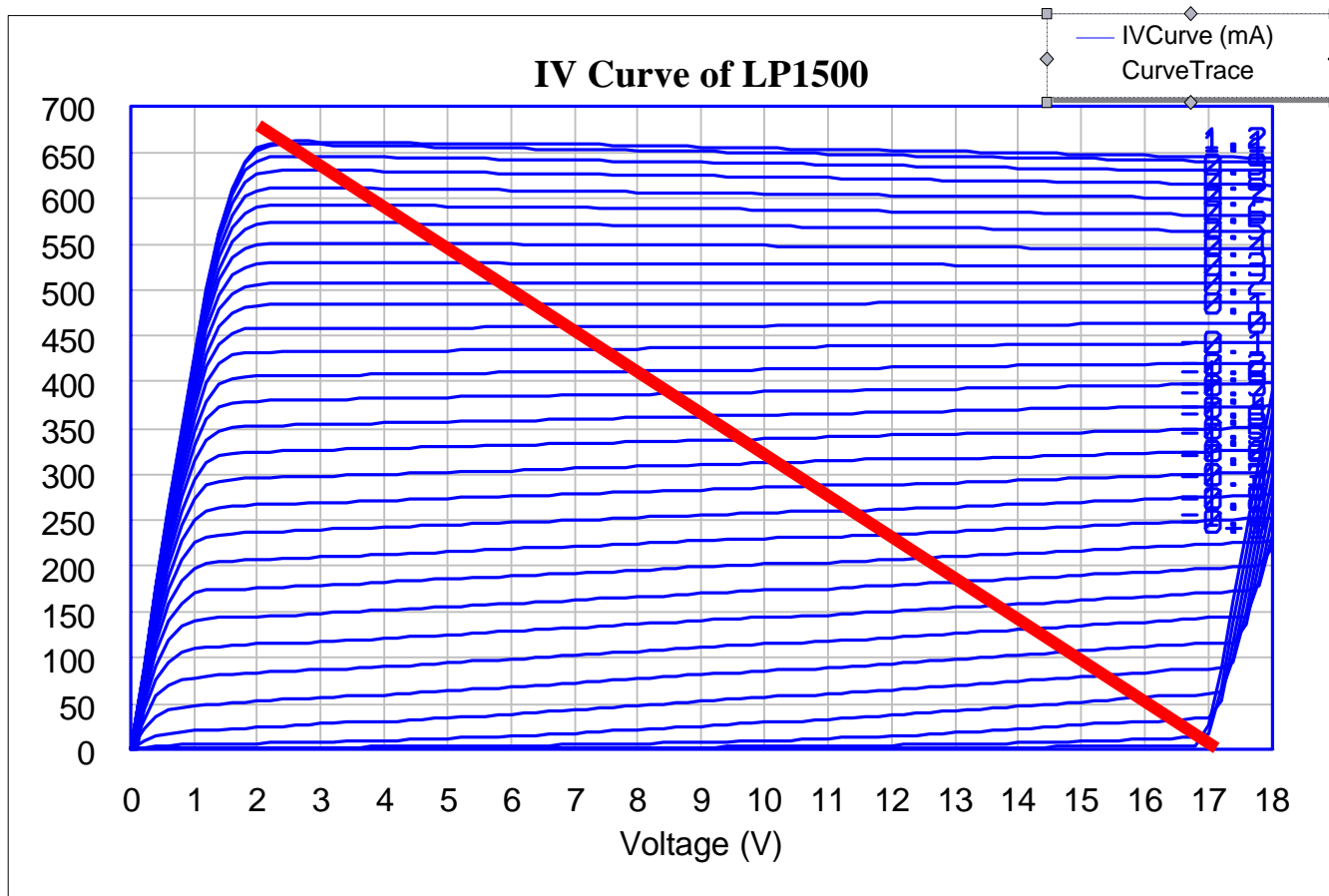
From this IV curve, the operating point was designed. The DC bias values turned out to be VDD=8.5 Volts and VGS= -0.5 Volts. The maximum power load line was determined and has a RL value of 22 ohms. RL was then translated to the Smith Chart and matched to 50 ohms using lumped elements.

Smith Chart

RL= 22

Match to 50

Swp Max

1

0.8
1.0
0.6
2.0
0.4
3.0
4.0
5.0
0.2
10.0

0   0.2   0.4   0.6   0.8   1.0   2.0   3.0 4.0 5.0   10.0
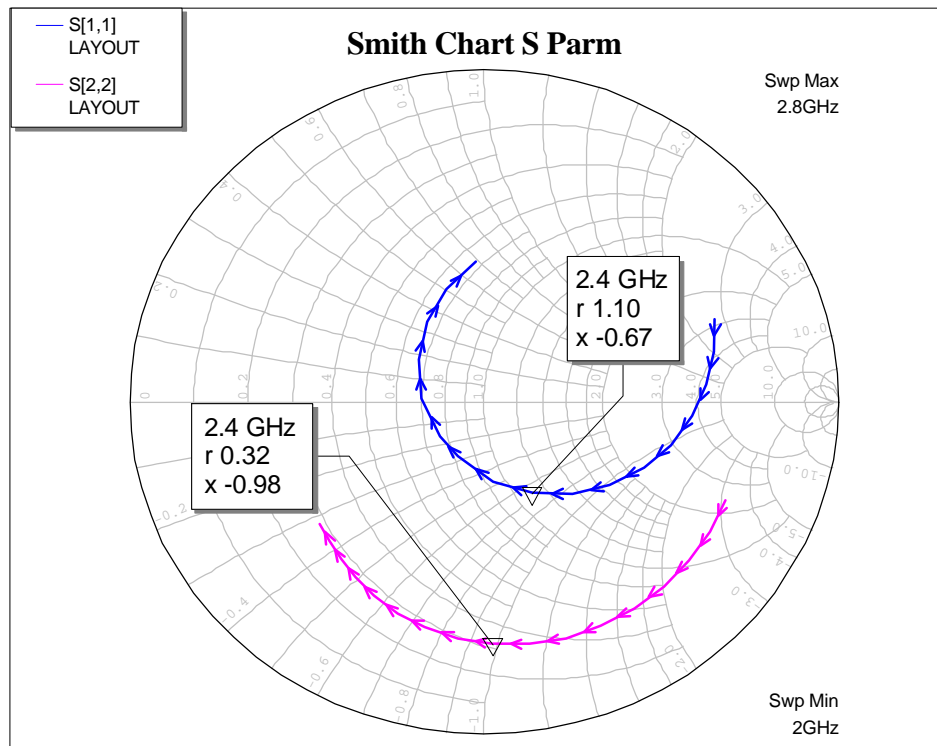
-0.2
-10.0

-5.0
-4.0
-0.4
-3.0

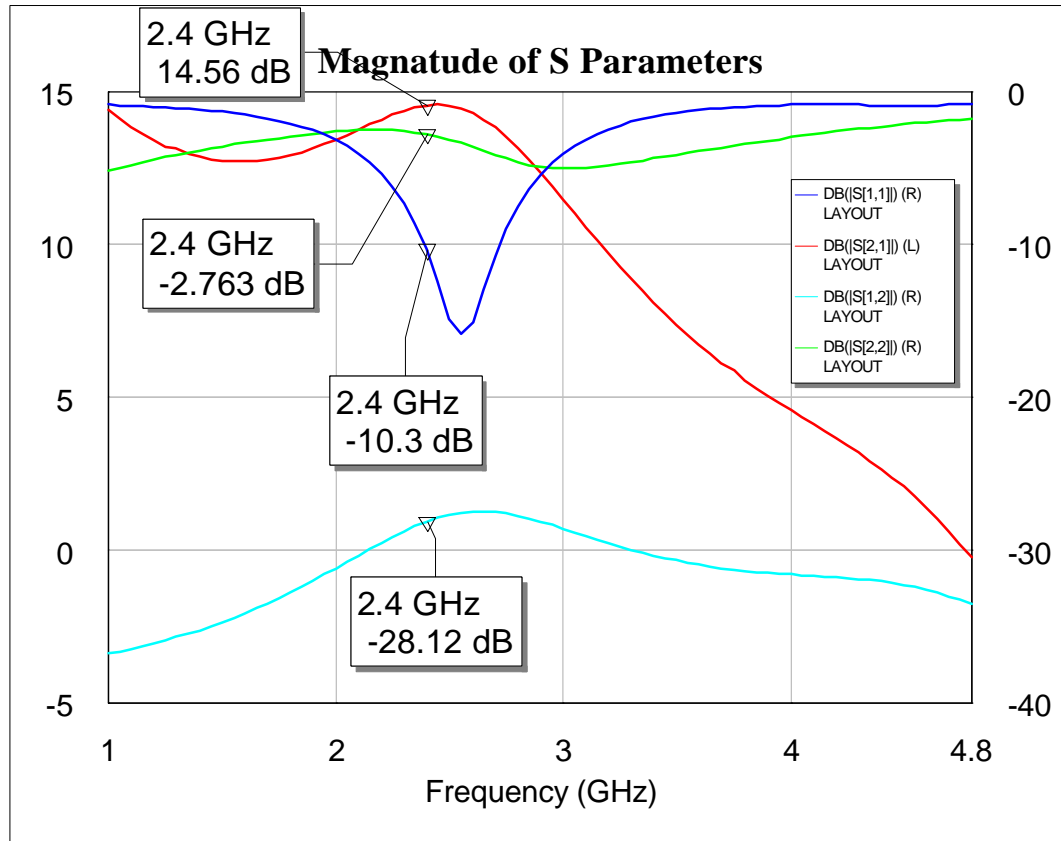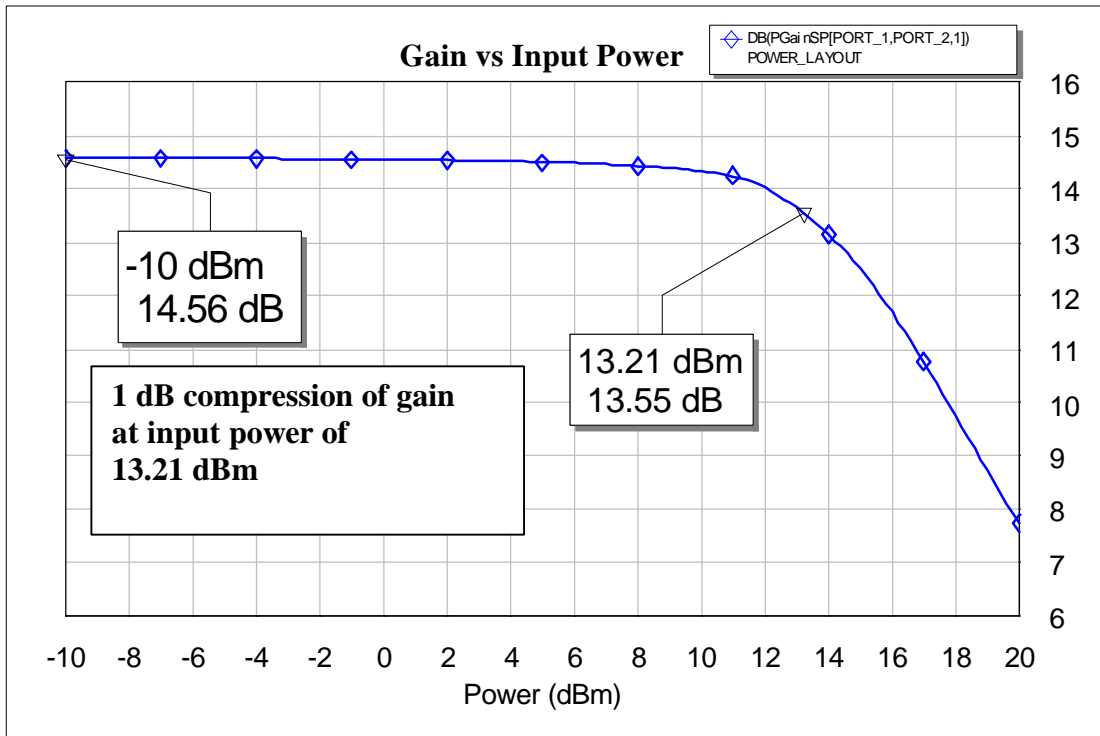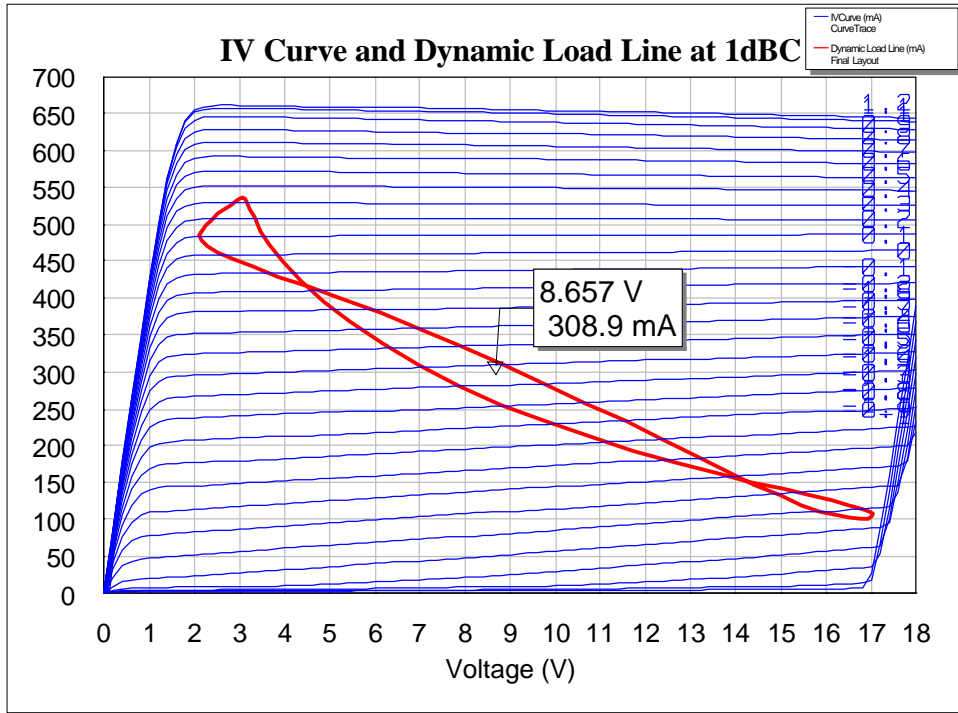-0.6
-2.0
-0.8
-1.0

Swp Min

-1
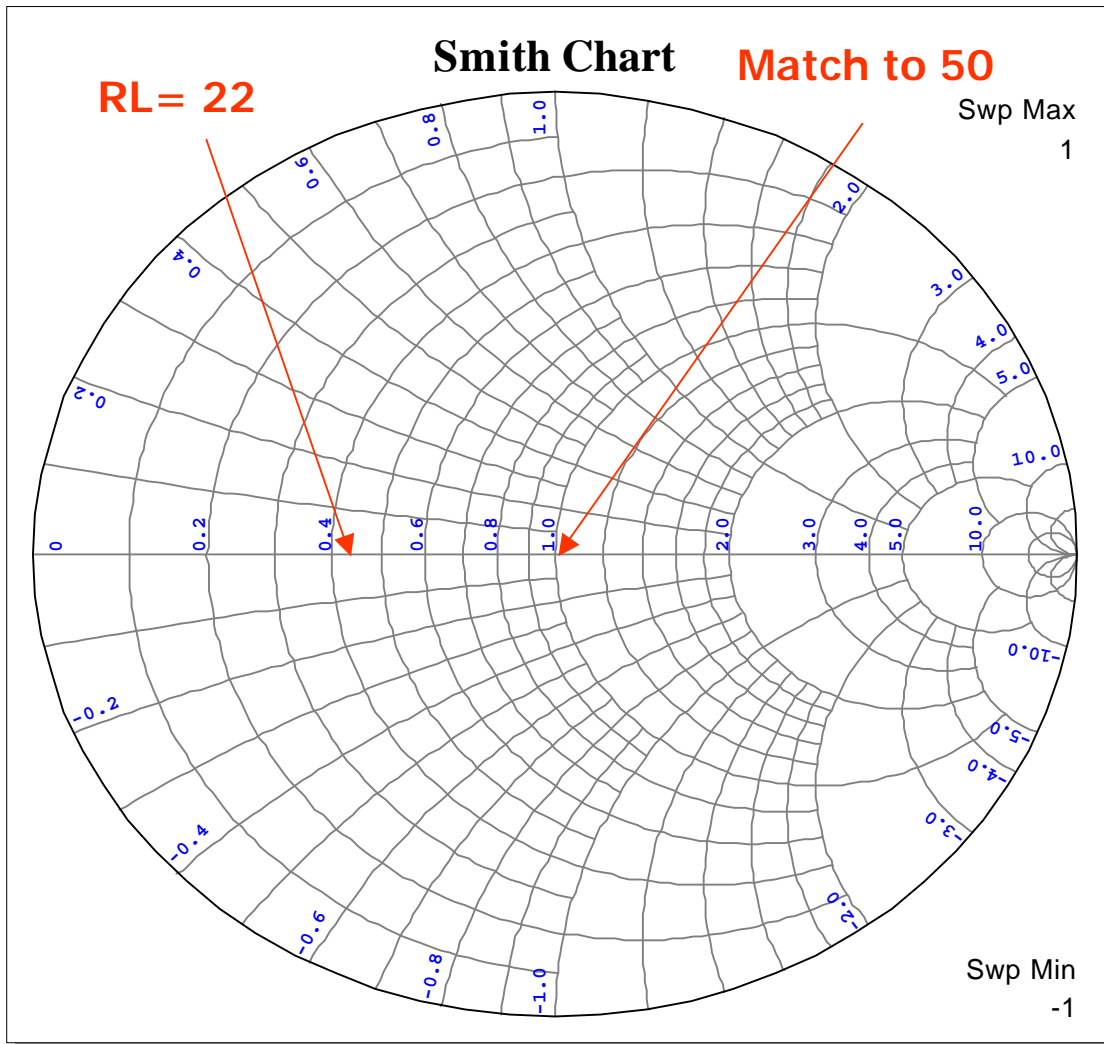
This determined the output match M2. M1 was then designed using S11' on the smith chart as described earlier. The final lumped element circuit is shown below.
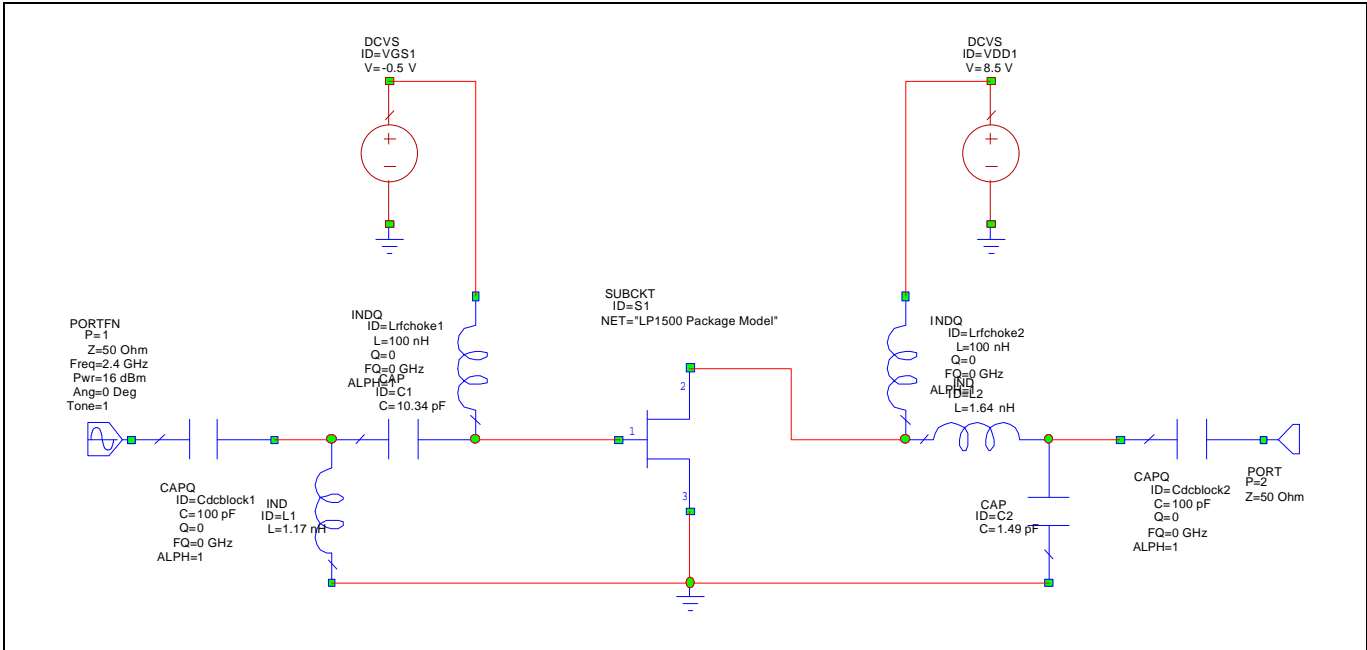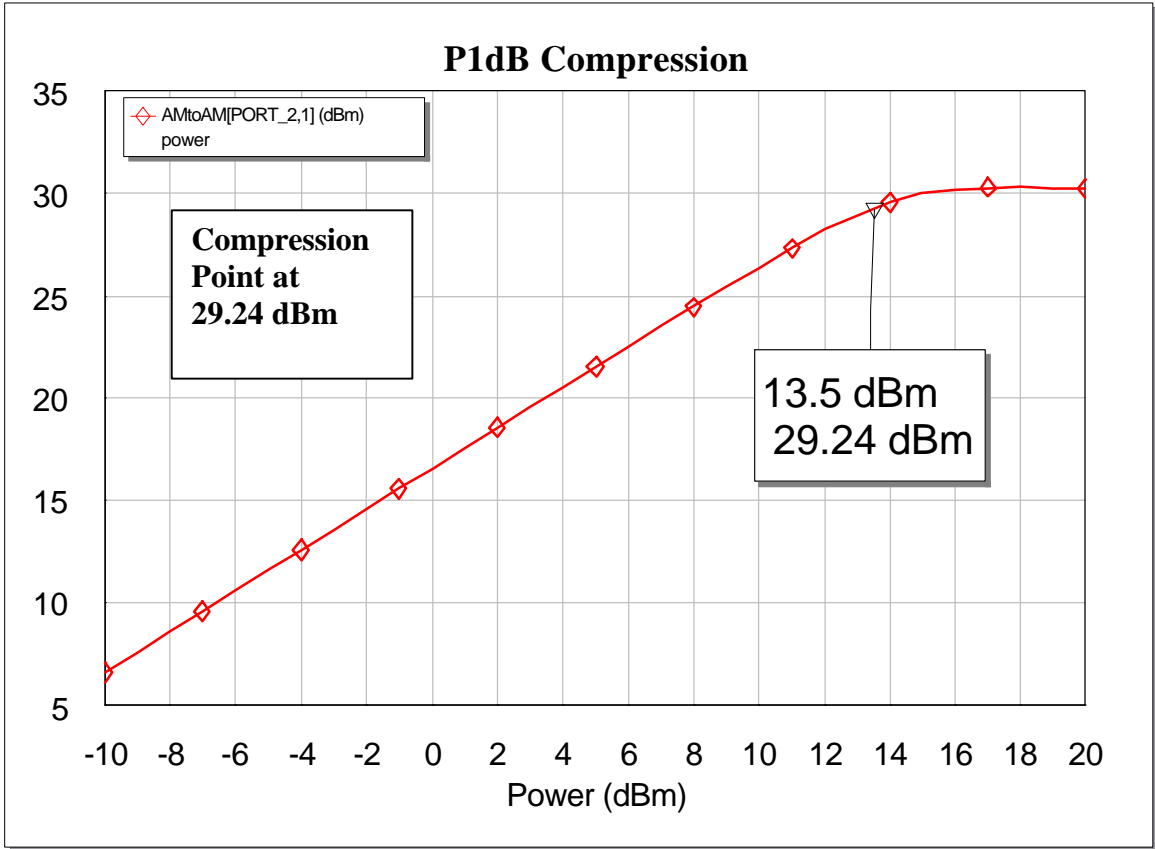
Because the circuit was to be built on a substrate, a mixed lumped element microstrip design had to be generated based on the above design. This is because every connection between all of the elements are in actuality microstrip pieces and therefore had to be considered and modeled in the design. This was a very long and drawn out process but it finally yielded a working circuit. This is the final circuit in Microwave Office along with the S-parameters and 1 dB compression point determination:

Magnatude of S Parameters

2.4 GHz
14.56 dB

2.4 GHz
-2.763 dB

2.4 GHz
-10.3 dB

2.4 GHz
-28.12 dB

15

10

5

0

-5

0

-10

-20

-30

-40

DB(|S[1,1]|) (R)
LAYOUT

DB(|S[2,1]|) (L)
LAYOUT

DB(|S[1,2]|) (R)
LAYOUT

DB(|S[2,2]|) (R)
LAYOUT

Frequency (GHz)

1   2   3   4   4.8

Smith Chart S Parm

S[1,1]
LAYOUT

S[2,2]
LAYOUT

Swp Max
2.8GHz

2.4 GHz
r 1.10
x -0.67

2.4 GHz
r 0.32
x -0.98

Swp Min
2GHz

IV Curve and Dynamic Load Line at 1dBC

IVCurve (mA)
CurveTrace
Dynamic Load Line (mA)
Final Layout

8.657 V
308.9 mA

Voltage (V)

Gain vs Input Power

DB(PGai nSP[PORT_1,PORT_2,1])
POWER_LAYOUT

-10 dBm
14.56 dB

**1 dB compression of gain
at input power of
13.21 dBm**

13.21 dBm
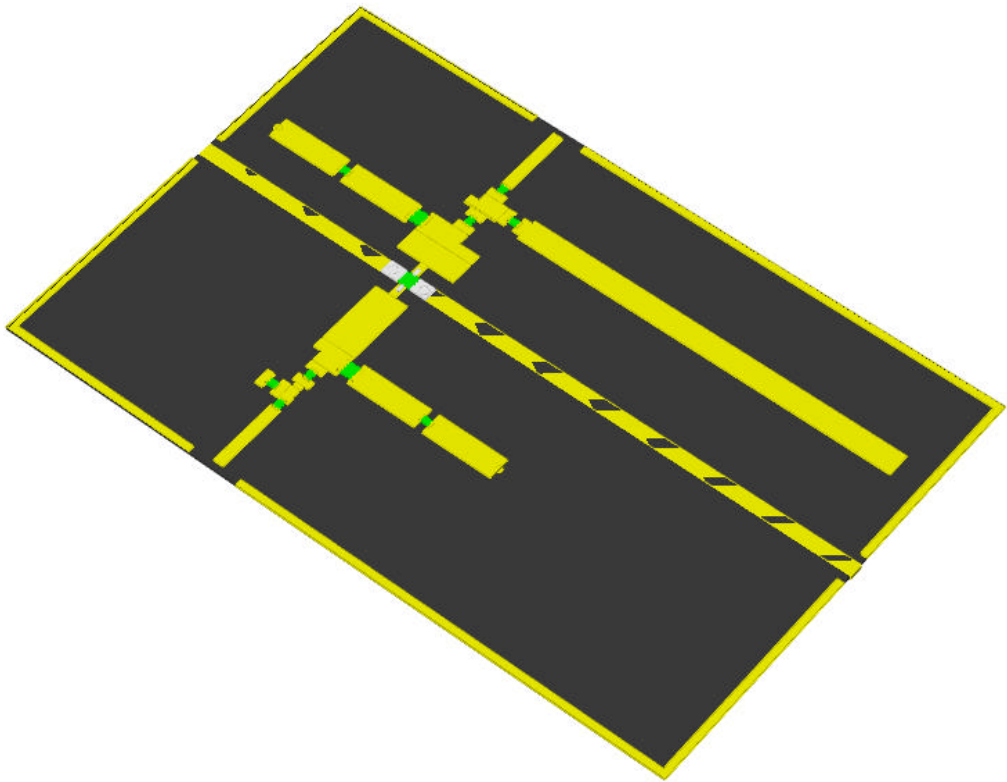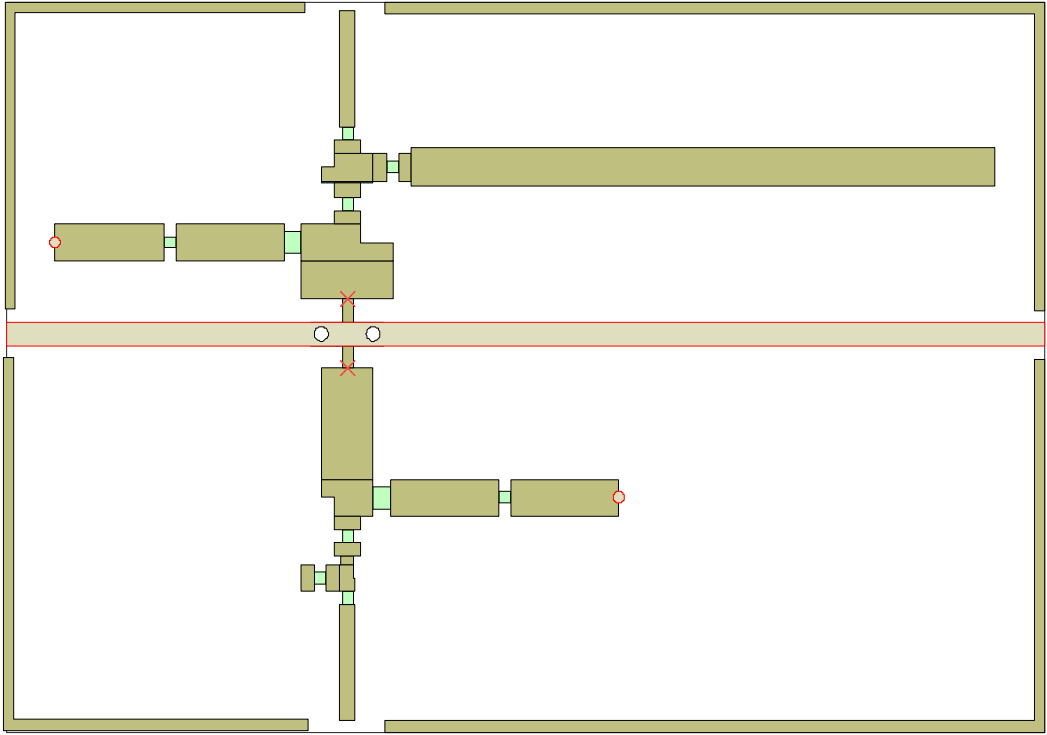13.55 dB

Power (dBm)

P1dB Compression

Which, in physical layout looks like this:

This layout was translated to the appropriate file for the circuit milling machine after which the circuit was built and tested.