Millimeter - Wave CMOS Power Amplifiers Design

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By

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University of California, Berkeley

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Abstract

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Professor Ali M. Niknejad, Chair

In the last few years we have seen an increased interest in millimeter-wave CMOS circuits and communication systems both in academia and industry. The feasibility of CMOS circuits at 60 GHz, the rising interest in digital video, short range, and other high data rate applications, along with the worldwide availability of unlicensed spectrum around 60 GHz have spurred a wave of research targeting integrated 60 GHz CMOS transceivers as a way to achieving low cost, highly integrated, high bandwidth, high data rate communication systems.

In recent years, a number of 60 GHz CMOS building blocks and integrated receivers have been demonstrated. However, the low supply voltage, thin gate oxide, low breakdown voltage, lossy silicon substrate, and power gain - output power tradeoff of CMOS technology result in the millimeter wave power amplifier being the most difficult block to implement in CMOS. A number of 60 GHz CMOS power amplifiers employing different topologies have been reported to date, however the output power has been relatively low, limiting the amplifiers to short-range applications. It is becoming

increasingly important to use more efficient power combining techniques in order to increase the output power capability of power amplifiers in order to enable medium and long-range applications.

This research aims at exploring the challenges facing the design and implementation of 60 GHz power amplifiers in standard 90 nm CMOS processes. The design, modeling, and layout optimization of both passive structures such as transmission lines, capacitors, RF pads as well as active devices operating at 60 GHz are investigated. A low-loss power combining technique taking advantage of millimeter-wave amplifiers topologies is presented. Four power amplifiers are implemented in a standard 90 nm 1V CMOS process. Record performance is reached in terms of 1dB compression and saturation output power.

Professor Ali M. Niknejad, Chair Date

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If only one page of this dissertation is worth reading, it is this one.

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My thanks go to my parents who poured all what they had into me to see this day. My father provided me an education he could not afford and my mother taught me how to fight and fight and never give up on my goals.

My respect goes to Abir, my wife, who believed in me when I was a teenager and stood by me in the ups and downs, when I was right and when I was wrong, and never doubted my abilities.

My heart goes to Lana. Lana is why I wake up every morning, and Lana is why I stay awake many nights. Lana is all what I live for.

Majd, my newborn son, made sure to always wake me up in the middle of the night to finish writing my thesis.

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My appreciation goes to Lina and Ghassan Chehab, the best friends I ever had, people who shaped me in many ways.

My Ph.D. years at Berkeley could have been easily cut in half if not for the time spent with my family: Lana and Hisham Noeimi, Dima and Ammar Rafei, Dina and Mahmoud Hachem, Mohammad and Soumaya Zalloukh, Nadia and Ziad Hafza. These people will never comprehend what they mean to me. People who make abroad feel like home.

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To the memory of my father

To my mother

Table of Contents

CHAPTER 1

INTRODUCTION

1 Introduction

1.1 Motivation for 60 GHz CMOS Power Amplifiers

In the last few years we have seen an increased interest in millimeter-wave (mm-wave) circuits and communication systems both in academia and industry. The feasibility of CMOS circuits at 60 GHz, the rising interest in digital video, short range, and other high data rate applications, along with the worldwide availability of unlicensed spectrum around 60 GHz as shown in Figure 1.1 have spurred a wave of research targeting integrated 60 GHz CMOS transceivers as a way to achieving low cost, highly integrated, high bandwidth, high data rate communication systems.

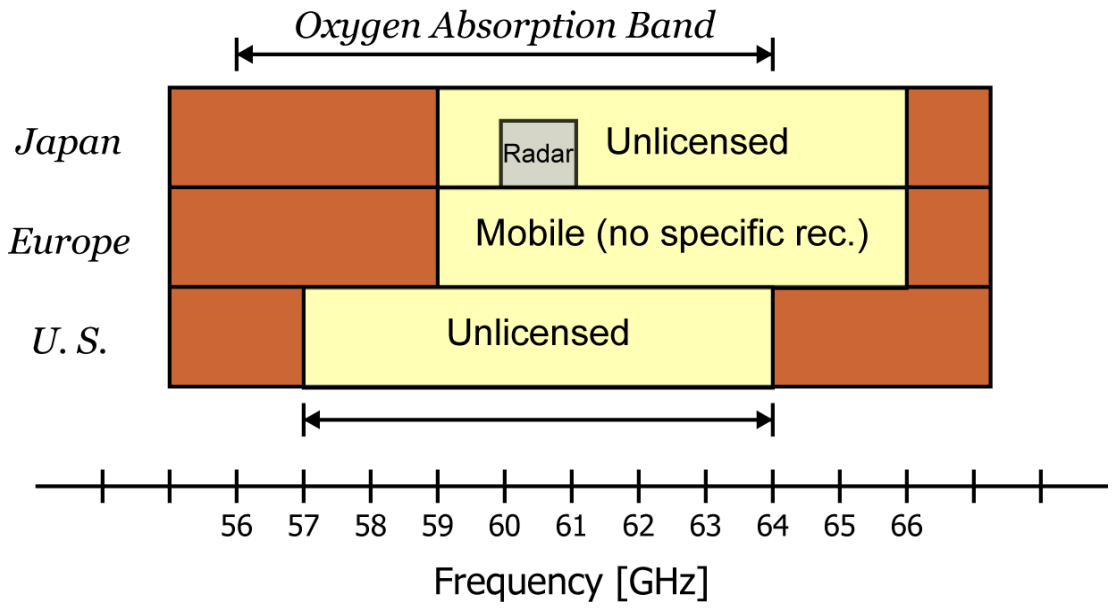

Figure 1.1: Allocation of spectrum around 60 GHz in the U.S., Japan, and Europe

While SiGe and III-V technologies are in general more suitable for mm-wave applications as they provide higher speed active devices and lower loss substrates, CMOS technology provides substantive advantages including low cost and potential of integration with other parts of the system which makes it a natural candidate for exploration. Moreover, the performance of CMOS technologies is continuously improving. Decreasing minimum feature size with every new generation leads to higher speed devices as shown in Figure 1.2. The unity current gain frequency (f_T) for the 90 nm technology node is above 100 GHz and it is continuing to increase for smaller nodes, reaching 280 GHz for 45 nm processes [1].

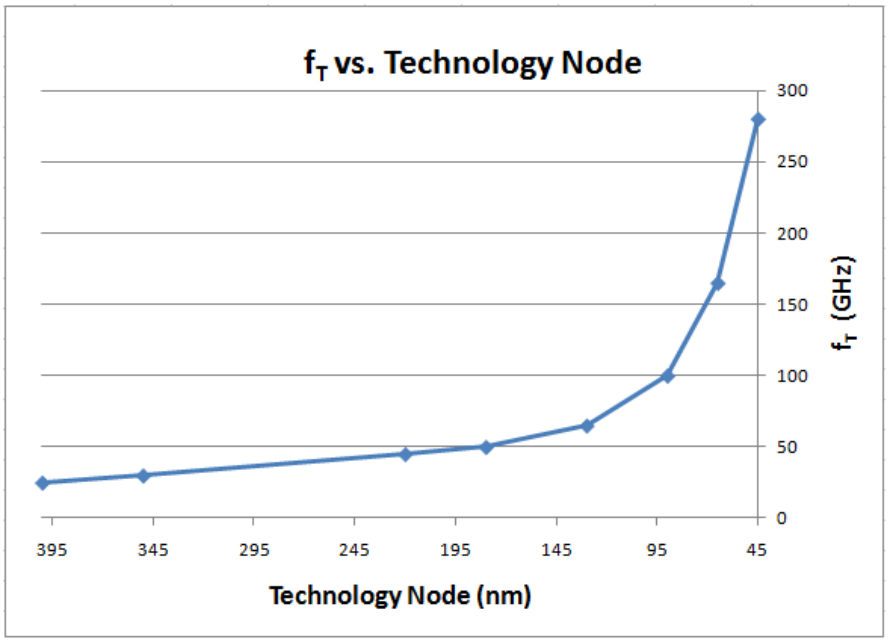

Figure 1.2: f_T vs. CMOS technology node

In recent years, a number of 60 GHz CMOS building blocks [2-7] have been demonstrated, and even complete 60 GHz integrated receivers [8-10] as the one shown in Figure 1.3 have been published.

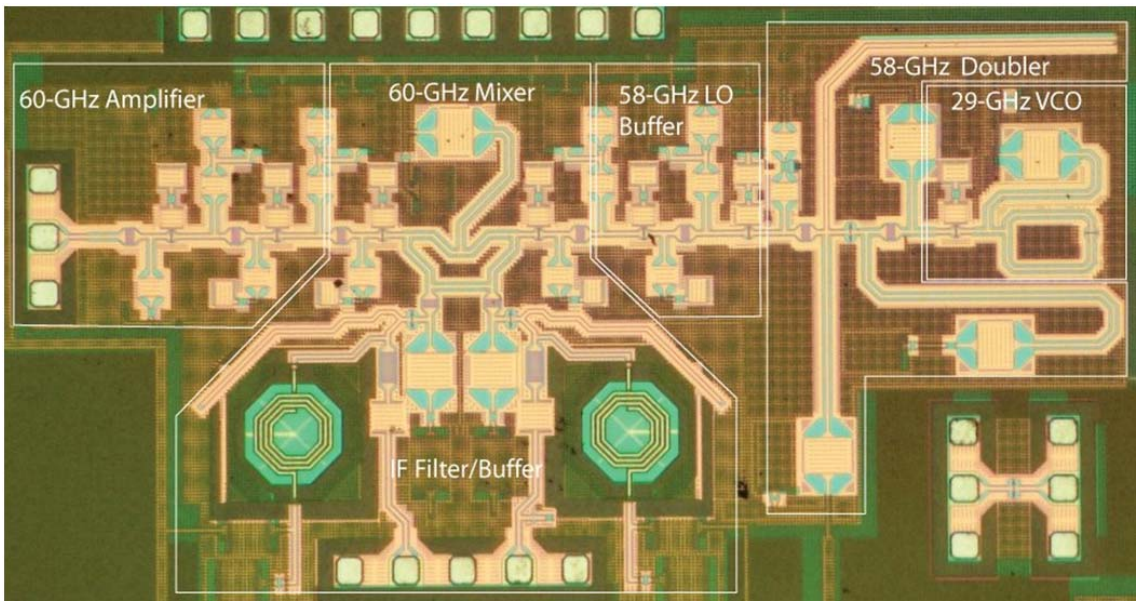

Figure 1.3: Die photo of a 60 GHz CMOS integrated receiver published in [8]

However, the low supply voltage, thin gate oxide, low breakdown voltage, and lossy Si substrate of CMOS technology result in the mm-wave power amplifier being the most difficult block to implement in CMOS. Many of the techniques used to realize high output power levels in the low GHz regime cannot be used at frequencies around 60 GHz because they necessitate the application of large CMOS transistors with a high degree of parasitics which considerably reduces the power gain at mm-wave frequencies. Thus, techniques other than using large bulky transistors need to be used in order to realize power amplifiers operating at mm-wave frequencies.

1.2 Existing 60 GHz CMOS Power Amplifiers

A number of 60 GHz CMOS power amplifiers have been reported to date [11-19], however the output power has been relatively low, limiting the amplifiers to short-range applications. It is becoming increasingly important to use more efficient power combining techniques in order to increase the output power capability of power amplifiers in order to enable medium and long-range applications.

In [11], a single-stage, single-ended power amplifier whose schematic is shown in Figure 1.4 is implemented in a 65 nm bulk CMOS process operating from a 1.2 V supply.

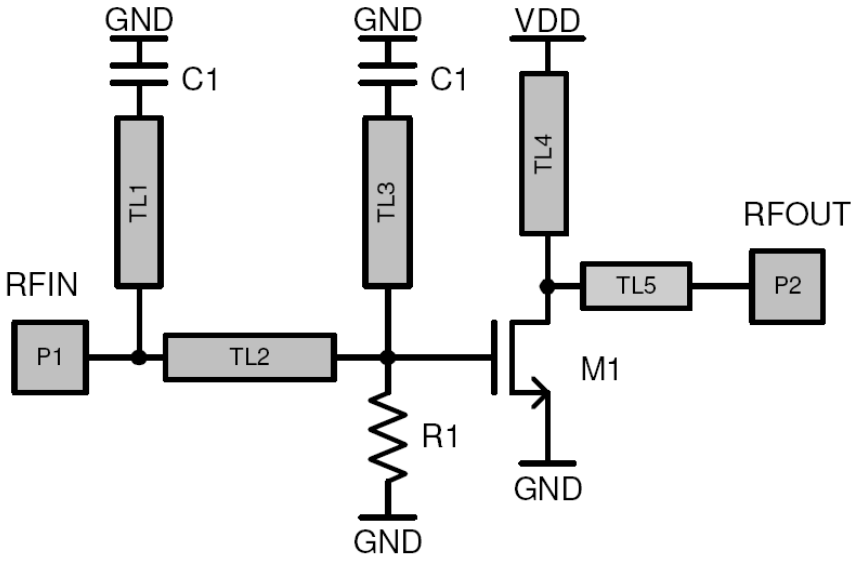

Figure 1.4: Schematic of single stage power amplifier presented in [11]

The amplifier achieves a peak power gain of 4.5 dB with 1 dB compression and saturation output power levels of +6 dBm and +9 dBm respectively with peak power added efficiency of 8.5%. While the layout, size, bias level, input impedance, and output impedance of the active device in a single stage power amplifier can be all optimized to

achieve the high output power with acceptable power gain, the fundamental mm-wave transistor power gain - output power tradeoff described in sections 2.2 and 2.3 poses an upper limit on the transistor size that can be used, and thus on the maximum output power that can be obtained from a single stage unit amplifier when operating at mm-wave frequencies. Optimizing the transistor size and impedances for maximum output power leads to low overall power gain, and optimizing for high power gain leads to low output power capability. Multi-stage amplifiers where the initial stages can be optimized for maximum gain and the output stage can be optimized for maximum output power are required to realize power amplifiers with both high gain and high output power levels.

In an attempt to achieve high output power with high gain, the three-stage power amplifiers whose schematics are shown in Figure 1.5 and Figure 1.6 were implemented in 90 nm bulk CMOS and presented in [14, 15].

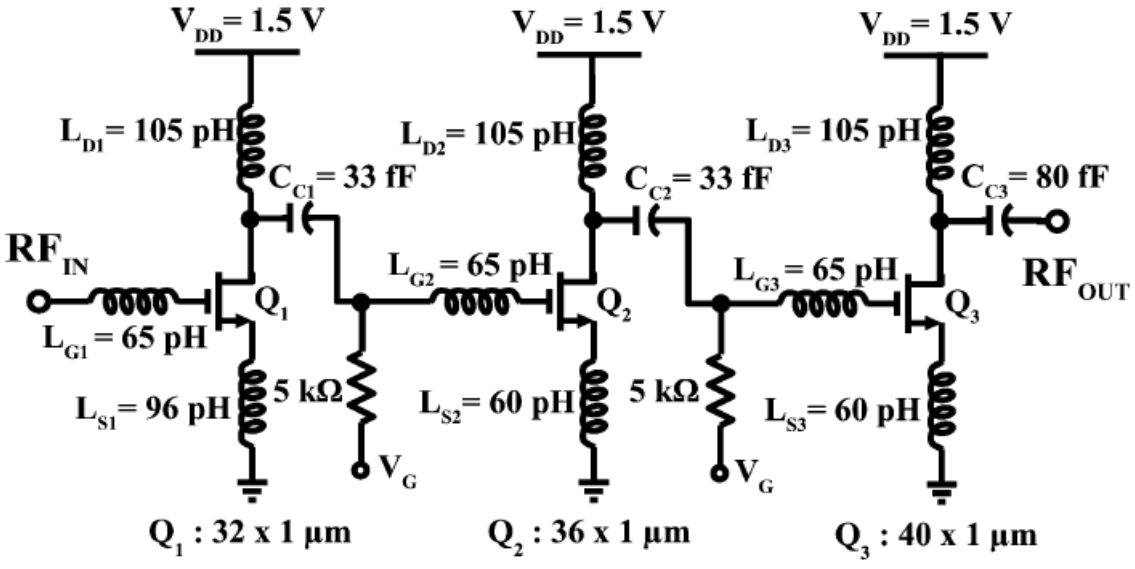

Figure 1.5: Schematic of three-stage power amplifier presented in [14]

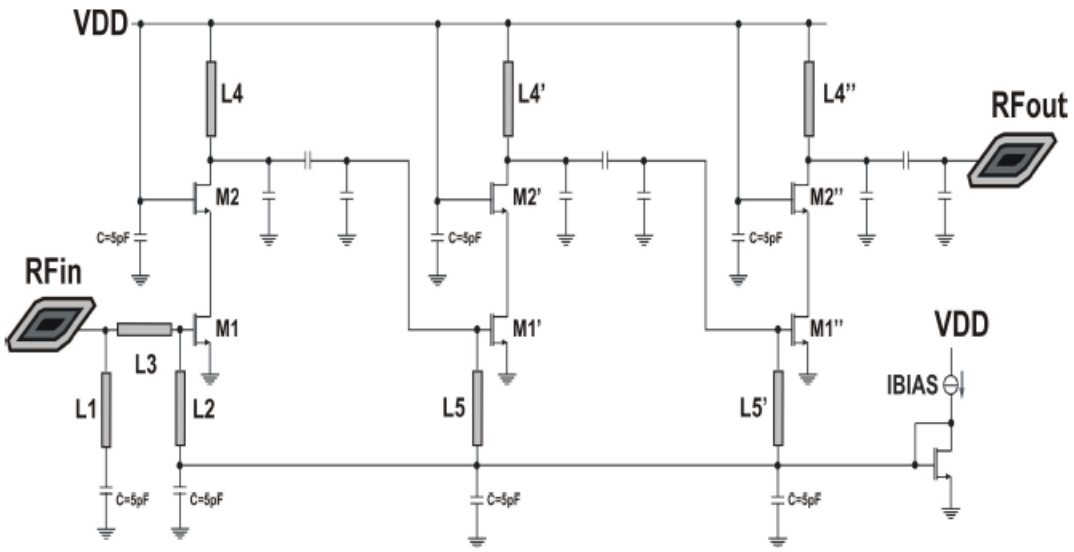

Figure 1.6: Schematic of three-stage power amplifier presented in [15]

The first power amplifier uses ring inductors extensively in lieu of transmission lines to achieve power gain of 5.2 dB with 1 dB compression and saturation output power levels of +6.4 dBm and +9.3 dBm respectively with peak power added efficiency of 7%. The second power amplifier uses microstrip transmission lines and cascade stages. It achieves a power gain of 10 dB and delivers 1 dB compression and saturation output power levels of 5 dBm and 8 dBm respectively with peak power added efficiency of 7%. While increasing the number of active stages can increase the overall power gain, the output power level is determined by the last stage. Since the last stage gain should not be made less than unity, the power gain - output power tradeoff plays a fundamental role in determining the size of the output stage, and thus puts an upper limit on the maximum output power that can be delivered from a single unit amplifier. Combining the power

from a number of unit amplifiers is necessary to achieving considerably higher output power levels.

In an attempt to increase the output power delivered from the last stage, the multi-stage amplifiers implemented in 90 nm bulk CMOS and presented in [18, 19] use two maximum size transistors in parallel in the last stage. Their schematics are shown in Figure 1.7 and Figure 1.8.

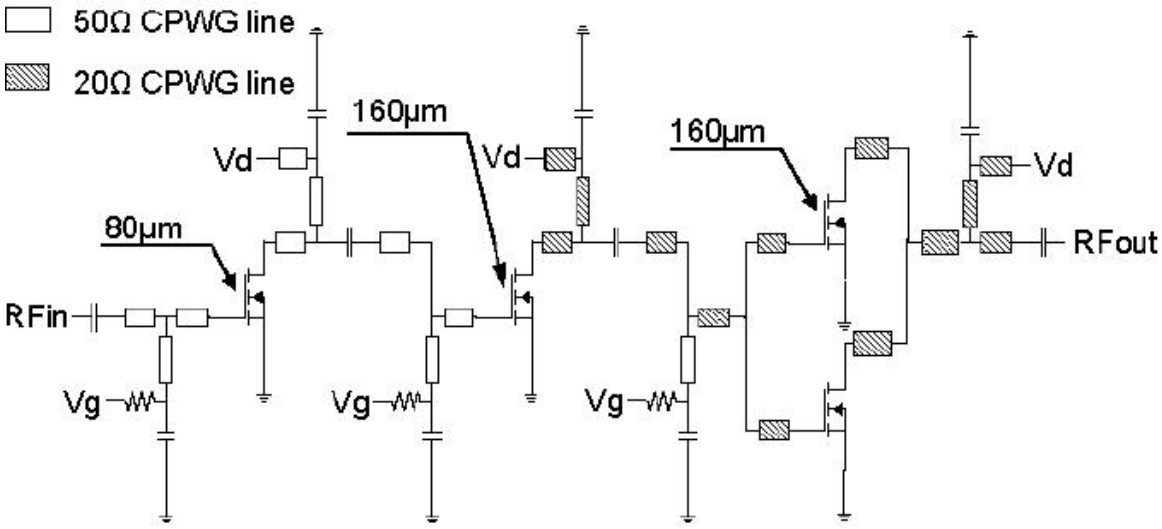

Figure 1.7: Schematic of three-stage power amplifier presented in [18]

The first power amplifier delivers 1dB compression and saturation output power levels of +10.5 dBm and +11.3 dBm respectively whereas the second provides power gain of 8 dB and delivers 1dB compression and saturation output power levels of +8.2 dBm and +10.6 dBm respectively.

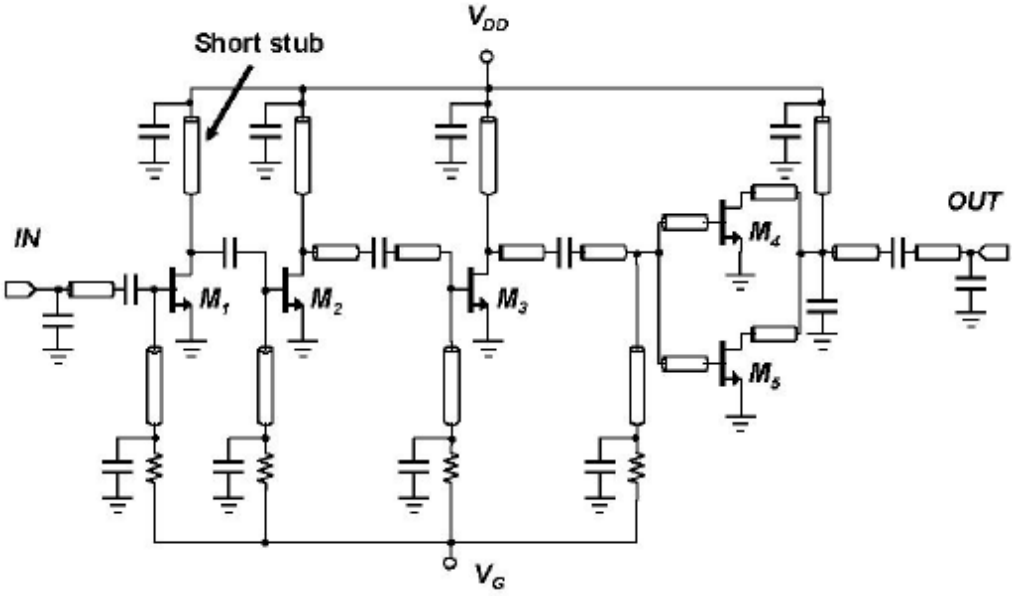

Figure 1.8: Schematic of three-stage power amplifier presented in [19]

Since the output stage of these amplifiers employ two large size transistors in parallel, the stage just before the last one will need to be composed of a transistor of about the same size in order to guarantee that compression starts at the output stage and is not determined by previous stages. As will be shown in section 2.2, large size transistors exhibit low gain characteristics due to the added parasitic losses in the gate and drain networks. Thus, in order to obtain high gain from the overall amplifier, more than two stages are needed in this topology. This increases the power consumption and reduces the amplifier efficiency. In order to optimize the output power, power gain, and efficiency of the amplifier, the output power from two unit amplifiers each employing a maximum size transistor at the output stage can be combined using on-chip power combiners.

In [12, 13], fully integrated two-way 60 GHz transformer-coupled differential power amplifiers are implemented in 90 nm standard CMOS. Both schematics are shown in Figure 1.9 and Figure 1.10.

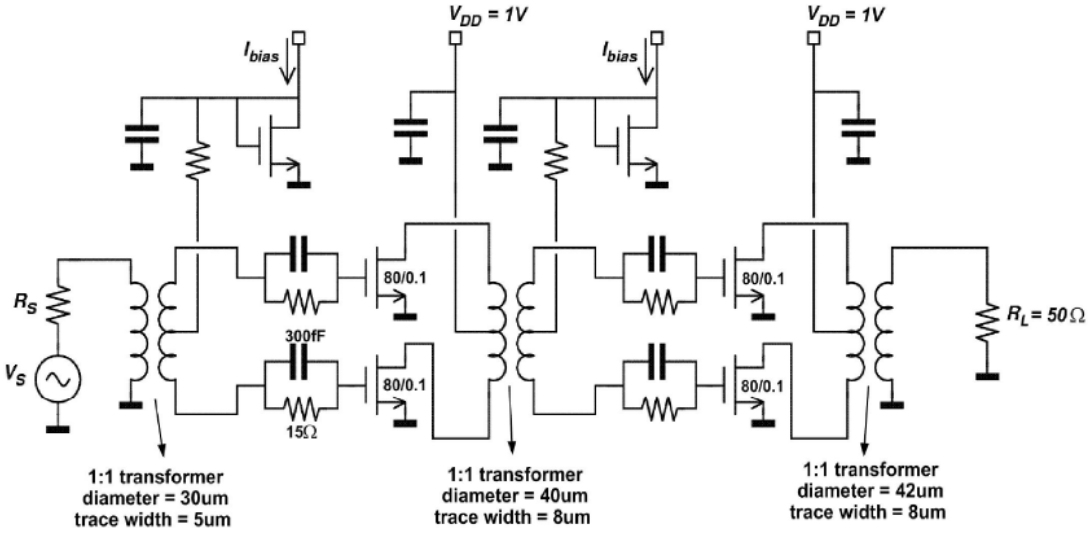

Figure 1.9: Schematic of two-way power amplifier presented in [12]

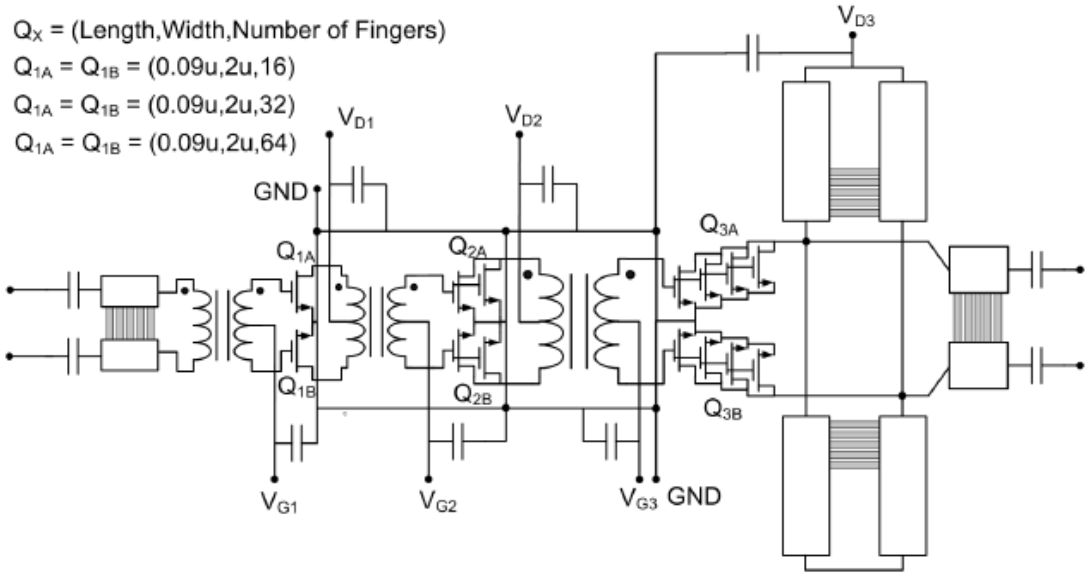

Figure 1.10: Schematic of two-way power amplifier presented in [13]

These power amplifiers use compact on-chip transformer-based power splitters and combiners in order to split and combine the output power of two unit amplifiers. The first delivers 1dB compression and saturation output power levels of +9 dBm and +12.3 dBm respectively while occupying only 660x380 μm^2 of chip area, whereas the second delivers +12 dBm of saturated output power while occupying only 0.15 mm^2 of area. While the extensive use of on-chip transformers for power splitting and combining results in a compact two-way power amplifier combining the output power of two unit amplifiers occupying a relatively very small area, this technique has two main disadvantages. First, as the transformer maximum gain is less than unity, power combining through the transformers can result in power loss and thus reduced output power levels and drain efficiency. Second, while combining the output power from two unit amplifiers using transformers is relatively easy, combining the output power from a larger number of unit amplifiers in order to provide even higher output power levels while keeping the transformer loss low becomes increasingly more difficult.

1.3 Research Contributions

This research aims at exploring the challenges facing the design and implementation of 60 GHz power amplifiers in standard 90 nm CMOS processes. The design, modeling, and layout optimization of both passive structures such as transmission lines, capacitors, RF pads as well as active devices operating at 60 GHz are investigated. A low-loss power combining technique taking advantage of millimeter-wave amplifier topologies is presented. Four power amplifiers are implemented in a standard 90 nm 1V CMOS

process. A record performance is reached in terms of 1dB compression and saturation output power.

1.4 Organization of the Thesis

Chapter 2 covers the technology challenges that face the design and implementation of 60 GHz power amplifiers in standard 90 nm CMOS processes. Section 2.1 presents the challenges pertaining to delivering high output power in the presence of the downward scaling of supply voltages. While section 2.2 covers the optimization of the transistor size and layout in the presence of the power gain – output power tradeoff, impedance matching in the presence of the power gain – output power tradeoff is presented in section 2.3. Power combining techniques as a means to increasing the output power of power amplifiers is discussed in section 2.4. The modeling methodology of passive structures and active devices at 60 GHz is presented in chapter 3. The design and modeling of passive structures is discussed in detail in chapter 4. Transmission lines, capacitors, and RF Ground-Signal-Ground pads are covered in sections 4.1, 4.2, and 4.3 respectively. Chapter 5 presents the design and modeling of 60 GHz active devices. The transistors design and layout optimization are covered is section 5.1, whereas small signal and large signal modeling are discussed in sections 5.2 and 5.3 respectively. Chapter 6 presents the implementation of two simple circuits in order to verify the modeling of passive structures and active devices up to 60 GHz. The measurement and simulation results of a Wilkinson power combiner and a simple 60 GHz amplifier are presented in sections 6.1 and 6.2 respectively. Four 60 GHz power amplifiers are presented in chapter

7. A four-way power amplifier is discussed in section 7.1, and three different two-way power amplifiers are presented in sections 7.2, 7.3, and 7.4. The measurement setup is described in section 7.6. Conclusions are given in chapter 8.

CHAPTER 2

TECHNOLOGY CHALLENGES

2 Technology Challenges

CMOS technology scaling has resulted in transistors with increasingly higher f_T and unity power gain frequency (f_{max}) such that the maximum available gain at frequencies around 60 GHz has become high enough to implement 60 GHz CMOS transceivers at the 130 nm technology node and beyond. However, many challenges still exist especially for implementing mm-wave power amplifiers. First, the low supply voltage, thin gate oxide, and low breakdown voltage that accompany smaller technology nodes make it harder to achieve high output power levels. Second, the power gain – output power tradeoff due to transistor sizing that presents itself at mm-wave frequencies poses an upper limit on the maximum transistor size that can be achieved with reasonably high gain and thus on the maximum output power of a single transistor. As a result, power combining becomes necessary to achieve high output power levels and presents the next challenge. Moreover, the power gain - output power tradeoff due to impedance matching makes it more challenging to achieve high output power levels with reasonable power gain from a single stage amplifier.

This chapter discusses the above mentioned challenges that face mm-wave power amplifiers design. Section 2.1 shows how decreasing supply voltages with smaller CMOS processes technology nodes necessitates the design of ever larger transistors in order to obtain high output power levels. Then, section 2.2 discusses how to optimize the power transistor size in the presence of the power gain – output power tradeoff. Section 2.3 investigates the power gain – output power tradeoff that results from impedance matching in transistors operated at mm-wave frequencies, and finally power combining as a way to

achieve higher output powers is presented in section 2.4. The challenges in mm-wave modeling of passive structures and active devices are presented in chapters 4 and 5 respectively.

2.1 Low Supply Voltage

Besides enabling operation at 60 GHz, CMOS technology scaling to 90 nm and beyond makes it harder to deliver high output power due to lower supply and breakdown voltages. As shown in Figure 2.1, the supply voltage has been decreasing as smaller technology nodes are introduced, although this trend has slowed considerably with the most recent processes. As transistors channel lengths are getting smaller, thinner oxides are required in order for the gate to control the channel which results in lower breakdown voltage. This necessitates the use of lower supply voltages. In order to keep the transistor current drive capability high, the overdrive voltage ($V_{GS} - V_{th}$) has to be kept high. As the transistor gate to source voltage V_{GS} is decreasing due to supply voltage scaling, the threshold voltage V_{th} has to be reduced. However, a lowering of the threshold voltage results in a considerable increase in the transistor leakage current, which has recently caused a deceleration in voltage scaling. The already low supply voltages make it considerably difficult to deliver high output power. The process used in this work dictates a 1 V supply voltage.

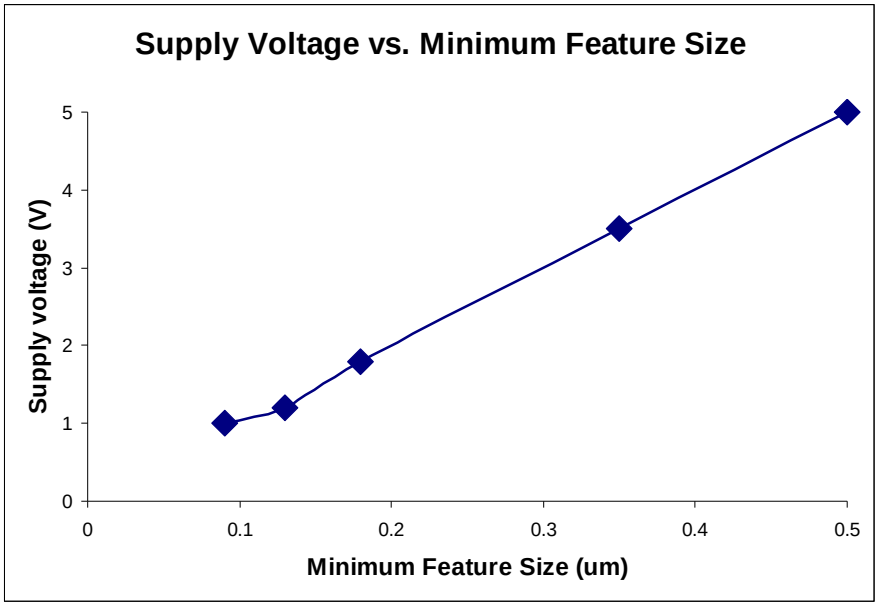

Figure 2.1: Supply voltage vs. CMOS process minimum feature size

Since the output power delivered by a transistor to a given load is limited by

$$P_{out} < V_{DD} I_Q \tag{2.1}$$

where V_{DD} is the supply voltage and I_Q is the transistor bias current, as the voltage is decreasing, the amplifier current drive capability has to be increased in order to keep the delivered power unchanged. The DC current in a CMOS transistor operating in the saturation region is [20]

$$I_D = \frac{1}{2} K' \frac{W}{L} (V_{GS} - V_{th})^2 \tag{2.2}$$

where K' is the process transconductance and W and L are the transistor gate width and channel length respectively. K' and V_{th} are technology constants, V_{GS} is determined by the supply voltage, and the minimum channel length is usually used in order to maximize the transistor f_T and f_{max}. Thus, in order to increase its current drive capability, the

transistor width W has to be increased proportionately since all other parameters are fixed either by the technology or the design.

2.2 Transistor Sizing in the Power Gain - Output Power Tradeoff

We have seen in the previous section that delivering high output power in the presence of supply voltage downward scaling requires an increase of the transistor total width, W. Since the transistor total effective width equals the number of fingers multiplied by the finger width, this can be achieved through either increasing the finger width, or increasing the number of fingers, or both. However, optimizing either the finger width or the number of fingers leads to a power gain – output power tradeoff. Optimization of the finger width is covered in section 2.2.1 while optimizing the number of fingers is discussed in section 2.2.2.

2.2.1 Optimization of Finger Width

In multi-finger CMOS transistors, a larger finger width results in higher gate resistance. This is because the gate resistance of each individual finger behaves as a distributed RC network which can be approximated by [20, 21]

$$R_g = \frac{R_{poly} W_F}{3n^2 L} \tag{2.3}$$

where R_{poly} is the polysilicon gate sheet resistance, W_F is the finger width, L is the channel length, and $n = 1,2$ depending on the number of gate contacts. In turn, a higher gate resistance, while it does not affect the f_T of the transistor because f_T can be approximated as [23]

$$f_T \approx \frac{g_m}{C_{gs}} \tag{2.4}$$

where g_m is the transistor transconductance and C_{gs} is its gate to source capacitance, and thus is independent of the gate resistance, it introduces additional power losses and causes a reduction in the transistor f_{max} and maximum stable gain (MSG) since f_{max} can be approximated as [24-26] (neglecting the drain resistance and substrate losses)

$$f_{max} = \frac{f_T}{2\sqrt{R_g\left(g_m \frac{C_{gd}}{C_{gg}}\right) + \left(R_g + r_{ch} + R_s\right)g_{ds}}} \tag{2.5}$$

where g_m is the transistor transconductance, $C_{gg} = C_{gs} + C_{gd}$ is its total gate capacitance, C_{gd} and C_{gs} are the gate to drain and gate to source capacitors respectively, R_g, r_{ch}, and R_S are the gate, channel, and source resistances respectively, and g_{ds} is the transistor output conductance. It is shown in Figure 2.2 from [27] that a transistor f_{max} decreases as its finger width increases. Thus, maximizing f_{max} places an upper limit on the maximum finger width of a transistor and thus on its output power capability. It can be noticed from the figure that f_{max} decreases slowly as the finger width approaches 1 μm but it decreases with much a higher slope beyond 1 μm. The optimum finger width given the f_{max} - output power tradeoff is around 1 μm. As the frequency of operation in mm-wave CMOS power amplifiers is already a large fraction of f_{max}, the designer cannot sacrifice significant loss in f_{max} when optimizing the finger width.

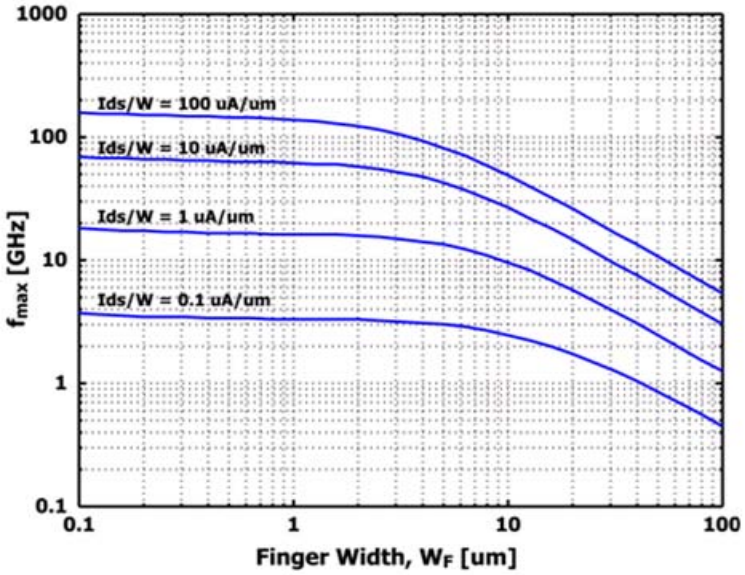

Figure 2.2: f_{max} vs. finger width [27]

In addition to reducing the transistor f_{max}, an increase in the transistor finger size can also generally cause a decrease in its maximum stable gain because of the increased gate resistive losses. A very small finger width results in very small gate resistance, which is usually smaller than that required to stabilize the device in the mm-wave band. For a device operated in the conditionally stable state, the calculation of MSG assumes that fictitious loss is added at the gate of the transistor to stabilize it, and therefore increasing the finger width further does not affect MSG. This is the case as long as the device is operated in the conditionally stable regime, i.e. at a frequency below the unconditional stability frequency. This frequency is associated with the kink of the transistor maximum available power gain which is a function of the gate resistance. Three test transistors with 100 fingers each but different finger widths of 1 μm, 2 μm, and 4 μm

were fabricated and their S-parameters measured. Figure 2.3 shows a comparison of the maximum stable gain for the 2 μm and the 4 μm finger widths transistors.

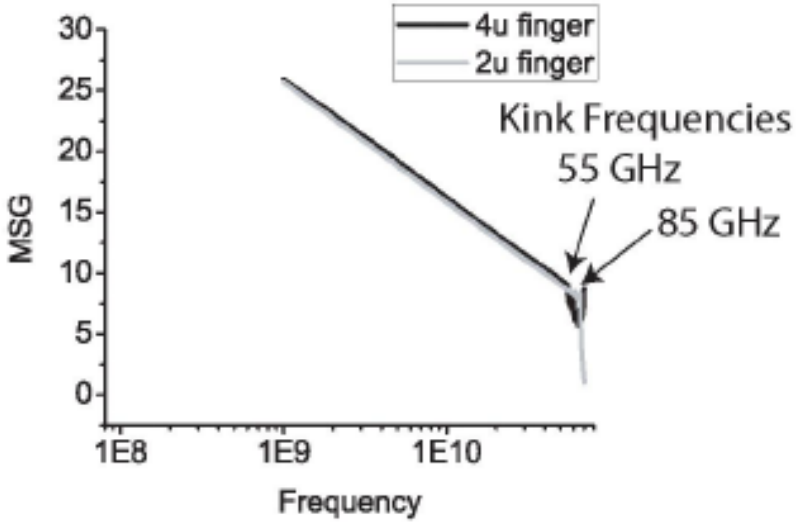

Figure 2.3: Measured MSG vs. frequency of 100 fingers, 2μm and 4μm per finger devices [28]

The maximum stable power gains at frequencies before the kink where both devices are conditionally stable are similar and independent of the finger width. However, the kink happens earlier for the 4 μm width device and thus the available gain of the 2 μm width device is larger beyond this frequency. That is the case because the maximum stable power gain decreases with a much steeper slope after the kink frequency.

The measured 60 GHz MSG of the three devices biased at the same current density is plotted in Figure 2.4.

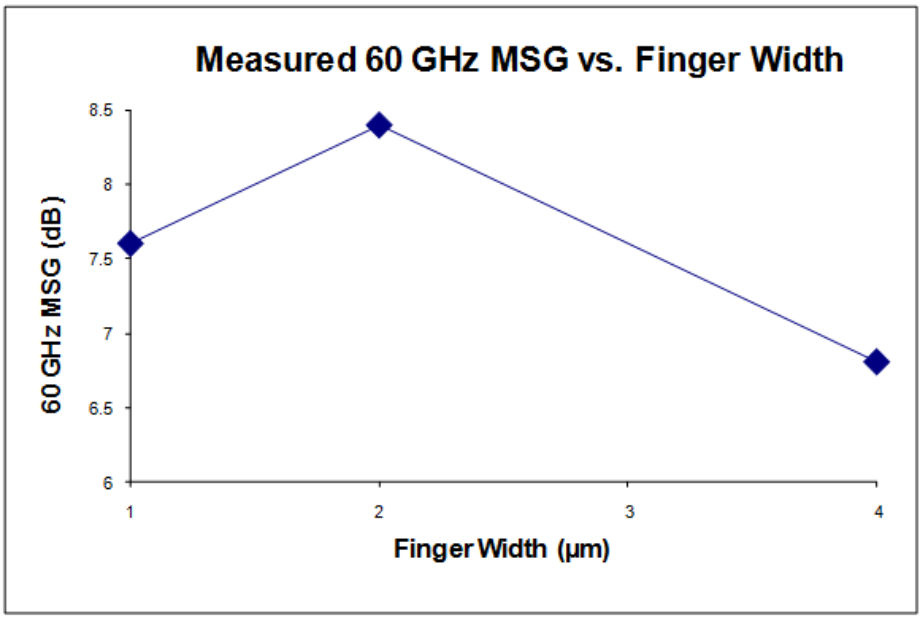

Figure 2.4: Measured 60 GHz MSG vs. finger width, 100 finger devices

The transistor with 4 µm wide fingers clearly shows a lower MSG than the other two. Contrary to the general trend, the transistor with 2 µm finger width shows a higher MSG than that with 1 µm finger width. The reason for this effect is that since both transistors have the same number of fingers, they both have identical source networks, i.e. identical total source resistances. However, since one transistor has larger finger width, it possesses lower source resistance per width unit, and thus lower source degeneration and higher MSG. The larger gate resistance effect takes over for the case of 4 µm finger width and results in overall lower MSG.

Despite its lower gain, the 100 fingers, 4 µm per finger device should in theory be able to deliver four times the output power than the 100 fingers, 1 µm / finger device because it would be biased at four times the current. However, as shown from the measured 60 GHz operating power gain circles of the three devices in Figure 2.5, the gain

variation is much more rapid for the 4 μm device as we move away from the optimal operating point. The operating power gain circles become much closer to each other as the finger width size increases. This results in lower design robustness in the presence of process variation and modeling inaccuracies.

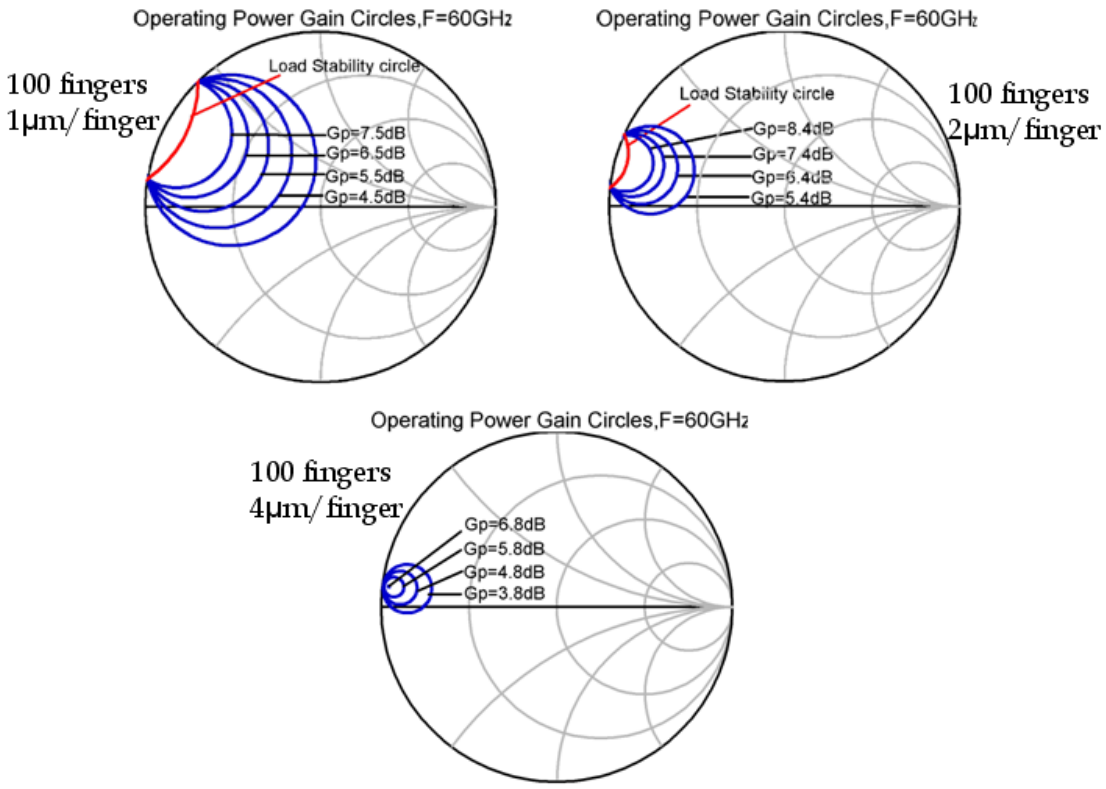

Figure 2.5: Measured 60 GHz operating power gain circles for different finger widths

2.2.2 Optimization of the Number of Fingers

Once the finger width is optimized to maximize f_{max}, in order to increase the effective transistor size, the number of fingers should be maximized. When operating at low frequencies, the number of fingers in a CMOS power device can be increased to the limits that process rules permit or until line edge roughness results in large gate resistance

variations. However, this is not the case when operating at mm-wave frequencies. As the number of fingers increases, the height of the transistor layout, as shown in Figure 2.6 and Figure 2.7, grows proportionately and results in large layout aspect ratio. As the number of fingers stays lower than around 100, the size of the gate, drain, and source networks used to connect these ports to all the fingers can be kept relatively small resulting in low gate, drain, and source resistances. This is evident in the layout of the 80 finger transistor in Figure 2.6 where very small gate and drain networks are needed. The transistor length is about 30 μm, only three times the width of the transmission line used to connected it to the rest of the circuit.

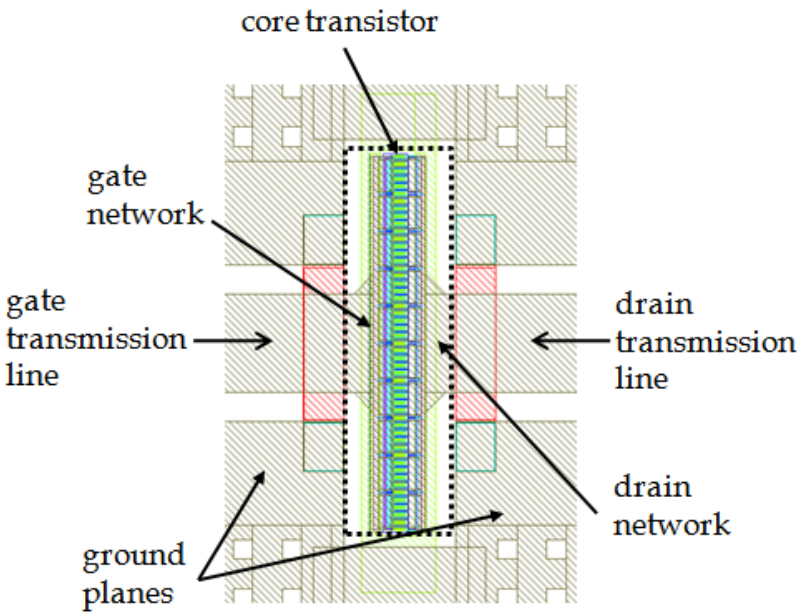

Figure 2.6: 80 finger transistors layout

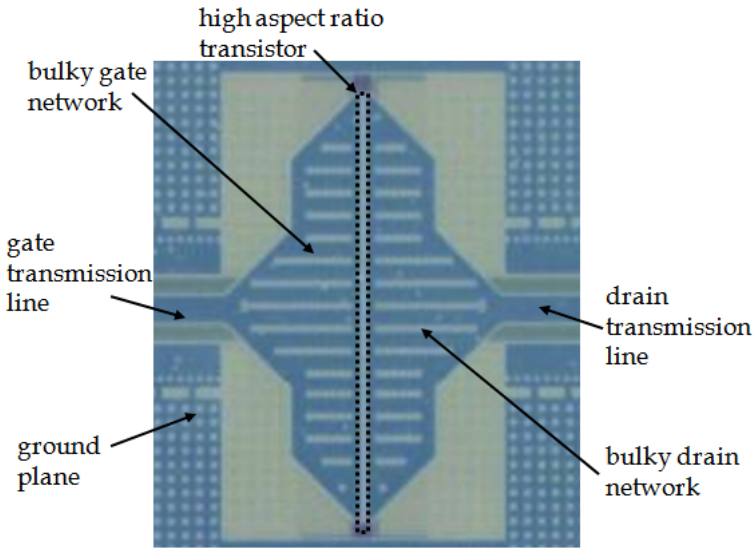

Figure 2.7: 400 finger transistors layout

However, as more fingers are added, larger networks with large tapers are needed introducing additional gate and drain resistive losses as well as resistive source degeneration, leading to lower f_{max} and MSG. This is evident in the layout of the 400 finger device in Figure 2.7. As the transistor length is much larger than the width of the transmission line feeding its gate and drain, large gate and drain networks are needed to reduce the gate and drain inductances.

In order to verify this effect, six transistors of varying number of fingers but of the same 1 μm finger width and biased at the same current density level were fabricated and their 60 GHz MSG was measured. The results shown in Figure 2.8 clearly indicate a lower MSG for the 400 finger device. All the other devices with less than 100 fingers have almost the same value of MSG.

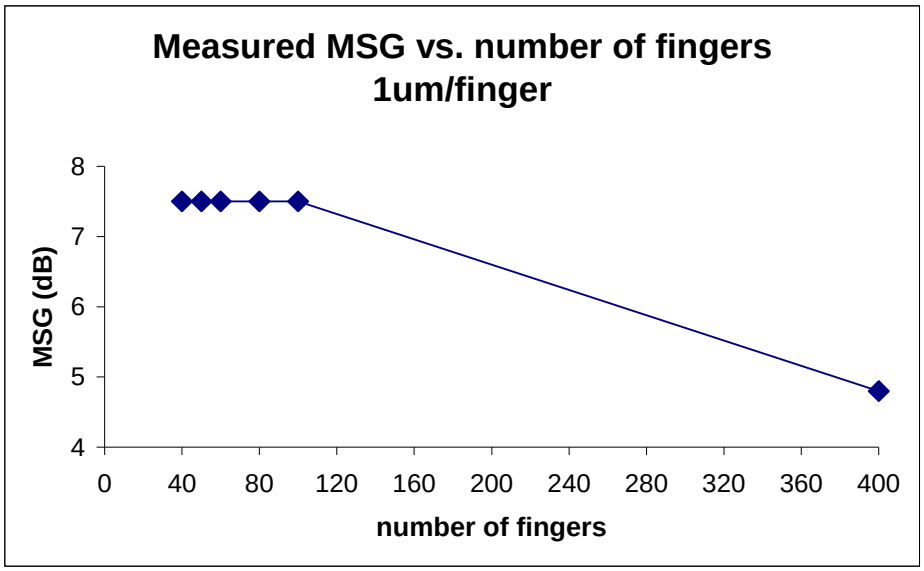

Figure 2.8: Measured MSG vs. number of fingers, 1µm/finger, all same current density

2.3 Impedance Matching in the Power Gain - Output Power Tradeoff

We have seen in section 2.2 that optimizing the transistor size, both its finger width and the number of fingers, leads to a power gain – output power tradeoff. In this section, the power gain – output power tradeoff resulting from the transistor input and output impedance matching is discussed. A transistor is typically driven with a 50 Ω source and drives a 50 Ω load as well. However, as shown in Figure 2.9, typically, input and output matching networks are used in order to transform these driving source and output load impedances and provide the power device with source and load impedances that insure stability and maximize power gain and output power. Both the power gain and the output power depend on the transistor load and source reflection coefficients, and thus on its load, source, output, and input impedances. However, the conditions on these impedances

that lead to maximum power gain are different than those that lead to maximum output power, thus the power gain – output power tradeoff. Input and output impedance matching for maximizing the power gain is covered in section 2.3.1 while matching for maximizing the output power is discussed in section 2.3.2.

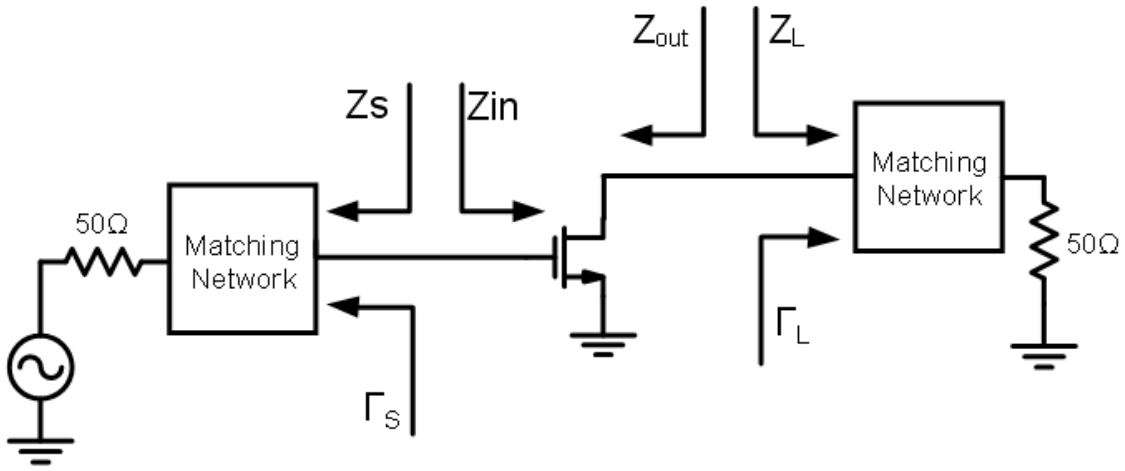

Figure 2.9: Transistor with input and output matching networks

2.3.1 Matching for Maximum Power Gain

There exist three different power gain definitions that are usually used in conjunction with power amplifiers. These are the transducer power gain G_T, the power gain, also called the operating power gain, G_P, and the available power gain G_A. They are defined as follows: [29]

$$G_T = \frac{P_L}{P_{AVS}} = \frac{power\ delivered\ to\ the\ load}{power\ available\ from\ the\ source} \quad \textbf{(2.6)}$$

$$G_P = \frac{P_L}{P_{IN}} = \frac{power\ delivered\ to\ the\ load}{power\ input\ to\ the\ network} \quad \textbf{(2.7)}$$

$$G_A = \frac{P_{AVN}}{P_{AVS}} = \frac{power\ available\ from\ the\ network}{power\ available\ from\ the\ source} \quad \textbf{(2.8)}$$

The source impedance Z_S, the input impedance Z_{in}, the load impedance Z_L, and the output impedance Z_{out} shown in Figure 2.9 determine the amplifier gain figures defined in equations (2.6)-(2.8). In order to obtain maximum transducer power gain, the source and input impedances should be conjugately matched, as well as the load and output impedances [29]. This is referred to as the simultaneous conjugate matched condition. This is possible only if the device is unconditionally stable, i.e. its stability factor K is larger than unity [29] where

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + -|\Delta|^2}{2|S_{12}S_{21}|} \quad \textbf{(2.9)}$$

and

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad \textbf{(2.10)}$$

Under these conditions, all the power gain definitions are equal, i.e.

$$G_T = G_P = G_A \quad \textbf{(2.11)}$$

and thus

$$G_{T,max} = G_{P,max} = G_{A,max} = \frac{S_{21}}{S_{12}}\left(K - \sqrt{K^2 - 1}\right) \quad \textbf{(2.12)}$$

The maximum stable gain, MSG, is defined as the value of $G_{T,max}$ when $K = 1$ which leads to [29]

$$G_{T,max} = \frac{S_{21}}{S_{12}} \quad \textbf{(2.13)}$$

If the device is operated in the conditionally stable case where $K < 1$, a simultaneous conjugate match is not possible, and it is more useful to consider the operating power gain G_P in this situation. Even though the value of G_P can approach infinity when the transistor is operated in the potentially unstable case, values of G_P that are above the MSG figure of merit result in values of Γ_L and Γ_S that are very close to the unstable region and thus decrease the design robustness. It is shown in [29] that the values of Γ_L that produce a constant power gain lie on a circle, called an operating power gain circle, when plotted on a Smith chart. In order to design an amplifier yielding a given power gain, a number of operating power gain circles corresponding to a transistor in a two-port common-source configuration can be drawn, a value of Γ_L corresponding to a given G_P value can be chosen from the stable region and not too close to the stability circle, and the output matching network can be designed to transform the load impedance, usually 50 Ω, into the corresponding Z_L. The resulting Zin can be calculated. In order to obtain maximum power gain under the given Γ_L chosen, the input matching network can then be designed to conjugately match Z_{in} and Z_S if this would result in a Γ_S in the stable region. 60 GHz operating power gain circles derived from measured S-parameters of a 100 fingers, 1 μm per finger transistor are shown in Figure 2.10.

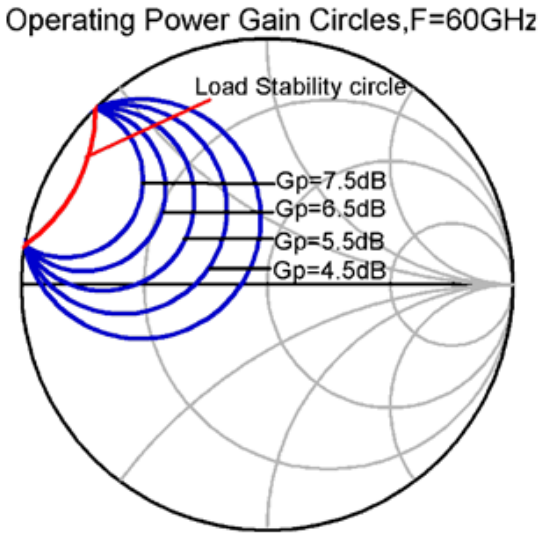

Figure 2.10: 60 GHz operating power gain circles, 100 fingers, 1 µm per finger, 90 nm NMOS transistor

2.3.2 Matching for Maximum Output Power

In power amplifiers, the matching requirements for maximizing the amplifier output power are different than those used for optimizing the amplifier power gain as presented in section 2.3.1. Even though the input matching requirement is the same, i.e. the input matching network needs to be designed such that the transistor source and input impedances are conjugately matched, the output match requirement is different. The transistor load and source impedances should not be conjugately matched as that would lead to sub-optimal output power capability, even in the case where the transistor is operated in the unconditionally stable region where such a match does exist. The exact value of the optimum output power match impedance is best found using load-pull measurement or simulation [30]. In such a measurement, tuning devices are connected

between the driving source and the transistor gate on the input side, as well as between the load and the transistor drain at the output side. The tuners are set such that the load impedance seen by the transistor is varied across a large range while the input is always conjugately matched. The measurement is done at a given frequency. The values of the output power for each load impedance can be plotted on a Smith chart as in Figure 2.11 which shows the results of a load-pull simulation of the 80 fingers, 1 µm per finger NMOS transistor. After performing such a measurement, the load impedance corresponding to the maximum output power can be chosen and the output matching network can be designed in order to change the 50 Ω load to the corresponding impedance.

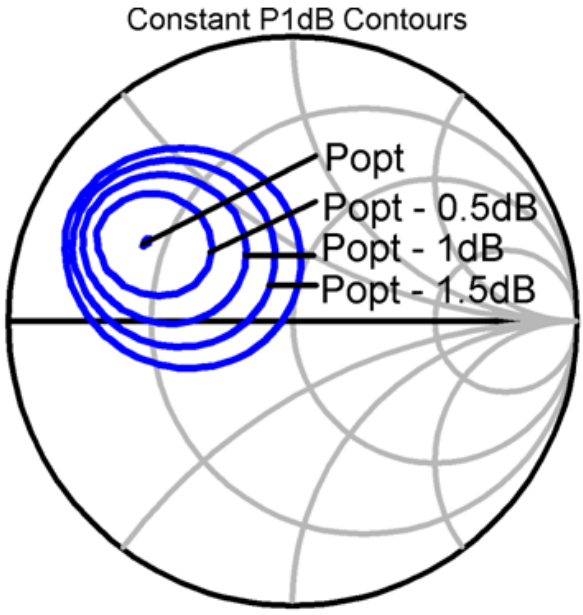

Figure 2.11: 60 GHz power contours, 100 fingers, 1 µm per finger, 90 nm NMOS transistor

2.4 Power Combining

Once the finger width and the number of fingers in a power transistor as well as the input and output matching networks are optimized in the presence of the power gain – output power tradeoff in order to obtain the maximum output power with reasonable power gain, an optimum unit size power amplifier can be designed. In order to increase the output power capability of the amplifier, a number of these unit size amplifiers can be combined to form one high output power amplifier as shown in Figure 2.12. The input power is equally split to the unit amplifiers at the input node using a passive power splitter and the output power of all unit amplifiers is combined using a passive power combiner at the output node.

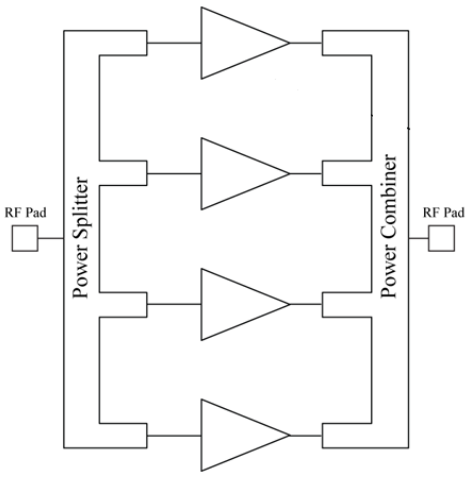

Figure 2.12: Power combining architecture

There exist different techniques to implement the power splitter and combiner. Wilkinson power combiners are covered in section 2.4.1 while transformer-based power combiners are presented in section 2.4.2. A low loss mm-wave power combining

technique that takes advantage of certain mm-wave amplifier topologies is discussed in section 2.4.3 and used in the power amplifiers implemented in this work and presented in chapter 7.

2.4.1 Wilkinson Power Combiners

Wilkinson power splitters and combiners [31] are popular because they can simultaneously provide port-to-port isolation, impedance matching, and the ability of being lossless, at least theoretically. In addition to introducing equal phase delay from the output of each amplifier to the combining node so that all signals add in phase, the Wilkinson power combiner transmission lines can be sized such that no impedance transformation is performed through the combiner as shown in Figure 2.13. If the inputs and outputs are reversed, it can also be used as a power splitter. A thorough analysis of Wilkinson power combiners can be found in [34]. At 60 GHz, the on-chip wavelength is around 2.5 mm, enabling the use of integrated Wilkinson power combiners which require transmission line lengths in the order of $\lambda/4$.

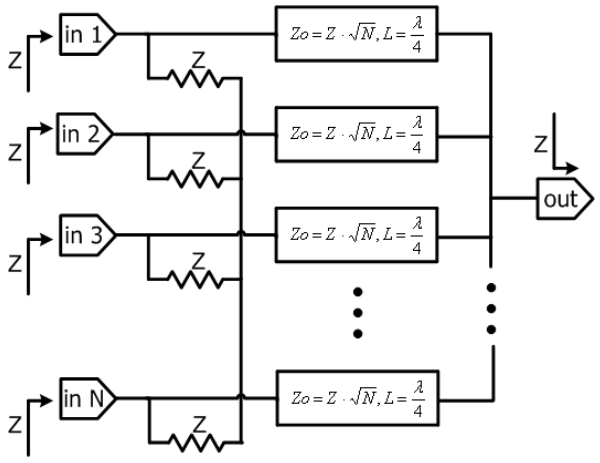

Figure 2.13: N-way Wilkinson power combiner

Integrated Wilkinson power splitters and combiners can be used in mm-wave CMOS power amplifiers, but they introduce significant power loss and thus lower the amplifier maximum output power and efficiency. For example, a four-way Wilkinson power combiner can be realized in two stages as shown in Figure 2.14 where two 2-way combiners are used in the first stage and their outputs are combined with one 2-way combiner in the second stage. Another method would be to use the Corporate structure shown in Figure 2.14 where the power of all four stages is combined simultaneously in one stage.

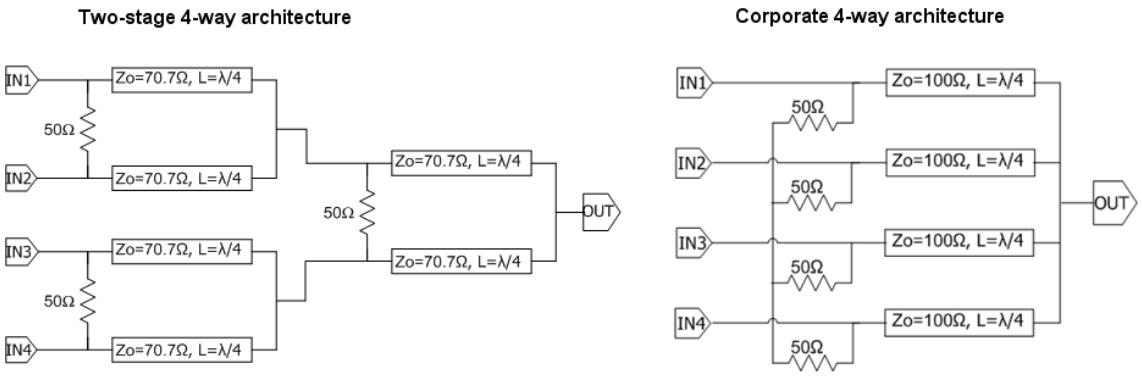

Figure 2.14: Four-way Wilkinson power combiner architectures

Even though the signal travels a total length of $\lambda/2$ in the two-stage architecture compared to only $\lambda/4$ in the corporate structure, the former employs transmission lines with characteristic impedance of 70.7 Ω while the latter uses transmission lines with characteristic impedance of 100 Ω. If implemented as coplanar waveguides, the higher characteristic impedance transmission lines will exhibit larger gap spacing resulting in higher loss as a larger portion of the electro-magnetic field will enter the substrate. Simulation of the two structures using practical coplanar transmission lines shows that

the two-stage architecture suffers an insertion loss of 2.2 dB while the corporate structure exhibits an insertion loss of only 1.4 dB. This amount of insertion loss can significantly reduce the amplifier output power and efficiency.

2.4.2 Transformer-Based Power Combiners

Transformer based power splitters and combiners have been used at 60 GHz [12, 13] as described in section 1.2. These combiners can simultaneously perform impedance transformation, AC coupling, and DC biasing, in addition to power splitting and combining. They have the advantage of being very compact. At 60 GHz, they can be achieved with one turn of diameter less than 50 μm [12]. It is shown also in [12] that 60 GHz transformer based power combiners can achieve an insertion loss as low as 0.85 dB when terminated with the optimal source and load impedances. Mm-wave transformer-based power combiners can be easily designed for two-way power amplifiers, but they become increasingly more complex when combining power form four or more amplifiers simultaneously.

2.4.3 mm-Wave Power Combining

In this work, a low-loss mm-wave power combining technique that takes advantage of mm-wave power amplifier topologies is introduced. Instead of using power splitters and combiners that are extrinsic to the unit amplifiers, these structures can be incorporated into the amplifier input and output matching networks. A schematic of a generic mm-wave power amplifier employing power splitting and combining is shown in Figure 2.15. The input and output matching networks are realized with transmission lines.

They usually present long series transmission lines at the input and output of each unit amplifier.

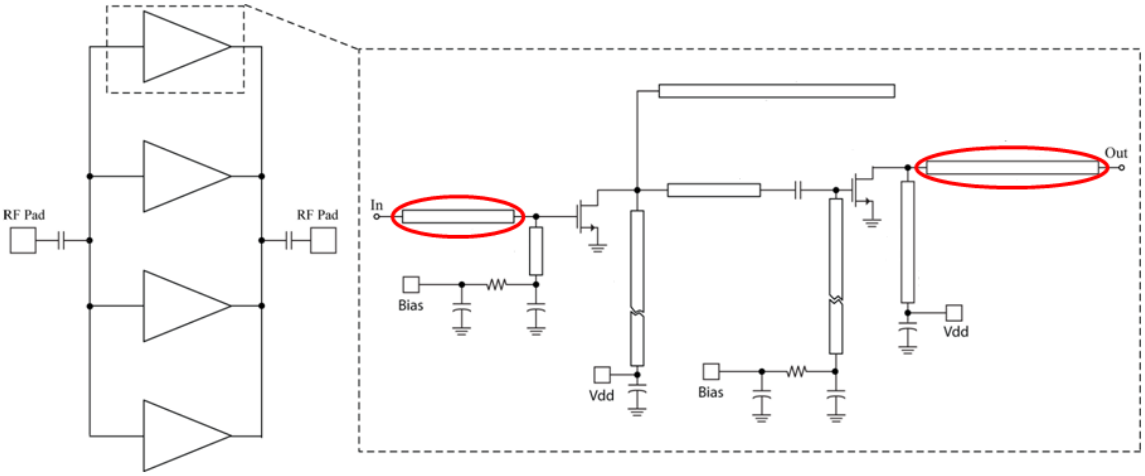

Figure 2.15: Generic mm-wave four-way amplifier

In order to realize power splitting and combining, these transmission lines of the different unit amplifiers, if long enough, can be routed to feed a common node. The matching networks topology would not need to be modified, but the transmission lines have to be routed in such a way that they all meet at a single point. Note that these transmission lines are present in the unit amplifier even if no power splitting and combining is performed, and thus do not introduce additional insertion loss. The feeding point itself presents additional capacitance and inductance seen by all the amplifiers, and thus the matching networks have to be changed accordingly in order to provide the desired impedance. There is obviously a practical layout limit to the number of amplifiers that can be used in such a scheme. It is shown in section 7.1 that combining the power from four amplifiers is possible. The power combiners resemble Wilkinson power combiners with two main

differences. First, since all signals at the amplifiers end are in phase, no resistors are used at the end of the power splitter and combiner transmission lines. This proves crucial in the four-way splitter and combiner where adding those resistors requires long leads that add considerable inductance and capacitance. Second, the transmission lines characteristic impedance and lengths are not chosen in such a way to preserve the impedances. Instead, the transmission lines of the matching networks themselves are used to perform the power splitting and combining as well as the impedance matching at the same time. This considerably reduces the insertion loss and the layout size.

If the transmission lines at the input and output of the unit amplifiers are not long enough, the input and output matching networks can be modified such that the input and output transmission lines are longer. This however would lead to higher loss in the matching networks.

Figure 2.16 shows a schematic of the described power combiner. The transmission lines represent the series lines in the output matching networks of the unit amplifiers. The power combiner drives the output pad and whatever load is presented at the output. The combiner is driven by the drains of the power transistors.

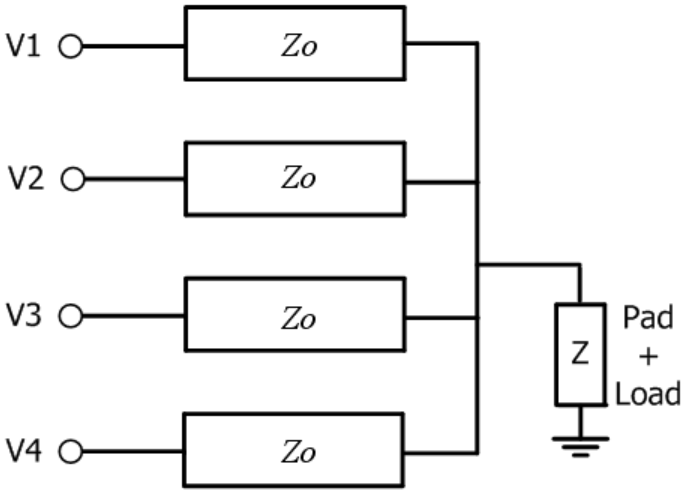

Figure 2.16: Power combiner schematic

As all unit amplifiers are identical, the four branches of the power combiner are driven with equal amplitude and phase, and thus $V_1 = V_2 = V_3 = V_4 = V_e$ as shown in Figure 2.17. The load driven by the combiner can be represented as four loads in parallel, each with four times the initial load impedance and driven by one branch of the combiner.

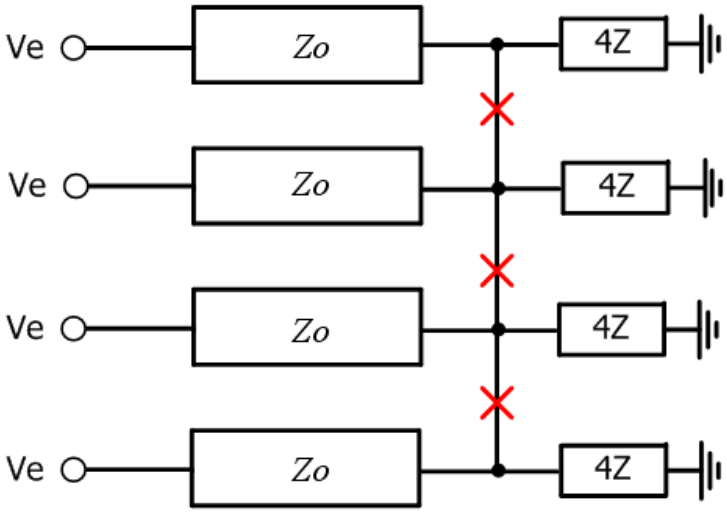

Figure 2.17: Power combiner with even mode excitation

As the voltages on the right side of the transmission lines are of equal amplitude and phase, no current flows in the short circuits that connect the right side of the transmission lines, and thus they can be eliminated without affecting the circuit behavior. This shows that the different amplifiers do not load each other, and each effectively drives four times the load represented by the output pad and the amplifier output load.

2.5 Conclusion

Although CMOS technology scaling at the 130 nm technology node and beyond has resulted in f_T and f_{max} levels high enough to implementing 60 GHz CMOS transceivers, mm-wave power amplifiers still face many challenges. Decreasing supply voltages necessitate the design of ever larger transistors in order to obtain high output power levels while the mm-wave power gain – output power tradeoff limits both the maximum finger width and the maximum number of fingers that can be used. Power combining as a way to achieve higher output power levels is investigated and a low-loss power combining technique taking advantage of millimeter-wave amplifiers topologies is presented. Impedance matching in the presence of the power gain – output power tradeoff necessitates the use of multi-stage amplifiers.

As supply voltages scale even further with future CMOS technology nodes, it will become even more challenging to deliver high output power levels and thus power combining will become more crucial. On the other hand, smaller technology nodes will provide higher gain, and thus relatively larger transistors will become feasible as the designer will afford to exchange gain for output power.

CHAPTER 3

MODELING METHODOLOGY

3 Modeling Methodology

Modeling of passive structures and active devices becomes increasingly more complex and plays an increasingly crucial role at mm-wave frequencies. As the frequency of operation increases, on one hand, losses in passive structures become more pronounced due to skin effect, proximity effect, and substrate loss, and, on the other hand, the maximum gain that can be obtained from active devices decreases as the operating frequency approaches f_T and f_{max}. At 60 GHz, the passive losses are substantially high and the active devices gains are considerably low such that circuit design barely meets specifications. Under these conditions, it is important that actual silicon performance be close to the simulated performance. Relatively small deviation between the simulated and the actual performance can result in chip failure because there exists a very small margin between simulation and specifications in the first place. Moreover, standard CMOS processes are in general not intended for operation around 60 GHz but rather at frequencies up to around 10 GHz. Thus, these processes usually ship with models that are accurate up to around 10 GHz, and no substantial effort is made to model them up to 60 GHz. For these reasons, extensive effort is spent in optimizing and modeling passive structures and active devices at mm-wave frequencies. Section 3.1 discusses why custom 60 GHz models are needed. The modeling strategy followed is covered in section 3.2, and the test chips fabricated for the modeling effort are described in section 3.3.

3.1 Need for 60 GHz Models

A generic CMOS power amplifier operating at microwave frequencies is shown in Figure 3.1.

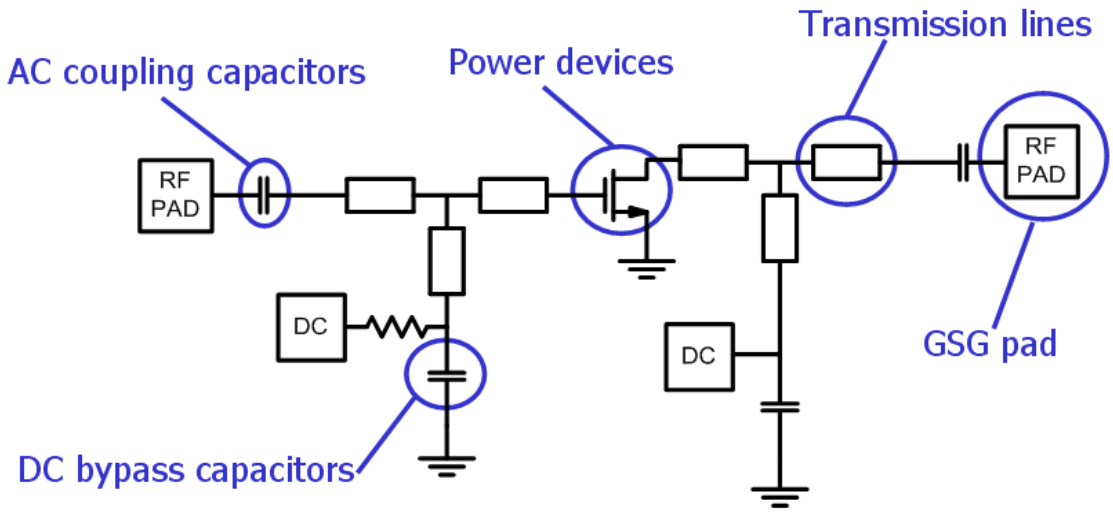

Figure 3.1: Schematic of generic amplifier operating at microwave frequencies

The amplifier is composed of a CMOS transistor, transmission lines, AC coupling and supply-ground bypass capacitors, resistors, RF Ground-Signal-Ground pads, and DC pads. Since the BSIM3V3 transistor models that ship with the employed 90 nm process are inaccurate at 60 GHz, custom models that take into account the extrinsic layout parasitics and are accurate in both small and large signal regimes are needed and discussed later in chapter 5. Figure 3.2 shows the large deviation between the measured S-parameters of a multi-fingered transistor and those simulated with the BSIM3V3 models that ship with the process. Large deviations exist around 60 GHz. Moreover, because the process does not ship with readily available and modeled transmission lines, custom designed transmission lines are modeled and used in the amplifier design. In

order not to use additional mask layers and thus reduce cost, no Metal-Insulator-Metal capacitors are used. Instead, metal multi-finger custom capacitors are designed and modeled to be used for AC coupling and supply-ground bypass. The junctions that connect the components together can result in significant parasitic capacitance and need to be modeled. Finally, RF Ground-Signal-Ground pads are considered part of the design, i.e. they are integrated into the input and output matching networks, and thus their losses are not de-embedded from the S-parameter measurements. Thus, accurate pad models are needed as well.

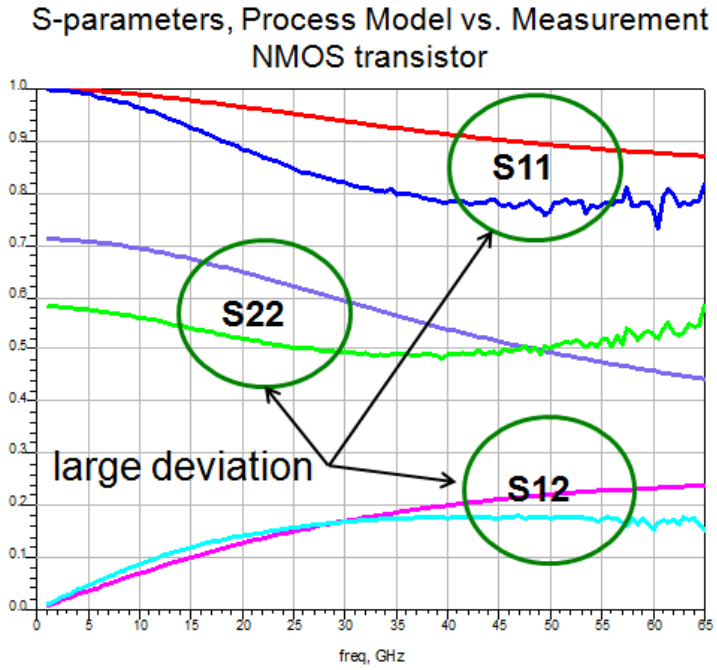

Figure 3.2: Measured vs. process model S-parameters of an NMOS transistor

3.2 Modeling Strategy

In order to achieve good agreement between measurement and simulation at 60 GHz, none of the models that ship with the process were employed. Instead, custom

models were created for each element and used in the simulations. The modeling strategy followed in this work consists in breaking up the amplifier into its basic constituent components, building test structures for each component, measuring their S-parameters at frequencies up to 65 GHz, modeling each component on its own by optimizing the model parameters to fit the measured data, and then putting together the complete model.

First, test structures were built for each of the basic constituent components of the power amplifier, i.e. active devices, transmission lines, AC coupling capacitors, low and high frequency supply-ground bypass capacitors, resistors, and Ground-Signal-Ground pads. As shown in Figure 3.3, each test structure consists of two RF Ground-Signal-Ground pads, the device under test in between, and coplanar transmission lines connecting the pads to the element under test.

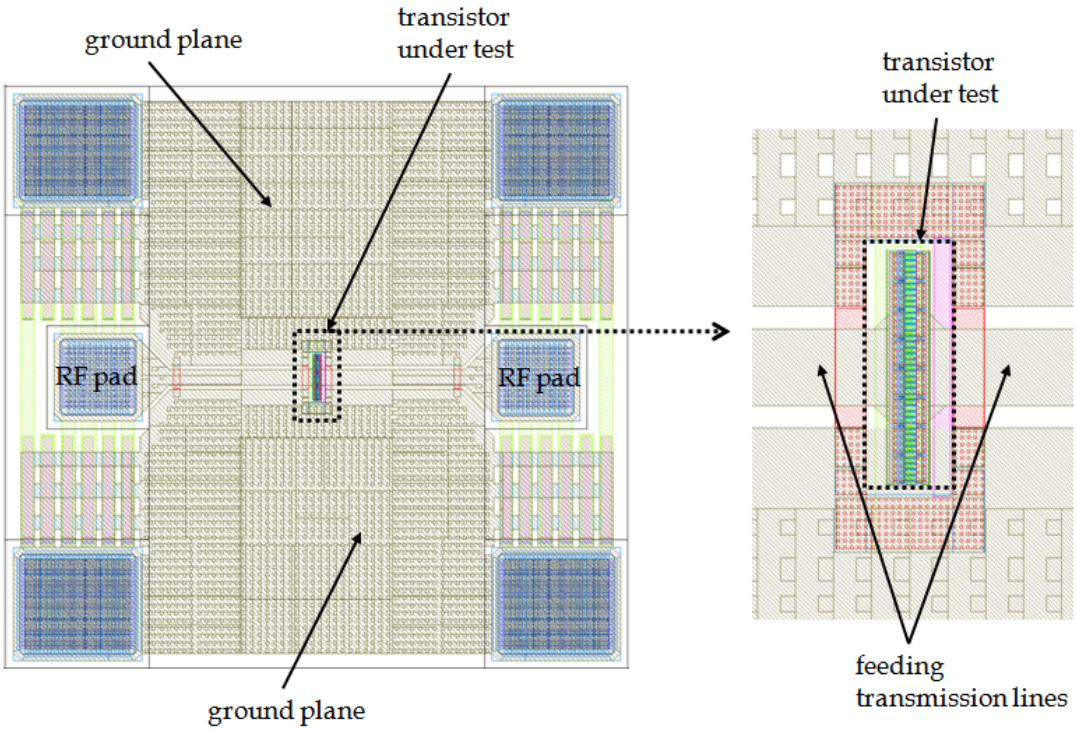

Figure 3.3: Test structure layout

Second, each test structure's S-parameters were measured up to 65 GHz. In order to obtain the S-parameters of the structure of interest excluding the pads and the transmission lines leading to it, the latter two were de-embedded using the "open-short" de-embedding procedure where a pad "open" structure is first measured to obtain the pad admittance, and the pad "short" structure is used to obtain the pad impedance versus frequency. The "open" and "short" structures used in the de-embedding are shown in Figure 3.4. The "open" structure consists of the test structure used to measure the element under test but with the element removed. The "short" resembles the "open" structure but with the ends of the transmission lines connected to their adjacent ground planes.

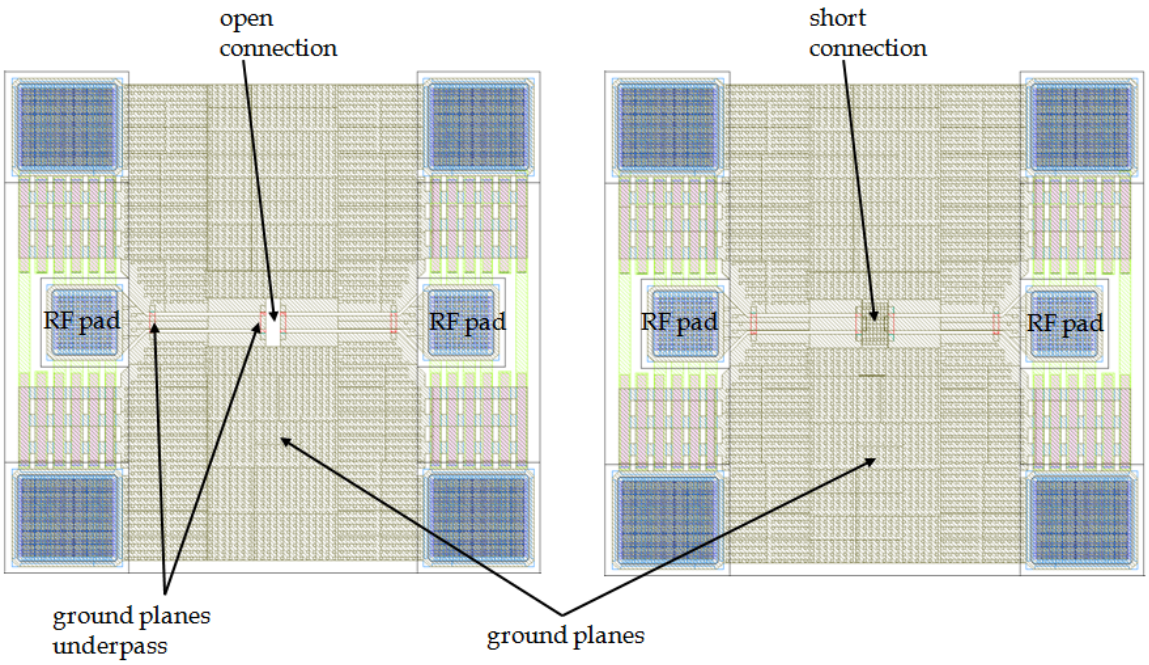

Figure 3.4: Open and short de-embedding strcutures layout

Next, a custom model was created for each component, and its parameter values were optimized in order to reach a good agreement between the simulated and measured S-

parameters. A detailed discussion of the models and fitting procedure for each component are presented in chapters 4 and 5.

In order to verify the models, a simple one-stage amplifier employing all the above mentioned components as well as a Wilkinson power combiner were built, and their measured performance compared to the simulated performance. These are presented in chapter 6. Once the models were verified, more complex power amplifiers, presented in chapter 7, are built. Figure 3.5 below shows a graphical description of the modeling milestones.

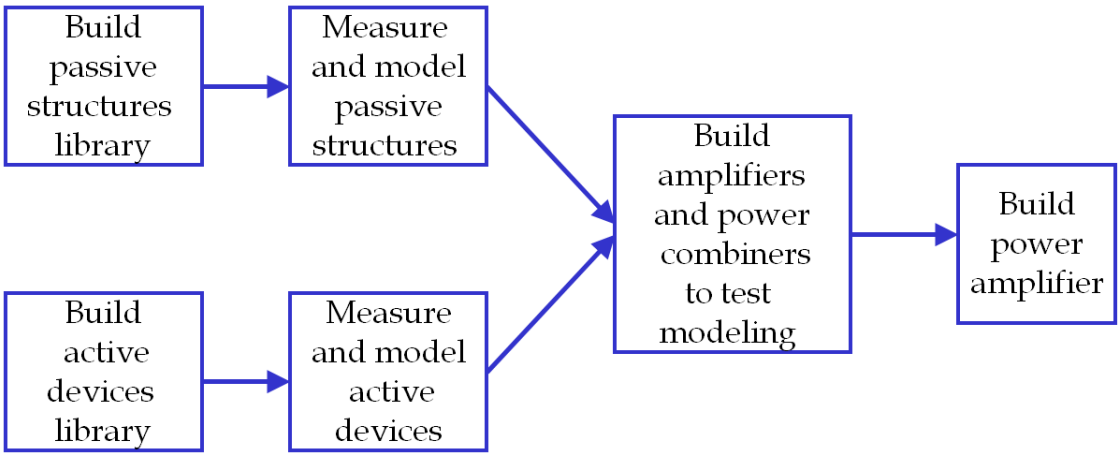

Figure 3.5: Modeling milestones

This modeling methodology results in geometry dependent, non scalable models. In other words, since the model parameter values are optimized through a curve fitting algorithm in order to match the simulated and measured results of a given structure, the values cannot be easily scaled as the structure geometry scales. As a result, only the structures that are built, measured, and modeled can be used in the amplifier design. Thus, in order to provide design flexibility, a large library of passive components and

active devices was built, measured, and modeled. The library is described next in section 3.3.

3.3 Test Chips

In order to create libraries of passive structures and active devices and to model each basic component on its own, two test chips comprising passive and actives structures of different sizes and types were built and measured. The two test chips die photos are shown in Figure 3.6 and Figure 3.7.

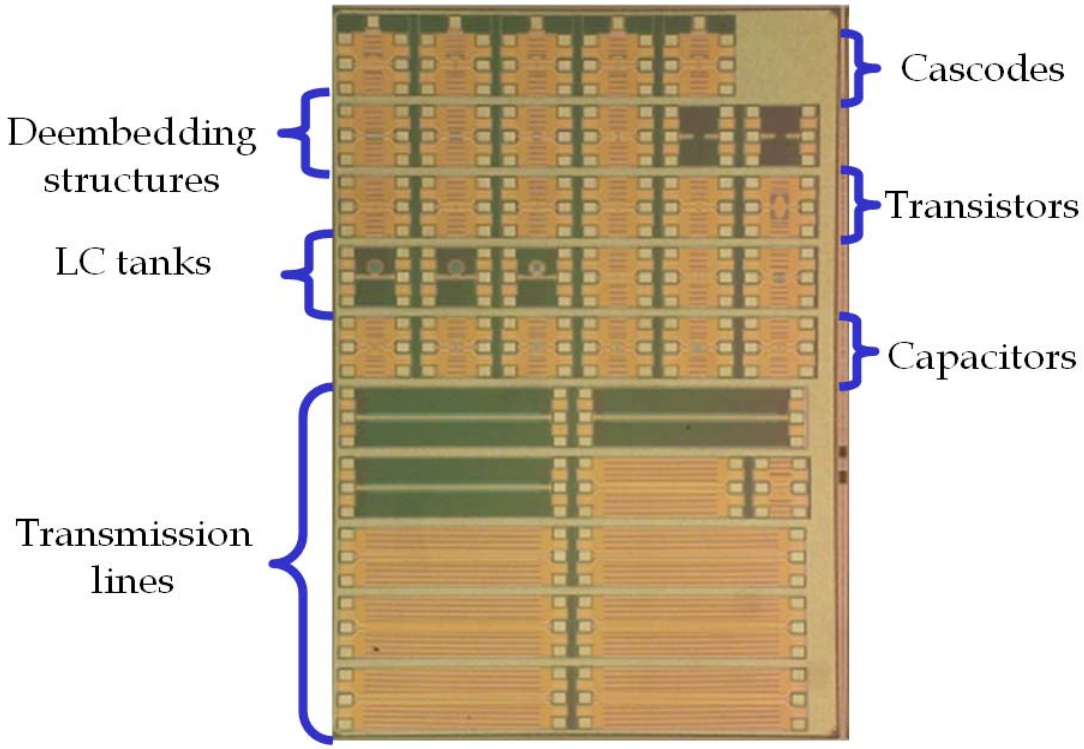

Figure 3.6: Test chip 1

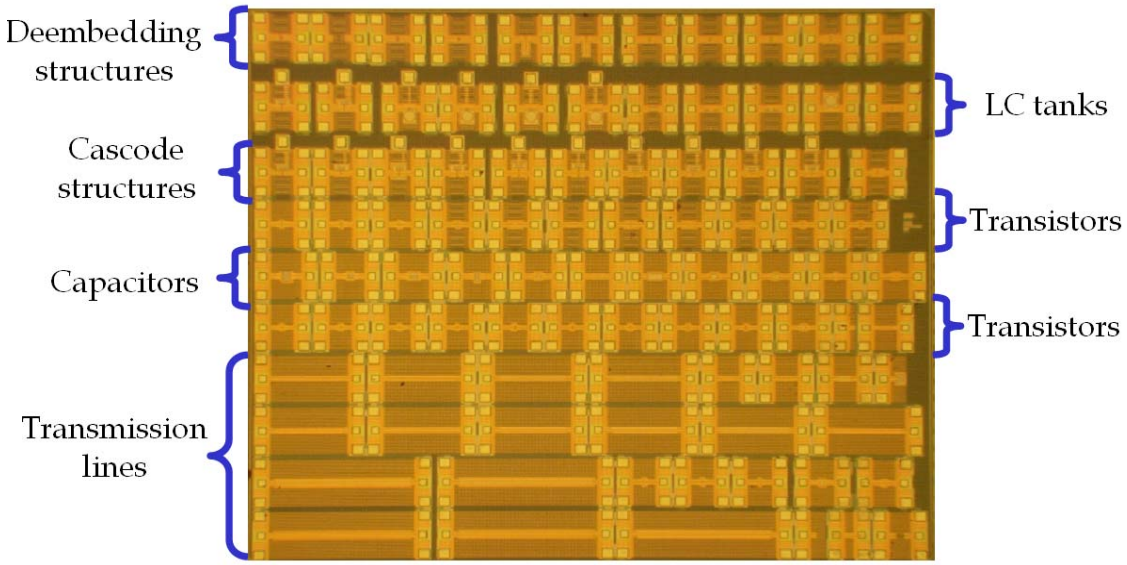

Figure 3.7: Test chip 2

The following is a detailed list of the fabricated test structures:

1. Transistors
    a. Common-source configuration, NMOS, 40 fingers, 1µm per finger
    b. Common-source configuration, NMOS, 50 fingers, 1µm per finger
    c. Common-source configuration, NMOS, 60 fingers, 1µm per finger
    d. Common-source configuration, NMOS, 80 fingers, 1µm per finger
    e. Common-source configuration, NMOS, 100 fingers, 1µm per finger
    f. Common-source configuration, NMOS, 400 fingers, 1µm per finger
    g. Cascode configuration, NMOS, 20 fingers, 1µm per finger
    h. Cascode configuration, NMOS, 40 fingers, 1µm per finger
    i. Cascode configuration, NMOS, 60 fingers, 1µm per finger
    j. Cascode configuration, NMOS, 80 fingers, 1µm per finger
    k. Cascode configuration, NMOS, 100 fingers, 1µm per finger
2. Transmission lines
    a. Coplanar, on metal 7, 1mm length, 10 µm metal width, 2 µm gap
    b. Coplanar, on metal 7, 1mm length, 10 µm metal width, 3 µm gap
    c. Coplanar, on metal 7, 1mm length, 10 µm metal width, 4 µm gap
    d. Coplanar, on metal 7, 1mm length, 10 µm metal width, 7 µm gap
    e. Coplanar, on metal 7, 1mm length, 10 µm metal width, 9 µm gap
    f. Coplanar, on metal 7, 500 µm length, 10 µm metal width, 2 µm gap
    g. Coplanar, on metal 7, 500 µm length, 10 µm metal width, 3 µm gap
    h. Coplanar, on metal 7, 500 µm length, 10 µm metal width, 4 µm gap
    i. Coplanar, on metal 7, 500 µm length, 10 µm metal width, 7 µm gap

   j. Coplanar, on metal 7, 500 µm length, 10 µm metal width, 9 µm gap
   k. Coplanar, on metals 6 and 7, 500 µm length, 10 µm metal width, 2 µm gap
   l. Coplanar, on metals 6 and 7, 500 µm length, 10 µm metal width, 3 µm gap
   m. Coplanar, on metals 6 and 7, 500 µm length, 10 µm metal width, 4 µm gap
   n. Coplanar, on metals 6 and 7, 500 µm length, 10 µm metal width, 7 µm gap
   o. Coplanar, on metals 6 and 7, 500 µm length, 10 µm metal width, 9 µm gap
   p. Coplanar, on metal 7, 100 µm length, 10 µm metal width, 2 µm gap
   q. Coplanar, on metal 7, 100 µm length, 10 µm metal width, 3 µm gap
3. AC coupling capacitors
   a. Multi- finger, metals 1-5, 10 µm x 12 µm
   b. Multi- finger, metals 1-5, 10 µm x 25 µm
   c. Multi- finger, metals 1-5, 25 µm x 25 µm
   d. Multi- finger, metals 1-5, 25 µm x 50 µm
   e. Multi- finger, metals 1-5, 50 µm x 25 µm
   f. Multi- finger, metals 1-5, 50 µm x 50 µm
4. Supply-ground bypass capacitors
   a. Multi-finger, 1-port, 50 µm x 25 µm
   b. Multi-finger, 1-port, 50 µm x 50 µm
5. 50 Ω resistor
6. 60 GHz LC tanks
7. De-embedding structures

3.4 Conclusion

Modeling of passive structures and active devices plays an increasingly crucial role at mm-wave frequencies as the passive losses due to skin effect, substrate loss, and proximity effects are substantially high and the active devices gains are considerably low such that a very small error margin between measurement and simulation can be tolerated.

The modeling strategy followed in this work consists in breaking up the amplifier into its basic constituent components, building test structures for each component, measuring their S-parameters at frequencies up to 65 GHz, modeling each component on

its own by using custom models and optimizing the model parameters to fit the measured data, and then putting together the complete model.

As CMOS technology scales further, future processes can provide higher gain and thus higher modeling error margin can be tolerated, simplifying the modeling process.

CHAPTER 4

PASSIVE STRUCTURES

DESIGN AND MODELING

4 Passive Structures Design and Modeling

This chapter discusses the design, optimization, and modeling of mm-wave passive structures in detail. The design and modeling of transmission lines, capacitors, and RF pads are covered in sections 4.1, 4.2, and 4.3 respectively.

4.1 Transmission Lines Design and Modeling

Transmission lines play a central role in mm-wave amplifiers. As the frequency of operation increases and the wavelength decreases, electrically long transmission lines such as quarter wave become short enough to be integrated on-chip. Moreover, as the actual physical circuit size approaches a substantial fraction of the signal wavelength when operating at frequencies as high as 60 GHz, the lumped circuit assumption breaks down, and all routing elements should be designed and treated as transmission lines.

Transmission line concepts are covered in section 4.1.1. The advantages of using transmission lines in lieu of lumped passive elements will be discussed in section 4.1.2 and a comparison between coplanar and microstrip transmission lines is given in section 4.1.3. Then, in section 4.1.4, a library of transmission lines of different geometries that are built, measured, and modeled is described. Finally, transmission lines modeling methodology with Agilent's Automated Design System (ADS) [32] and Ansoft's High Frequency Structure Simulator (HFSS) [33] is presented in sections 4.1.5 and 4.1.6 respectively.

4.1.1 Transmission Line Concepts

There exist a variety of transmission lines types. However, the coplanar and the microstrip transmission lines shown in Figure 4.1 and Figure 4.2 are the most appropriate to be integrated on silicon and used in amplifier design.

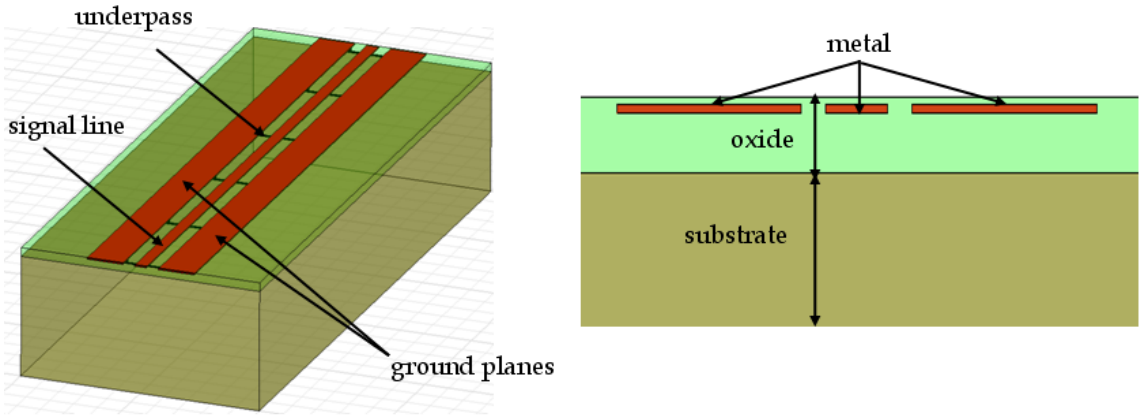

Figure 4.1: Layout of a coplanar transmission line

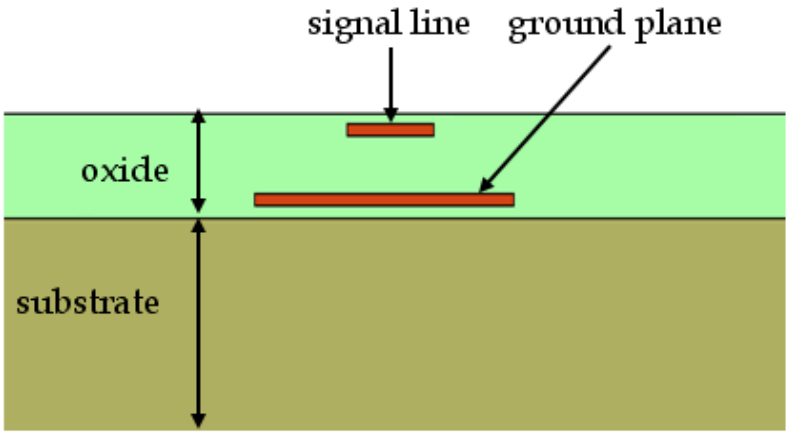

Figure 4.2: Cross sectional view of the layout of a microstrip transmission line

A transmission line is a distributed structure whose voltages and currents can vary in magnitude and phase over length. It can be characterized by its equivalent distributed circuit model shown in Figure 4.3 [29]

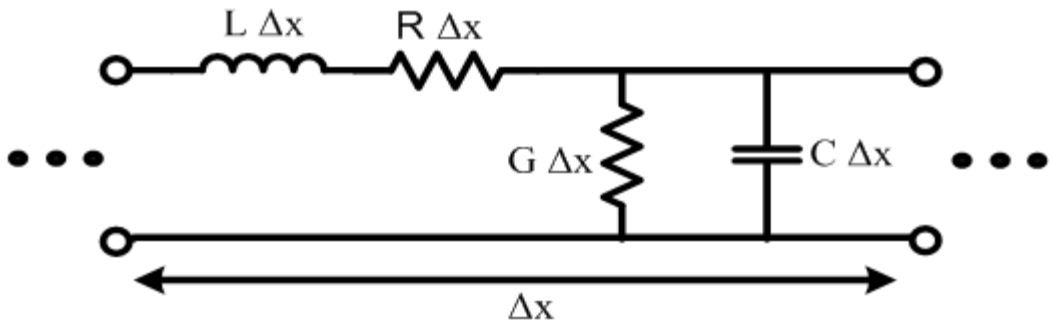

Figure 4.3: Transmission line distributed model

The short piece of the transmission line of length Δx is modeled as a frequency dependent lumped element circuit where R, L, G, and C are per unit length quantities defined as follows [34]:

R = series resistance per unit length

L = series inductance per unit length

G = shunt conductance per unit length

C = shunt capacitance per unit length

The R, L, G, and C parameters that characterize a transmission line can be related to its characteristic impedance (Z_o) and its complex propagation constant (γ) by: [35]

$$Z_o = \sqrt{\frac{R + j\omega_o L}{G + j\omega_o C}} \tag{4.1}$$

$$\gamma = \sqrt{(R + j\omega_o L)(G + j\omega_o C)} = \alpha + j\beta$$

where α and β are the attenuation and phase constants. For low loss lines, α and β can be approximated as follows: [35]

$$\alpha \approx \frac{R}{2Z_o} + \frac{GZ_o}{2} \tag{4.2}$$

$$\beta = \frac{2\pi}{\lambda_g} = \omega_o\sqrt{LC}$$

When transmission lines are fabricated on high resistivity substrates such as GaAs, the shunt conductance is essentially zero and drops from the attenuation constant equation which becomes a function of the series unit resistance only. However, silicon substrates have relatively low resistivity of about 10 Ω-cm which leads to non-negligible shunt conductances, and thus both R and G remain combined in the attenuation constant in equation (4.2). In order to de-couple the two loss mechanisms and make it easier to discern the relative importance of R and G, the following four real parameters that characterize the transmission line are proposed in [4]:

$$Z \equiv \sqrt{L/C}$$

$$\lambda \equiv \frac{2\pi}{\omega_o \sqrt{LC}} \tag{4.3}$$

$$Q_L \equiv \omega_o \, L/R$$

$$Q_C \equiv \omega_o \, C/G$$

Q_L and Q_C are referred to as the inductive and capacitive quality factors respectively.

Quality Factor Metrics

When a transmission line is used as a resonator, the relevant definition of the quality factor (Q) of the line is [35]

$$Q_{res} = \omega_o \frac{average\ energy\ stored}{average\ power\ loss} = \frac{\omega_o (W_m + W_e)}{P_L} \tag{4.4}$$

where ω_o is the resonance frequency, W_m and W_e are the average magnetic and electric energy stored, and P_L is the average power dissipated in the line. Q_{res} can be related to Q_L and Q_C by [35]

$$\frac{1}{Q_{res}} \approx \frac{1}{Q_L} + \frac{1}{Q_C} \tag{4.5}$$

If on the other hand a transmission line is used as an inductive element whether to resonate with a transistor capacitance or as a matching network element, most of the energy stored in the line is magnetic, and thus a more meaningful definition of its quality factor is [4]

$$Q_{net} \equiv 2\omega_o \frac{net\ energy\ stored}{average\ power\ loss} = \frac{2\omega_o(W_m - W_e)}{P_R + P_G} \tag{4.6}$$

where P_R and P_G are the average power dissipated in the resistance and conductance respectively. It is shown in [4, 27] that Q_{net} can be related to the inductive and capacitive quality factors Q_L and Q_C as

$$\frac{1}{Q_{net}} = \frac{1}{\eta_L Q_L} + \frac{1}{\eta_C Q_C} \tag{4.7}$$

where

$$\eta_L = 1 - \frac{W_e}{W_m}$$
$$\eta_C = \frac{W_m}{W_e} - 1 \tag{4.8}$$

Thus, if the transmission line is used as an inductive element where $W_m >> W_e$, we get $Q_{net} \approx \eta_L Q_L$ and therefore the loss in the line is determined primarily by Q_L. If on the other hand the transmission line is used as a capacitive element where $W_e >> W_m$, we get $Q_{net} \approx \eta_C Q_C$ and therefore the loss in the line is determined primarily by Q_C [4, 36].

4.1.2 Advantages of Using Transmission Lines

The on-chip signal quarter wavelength at 60 GHz is around 625 μm which makes possible the realization of integrated electrically long transmission lines on chip. The use of integrated transmission lines opens up a realm of opportunities because it means that complete matching networks, power splitters, and power combiners can be designed

using solely transmission lines and integrated on chip. Transmission lines can be designed to obtain specific characteristic impedances leading to optimized network design. Short sections of transmission lines can be used as capacitors or inductors. Compared to lumped spiral inductors, the transmission lines reactance is more predictable, less influenced by surrounding structures, and provides better isolation.

The use of transmission lines in mm-wave circuits solves the problem of ambiguity as to how the reference planes are defined. Since the ground planes and the signal line in a transmission line are in close proximity and the distance between them is well defined, the return signal path is well known and thus the resulting reactances are well predicted. The well defined return path also reduces magnetic and electric field coupling to adjacent structures.

Moreover, since well modeled transmission lines are used as interconnect between all the basic components, i.e. transistors, capacitors, pads, etc, no parasitic interconnect is left un-modeled. This proves crucial at mm-wave frequencies where short parasitic metal slabs of impedances less than 100 pH can result in large deviation between simulation and measurement results.

Furthermore, transmission lines are scalable in length, i.e. a transmission model that is verified for a 1 mm line would work with any transmission line length. As a result, precise desired impedances can be realized by just changing the length of a given transmission line. This inherent scalability of transmission lines also simplifies simulation and design.

4.1.3 Coplanar vs. Microstrip Transmission Lines

Microstrip transmission lines can be realized on silicon by using the top metal layer for the signal line and the lowest metal layer as the ground line. This geometry results in an easy way to connect the transmission lines to the rest of the circuit elements since all signal lines will reside in the top metal layer with a large ground shield underneath. However, since the distance between the metal layers is fixed, microstrip transmission lines provide only one geometry variable, the signal line width, that affects both the line loss as well as the distributed inductance and capacitance along the line. As the distance between the top and the lowest metal layer in standard CMOS processes is usually small, in the order of 4 μm, microstrip transmission lines in such processes enjoy large capacitance per unit length while they suffer from small inductance per unit length. According to equation (4.3), this results in large capacitive and low inductive quality factors. If the signal line width is decreased in order to increase the distributed inductance in an attempt to increase the inductive quality factor, the resistive losses in the line will increase and as a result will lead to low quality factors.

Coplanar transmission lines [37, 38], on the other hand, reside entirely in the top metal layer and their distributed inductance and capacitance are largely determined by the gap spacing between the signal line and the ground planes. This provides an additional degree of freedom in their design as the signal line width can be optimized for minimum resistive losses and the gap spacing can be optimized for the Q_L-Q_C tradeoff. Since transmission lines in amplifiers are usually used to resonate transistor capacitances and serve as inductive elements in matching networks, coplanar transmission lines are

preferred over microstrip transmission lines in mm-wave design. As shown in Figure 4.4, inductive quality factors of about 27 are achievable at 60 GHz for coplanar transmission lines with gap spacing of 9 μm. Moreover, since the gap spacing in coplanar transmission lines is a lateral dimension determined by lithography while in a microstrip it is a vertical dimension, the characteristic impedance of coplanar lines are more predictive and constant over process than that of microstrip lines.

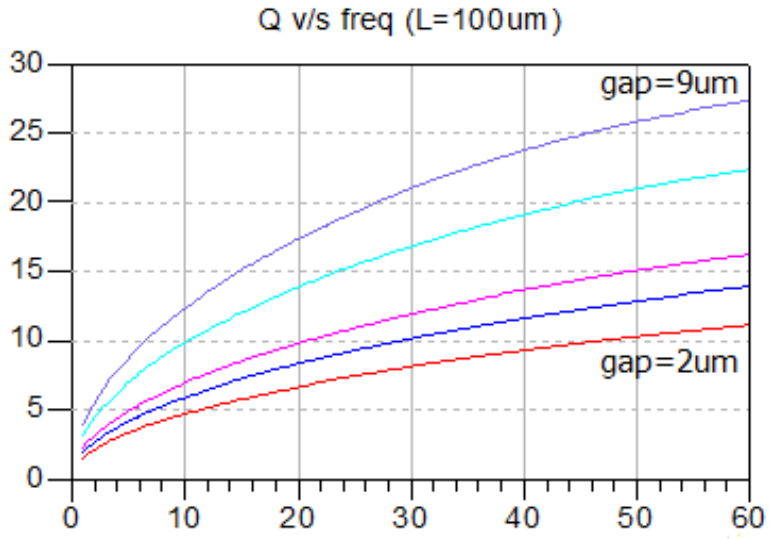

Figure 4.4: Simulated coplanar transmission lines inductive quality factor vs. frequency

4.1.4 Transmission Lines Library

Two sets of coplanar transmission lines have been built. The first set resides exclusively in the top metal layer, M7, i.e. both the signal line and the ground planes are composed of M7 only. In an attempt to achieving lower resistance and thus higher quality factors, the second set of transmission lines utilizes the top metal layer M7 as well as the layer beneath it, M6. Both the signal line and the ground planes are composed of both

metal layers strapped with large density vias. Using M6 effectively increases the metal thickness. Thus, besides resulting in lower metal resistivity, it also results in large capacitance per unit length along the transmission line. This in turn results in lower transmission line characteristic impedance since

$$Z_o = \sqrt{\frac{R + j\omega_o L}{G + j\omega_o C}} \tag{4.9}$$

In this case, in order to realize a given impedance, a longer transmission line that utilizes M6 and M7 is needed than that utilizing only M7 which may result in higher overall loss. For each set, transmission lines of five different geometries are built. All transmission lines use 10 μm wide signal lines to reduce the resistive losses with wide ground planes, but the gap spacing between the signal line and the ground planes are 2, 3, 4, 7, and 9 μm. Underpasses residing in the lowest two metal layers, M1 and M2, connecting the two ground planes are placed at 100 μm intervals. They serve to keep the two ground planes at the same potential level and suppress higher order and undesired modes of propagation.

In order to model the transmission line losses accurately, the transmission lines that are built and measured need to have significantly larger loss than the test structure pad losses. Even though the pad losses are de-embedded from the test structure S-parameter measurements, if the transmission line structure itself have very small loss, de-embedding errors will constitute a large fraction of the actual transmission line loss and result in inaccurate results. It has been verified that transmission lines between 500 μm and 1 mm of length lead to robust results.

4.1.5 Transmission lines modeling with ADS

The ADS suite from Agilent provides a simple, length scalable, electric transmission line model that captures the line high level behavior and proved to be accurate at frequencies as high as 60 GHz. The model possesses a number of advantages over other simulation tools.

First, ADS provides a clear advantage when it comes to speed of simulation. The ADS model simulation is orders of magnitude faster than that resulting from other tools, such as Agilent's High Frequency Structure Simulator (HFSS). This becomes more pronounced as the number of transmission lines increases. The four-way power amplifier presented in section 7.1 uses upward of 30 transmission lines of different sizes and geometries. Simulating the entire amplifier with ADS can be performed in a few seconds, while simulating only the transmission lines in HFSS would take hours or days to complete.

Second, another main advantage the ADS model offers is length scalability. The model is scalable in length, i.e., all its defining parameters (except obviously the length parameter) are independent of the transmission line length. Thus, the model can be optimized to fit the measured S-parameters of specific transmission line geometry of some given length, say 1 mm, and then it can be used to model a transmission line of the same geometry, but of any length, by just changing its length property. This significantly eases the overall amplifier design as transmission lines lengths often need to be changed multiple times in a trial and error fashion in order to realize a given impedance.

The third important advantage that the ADS transmission line model presents is its compatibility with the ADS optimization engine. ADS provides an optimization engine in the same suite where its transmission line model resides. Thus, using ADS, the transmission lines length in a given circuit can be all optimized at once in order to obtain specific performance criteria. For example, a complete amplifier model can be built where matching networks and interconnects employ transmission lines, and the transmission lines lengths can be optimized in order to obtain given overall S-parameters and stability criteria.

On the other hand, the ADS transmission line model presents one main disadvantage. The model is geometry dependent, i.e. once the model is optimized to fit a given transmission line, the model can be employed only to arbitrary length of the same transmission line cross-sectional geometry. As a result, only transmission lines geometries that have been built, measured, and modeled can be used.

The parameters of the ADS two-port transmission line model (TLINP) are tabulated in Table 4.1.

Model parameter	Description
Zo	Characteristic impedance
L	Length
Keff	Oxide effective relative permittivity
A	Skin effect constant
F	Relative frequency
TanD	Loss tangent

Table 4.1: ADS transmission line model parameters

The model assumes that the conductor loss is caused only by skin effect, and that the shunt loss is due solely to the loss tangent.

For each transmission line in the built library, the ADS model parameters are optimized in order to fit the simulated model S-parameters to the measured S-parameters. It is important to note that the values of the oxide effective relative permittivity, the skin effect constant, and the substrate loss tangent are different for each transmission line geometry, even though all lines use the same metals and are built on the same oxide and substrate. The reason is that the model assumes one uniform oxide layer and one uniform substrate layer. However, the actual process stack includes a multitude of oxide layers with varying relative permittivities. As the transmission line geometry changes, for example, as the gap between the signal line and the ground line widens, a larger portion of the electro-magnetic field will enter lower oxide layers which have different relative permittivities than the higher layers, and thus changing the effective relative permittivity that would be computed if only one uniform layer is assumed. Moreover, while the model account for dielectric losses in the substrate, it does not account for substrate conductive losses, which are higher for larger gap transmission lines. The loss tangent can be used to account for these losses.

Each of the ten built and measured transmission lines geometries is modeled, and good agreement between the measured and simulated S-parameters over a wide frequency range (10 GHz – 65 GHz) is reached. The first set of transmission lines employ only the top metal layer with gap spacing of 2, 3, 4, 7, and 9 μm. These geometries lead to characteristic impedances of 42, 47, 52, 60, and 64 Ω respectively. The ADS model parameters for each transmission line are tabulated in Table 4.2. Figure 4.5 to Figure 4.9 show the measured vs. model S-parameters match. As the gap spacing between the signal

line and the ground planes increases, the transmission line capacitance per unit length decreases while the inductance per unit length increases, and thus the characteristic impedance increases. Moreover, as the gap spacing increases, a larger portion of the electro-magnetic field enters the substrate causing larger effective substrate loss. This is captured by an increase in the substrate loss tangent as is evident from Table 4.2.

Model parameters	gap = 2µm M7 only	gap = 3µm M7 only	gap = 4µm M7 only	gap = 7µm M7 only	gap = 9µm M7 only
Zo	41.8 Ω	47.3 Ω	51.7 Ω	60.1 Ω	64.2 Ω
Keff	4.59	4.47	4.40	4.66	4.65
A	637 dB/m	515 dB/m	418 dB/m	368 dB/m	303 dB/m
F	20 GHz	20 GHz	20 GHz	20 GHz	20 GHz
TanD	0.028	0.042	0.048	0.060	0.079

Table 4.2: ADS's TLINP transmission line model parameter values for the transmission lines using M7 only

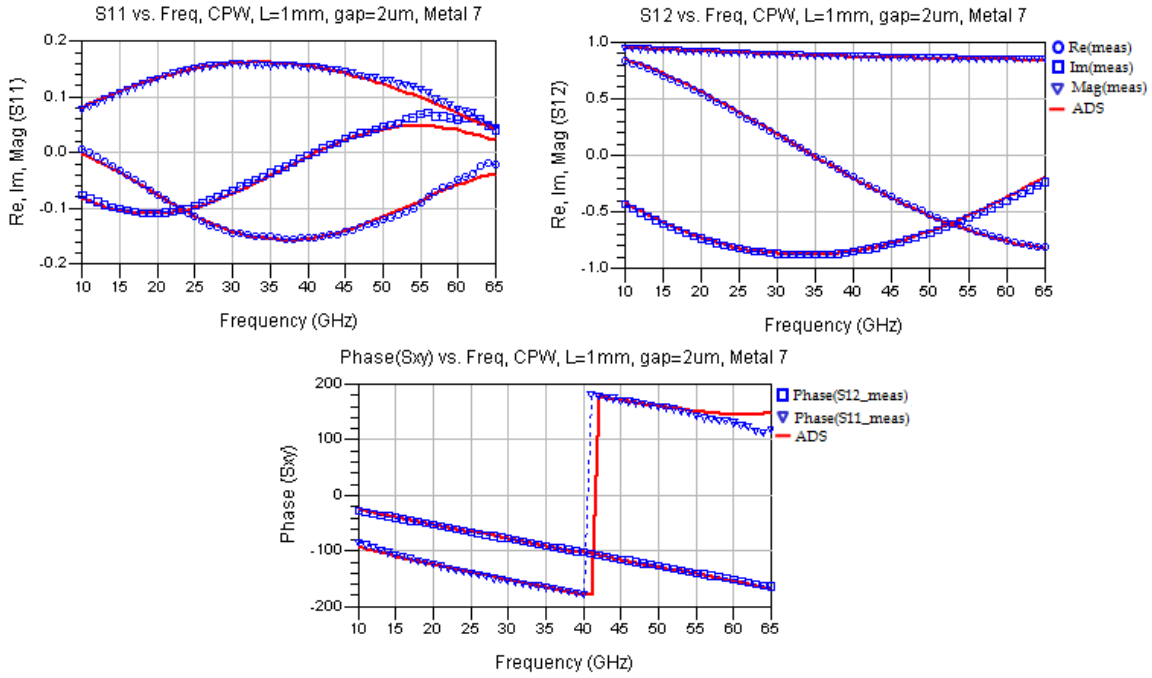

Figure 4.5: Meas vs. ADS model S-parameters for CPW on M7 with G=2µm, L=1mm

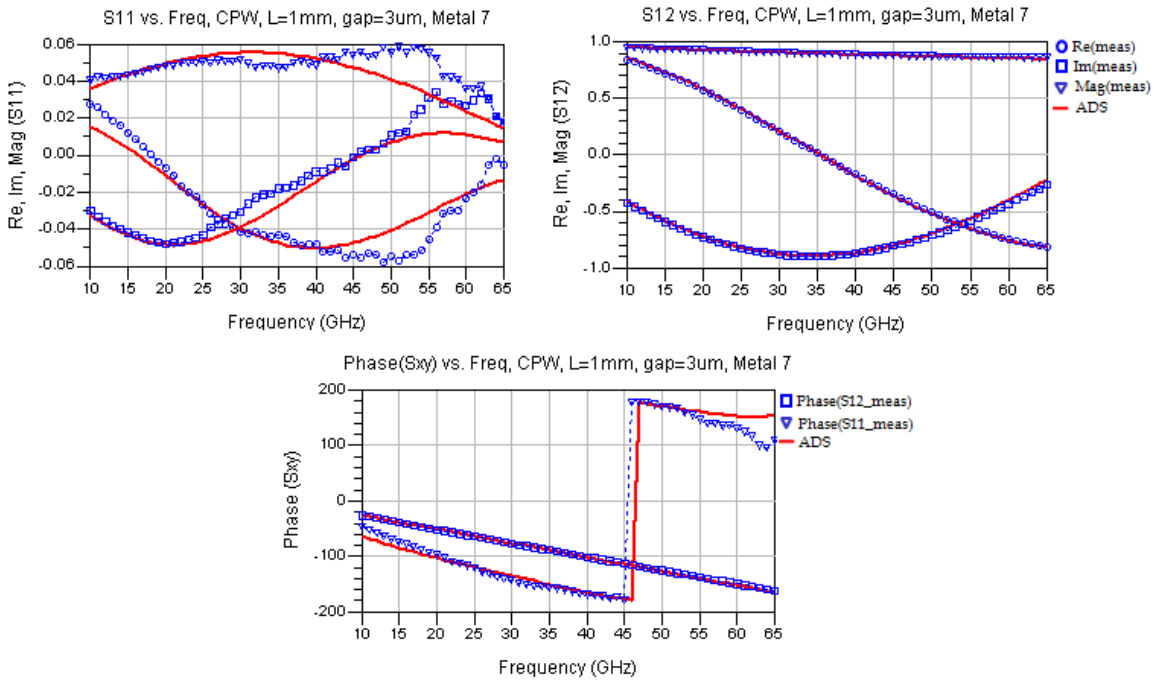

Figure 4.6: Meas vs. ADS model S-parameters for CPW on M7 with G=3µm, L=1mm

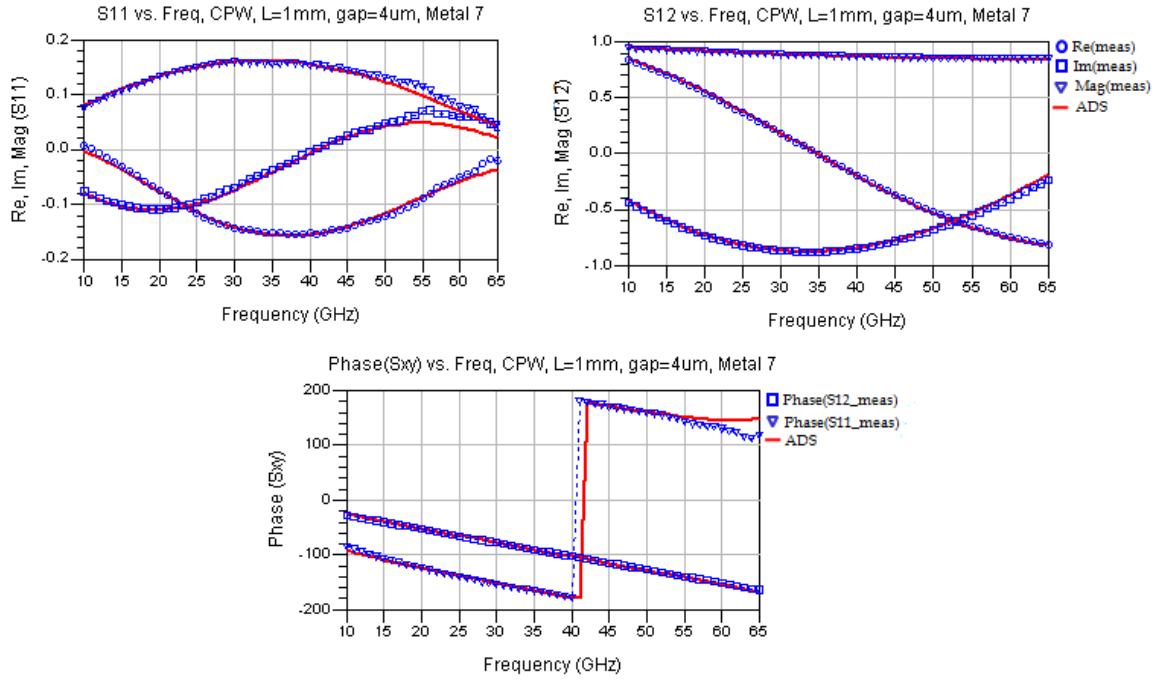

Figure 4.7: Meas vs. ADS model S-parameters for CPW on M7 with G=4µm, L=1mm

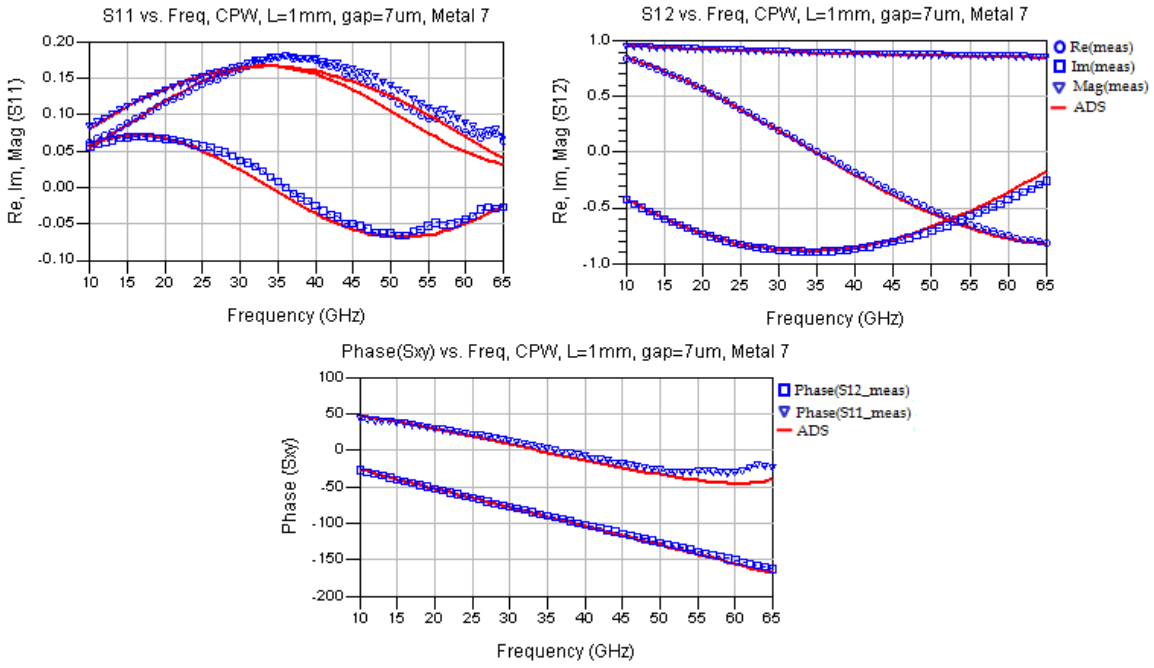

Figure 4.8: Meas vs. ADS model S-parameters for CPW on M7 with G=7µm, L=1mm

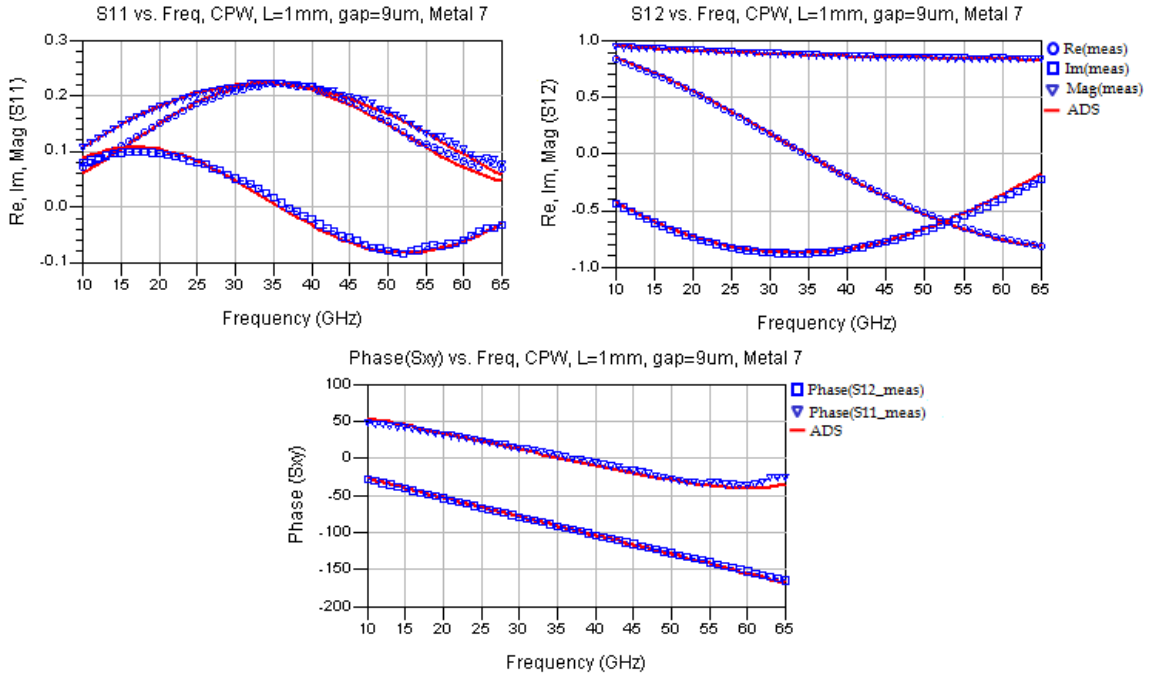

Figure 4.9: Meas vs. ADS model S-parameters for CPW on M7 with G=9µm, L=1mm

The second set of transmission lines employ the two top metal layers, M6 and M7, with gap spacing of 2, 3, 4, 7, and 9 μm as well. These geometries lead to characteristic impedances of 32, 38, 42, 51, and 54 Ω respectively. The ADS model parameters for each transmission line are tabulated in Table 4.3. Figure 4.10 to Figure 4.14 show the measured vs. model S-parameter match. Because these transmission lines use the two top metal layers, they posses higher capacitance and lower inductance per unit length. Other than having lower characteristic impedances than the transmission lines residing in M7 only, they also exhibit lower skin effect constants but higher substrate loss tangents as is evident from Table 4.2 and Table 4.3. The lower skin effect constant is a manifestation of the effective thicker metal, and the higher substrate loss tangent is due to the smaller distance between the transmission line and the substrate leading into larger substrate losses as a larger portion of the field enters the substrate.

Model parameters	**gap = 2μm M6 and M7**	**gap = 3μm M6 and M7**	**gap = 4μm M6 and M7**	**gap = 7μm M6 and M7**	**gap = 9μm M6 and M7**
Zo	31.9 Ω	37.6 Ω	42.2 Ω	50.8 Ω	54.4 Ω
Keff	4.83	4.70	4.70	4.84	5.15
A	599 dB/m	472 dB/m	401 dB/m	287 dB/m	236 dB/m
F	20 GHz	20 GHz	20 GHz	20 GHz	20 GHz
TanD	0.035	0.040	0.054	0.084	0.094

Table 4.3: ADS TLINP transmission line model parameter values for the transmission lines using M6 and M7

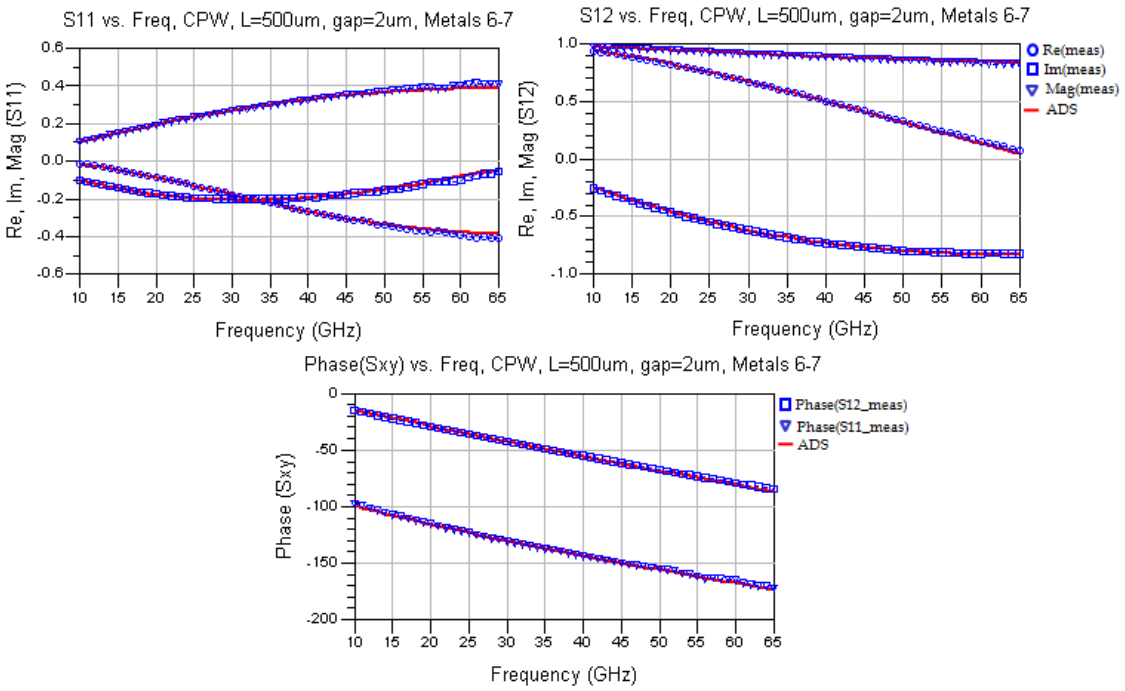

Figure 4.10: Meas vs. ADS model S- params for CPW on M6-7 with G=2µm, L=500µm

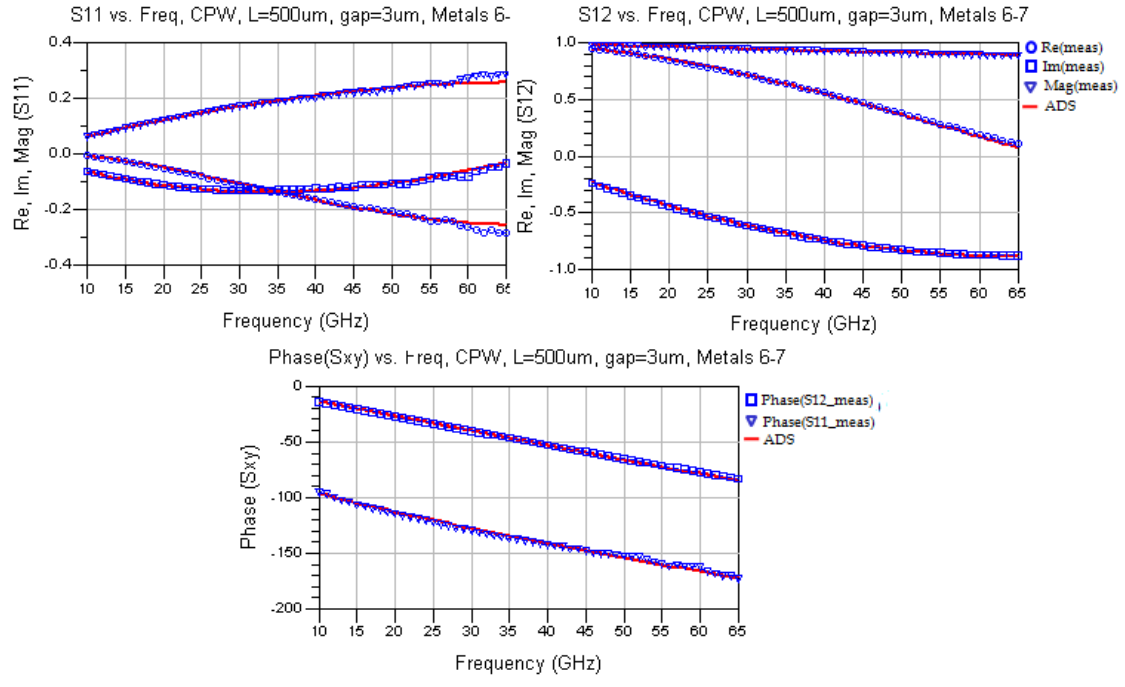

Figure 4.11: Meas vs. ADS model S- params for CPW on M6-7 with G=3µm, L=500µm

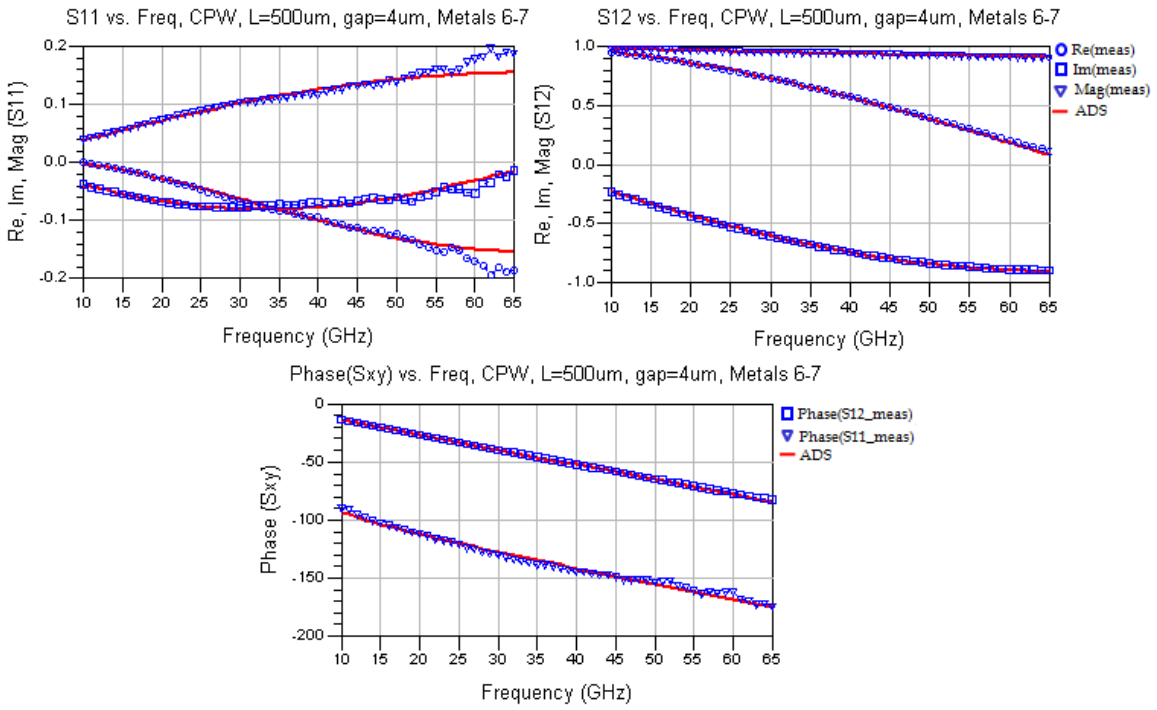

Figure 4.12: Meas vs. ADS model S-params for CPW on M6-7 with G=4µm, L=500µm

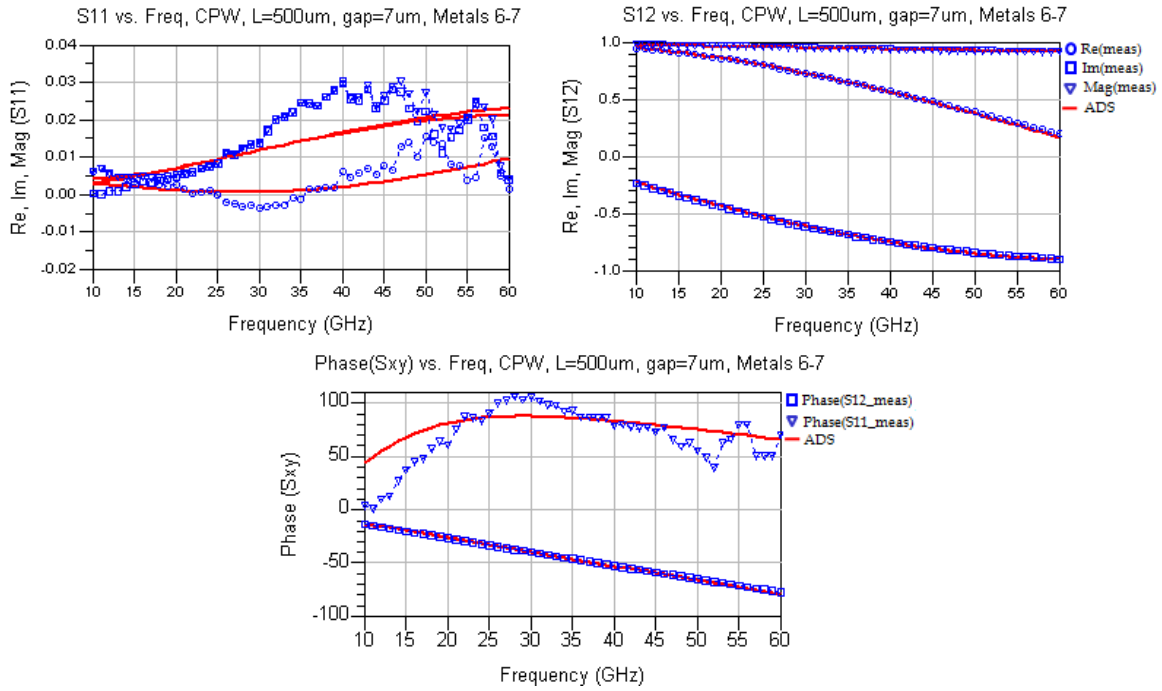

Figure 4.13: Meas vs. ADS model S-params for CPW on M6-7 with G=7µm, L=500µm

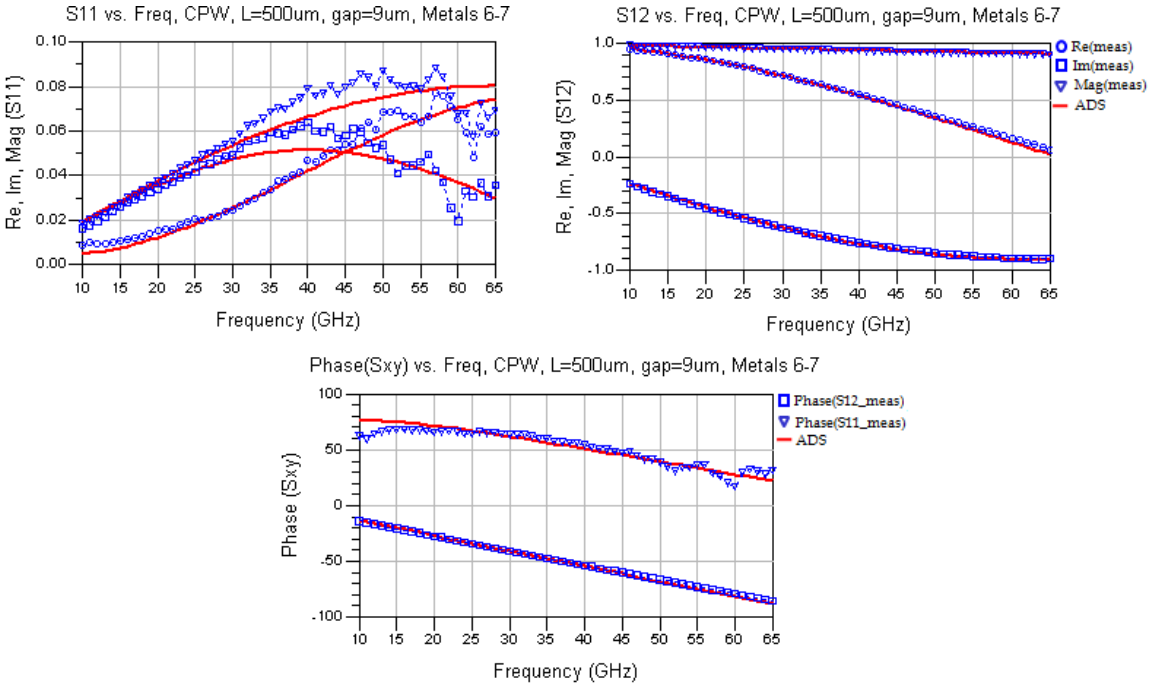

Figure 4.14: Meas vs. ADS model S-params for CPW on M6-7 with G=9µm, L=500µm

It was previously mentioned that the ADS transmission line model is length scalable, i.e. the model can be optimized for a given transmission line geometry of a given length, then the model can be used for arbitrary lengths of that transmission line geometry by changing only the length parameter. This is the case because the transmission line is uniform along its length. In order to verify this result, along with the 1 mm transmission lines, 500 µm and 100 µm lines were taped-out and measured, and their measured S-parameters were compared to the model that is optimized for the 1 mm line of the same geometry. A good S-parameter fit between measured and simulated results is obtained as shown in Figure 4.15 to Figure 4.21. As can be seen in Figure 4.20 and Figure 4.21, the measured data for the 100 µm lines is noisier than that of the 500 µm

and 1 mm lines. That is because the short transmission lines are more prone to de-embedding inaccuracies as their losses are comparable to the de-embedded pad losses.

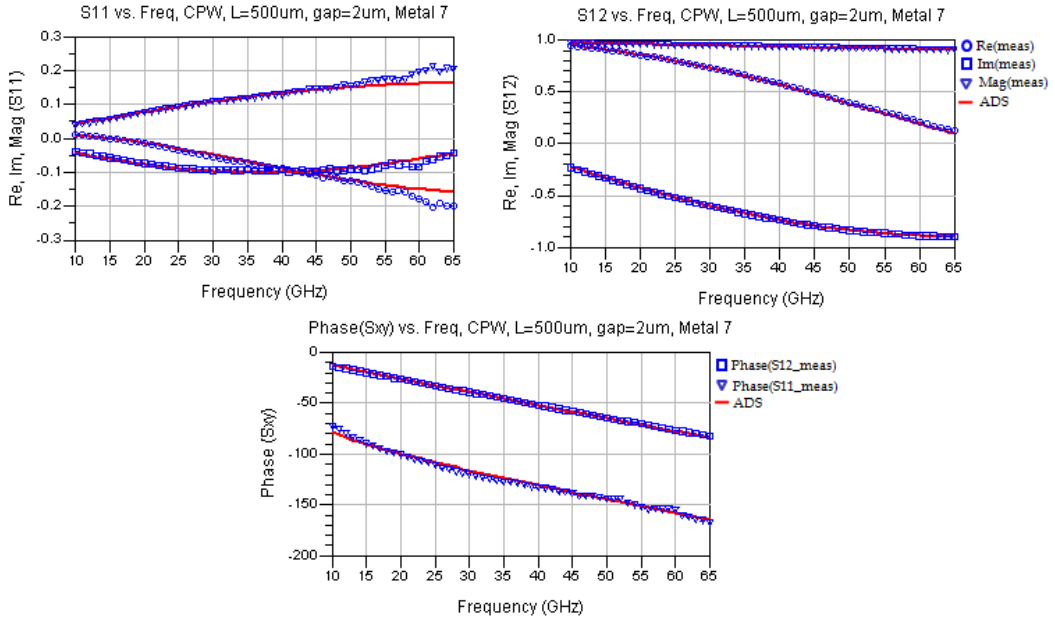

Figure 4.15: Meas vs. ADS model S-parameters for CPW on M7 with G=2µm, L=500µm

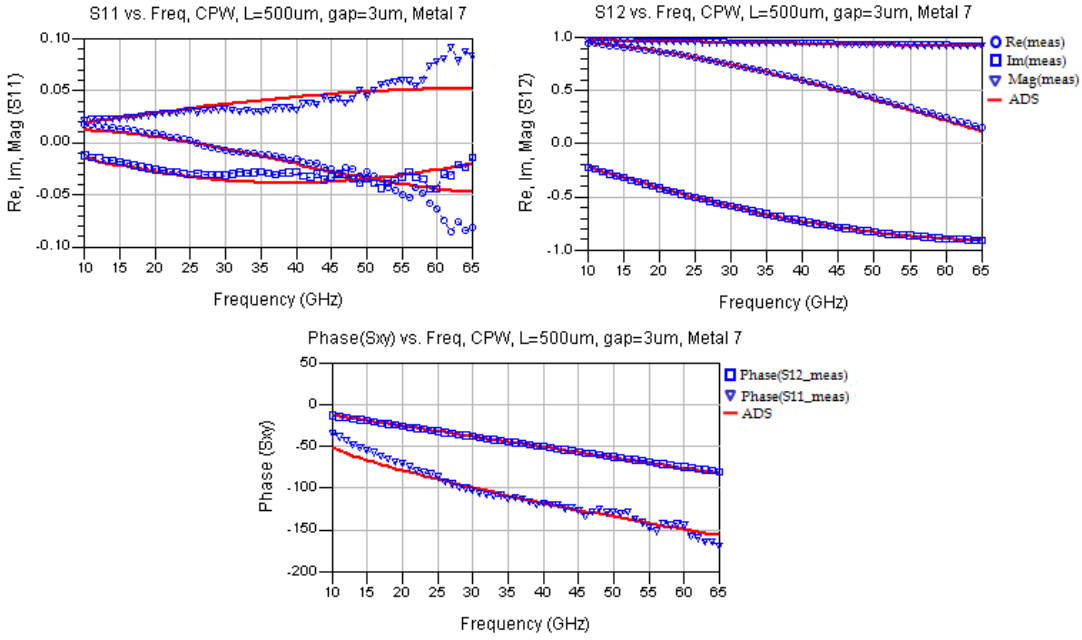

Figure 4.16: Meas vs. ADS model S-parameters for CPW on M7 with G=3µm, L=500µm

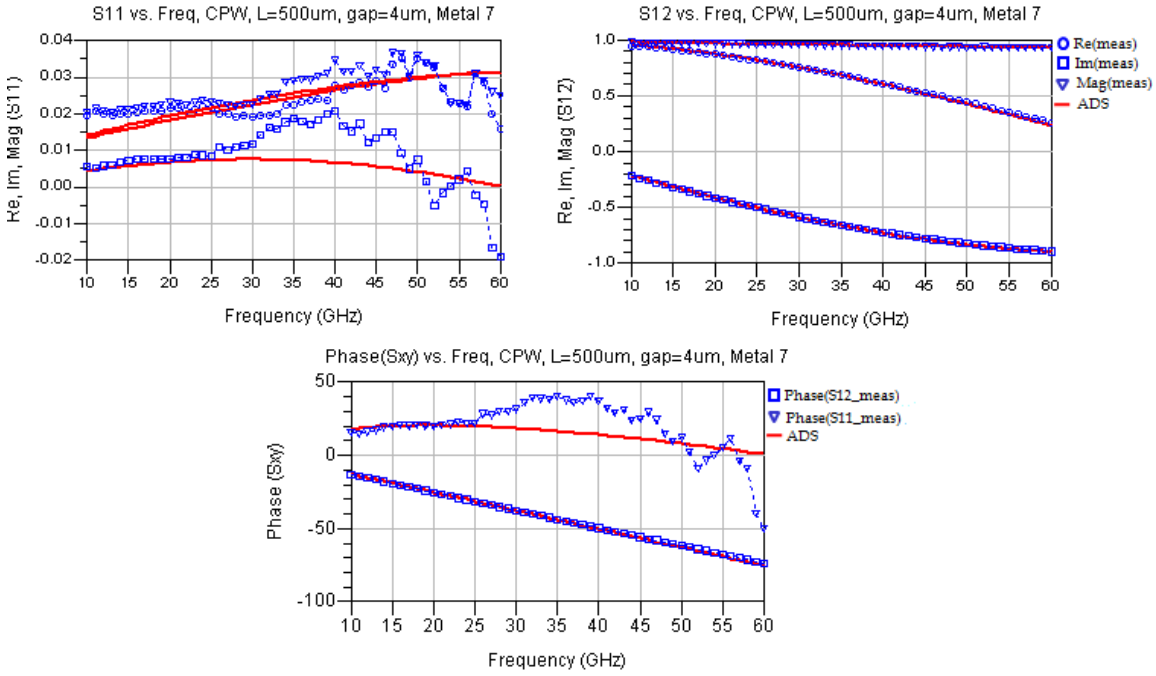

Figure 4.17: Meas vs. ADS model S-parameters for CPW on M7 with G=4µm, L=500µm

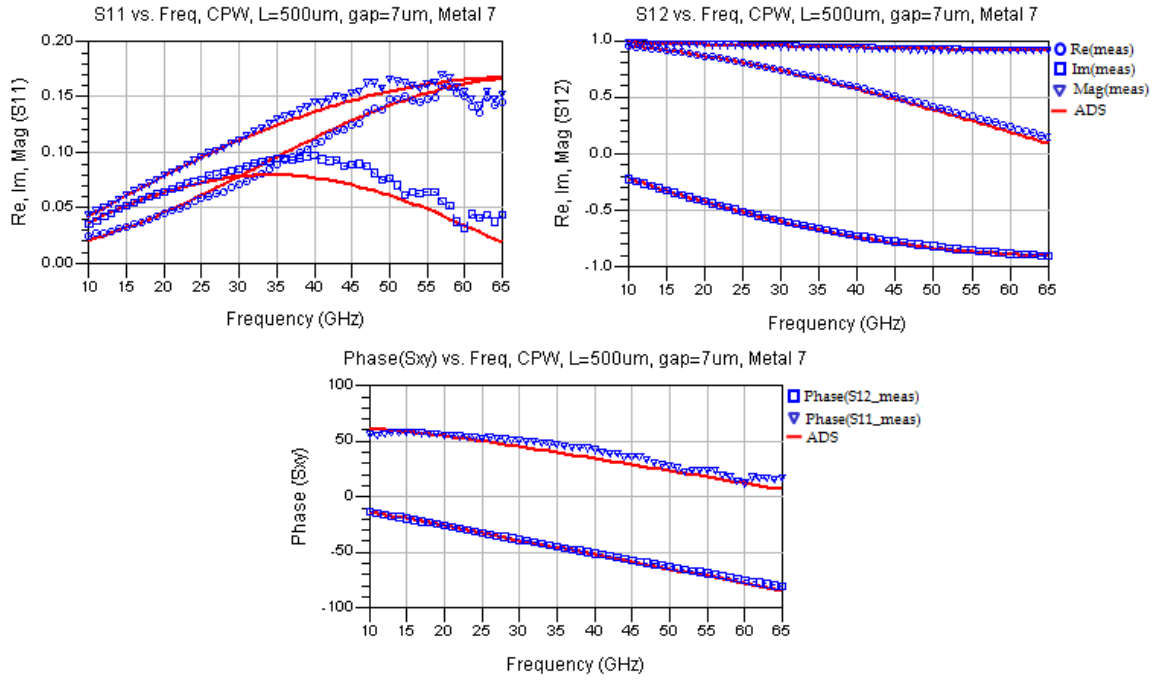

Figure 4.18: Meas vs. ADS model S-parameters for CPW on M7 with G=7µm, L=500µm

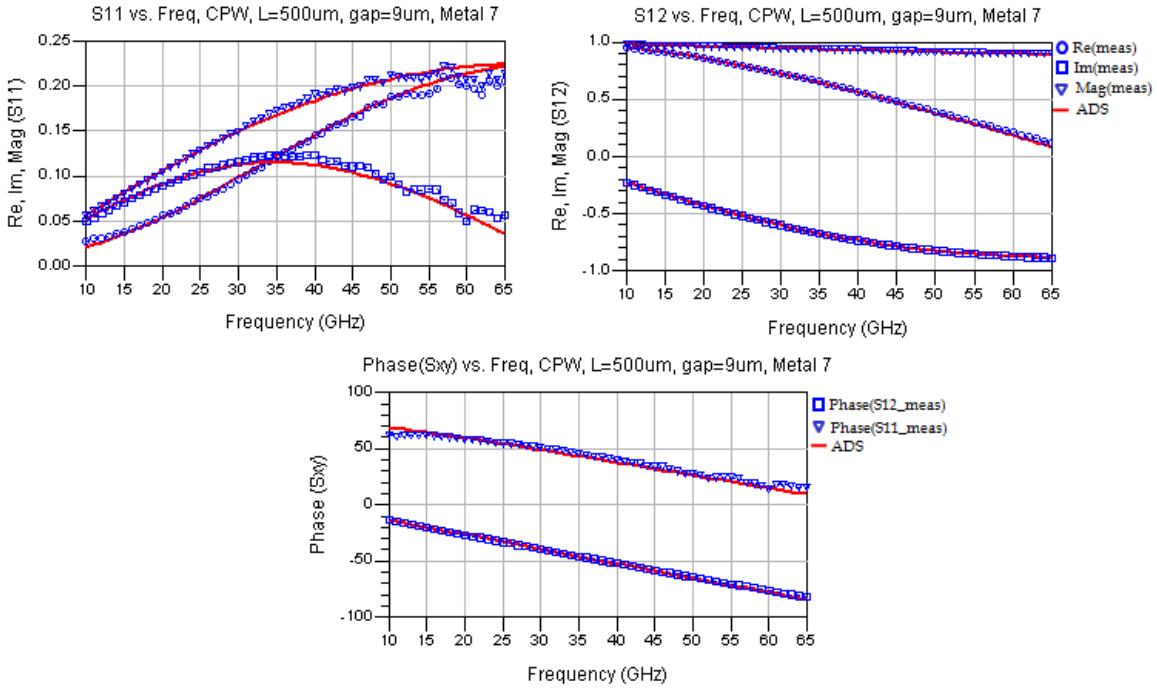

Figure 4.19: Meas vs. ADS model S-parameters for CPW on M7 with G=9µm, L=500µm

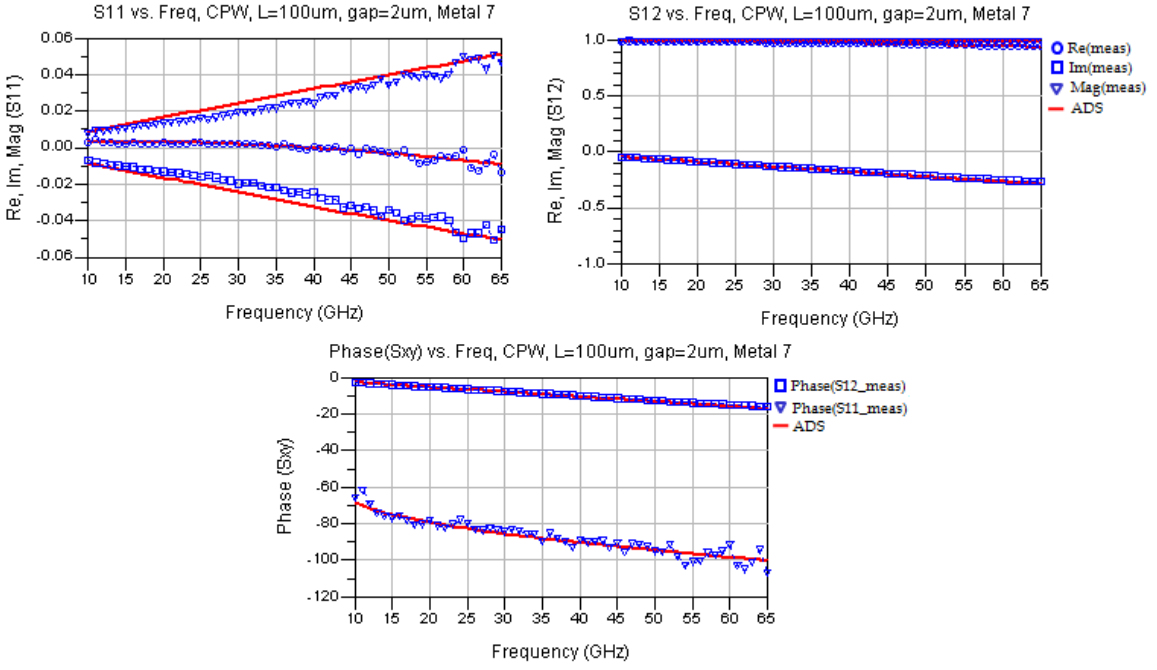

Figure 4.20: Meas vs. ADS model S-parameters for CPW on M7 with G=2µm, L=100µm

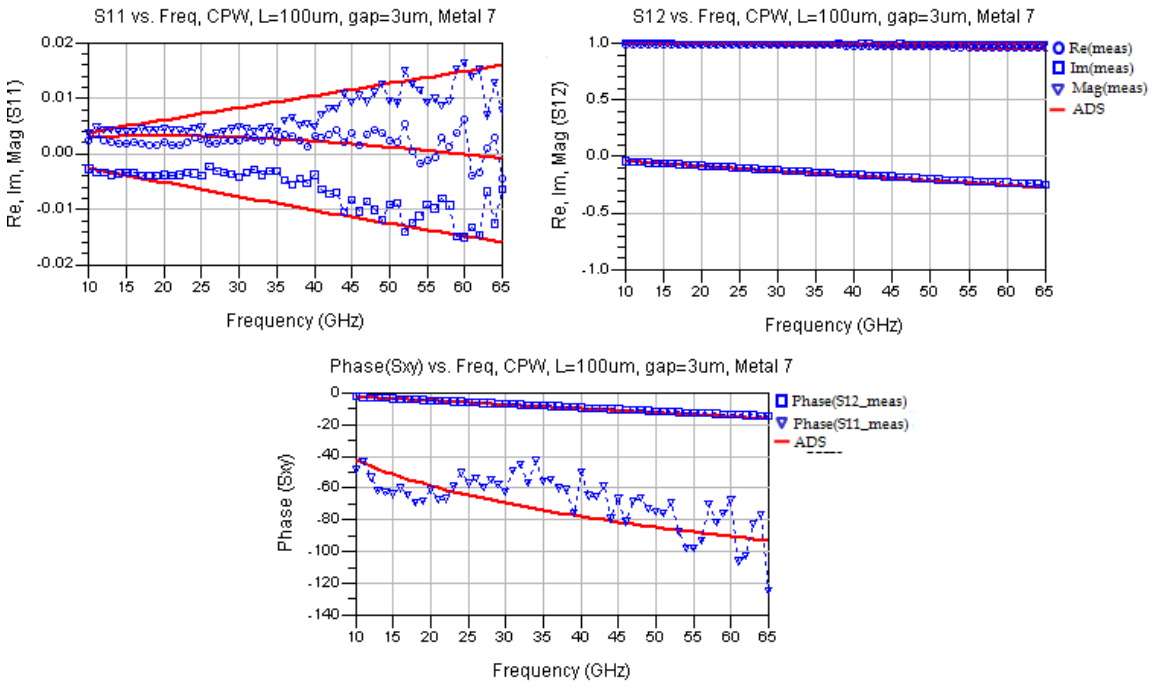

Figure 4.21: Meas vs. ADS model S-parameters for CPW on M7 with G=3µm, L=100µm

4.1.6 Transmission Lines Modeling with HFSS

The main problem with modeling transmission lines with ADS is that the model is geometry specific. Due to this limitation, only transmission line geometries that have been taped-out, measured, and modeled can be used in actual designs. In order to alleviate this problem, the full-wave electromagnetic field simulator, HFSS, can be used. HFSS possesses a number of advantages over ADS.

First, in HFSS, any arbitrary transmission line geometry, and in more general, any arbitrary passive structure can be simulated. In order to simulate a transmission line in HFSS, the process substrate stack is drawn, i.e. the silicon substrate, the oxides, the metals, the vias, the passivation, etc, each layer properties are specified, i.e. the thickness, resistivity, permittivity, loss tangent, etc., then the passive structure of a given geometry,

e.g. a transmission line, is drawn. HFSS is then used to solve the electromagnetic field in the 3D structure and S-parameters can be obtained. Thus, in contradiction to the ADS model, HFSS takes as input unique values for the parameters defining the substrate stack, i.e. the metals resistivity, oxides permittivities and loss tangents, silicon substrate resistivity and loss tangent, etc, and the same values are used in the simulation of all structures. These parameter values do not need to be optimized for each geometry. However, in order to shorten simulation time, all the oxide layers are replaced by one effective oxide layer, and all passivation layers are replaced by one effective passivation layer. Contradictory to the ADS model where the model parameters are optimized uniquely for each given transmission line geometry, the HFSS substrate parameters are optimized collectively to fit all the measured transmission lines. In other words, the HFSS substrate parameters are optimized such that all measured transmission lines S-parameters fit the HFSS simulated S-parameters. In this fashion, the transmission lines are effectively used to model the process substrate stack. Once this is achieved, not only arbitrary transmission lines models can be drawn and simulated in HFSS using the substrate model, but any arbitrary passive structure can be modeled as well.

On the other hand, the HFSS modeling strategy possesses two disadvantages when compared to ADS.

First, the HFSS simulation is considerably slow. It is orders of magnitude slower than the ADS simulation and consumes substantially more computing resources. A simulation that takes two seconds in ADS can take two hours in HFSS with comparable

results. Thus, ADS is preferred to simulate transmission lines that are already fabricated, but HFSS is used when simulating arbitrary structures.

Second, HFSS is incompatible with the ADS optimization engines. The ADS transmission line model is compatible with the ADS optimization engine, and thus ADS transmission line lengths can be optimized collectively in an amplifier circuit in order to obtain a given amplifier matching, gain, stability criteria, etc. This is not possible with HFSS.

Figure 4.22 and Figure 4.23 show the measured vs. HFSS simulated S-parameters match of some of the transmission lines.

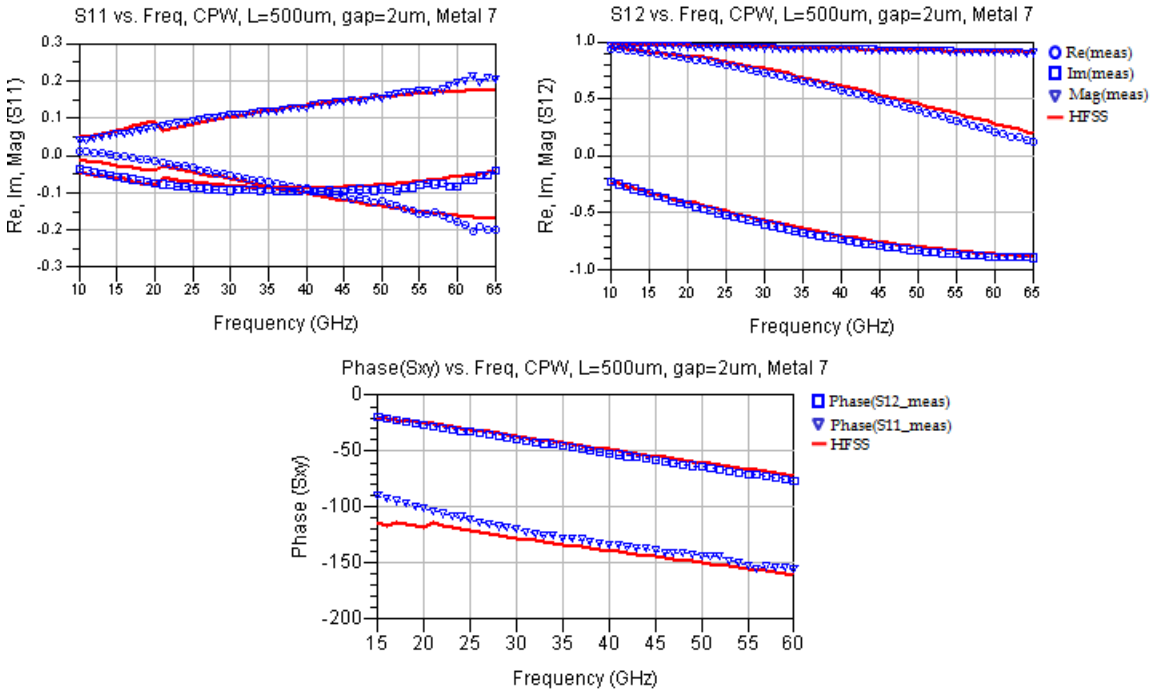

Figure 4.22: Meas vs. HFSS model S-parameters for CPW on M7 with G=2µm, L=500µm

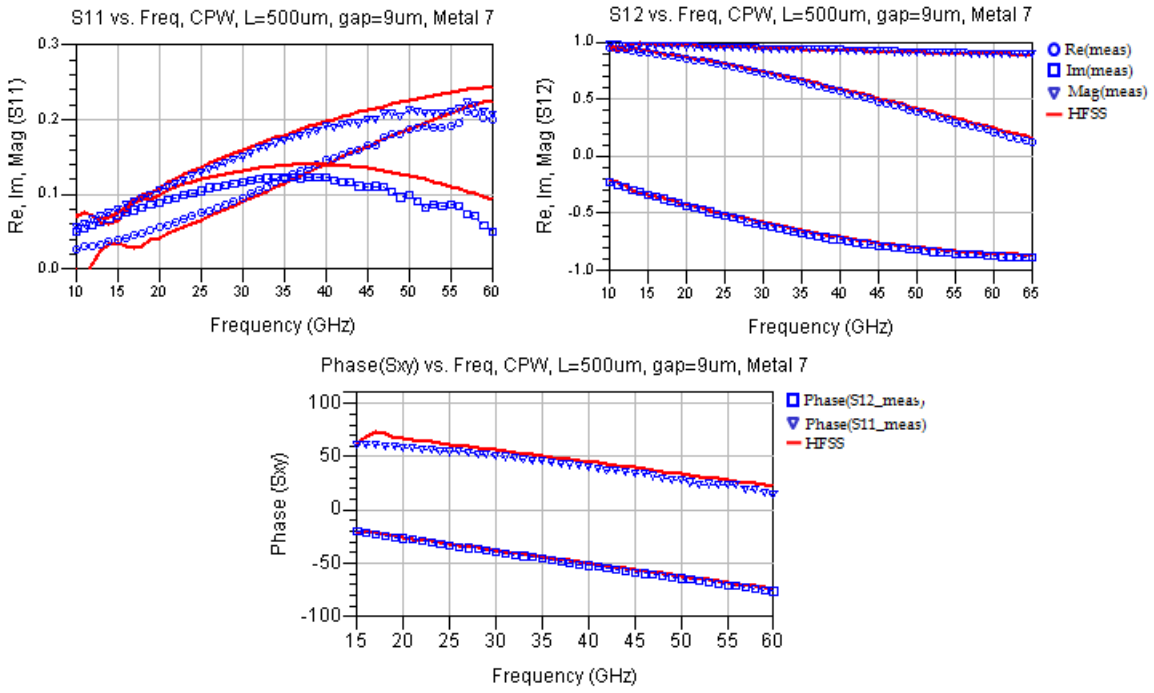

Figure 4.23: Meas vs. HFSS model S-parameters for CPW on M7 with G=9µm, L=500µm

4.2 Capacitor Modeling

In mm-wave circuits, the capacitances needed in matching networks and resonators are usually realized through transmission lines. However, lumped capacitors are needed for AC coupling and supply - ground bypass since transmission lines cannot be used for these functions. Because these lumped capacitors reside in the signal path, optimizing their design and layout as well as modeling their behavior accurately over a broad frequency range up to 60 GHz are of a crucial importance.

For both AC coupling and supply - ground bypass, an ideal structure would have infinite impedance at DC and zero impedance at the frequency of interest. Thus, large, high quality factor capacitors with series self-resonance frequencies situated at the

frequency of interest are desirable. Even if the capacitor self-resonates at a frequency below the frequency of interest, as long as its impedance at the frequency of interest is sufficiently low even if inductive, it can still be used as an effective structure for both AC coupling and supply - ground bypass. The design, layout, and modeling of AC coupling and supply - ground bypass capacitors is discussed in sections 4.2.1 and 4.2.2 respectively.

4.2.1 AC Coupling Capacitors

Design and Layout

Metal multi-finger capacitors, sometimes referred to as "MOM" (Metal-Oxide-Metal) capacitors, are preferred over Metal-Insulator-Metal (MIM) capacitors for two main reasons. First, MIM capacitors, which employ a sandwich structure with a thin high-K dielectric, require additional mask layers which result in higher fabrication cost. Second, they are defined by a vertical dimension and thus exhibit larger lot to lot variability than finger capacitors which are defined by a lateral dimension through lithography. On the other hand, MIM capacitors have the advantage of having a very high density. If the density of MIM capacitors is sufficiently larger than MOM structures, then the area savings may outweigh the additional fabrication costs. However, the availability of six or more metal layers in modern CMOS processes means that very high density structures can be realized with the metallization at no added cost. Furthermore, the high-k dielectric used in MOM capacitors may have a large loss tangent at mm-wave frequencies reducing the capacitor quality factor.

Finger capacitors are composed of a large number of parallel fingers where each other finger is connected to either port of the device as shown in Figure 4.24.

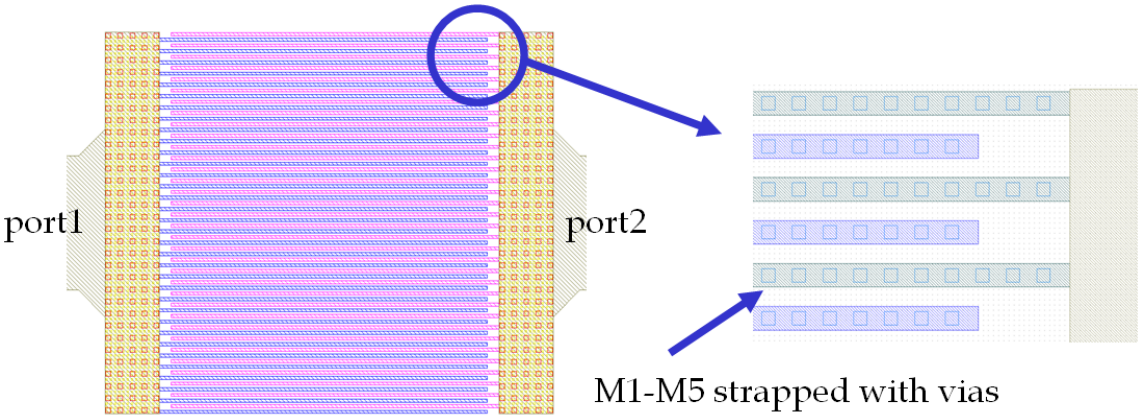

Figure 4.24: Top level view of a multi-finger metal capacitor layout

Each finger consists of all available metal layers stacked on top of each other and strapped in shunt in order first to decrease its resistance and thus increasing its quality factor, and second to increase the capacitance density. The metal layers are connected together through the maximum number of vias possible in order to take advantage of the added via to via capacitance. At each port, a port network composed of a wide slab consisting of all metal layers with a small 45^{o} taper is used to connect the fingers. If a lower parasitic substrate capacitance is desired, the lowest metal layer can be omitted, but this negatively affects the quality factor and the self-resonance frequency of the structure.

In order to realize a given capacitance, either a large number of short fingers in parallel or a small number of long fingers can be used. The former structure results in smaller finger resistance and inductance but larger port network resistance and

inductance since a bulkier port network is then required. The latter structure exhibits the opposite tradeoff.

The two-port metal multi-finger capacitor shown in Figure 4.24 and used for AC coupling presents at its two ports 10 μm wide metal leads with small 45^o tapers that reside in the top metal layer in order to connect to the driving transmission lines on the outer side and to the fingers on the inner side of the capacitor. The metal fingers are composed of all five metal layers strapped together with vias along the length of the line. This increases the capacitance density and reduces the finger resistance simultaneously. In order to maximize the capacitance density, minimum allowed metal width and minimum metal spacing are used. Noting that substantial capacitance exists between the vias themselves, the spacing between the vias is reduced to the minimum allowed by layout rules. In order to reduce the inductance between the port and the different fingers of the capacitor, 5 μm wide slabs composed of all metal layers are sandwiched between each port and the corresponding metal fingers.

A library of six capacitors of different sizes was fabricated and measured. Table 4.4 shows the measurement results for the capacitors.

Dimensions	**Capacitance at low frequency**	**$F_{resonance}$**	**Z_{in} at 60 GHz**
10 x 12 μm^2	155 fF	> 60 GHz	1.2 Ω -j 12.6
10 x 25 μm^2	308 fF	> 60 GHz	800 mΩ - j 2.5
25 x 25 μm^2	914 fF	41 GHz	250 mΩ + j 3.2
25 x 50 μm^2	1.80 pF	23 GHz	550 mΩ + j 9.8
50 x 25 μm^2	1.83 pF	25 GHz	150 mΩ +j 6.1
50 x 50 μm^2	3.74 pF	15 GHz	150 mΩ + j 9.2

Table 4.4: Finger capacitors measured performance

The measurement results in Table 4.4 show that the 25x25 μm^2 capacitor is the most suitable for AC coupling because it has the combination of both a low resistance and a small reactance at 60GHz. Even though the capacitor exhibits a series resonance at 41 GHz, below the operating frequency of 60 GHz and thus have inductive impedance at 60 GHz, its reactance and resistance are low enough to be used for AC coupling without incurring much signal loss. The 10x12 μm^2 capacitor has relatively very short fingers and thus very low series inductance. Thus, it resonates well above 60 GHz and has a capacitive reactance at 60 GHz. For this reason, it is very well suited to be used as the capacitive element in LC tanks. The 50x50 μm^2 capacitor provides the highest low frequency capacitance and thus may be suitable for supply - ground bypass. However, it presents a high inductance at 60 GHz which is undesirable. It is shown in the next section that a slightly different layout taking advantage of the fact that one of the bypass capacitor sides is always connected to ground results in lower series inductance and is better suited for supply - ground bypass. It is interesting to note the difference between the 25x50 μm^2 capacitor and the 50x25 μm^2 capacitor. Both have the same effective area and low frequency capacitance. However, the former has a smaller number of long fingers in parallel, whereas the latter has a larger number of shorter fingers in parallel. As a result, the latter structure exhibits smaller series resistance and inductance which increases its quality factor and self resonance frequency.

Modeling

In order to model the finger capacitors, the symmetric two port model shown in Figure 4.25 was used.

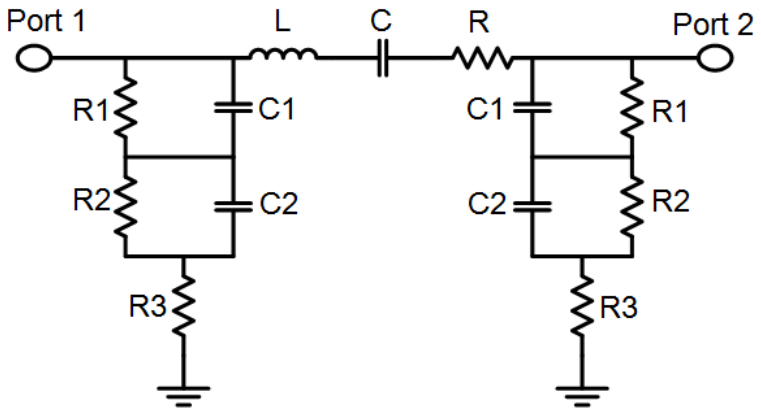

Figure 4.25: Two-port AC coupling multi-finger capacitor model

The capacitor C, the inductor L, and the resistor R model the fingers and port networks capacitance, inductance, and resistance respectively. Capacitor C_1 and resistance R_1 model the oxide capacitance and resistance respectively, whereas capacitor C_2 along with resistances R_2 and R_3 model the substrate capacitance and resistance. In order to model the overall structure, the circuit components values are optimized in order to match the model simulated network parameters to the measured network parameters. If only S-parameters are used in the optimization, it would result in an inaccurate value for the series resistance R and thus an inaccurate value of the quality factor of the capacitor. This is the case because the S-parameter simulation adds a 50 Ω resistance in series with each port overshadowing the capacitor series resistance which is in the order to hundreds of mΩ's. Thus, large variation in the series resistance would cause only small variations in the S-parameters. Instead of using the S-parameters in the fitting, Z and Y parameters are derived from the S-parameters and are used simultaneously in the optimization. Z and Y

parameters employ open and short circuits at the ports instead of 50 Ω resistors, and thus can result in accurate prediction of the fingers series resistance.

For the sake of the discussion below, we will call the series combination of C, L, and R the series branch, and we call the circuits formed by C_1, C_2, R_1, R_2, and R_3 the parallel branches. The series branch impedance is much lower than the parallel branches impedances. When simulating Z_{11}, port 2 is left open, and port 1 is driven with a current source. Since the series branch in this case appears in series with the right parallel branch, and because it has much lower impedance, the entire series branch can be replaced with a short circuit without much affecting the value of Z_{11}. Thus, fitting the simulated Z-parameters to the measured Z-parameters (extracted from the measured S-parameters) results in accurate values only for C_1, C_2, R_1, R_2, and R_3. On the other hand, when simulating Y_{12}, a short circuit is applied to port 1, and port 2 is driven with a voltage source. In this case, the left parallel branch is short circuited and no current passes through it. The current measured at port 2 is dominated by the current that passes through the series branch. Thus, fitting the simulated Y-parameters to the measured Y-parameters (extracted from the measured S-parameters) results in accurate values only for C, L, and R. As such, the series branch dominates the Y -parameters and the parallel branches dominate the Z-parameters. Thus, in order to obtain accurate values for all the model parameters, a simultaneous Z and Y parameters fit should be performed.

The model parameters for the 25x25 μm^2 capacitor are shown in Table 4.5 and its simulated and measured Z and Y – parameters are shown in Figure 4.26 and Figure 4.27.

Parameter	Value
C	917 fF
L	16 pH
R	185 mΩ
C_1	26 fF
R_1	45 kΩ
C_2	19 fF
R_2	400 Ω
R_3	47 Ω

Table 4.5: Model parameter values for the 25 x 25 µm^2 multi-finger metal AC capacitor

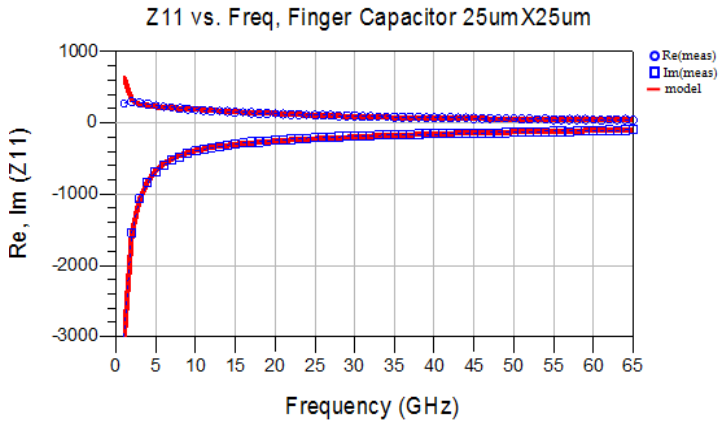

Figure 4.26: Z-parameters (derived from S-parameters) measurement vs. model for the 25µmX25µm AC coupling metal finger capacitor

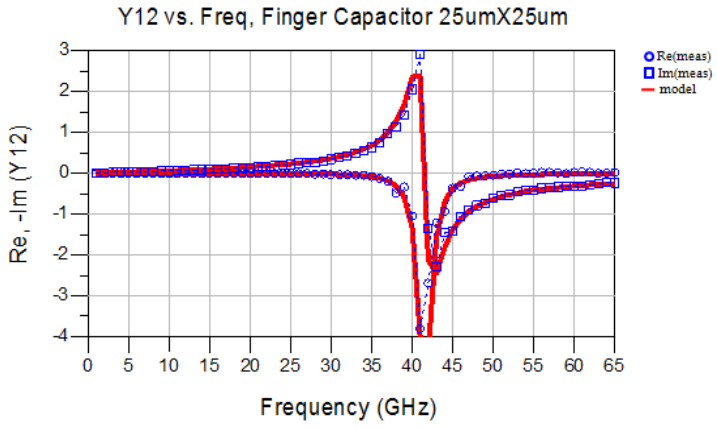

Figure 4.27: Y-parameters (derived from S-parameters) measurement vs. model for the 25µmX25µm AC coupling metal finger capacitor

4.2.2 Supply - Ground Bypass Capacitors

Design and Layout

Supply - ground bypass capacitors are required to provide sufficiently low impedance at relatively low frequencies. For this reason, very large capacitors (e.g. 2–4 pF) are desirable. However, scaling the AC coupling capacitors described above would result in considerably lower self-resonance frequency and adversely affect the capacitor behavior at mm-wave frequencies. For the same reasons as for AC coupling capacitors, multi-finger metal capacitors are also used for supply - ground bypass. However, since one port is always connected to ground, the grounded port's network (metal slab and taper) is not needed. It is eliminated from the layout, and the lowest metal layer is used as a ground plane that connects to every other finger as shown in Figure 4.28. Having a low impedance ground plane considerably lowers the series inductance and thus increases the self-resonance frequency of the capacitor enabling large capacitors to be functional at mm-wave frequencies. Similarly, a metal plane can also be used on the other port further lowering the series inductance. This increase in self resonance frequency comes at the price of lower capacitance per unit area. Capacitors measuring around 2 pF with self-resonant frequencies of 45 GHz are achieved.

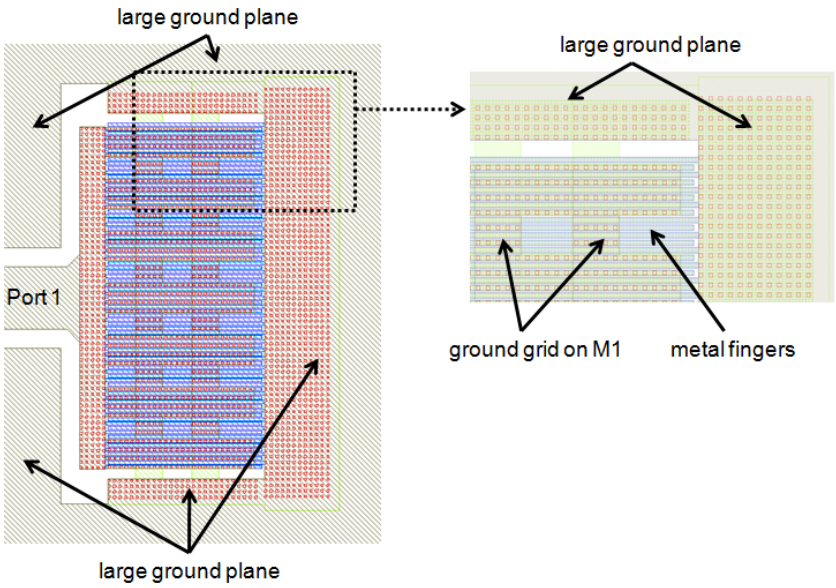

Figure 4.28: Top level view of a 1-port metal multi-finger supply-ground bypass capacitor layout

Modeling

The same modeling technique used for AC coupling capacitors is also used for supply - ground bypass capacitors. Since one port is always connected to ground, only a 1-port model is needed with the parallel branch at the second port eliminated. The model used for the supply – ground bypass capacitor is shown in Figure 4.29.

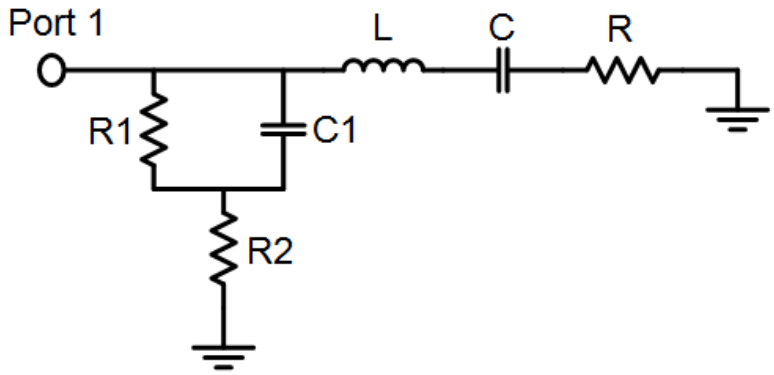

Figure 4.29: Two-port supply- ground bypass multi-finger capacitor model

The model parameters for the 50x50 μm^2 capacitor are shown in Table 4.6 and its Z and Y – parameters are shown in Figure 4.30.

Parameter	Value
C	1.92 pF
L	6.84 pH
R	177 mΩ
C_1	53 fF
R_1	1.1 kΩ
R_2	3 kΩ

Table 4.6: Model parameter values for the 50 x 50 μm^2 multi-finger metal supply-ground bypass capacitor

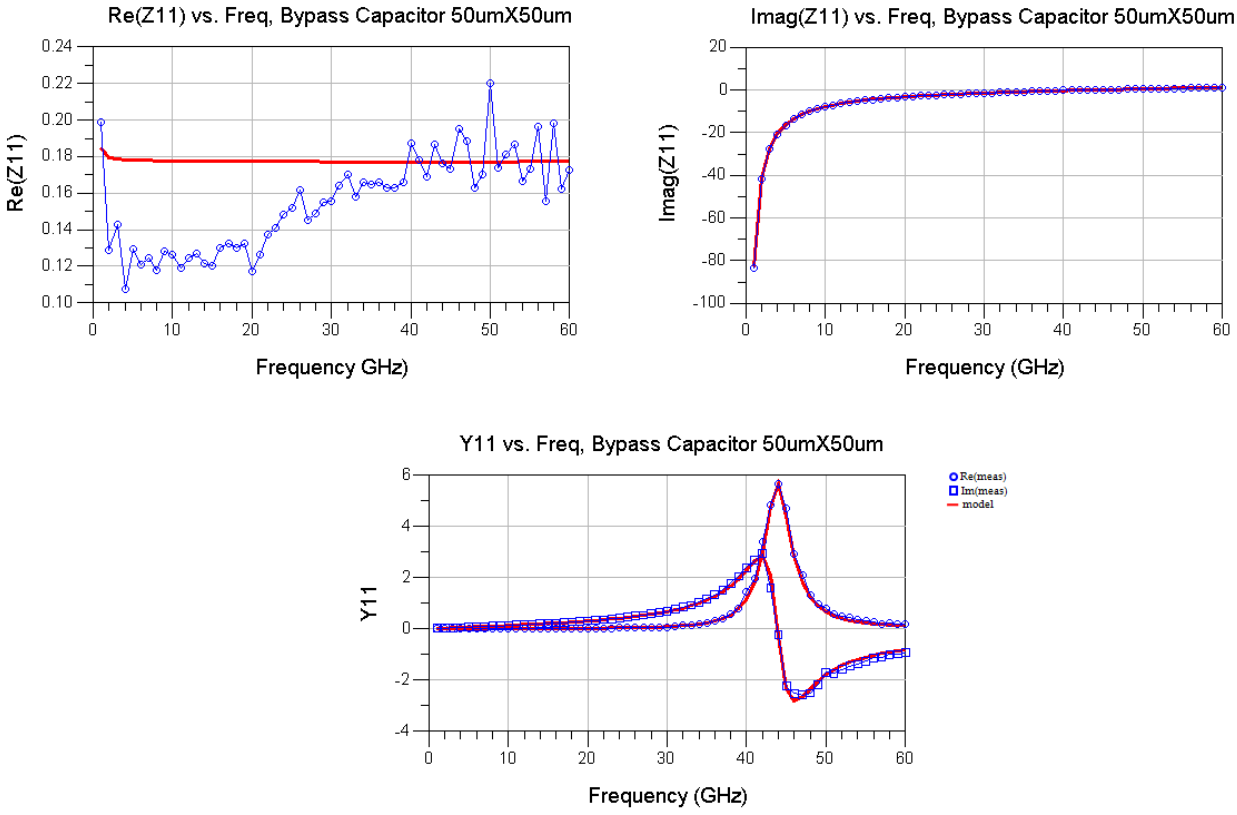

Figure 4.30: Z and Y-parameters (derived from S-parameters) measurement vs. model for the 50µmX50µm supply-ground bypass metal multi-finger capacitor

4.3 RF Ground-Signal-Ground Pad Modeling

The 60 GHz signals are injected into the circuit through RF Ground-Signal-Ground pads whose die photo is shown in Figure 4.31. Typically, the pads are treated as part of the design, i.e. pad losses are not de-embedded from the measurement results of amplifiers. Thus, they are treated as parts of the input and output matching networks, and therefore, modeling them accurately is of significant importance.

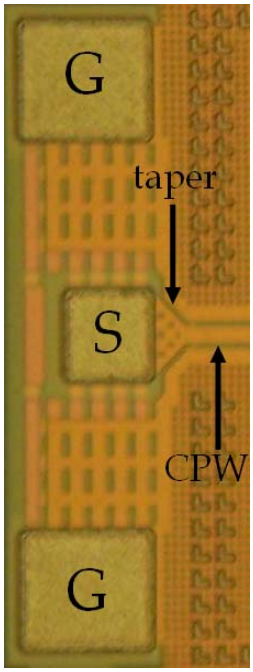

Figure 4.31: RF Ground-Signal-Ground pad die photo

4.3.1 RF Ground-Signal-Ground pad geometry

The pad exhibits a ground shield situated on the first metal layer that limits the penetration of the electric field into the substrate. In order to reduce the pad parasitics and thus the pad losses, the signal pad side is reduced to only 55 μm, the minimum dimensions required for probing. Moreover, the signal pad is composed of the top metal

layer only which reduces its parasitic capacitance. On the other hand, the ground pads are made larger in order to make probing easier, and they are composed of all metal layers. The pad connects to the rest of the circuitry through a 3 μm gap, 40 μm long coplanar transmission line. In order to reduce the discontinuity between the pad and the transmission line and therefore reduce the signal reflections at the pad – transmission line interface, a small 45^{o} taper is added in between.

4.3.2 RF Ground-Signal-Ground Pad Modeling

The circuit shown in Figure 4.32 is used to model the RF Ground-Signal-Ground pad.

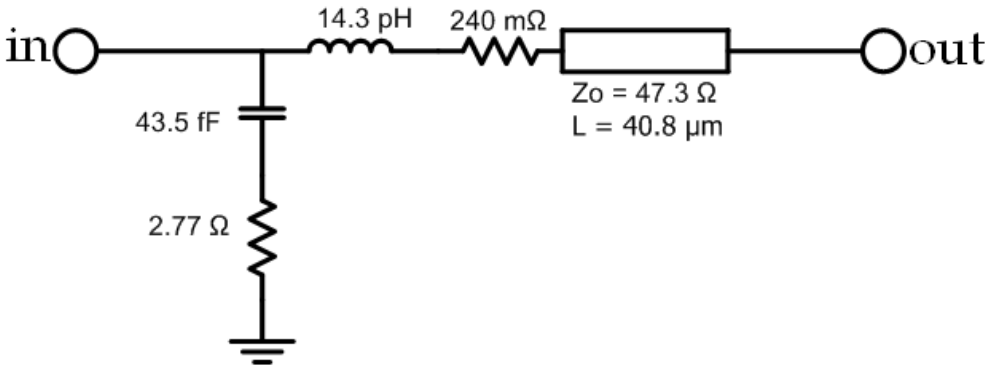

Figure 4.32: RF Ground-Signal-Ground pad model

The capacitor, inductor, and resistors values are optimized to obtain a simultaneous Z and Y - parameters fit as is the case for the capacitors modeling discussed in section 4.2, whereas the ADS transmission line model previously discussed in section 4.1.5 is used to model the 3 μm gap, 40 μm long coplanar transmission line. Figure 4.33 and Figure 4.34 show the measured vs. simulated Z and Y – parameters fit.

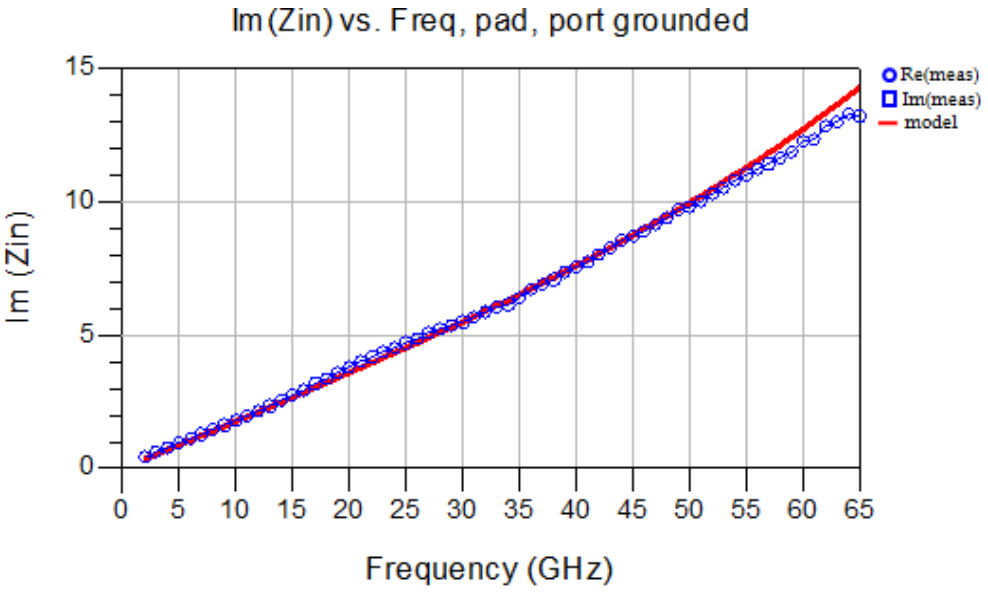

Figure 4.33: Im(Zin) (derived from S-parameters) measurement vs. model results for the Ground-Signal-Ground RF pad with port2 grounded

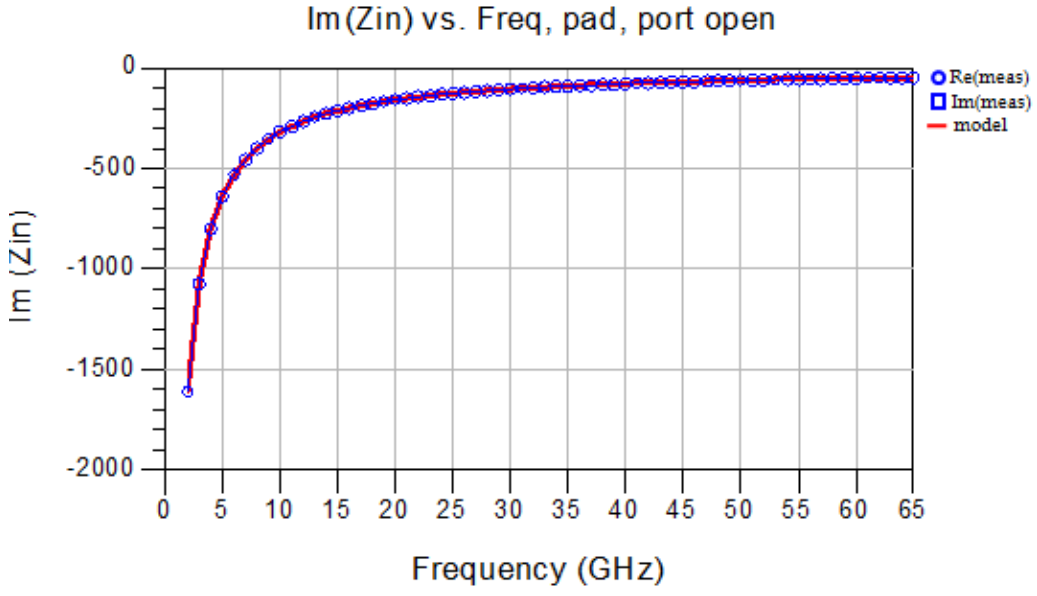

Figure 4.34: Im(Zin) (derived from S-parameters) measurement vs. model results for the Ground-Signal-Ground RF pad with port2 open

4.4 Conclusion

In this chapter, the design, optimization, and modeling of mm-wave passive structures such as transmission lines, capacitors, and RF pads are discussed in detail.

A library of transmission lines of different geometries is built, measured, and modeled using both ADS and HFSS. High density metal multi-finger capacitors employing all metal layers are used for both AC coupling and supply - ground bypass. A library of capacitors is built, measured, and modeled with custom Π models. As RF Ground-Signal-Ground pads are considered part of the amplifiers design and thus not de-embedded, the structure is optimized and modeled as well.

As this modeling methodology scales well with technology scaling if the same materials are used, once the passive structures of a specific technology node are modeled, few modifications are needed when scaling to smaller nodes.

CHAPTER 5

ACTIVE DEVICES

DESGIN AND MODELING

5 Active Devices Design and Modeling

90 nm standard CMOS processes provide f_T values around 130 GHz and f_{max} values in the order of 200 GHz if the transistors are carefully laid out. When operating the transistors at 60 GHz, as the frequency of operation approaches a substantial fraction of f_T and f_{max}, the transistors provide maximum stable power gain figures of just a few dBs (6 – 7 dB). In such a scenario, it becomes very important to obtain accurate transistor models since any substantial difference between actual and simulated performance can result in circuit failure. Moreover, at mm-wave frequencies, the device layout parasitics have a significant impact on its performance. Thus, careful design and layout are necessary to push the performance limits of the active devices. Optimization of transistors layout is discussed in section 5.1 and active devices small signal and large signal modeling are discussed in sections 5.2 and 5.3 respectively.

5.1 Transistors Design and Layout

The transistor unity f_T and f_{max} are the two most common and important metrics used to measure transistor speed characteristics. They can be related to the transistor intrinsic and extrinsic parameters through equations (2.4) and (2.5). From equation (2.4) it is shown that the transistor f_T is dependant only on the its intrinsic parameters. Circuit designers don't have control over these parameters and have to work with the transistors at hand. On the other hand, equation (2.5) shows that the transistor f_{max} is dependent on

f_T as well as on the extrinsic resistive networks at the transistor gate and source. These resistances depend on how the transistor gate and source networks are laid out. Careful layout can have a major effect on the value of f_{max}. For instance, f_{max} variation from 80 GHz to 280 GHz due to layout differences in the same CMOS 90 nm process was reported [39, 40]. As transistors in amplifiers are used to provide power gain rather than current gain, much effort is spent in improving the transistor f_{max}. It will be shown that with careful layout, a transistor f_{max} can practically approach three times its f_T value.

The common-source configuration transistor layout shown in Figure 5.1 has been used in all the 60 GHz amplifiers implemented in this work and presented in chapter 7.

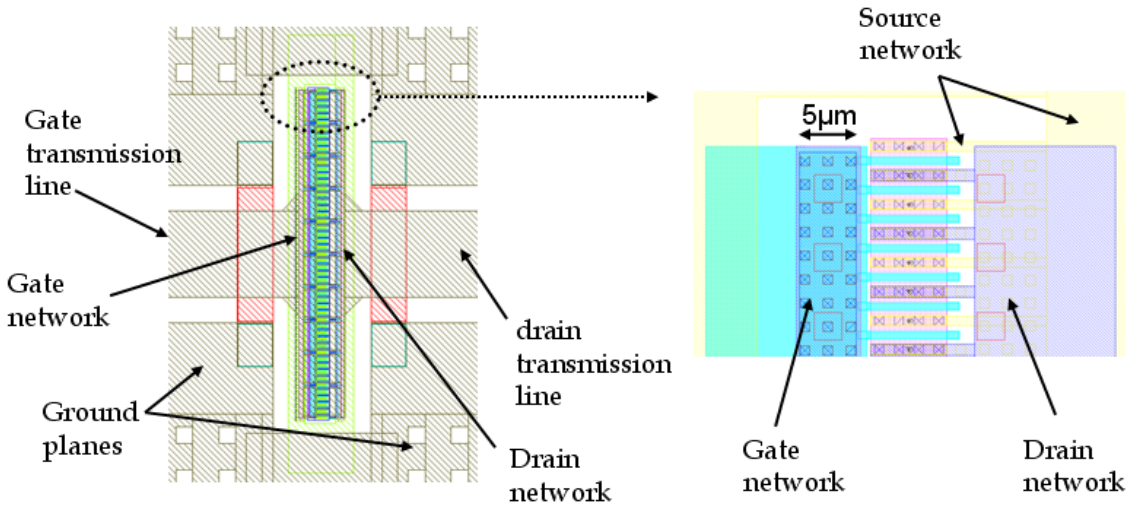

Figure 5.1: Layout for the 80 fingers, 1µm/finger, 90nm NMOS device in common-source configuration

As is shown in Figure 2.2, the transistor f_{max} drops significantly as its finger width increases beyond a threshold slightly above 1 µm. Thus, all transistors used employ a finger width of 1 µm. As shown in Figure 5.1, a multi-finger structure is used in order to

increase the effective transistor size. The gate and drain networks are composed of 5 µm wide vertical multi-layer metal slabs with ample vias in order to minimize the gate and drain extrinsic resistances and inductances. Increasing the gate and drain networks sizes excessively would increase their associated capacitances. A source network situated in the lowest metal layer picks up all the fingers sources and connects them to the two top and bottom ground planes. The transistor gate and drain connect to the circuit through 10 µm wide coplanar transmission lines. These transmission lines are not considered part of the transistor model. This structure provides measured MSG of 7.6 dB and f_{max} of 176 GHz. Note that because the measurement has been performed up to 100 GHz only, the Mason's unilateral gain was extrapolated in order to extract the f_{max} value. The measured MSG and Mason's unilateral gain results are shown in Figure 5.2.

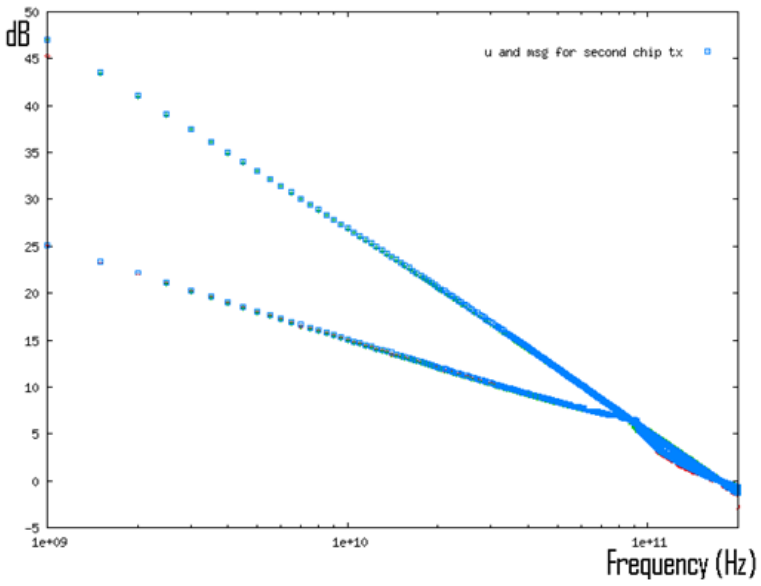

Figure 5.2: Measured Mason's gain and MSG of the 80 fingers, 1µm/finger, 90nm NMOS device in common-source configuration

Mason's unilateral gain can be written in terms of the two-port device Y-paramerters as [41]

$$U = \frac{1}{4}\frac{|y_{21}-y_{12}|^2}{g_{11}g_{22} - g_{12}g_{21}} \quad \textbf{(5.1)}$$

where $g_{ij} = Re(y_{ij})$. The device becomes passive when $U = 1$, the frequency at which f_{max} is reported. Since f_{max} is in this case, as is often the case, beyond the frequency capability of the measurement equipment, it is derived from the extrapolation of Mason's unilateral gain assuming a 20 dB / decade slope.

A previous sub-optimal version of the layout shown in Figure 5.3 was implemented. The sub-optimal layout suffers from bulky gate and drain tapers as well as a narrow 2 μm wide gate and drain networks with small number of vias and poly contacts. This results in large gate and drain resistances. The layout is shown in Figure 5.3. Not surprisingly, this layout measured an $f_{\max}$ of only 143 GHz. However, since the device is conditionally stable at 60 GHz, reducing its gate and drain resistance does not alter its 60 GHz MSG of 7.6 dB.

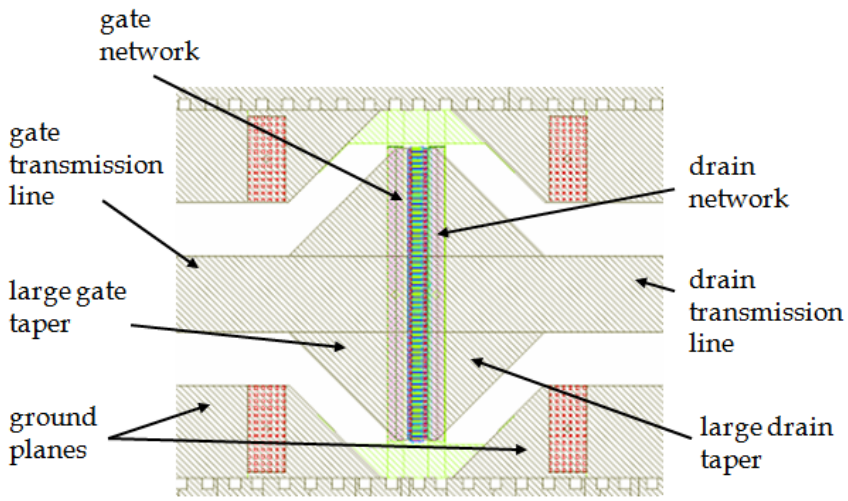

Figure 5.3: Initial bulky layout for the 80 fingers, 1µm/finger, 90nm NMOS device in common-source configuration

5.2 Transistors Small Signal Modeling

Compact models [42, 45] that use combination of physical and empirical methods to develop general equations to describe the transistor behavior are usually used in circuit simulations. Most compact models have the advantage of describing the device behavior in all regions of operation with small and large signal excitations. These models also operate over a large range of device geometry, accurately capturing the behavior of transistors with different width and gate lengths. However, compact models that ship with standard CMOS processes are usually optimized to accurately model transistor behavior up to frequencies around 20 GHz. Moreover, these models pertain only to the intrinsic device, i.e. the bare transistor without its gate, drain, and source networks that are used to connect its ports to the rest of the circuit. Eventually, when used in a circuit, the gate and drain connections would add parasitic resistances, capacitances, and inductances around

the transistor ports. These parasitics are insignificant at low frequencies and can be ignored without much performance penalty. However, they significantly modify, and potentially can dominate, the transistor behavior at mm-wave frequencies. Therefore, these connections should be considered part of the transistor and modeled as well.

One solution is to bypass the entire modeling process and work directly with measured S-parameter data, thus treating the transistor as a black box. While this approach leads to accurate results since the measured data account for all parasitics and distributed effects, it is suitable only for small signal simulations. It is not suitable for power amplifiers exhibiting large signal swings.

The active device modeling approach preferred at mm-wave frequencies requires measuring the small signal S-parameters of a given transistor at a given bias point then optimizing the parameters values of the custom designed model shown in Figure 5.4 in order to fit the measured and simulated S-parameters [46, 47].

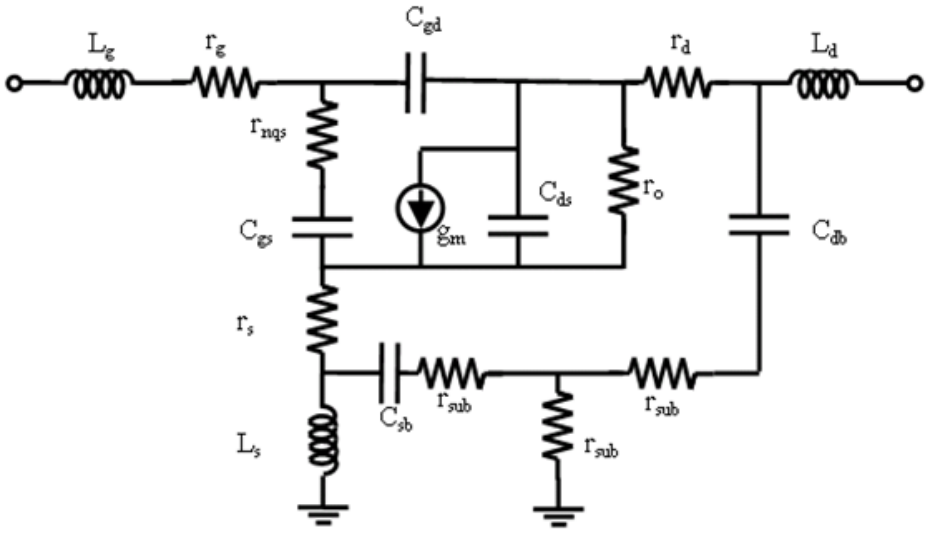

Figure 5.4: CMOS transistor custom mm-wave bias dependant small signal model [46, 47]

The elements $g_m, r_o, r_{nqs}, C_{gs}, C_{gd}, r_d$, and C_{ds} form the well known hybrid-Π model to model the intrinsic core part of the transistor, while the gate network is captured by r_g and L_g and the drain network is formed by r_d, C_{db} and L_d. The source network is modeled by r_s, C_{sb} and L_s. The three resistors termed r_{sub} form the substrate network. While this model provides very accurate results shown in the excellent fit between the measured and simulated S-parameters in Figure 5.5, it has two main drawbacks. First, it is layout specific, i.e. its parameter values are not function of the transistor geometry and thus it does not scale with the gate width or number of finger. Thus, each transistor geometry that is to be used in amplifier design has to be fabricated, measured, and modeled. In order to alleviate this problem, a large library of different transistor sizes as show in section 3.3 has been fabricated. The other disadvantage of this modeling approach is that the resulting model is bias dependant since it is optimized to fit given S-parameters measured at a given bias point. This makes the model not suitable for large signal simulations where voltages across the gate and drain can vary substantially. A different large signal modeling approach is used for large signal simulations and is discussed in section 5.3.

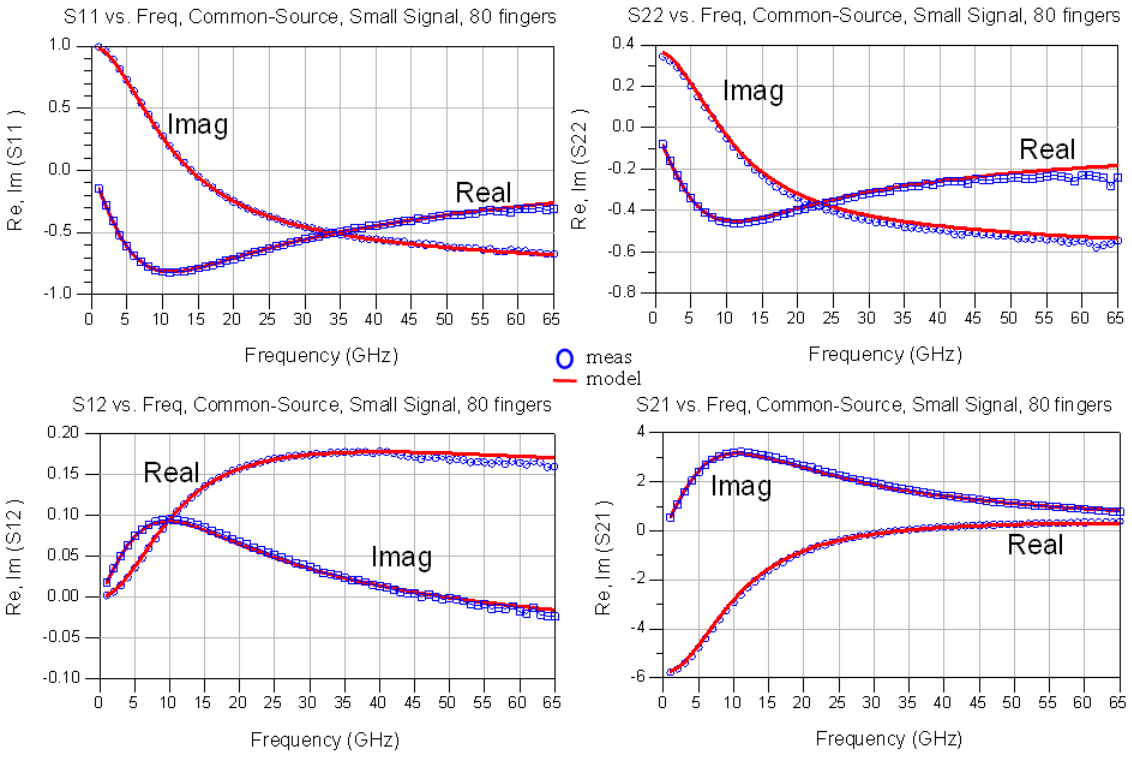

Figure 5.5: Measurement vs. model S-parameters for the 80 fingers, 1 µm per finger NMOS device in common-source configuration with I_{DS} = 16 mA [46]

5.3 Transistors Large Signal Modeling

Large signal models need to capture the device bias dependency because they exhibit large signal swings. In that order, the BSIM3V3 [42] model can be used. BSIM3V3 only models the core intrinsic transistor parameters. The extrinsic gate, drain, and source networks that add substantial parasitics still need to be modeled. In order to obtain a bias dependent mm-wave transistor model, the modeling approach followed in [48] was used where the intrinsic transistor is modeled using the BSIM3V3 model, and

the extrinsic gate, drain, and source networks are modeled with additional resistors, capacitors, and inductors as shown in Figure 5.6. A modified substrate network is used as well. The transistor S-parameters were measured over a wide range of bias values, and the extrinsic elements parameter values were optimized to fit the measured and simulated S-parameters over the different bias points simultaneously.

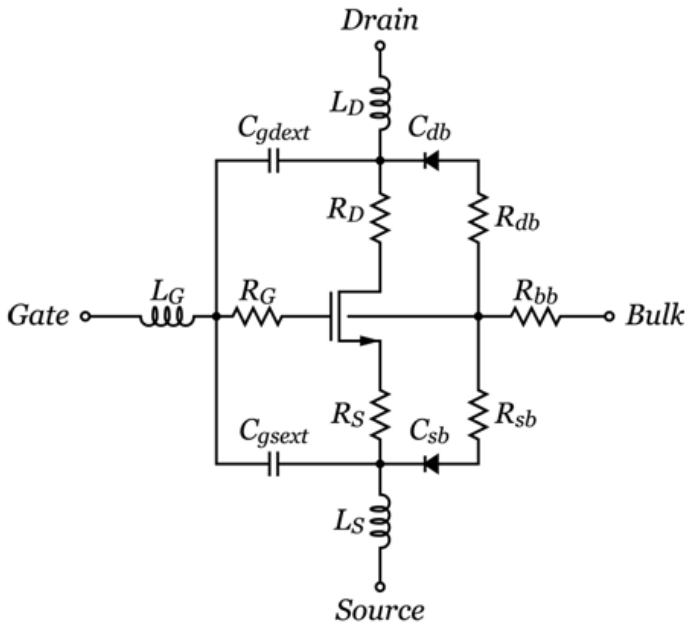

Figure 5.6: mm-wave large signal transistor model [48]

5.4 Conclusion

Current CMOS transistors operating at mm-wave frequencies provide low gain figures and thus modeling their behavior accurately is necessary. Careful design and layout are required to push the performance limits of the active devices as device layout parasitics have a significant impact on performance. Multi-finger transistor layouts with

small tapered gate and drain networks proved to provide optimum performance. Custom small signal and large signal models were developed.

As technology scales, CMOS transistors will be capable of providing larger gain figures at mm-wave frequencies, and thus a large modeling error margin can be tolerated. Readily available transistor models that ship with the processes could be used, significantly reducing the modeling effort required. This would also free the designer from the limitation of using only transistor geometries that have been built and measured.

CHAPTER 6

MODELING VERIFICATION

6 Modeling Verification

In the passive structures and active devices modeling methodology followed in chapters 4 and 5 all elements were modeled in a stand-alone fashion. Each element was fabricated in its own test structure and modeled in the absence of other elements in its surrounding. For example, single transmission lines and single transistors connected only to de-embedded RF pads were fabricated and modeled. However, in actual amplifiers, these elements are connected to different structures and are surrounded by a different environment. Long transmission lines might be bent to accommodate a given layout. Transmission lines of different gap spacing might need to be connected to each other causing discontinuities at the connection. Large parasitic junctions are formed when three or four elements are connected together at the same connection node. Transistors might be surrounded by other transmission lines and coupling capacitors. In power amplifiers employing power combining, entire unit amplifiers might be placed in close proximity so that their output power can be combined into a single node. In order to verify the validity of the passive structures and actives devices modeling methodology followed in chapters 4 and 5 once the elements are used in more complex circuits, two circuits of moderate complexity were implemented and their measurement and simulated performance compared. First, a Wilkinson power combiner was used to verify the modeling of transmission lines and RF Ground-Signal-Ground pads and is presented in section 6.1. Second, a one-stage amplifier employing all the elements modeled in chapters 4 and 5

was fabricated, and its measured and simulated results compared as presented in section 6.2.

6.1 Wilkinson Power Combiner

A Wilkinson power combiner whose schematic is shown in Figure 6.1 was fabricated in order to verify the modeling of transmission lines and RF Ground-Signal-Ground pads.

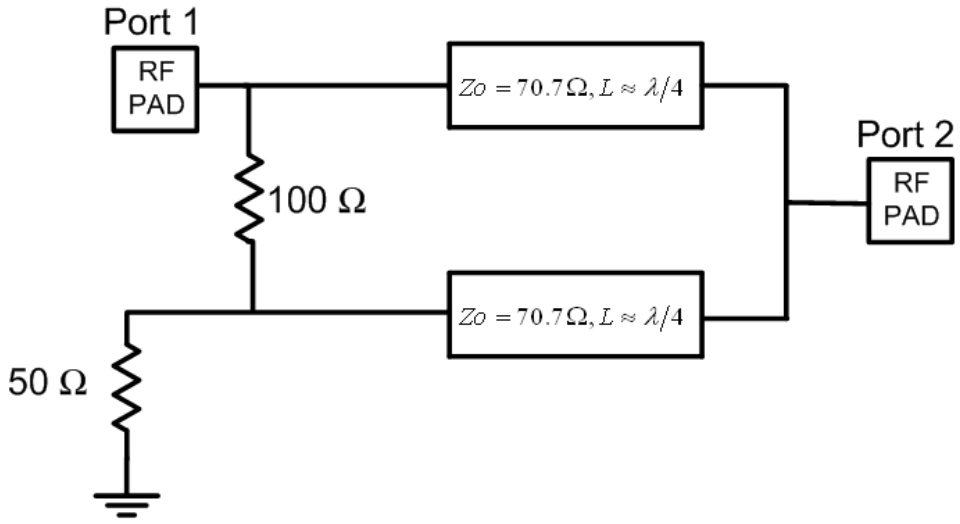

Figure 6.1: Schematic of Wilkinson power combiner

Since the measurement equipment capability is limited to two-port measurements, the Wilkinson power combiner is treated as a two-port network with the third port terminated by an on-chip 50 Ω resistor. The RF pads are considered part of the design and thus are not de-embedded from the measurements. The transmission lines length was adjusted in order to obtain a 50 Ω match at the input and output ports in the presence of the RF pads. HFSS was used to design the transmission lines with characteristic impedance of 70.7 Ω.

The 50 Ω and 100 Ω resistors employ silicided polysilicon. A die photo of the Wilkinson power combiner is shown in Figure 6.2.

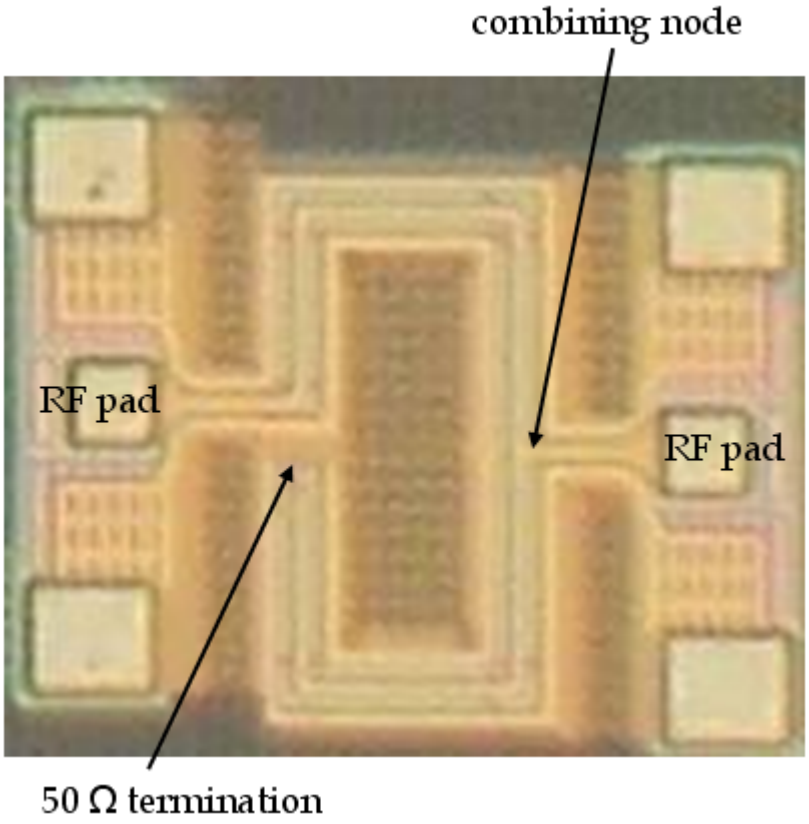

Figure 6.2: Layout of Wilkinson power combiner

The two long transmission lines that form the combiner meet with the RF output pad transmission line at the combining node forming 90^{o} angles. It was later found that this causes current crowding resulting in additional power loss. 45^{o} junctions were found to result in considerably lower loss. All power combiners and splitters employed in the power amplifiers presented in chapter 7 employ 45^{o} junctions.

Because the structure uses custom transmission lines, HFSS was used for simulation. This also allows for better modeling of the junction formed at the combining node at the output port where both transmission lines meet. The HFSS drawing of the Wilkinson power combiner is shown in Figure 6.3. The HFSS simplified substrate stack described in section 4.1.6 and the RF pad model described in section 4.3 were used.

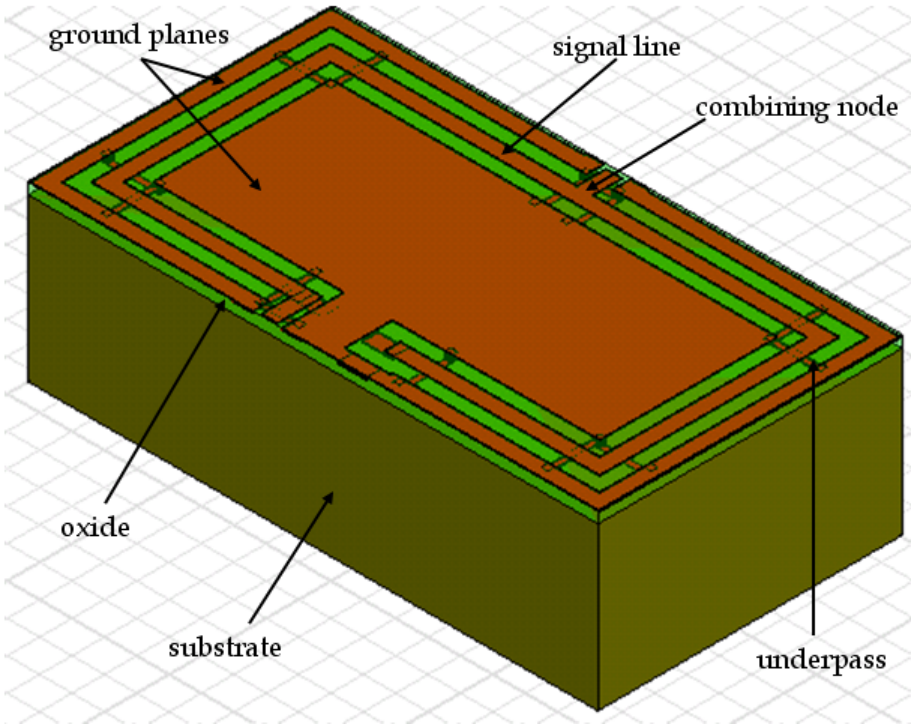

Figure 6.3: Drawing of the Wilkinson power combiner in HFSS

An excellent match between measurement and simulation results is obtained, as shown in the measured and simulated S-parameters in Figure 6.4. The measured S_{21} at 60 GHz is -4.03 dB compared to a simulated value of -4.1 dB. This puts the insertion loss of

the Wilkinson power combiner at about 1dB since an ideal lossless combiner exhibits S_{21} of -3 dB.

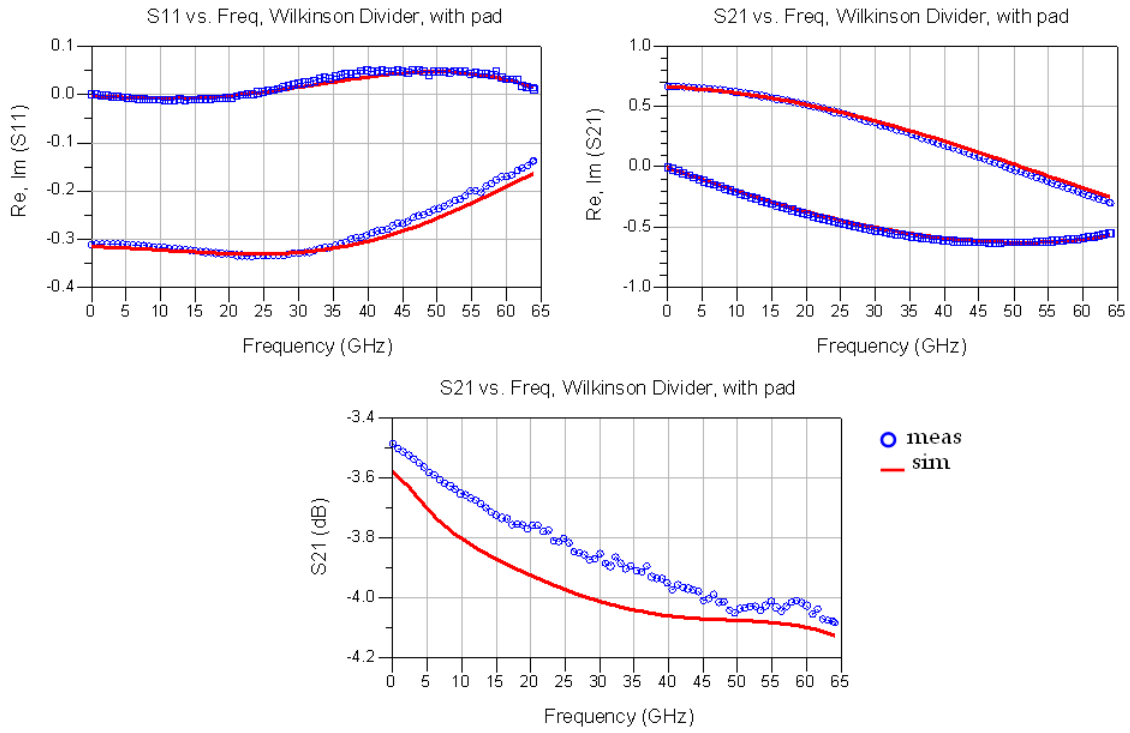

Figure 6.4: Measurement and simulation S-parameters results for a 60 GHz Wilkinson power combiner

6.2 One-Stage Amplifier

The 60 GHz one-stage amplifier whose schematic and die photo are shown in Figure 6.5 and Figure 6.6 employing all the elements modeled in chapters 4 and 5 was fabricated, and its measured and simulated results were compared in order to verify the modeling methodology followed. The amplifier uses the 80 fingers, 1 μm per finger NMOS transistor in a common-source configuration employing the layout described in section 5.1. The AC coupling and supply-ground bypass metal multi-finger capacitors

described in section 4.2 are used as well as the RF Ground-Signal-Ground pads modeled in section 4.3. The input is matched to 50 Ω. In order to attenuate the low frequency gain, a two stage input matching network with the first stage exhibiting a shunt transmission line connected to ground is used. At low frequencies, the grounded transmission line presents low impedance to ground shunting the input signal, whereas it presents high impedance at higher frequencies. The RF pads are considered part of the design, and thus their loss is not de-embedded from the measurement results. The gate and drain bias voltages are supplied to the circuit through transmission lines in the input and output matching networks. The junctions formed when three transmission lines are connected together are modeled as three-port networks in HFSS.

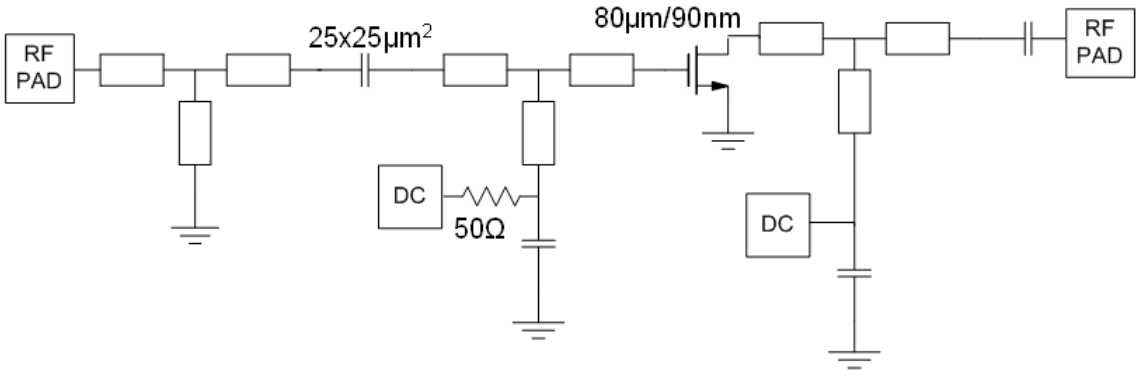

Figure 6.5: Schematic diagram of one-stage 60 GHz amplifier

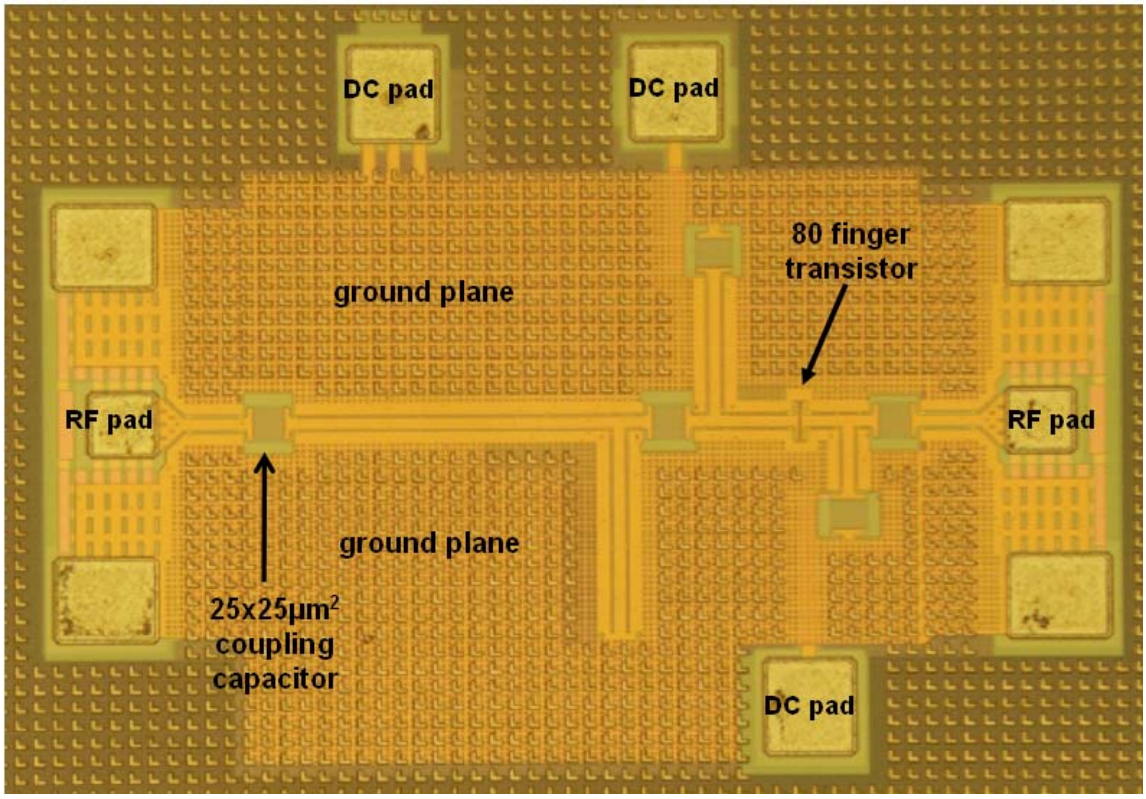

Figure 6.6: Die photo of one-stage 60 GHz amplifier

A good agreement is obtained between the measured and simulated results over the broad frequency range of 0-65 GHz, verifying the validity of the modeling approach followed. The measured and simulated S-parameters are shown in Figure 6.7. The amplifier achieves a measured peak S_{21} of 5.5 dB while the simulated value is 5.2 dB. The measured and simulated peak S11 are -22 dB and -14 dB respectively.

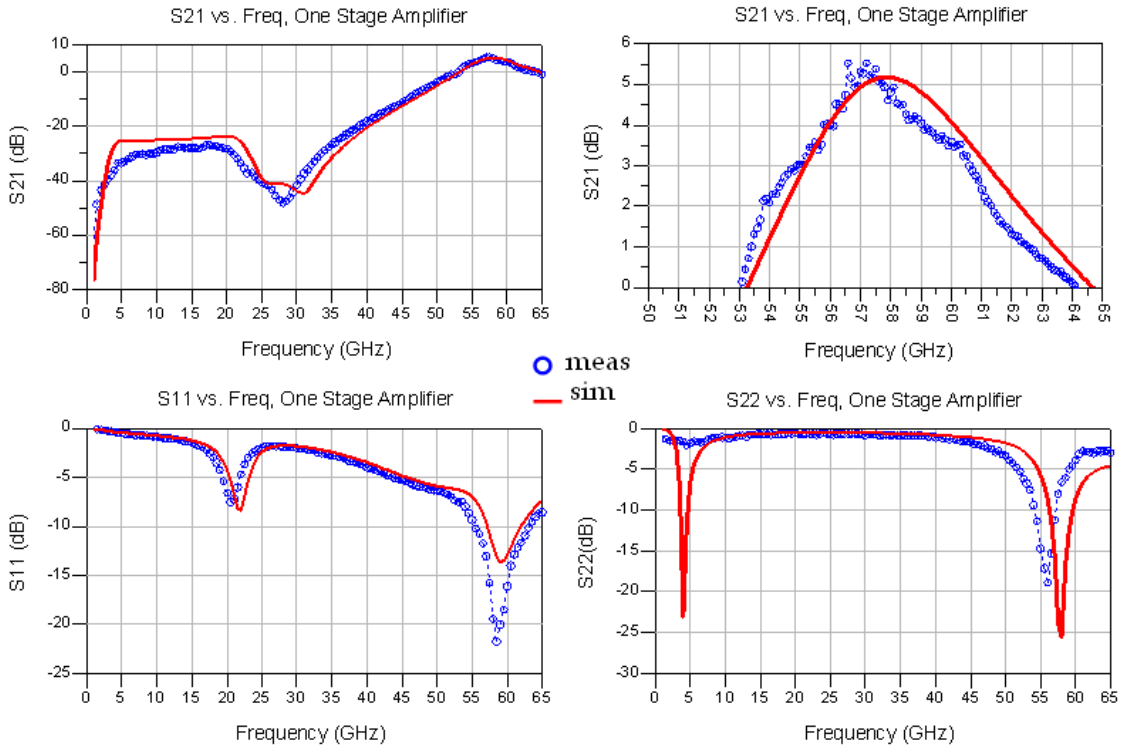

Figure 6.7: Measurement and simulation S-parameters of one-stage 60 GHz amplifier

CHAPTER 7

POWER AMPLIFIERS

7 Power Amplifiers

Four prototype power amplifiers are implemented in ST Microelectronics' 90 nm 1V standard CMOS process. Instead of using separate power splitters and combiners to split and combine the power to and from the unit amplifiers, the amplifiers incorporate the power splitters and combiners into their input and output matching networks following the scheme described in section 2.4.3. Combining the output power from four unit amplifiers, the four-way power amplifier presented in section 7.1 provides record performance in terms of 1dB compression and saturation output power. The first of the three two-way power amplifiers exhibits high gain with high output power while the second provides lower gain but higher stability margin. The fourth power amplifier uses inductive source degeneration for linearization. The two-way amplifiers are presented in sections 7.2, 7.3, and 7.4.

7.1 Four-Way Power Amplifier

A four-way 60 GHz power amplifier has been designed and fabricated in ST Microelectronics' standard 90 nm CMOS process. Instead of using separate power splitters and power combiners to split and combiner the power to and from the four unit amplifiers, the amplifier uses the scheme described in section 2.4.3 in order to incorporate the power splitter and combiner into its input and output matching networks. The power amplifier provides 4.2 dB of power gain and achieves a saturation output power of +14.2 dBm and a 1dB compression output power of +12.1 dBm. It consumes

145 mW from a 1V power supply leading to saturation efficiency of 18.1%, 1dB compression efficiency of 11.2%, and peak power added efficiency of 5.8%.

7.1.1 Circuit Description

The circuit diagram of the four-way power amplifier showing the overall amplifier topology and the unit amplifier schematic is shown in Figure 7.1.

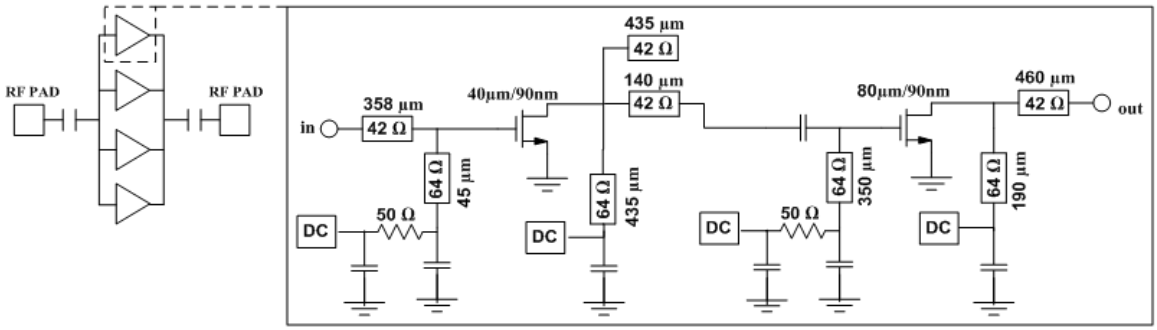

Figure 7.1: Schematic diagram of the 4-way 60 GHz power amplifier

The power amplifier consists of four identical unit amplifiers along with the power splitting and combining scheme described in section 2.4.3. The input matching network is designed such that a long series transmission line is presented at the unit amplifier input. This allows using the power splitting and combining scheme described in section 2.4.3 which results in higher output power levels and higher power efficiency. Thus, the 358 µm long transmission lines at the four unit amplifiers inputs are routed to feed a common splitting node and the 460 µm long transmission lines at the four unit amplifiers outputs are routed to feed a common combining node to realize the power splitting and combining functions respectively. In this fashion, no external power splitter or combiner is added to the power amplifier, and thus no additional power loss is introduced.

Each unit amplifier consists of two conditionally stable common-source stages. The first and second stages use 40 μm and 80 μm (1μm/finger) transistors respectively. The second stage transistor is made twice as large as the first stage transistor in order to insure that the output transistor enters compression first. The transistors layouts are implemented using the multi-finger structure described in section 5.1 and shown in Figure 5.1. The transistors have f_{max} and f_T of 176 GHz and 100 GHz respectively and MSG of 7.6 dB when biased at a current density of 1.2mA/μm. The output stage consumes 24 mA of current whereas the driver input stage consumes 12.4 mA, both from a 1V power supply. All matching networks have been realized using coplanar transmission lines. The series transmission lines use the top metal (M7) only and have a 2 μm gap between the signal line and the ground planes with characteristic impedance Z_o of 42 Ω. On the other hand, the inductive short-terminated lines are realized with coplanar transmission lines that reside in the top metal layer (M7) but employ a higher gap of 9 μm between the signal line and the ground planes and thus have a higher Zo of 69 Ω. This results in a higher inductive quality factor. The Ground-Signal-Ground pads are incorporated as part of the input and output matching networks and thus their losses is not de-embedded. Custom designed metal finger capacitors described in section 4.2 are used for AC coupling and DC bypass. They possess a low frequency capacitance of 1pF, but are designed to have a series resonance close to 60 GHz where they present low impedance and serve as short circuits. Large MOS capacitors are used for low frequency bypass in order to insure low frequency stability. The DC voltages are provided to the gates and drains of all transistors through the transmission lines of the matching

networks. The gate bias networks are de-Q'ed using series 50 Ω resistors in order to suppress potential instability at low frequencies.

In order to realize high output power, the output matching networks along with the power combining node are designed to convert the 50 Ω load at the power amplifier output into the optimum power impedances seen at the drain of the second stage 80 μm transistor. Note that the output transistor gain would drop significantly if it were to drive a 50 Ω load. A compromise is made between gain and output power when selecting the optimum load impedance. An inter-stage matching network is also introduced between the driver stage and the output stage in order to insure maximum power transfer between the stages as well as the stability of each stage. The input matching networks along with the power splitting node provide a 50 Ω input match. Even though all transistors are conditionally stable, the impedances seen by each amplifier are chosen such as to insure stable operation.

The chip micrograph of the four-way amplifier is shown in Figure 7.2. It measures 1300x920 μm^2.

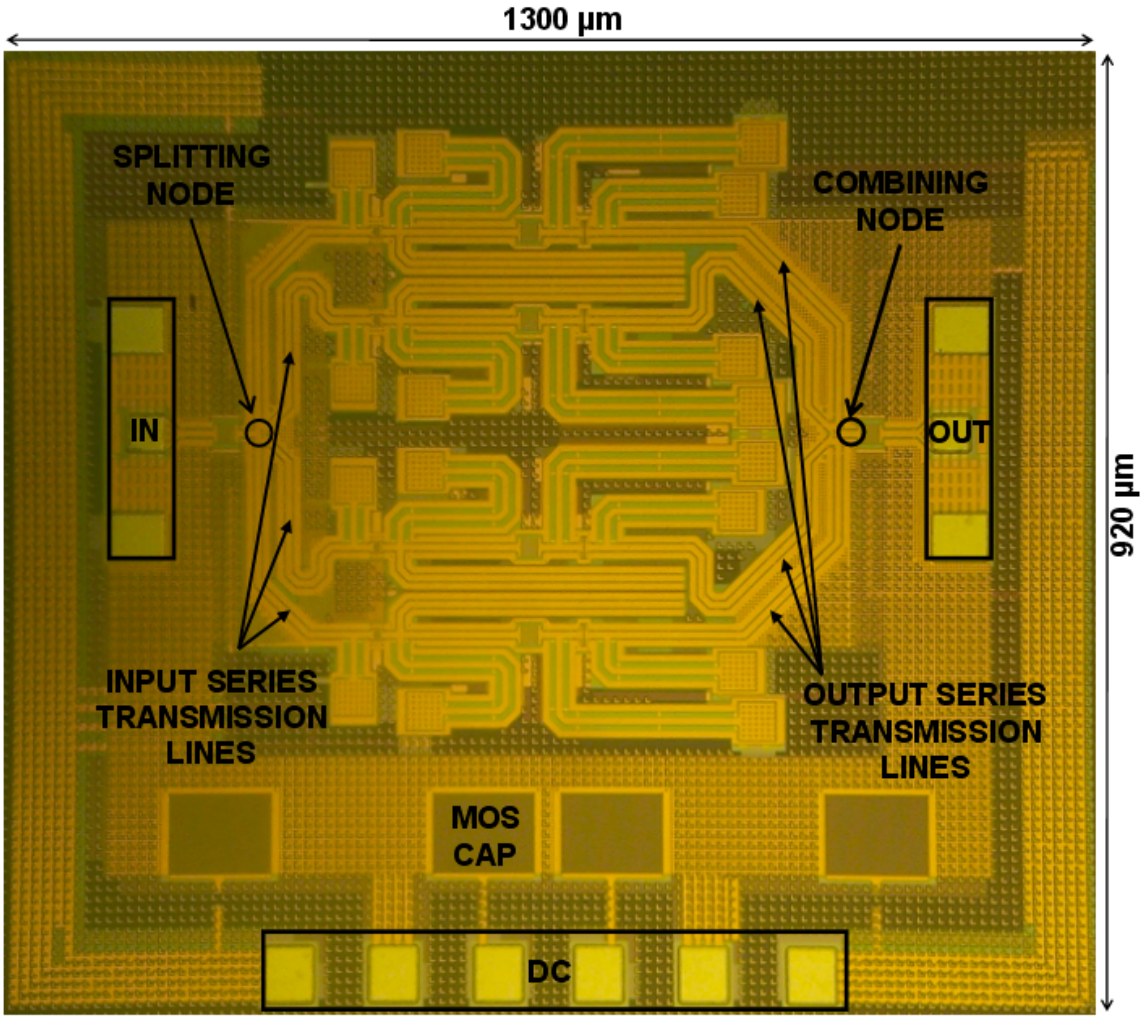

Figure 7.2: Chip micrograph of the 4-way 60 GHz power amplifier

7.1.2 Measurement and Simulation Results

S-parameter measurement and simulation results are shown in Figure 7.3 to Figure 7.8. The power amplifier provides a measured peak S_{21} of 4.4 dB at 58 GHz compared to a simulated S_{21} of 6.3 dB. The S_{21} 3-dB bandwidth is 9 GHz centered around 58 GHz. The measured S_{21} is about 1.5 dB lower than the simulated value over the range of 50 GHz to 65 GHz. A gain peaking behavior is observed around 27 GHz. However, the

amplifier stability is preserved as S_{21}, S_{11}, and S_{22} stay below 0 dB, and the stability factor K stay above 4 over the entire frequency range. As the input is matched to 50 Ω impedance, it provides a peak measured S_{11} of -10 dB at 58 GHz. S_{12} is better than -25 dB over the entire frequency range.

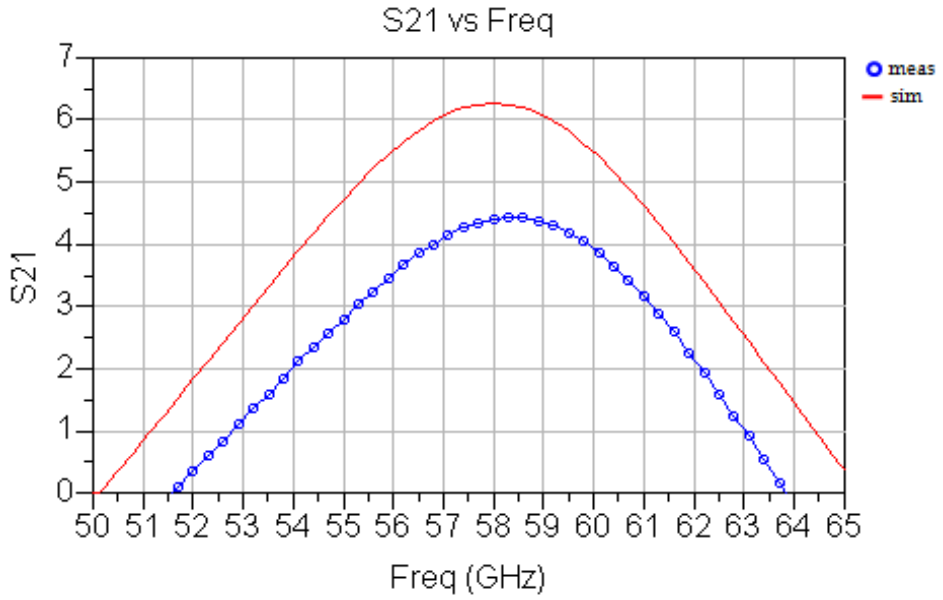

Figure 7.3: S21 measurement vs. simulation of the four-way 60 GHz power amplifier

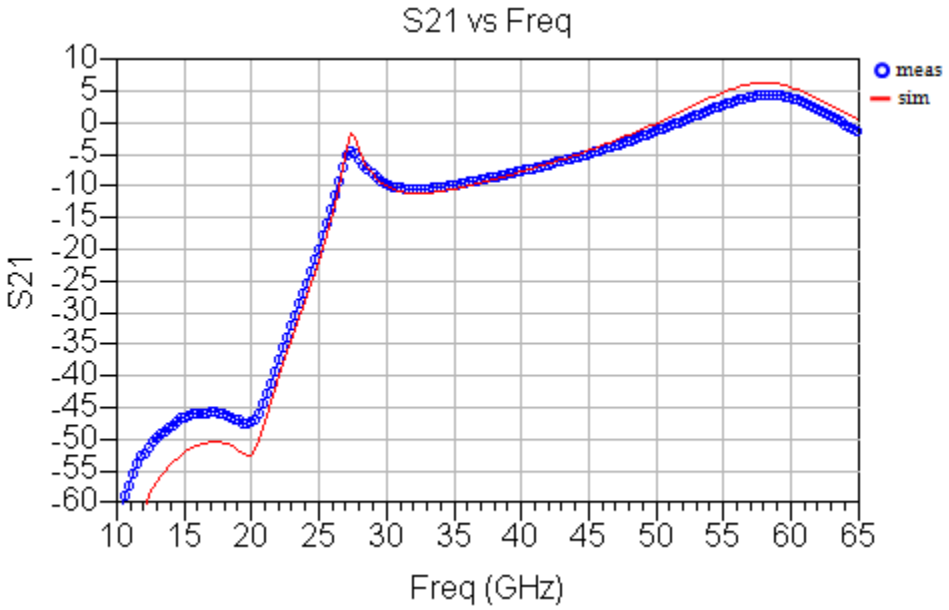

Figure 7.4: S21 measurement vs. simulation of the four-way 60 GHz power amplifier

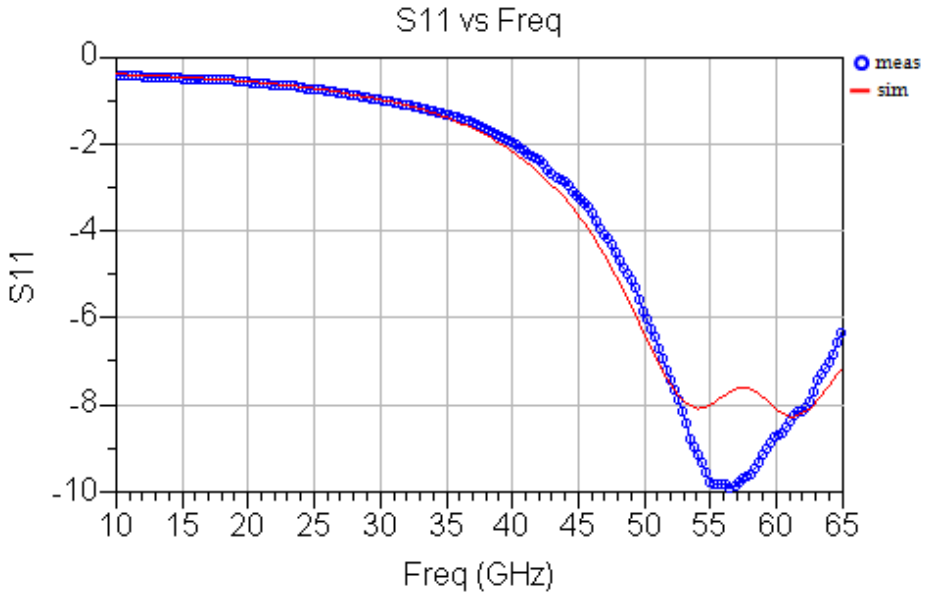

Figure 7.5: S11 measurement vs. simulation of the four-way 60 GHz power amplifier

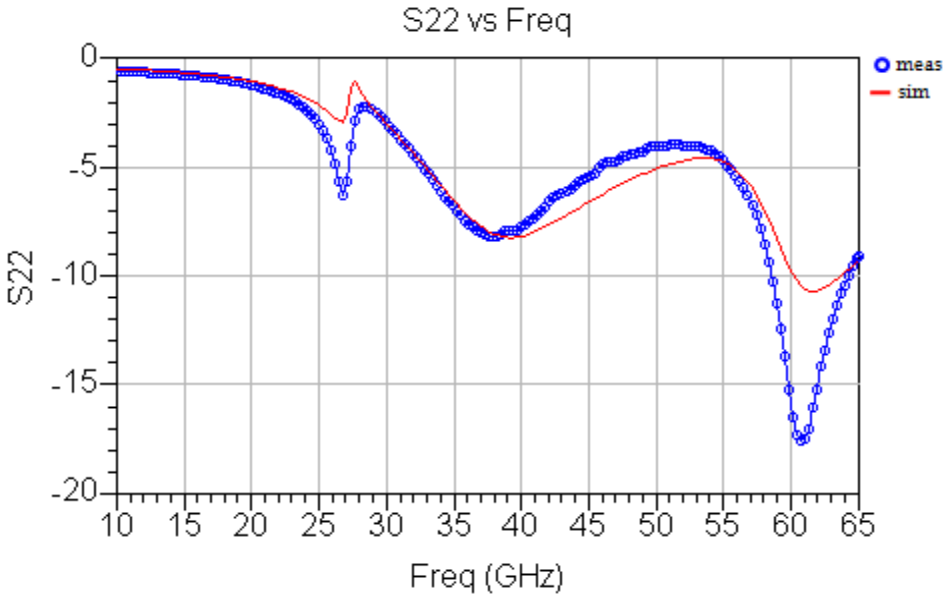

Figure 7.6: S22 measurement vs. simulation of the four-way 60 GHz power amplifier

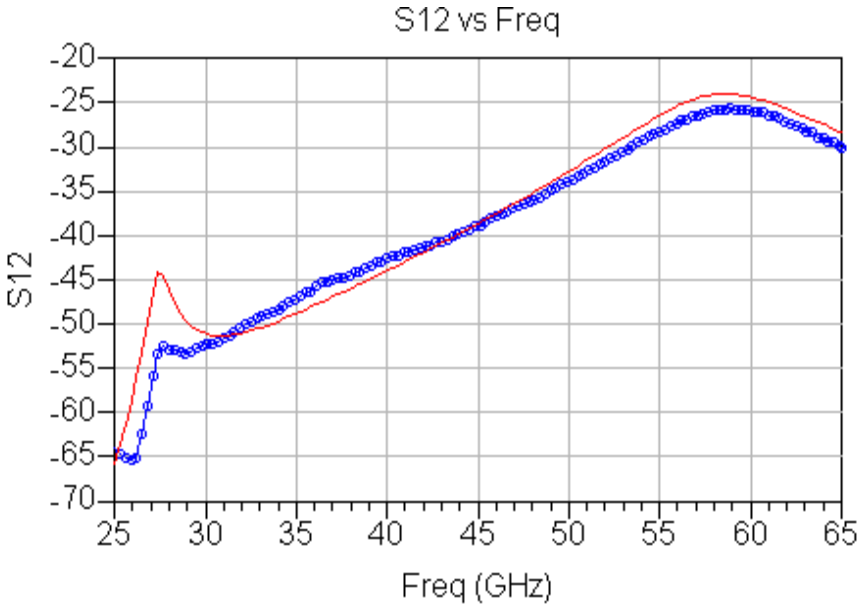

Figure 7.7: S12 measurement vs. simulation of the four-way 60 GHz power amplifier

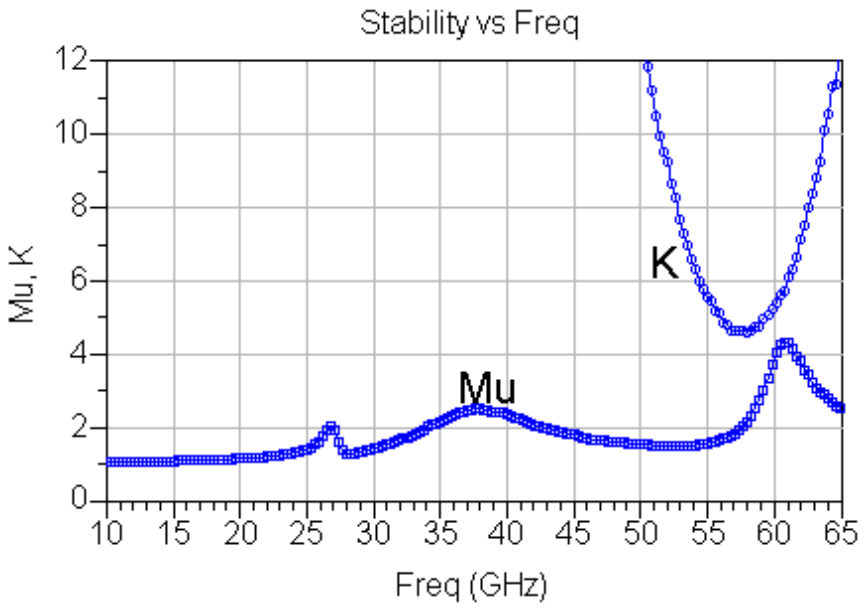

Figure 7.8: Stability factor (K) and μ factor measurement vs. simulation of the four-way 60 GHz power amplifier

Power measurement and simulation results are shown in Figure 7.9 to Figure 7.12. The power amplifier delivers a 1dB compression and saturation output powers of +12.1 dBm and +14.2 dBm respectively, the highest reported to date, with a 1dB compression and saturation efficiencies of 11.2% and 18.1% respectively. The peak measured power added efficiency is 5.8% partly due to the low gain. The amplifier consumes 145 mW from a 1V power supply. The linear behavior between the input and output power levels indicates amplifier stability.

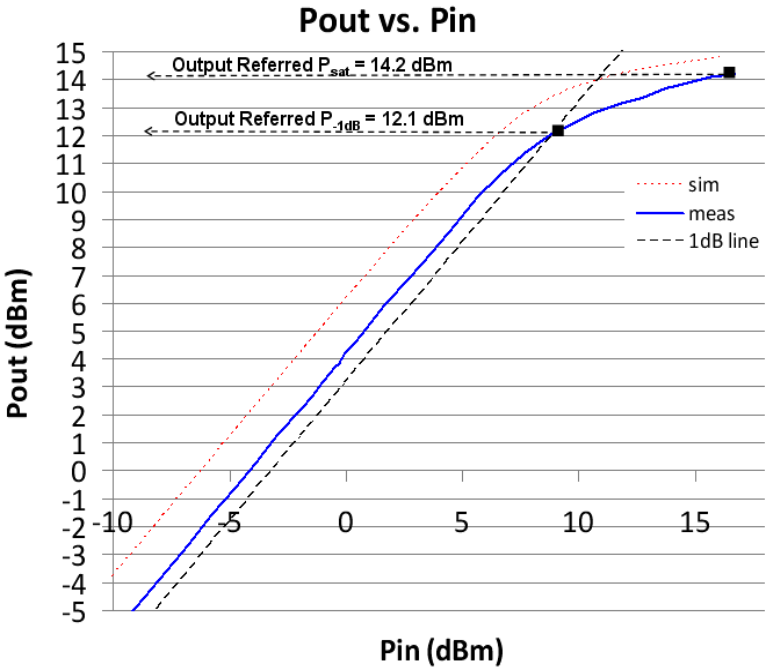

Figure 7.9: Measurement vs. simulation of the four-way 60 GHz PA output power

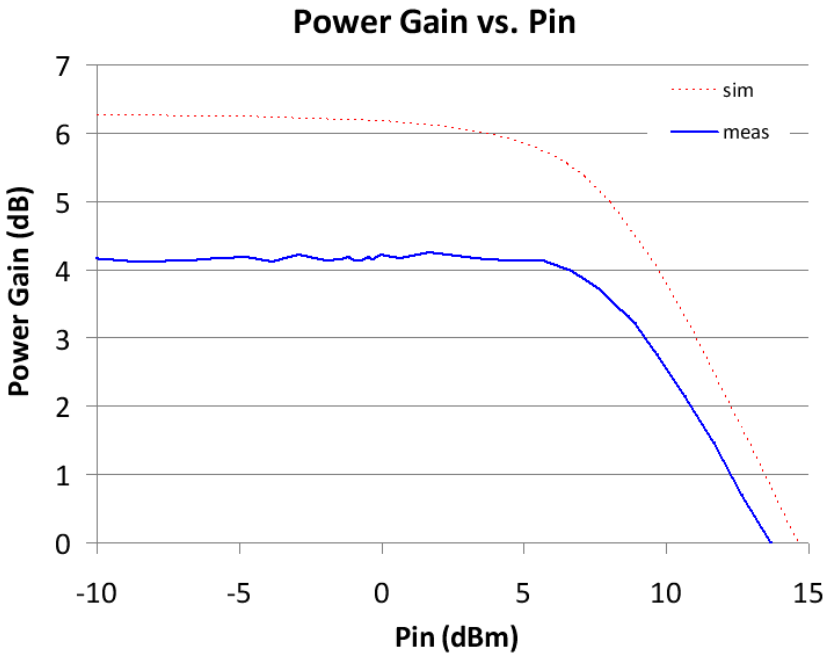

Figure 7.10: Measurement vs. simulation of the four-way 60 GHz PA power gain

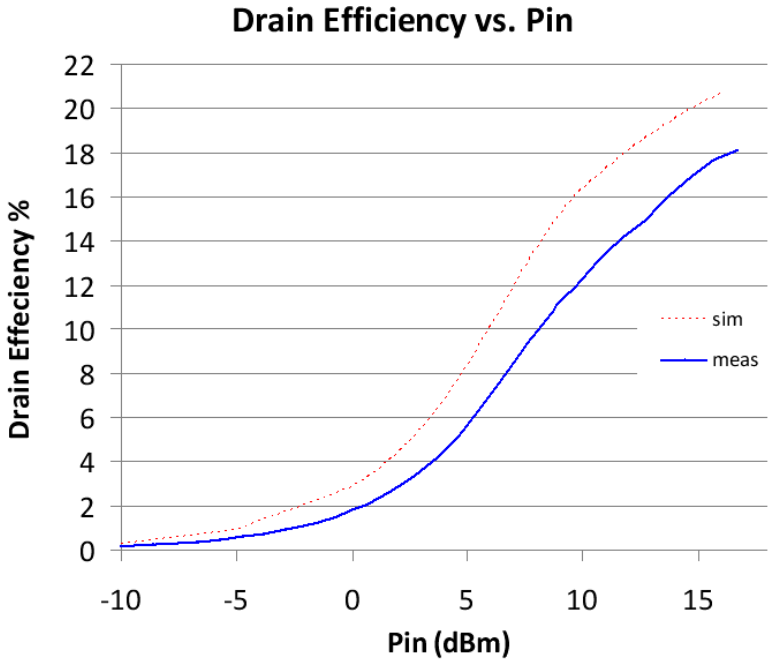

Figure 7.11: Measurement vs. simulation of the four-way 60 GHz PA drain efficiency

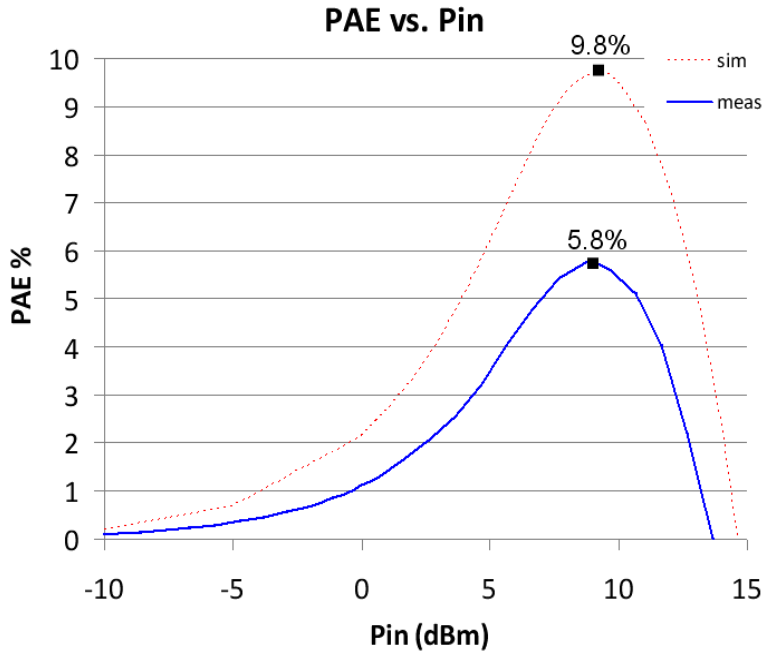

Figure 7.12: Measurement vs. simulation of the four-way 60 GHz PA power added efficiency

The measurement and simulation results are summarized in Table 7.1.

	Measurements	Simulation
Output P_{1dB}	+ 12.1 dBm	+ 12.8 dBm
Output $P_{saturation}$	+ 14.2 dBm	+15.0 dBm
Power Gain	4.2 dB	6.2 dB
1dB compression drain efficiency	11.2%	13.2%
Saturation efficiency	18.1%	20.7%
Maximum PAE	5.8%	9.8%
Peak S_{21}	4.5 dB	4.2 dB
Peak S_{11}	-10 dB	-8 dB
Peak S_{12}	-25 dB	-24 dB
DC power dissipation	145 mW	145 mW

Table 7.1: Summary of the measured and simulated performance results of the four-way 60 GHz power amplifier

7.2 Two-Way Power Amplifier

Along with the four-way power amplifier, a two-way power amplifier that employs the same topology but consists of two unit amplifiers instead of four was also implemented. Similarly, instead of using separate power splitters and combiners to split and combine the power to and from the four unit amplifiers, the amplifier incorporates the power splitter and combiner into the input and output matching networks using the power combining scheme described in section 2.4.3. The power amplifier provides 8.2 dB of power gain and achieves a saturation output power of +14.2 dBm and a 1dB compression output power of +12.1 dBm. It consumes 145 mW from a 1V power supply leading to a saturation efficiency of 18.1%, a 1dB compression efficiency of 11.2%, and peak power added efficiency of 11.5%.

7.2.1 Circuit Description

The circuit diagram of the two-way power amplifier showing the overall amplifier topology and the unit amplifier schematic is shown in Figure 7.13.

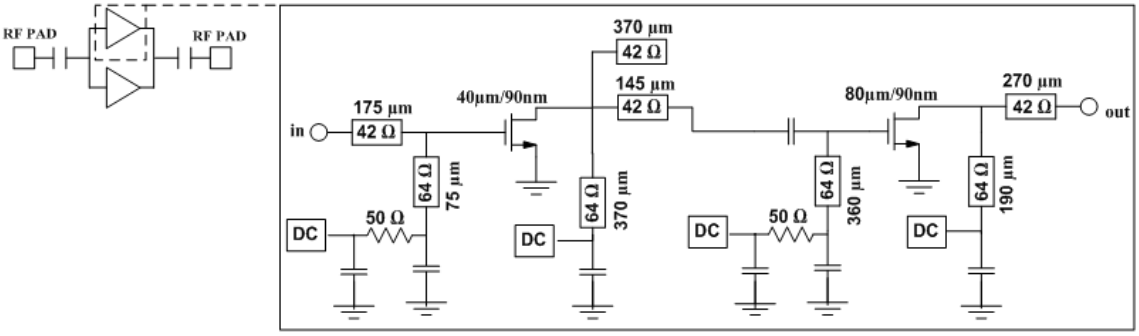

Figure 7.13: Schematic diagram of the two-way 60 GHz power amplifier

The power amplifier consists of two identical unit amplifiers along with the power splitting and combining scheme described in section 2.4.3. The overall architecture and the unit amplifiers topology is similar to that used in the four-way amplifier described in section 7.1. As in the four-way power amplifier, the input matching network is designed such that a long series transmission line is presented at the unit amplifier input allowing the usage of the power splitting and combining schemed described in section 2.4.3. In this case, the 175 µm long transmission lines at the four unit amplifiers inputs are routed to feed a common splitting node and the 270 µm long transmission lines at the four unit amplifiers outputs are routed to feed a common combining node to realize the power splitting and combining functions respectively. In this fashion, no external power splitter or power combiner is added to the power amplifier, and thus no additional power loss is introduced, resulting in higher output power levels and higher power efficiencies. Even

though the overall amplifier input and output ports are matched to the same impedances as in the four-way amplifier, the input and output ports in this case see only two unit amplifiers instead of four. Thus, each unit amplifier input and output are matched to different impedances and thus use different lengths transmission lines.

The chip micrograph of the four-way amplifier is shown in Figure 7.14. It measures 1240x830 μm^2.

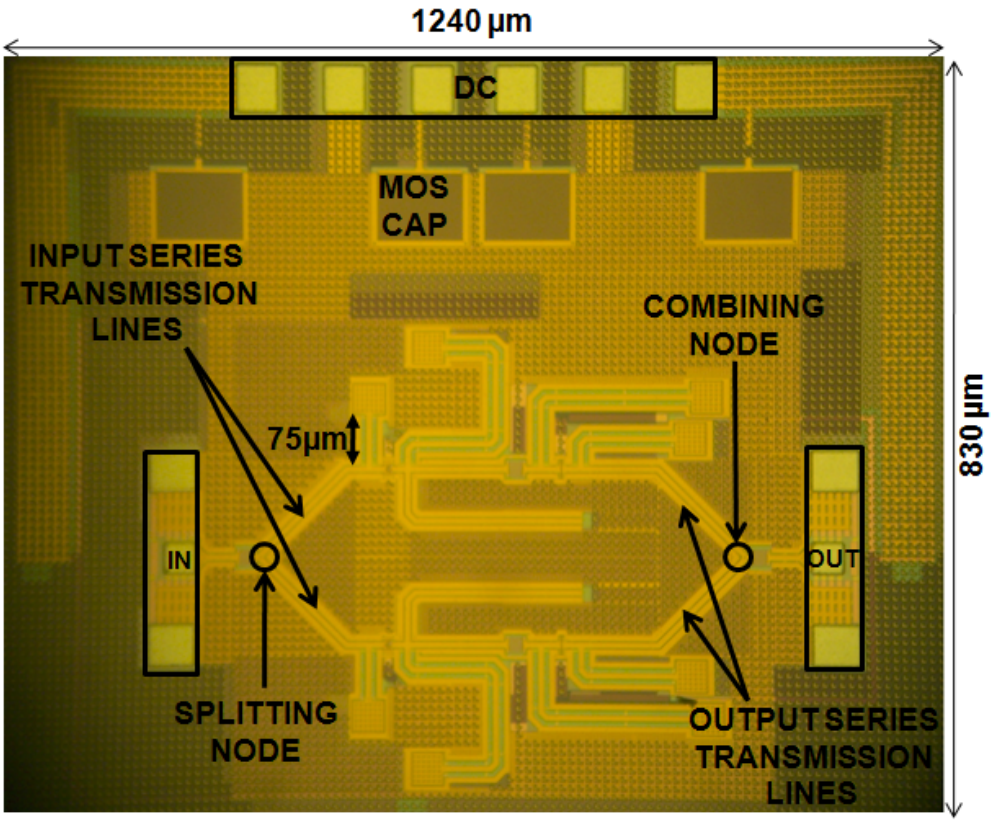

Figure 7.14: Chip micrograph of 2-way 60 GHz power amplifier

7.2.2 Measurement and Simulation Results

Measurement and simulation results are shown in Figure 7.15 to Figure 7.20. The power amplifier provides a measured peak S_{21} of 8.2 dB at 59 GHz compared to a

simulated peak S_{21} of 9 dB at 56 GHz. The S_{21} 3-dB bandwidth is 13 GHz centered around 59 GHz. There exists a 2 GHz shift between the measured and simulated S-parameters. A gain peaking behavior is observed around 27 GHz. However, the amplifier stability is preserved as S_{11} and S_{22} stay below 0 dB, and the stability factor K stay above unity. As the input is matched to 50Ω impedance, it provides a measured S_{11} of -6 dB at 60 GHz compared to a simulated S_{11} of -8.2 dB. S_{12} is better than -22 dB over the entire frequency range.

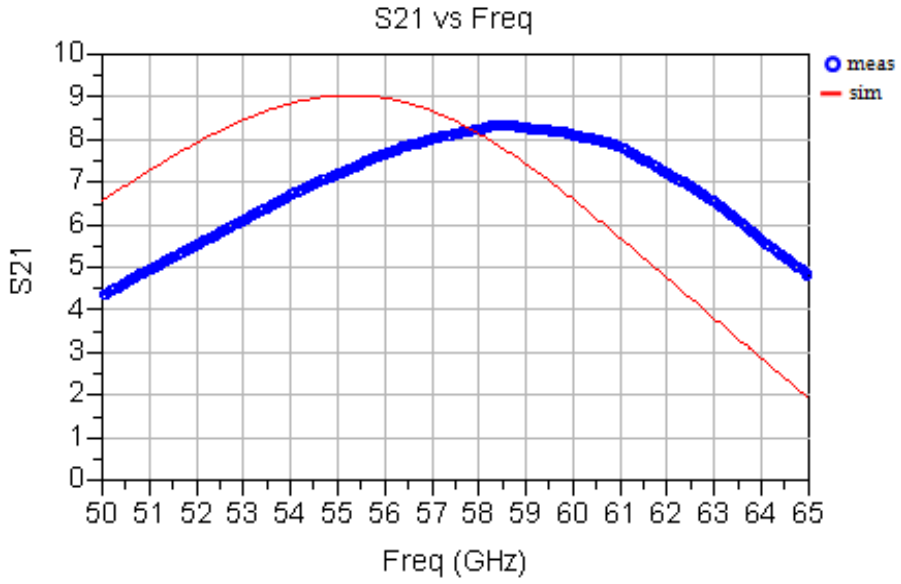

Figure 7.15: S21 measurement vs. simulation of the two-way 60 GHz power amplifier

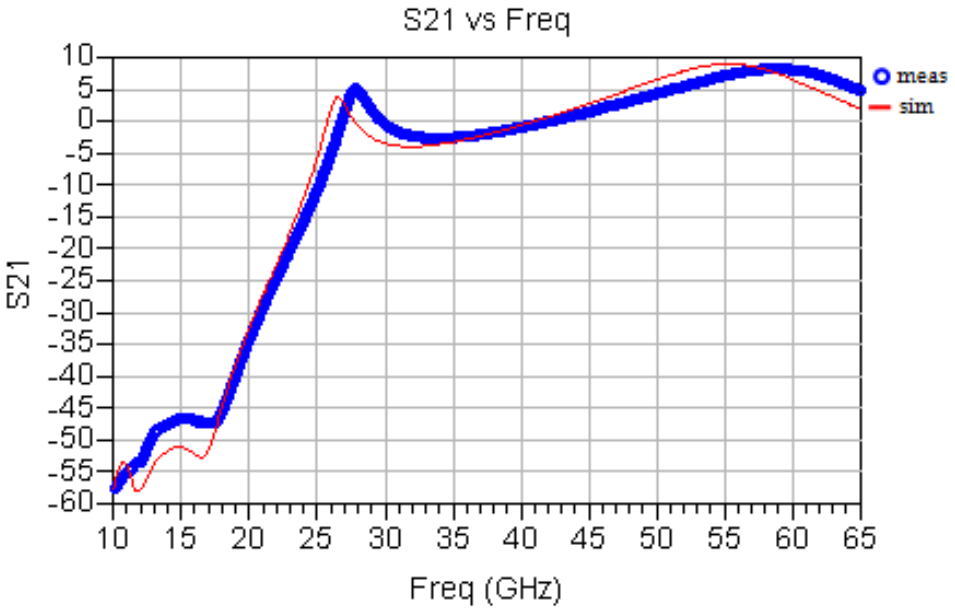

Figure 7.16: S21 measurement vs. simulation of the two-way 60 GHz power amplifier

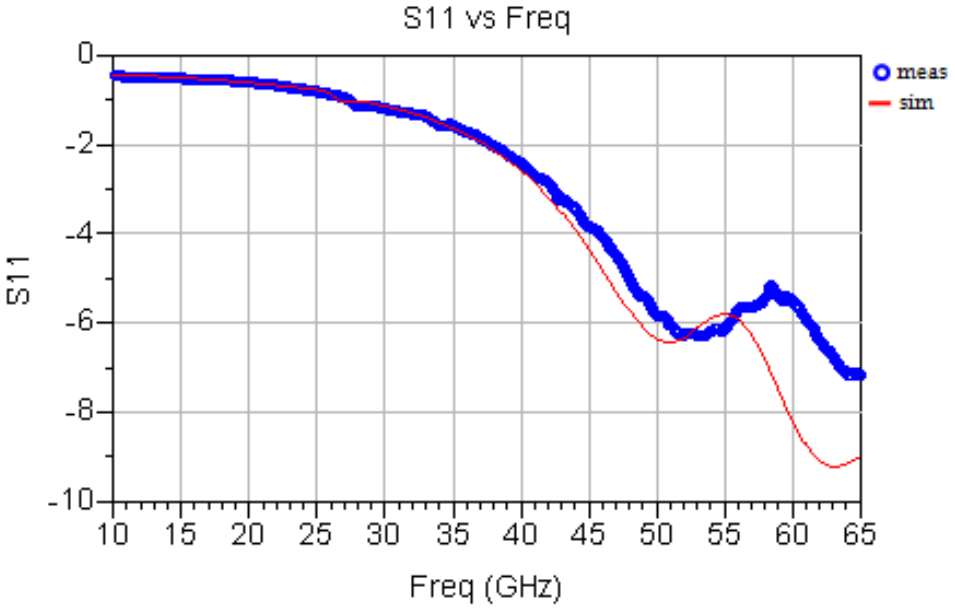

Figure 7.17: S11 measurement vs. simulation of the two-way 60 GHz power amplifier

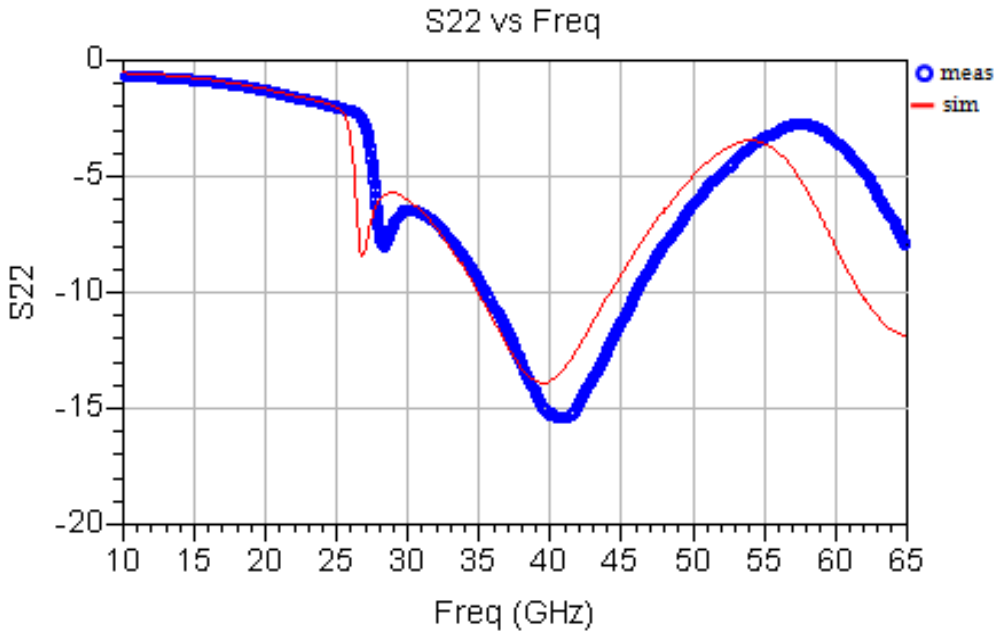

Figure 7.18: S22 measurement vs. simulation of the two-way 60 GHz power amplifier

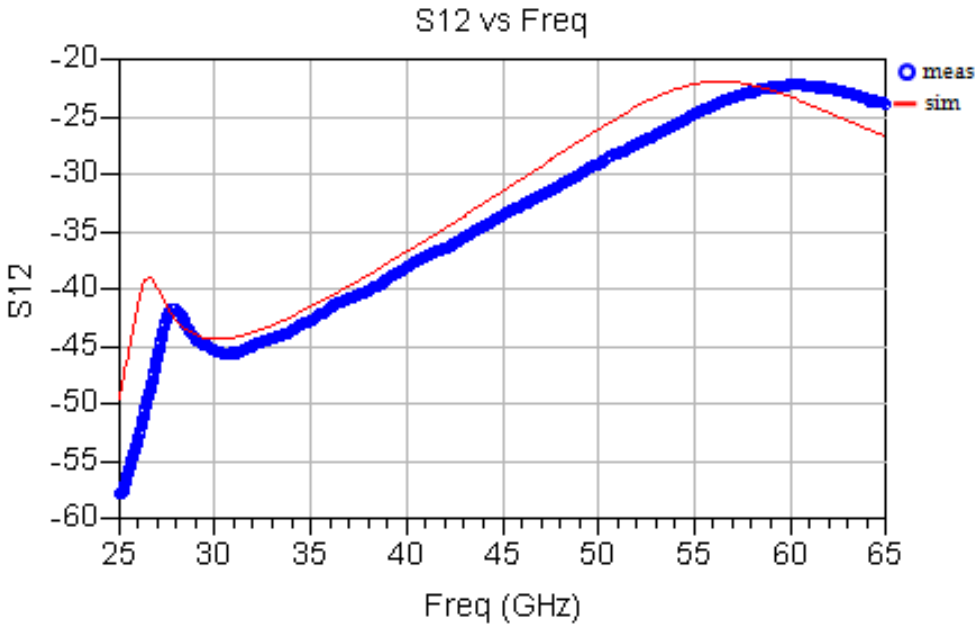

Figure 7.19: S12 measurement vs. simulation of the two-way 60 GHz power amplifier

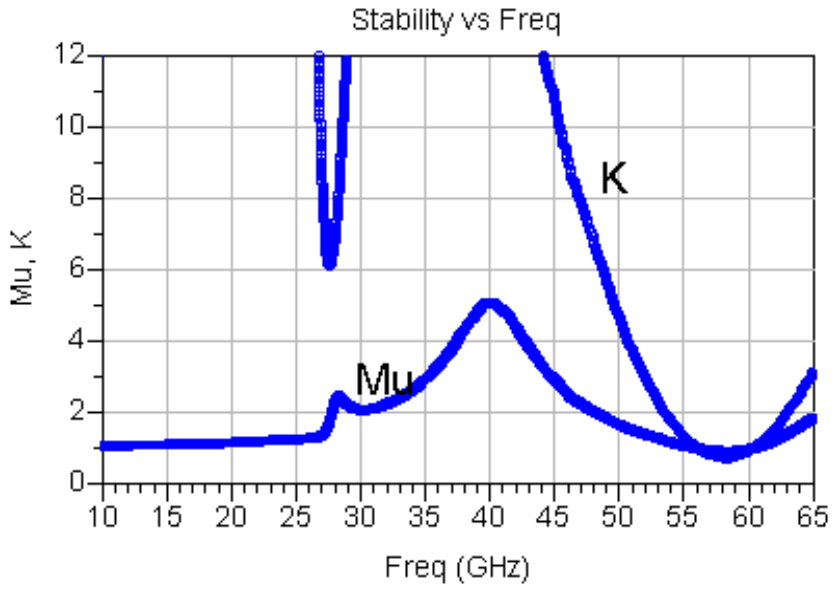

Figure 7.20: Stability factor (K) and μ factor measurement vs. simulation of the two-way 60 GHz power amplifier

Power measurement and simulation results are shown in Figure 7.21 to Figure 7.24. The power amplifier delivers a 1dB compression and saturation output powers of +10.1 dBm and +11.6 dBm respectively, with a 1dB compression and saturation efficiencies of 12.6% and 17.7% respectively. The measured peak power added efficiency is 11.5%. The amplifier consumes 81 mW from a 1V power supply. The linear behavior between the input and output power levels indicates amplifier stability.

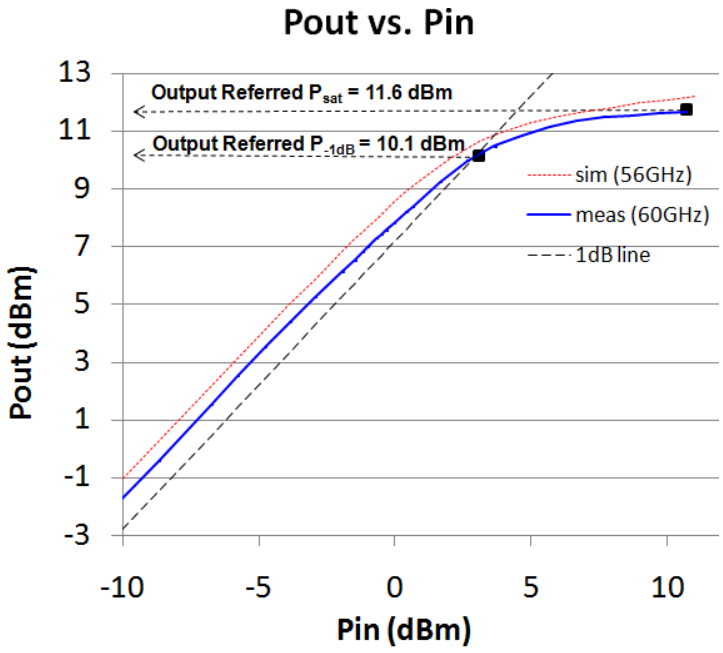

Figure 7.21: Measurement vs. simulation of the two-way 60 GHz PA output power

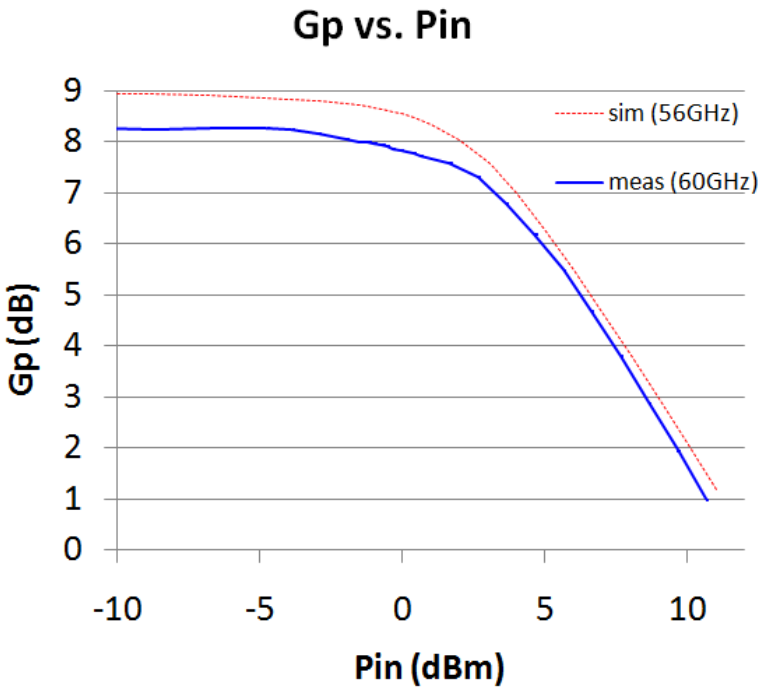

Figure 7.22: Measurement vs. simulation of the two-way 60 GHz PA power gain

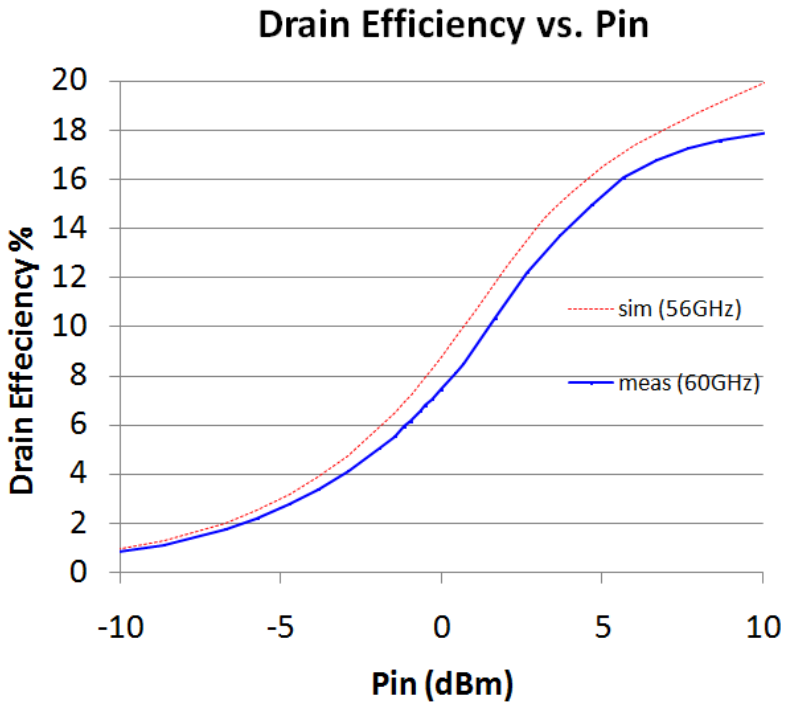

Figure 7.23: Measurement vs. simulation of the two-way 60 GHz PA drain efficiency

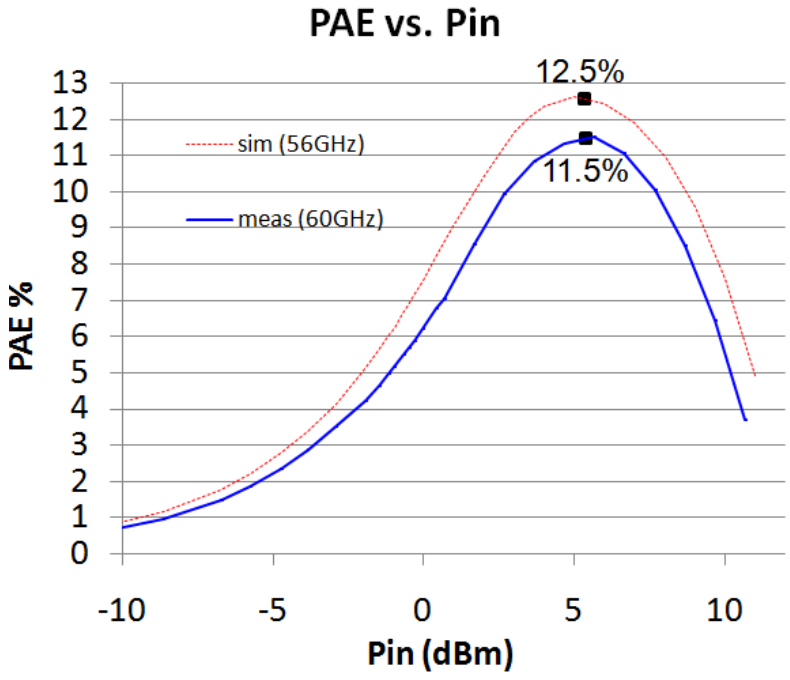

Figure 7.24: Measurement vs. simulation of the two-way PA power added efficiency

The measurement and simulation results are summarized in Table 7.2.

	Measurements	Simulation
Output P_{1dB}	+10.1 dBm	+ 10.5 dBm
Output $P_{saturation}$	+ 11.6 dBm	+ 12.2 dBm
Power Gain	8.2 dB	9 dB
1dB compression drain efficiency	12.6%	13.8%
Saturation efficiency	17.7%	20.5%
Maximum PAE	11.5%	12.5%
Peak S_{21}	8.2 dB	9 dB
Peak S_{11}	-6 dB	-8 dB
Peak S_{12}	-22 dB	-22 dB
DC power dissipation	81 mW	81 mW

Table 7.2: Summary of the measured and simulated performance results of the two-way 60 GHz power amplifier

7.3 Two-Way High Stability – Low Gain Power Amplifier

A second, lower gain, higher stability version of the two-way power amplifier described in section 7.2 above was implemented. The amplifier possesses the same architecture and unit amplifier topology as the first version except for the length of one transmission line only: The shunt transmission line in the input matching network of the first stage has a length of 45 μm instead of 75 μm which results in a more stable operation at the expense of lower power gain.

This power amplifier provides 5 dB of power gain and achieves a measured saturation output power of 10.8 dBm and a measured 1dB compression output power of 9.1 dBm. It consumes 145 mW from a 1V power supply leading to a saturation efficiency of 14.8%, 1dB compression efficiency of 10%, and maximum power added efficiency of 8.8%.

7.3.1 Circuit Description

The circuit diagram of the two-way high stability power amplifier showing the overall amplifier topology and the unit amplifier schematic is shown in Figure 7.25.

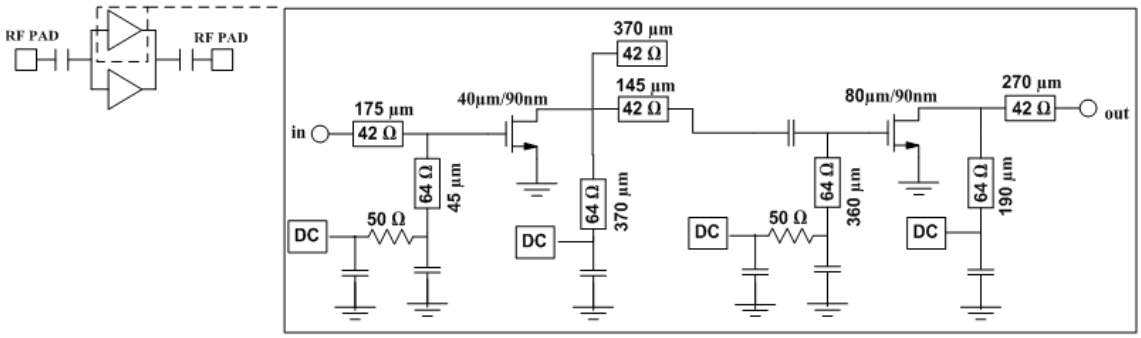

Figure 7.25: Schematic diagram of the high stability two-way 60 GHz power amplifier

This version has about 3 dB less gain than the high gain version presented in section 7.2 but it provides better stability as shown in the stability factor K plot in Figure 7.32.

The chip micrograph of the four-way amplifier is shown in Figure 7.26. It measures 1240x830 μm^2.

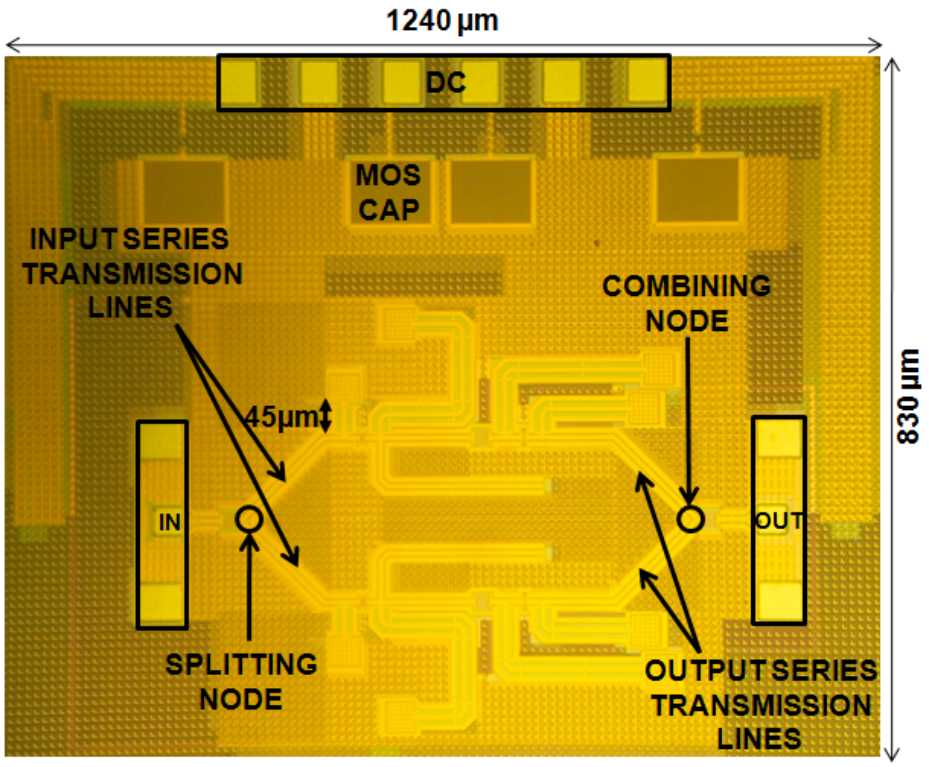

Figure 7.26: Chip micrograph of the high stability two-way 60 GHz power amplifier

7.3.2 Measurement and Simulation Results

S-parameter measurement and simulation results are shown in Figure 7.27 to Figure 7.32. The power amplifier provides a measured peak S_{21} of 5.4 dB at 61 GHz compared to a simulated peak S_{21} of 6.6 dB at 58 GHz. The S_{21} 3-dB bandwidth is 12 GHz centered around 61 GHz. There exists a 3 GHz shift between the measured and simulated S-parameters. A gain peaking behavior is observed around 27 GHz. However, the amplifier stability is preserved as S_{11} and S_{22} stay below 0 dB, and the stability factor K stays above unity. As the input is matched to 50Ω impedance, it provides a measured S_{11} of -7 dB at 60 GHz compared to a simulated S_{11} of -11.5 dB. S_{12} is better than -22 dB

over the entire frequency range. Note that the stability factor of this lower gain - higher stability amplifier provides a larger stability factor margin around 60 GHz (K > 2) compared to the higher gain - lower stability amplifier presented in section 7.2 where the stability factor is barely larger than unity around 60 GHz.

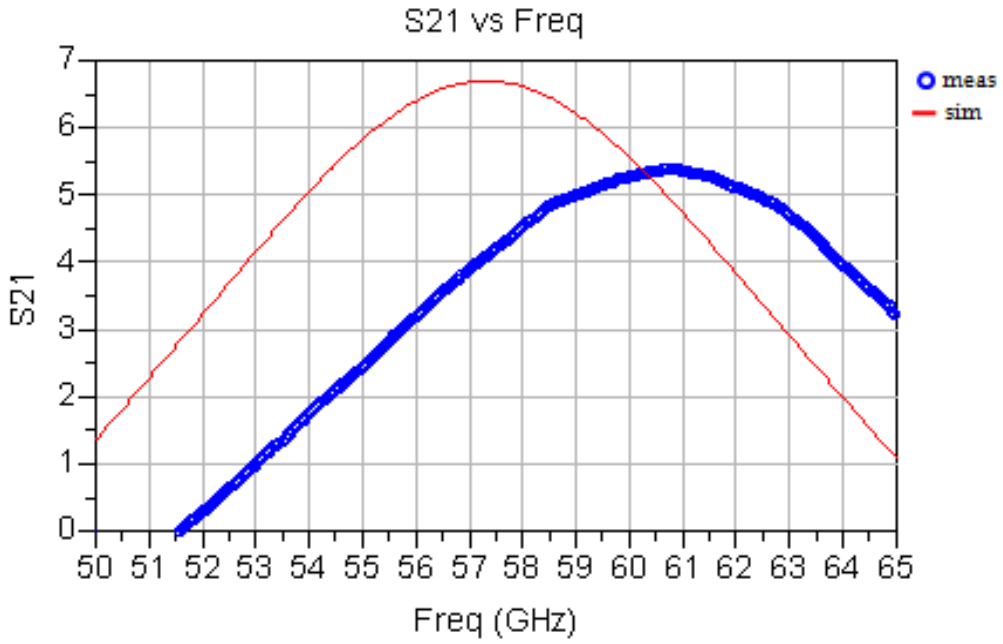

Figure 7.27: S21 measurement vs. simulation of the high stability two-way 60 GHz PA

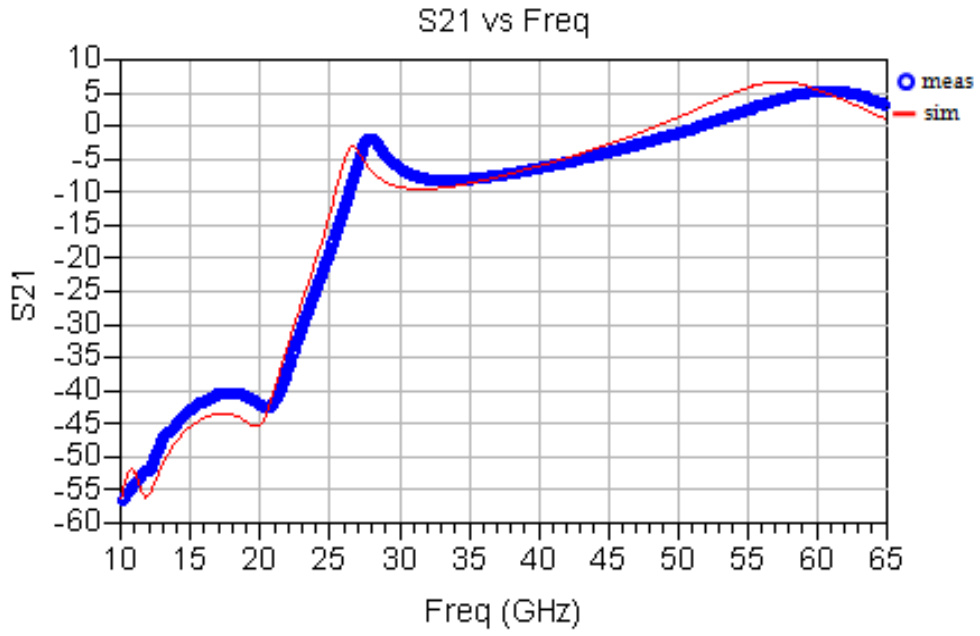

Figure 7.28: S21 measurement vs. simulation of the high stability two-way 60 GHz PA

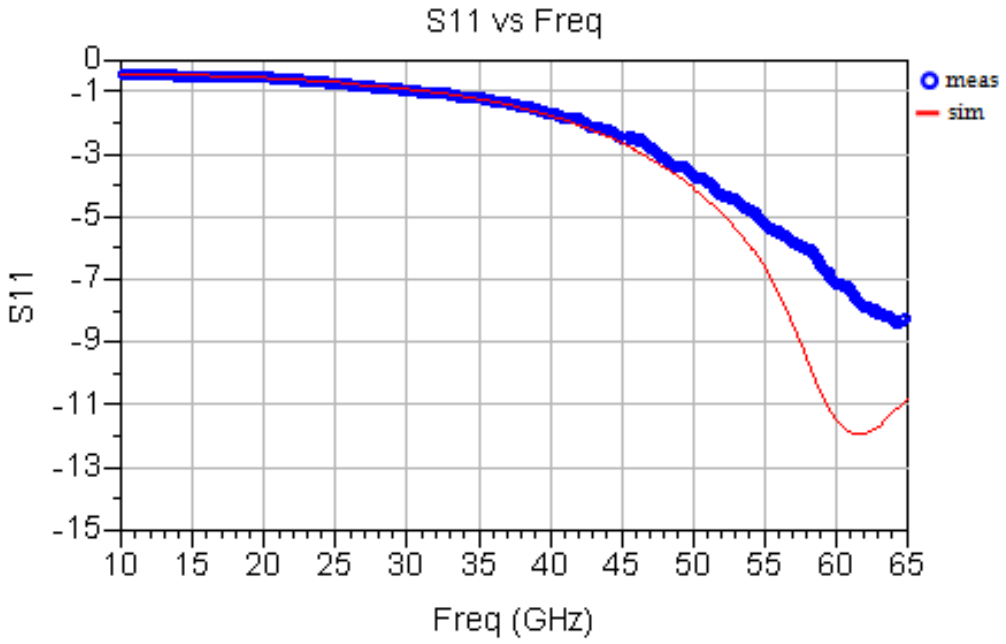

Figure 7.29: S11 measurement vs. simulation of the high stability two-way 60 GHz PA

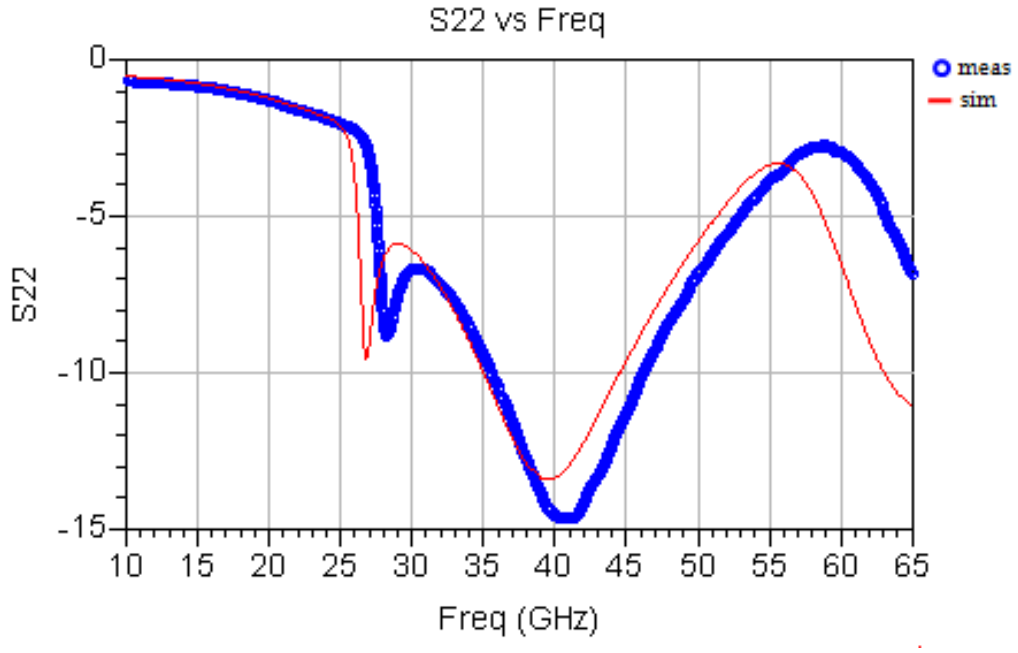

Figure 7.30: S22 measurement vs. simulation of the high stability two-way 60 GHz PA

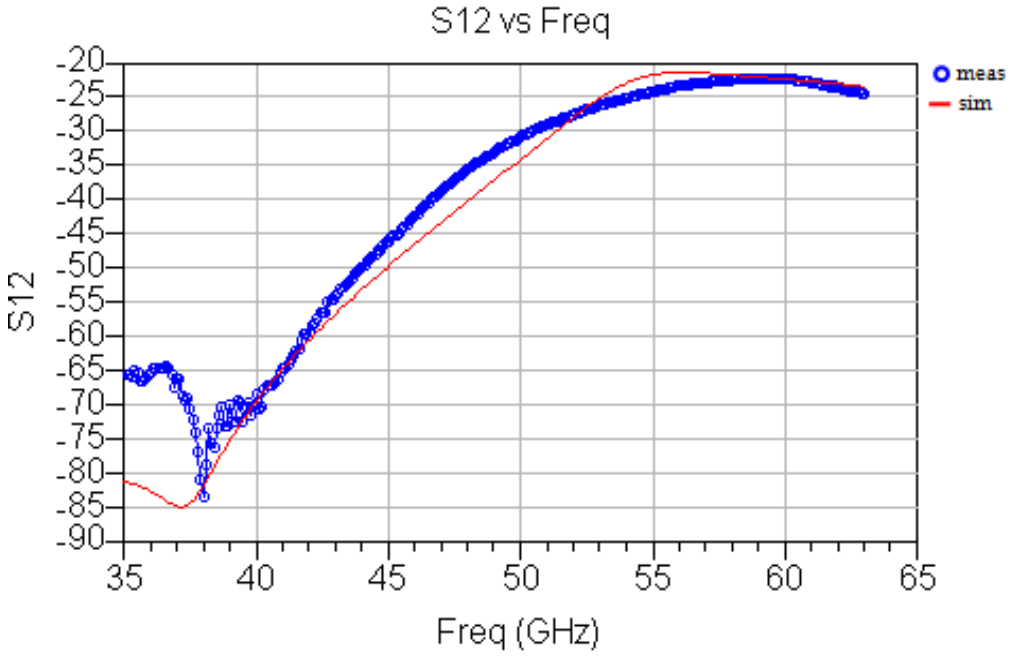

Figure 7.31: S12 measurement vs. simulation of the high stability two-way 60 GHz PA

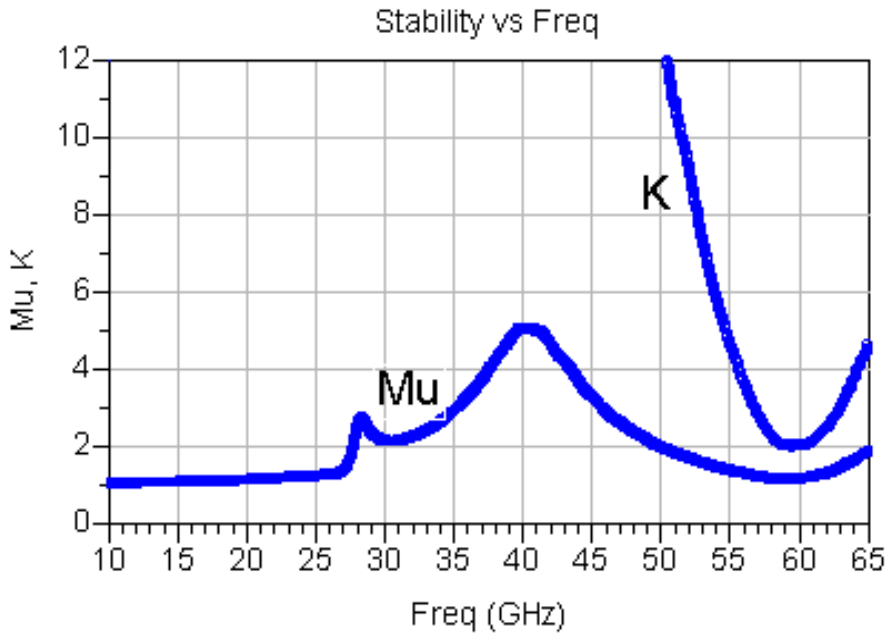

Figure 7.32: Stability factor (K) and μ factor measurement vs. simulation of the high stability two-way 60 GHz PA

Power measurement and simulation results are shown in Figure 7.33 to Figure 7.36. The power amplifier delivers measured 1dB compression and saturation output powers of +9.1 dBm and +10.8 dBm respectively, with a 1dB compression and saturation efficiencies of 10% and 14.8% respectively. The peak measured power added efficiency is 6.6%. The amplifier consumes 81 mW from a 1V power supply. The linear behavior between the input and output power levels indicates amplifier stability.

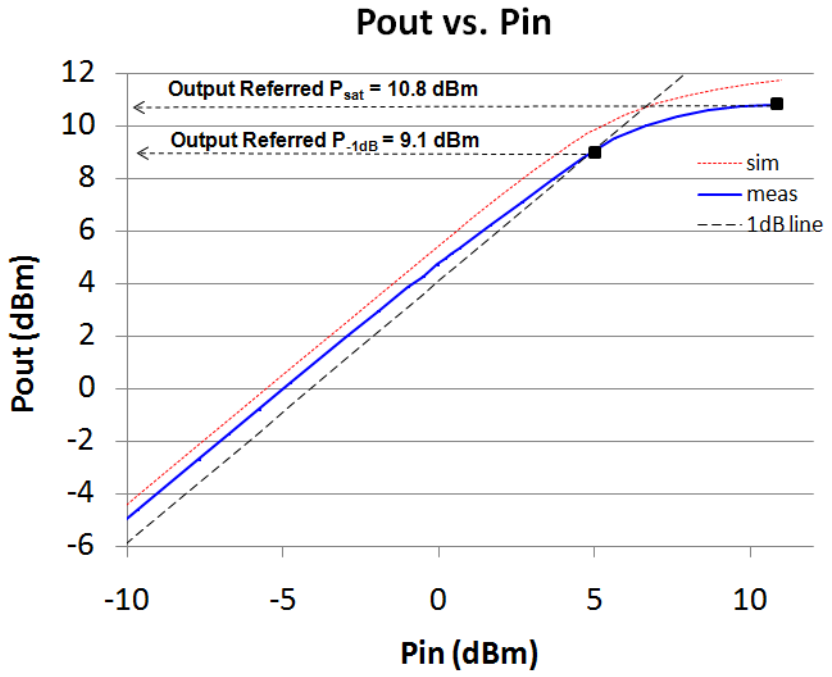

Figure 7.33: Measurement vs. simulation of the high stability two-way 60 GHz PA output power

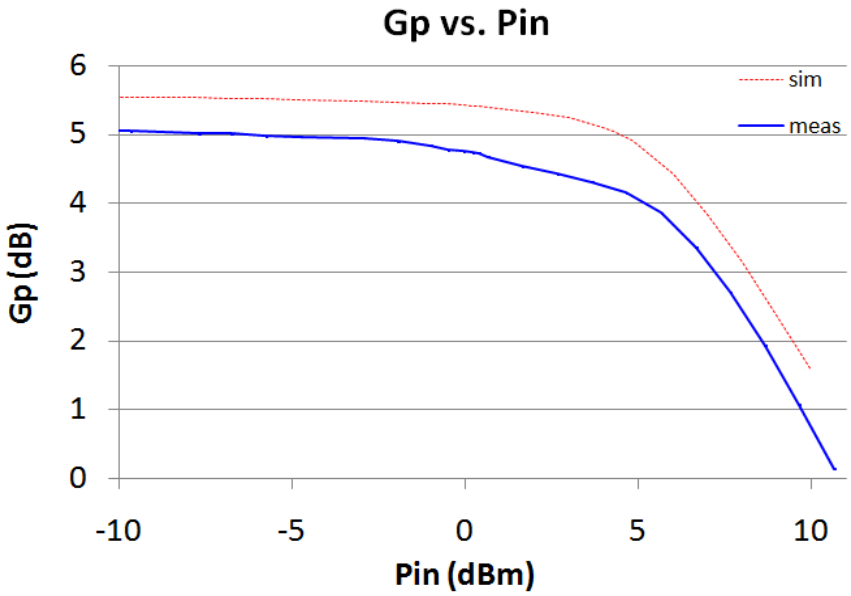

Figure 7.34: Measurement vs. simulation of the high stability two-way 60 GHz PA power gain

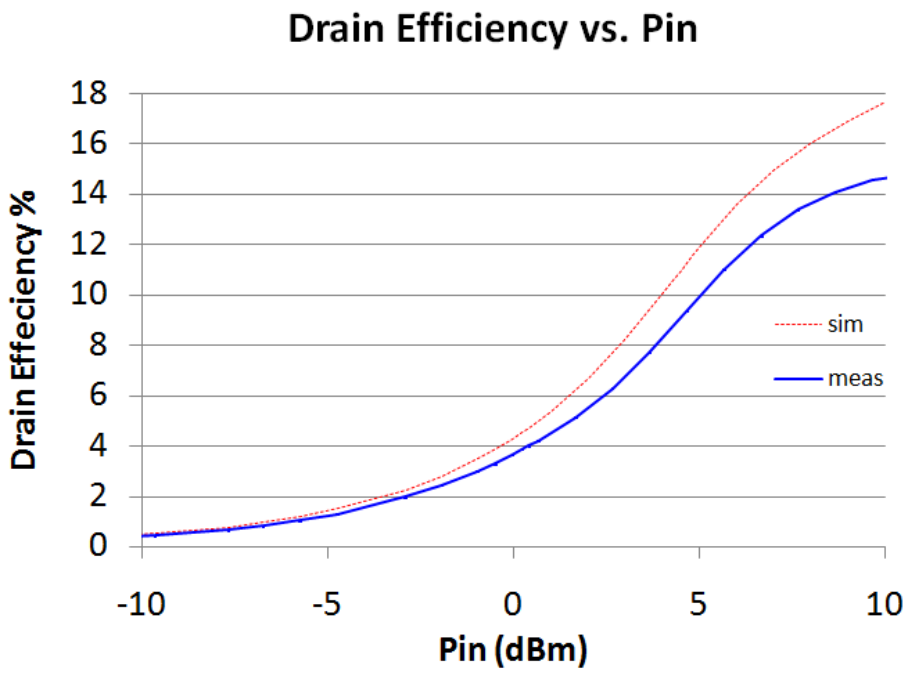

Figure 7.35: Measurement vs. simulation of the high stability two-way 60 GHz PA drain efficiency

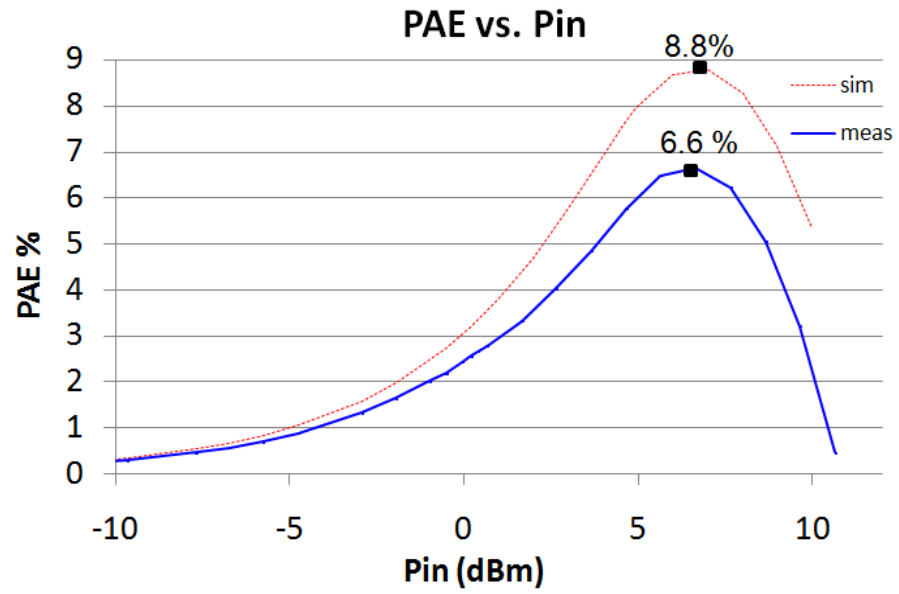

Figure 7.36: Measurement vs. simulation of the high stability two-way 60 GHz PA power added efficiency

The measurement and simulation results are summarized in Table 7.3.

	Measurements	Simulation
Output P_{1dB}	+ 9.1 dBm	10.1 dBm
Output $P_{saturation}$	+ 10.8 dBm	11.7 dBm
Power Gain	5 dB	5.5 dB
1dB compression drain efficiency	10%	12.6%
Saturation efficiency	14.8%	11.3%
Maximum PAE	8.8%	6.6%
Peak S_{21}	5.4 dB	6.6 dB
Peak S_{11}	-7 dB	-11.5%
Peak S_{12}	-22 dB	-21 dB
DC power dissipation	81 mW	81 mW

Table 7.3: Summary of the measured and simulated performance results of the high stability two-way 60 GHz power amplifier

7.4 Two-Way Power Amplifier with Inductive Source Degeneration

A two-way power amplifier based on a unit amplifier that employs source degeneration [28] has been designed and implemented in ST Microelectronics' 90 nm standard CMOS process. Even though this power amplifier employs integrated power splitter and combiner, it does not use the low loss mm-wave power splitting and combining scheme described in section 2.4.3 where the power splitter and combiner are integrated into the input and output matching networks. On-chip power splitter and combiner are introduced as extrinsic to the unit amplifiers in order to split / combine the power into / from the two unit amplifiers, and thus the overall power amplifier results in lower output power and efficiencies. The power amplifier provides 7.1 dB of power gain

and achieves a saturation output power of +10 dBm and a 1 dB compression output power of +8 dBm while consuming 77 mW from a 1V power supply leading to a saturation efficiency of 13%, a 1dB compression efficiency of 8.2%, and a peak power added efficiency of 6.8%.

7.4.1 Circuit Description

The circuit diagram of the two-way power amplifier with inductive source degeneration showing the overall amplifier topology and the unit amplifier schematic is shown in Figure 7.37.

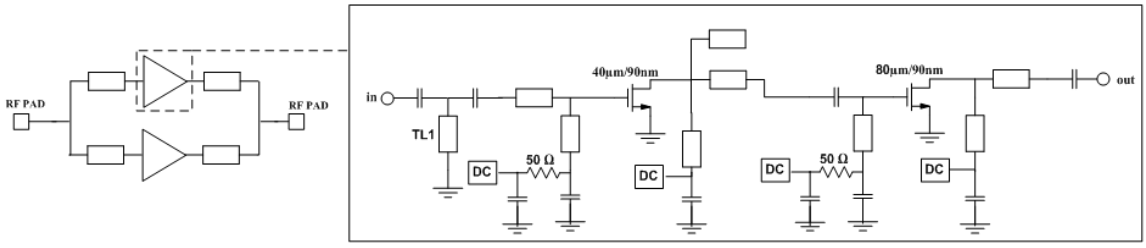

Figure 7.37: Schematic diagram of the two-way 60 GHz power amplifier with inductive source degeneration

Since this unit amplifier topology does not present a long series transmission line at the input and output of the amplifier as part of the input and output matching networks, the low loss mm-wave power splitting and combining scheme of section 2.4.3 could not be used. That scheme requires that the first element of the first stage input matching network following the input AC coupling capacitor be a long series transmission line and that the last element of the last stage output matching network just before the output AC coupling capacitor be a long series transmission line. Instead, the unit amplifier employed

in this PA presents a shorted parallel transmission line (TL1) at its input. Thus, on-chip integrated power splitter and power combiner have been introduced as extrinsic parts to the unit amplifiers in order to split / combiner the power into / from the two unit amplifiers rather than integrate them into the input and output matching networks. As will be shown in the next section, this leads to significantly lower output power levels and efficiency than the power amplifiers described in sections 7.1, 7.2, and 7.3.

The unit amplifier is comprised of two active stages. The first stage uses a 40 fingers (1μm/finger) transistor whereas the second uses an 80 fingers device. The second stage transistor is made twice as large as the first stage transistor in order to insure that the output transistor enters compression first. Both transistor layouts are implemented using the "round table" structure described in [6, 47]. This structure shows an improved available gain compared to the regular multi-finger structure and thus is preferred especially for the first stage which is optimized for maximum gain rather than maximum output power. The output stage consumes 14 mA of current whereas the driver input stage consumes 7 mA, both from a 1V power supply. All matching networks have been realized using coplanar transmission lines with characteristic impedance of 51 Ω and length varying between λ/20 and λ/6. The metal finger capacitors described in sections 4.2 are used for AC coupling and supply - ground bypass. The RF Ground-Signal-Ground pads are incorporated as part of the input and output matching networks. The shunt transmission line at the input (TL1) provides high impedance around 60 GHz but low impedance at low frequencies and thus helps ensure low frequency stability where the transistor gain is very large. In order to add a degree of freedom in the stability - power

gain tradeoff, the output stage transistor employs inductive source degeneration using a short transmission line connected to ground. The DC voltages are provided to the gates and drains of all transistors through the transmission lines of the matching networks. The gate bias networks are de-Q'ed using series 50 Ω resistors in order to suppress potential instability at low frequencies. In order to realize high output power, the power combiner and the output matching networks are designed to convert the 50 Ω load at the power amplifier output into 15 Ω impedances seen at the drain of the second stage 80 μm transistor. Note that the output transistor gain would drop significantly if it were to drive a 50 Ω load. A compromise is made between gain and output power when selecting the optimum load impedance. An inter-stage matching network is also introduced between the driver stage and the output stage in order to insure maximum power transfer between the stages as well as the stability of each stage. The input matching networks along with the power splitter provide a 50 Ω input match.

The chip micrograph of the four-way amplifier is shown in Figure 7.38. It measures 1580 x 1150 μm^2.

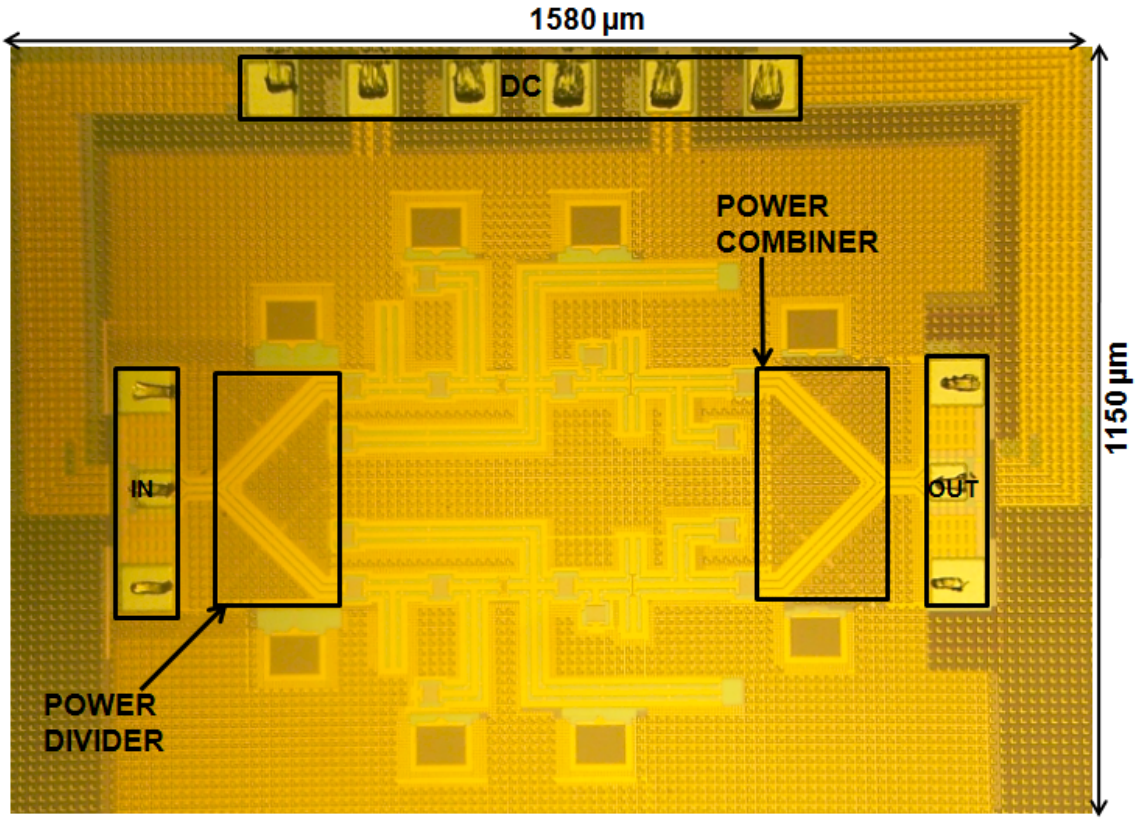

Figure 7.38: Chip micrograph of 2-way 60 GHz power amplifier with inductive source degeneration

7.4.2 Measurement and Simulation Results

S-parameters measurement and simulation results are shown in Figure 7.39 to Figure 7.44. The power amplifier provides a measured peak S_{21} of 7.8 dB at 58 GHz compared to a simulated peak S_{21} of 10 dB at 56 GHz. The mismatch between measurement and simulations might be the result of inaccurate modeling of the source degenerated transistor in the output stage in addition to process variations. As a result of introducing the shunt transmission line at the input matching network to reduce low frequency gain, no gain peaking is observed as opposed to the three amplifiers presented

in sections 7.1, 7.2, and 7.3. S_{21} stays below -40 dB for all frequencies below 40 GHz. As the input is matched to 50Ω impedance, it provides a measured S_{11} of -11 dB at 60 GHz compared to a simulated S_{11} of -11.5 dB. S_{12} is better than -22 dB over the entire frequency range. For stable operation, the measured S_{11} and S_{22} are less than 0 dB and the stability factor K is larger than two over the entire frequency range.

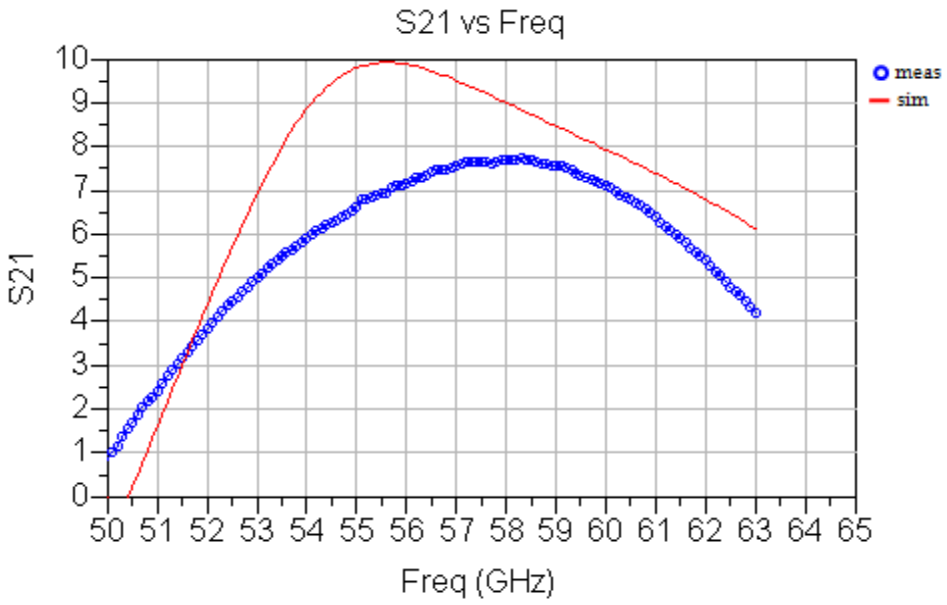

Figure 7.39: S21 measurement vs. simulation of the two-way 60 GHz power amplifier with inductive source degeneration

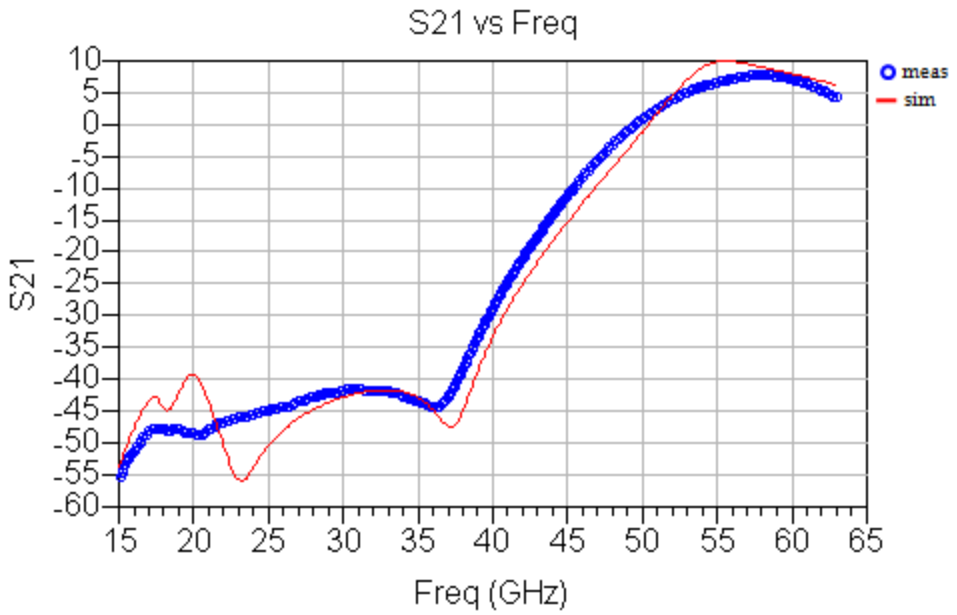

Figure 7.40: S21 measurement vs. simulation of the two-way 60 GHz power amplifier with inductive source degeneration

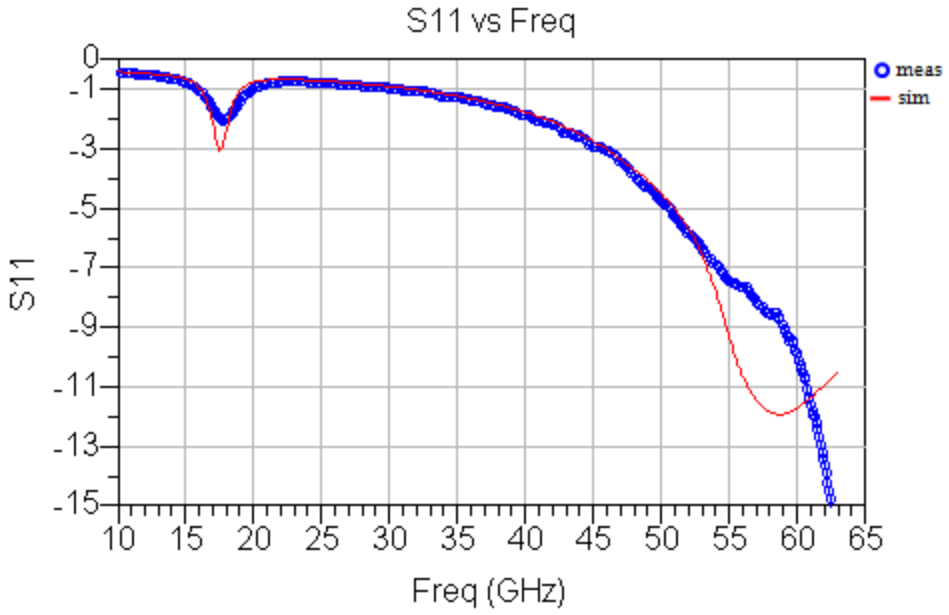

Figure 7.41: S11 measurement vs. simulation of the two-way 60 GHz power amplifier with inductive source degeneration

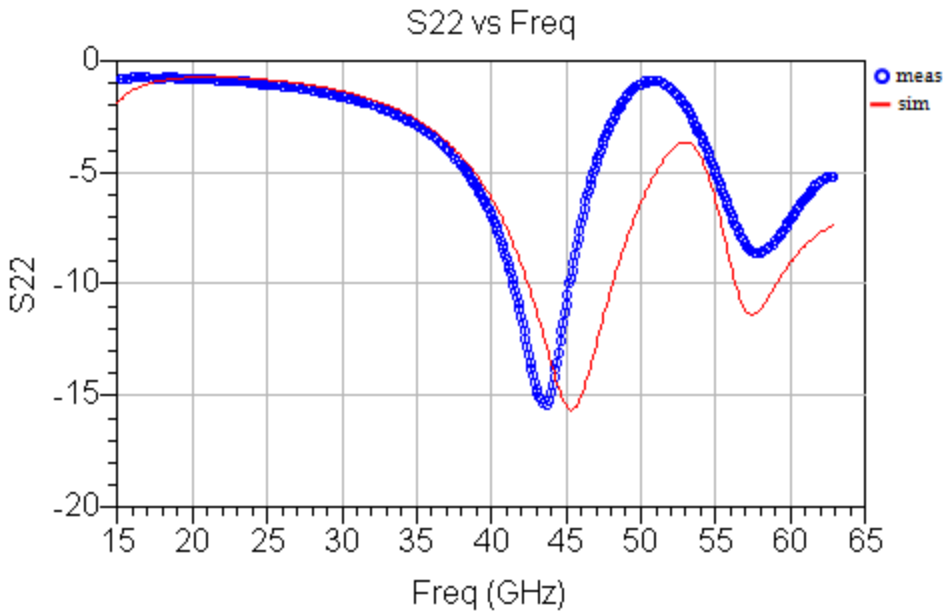

Figure 7.42: S22 measurement vs. simulation of the two-way 60 GHz power amplifier with inductive source degeneration

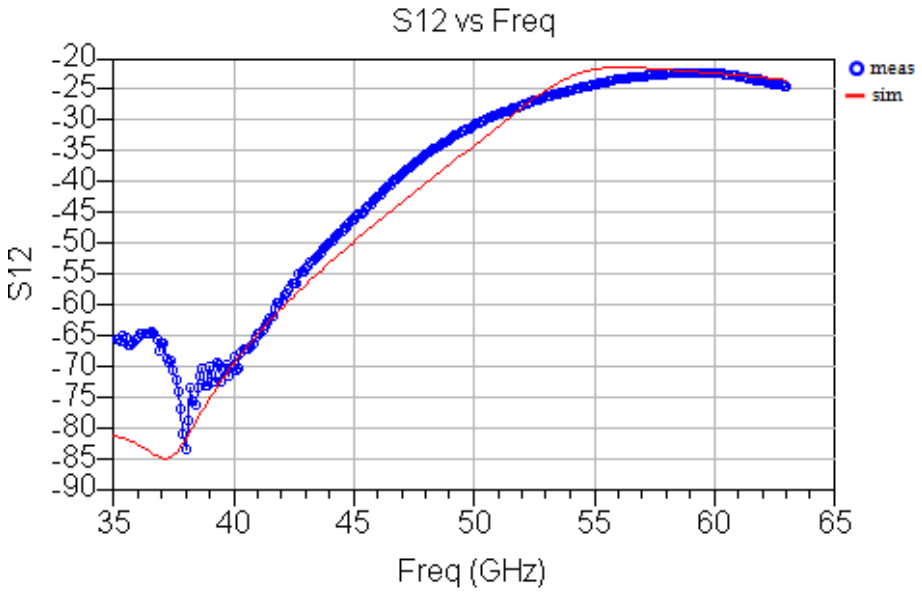

Figure 7.43: S12 measurement vs. simulation of the two-way 60 GHz power amplifier with inductive source degeneration

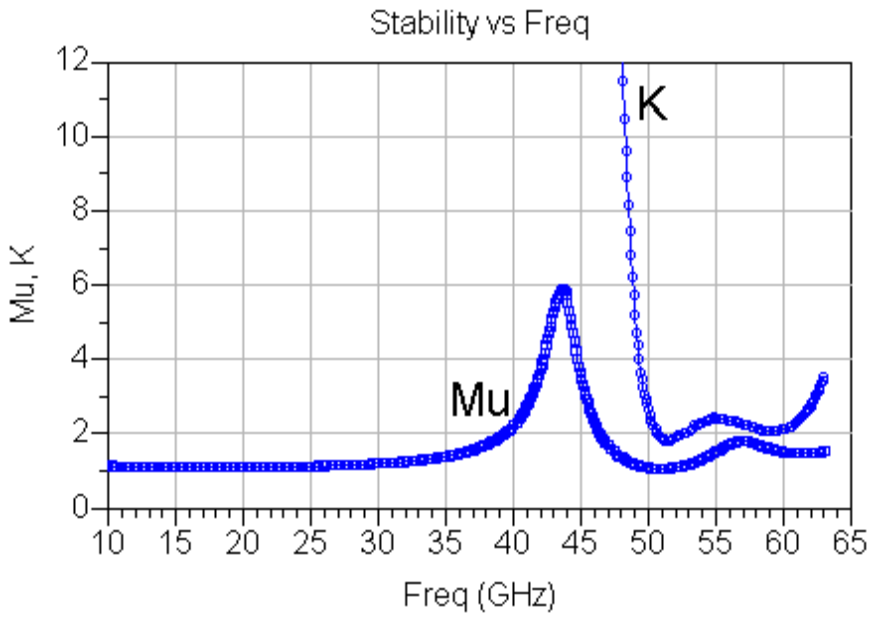

Figure 7.44: Stability factor (K) and μ factor measurement vs. simulation of the two-way 60 GHz power amplifier with inductive source degeneration

Power measurement and simulation results are shown in Figure 7.45 to Figure 7.48. The power amplifier delivers measured 1dB compression and saturation output powers of +8 dBm and +10 dBm respectively, with a 1dB compression and saturation efficiencies of 8.2% and 13% respectively. The peak measured power added efficiency is 6.8%. The amplifier consumes 77 mW from a 1V power supply. The linear behavior between the input and output power levels indicates amplifier stability.

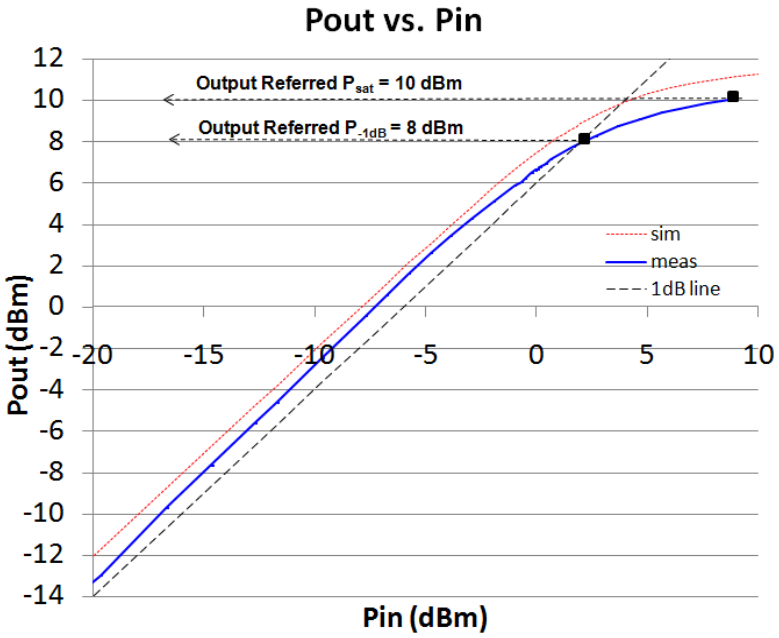

Figure 7.45: Measurement vs. simulation of the output power of the two-way 60 GHz power amplifier with inductive source degeneration

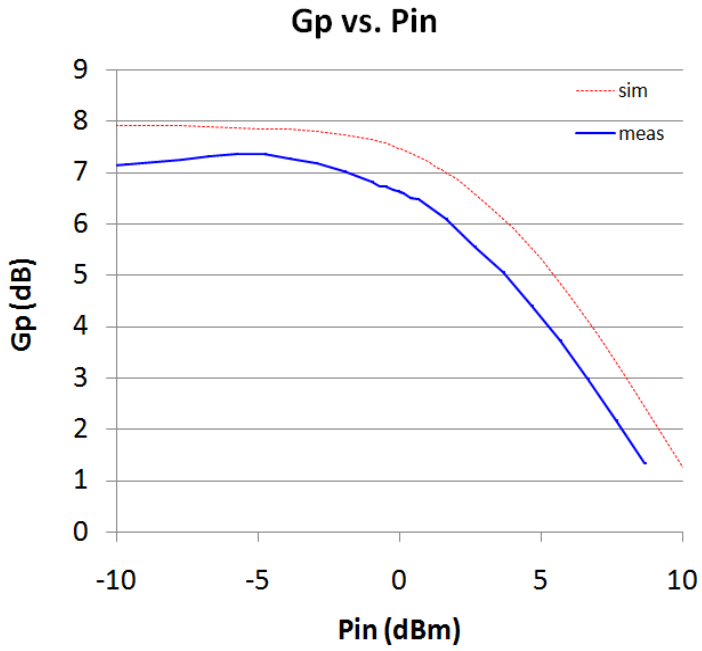

Figure 7.46: Measurement vs. simulation of the power gain of the two-way 60 GHz power amplifier with inductive source degeneration

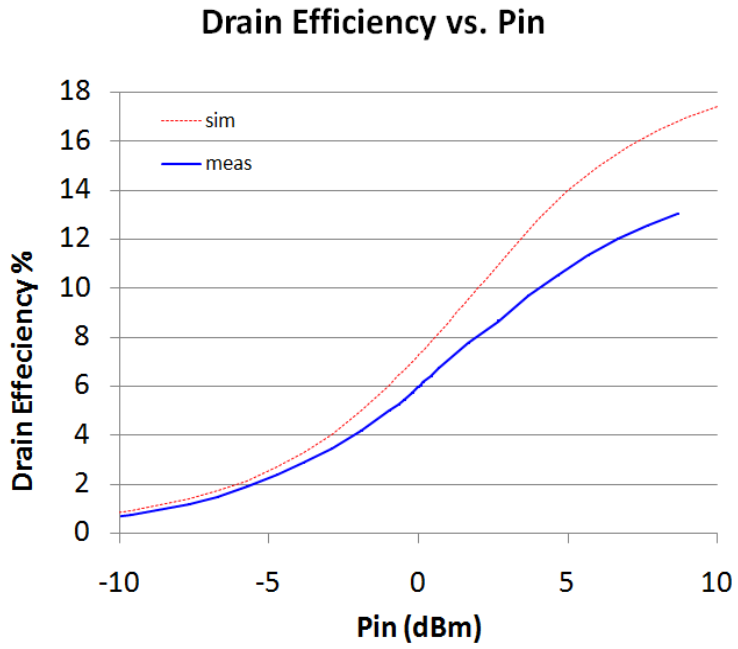

Figure 7.47: Measurement vs. simulation of the drain efficiency of the two-way 60 GHz power amplifier with inductive source degeneration

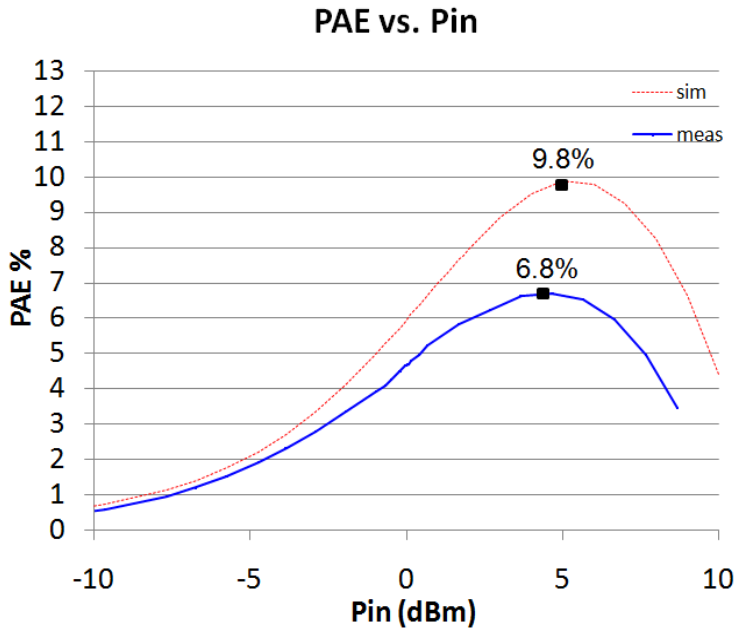

Figure 7.48: Measurement vs. simulation of the power added efficiency of the two-way 60 GHz power amplifier with inductive source degeneration

The measurement and simulation results are summarized in Table 7.4.

	Measurements	Simulation
Output P_{1dB}	8 dBm	8.9 dBm
Output $P_{saturation}$	10 dBm	11.3 dBm
Power Gain	7.3 dB	7.9 dB
1dB compression drain efficiency	8.2%	9.9%
Saturation efficiency	13%	17.4%
Maximum PAE	6.8%	9.8%
Peak S_{21}	7.8 dB	10 dB
Peak S_{11}	-11 dB	-11.5 dB
Peak S_{12}	-23 dB	-22 dB
DC power dissipation	77 mW	77 mW

Table 7.4: Summary of the measured and simulated performance results of the two-way 60 GHz power amplifier with inductive source degeneration

7.5 Comparison to Power Amplifiers in the Literature

References	[28]	[14]	[15]	[16]	[17]	[12]	[18]	[19]	**This work 4way / 2way**
Frequency (GHz)	60	60	48	61.5	77	60	60	77	**60**
Supply voltage (V)	1.0	1.5	1.5	2.5	2.5	1.0	1.0	1.2	**1.0**
P-1dB (dBm)	6.7	6.4	5.0	11.2	11.6	9.0	10.0	4.7	**12.1 / 10.1**
Psat (dBm)	-	9.3	8.0	16.0	12.5	12.3	11.3	10.6	**14.2 / 11.6**
Peak PAE (%)	20	7.4	7	4.3	3.5	8.8	8.2	-	**5.8 / 11.5**
S21 (dB)	9.8	5.2	25	10.8	6.1	5.6	14.3	8.0	**4.4 / 8.3**
Area (mm^2)	0.54	0.15	1.13	1.68	1.58	0.25	0.18	0.975	**1.20 / 1.03**
Technology	90nm CMOS	90nm CMOS	90nm CMOS	0.12µm SiGe HBT	0.12µm SiGe HBT	90nm CMOS	90nm CMOS	90nm CMOS	**90nm CMOS**

Table 7.5: Comparison to state of the art 60 GHz power amplifiers in the literature

7.6 Measurement Setup

The power measurements have been performed using the Anritsu 69397B synthesized signal generator, the Anritsu SC6230 thermal power sensor, and the Anritsu ML2437A power meter, while the S-parameter measurements haven been performed using the Anritsu 37397C Vector Network Analyzer. While measurement equipment and

cable losses have been carefully de-embedded, pad losses are included in the measurements.

7.7 Conclusions

Four prototype power amplifiers are implemented in ST Microelectronics' 90 nm 1V standard CMOS process. Instead of using separate power splitters and power combiners to split and combiner to power to and from the unit amplifiers, the amplifiers incorporate the power splitters and combiners into the input and output matching networks. The unit amplifiers employ optimum size transistors of 100 fingers, 1 μm per finger, in the last stage. Combining the output power from four unit amplifiers, the four-way power amplifier provides record performance in terms of 1dB compression and saturation output power. The first of the three two-way power amplifiers exhibits high gain with high output power while the second provides lower gain but higher stability margin. The fourth power amplifier uses inductive source degeneration for linearization.

CHAPTER 8

CONCLUSIONS

8 Conclusions

Although CMOS technology scaling at the 130 nm technology node and beyond has resulted in f_T and f_{max} levels high enough to implementing 60 GHz CMOS transceivers, mm-wave power amplifiers still face many challenges. Decreasing supply voltages necessitate the design of ever larger transistors in order to obtain high output power levels while the mm-wave power gain – output power tradeoff limits both the maximum finger width and the maximum number of fingers that can be used. Power combining as a way to achieve higher output power levels is investigated and a low-loss power combining technique taking advantage of millimeter-wave amplifier topologies is presented. Impedance matching in the presence of the power gain – output power tradeoff necessitates the use of multi-stage amplifiers.

As supply voltages scale even further with future CMOS technology nodes, it will become even more challenging to deliver high output power levels and thus power combining will become more crucial. On the other hand, smaller technology nodes will provide higher gain, and thus relatively larger transistors will become feasible as the designer will afford to exchange gain for output power.

Modeling of passive structures and active devices plays an increasingly crucial role at mm-wave frequencies as the passive losses due to skin effect, substrate loss, and proximity effects are substantially high and the active devices gains are considerably low

such that a very small error margin between measurement and simulation can be tolerated.

The modeling strategy followed in this work consists in breaking up the amplifier into its basic constituent components, building test structures for each component, measuring their S-parameters at frequencies up to 65 GHz, modeling each component on its own by using custom models and optimizing the model parameters to fit the measured data, and then putting together the complete model.

As CMOS technology scales further, future processes can provide higher gain and thus higher modeling error margin can be tolerated, simplifying the modeling process.

The design, optimization, and modeling of mm-wave passive structures such as transmission lines, capacitors, and RF pads are investigated. A library of transmission lines of different geometries is built, measured, and modeled using both ADS and HFSS. High density metal multi-finger capacitors employing all available metal layers are used for both AC coupling and supply - ground bypass. A library of capacitors is built, measured, and modeled with custom Π models. As RF Ground-Signal-Ground pads are considered part of the amplifiers design and thus not de-embedded, the structure is optimized and modeled as well.

As this modeling methodology scales well with technology scaling if the same materials are used, once the passive structures of a specific technology node are modeled, few modifications are needed when scaling to smaller nodes.

Current CMOS transistors operating at mm-wave frequencies provide low gain figures and thus modeling their behavior accurately is necessary. Careful design and

layout are required to push the performance limits of the active devices as device layout parasitics have a significant impact on performance. Multi-finger transistor layouts with small tapered gate and drain networks proved to provide optimum performance. Custom small signal and large signal models were developed.

As technology scales to smaller technology nodes, CMOS transistors will be capable of providing larger gain figures at mm-wave frequencies, and thus a large modeling error margin can be tolerated. Readily available transistor models that ship with the processes could be used, significantly reducing the modeling effort required. This would also free the designer from the limitation of using only transistor geometries that have been built and measured.

Four prototype power amplifiers are implemented in ST Microelectronics' 90 nm 1V standard CMOS process. Instead of using separate power splitters and power combiners to split and combiner to power to and from the unit amplifiers, the amplifiers incorporate the power splitters and combiners into the input and output matching networks. The unit amplifiers employ optimum size transistors of 100 fingers, 1 μm per finger, in the last stage. Combining the output power from four unit amplifiers, the four-way power amplifier provides record performance in terms of 1dB compression and saturation output power. The first of the three two-way power amplifiers exhibits high gain with high output power while the second provides lower gain but higher stability margin. The fourth power amplifier uses inductive source degeneration for linearization.

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