Keysight Technologies
MIPI Design & Test
Gain Insights Into Your Best Design




Mobile devices are driving the needs for higher performance and lower power usage.

KEYSIGHT TECHNOLOGIES

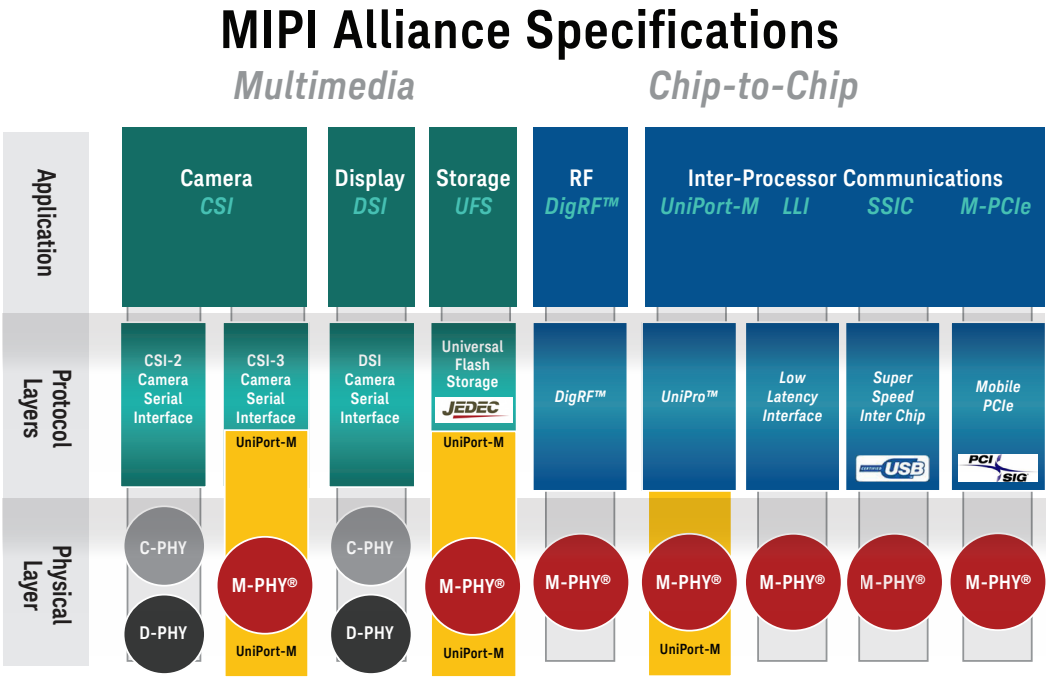
Introduction

The constant addition of capabilities to smartphones and tablets has brought a proliferation of interfaces between processors and devices such as microphones, cameras, loudspeakers, displays, and peripheral electrical devices. This has made ASIC development and system integration of mobile devices an increasingly complex task.

The MIPI® Alliance

The MIPI Alliance is a standard body that promotes hardware and software standardization in mobile designs in an effort to streamline the integration of so many different and rapidly changing technologies. The mission of the Alliance is to benefit the entire mobile industry by establishing standards for hardware and software interfaces within mobile devices. The Alliance believes that openness and standardization fuel market growth for mobile devices, as well as addresses numerous roadblocks currently facing designers, developers, and manufacturers. Currently, more than 250 member companies (including Keysight Technologies, Inc.) actively participate in the Alliance, developing specifications which drive consistency in processor and peripheral interfaces, promoting reuse and compatibility in mobile devices. The specifications it has generated maximize design reuse, drive innovation and reduce time-to-market for all participants.

In contrast to other digital standards, such as USB or PCIe, which are monolithic, i.e. contain both protocol as well as physical (PHY) layers, most of the high-speed MIPI standards are not, i.e. different protocols reside on the same common PHY-layer.



The structure of MIPI high-speed digital standards with separate protocols and PHY layers. Unlike other digital standards, the MIPI standard has several different protocols on 3 separate physical layers.

Introduction (continued)

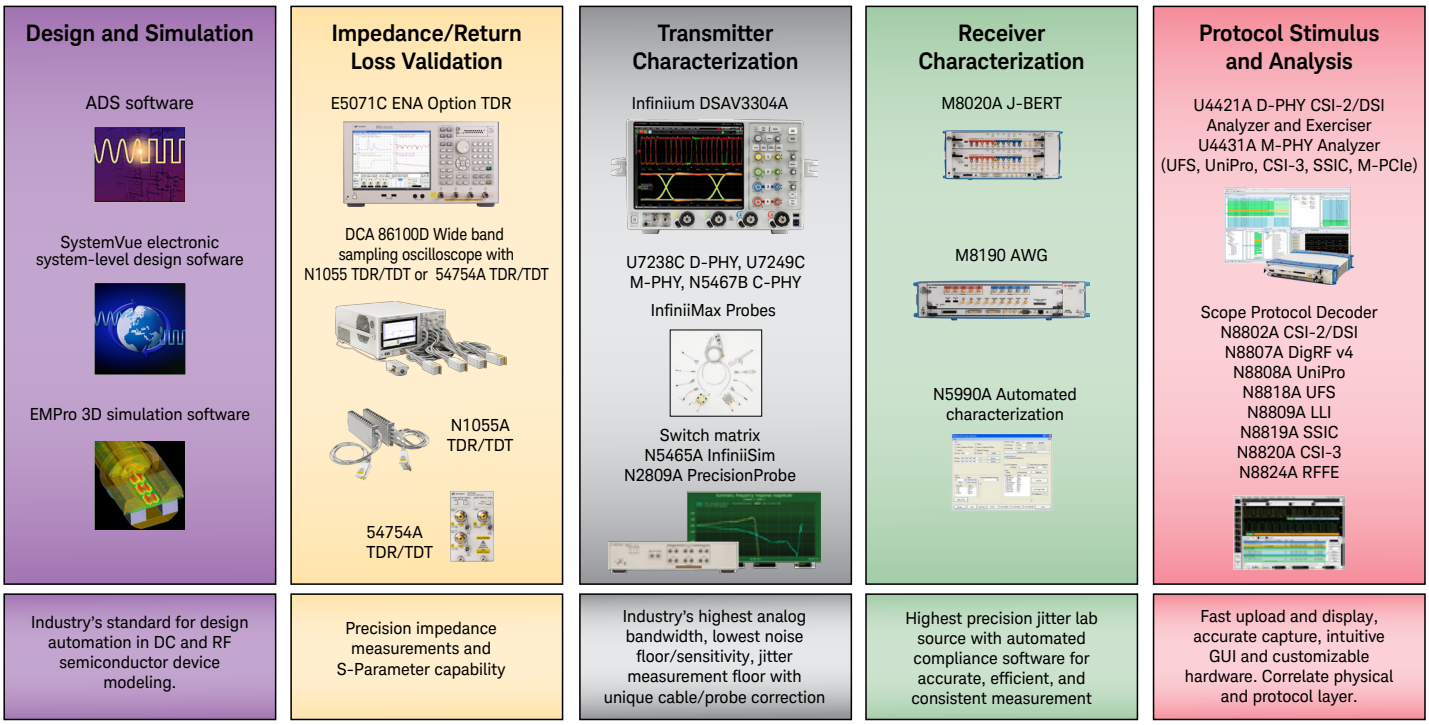
The D-PHY and C-PHY Physical layers support the camera and display applications while camera (CSI-3), UFS and all Chip-to-Chip applications are supported on top of the M-PHY layer. CSI-3 and UFS are using the UniPro protocol stack layer, depicted in yellow as an intermediate interface between the M-PHY and the higher level protocol layers for camera, display and UFS.

The Physical Layer parameters are typically tested by electrical layer tools such as the oscilloscopes, bit error rate testers and network analyzers. Protocol Layers are typically tested by protocol-capable tools.

Leverage outside of the MIPI alliance

In addition to the use within the MIPI standards and because the M-PHY layer delivers more performance and power savings, other standard bodies have started to leverage the M-PHY specification. For instance, the SSIC protocol from the USB standard body uses the M-PHY layer to transmit USB 3.0 protocol. The UFS or Universal Flash Storage protocol from the JEDEC standard body and also PCI Express are adopting the M-PHY spec as well. The MIPI M-PHY layer offers power saving features and provisions for bandwidth on demand as a quick way to leverage existing IPs into the mobile segment and also vice versa, leveraging these typical “mobile features” into standard computer applications.

Keysight test solutions provide complete coverage for your MIPI validation needs.



Keysight has total test solution coverage across all MIPI validation needs – from design to test across all protocols and all physical stands

Design and Simulation

Count on Keysight to help you through to a complete gigabit design. Our deep expertise in this area is built into our Advanced Design System (ADS) software and its capabilities that model RF and microwave effects quickly and accurately. You can use ADS and the Keysight Physical layer test system (PLTS) software to solve tough modeling problems such as long, lossy interconnects or crosstalk in densely packed interconnects. Furthermore, you can make both vector network analyzer (VNA) and time domain reflectometry (TDR) measurements that can be easily calibrated and controlled by the PLTS software.

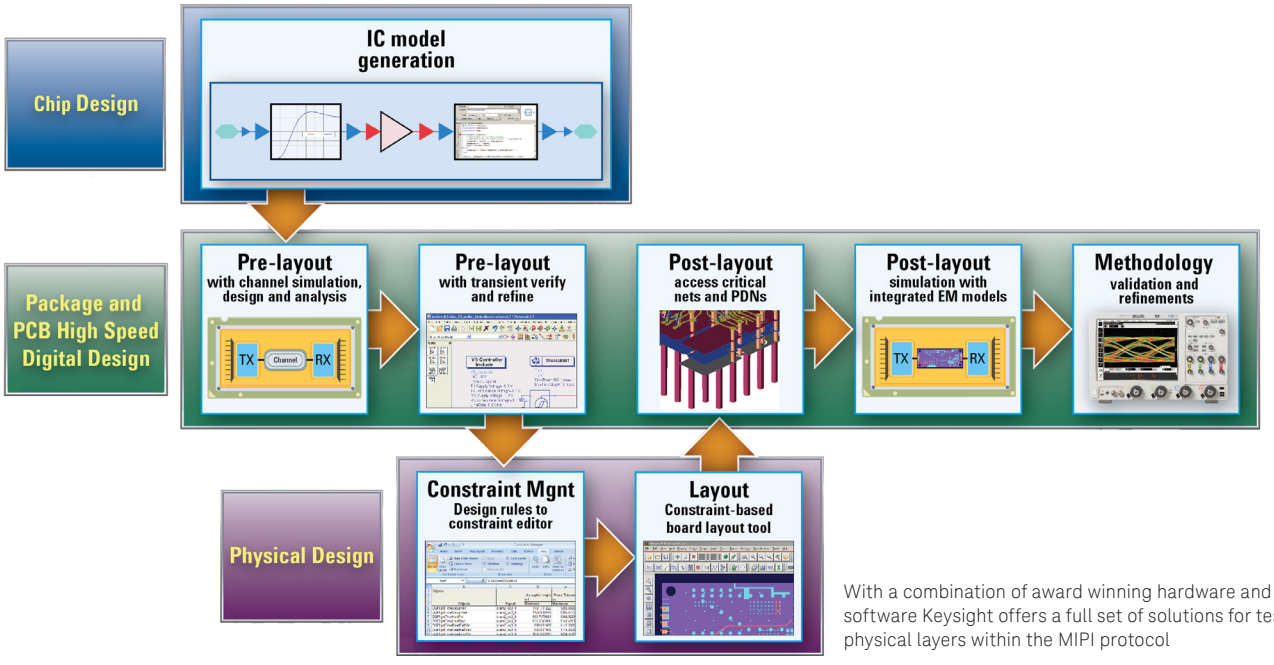
ADS provides an integrated workflow that unites system, circuit and Physical-level design and simulation. One important benefit of this tight integration is to help you eliminate time-consuming and error-prone transfers between single-function tools. With ADS, you can work where you're most comfortable: work in the time or frequency domain, or straddle both, to suit each task, component or problem. Straddling the domains is an effective way to debug stubborn problems. For example, mode-conversion analysis in the PLTS software helps you pinpoint crosstalk problems in high-speed inter¬connects, and multi-domain analysis will help you locate Physical layer problems in high speed channels.

To help you pinpoint problems, ADS provides integrated simulation and data displays. You can visualize channel- or circuit-simulation results, with eye-diagram, mask and bit error rate-contour displays.

Available statistical analysis techniques include a unique treatment of transmitter jitter modeling that correlates closely with measured data. Channel Simulator supports not only built-in generic models but also IC models conforming to the IBIS AMI industry standard.

ADS supports your whole development flow, from early data-link engineering through the pre-layout and post-layout stages. You can import post-layout artwork from constraint-based enterprise tools such as Cadence Allegro, Mentor1 Expedition and Zuken CR5000. Using ADS Momentum, you can create an EM model of your critical net and power delivery network (PDN) artwork for use in both the frequency and time domains. For power integrity analysis in the time domain, ADS supports hybrid convolution that accurately accounts for the low frequency PDN impedance changes from the decoupling capacitors.

High Speed Digital Design Flow



With a combination of award winning hardware and automation software Keysight offers a full set of solutions for testing the different physical layers within the MIPI protocol

Physical layer

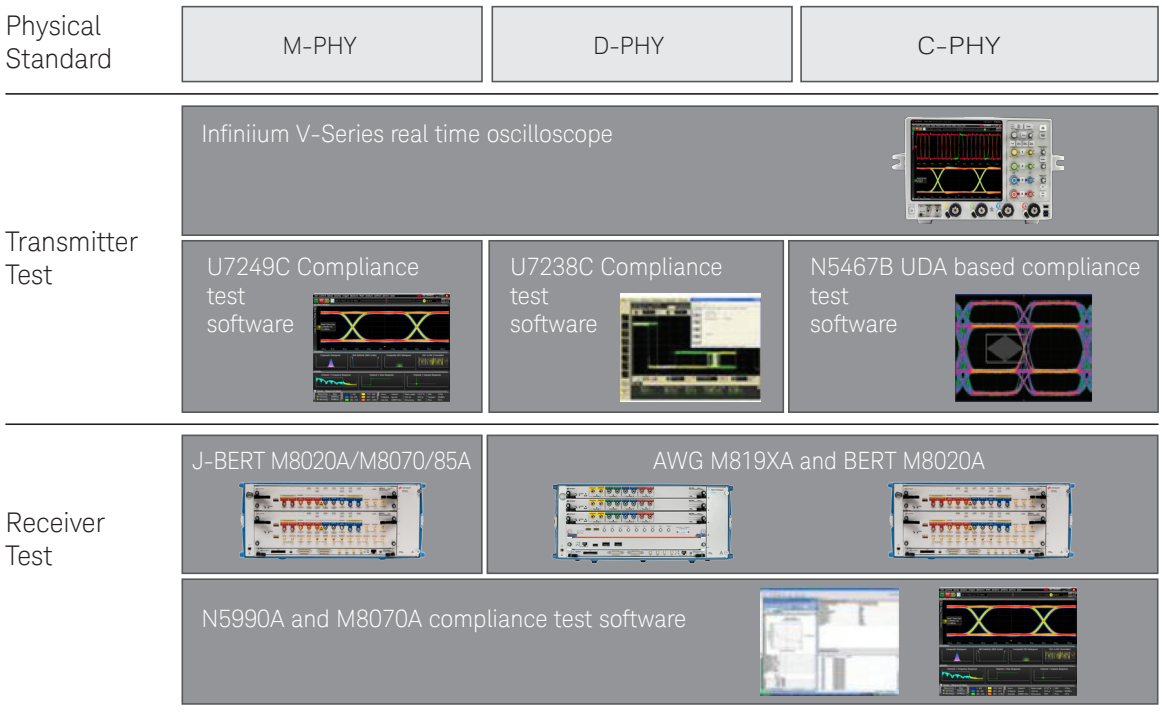
The MIPI Alliance provides a set of specialized physical layers with both complementary and unique features to support a wide variety of application protocols requiring high performance, low-power serial interfaces.

Each physical layer offers unique advantages and features that collectively address every important aspect of today's integrated handheld mobile devices.

	PHY Characteristics		
	M-PHY v3.1	**D-PHY v1.2**	**C-PHY v1.0**
Primary use case	Performance driven, bidirectional packet/network oriented interface	Efficient unidirectional streaming interface, with low speed in-band reverse channel	Efficient unidirectional streaming interface, with low speed in-band reverse channel
HS Clocking method	Embedded clock	DDR source-sync clock	Embedded clock
Channel compensation	Equalization	Data skew control relative to clock	Encoding to reduce data toggle rate
Minimum configuration and pins	1 lane per direction, dual-simplex, 2 pins each (4 total)	1 lane plus clock, simplex, 4 pins	1 lane (trio), simplex, 3 pins
Data rate per lane (HS)	HS-G1: 1.25, 1.45 Gb/s HS-G2: 2.5, 2.9 Gb/s HS-G3: 5.0, 5.8 Gb/s HS-G4: 10 Gb/s, 11.6 Gb/s (Line rates are 8b10b encoded)	80 Mbps to 2.5 Gbps	80 Msym/s to 2.5 Gsym/s times 2.28 bits/sym, or max 5.7 Gbps (aggregate)
Data rate per lane (LS)	10kbps – 600 Mbps	Less than 10 Mbps	Less than 10 Mbps
Bandwidth per port (3 or 4 lanes)	~ 4.0 – 18.6 Gb/s (aggregate BW)	Max ~10 Gbps per 4-lane port (aggregate)	Max ~ 17.1 Gbps per 3-lane port (aggregate)
Typical pins per port (3 or 4 lanes)	10 (4 lanes TX, 1 lane RX)	10 (4 lanes, 1 lane clock)	9 (3 lanes)

Table 1. An overview look at the differences in the MIPI PHY layer characteristics.

Complete support M-PHY, D-PHY and C-PHY



With a combination of award winning hardware and automation software Keysight offers a full set of solutions for testing the different physical layers within the MIPI protocol

MIPI M-PHY

M-PHY is an embedded clock serial interface technology with ultra-high bandwidth capabilities, specifically developed for the extreme performance and low power requirements of mobile applications. M-PHY currently supports protocols including; CSI-3, UFS, DigRF, UniPro, LLI, SSIC and M-PCIe. These different protocols cover applications from advanced cameras to high speed memory, where low pin count, lane scalability and power efficiency are paramount requirements.

The high M-PHY data rates as well as multilane testing and the huge list of conformance test requirements make validating the M-PHY layer a challenge. To fully test the functionality of the layer both transmitter (Tx) and receiver (Rx) characterization has to be done and Keysight offers a solution for both.

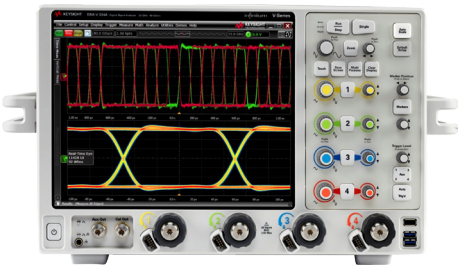
Transmitter validation is checking to see if the device/DUT is sending the signal accurately. An oscilloscope is used to display/show the results. A receiver on the other hand is located at the end of a transmission chain. The signal arriving at its input generally is degraded and carries impurities. These impurities can stem from the associated transmitter or can be picked up on the way from TX to RX. Signal degradation is mainly due to channel loss. The RX's capability to nevertheless detect the digital content properly is characterized during a receiver stress test. For this purpose a test signal is defined, emulating conditions when operating in a real or worst case scenario. A Bit Error Ratio Tester (BERT) is commonly used for RX testing. It consists of a Pattern Generator (PG) and an Error Detector (ED). It allows the user to set up the test signal in application terms, such as data rate, signal amplitude, signal offset, data patterns (such as CJTPat) and in case of the Keysight J-BERTs, jitter components such as Sinusoidal or Random jitter (SJ or RJ).

Characterization of M-PHY Transmitter

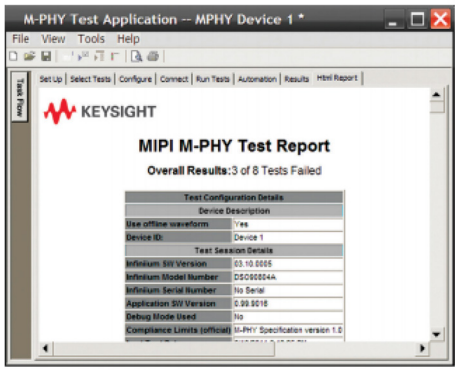
The high data rate is a challenge with gear 4 running, above 10 GHz a real-time oscilloscope over 32 GHz is needed to accurately characterized the edge transitions. In addition to bandwidth the noise floor performance is critical in M-PHY electrical characterization because of the tight amplitude parameters defined in the specification.

The combination of Keysight's best-in-class oscilloscope and InfiniiMax probing technology means you can trigger on and measure all of the signals necessary. Probe noise, response and loading as well as test setup can greatly impact an otherwise successful M-PHY data link. Multi-lane testing can be accomplished with a switch matrix calibrated to remove loss and skew connected to the oscilloscope.

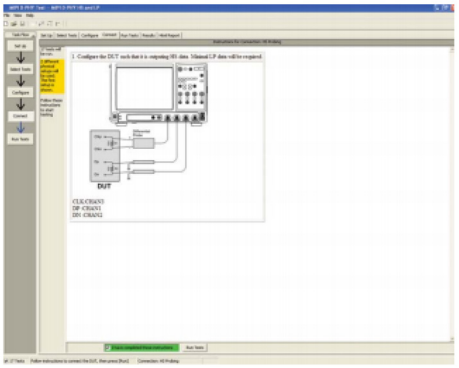
Keysight's U7294C M-PHY conformance test software for Infiniium oscilloscopes is available to provide a fast, easy way to validate and debug your embedded M-PHY data links. The M-PHY electrical test software U7294C allows you to automatically execute M-PHY electrical checklist tests and displays the results in a flexible report format. In addition to the measurement data, the report provides margin analysis that shows how closely your product passed or failed each test.



Keysight Infiniium V-Series provides up to 33 GHz and up to 2 Gpts of memory. It has the lowest noise floor, jitter noise floor and trigger jitter by a real-time oscilloscope in the industry.



Results reports quickly highlight test margins versus specified limits and provide a summary of measurements that pass or fail. A complete HTML-formatted report provides a results summary for documentation and archiving with full detail on measurement definitions referenced to the specification and screen images from the oscilloscope during test.



Guided configuration diagrams provide you with channel and probe configuration needed to properly connect your product and accurately perform tests.

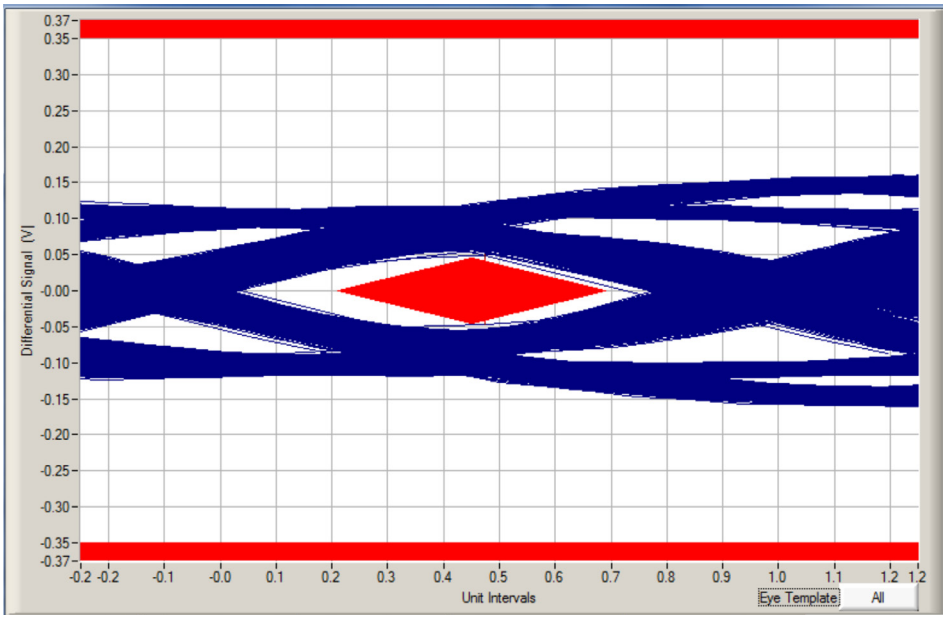
Characterization of M-PHY Receiver

The RX test is done in 3 steps:

1. Calibrate the test signal in the actual test set-up with respect to the specified calibration plane
2. Set the RX under test into an appropriate test mode and stimulate the RX with the calibrated signal (also delivering all necessary aux signals such as ref clock)
3. Check proper detection, i.e. if actual Bit Error Ratio (BER) is less than the target BER

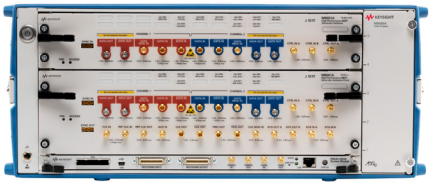
The signal for the RX test is calibrated according to the conformance test suite (CTS). While the first revision for M-PHY gears 1 and 2 defined the stress signal by the exact amounts of the contributing jitter components, we now observe a trend for all PHY specs to use the eye diagram (eye height and eye width (EH and EW) as the finally defining parameters for the stress signal. In gear 4 the calibration plane moved into the ASIC behind built-in equalizers and so it became necessary to include signal simulation (and filter optimization) into the calibration procedure, both of which can be delivered by the SigTest software.

The figure of merit for the final pass-fail decision is the BER. A BERT ED can determine the BER by comparing the data looped back by the RX with the expected data. However, this loop back test mode is not always available, sometimes because of the unidirectional nature of the port (camera or display) or sometimes because the protocol residing on M-PHY does not specify that test mode. In these cases other methods such as reading out built-in bit verifiers or error-packet counters need to be used.

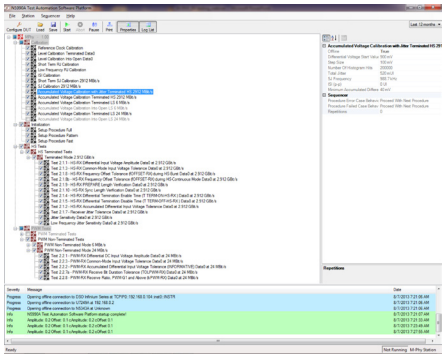


The M8020A makes it easy to add the different kinds of jitter necessary to simulate a stressed signal

The Keysight BERT M8020A and N5990A test automation software together complete the Keysight M-PHY RX test solution.



The Keysight M8020A provides straight forward and unambiguous adjustments of all parameters required to compose the M-PHY RX stress test signal with built-in capabilities such as, jitter and common- and differential-mode interference sources and de-emphasis to emulate the associated TX. Furthermore the built-in reference clock multiplier allows synchronization of the BERT PG with the DUT's reference clock.

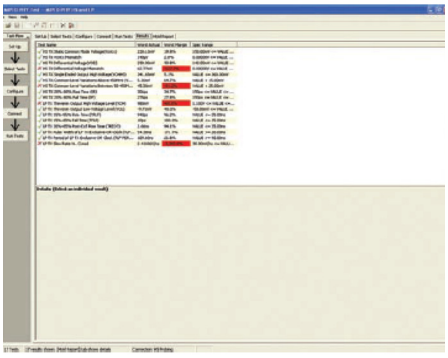


N5990A offers test configuration and automation of the required Rx testing. Simplifying the test complexity and allowing easier handling of the many different tests required to pass conformance according to the CTS. Select and sequence tests from an intuitive tree structure and then evaluate results in a Microsoft Excel format.

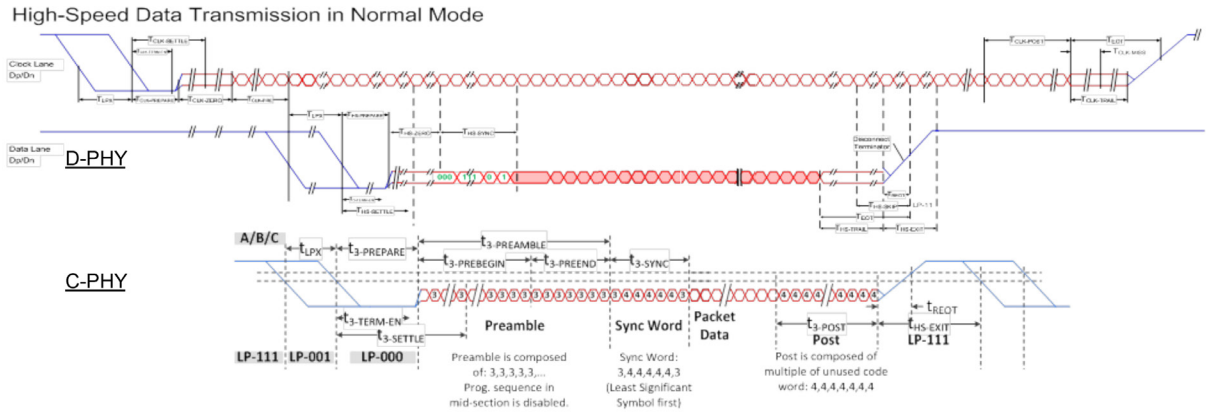
MIPI D-PHY

D-PHY is a PHY layer interface technology for band-limited channels that today is used by streaming applications such as Serial Display Interface (DSI) and Camera Serial Interface (CSI) protocols. It has a multilane architecture enabling scalability. When operating in high speed mode, it uses NRZ data format with differential signaling and source synchronous clocking. The latter allows it to adapt the data transmission rate to match the requirements of the video frame size and rate. By this and the unterminated low power mode, it is very power efficient.

Timing measurements during the transition phase from low power to high speed mode (and vice versa) are emphasized on the D-PHY interface because of the on-off switching of the receiver termination and therefore there are many timing requirements that signals have to meet for the interface to work correctly. Additional challenges of D-PHY testing are the joint presence of low and high speed signals.



Results reports quickly highlight test margins versus specified limits and a summary of measurements that pass/fail or violate the margin warnings you have set.

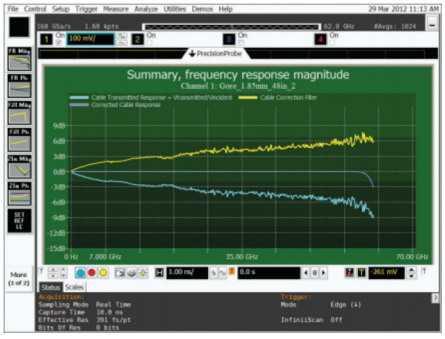


Physical layer timing diagram in transition from low power to high speed for both D-PHY and C-PHY. The signals when compared are very similar with a few exceptions; in naming of transition phases and in HS-mode with different data content. The main difference however is the missing clock in C-PHY, which is embedded / encoded into the data.

Characterization of D-PHY Transmitter

The special D-PHY signal characteristics have implications for Tx testing – notably measuring low-level signals in the neighborhood of high speed signals. Keysight's oscilloscope with low noise and low jitter floor means that you see your signals with the lowest possible jitter contribution from the scope itself. While PrecisionProbe application can characterize and remove the loss of the probe from your measurements.

The Keysight U7238C MIPI D-PHY compliance test software gives a specific D-PHY trigger to debug and test designs with embedded D-PHY data links. The U7238C D-PHY electrical test software allows you to automatically execute D-PHY electrical tests and displays the results in a flexible report format. In addition to the measurement data, the report provides margin analysis that shows how closely your product passed or failed each test.



Example of frequency response correction of a cable using PrecisionProbe

Characterization of D-PHY Receiver

D-PHY signals consist of high speed and low power modes with different signal amplitudes, data rates and formats. High-speed receiver testing is basically stressing set-up and hold time conditions with eye closure due to DDJ and skew between the data and the clock. A classical NRZ BERT PG matches the differential NRZ format of the D-PHY high speed mode and could therefore be used to generate the required test signals when solely this mode is tested. However, testing the transitions between the high speed and low power mode requires seamless switch between the associated amplitudes, data rates and formats. This can best be achieved using an AWG such as the M819xA*, which of

Keysight AWG M819xA can easily switch between amplitudes, data rates and formats according to CTS requirements for D-PHY RX testing. Add the M8070A user interface software to your M819xA to enable a BERT-like and application specific user interface.
* contact the factory for availbility

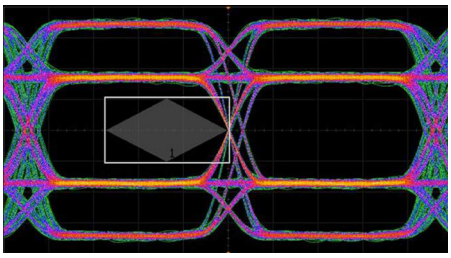
Characterization of D-PHY Receiver (continued)

course can also generate the high speed test signals with the required impairments. The necessary check of proper detection of digital content or just mode switching for D-PHY (and C-PHY, see below) is checked in a different way than for M-PHY; loopback is usually not implemented due to the unidirectional nature of the (camera and display) ports using D-PHY. So in this case the BERT instrument used for RX testing only consists of a BERT-PG (in this case of an AWG-type) while the BERT functionality extends into the DUT (the error detection and counting is performed by the DUT, as described earlier for M-PHY).

MIPI C-PHY

MIPI C-PHY is a serial bus that supports the same display and camera interfaces as D-PHY. The C-PHY data transmission in high speed mode uses a 3 level, 3 wire scheme forming a lane that enables transmission of 2.28 bits per symbol. This allows a higher data rate than D-PHY without increasing the toggle rate and by this the power consumption.

The C-PHY clock is embedded or encoded into the data. This saves two wires and the associated power vs D-PHY. Data encoding makes sure that there is a transition at every symbol boundary, such that a logic (not PLL) based RX clock recovery can be realized, preserving the data rate flexibility of D-PHY. By having the clock embedded into data it furthermore provides flexibility to assign individual lanes in any combination to any port on the application processor via software control. Due to similarities in basic electrical specifications (and the whole low power mode), C-PHY and D-PHY can be implemented on the same device pins.

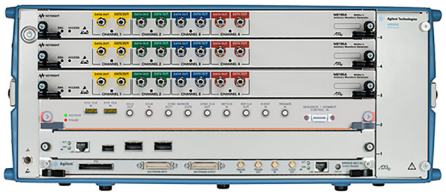


N5467B UDA based, compliance test software for Tx C-PHY testing

Characterization of C-PHY Transmitter

There is a wide range of timings that are different and modified from D-PHY. Eye and jitter measurements are crucial to accurate characterization and with the Keysight Infiniium with a noise floor of just 2.10 mV at 50 mV /div at 33 GHz and jitter measurement floor or 100 fs you get better spectral analysis and more confidence in measurement accuracy including eye diagrams and jitter.

The N5467B User Defined Application (UDA) software provides the critical electrical tests that include amplitude, rise/fall time, common point voltage and eye-diagram for early validation of C-PHY designs. The software also provides the C-PHY specific clock recovery emulating its delay circuit with negative hold time for the sample clock. Many of the earlier mentioned tests need to be done with respect to this C-PHY clock recovery. Upon completion of the test, the software provides a comprehensive test report which includes the screenshots from the tests.

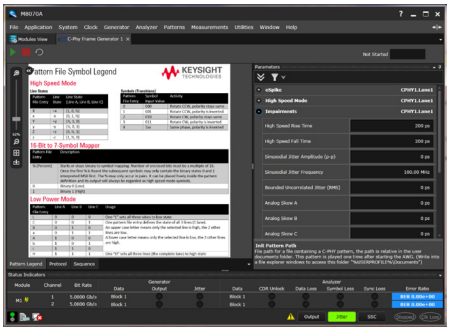


M819xA can be configured for either single lane or multilane C-PHY RX testing.

Characterization of C-PHY Receiver

Doing RX testing for a C-PHY receiver is comparable to D-PHY, however, with its 3-level signaling in high speed mode an AWG is the best choice for a BERT PG.

The Keysight M8000 Series can be configured for support of a wide range of data rates and standards, and provides accurate, reliable results that accelerate your insight into the performance margins of high-speed digital devices. With a combination of AWG, synchronization modules and application specific software you can generate all of the signals necessary with required impairments such as ISI or inter lane skew for single- or multi-lane RX testing for both low power and high speed modes plus transitions between them.



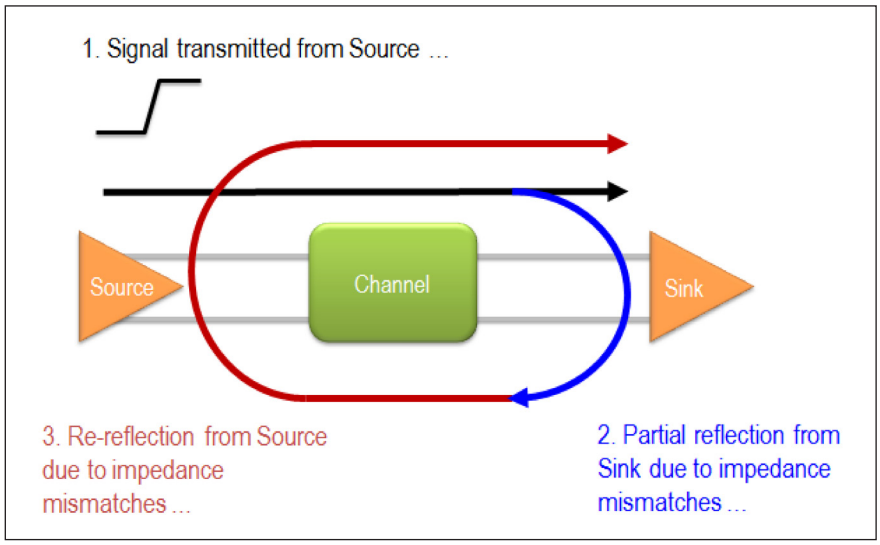
C-PHY editor software enabled in M8070.

PHY Impedance Measurement

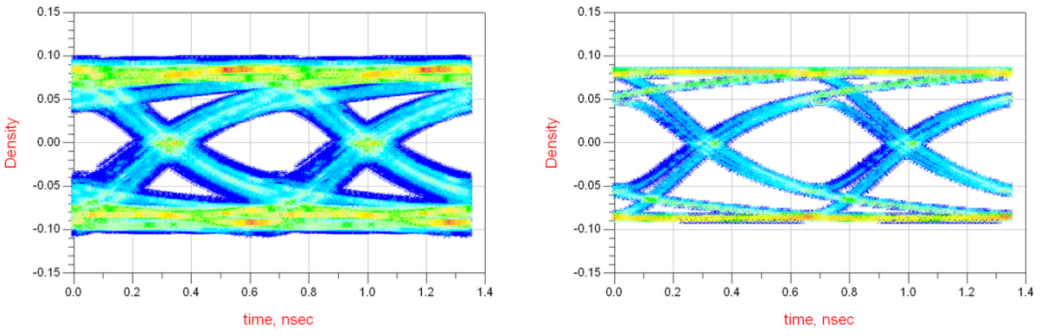
Return loss/channel characterization

There are impedance measurements required for both D-PHY, M-PHY trasmission and reception. Impedance matching is essential in high speed serial applications because signal reflections due to impedance mismatches may have a significant impact on signal integrity.

For transmission measurements, because the device characteristics are different between the power-on state and the power-off state, impedance analysis under actual operation conditions is required. If there is more than one impedance mismatch in the link, multiple reflections occur and degrade signal integrity.



This effect becomes more critical for multi-gigabit systems and accurate impedance matching is essential to maintain signal integrity and open up the eye diagram. The increase in bit rates means that the impedance of active devices must be properly evaluated to provide new insight into signal integrity issues. Signal integrity of interconnects drastically affects system performance at Gb/s data rates. Fast and accurate analysis of interconnect performance in both time and frequency domains becomes critical to ensure reliable system performance.

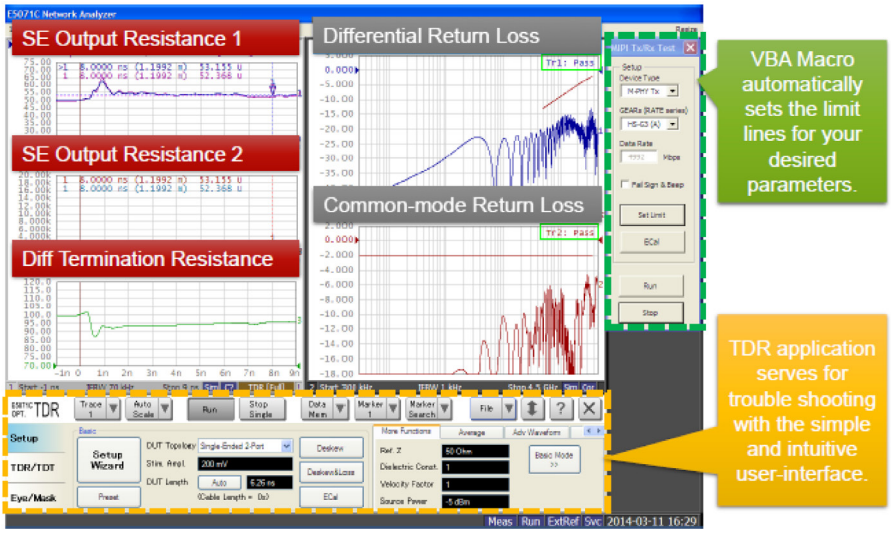


The eye diagrams are simulation results comparing different termination conditions. The eye diagram on the left was computed using the return loss extracted from an actual transmitter which is not impedance matched. The eye diagram on the right was computed assuming a perfectly terminated transmitter. Obviously, the eye diagram on the right has a wider eye opening and verifies that impedance matching of the transmitter can dramatically improve eye opening.

Keysight E5071C ENA Option TDR

The E5071C ENA Option TDR provides you a way to not only make passive component measurement, but to also carry out impdedance analysis of active devices under actual operation conditions. It can also provide you with a solution for detailed high speed interconnect analysis, including time domain, frequency domain, and eye diagram analysis for system integrity and compliance testing.

Measuring the S-parameters and impedance of the channel ensures interoperability and is specificed as part of the standard.

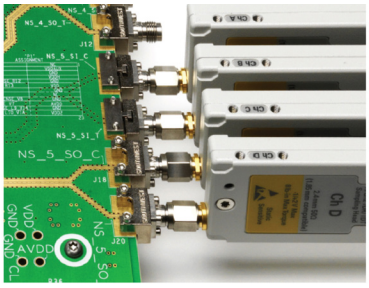


A screen capture from the E5071C ENA option TDR has all measurements in one screen.

DCA 86100D

Another alternative for characterizing the channel in a MIPI system is to use a Keysight DCA 86100D Wideband sampling oscilloscope outfitted with a 54754A or a N1055A TDR/TDT module and 86100D option 202, Enhanced Impedance and S-Parameter software. The 86100D DCA-X mainframe, equipped with a 54754A or N1055A TDR/TDT module and option 202 creates a fully-integrated TDR/TDT/S-parameter measurement system. Electronic calibration (ECal) modules provide fast and accurate calibration with a minimum number of connections and ultra-slim remote heads in the N1055A TDR/TDT module connect directly to the DUT to optimize signal fidelity.

The 86100D with option 202 and the 54754A or N1055A can provide TDR and TDT measurements to characterize your MIPI M-PHY, D-PHY or C-PHY channels using both impedance and S-parameter measurements.

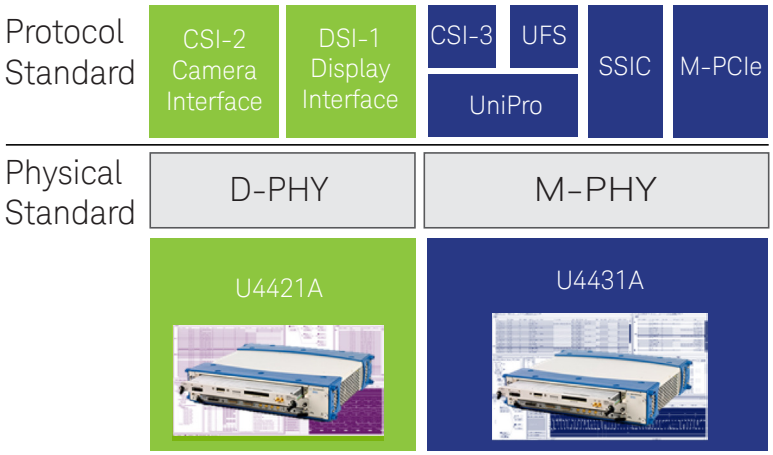


The industry's smallest TDR/TDT remote heads optimize signal fidelity.

Protocol test

Broad and deep insight into your mobile computing designs.

Protocol validation occurs predominately at the interface layer. There are many different protocols supported on the physcial (PHY) layers with the MIPI specifications. Including; CSI-2, DSI-1, DigRF, CSI-3, UFS, UniPro, SSIC, and MPCIe all have different protocol requirements and tests.



Keysight offers support for protocol applications on both D-PHY and M-PHY layers.

See the 'Why' behind your protocol

For both D-PHY and M-PHY protocols there is really a stack between the physical layer and the link layer, and from the transport layer to the high-level application layer. To truly identify where an error might exist it would be nice to be able to 'see into' that stack.

The Keysight Protocol analyzers the U4421A D-PHY and U4431A M-PHY can do just that. With what is called a 'Raw mode' there is visibility to the time-correlated 8b/10b data that underlies each protocol. These states can be displayed as a waveform or listing, providing insight into how a packet is formed at the Physical layer. These views allow you to unravel data as it travels throughout the entire transmission process, and look even deeper by adding time-correlated traces from an Infiniium oscilloscope.

'Raw Mode' in a working system. This system is triggering on any Low Power Data Transition. In the exploded view we see that the captured sequence behaves exactly as expected from the specification.

Protocol standards supported on D-PHY

CS1-2

The Camera Serial Interface 2 specification defines an interface between a camera and a host processor for mobile device applications. CSI-2 provides the mobile industry a standard, robust, scalable, low-power, high-speed, cost-effective interface that supports a wide range of imaging solutions.

DSI

The DSI specification defines a high-speed serial interface between a peripheral, such as an active-matrix display module, and a host processor in a mobile device. By standardizing this interface, components may be developed that provide higher performance, while using lower power and causing less electromagnetic interference.

Protocol standards supported on M-PHY

UniPro

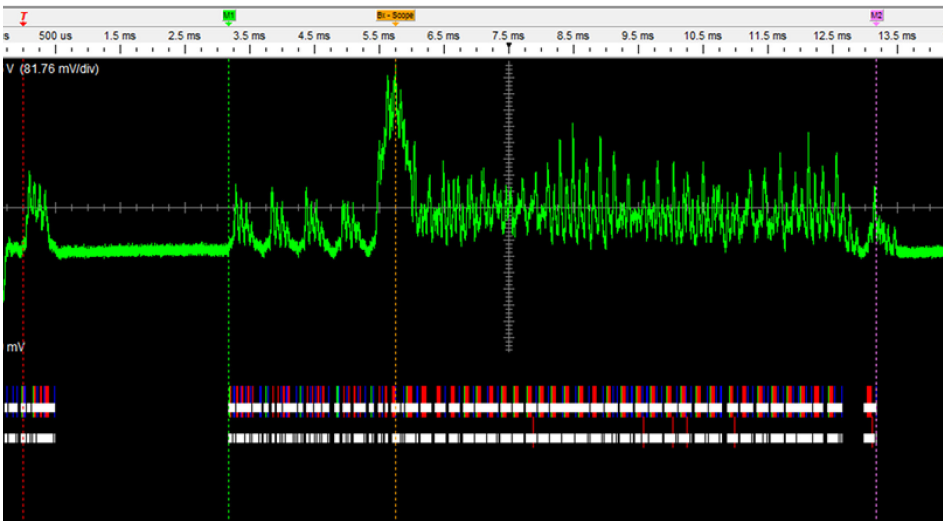
The Unified Protocol (UniPro) v1.6 specification is applicable to a wide range of component types including application processors, co-processors and modems. Target applications for UniPro include wireless handsets, tablets, digital cameras and multi-media devices. UniPro is scalable from single link to full network.

UFS

JEDEC Universal Flash Storage (UFS) standard leverages the MIPI M-PHY and UniPro specifications. To achieve the highest performance and most power efficient data transport, UFS uses the leading industry interface standards to form its Interconnect Layer.

Correlate the physical and protocl layers and gain even more insight into link layers with the following software applications and an Infiniium oscilloscope:	
N8802A CSI-2/DSI	N8818A UFS
N8802A CSI-2/DSI	N8809A LLI
N8807A DigRF/v4	N8819A SSIC
N8808A UniPro	N8820A CSI-3
	N8824A RFFE

Connect the oscilloscope and the protocol analyzer together to get powerful cross trigger capabilities. Enabling the oscillsocope to trigger on errors and protocol packets, correlate markers between the two and even bring the oscillsocope trace into the protocol analyzer to get a deeper understanding of the protocol packets being viewed.



This screen shows the powerful correlation between the oscilloscope and protocol views. On the bottom is a packet burst and above it in green is the analog view from the oscilloscope showing power consumption.

CSI-3

The CSI-3 interface also runs on top of the UniPro specification. It is a standard interface to attach camera subsystems to a host device. It is newer than the CSI-2 interface offering more bandwidth to enable high resolution sensors for digital zoom and increase dynamic range for still images as well as for moving images at high frame rates.

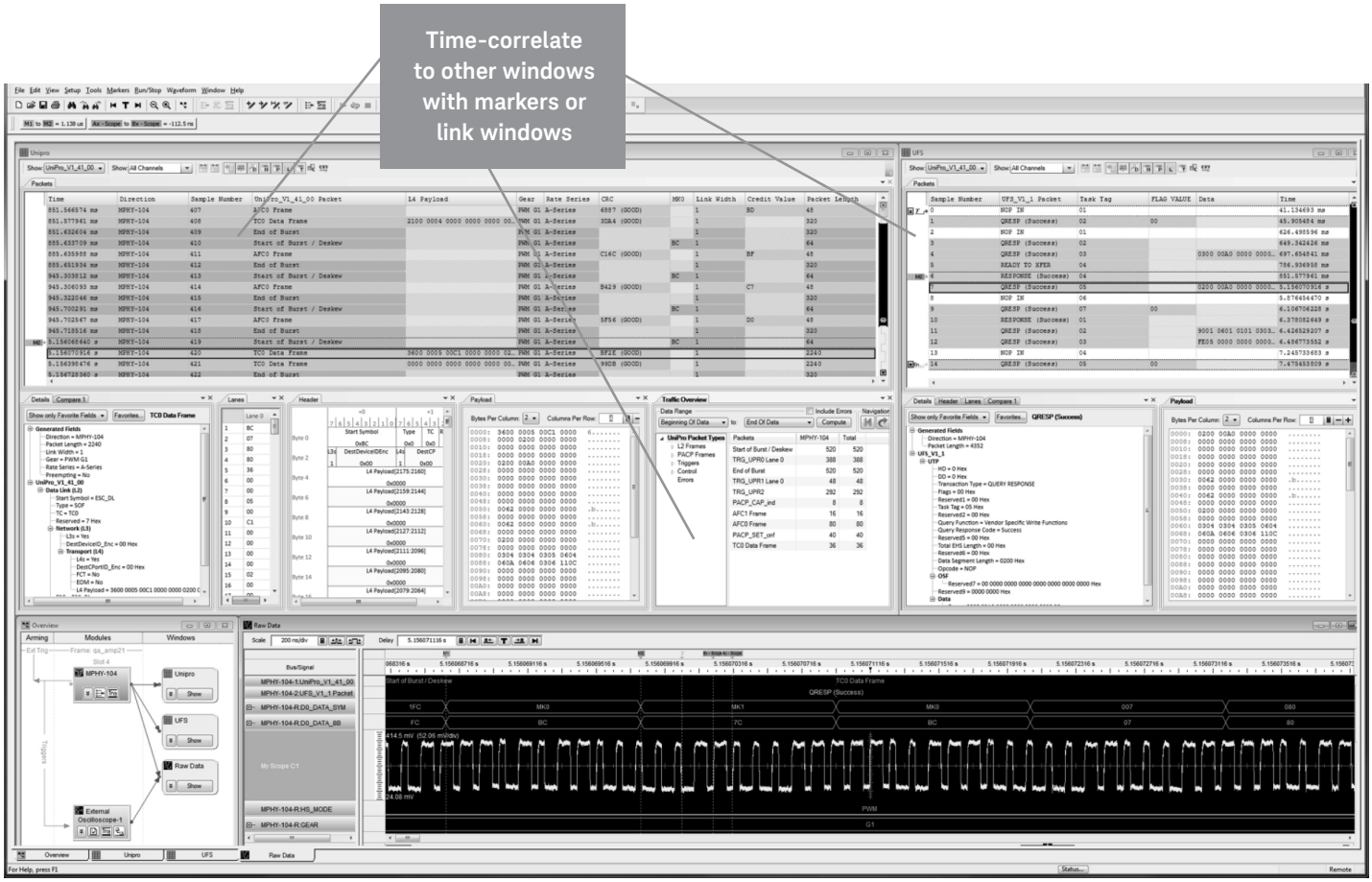
SSIC

SSIC (Super Speed in Chip) is designed to leverage existing USB 3.0 software stack investments, while providing extremely low power consumption for next generation devices. SSIC offers mobile device developers the opportunity to take advantage of USB 3.0's gigabit speeds with minimal power consumption.

M-PCIe

M-PCIe leverages proven M-PHY technology and the broadly adopted standard of PCIe. The EMI-friendly, bandwidth scalable, low-power MIPI M-PHY Physical layer enables device manufacturers to leverage the highest performance and most power efficient data transport interface technology available today.

Get the big picture with analysis tools. The overview tab generates a count of the various types of traffic in any period of time, including errors; then steps through each occurrence with embedded navigation tools. Use global markers to make time and occurrence measurements across all display views. In addition, a user can customize your display in seconds, isolate any packet's header or data as a packet payload, or individual lanes with "peel off" tabs. Adjust data columns like in a spreadsheet – drag and drop columns, double click dividers to resize, right-click to add/delete content.



Link any number of windows together or track correlated events with markers. Any number of filters and views can be applied. Organize them easily in the overview GUI with peel-off tabs and drag-and drop screens. Notice the oscilloscope trace integrated into the view to gain access to some of the analog qualities of the packet under view.

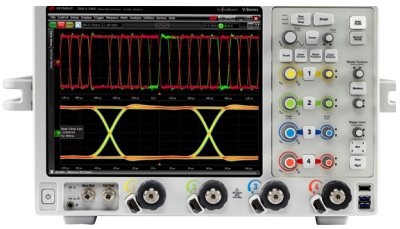
Keysight MIPI solutions

Advanced Design System (ADS)

With a complete set of simulation technologies ranging from frequency-, time-, numeric and physical domain simulation to electromagnetic field simulation, ADS lets you fully characterize and optimize designs. The single, integrated design environment provides system, circuit, and electromagnetic simulators, along with schematic capture, layout, and verification capability - eliminating the stops and starts associated with changing design tools in mid-cycle. **http://www.keysight.com/find/ads**

Infiniium DSAX90000A Series Oscilloscope

The Keysight Infiniium V-Series oscilloscopes deliver the highest performance real-time measurement system available. V-Series offers you the industry's lowest noise floor, jitter measurement floor and highest ENOB, making it the ideal tool for transmitter signal integrity measurements. Models are available from 8 GHz to 33 GHz, and can be upgraded in bandwidth to meet your future needs. Together with the InfiniiMax III and III+ probing systems, they deliver the most accurate measurement and achieve tighter design margins. The U7238C D-PHY and the U7294C M-PHY compliance software applications are available to provide automated testing of MIPI Physical layer attributes. Protocol decode software offers links between the physical and protocol layers.

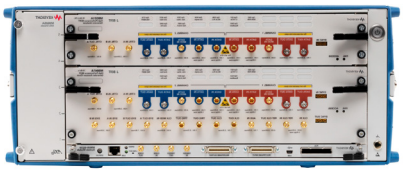


N8802A CSI-2/DSI	N8809A LLI
N8807A DigRF/v4	N8819A SSIC
N8808A UniPro	N8820A CSI-3
N8818A UFS	N8824A RFFE

www.keysight.com/find/V-Series

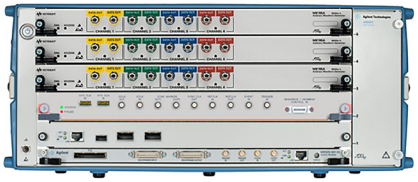
M8020A BERT

The high-performance Keysight J-BERT M8020A enables fast and accurate receiver characterization of single- and multi-lane devices running up to 16 or 32 Gb/s. With today's highest level of integration, the M8020A streamlines your test setup. In addition, automated in- situ calibration of signal conditions ensures accurate and repeatable measurements. And, through interactive link training, it can behave like your DUT's link partner. N5990A software offers automated testing for MIPI applications.
www.keysight.com/find/M8020A

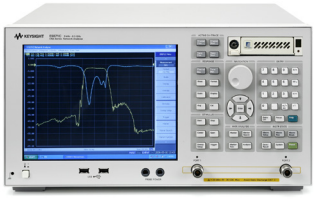


M819xA AWG

The Keysight M8190A is a 12 GSa/s arbitrary waveform generator (AWG) and the M8195A offers 65 GSa/s. They offer great fidelity and deliver high resolution and wide bandwidth simultaneously.
www.keysight.com/find/M8190A
www.keysight.com/find/M8195A
* please contact the factory for all BERT and AWG product configuration questions

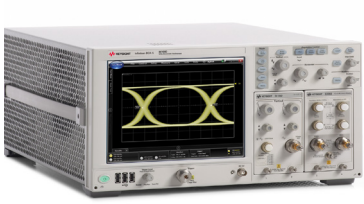


Keysight E5071C ENA Option TDR



The ENA Option TDR provides a one-box solution for high-speed serial interconnect analysis: frequency domain, time domain, and eye diagram analysis is available in a single instrument. By observing both the time and frequency domain response at the same time, you can obtain deeper insight into signal integrity issues. The MOI is a step-by-step measurement procedure guide to support compliance testing for each standard and is provided to give you confidence you're running the right tests. Using the setup files and MOI documents, you can perform compliance tests efficiently with the ENA Option TDR. For more information: **www.keysight.com/find/ena-tdr_compliance**

Keysight DCA 86100D Wideband sampling oscilloscope with N1055A TDR/TDT module



The 86100D Infiniium DCA-X oscilloscope combines high analog bandwidth, low jitter, and low noise performance to accurately characterize optical and electrical designs from 50Mb/s to over 40Gb/s, while the easy to use N1055A 35/50 GHz 2/4 Port TDR/TDT Remote Sampling Head enables high resolution TDR and TDT measurements with fast and accurate mulit-port S-parameters. **http://www.keysight.com/find/dca**

Keysight U4421A MIPI D-PHY Anaylzer and Exerciser

The U4421A MIPI D-PHY Analyzer/Exerciser for CSI-2 and DSI provides deep insight into mobile computing designs. The U4421A MIPI D-PHY Exerciser option for CSI-2 and DSI provides the record length necessary to stimulate designs with high-definition images and video that best simulates traffic from a wide variety of device busses of varying signal performance. **http://www.keysight.com/find/U4421A**

Keysight U4431A MIPI M-PHY Protocol Analyzer

Track multiple M-PHY busses from the PHY to the Application layer with up to Gear 3 HS data rates, 16GB trace depth, 4 data lanes and powerful interface that allows unlimited customization of system views. In addition you can add new protocols and capability at any time after purchase.
http://www.keysight.com/find/U4431A

Related Literature

Publication Title	Publication Type	Publication Number
Advanced Design System	Brochure	5988-3326EN
Keysight Infiniium V-Series Oscilloscopes	Data Sheet	5992-0425EN
U7238A MIPI D-PHY Compliance Test Software for Infiniium Oscilloscopes	Data Sheet	5989-9337EN
U7249A MIPI M-PHY Compliance Test Software for Infiniium Oscilloscopes	Data Sheet	5990-8933EN
Keysight J-BERT M8020A High-Performance BERT Master Your Next Designs	Data Sheet	5991-3647EN
E5071C ENA Network Analyzer	Data Sheet	5989-5479EN
Keysight Infiniium DCA-X 86100D Wide-Bandwidth Oscilloscope Mainframe and Modules	Data Sheet	5990-5824EN
N1055A Remote Head Module 35/50 GHz 2/4 Port TDR/TDT For the 86100D DCA-X Series Oscilloscope Mainframe	Data Sheet	5991-3813EN
Keysight U4421A MIPI D-PHY Protocol Exerciser/Analyzer	Data Sheet	5991-0488EN
Keysight U4431A MIPI M-PHY Protocol Analyzer	Data Sheet	5991-2544EN
Mobile Computing Interfaces Architecture Anticipate Design Challenges– with Keysight MIPI Test Solutions	Poster	5990-9154EN
How to Test a MIPI M-PHY High-Speed Receiver Challenges and Keysight Solutions	Application Note	5991-2848EN
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