Mitigation of Various Power Quality Problems Using Unified Series Shunt Compensator in PSCAD/EMTDC

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***Abstract*—Power quality in the distribution system is the important issue for industrial, commercial and residential applications. An increasing demand for high quality, reliable electrical power and an increasing number of distorting loads have led an increased awareness of power quality both by customers and utilities. This paper deals with the simulation of a Unified Series Shunt Compensator (USSC), which is aimed at mitigating most of the Power Quality problems such as, (i) Voltage Sag compensation, (ii) Voltage Swell compensation, (iii) Voltage Flicker reduction, (iv) Voltage Unbalance mitigation (v) UPS mode of operation and (vi) Harmonics elimination. The modeling and simulation of the USSC has been carried out by using Power Systems Computer Aided Design (PSCAD) software. The USSC simulation model comprises of two 12-pulse inverters which are connected in series and in shunt to the system. A generalized sinusoidal pulse width modulation switching technique has been developed in the proposed controller design for fast control action of the USSC. The USSC has mitigated several Power Quality problems giving better performance.**

Keywords-12-pulse inverters, GTO switches, Power quality, PWM technique, Unified Series Shunt Compensator.

I. INTRODUCTION

Now a days, the high quality of electric power has become very much importance to electric utilities and for customers. Utility and customer-side disturbances result in terminal voltage fluctuations, transients, and waveform distortions on the electric grid resulting in power quality problems. Power Quality is mainly affected by the increased use of non-linear loads such as power electronic equipment, variable speed drives, electronic control gears etc. Poor power quality can affect the safe, reliable and efficient operation of the equipment. Various aspects of power quality are voltage sag, voltage swell, voltage fluctuations, voltage unbalance, harmonics etc [1], [2].

For power-quality improvement, the development of power electronic devices such as Flexible AC Transmission Systems (FACTS) and custom power devices have introduced an emerging branch of technology providing the power system with versatile new control capabilities [3], [4]. In general, FACTS devices are used in transmission control whereas custom power devices are used for distribution control. Since the introduction of FACTS and custom power concept, devices such as Unified Power Flow Controller (UPFC), Synchronous Static Compensator (STATCOM), Dynamic Voltage Restorer (DVR), solid-state transfer switch, and solid-state fault current limiter are developed for improving power quality and reliability of a system [3], [4]. Advanced control and improved semiconductor switching of these devices have achieved a new era for power-quality mitigation.

Investigations have been carried out to study the effectiveness of these devices in power-quality mitigation such as sag compensation, harmonics elimination, unbalance compensation, reactive power compensation, power-flow control, power factor correction and flicker reduction [5] – [11]. These devices have been developed for mitigating specific power-quality problems. For example, UPFC works well for power-flow control. DVR, which acts as a series compensator, is used for voltage sag compensation. STATCOM, which is a shunt compensator, is used for reactive power and voltage sag compensation.

The STATCOM and DVR are only useful for compensating a particular type of power-quality problem and therefore, it is necessary to develop a new kind of unified series-shunt compensator (USSC) which can mitigate various power-quality problems [12], [13]. By using a unified approach of series-shunt compensators, it is possible to compensate for a variety of power-quality problems in a distribution system including voltage sag compensation, swell compensation, unbalance voltage mitigation and flicker reduction. This paper deals with the modeling and simulation of Unified Series Shunt Compensator and it's effectiveness in mitigating various power quality problems. The simulations are carried out by using Power Systems Computer Aided Design (PSCAD), the most powerful and intuitive CAD software.

The section-II gives the basic configuration of Unified Series Shunt Compensator used for the study. The section III deals with the principle operation of USSC. The section IV gives the simulation circuit diagram of USSC which is developed in PSCAD. The section V describes the shunt and series controllers of USSC. The section VI gives the simulation results obtained by operating USSC under voltage sag, voltage swell, voltage unbalance, voltage flicker, and UPS mode. The harmonic elimination of USSC is also presented.

II. BASIC CONFIGURATION OF USSC

The Unified Series Shunt Compensator is a combination of series and shunt voltage source inverters as shown in Fig. 1. The basic components of the USSC are two 12-pulse voltage source inverters composed of forced commutated power semiconductor switches, typically Gate Turn Off (GTO) thyristor valves. One voltage source inverter is connected in series with the line through a set of series injection transformers, while the other is connected in shunt with the line through a set of shunt transformers. The dc terminals of the two inverters are connected together and their common dc voltage is supported by a capacitor bank.

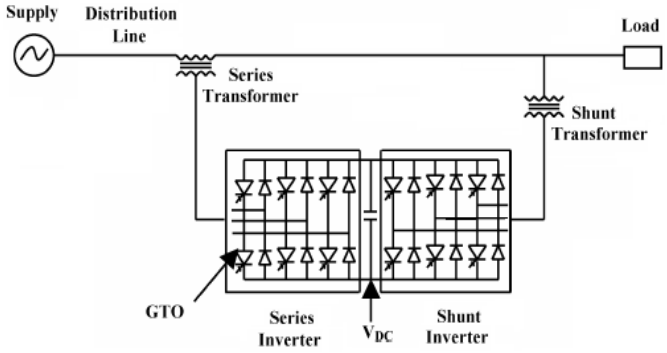

Fig. 1. Basic Configuration of USSC

III. PRINCIPLE OPERATION OF USSC

The principle operation of a USSC is described by referring to the model shown in Fig. 2. The series connected inverter injects a voltage V_{dq} in series with the distribution line, which in turn changes the voltage V_L across the distribution line, hence changing the current and the power flow through the distribution line. The exchange of real power P_{inv} and reactive power Q_{inv} can be written in terms of phase angle Φ (the angle between the injected voltage V_{dq} and the line current I_L), the injected voltage V_{dq} and the line current I, as

$$P_{inv} = V_{dq} I_L \cos\varphi \quad (1)$$

$$Q_{inv} = V_{dq} I_L \sin\varphi \quad (2)$$

The current injected by the shunt inverter has a real or direct component I_d, which can be in phase or in opposite phase with the line and a reactive or quadrature component I_q, which is in quadrature with the line voltage, thereby emulating an inductive or a capacitive reactance at the point of connection with the distribution line. The reactive current can be independently controlled which in turn will regulate the line voltage.

The USSC behaves as an ideal ac-to-ac inverter, in which the exchange of real power at the terminal of one inverter to the terminal of the other inverter is through the common dc link capacitor. The shunt inverter is controlled in such a way as to provide precisely the right amount of real power at its dc terminal to meet the real power needs of the series inverter and to regulate the dc voltage of the dc bus. Thus, real power is absorbed from or delivered to the distribution line through the shunt connected inverter, which injects a current at the point of

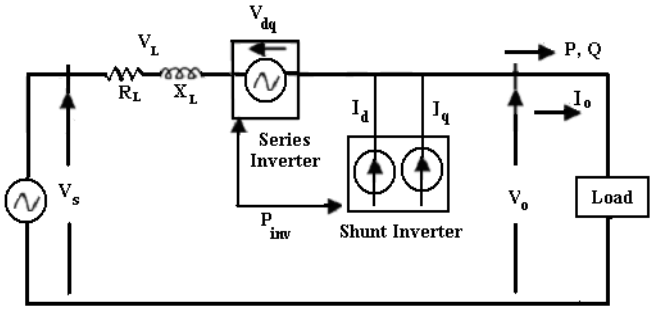

Fig. 2. Principle Operation of USSC

connection. Thus, USSC includes the functions of both series and shunt connected inverters which generates or absorbs reactive power to regulate voltage magnitude and current flow at the ac terminal, respectively.

IV. SIMULATION CIRCUIT DIAGRAM OF USSC DEVELOPED IN PSCAD

The simulation circuit diagram of USSC which has been developed to mitigate various power quality problems is shown in Fig. 3. It consists of 22 kV distribution system having a static load of 5.2 MVA with USSC connected.

The USSC consist of two 12-pulse inverters in which one is connected in series and the other in shunt. The shunt connected inverter is connected to the line by means of two sets of three single- phase transformers which are of Y-Y and Y-Δ configurations to avoid phase shift of other than the order of $12n \pm 1$ harmonics in the secondary of the transformers, which may result in large circulating current due to common core of flux. However, the series connected inverter is connected to the line by means of two sets of three single-phase transformers which are of Y-Δ configuration. This is because, usually Y-connected secondary windings allow only the injection of positive and negative sequence voltages. The delta connection prevents zero sequence currents entering into the system from the inverter. The primary windings of all the single-phase transformers are connected in series in order to avoid harmonic circulating current. The leakage reactance of all the transformers is kept low so as to prevent a large voltage drop. The 22/4.16-kV step-down transformers with a leakage reactance of 0.01 per unit are considered. The capacitor plays an important role in the USSC operation by acting as a dc source to provide reactive power to the load and to regulate the dc voltage. The size of the dc capacitor considered in this simulation is 3340 μF [13].

V. CONTROL SYSTEM OF USSC

The control system of the USSC consists of a shunt inverter controller and a series inverter controller. The shunt inverter controller controls the current injected into the line and whereas the series controller controls the series voltage injected into the line. When the series and the shunt connected inverters operate as stand-alone devices, they exchange almost exclusively reactive power at their terminals. The series connected inverter injects a voltage in quadrature with the line current thereby emulating an inductive or a capacitive reactance in series with

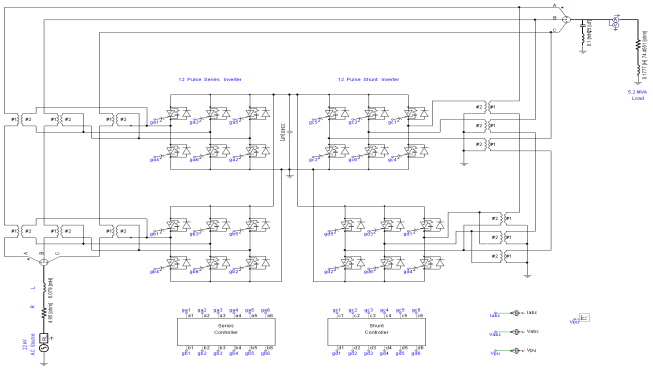

Fig. 3. Simulation circuit diagram of USSC

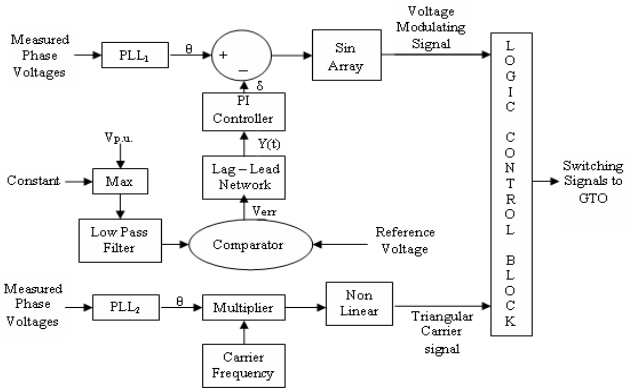

Fig. 4. Simplified block diagram of Shunt Inverter Control System

the line. The shunt connected inverter injects a reactive current, thereby also emulating a reactance at the point of connection. While operating both series and shunt-connected inverters together as a USSC, the series injected voltage can be at any angle with respect to the line current. The exchange of real power flow can be between the terminals of series and shunt connected inverters through the common dc link capacitor.

A. Shunt Inverter Controller of USSC

The controller of a shunt inverter is used to operate the voltage source inverter such a way that the phase angle between the inverter voltage and the line voltage is dramatically adjusted so that the shunt inverter generates or absorbs reactive power at the point of connection of the system. Fig. 4 shows the simplified block diagram of shunt inverter control system using Sinusoidal Pulse Width Modulated (SPWM) switching.

The measured three-phase voltages are fed to the Phase Locked Loop (PLL_1), which provides the voltage synchronizing signal with an angle θ. The reference and measured voltages are compared and processed through lag-lead network and PI controller to generate angle order δ which is combined with θ to generate voltage modulating signal.

The Phase Locked Loop (PLL_2), also provides a voltage synchronizing signal which is multiplied by a carrier frequency of 1.65 kHz and is passed through non-linear block to generate triangular carrier signal. In the SPWM technique, the triangular carrier signal is compared with the voltage-modulating signal so as to obtain the firing signals of the GTOs. The zero crossings of the voltage ramps fire/block the GTOs, depending on the displacement angle δ. If $\delta = 0$, the shunt inverter output voltage is said to be in phase with the ac system voltage. However, if there is an error between the reference voltage and the system voltage in per unit, that is, $V_{p.u} < V_{ref}$, then the displacement angle $\delta > 0$ and the shunt inverter voltage lags behind the ac system voltage thus causing real power flow into the shunt inverter. Consequently, the dc capacitor voltage will increase, thus causing an increase in the ac output voltage of the shunt inverter. The increase in ac output voltage causes a reduction in the error voltage until $V_{p.u} = V_{ref}$. If $V_{p.u} > V_{ref}$, then the displacement angle $\delta < 0$ and the shunt inverter voltage leads the ac voltage thus causing real power flow into the system. Consequently, the dc capacitor voltage will decrease, thus causing a decrease in the ac output voltage of the shunt inverter and a reduction in the error voltage until $V_{p.u} = V_{ref}$.

B. Series Inverter Controller of USSC

In the series inverter, the SPWM technique is also used to control the magnitude and phase of the ac voltage by synchronizing the GTO's switching to the ac system voltages. The control for the series inverter is almost similar to that of the shunt inverter, but the only difference is that, the measured phase currents are input to the PLL. The series inverter injected voltages are kept in quadrature with the line currents to provide series compensation, whereas in the shunt inverter injected currents are kept in quadrature with the line voltage.

VI. SIMULATION RESULTS

Simulations were carried out on USSC to illustrate it's effectiveness in compensation for voltage sag, voltage swell, voltage unbalance, voltage flicker, and UPS mode of operation. The harmonic elimination of USSC is also presented.

A. Voltage Sag Compensation

Voltage sag condition is simulated by creating a balanced three phase to ground fault at time t = 1 s for a duration of 0.75 s. For the system without the USSC, the load voltage drops from 0.9 p.u. to 0.5 p.u., as shown in Fig. 5(a). For the system with the USSC connected, the load voltage increases from 0.50 to 1.0 p.u., as shown in Fig. 5(b). The minimum and maximum voltage values obtained at the starting and ending of voltage sag are 0.91 and 1.1 p.u., respectively. Thus it can be seen from the simulation results that the USSC show a better voltage sag compensation capability in terms of the voltage magnitudes.

B. Voltage Swell Compensation

Voltage swell is generated by connecting a capacitive load to the line by switching on the breaker at time t = 1 s and is switched off at time t = 1.75 s. For the system without the USSC, the load voltage increases from 0.9 to 1.3 p.u. due to the energization of the capacitor, as shown in Fig. 6(a). For the system with the USSC connected, the load voltage is decreased from 1.3 p.u. to the rated value 1.0 p.u., as shown in Fig. 6(b). The minimum and maximum voltages values at the starting and ending of voltage swell are 0.94 p.u. and 1.07 p.u., respectively. Thus it can be seen from the simulation results that the USSC show a better voltage swell compensation capability in terms of the voltage magnitudes.

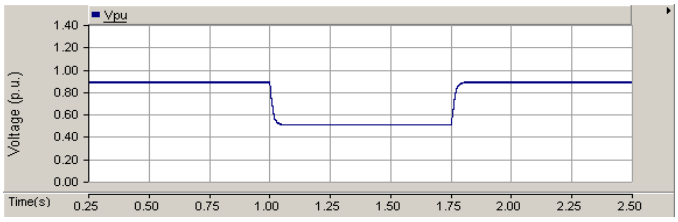

Fig. 5(a). Load Voltage during Voltage Sag without USSC

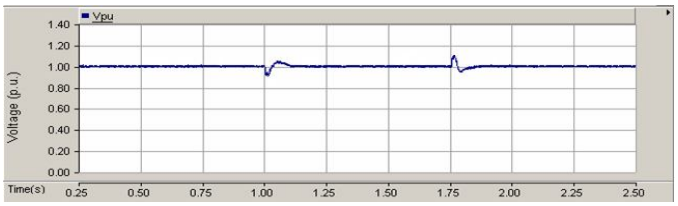

Fig. 5(b). Load Voltage during Voltage Sag with USSC

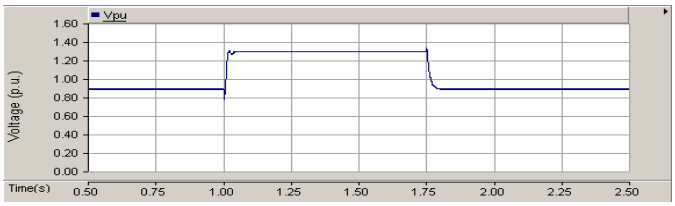

Fig. 6(a). Load Voltage during Voltage Swell without USSC

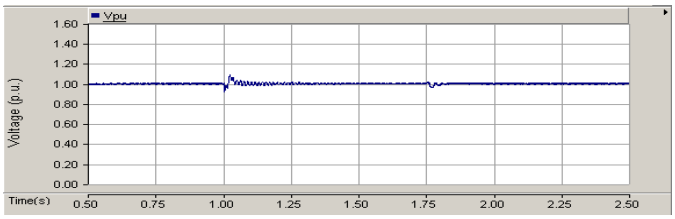

Fig. 6(b). Load Voltage during Voltage Swell with USSC

C. Voltage Unbalance Mitigation

The effect of voltage unbalance is detrimental as it causes heating in motors, thus requiring them to be derated. Unbalance can also affect sensitive single phase loads because it creates under voltage in one or more of the lines. Therefore, it is important to investigate on whether the USSC can mitigate voltage unbalance. Unbalanced voltage conditions are created by applying a single LG fault and two LG faults.

(i) Single LG fault: A Single phase to ground fault on the phase A is created at time t = 1 s for a fault duration of 100 ms. Fig. 7(a) shows the simulation results of the three-phase unbalanced voltages for the system without the USSC connected. It can be seen that during the fault condition, the maximum phase voltages are, V_{Amax}=12.25 kV, V_{Bmax}=16 kV and V_{Cmax}=16 kV. The percentage of voltage unbalance is 16.94%. This value is above the voltage unbalance limit of 2%. With the USSC connected in the system, the three-phase load voltages are obtained as shown in Fig. 7(b) with the maximum phase voltages of, V_{Amax}=17.7 kV, V_{Bmax}=18.2 kV and V_{Cmax}=18 kV. It is evident from Fig. 7(b) that in the presence of the USSC, the load voltage profile has improved and the percentage of voltage unbalance decreases from 16.94 % to 1.48 %.

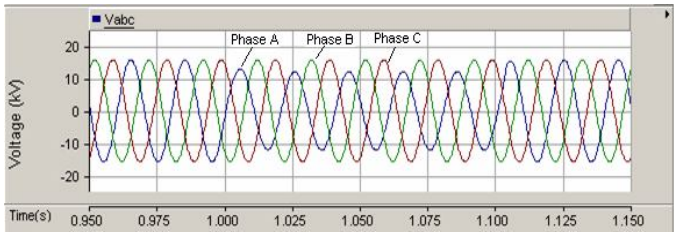

Fig. 7(a). Three Phase Load Voltages during Voltage Unbalance caused by LG fault without USSC connected

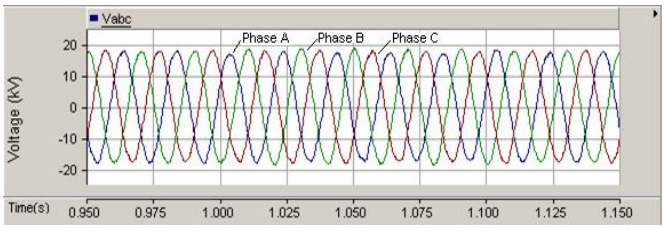

Fig. 7(b). Three Phase Load Voltages during Voltage Unbalance caused by LG fault with USSC connected

(ii) Two LG faults: Two single phase to ground faults of different severity on the phases A and C are applied at time t = 1 s for a fault duration of 100 ms. Fig. 8(a) shows the simulation results of the three-phase unbalanced voltages for the system without the USSC connected. It can be seen that during the fault condition, the maximum phase voltages are, V_{Amax}=12.25 kV, V_{Bmax}=16 kV and V_{Cmax}=9.5 kV. The percentage of voltage unbalance is 27.15 %. This value indicates that the voltage unbalance is severe during the fault because the limit of the voltage unbalance is specified as 2%.

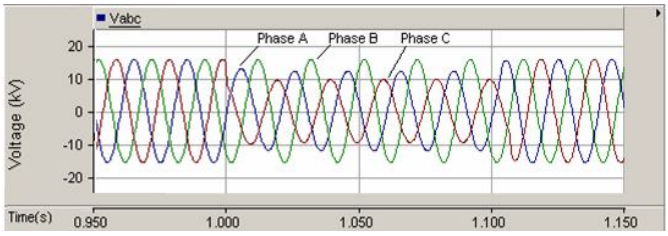

Fig. 8(a). Three Phase Load Voltages during Voltage Unbalance caused by two LG faults without USSC connected

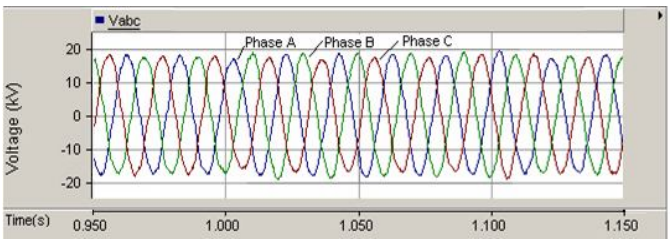

Fig. 8(b). Three Phase Load Voltages during Voltage Unbalance caused by two LG faults with USSC connected

With the USSC connected in the system, the three-phase load voltages are obtained as shown in Fig. 8(b) and the maximum phase voltages are, V_{Amax}= 18.13 kV, V_{Bmax}=18.5 kV and V_{Cmax}= 17.8 kV. It is evident from Fig. 8(b) that in the presence of the USSC, the load voltage profile has improved in which the phase A and C voltages are increased and the phase B voltage is reduced, thus making the three phase voltages more balanced. The percentage of voltage unbalance decreases from 27.15 % to 1.892%.

D. Voltage Flicker Reduction

Voltage flicker is a phenomenon of annoying light intensity fluctuation caused by variable electric loads and arc furnaces have been a major power-quality concern. To illustrate the use of the USSC in reducing voltage flicker, simulations were carried out by connecting a variable electric load of 5.2 MVA, 22 kV as the source of voltage flicker.

Fig. 9(a) shows the flicker effect of a phase A voltage for the system without the USSC connected. By connecting the USSC, it can be seen that the voltage of phase A is flicker free, as shown in Fig. 9(b). The results shown here are for the phase A voltage but however the responses are similar for the phase B and phase C voltages.

The simulation results show that without the USSC connected, the effect of the variable electric load results in a voltage flicker index of 0.321 in which the value exceeds its IEEE SCC22 standard limit of 0.07. However, with the USSC connected, it is noted that the calculated voltage flicker index is reduced to 0.013.

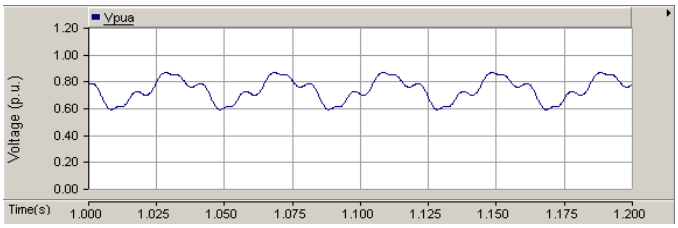

Fig. 9(a). Load Voltage during Voltage Flicker without USSC

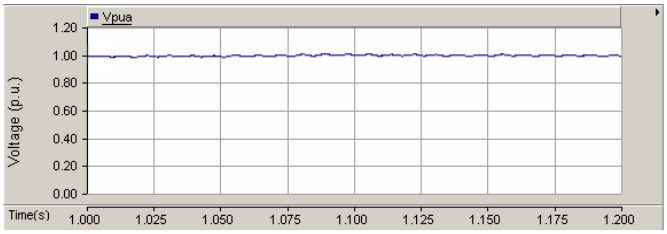

Fig. 9(b). Load Voltage during Voltage Flicker with USSC

E. UPS Mode of Operation

To operate the USSC in Uninterruptible Power Supply (UPS) mode, an outage is first created by applying a three phase fault at time t = 1 s for a duration of 0.75 s. A DC source is connected to the common DC bus to function as an energy source for UPS operation to supply real power to the load. The outage simulation result is as shown in Fig. 10(a).

When the USSC is connected in the system, the USSC recovers the load voltage from 0.0 to 1.0 p.u. within a short time as shown in Fig. 10(b). In the UPS mode, both the series and shunt inverters of the USSC operate in parallel and support a load of the sum of the inverters rating.

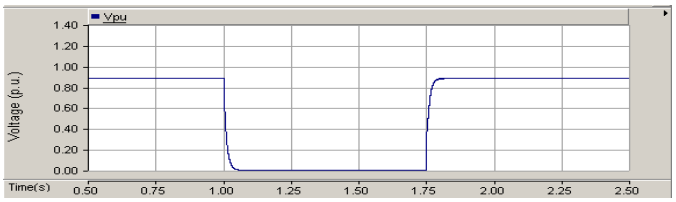

Fig. 10(a). Load Voltage during Outage without USSC

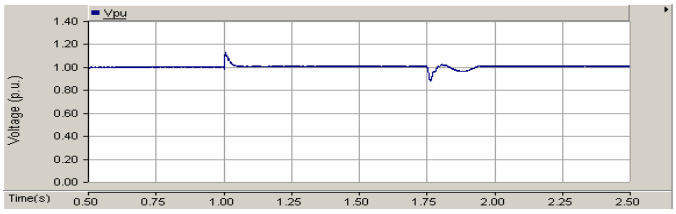

Fig. 10(b). Load Voltage during Outage with USSC

F. Harmonic Elimination of USSC

Due to high frequency switching losses, the inverters have generated a voltage Total Harmonic Distortion (THD) of about in the range of 45% to 60% as shown in Fig. 11(a). This value is higher than the acceptable level of 5%. Therefore, an inductance-capacitance (LC) passive filter is connected at the load side of distribution system in order to eliminate harmonics. The filter parameters used are L = 0.1 mH and C = 25 µF. Simulations were carried out and the THD of the system without and with the filter inserted into the system recorded are as shown in Fig. 11(a) and 11(b), respectively.

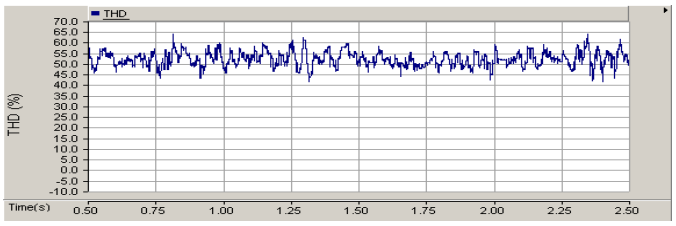

Fig. 11(a). Total Harmonic Distortion without Filter

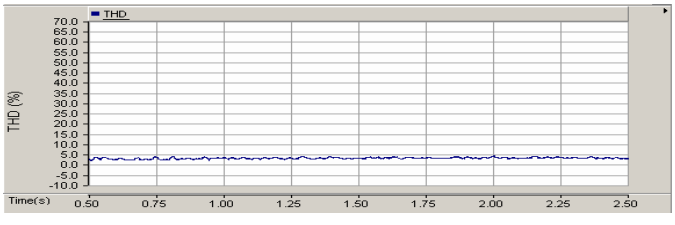

Fig. 11(b). Total Harmonic Distortion with Filter

From the simulation results, it can be seen that with the filter connected, the harmonics are suppressed and the THD of the

system is reduced to about 3 to 4% which is below the value of the IEEE standard THD limit of 5%. The three phase load voltages without and with filter connected into the system is shown in Fig. 12(a) and Fig. 12(b) respectively. From the figures, it is clear that the distortions in the voltage waveforms due to the harmonics generated by the USSC have been reduced by connecting a passive filter into the system.

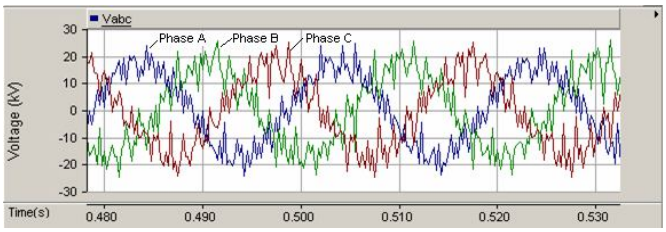

Fig. 12(a). Three Phase Load Voltages without Filter

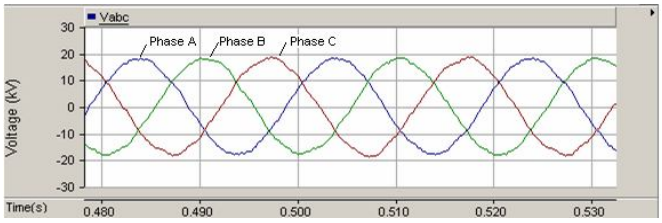

Fig. 12(b). Three Phase Load Voltages with Filter

CONCLUSIONS

The Unified Series Shunt Compensator incorporating 12-pulse series and shunt connected inverters with SPWM based control scheme has been modeled using the PSCAD software package. Simulations have been carried out on USSC to evaluate its performance in mitigating various power quality problems.

The USSC has effectively compensated the voltage sag of 0.5 p.u. for a duration of 0.75 s by maintaining the load voltage at 1 p.u. through out the duration with maximum and minimum voltages of 1.1 p.u. and 0.91 p.u. at starting and ending of the sag respectively. The voltage swell of 1.3 p.u. for duration of 0.75 s has been reduced to the rated voltage 1 p.u. by using USSC in the system with maximum and minimum voltages of 1.07 and 0.94 respectively during starting and ending of the voltage swell. The unbalance in the three phase voltages has been reduced to below the voltage unbalance limit of 2%. The voltage flicker generated by the variable electric load has been reduced from 0.321 to 0.013 which is below the voltage flicker index limit of 0.07 by connecting the USSC to the system. The USSC has operated in UPS mode during an outage for a period of 0.75 s, supplying power to the load and retaining the rated voltage. It was also observed that the harmonics generated by the USSC has been significantly reduced to below 5% from about 60% by inserting a passive LC filter into the system.

Thus, it is observed that the USSC has responded well in mitigating voltage sag, voltage swell, voltage unbalance, voltage flicker, UPS mode of operation for improvement of power quality in distribution system.

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