MODULAR MULTILEVEL CONVERTER WITH EMBEDDED BATTERY CELLS FOR TRACTION DRIVES

by MAHRAN QURAAN

A thesis submitted to the

University of Birmingham

for the degree of

DOCTOR OF PHILOSOPHY

School of Electronic, Electrical and Systems Engineering

University of Birmingham

April 2016

Abstract

This thesis proposes a new modular multilevel converter with embedded cell balancing for battery electric vehicles. In this topology, the battery cells are directly connected to the half-bridge choppers of the sub-modules, allowing the highest flexibility for the discharge and recharge of each individual cell. The traditional battery management system is replaced by the control of the converter, which individually balances all the cells. A new balancing algorithm is presented and discussed in the thesis, showing that the converter generates symmetric three-phase voltages with low harmonic distortion even for significantly unbalanced cells. The thesis also analyses stationary recharge of the battery cells from both three-phase and single-phase ac sources.

The performance of the converter as a traction drive is assessed in terms of torque-speed characteristic and power losses for the full frequency range, including field weakening. A simplified model for estimating conduction and switching losses for the proposed modular multilevel converter is presented and the results for a typical driving cycle are compared with a traditional two-level converter. Simulation and experimental results on a kW-size prototype have confirmed the feasibility of the proposed traction modular converter in terms of effectiveness of the cell balancing control, validity of the proposed loss model, suitability of use for traction and effectiveness of recharging operations.

***Index Terms*--Battery electric vehicles, modular multilevel converters, state of charge balancing, traction drives, battery charger, switching losses, conduction losses**.

Acknowledgements

My deep gratitude goes first to my supervisor Dr. Pietro Tricoli for his constant support, advice and encouragement over the three years. I am very grateful for his patience, motivation, enthusiasm, and immense knowledge.

I would like to thank Dr. Stuart Hillmansen with high respect and deep sense of appreciation for his unwavering support, collegiality, and mentorship throughout this research.

My sincere thank also goes to Prof. Clive Roberts who provided me an opportunity to carry out my research at Birmingham Centre for Railway Research and Education.

I would like also to say thank you to Dr. Wael Hashlamoun from Birzeit University, Palestine, for his unconditional support and advice.

Special thank to Mrs. Mary Winkles in the postgraduate office for her great help and support.

So many wonderful people have also supported me through this PhD project based on their research experience. I would like to specifically thank:

- Dr. Paul Weston, *University of Birmingham, UK*
- Mr. Louis Saade, *University of Birmingham, UK*
- Dr. Mani Entezami, *University of Birmingham, UK*
- Dr. Hamed Rowshandel, *University of Birmingham, UK*
- Mr. Adnan Zentani, *University of Birmingham, UK*
- Prof. Luigi Piegari, *Politecnico di Milano, Italy*
- Dr. Salvatore D'Arco, *SINTEF Energy Research, Norway*
- Prof. Barry Williams, *University of Strathclyde, UK*
- Prof. Graham Ault, *University of Strathclyde, UK*
- Dr Campbell Booth, *University of Strathclyde, UK*
- Dr. Muhammad Abu-Khaizaran, *Birzeit University, Palestine*
- Dr. Wasfi Kafri, *Birzeit University, Palestine*

This project was supported by Samsung Advanced Institute of Technology under the Global Research Outreach Program 2012, Palestinian Telecommunication Group (PalTel), and the University of Birmingham. I gratefully acknowledge the funding received from them.

Finally, I would like to thank my parents, brothers, sister, and wife for their love, patience, understanding, and encouragement in every possible way.

Contents

Acronyms and Abbreviations

ADC	Analogue to Digital Converter
BBC	Buck/Boost Converter
BEV	Battery Electric Vehicle
BMS	Battery Management System
CC	Ćuk Converter
CCM	Continuous Conduction Mode
CD-SPWM	Carrier Disposition-Sinusoidal Pulse Width Modulation
CD-THISPWM	Carrier Disposition-Third Harmonic Injection Sinusoidal Pulse Width Modulation
CHB	Cascaded H-Bridge
DCM	Discontinuous Conduction Mode
DCVM	Discontinuous Capacitor Voltage Mode
DSHB	Double-Star Half-Bridge
DTSC	Double-Tiered Switched Capacitor
EMI	Electromagnetic Interference
EUDC	Extra-Urban Driving Cycle
EV	Electric Vehicle
FbC	Flyback Converter
FBC	Full-Bridge Converter
FPGA	Field Programmable Gate Array
FSR	Fixed Shunt Resistor
HEV	Hybrid Electric Vehicle

ILED	Infrared Light-Emitting Diode
MMC	Modular Multilevel Converter
MosFET	Metal-Oxide-Semiconductor Field Effected Transistor
MpT	Multiple Transformers
MSC	Modularized Switched Capacitor
MSI	Multi Switched Inductor
MWT	Multi Winding Transformer
NEDC	New European Driving Cycle
NEMA	National Electrical Manufacturers Association
NPC	Neutral Point Clamping
OCV	Open Circuit Voltage
PHEV	Plug-in Hybrid Electric Vehicle
PLL	Phase Locked Loop
PSC-SPWM	Phase Shifted Carrier- Sinusoidal Pulse Width Modulation
PWM	Pulse Width Modulation
QRC	Quasi-Resonant Converter
RC	Ramp Converter
RT	Real Time
SC	Switched Capacitor
SLR	Series Loaded Resonant
SM	Sub-Module
SOC	State of Charge
SSC	Single Switched Capacitor

SSI	Single Switched Inductor
SSR	Switched Shunt Resistor
SWT	Single Winding Transformer
THD	Third Harmonic Distortion
TMS	Thermal Management System
UDC	Urban Driving Cycle
ZCQR	Zero-Current Quasi-Resonant
ZCS	Zero Current Switching
ZVQR	Zero-Voltage Quasi-Resonant
ZVS	Zero Voltage Switching

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Chapter 1

Introduction

In September 2009, both the European Union and G8 leaders agreed to cut CO_2 emissions by 80% by 2050 to keep global warming below the safe level of 2°C. But 80% reduction of carbon footprint by 2050 may require 95% curtailment of emissions from the road transport sector. With the number of passenger cars set to rise to 273 million in Europe by 2050, decarbonising road transport may not be achievable only by means of improvements to traditional internal combustion engines or introduction of alternative fuels. It is therefore vital to bring to market new technologies that will ensure long-term sustainability of mobility in Europe and all over the world. Electrical vehicles (EVs) are attractive alternatives to conventional petrol and diesel internal combustion engine counterparts because they produce zero emissions at the exhaust pipe. However, they are limited by the short range due to the limited amount of energy stored in the electrochemical batteries. The diffusion of EVs could be significantly improved with a better use of the available energy, and this could be achieved making the power conversion system more and more light, compact, flexible and reliable. This work tackles this problem by introducing a new converter topology that enables a better exploitation of battery cells and improve the efficiency of the power conversion system [1].

1.1 Problem statement

At present, the standard power conversion system of a battery powered EV is constituted by a battery pack feeding a conventional two-level inverter [2], [3]. The battery pack is formed by

a large number of low voltage electrochemical cells connected in series to meet the voltage requirement of the inverter dc-link. This solution is simple and consolidated in power electronics applications, but presents many drawbacks. The series connection implies that the current is always the same for all battery cells and, hence, voltage imbalance between the cells appears when the battery is charged or discharged several times, because of the differences in leakage currents and chemical characteristics; this results in a progressive damage of battery cells and reduction of their service life time [4]. For this reason, battery management systems (BMSs) are normally added to the battery pack to balance the battery cells [4]. However, BMSs consume energy from the batteries and this reduces the conversion efficiency and the vehicle range. Moreover, the recharge of the battery pack requires an additional built-in charger and the harmonic content of the inverter output waveforms is not low enough to avoid the need for filters. Additionally, if there is a fault in one of the semiconductor devices, the functionality of the inverter is compromised and the vehicle must stop for maintenance. As a result, the unbalancing due to series connection of several batteries, the high stress of semiconductor devices and the reduced converter's reliability are all factors that limit the attraction of customers to EV and, consequently, their penetration into the market.

Multilevel inverters have the potential to improve the performance of the traction systems of EVs as well as their conversion efficiency. Multilevel converters generate ac waveforms from small voltage steps by either using isolated dc sources or dividing the voltage across the dc link. The small voltage steps yield waveforms with low harmonic distortion as well as low voltage gradients [5], [6]. The advantages of multilevel converters compared to conventional two-level converters have been well-known for many years. For EVs, cascaded H-bridges (CHBs) multilevel inverters can be used to drive the traction motor from several battery packs,

allowing continuous operations even with the failure of one level of the structure [7]. Nevertheless, problems attributed to the battery pack include variations between cells and exposure to different charge and discharge rates, leading to unequal states of charge (SOC) of batteries within the pack. Over extended cycling, this can cause premature failure of the pack due to the over- or undercharging of individual cells.

A significant improvement to present topologies of multilevel converters could be the modular multilevel converter (MMC) with embedded battery cells, which is proposed by this PhD project. MMCs can be successfully used as traction converters of BEVs due to the modularity of the design, flexibility of the energy management, fault-tolerance capabilities, low total harmonic distortion (THD) of the output waveforms, four-quadrant operations, and low switching frequencies of the devices, which results in reduced switching losses [5], [6]. The proposed MMC has several functions: driving the traction motor and balance the SOC of battery cells both for the discharge and recharge either from dc or ac power sources, single-phase or three-phase.

1.2 Research objectives

This research endeavours to study, design and test a new converter concept with embedded electrochemical cells that achieves very low cell unbalancing without the need for the traditional BMSs and produces a negligible harmonic content of the output currents.

The objectives of the thesis are as follows:

- Design a new MMC with embedded battery cells which can be successfully applied for BEVs with high flexibility of energy management at the same time of energy conversion;

- Demonstrate the operating principle and design the control of the proposed MMC with a detailed mathematical model;
- Design a cell SOC balancing that operates simultaneously with the traction control
- Define the most suitable modulation technique for the proposed converter
- Confirm that the proposed power converter can be used as a traction drive for EVs using numerical simulations on a model of a commercially available city car
- Undertake a thorough analysis of the converter power losses for different operating condition of the EVs.
- Enable stationary recharge from a three-phase source at unity power factor.
- Verify experimentally the proposed MMC on a small scale laboratory prototype

1.3 Publications

Part of the work presented in this thesis has been published in peer-reviewed international journal and proceedings of international conferences:

- M. Quraan, T. Yeo, and P. Tricoli, "Design and control of modular multilevel converters for battery electric vehicles", *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 507-515, Jan. 2016.
- M. Quraan, P. Tricoli, D'Arco, and L. Piegari "Efficiency assessment of modular multilevel converter for battery electric vehicles", *IEEE Trans. Power Electron.*, accepted for publication, DOI: 10.1109/ TPEL.2016.2557579.
- S. D'Arco, L. Piegari, M. S. Quraan, and P. Tricoli, "Battery charging for electric vehicles with modular multilevel traction drives," in *Proc. 7th IET Int. Conf. on Power Electron., Mach. and Drives (PEMD 2014)*, pp.1,6, 8-10 April 2014.

- M. S. Quraan, and P. Tricoli, "Low frequency operation of modular multilevel converter with embedded battery cells for traction drives," accepted for publication, *23rd Int. Symposium on Power Electronics, Electrical Drives, Automation and Motion*.

1.4 Organization of the thesis

Other than the introduction, the thesis includes eight more chapters:

- Chapter 2 presents a review and comparisons between different battery management systems for battery cells. The chapter also presents a review and comparisons between traction drive converter topologies.
- Chapter 3 introduces the structure and the operation principle of the proposed MMC and includes the mathematical model to design the control of the converter.
- Chapter 4 describes the control of the converter in terms of circulating current control, motor vector control, SOC balancing control, and grid power control.
- Chapter 5 undertakes a thorough analysis of the converter efficiency for different operating conditions of the EV. The chapter also compares the efficiency of the MMC with a traditional two-level converter.
- Chapter 6 presents simulation results based on Matlab/Simulink to demonstrate the main features of cell balancing and the converter performance considering different load types. The Simulation results for the recharge control algorithm are also included in the chapter.
- Chapter 7 presents the design of the laboratory prototype of the proposed converter including the design of the converter auxiliary circuitry.

- Chapter 8 presents experimental results on kW-size driving an induction motor. The experimental results for the recharge control algorithm are also presented in the chapter.
- Chapter 9 presents the conclusions of the work and describes future research.

Chapter 2

Review of BMSs for Battery Cells and Traction Drives

This chapter reviews the BMSs for battery cells and converter topologies available in the technical literature. The comparison among the BMSs has been carried out according to the complexity of the circuit design, balancing speed, voltage/current stress across the devices, balancing system efficiency, size and cost. The comparison between traction drive topologies has been carried out in terms of the complexity of the converter design and control system, harmonic content of output voltages and currents, blocking voltage of each semiconductor switch, switching losses, and fault tolerant capabilities.

2.1 Battery Management Systems

Series connection of battery cells are widely used to reach the voltage required by the dc-link of battery EV traction inverter [8]. However, voltage imbalance between the cells appears when the battery is charged or discharged several times, because of the differences in leakage currents, temperatures, internal impedances, charge storage volumes and chemical characteristics of the cells themselves. The voltage imbalance results in progressive damage of battery cells and reduction of their service life time [9]. In order to avoid this, BMSs are normally added to the battery pack [10]. One of the most important parameter that is required by the BMS is the SOC of the cells, which is a good indicator of the current state of the battery. A tight equalisation of the SOC across the cells minimises the damage to the cells [11]. There

are two categories of charge equalising techniques used in BMS: passive BMSs and active BMSs. Passive BMSs use external passive resistors to dissipate the excess energy from the cells at higher SOC until their SOCs match those of at lower SOC. The resistors used in passive BMS can be either fixed in value [12], [13] or switched [12], [14]-[18], [19]-[21]. Active BMSs transfer the excess energy from the cells at higher SOC to the cells at lower SOC. Active BMSs topologies use different active elements as a buffer to transfer the energy between the cells, i.e. capacitors, inductors or transformers, as well as different controlled switches or converters [12], [14]-[18] and [21]-[46].

Passive BMSs are cheap and simple to implement with a reduced number of extra components. However, the equalisation rate is slow and the efficiency is low, because all the excess energy is dissipated across the balancing resistors. On the other hand, active BMSs provide a faster balancing rate and a higher efficiency, although they have higher complexity and cost [47]. The next sections provide a review of the different proposed passive and active BMSs [12]-[46], including their operating principle and the advantages and disadvantages of each method.

2.1.1 Passive BMSs

Passive BMSs dissipate the excess energy from the cells at higher voltage by using bypass shunting resistors connected in parallel to each battery cell. They are divided into fixed shunt resistor (FSR) and switched shunt resistor (SSR) method. The two methods can be used for low power applications with balancing current smaller than 10mA/Ah as recommended in [17] to limit the energy dissipated across the shunt resistors. The main disadvantage of passive BMSs is that the excess energy is converted into heat, thus a thermal management system

(TMS) is normally required. Another drawback is that when passive BMSs are applied during the discharge, the battery discharge time is reduced compared to active methods [17].

2.1.1.1 Fixed shunt resistors

In this method, *N* shunt resistors are connected across each cell of the battery system as shown in Fig. 2.1. The current drawn by each shunt resistor is linearly proportional to the cell voltage. As the cell voltage increases, more current is drawn by the resistor. This tends to decrease the voltage differences between the different cells, since the cells at higher voltage are discharged more by the shunt resistors. The FSR method can be only used for lead-acid and nickel-metal hydride batteries, because they can operate with over voltages without cell damage.

Implementation of the FSR method is simple and cheap. However, the current drawn by each shunt resistor is not regulated. Therefore, the balancing time is not controllable and the cell voltages are not fully regulated [12], [13], [17].

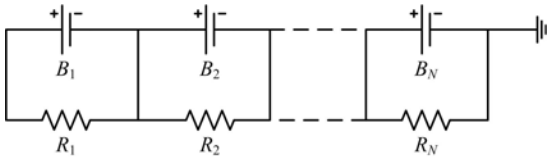


Fig. 2.1: The circuit diagram of the FSR method.

2.1.1.2 Switched shunt resistors

In this method, the excess energy is dissipated from the cells at a higher voltage in a controlled way using switches, as shown in Fig. 2.2, in order to regulate the current drawn by each shunt resistor. Thus, this technique prevents the overcharge of fully charged cells while other cells at a lower voltage are still recharged. In a similar way, the cells at a lower voltage are not connected to the shunting resistor during the discharge.

This method can be applied either in continuous mode or detecting mode. In continuous mode, the switches are controlled together by the same control signal. In the detecting mode, the cell voltages are measured to decide which resistor has to be connected. The SSR method is more efficient than the FSR method and it is still simple and reliable. The energy dissipated in the recharge is minimised, because the shunt resistors are connected only when the cell voltage is above a certain threshold. Therefore, it can be used for Li-ion batteries [17], [19], [20]. However, the use of this method for the discharge is not recommended because the balancing is obtained at the expense of the available energy for the EV.

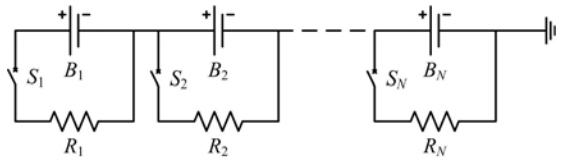


Fig. 2.2: The circuit diagram of the SSR method.

2.1.2 Active BMSs

Active BMS are divided into capacitor-based BMSs, inductor and/or transformer-based BMSs, and converter-based BMSs

2.1.2.1 Capacitor-based BMSs

Capacitor-based BMSs use capacitors as external storage device to transfer energy between battery cells. They work for both recharging and discharging operations. Capacitor-base BMSs can be divided into switched capacitors (SC), double-tiered switched capacitors (DTSC), single switched capacitors (SSC), and modularised switched capacitors (MSC).

2.1.2.1.1 Switched capacitors

The simplified circuit diagram of the SC method is shown in Fig. 2.3. It uses $N-1$ capacitors with $2N$ switches to balance the series string of N battery cells. The function of the switches is to connect the capacitors to the proper terminals where each capacitor is alternately switched

across adjacent battery cells at switching frequency of f_{sw}. The control signal of each switch has a dead time, αT_{sw} (where T_{sw} is the switching time) to avoid the short circuit of cells, as indicated in Fig. 2.3. The balancing current depends on the switching frequency, the value of the capacitance and the voltage difference between the battery cells.

This method can operate in both recharge and discharge processes. Its control strategy is simple because it has only two states. The main disadvantage of the SC method is that the equalisation time is relatively long because the energy can be only transferred between two adjacent cells [14]-[18], [22], [23].

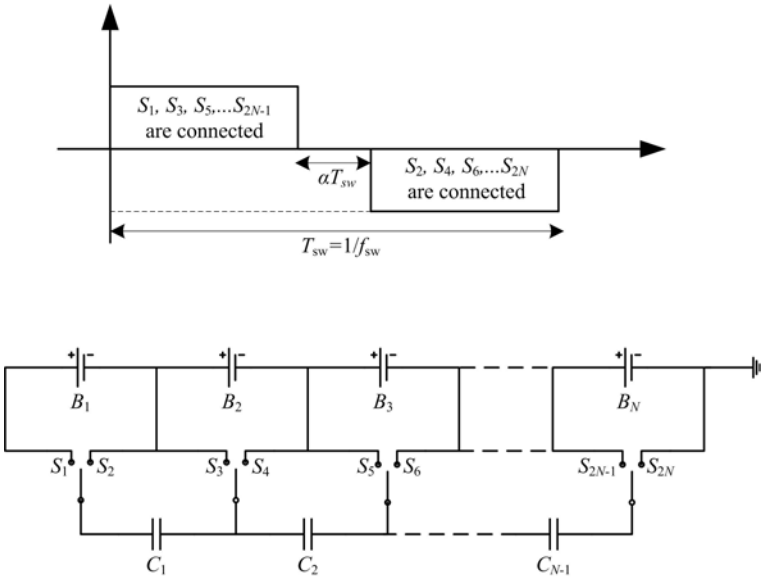


Fig. 2.3: The circuit diagram of the SC method.

2.1.2.1.2 Double-tiered switched capacitor

The circuit diagram of the DTSC is shown in Fig. 2.4. The number of cells in this method must be an odd number (e.g. $N = 2k + 1$, $k = 1, 2, \ldots, r$) to achieve the balance between the cells. The method uses $3r$ capacitors and $2N$ switches to balance the series string of N battery cells. In this method, a second tier of capacitors is connected in parallel to the capacitors of the SC circuit.

The idea is to transfer the charge between nonadjacent batteries through the bridging capacitors of the second tier. In the SC method, two switching cycles are required to shuttle the energy between nonadjacent cells, e.g. B_1 and B_3. However, the DTSC method can provide a path for the charge transfer between B_1 and B_3 through the capacitor C_3, increasing the speed of the charge transfer between batteries. The overall equalising time reduces to approximately a quarter of that achieved by the SC method [25], [26].

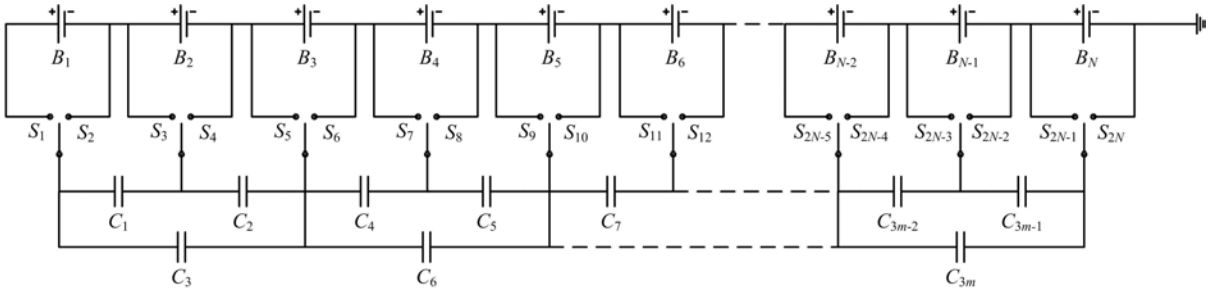


Fig. 2.4: The circuit diagram of the DTSC method.

2.1.2.1.3 Single switched capacitor

The circuit diagram of the SSC method is shown in Fig. 2.5. This method uses only one capacitor with $N + 5$ switches to balance the N series connected battery cells. During every cycle, one cell charges the capacitor C and another cell gets the charge from C. The method can be applied either in continuous mode or detecting mode.

In continuous mode, the control system uses a fixed switching sequence to open and close the switches. The control system connects the battery cell B_1 to the capacitor by closing the switches S_1, S_2, S_{N+2}, and S_{N+5}. When the capacitor is charged, the controller opens these switches and closes the switches S_2, S_3, S_{N+3}, and S_{N+4} to transfer the charge to the cell B_2. The net energy transfer depends on the voltage difference between B_1 and B_2. Using the same logic, the capacitor is then connected across (B_3, B_4, …, B_N, B_1,…). In this way, the excess charge of the cells at higher voltage are distributed step-by-step to those at lower voltage.

In detecting mode, the controller selects the cells to balance. The capacitor is charged from the cell at the highest voltage and selectively discharged to the cell at the lowest voltage. The process continues until the difference in voltage or SOC between the cells is smaller than a pre-defined threshold, which is normally accepted as 1-2%. This mode reduces significantly the equalising time in comparison to the continuous mode, especially if the highest and lowest charged cells are on the opposite ends of the battery pack. However, a much more complex controller is needed to detect and select the target cells [14], [17], [18], [24].

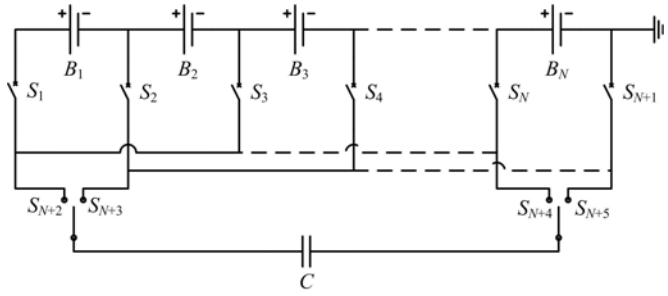


Fig. 2.5: The circuit diagram of the SSC method.

2.1.2.1.4 Modularised switched capacitor

When the number of battery cells is large like in the case of EVs, the design of a switched capacitor system is not easy due to the complexity, size and cost of the circuit. Moreover, the cell balance speed and cell balance efficiency are limited. However, the concept can be applied only to a part of the cells and repeated several time with a modular concept, simplifying the design and reducing the costs. In this configuration, the N battery cells are grouped into m modules and each module consists of a series n connected battery cells (i.e. $N = m \times n$). Each module is used to achieve the balance of n cells as a separate balancing system. In addition, only one equaliser is added externally to the modules to achieve the balance between the adjacent modules, because in the modular structure, each module can be reviewed as a battery cell at higher voltage. The main advantages of MSC are the modular design, the low voltage

stress across the cell, and the simplicity of the controller. Compared with a conventional switched capacitor, the modularised switched capacitor can transfer a large amount of energy not only between cells, but also between modules. Thus, a shorter equalising time can be achieved. Fig. 2.6 shows the structure of the MSC considering a string of *N* cells modularised into *m* modules [27].

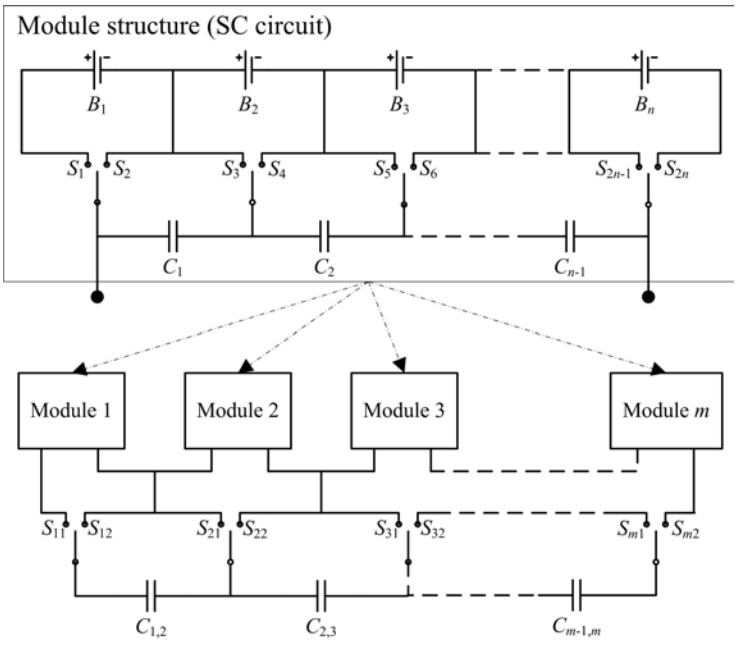


Fig. 2.6: The structure of modularised switched capacitor.

2.1.2.2 Inductor/transformer-based BMSs

Inductor-based BMSs use inductors or transformers to transfer energy from a cell or group of cells to another cell or group of cells to achieve balancing. These methods can be divided into single switched inductors (SSI) and multi switched inductors (MSI), single winding transformers (SWT), multi winding transformers (MWT), and multiple transformers (MpT).

Since these methods offer a balancing current higher than that based on capacitors, a shorter balancing time can be achieved. The main disadvantages of inductor/transformer-based BMSs are the higher cost and core losses. In addition, the methods may require a high switching

frequency operation to reduce the inductor or transformer size and achieve fast equalising speed, thus extra capacitors should be added across each battery cell to filter high frequency current harmonics [12].

2.1.2.2.1 Single switched inductors

The circuit diagram of SSI is shown in Fig. 2.7. This method uses one inductor, 2*N* switches and 2*N* diodes to balance the series string of *N* battery cells. Each cell terminal has two unidirectional paths connected with the inductor *L*. Each path is composed of a series connected switch and diode, except for the first and last paths. The control system senses the voltage of each cell and selects the two cells which will be used to transfer the energy [29]. For example, if the cell B_1 has the highest voltage and the cell B_2 has the lowest voltage, the switches S_1 and S_3 are initially turned on. Once the inductor is charged, S_1 is turned off and the switch S_4 is turned on to transfer energy stored in the inductor to B_2.

This method achieves fast equalising speed and good efficiency, but the control is complex, the switches current stress is relatively high, and filtering capacitors are required for high switching frequency operations.

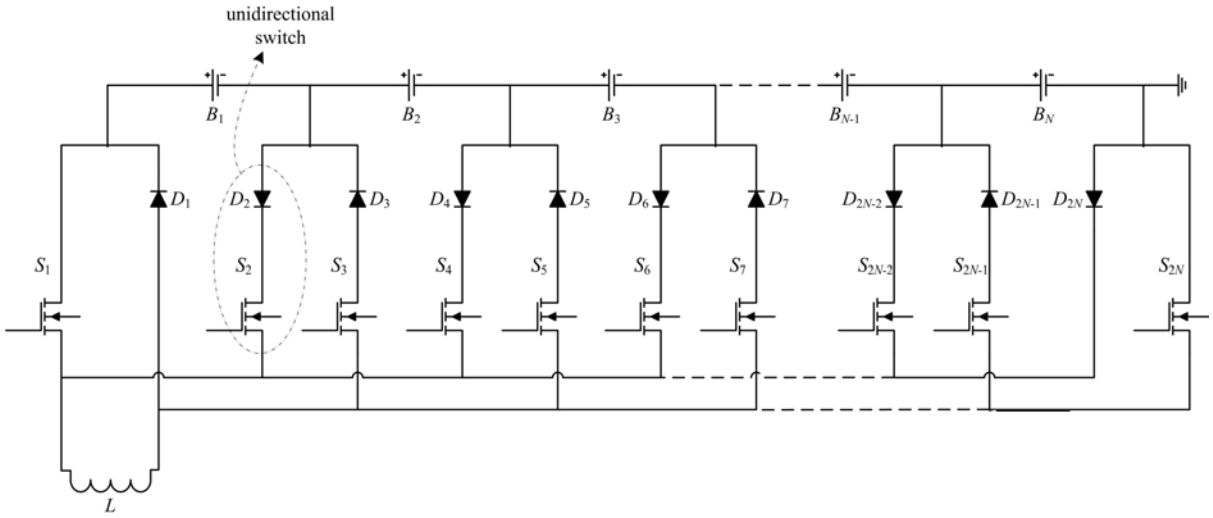


Fig. 2.7: The circuit diagram of SSI method.

2.1.2.2.2 Multi switched inductors

Fig. 2.8 shows the circuit diagram of the MSI method. This method uses $N-1$ sub-modules (SMs) to balance a series string of N battery cells where each SM consists of two switches and an inductor. Each SM is connected across the two adjacent cells to allow energy transfer from the cell with higher voltage to the cell with lower voltage.

The controller senses the voltage difference of the two adjacent cells and then applies a pulse width modulation (PWM) signal to the switches with a condition that the cell at higher voltage must be switched on first. The two switches within each SM are controlled in a complementary way. By adjusting the duty cycle of the modulating signal, the current flow through the inductor in both directions. For example, if the voltage across cell B_2 is higher than that across cell B_1, the switch S_2 is closed to transfer energy from B_2 to the inductor L_1. Once the inductor is charged, the switch S_2 is opened and S_1 is closed, allowing the current to flow in the loop formed by B_1, L_1 and S_1. As a result, the energy is transferred from B_2 to B_1.

A less complex control is needed for this method in comparison with the SSI, but a longer time is required to transfer the energy from the first cell to the last one, especially for a long string of battery cells. Additionally, this method has higher core losses, since it needs $N-1$ inductors to achieve the cell balancing [28], [30].

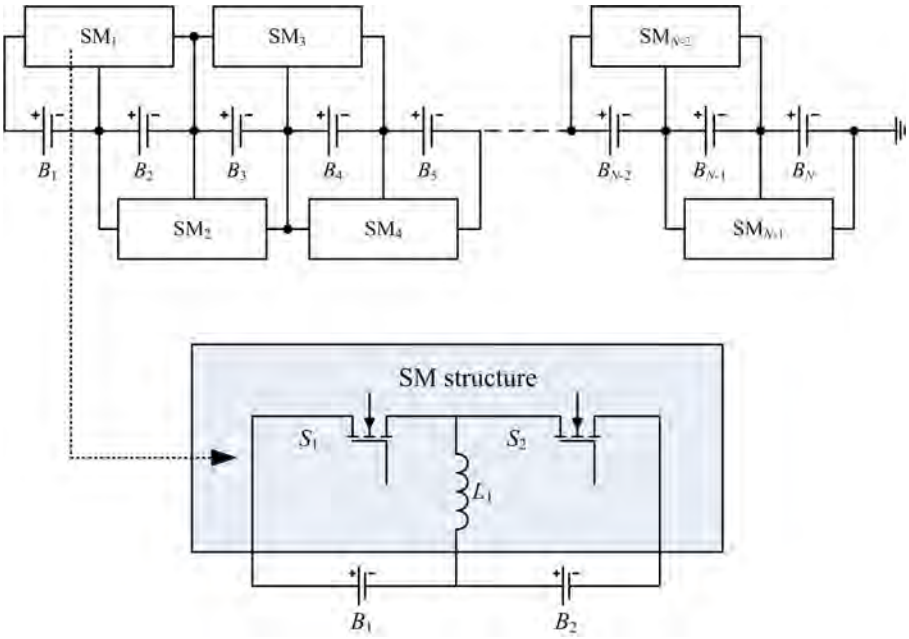


Fig. 2.8: The circuit diagram of MSI method.

2.1.2.2.3 Single winding transformers

This method uses one transformer to balance the series string of N battery cells. Two different circuit configurations are available, the pack-to-cell and cell-to-pack as shown in Fig. 2.9 and Fig. 2.10, respectively.

In the pack-to-cell topology, the energy is transferred from the entire battery pack to the primary winding of the transformer. The output of the transformer is rectified through the diode D and the energy is transferred to the cells at a lower voltage using the corresponding switches. This method can rapidly balance low voltage cells at the cost of removing the energy from the entire pack [21].

In the cell-to-pack topology, the controller decides which cell has the lowest voltage (e.g. B_1) and then activates the corresponding switches of the other $N - 1$ cells periodically to discharge them. The controller continues to monitor the cell voltages and, if the voltage across one of the other $N - 1$ cells (e.g. B_2) becomes equal to the voltage across B_1, the cell B_2 is taken

out of the pack and is recharged together with cell B_1. The charging operation continues until all cells reach the same voltage level [31].

The SWT method achieves fast equalisation speed with low core losses. However, a complex control is needed and the implementation is expensive. Moreover, there is no flexibility in the design and if one or more cells have to be added to the battery pack the transformer must be changed [14]-[17], [21], [31].

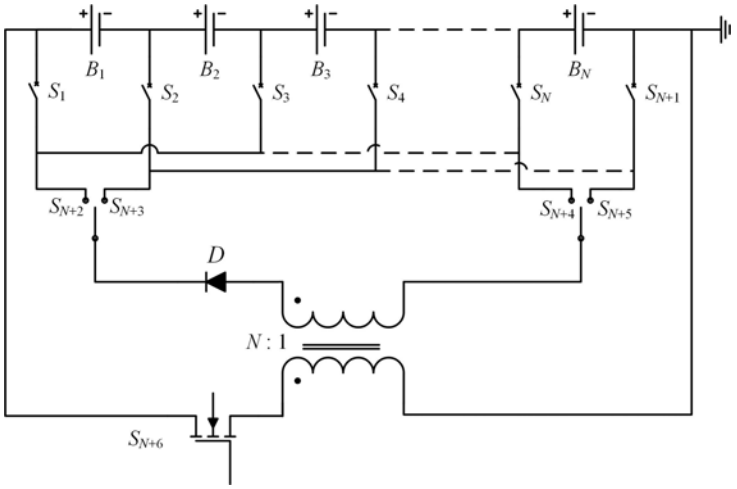


Fig. 2.9: The circuit diagram of SWT method (pack-to-cell topology).

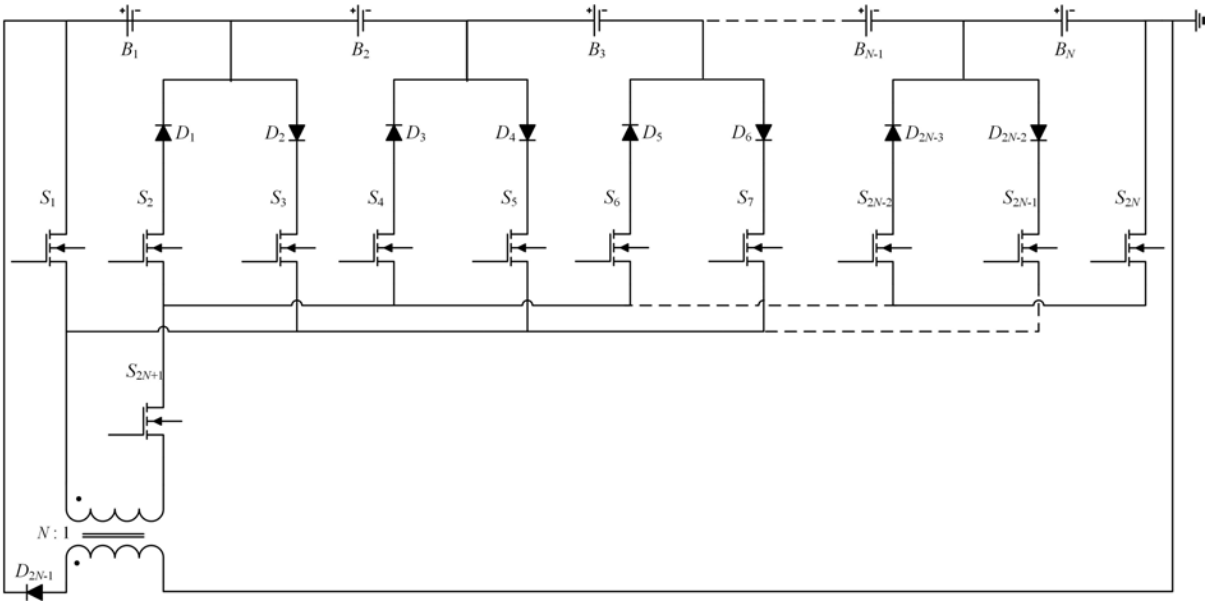


Fig. 2.10: The circuit diagram of SWT method (cell-to-pack topology).

2.1.2.2.4 Multi winding transformers

The MWT has a single transformer with one primary winding and *N* secondary windings and each of these windings is connected to one battery cell. This method can be implemented with two different circuit configurations: MWT flyback and MWT forward, as shown in Fig. 2.11.

The flyback structure uses *N* diode and one switch to balance *N* series connected battery cells. In this topology, the primary winding of the transformer is energised by turning on the switch *S*. When *S* is turned off, the energy is transferred into the secondary side of the transformer and the induced current supplies the cell at lower voltage through the corresponding diodes [14]-[17], [21], [33], [34].

The forward structure uses instead *N* switches and one diode to balance a series string of *N* battery cells. In this topology, the appropriate switch connects to cell with the highest voltage to the corresponding secondary winding of the transformer. In this case, the energy is transferred from this cell to all the others via the transformer and the anti-parallel diodes of the switches.

The MWT method can rapidly balance the cells without a closed-loop control, so it is suitable for both EV and hybrid electric vehicle (HEV) applications, although the circuit is complex, the implementation cost is high. However, the problem associated with this topology is the flux imbalance. Differences in the resistances of secondary windings and the on time forward resistances of semiconductor switches drive into deep saturation with risk of damage the power switches [14]-[17], [21], [33], [34].

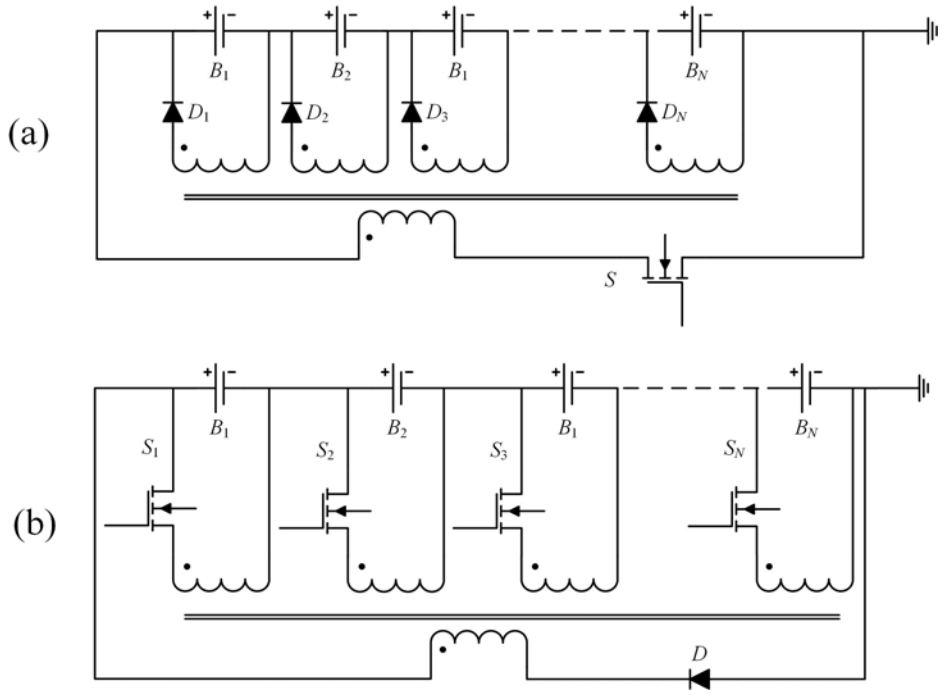


Fig. 2.11: The circuit diagram of MWT method: (a) Flyback configuration. (b) Forward configuration.

2.1.2.2.5 Multiple transformers

Fig. 2.12 shows the circuit diagram of the method based on MpTs. This method uses N diodes, N transformers, and one switch to balance the string of N battery cells. The current drawn from the entire battery pack is switched into each transformer primary winding and then transferred to all the secondary windings and the cells through the diodes. The charging currents through the cells will be dependent upon the voltage of the cells themselves [14]-[17], [21].

Compared to the MWT method, this method is more flexible in terms of modularity of the design and battery pack extension, because each cell has its own transformer. However, the circuit implementation is still more expensive than the methods based on capacitors.

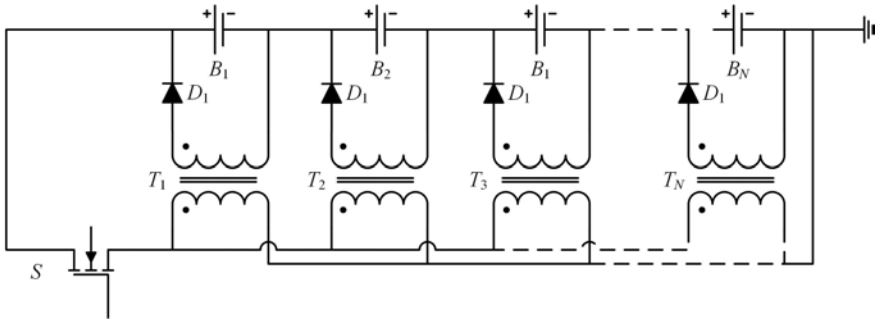


Fig. 2.12: The circuit diagram of MpT method.

Both inductor-based and transformer-based BMSs can also be implemented in a modular way similar to the modularised switched capacitor method [27], [35].

2.1.2.3 Converter-based BMSs

Converter-based BMSs use power converters to balancing the cells or group of cells in a battery. These methods can be divided into Ćuk converters (CC), buck/boost converters (BBC), flyback converters (FbC), quasi-resonant converters (QRC), ramp converters (RC), and full-bridge converters (FBC). They feature a fully controlled balancing process, but the resulting BMS has relatively high cost and complexity [36]-[44].

2.1.2.3.1 Ćuk converters

Fig. 2.13 shows the circuit diagram of the bi-directional CC balancing system. This method uses $N - 1$ bi-directional Ćuk converters to balance a series string of N battery cells; each converter consists of two switches, two inductors and one capacitor. Each converter is connected across two adjacent cells to allow the energy transfer from the cell with a higher voltage to the cell with a lower voltage. Therefore, this method takes a relatively long time to equalise the entire pack, especially for a high number of cells. The maximum voltage across each switch is equal to the maximum capacitive voltage ($V_{B1} + V_{B2}$) and, hence, low voltage MosFETs can be used as power devices to reduce conduction and switching losses [36], [37].

The energy is transferred between two adjacent cells through the capacitor, where the direction of the power is determined by the voltage imbalance between the two cells and the switching function of the switches. The converter is usually designed to operate in discontinuous capacitor voltage mode (DCVM) in order to reduce MosFETs switching losses. The initial voltage across the capacitor is equal to the voltage sum of the two adjacent cells [36], [37].

This method can achieve cell balancing with high efficiency, so it is suitable for both EV and HEV applications, but the speed of cell balancing is slow and the control system is complex [36], [37].

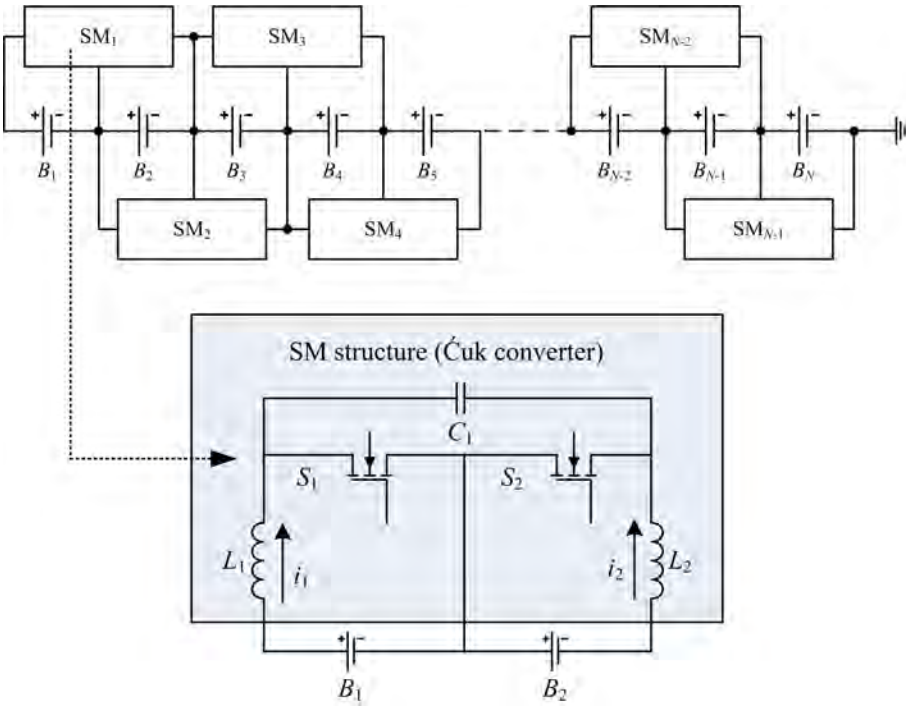


Fig. 2.13: The circuit diagram of the CC balancing system.

2.1.2.3.2 Buck/boost converter

The buck, boost, and buck-boost converters are commonly used as active BMSs. Buck converters are used to transfer the energy from the battery pack to the cells at lower voltage;

boost converters are used to transfer the excess energy from the cells at higher voltage to the battery pack; and buck-boost converters can be used in either direction. The BBC methods can achieve a good equalisation speed with high efficiency and they are suitable for modular design. On the other hand, the implementation is relatively expensive and complex and a complex control is needed to achieve cell balancing [14]-[16], [38], [39].

Fig. 2.14 shows the circuit diagram of the buck/boost conversion balancing system. This method uses *N* bidirectional SMs to balance the series string of *N* battery cells. Each SM consists of two switches, one inductor and one capacitor. The converters can be operated in continuous conduction mode (CCM) or discontinuous conduction mode (DCM), depending on the design of the control and the circuit parameters. The maximum voltage of each SM is equal to the cell voltage and, hence, low voltage MosFETs can be used also in this case [14]-[16], [38], [39].

During the charging process, each SM operates as a buck converter. Therefore, the capacitors of the output filters are connected first in series, and then to the dc power source. The balancing system operates without filter capacitor at the SM input terminals [14]-[16], [38], [39].

During the discharge process, the SMs draw currents from cells to increase the voltage of the output capacitors and then the sum of the output voltages of SMs is controlled to meet the required load voltage. The average input/output voltage of each SM depends on the corresponding cell voltage and the SM duty cycle. Therefore, the average input/output voltage of the SMs may be different. However, the average input/output current of the SM is equal to the input charge current or to the output load current, because all SMs are connected in series and either charged by the same dc power source or discharged to the same load [14]-[16], [38], [39].

For CCM, the battery current can be regulated individually by adjusting the duty cycles of the converters. The cell current is inversely proportional to the duty cycles of the corresponding SM. For DCM, the module with higher voltage has the smaller time ratio of the switching period when the inductor current decreases from the peak value to zero, revealing that cell balancing can be automatically achieved when all SMs are operated with the same duty cycle [14]-[16], [38], [39].

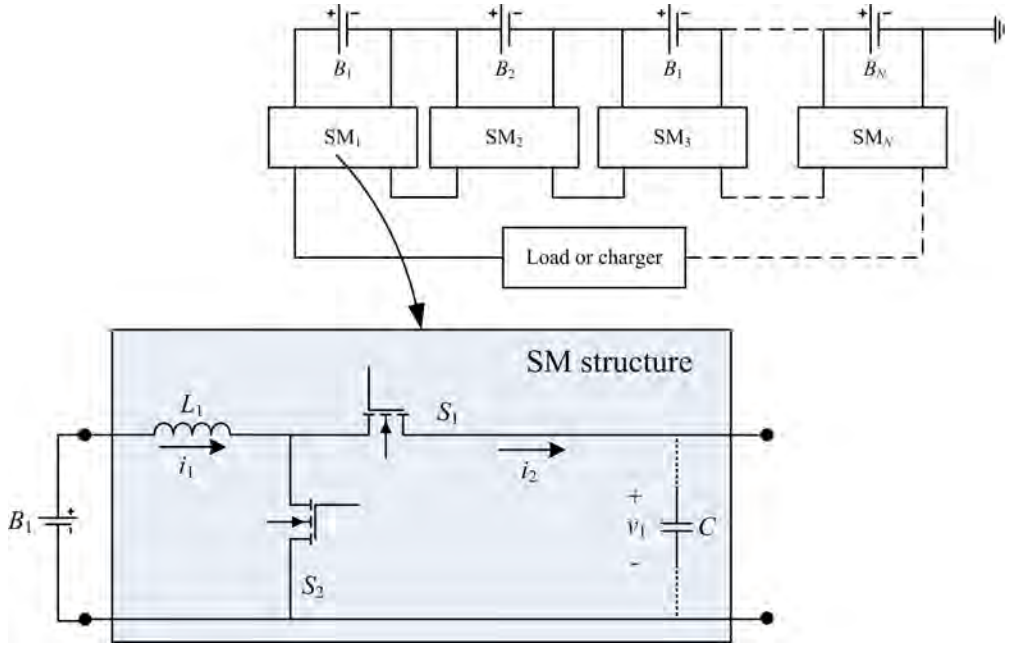


Fig. 2.14: Circuit diagram of the buck or boost converter balancing system.

2.1.2.3.3 Flyback converter

This method uses N SMs to balance N battery cells and it can be divided into unidirectional or bidirectional flyback configurations. Fig. 2.15 shows the circuit diagram of the flyback converter balancing system.

In the unidirectional configuration, each SM consists of two switches and one transformer to provide the required level shifting. The transformer turns ratio, a, is less than or equal to the number of cells. The control system measures the cell voltages and compares them with an

average pre-set value. When the voltage of a given cell exceeds a certain voltage level, the excess energy is transferred back to the battery pack until the cell voltage returns within the limit. Filter capacitors can be added across each battery cell to filter the high switching frequency current [14], [16], [40], [41].

In the bidirectional flyback configuration, each SM consists of two switches and one transformer. This structure is more flexible than the unidirectional, because the energy can be also transferred from the battery pack to the cells. During charging, the cell voltages are regulated by transferring the excess energy of cells at higher voltages to the battery pack. During discharging, the energy is transferred from the battery back to the cells at lower voltages, improving the use of the whole battery pack. In a way similar to the unidirectional configuration, the driving signals for the semiconductor switches are derived using simple comparative circuitry which activates the appropriate SMs. For example, when the switch S_1 is turned on, the cell B_1 transfers energy to the transformer T_1. The current i_1 increases and the current i_2 is equal to zero. When S_1 is turned off, the body diode of S_2 conducts the current and the energy stored in the transformer is transferred to the cell B_2. The current i_1 decreases as the transformer stored energy decreases. Once the transformer is fully discharged, the currents i_1 and i_2 are both equal to zero [14], [16], [40], [41].

The flyback converter method achieves cell balancing with high efficiency, so it is suitable for both EV and HEV applications, but the speed of balancing is slow, the transformers must have the same characteristics to avoid the core saturation problem, the magnetic losses are high, and the control system is complex [14], [16], [40], [41].

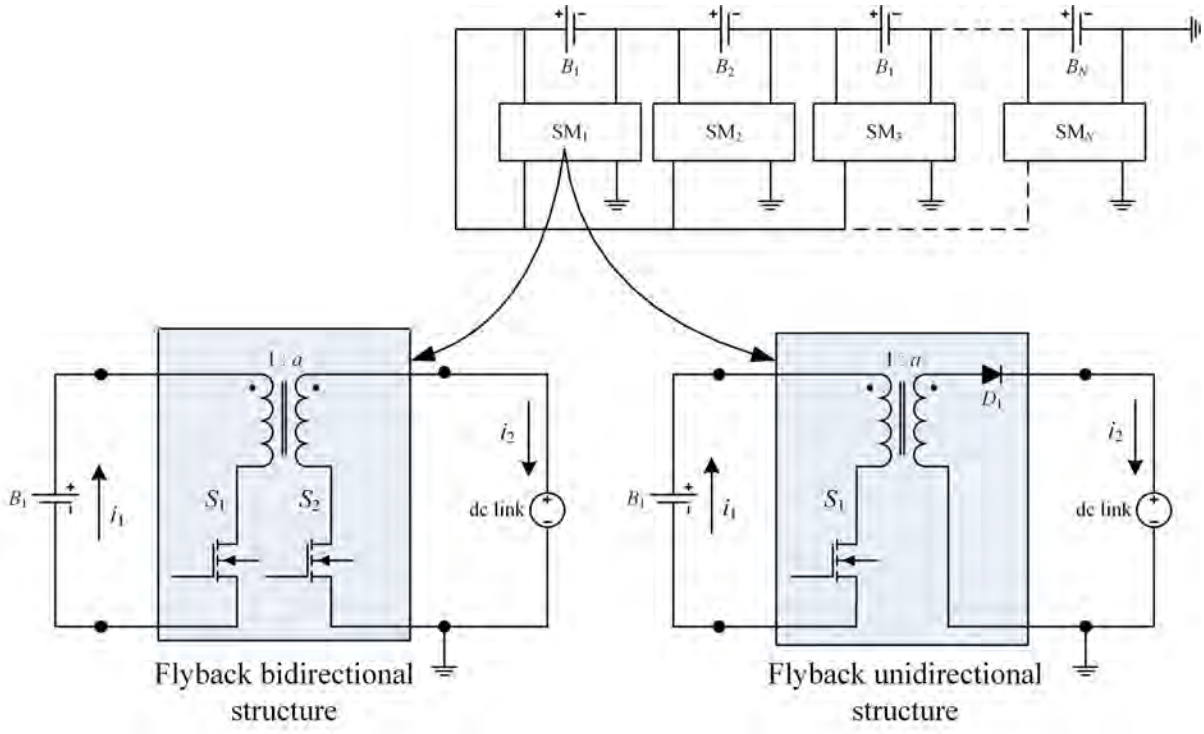


Fig. 2.15: The circuit diagram of the FbC balancing system.

2.1.2.3.4 Quasi-resonant converter (QCR)

Fig. 2.16 shows the circuit of the QRC balancing system. This method uses $N-1$ QRCs to balance the series string of N battery cells. Each QRC consists of two switches, two inductors and one capacitor. Each QRC is connected across two adjacent cells to allow bidirectional energy transfer from the cells. Therefore, this method is characterised by a relatively long equalization time, especially for battery packs with a large number of cells. The QRCs can have either zero-current quasi-resonant (ZCQR) or zero-voltage quasi-resonant (ZVQR) topologies [14], [15], [42], [43].

The main advantage of QRCs is that they reduce the switching losses and increase the BMS efficiency. However, they have a very complex control, difficult implementation and high cost. The resonant inductor L_{r1} and resonant capacitor C_{r1} are designed to operate as a resonant tank

in order to achieve the zero current switching function for a bi-directional power flow [14], [15], [42], [43].

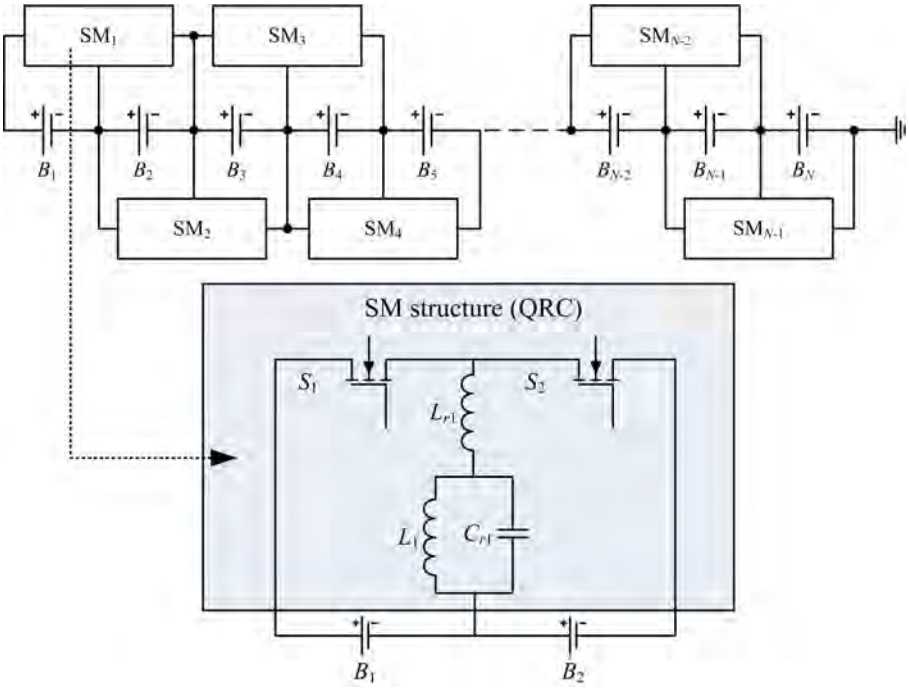


Fig. 2.16: The circuit diagram of the QRC balancing system.

2.1.2.3.5 Ramp converter (RC)

This method uses a single transformer with one primary winding and $N/2$ secondary windings and N diodes to balance N battery cells. It shares the idea of the MWT method, but the connections between the transformer secondary windings, the diodes, and the cells are modified to decrease by 50% the number of secondary windings and, thus, reduce the transformer size. In this configuration, each pair of battery cells is connected to one secondary winding. Fig. 2.17 shows the configuration of the RC balancing system and the ideal primary current waveform. In case of an odd number of battery cells, one of the transformer secondary windings is connected to a single cell [14], [15], [45].

This circuit is called ramp converter because of the shape of the primary current waveform i_o. The primary current is generated using a series load resonance (SLR) converter, which is

similar to the square wave inverter except the fact that the switching frequency is much higher than the resonant frequency in order to avoid high voltages across the resonant inductor and capacitor. Since the batteries always limit the maximum output voltage, the converter is operated only in constant current mode. The method uses the frequency modulation technique to control the peak value of the primary current, which implies that the sum of the rectified secondary currents is also regulated. Soft switching can be employed, so all the semiconductors have zero voltage switching (ZVS) and/or zero current switching (ZCS) at both turn-on and turn-off periods to reduce switching losses. During the positive half cycle of the primary current, the induced secondary currents charge the odd-numbered cells with the lowest voltages. In the next half cycle, the currents charge the even-numbered cells with the lowest voltages [14], [15], [45].

Although the RC method uses soft switching technique along with a relatively simple transformer, the cell equalisation speed is slow and a complex control is needed to achieve cell balancing [14], [15], [45].

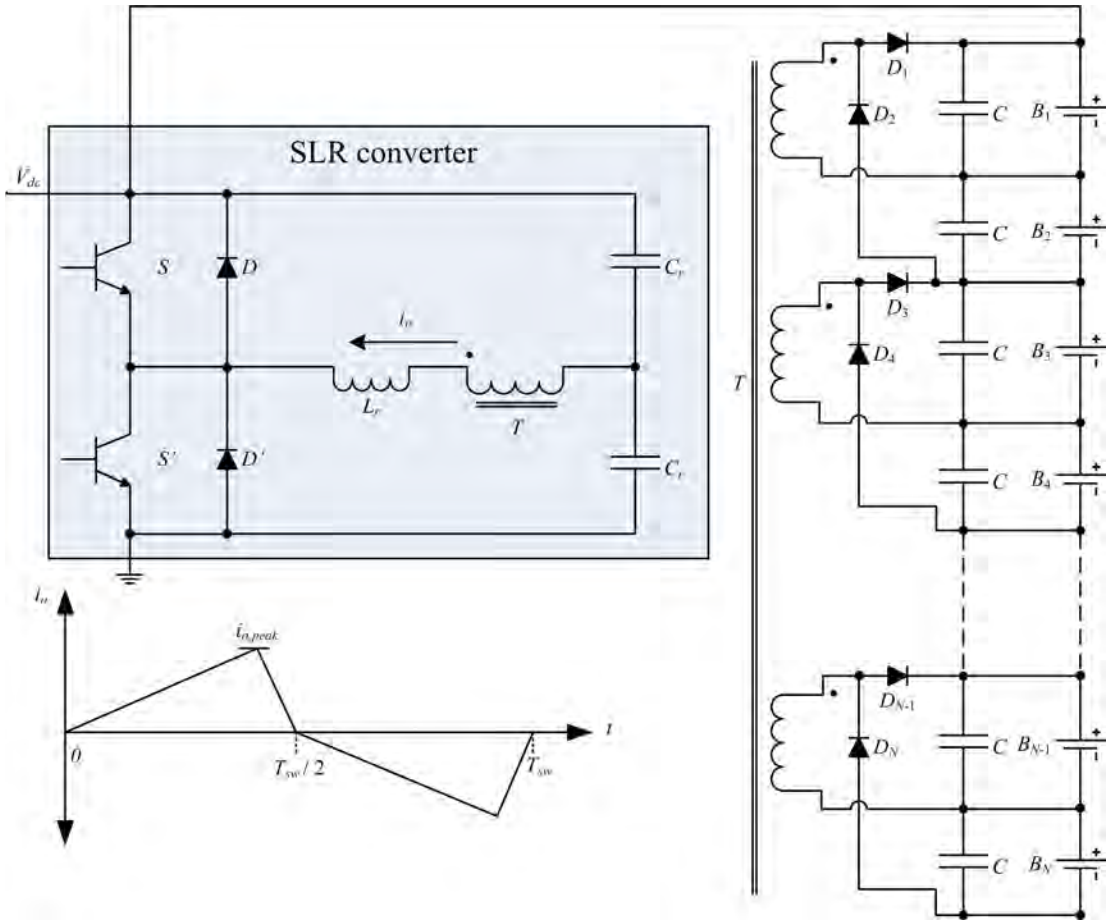


Fig. 2.17: The circuit diagram of the RC balancing system.

2.1.2.3.6 Full-bridge converter (FBC)

The full-bridge converter shares the idea of the buck/boost converter balancing system, except the fact that the converter can operate either as ac/dc or dc/dc. However, both modes need an intelligent control [44].

Fig. 2.18 shows the circuit diagram of the FBC balancing system working in the dc-dc mode. This method uses *N* bidirectional SMs to balance the series string of *N* battery cells. Each SM consists of four switches. The operating principle of each SM is quite similar to the buck/boost converter. For high voltage applications, each SM is connected to a series string of *n* cells instead of just one cell to increase the output voltage, as indicated in Fig. 2.18. In this case, the

circuit balances battery units instead of battery cells. The main drawback of FBC is its high cost and complex control [44].

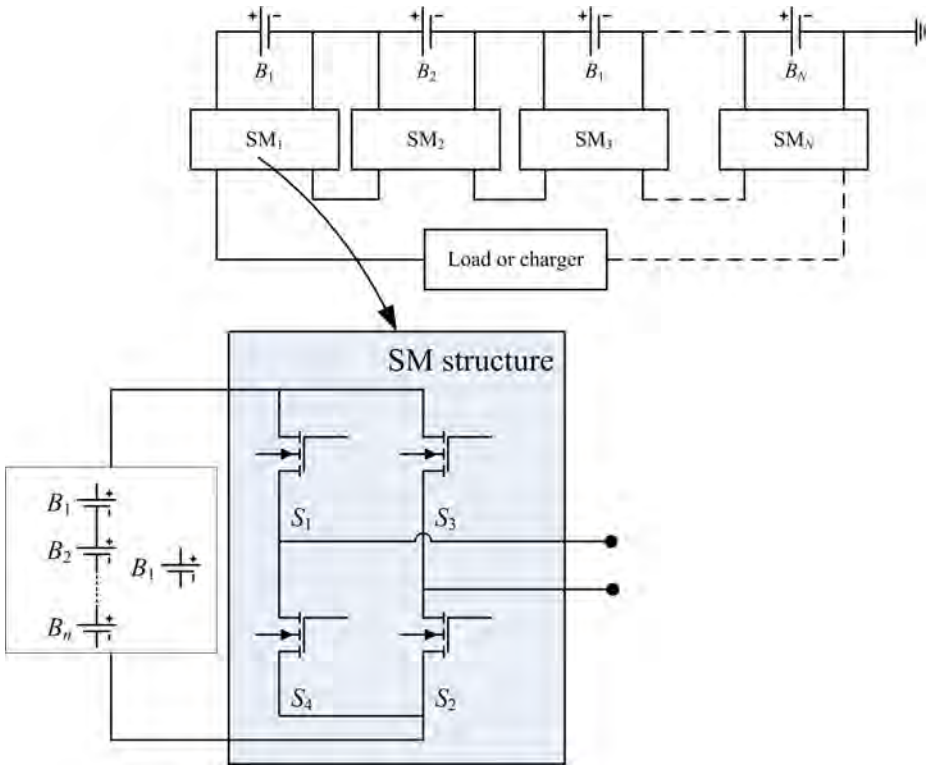


Fig. 2.18: The circuit diagram of the FB balancing system.

2.2 Traction drives for battery electric vehicles

Variable speed drives require flexible supply of electric motors in terms of voltage frequency and magnitude. Traction drives require also that the motors develop the limit torque for the whole frequency range. The limit torque is equal to the full load torque below the base speed of the machine and is decreasing with an approximately inverse law above the base speed and below the machine limit and with an approximately inverse square law above the machine limit. The converter output voltages are usually pulsed in nature and, as such, contain high-order harmonics that may reduce the motor efficiency and performance. Additionally,

harmonic currents produce torque oscillations of the motors. Current harmonics can be reduced by either filtering or pulse-width modulation techniques [48].

The quality of the inverter output is normally evaluated in terms of its total harmonic distortion (THD), which is defined in terms of the output voltage harmonics as follow [48]:

$$\mathrm{THD} = \sqrt{\frac{V^2 - V_1^2}{V_1^2}}, \tag{2.1}$$

where V_1 is the rms value of fundamental component of the output voltage and V is the total rms value of the output voltage.

Traction drives are classified into two-level inverters and multilevel inverters and are reviewed in the following sections.

2.2.1 Two-level inverters

Two-level inverters are the most common topology used for traction motors. The standard topology of the three-phase inverter is shown in Fig. 2.19 with a detail on the line-to line output voltage. The ac output line voltages can be only $\pm V_{dc}$ and 0 as indicated in Fig. 2.19. [48], [49], [50]. A string of low-voltage battery cells are connected in series to reach the voltage level required by the dc-link of the inverter.

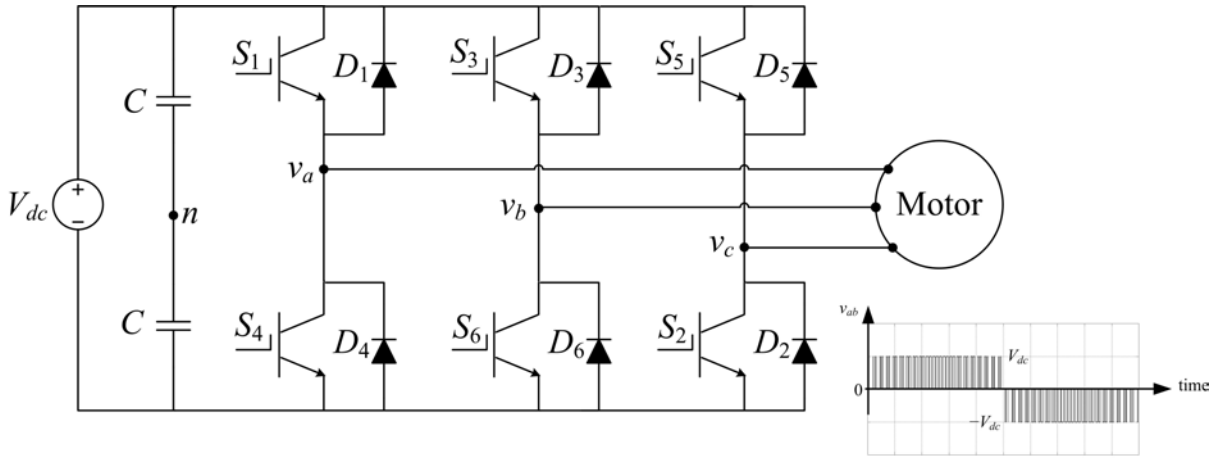


Fig. 2.19: The circuit diagram of the standard two-level inverter.

The major advantages of two-level inverters are:

- Simple control method.
- Equal ratings of the switching devices.

The major disadvantages of two-level inverters are:

- High harmonic content of the current especially in field-weakening mode that may require filters;
- High switching losses;
- Necessity of an additional BMS for the battery pack;
- Unable to cope with faults of devices.

Many commercial hybrid electric vehicles, such as Prius, Camry and Fusion, use a bidirectional dc-dc boost converter to interface the battery pack to the inverter dc link, as shown in Fig. 2.20. The inductor of the boost converter is rated for the full power of the drive. Besides its large size and heavy weight, the inductor losses limit the operating temperature. For this reason, the efficiency of the dc-dc converter is relatively low compared to that of the inverter. The problem is much more serious for EVs, because the boost converter has to deliver the full power needed by the traction drive. The problem cannot be simply solved increasing the switching frequencies to limit size, weight, and cost of the boost converter, since the core and copper losses of the inductor increases significantly. In addition, the maximum switching frequency of the boost converter is limited by the heat dissipation of the semiconductors. In response to this problem, multiphase dc-dc converters have been developed for high power HEVs and EVs. In these topologies, the inductor design is still a challenge that limits the converter efficiency and the power density. Very recently, multilevel dc-dc converters have been proposed for different applications including HEVs and EVs. Unlike traditional dc-dc

converters, multilevel dc-dc converters greatly reduce the inductance requirements in addition to other benefits, such as much lower device voltage rating and faster dynamic response. However, the two-stage energy conversion reduces the general efficiency of the traction drive [51].

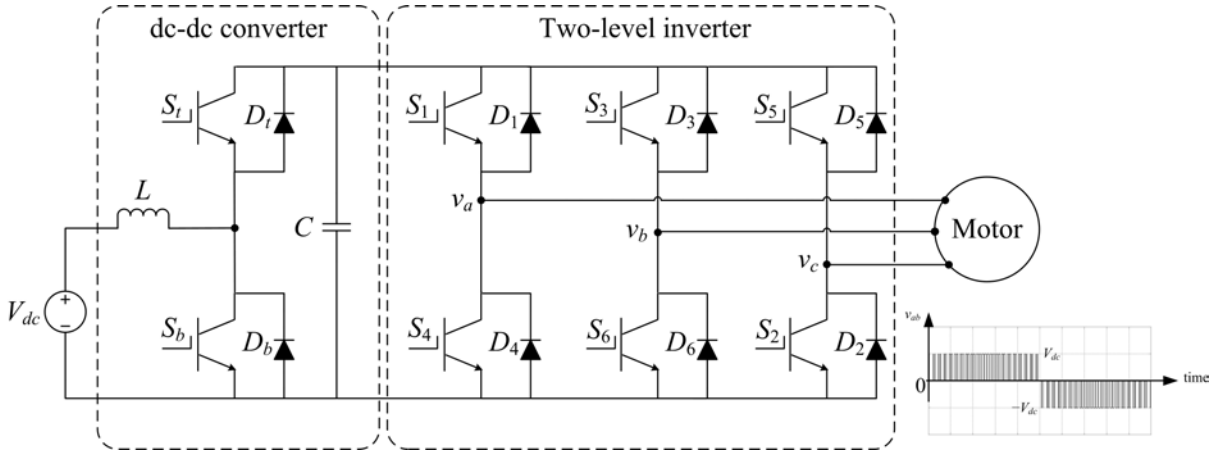


Fig. 2.20: Traction package with two-stage power conversion.

2.2.2 Multilevel inverters

Multilevel inverters divide the dc link directly or indirectly, so that the output of each phase leg has more than two levels. The quality of the voltage output is improved, because both pulse width modulation and amplitude modulation can be used. The advantages of multilevel converters compared to conventional two-level converters are well-known. They have higher output voltage magnitude, reduced THD of output voltages and currents, reduced output voltage gradients and reduced voltage supported by each power semiconductor switch [48], [50], [52], [53].

There are three main types of multilevel traction drive converters:

- Neutral point clamped (NPC) multilevel inverters;
- Flying capacitors (FC) multilevel inverters;
- Cascaded H-bridge (CHB) multilevel inverters.

2.2.2.1 NPC multilevel inverters

The n-level NPC multilevel inverter has been proposed as a variable motor speed drive for EVs [54]-[68]. Each leg of the converter consists of $2n - 2$ switches with $2n - 2$ anti-parallel diodes, and $2n - 4$ clamping diodes to produce a line-to-line output voltage with n-levels. Additionally, the dc link has $n - 1$ capacitors connected in series.

Fig. 2.21 shows the basic structure of a four-level NPC inverter with a detail on the four-level line-to line voltage. Each phase leg is identical and all of them share the dc link capacitors. The switches S_j and S_j', where $j = 1, 2, 3$, are controlled in a complementary way. When S_j is turned on, S_j' is turned off and vice versa.

The output voltage v_{ao} has four voltage levels, V_{dc}, $\frac{2}{3}V_{dc}$, $\frac{1}{3}V_{dc}$ and 0. The clamping diodes have the essential role to clamp the outer switches to the terminal points of the capacitors. Therefore, no switches experience a voltage greater than one-third of the dc link voltage [48], [53], [50].

Although each switching device is required to block only a voltage level of $\frac{1}{3}V_{dc}$, some of the clamping diodes have larger blocking voltages. The blocking voltage of each clamping diode depends on its position in the converter structure. For example, when all the bottom switches are switched on, diodes $D_{c,a1}'$ and $D_{c,a2}$ need to block $\frac{2}{3}V_{dc}$. Similarly, diodes $D_{c,a1}$ and $D_{c,a2}'$ need to block $\frac{1}{3}V_{dc}$ [48], [53], [50]. The series connection of the clamping diodes avoids this limitation, but at the expense of a higher number of components. Using the blocking voltage for all the diodes, the number of required clamping diodes is $n(n - 1)$. Therefore, when n is high, the high number of diodes makes the converter impractical to implement [48], [53], [50].

Since the voltage levels at the capacitor terminals are different, the currents of the capacitors are also different and this causes an imbalance of the capacitor voltages. This problem can be solved replacing capacitors with controlled dc voltage sources, or specific PWM strategies, or balancing resistors [48], [53], [69].

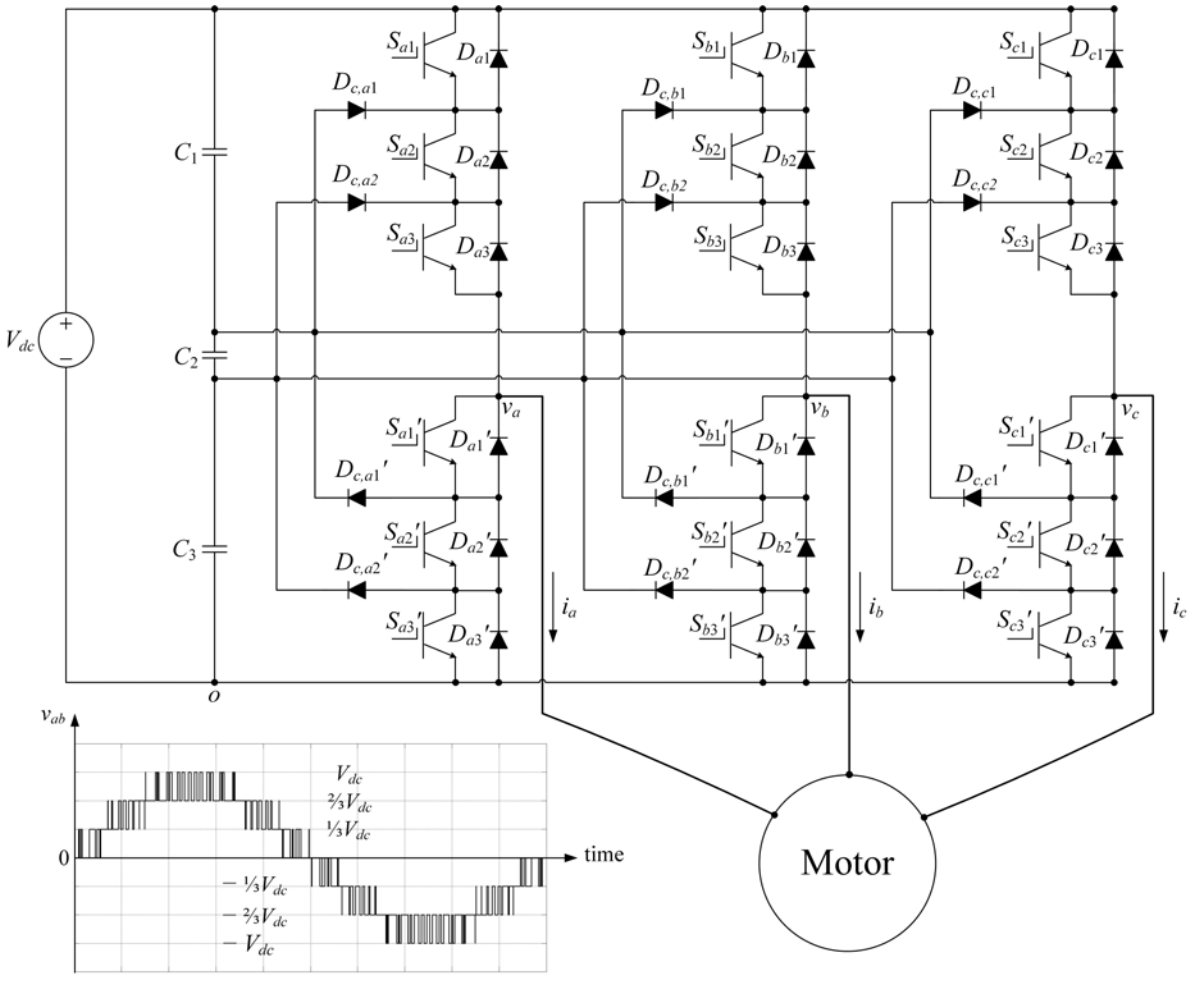


Fig. 2.21: Circuit diagram of a four-level NPC inverter.

The major advantages of NPC inverters are:

- THD of output voltages and currents lower than two-level inverters.
- Lower switching frequency for a given THD of the output voltage, which produces lower switching losses and higher efficiency.
- Lower blocking voltage of each semiconductor switch.

- Simple control method.

The major disadvantages of NPC inverters are:

- The clamping diodes have unequal reverse voltage blocking ratings, so a large number of clamping diodes is required when the number of level increases.
- The switching devices have unequal ratings.
- The capacitor voltages between the different converter levels are unbalanced.
- The battery pack needs an additional BMS to balance the cells.

2.2.2.2 Flying capacitor multilevel inverters

The *n*-level FC multilevel inverter has been proposed as a variable motor speed drive for EVs in [70]. The structure of the converter is similar to the NPC inverter. However, instead of using clamping diodes, the inverter uses clamping capacitors. Each phase of the converter consists of $2n$ switches with $2n$ anti-parallel diodes, and $\sum_{i=1}^{n} n - i$ clamping capacitors to produce the n levels of the line-to-line output voltage. Additionally, the main dc link is connected to $n - 1$ capacitors.

Fig. 2.22 shows the basic structure of the four-level FC inverter with a detail of the basic four-level line-to line voltage, v_{ab}. The phase legs are identical and share the capacitors of the dc-link. The capacitors are used to clamp the switch voltages to $\frac{1}{3}V_{dc}$. The switches, S_j and S_j' where $j = 1, 2, 3$, are controlled in a complementary way as the case of NPC inverters.

The output voltage of the inverter is similar to NPC inverters. However, the configuration offers more usable switch states than the NPC inverter, and this redundancy allows a better and more flexible control of the capacitor voltages. The output voltage, v_{ao}, has four voltage levels, V_{dc}, $\frac{2}{3}V_{dc}$, $\frac{1}{3}V_{dc}$ and 0. Unlike NPC inverters, the inner voltage levels (i.e., $\frac{2}{3}V_{dc}$ and $\frac{1}{3}V_{dc}$) are

redundant and can be obtained by three switch combinations, giving a certain flexibility in the control of the individual voltages across the flying capacitors [48], [53], [69].

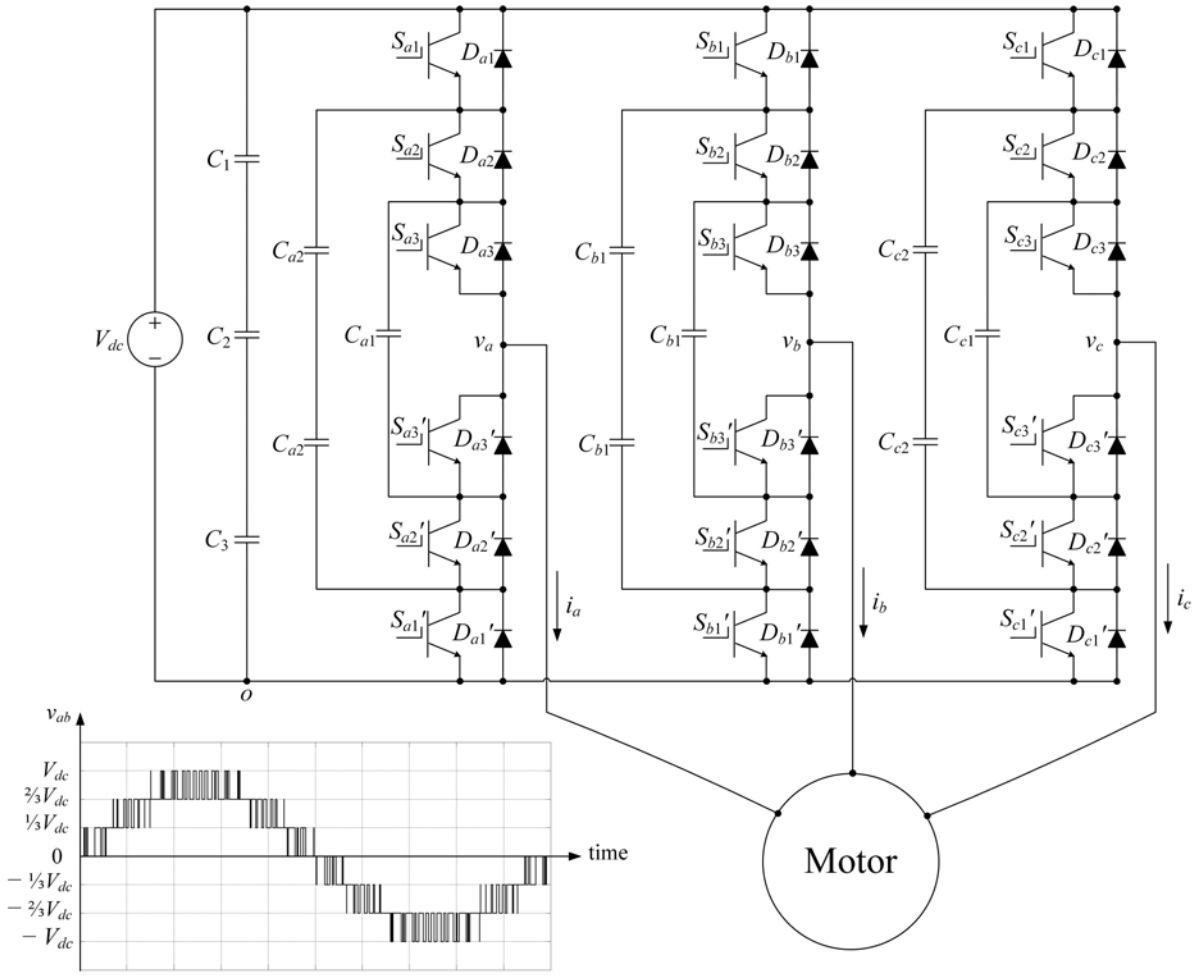


Fig. 2.22: The circuit diagram of the four-level FC inverter.

The major advantages of FC inverters are:

- Lower THD of output voltages and currents compared to two-level inverters.
- Fault-tolerance due to the large number of capacitors
- Switching combination redundancy for the individual balancing of the flying capacitors.
- Lower blocking voltage of each semiconductor switch.

The major disadvantages of the FC inverters are:

- Large number of storage capacitors when the number of levels increases.
- Packaging difficulties for a high number of levels due to the presence of a large number of capacitors.
- Complex control
- High switching losses.
- The battery pack needs a BMS to balance the cells.

2.2.2.3 CHB multilevel inverters

CHB multilevel inverters have also been proposed as variable motor speed drive for traction drives of EVs. Separate batteries provide the separate dc sources needed by this converter [56]-[63]. The CHB consists of a number of series connected H-bridge converters, where each bridge is connected to a separate dc source. Fig. 2.23 shows the basic structure of a three-phase CHB inverter; all the phase legs are identical. If each leg consists of n series connected H-bridge converters, the number of levels of the line-to-line voltage waveform is $n + 1$. The phase output voltage is the sum of H-bridge converters outputs. Each bridge generates three different output voltages, $\pm V_{dc}$ and zero, through different combinations of the four switches, S_1, S_2, S_3, and S_4 [48], [53], [69].

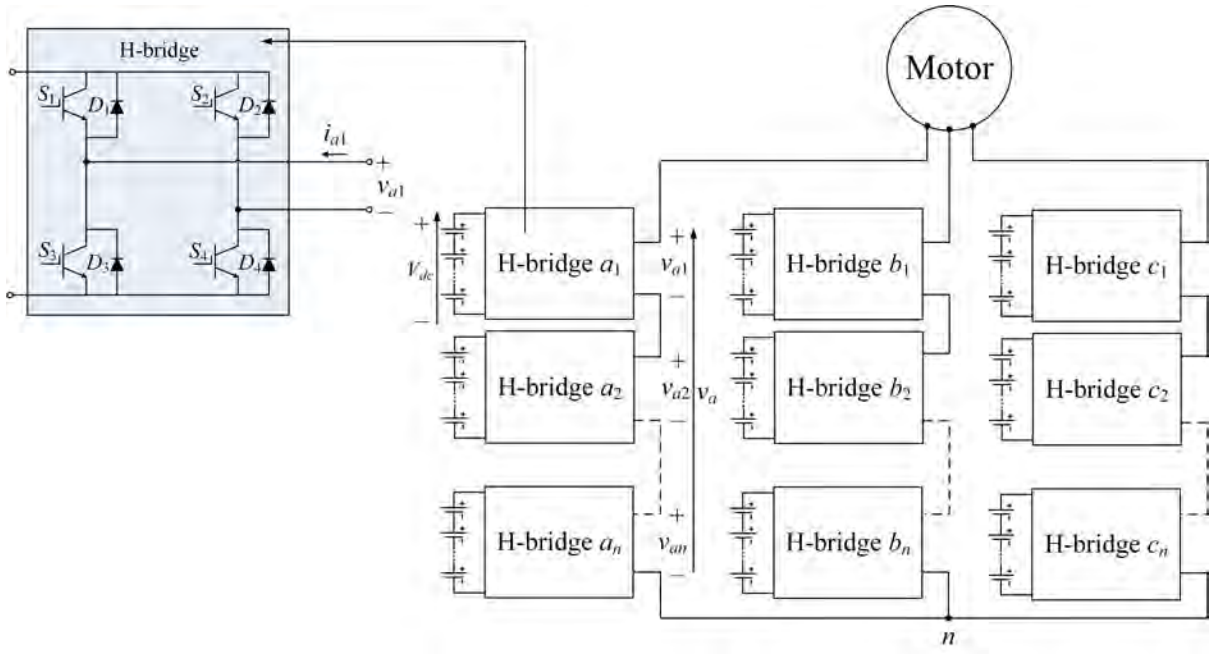


Fig. 2.23: The circuit diagram of the CHB inverter.

The major advantages of CHB multilevel inverters are:

- In comparison to two-level-inverters, the harmonic content decreases as the number of levels increases and filtering requirements are reduced.
- In comparison to NPC inverters, CHB inverters require a lower number of components to obtain the same number of output voltage levels.
- Optimized circuit layout and packaging are possible, because each level has the same structure.
- The switching devices have equal ratings.
- Soft switching techniques can be used to reduce switching losses and device stresses
- It has fault tolerant capabilities and can work with a reduced number of levels in case of a fault bypassing the faulty module.

The major disadvantages of the CHB multilevel inverters are:

- It needs separate dc sources, but this is not a problem for battery EVs.

- When batteries are used as dc sources instead of cells, the difference between the cells and recharge and discharge cycles lead to unequal SOCs of cells within the batteries. Therefore, an external BMS is needed for each battery.
- The CHB topology does not allow the recharge the battery units either from dc or single phase ac power sources.
- In Y-connected CHB, it is difficult to balance the converter legs using circulating currents, because this will result in distorted motor currents. This disadvantage is partially mitigated by D-connected CHB where zero-sequence current can be used. However, it is not possible to balance independently the converter legs because the same zero sequence current will flow through the three legs.

2.2.2.4 Modular multilevel inverters

Modular multilevel inverter has been firstly proposed in [71], where the authors have described the basic concept of the converter using the modular arm structure, along with the operating principle and performance of the converter under an ideal condition. Siemens has a plan of putting it into practical use with the trade name "HVDC-plus". It was reported in [72] that the system configuration of the HVDC-plus has a power rating of 400 MVA, a dc-link voltage of ±200 kV, and a stack of 200 cascaded chopper-cells per leg. Because of easy assembling and flexibility in converter design, the modular multilevel inverter is especially suitable to high-power converters for medium-voltage motor drives [73]-[76], high-voltage STATic synchronous COMpensator (STATCOM), back-to-back systems, etc.

Fig. 2.24 shows the basic structure of a three-phase modular multilevel inverter; all the phase legs are identical. If each leg consists of n series connected half bridge converters, the number of levels of the line-to-line voltage waveform is $n + 1$ where each voltage level can be

synthesized by turning n submodules simultaneously in each phase leg. The number of capacitors required for three-phases is $6n$ ($2n$ per phase), while no clamping diodes are required. For a dc bus of V_{dc}, the voltage across each capacitor is V_{dc}/n and each switching device voltage stress is limited to one capacitor voltage. Therefore, the voltage across each capacitor and switching device is limited to V_{dc}/n. The number of capacitors required for three-phases is $6n$ ($2n$ per phase), while no clamping diodes are required. Each half bridge generates two different output voltages, V_{dc}/n and zero, when the switching device S_1 is turned on and S_2 is turned off, the voltage $v_{at1} = V_{dc}/n$; when the switching device S_1 is turned off and S_2 is turned on, the voltage $v_{at1} = 0$.

The major advantages of modular multilevel inverters are:

- In comparison to two-level-inverters, for a large number of voltage levels extremely low total harmonic distortion can be achieved without the need for filters.
- In comparison to NPC inverters, modular multilevel inverters require a lower number of components to obtain the same number of output voltage levels.
- It has a feature of modularity design; it can be extended to any number levels
- It has failure management capability in the case of device failures.
- It has low voltage stress on switching device.
- The capacitor voltage balance is attainable for any number of voltage levels.
- The switching devices have equal ratings.
- Soft switching techniques can be used to reduce switching losses and device stresses
- The CHB topology does not allow the recharge the battery units either from dc or single phase ac power sources.

- It is easy to balance the converter legs using circulating currents without distorting motor currents.

The major disadvantages of the CHB multilevel inverters are:

- The battery pack needs a BMS to balance the cells.
- It needs a special care to be taken for starting and operation at low motor speeds, where the low-frequency current may cause an energy pulsation and a significant unbalance between the converter sub-module capacitor voltages and then disturb the output waveforms.

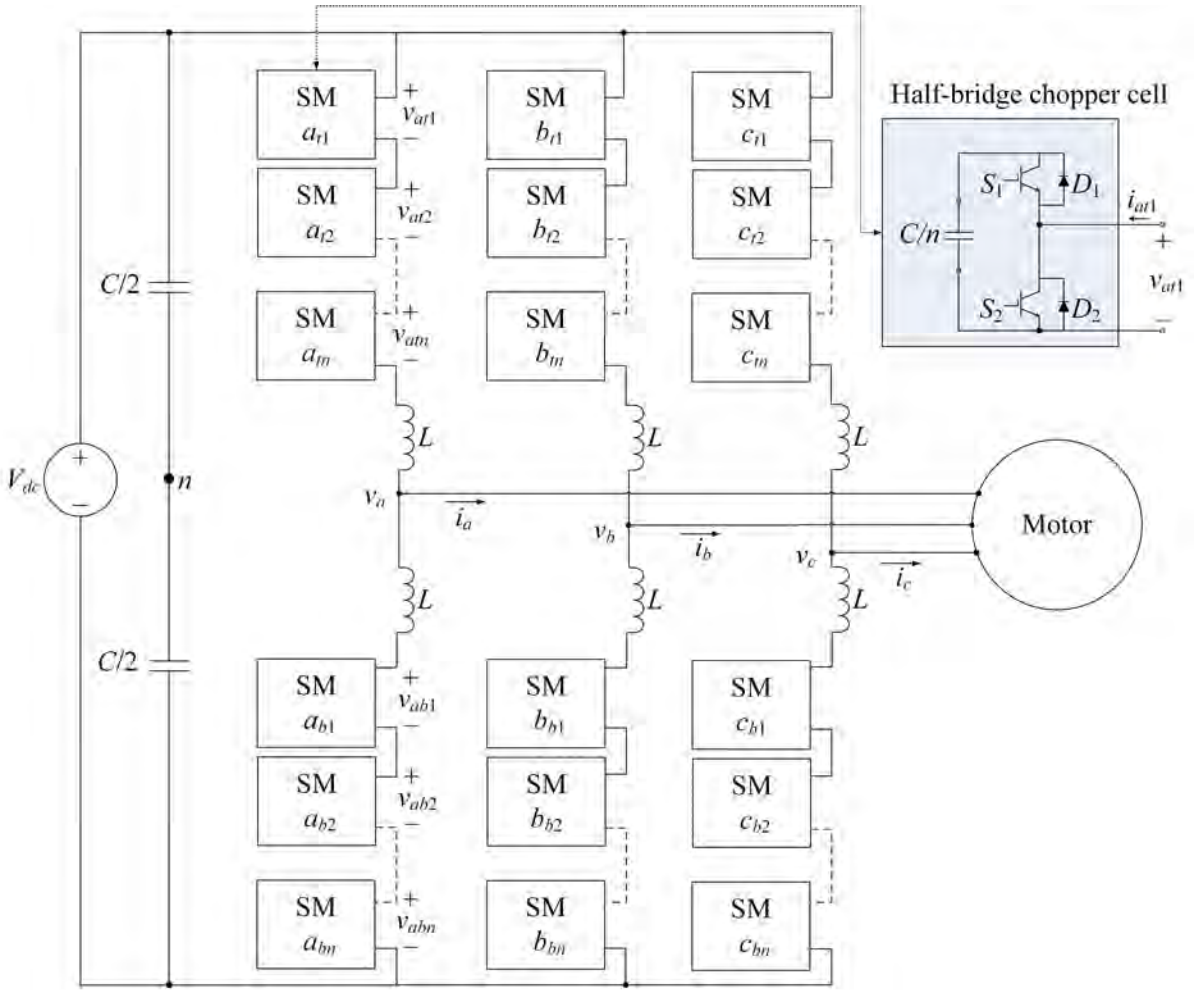


Fig. 2.24: The circuit diagram of the typical modular multilevel inverter.

A significant improvement to the present state of the art could be done adopting modular multilevel converter (MMC), which is proposed by the present PhD project. MMC can be successfully applied as a main converter for EVs, with the additional possibility of using the same converter to recharge the battery with a cell charging equalisation method. For motoring operations, the proposed solution is theoretically capable of avoiding completely the need of a BMS. In this new approach, cell balancing is obtained at the same time of the energy conversion, by loading more the cells with higher SOC and less that with lower SOC [3], [77]-[79]. The following chapters will describe in details the characteristics of these inverters and their applicability to HEVs and EVs.

Chapter 3

Converter Structure and Mathematical Modelling

This chapter describes the structure and the operating principle of the proposed MMC and the mathematical model used for the control design. The model includes a circuit-oriented model of the battery cells with a focus on Li-Ion batteries that are widely used today for EV applications. The modulation techniques used for the control of the proposed MMC and the estimation of the reliability are also discussed.

3.1 Converter structure and operating principle

The block diagram of the proposed power converter is shown in Fig. 3.1. Unlike traditional MMCs the power is supplied by the SMs and, hence, the dc bus bars are electrically isolated. The converter drives an ac traction motor, which is assumed to be a three-phase induction motor. The battery cells within the MMC can be recharged from a three-phase or a single-phase ac power supply via the charge switch that disconnects the motor during the recharge mode. Alternatively, the battery cells can be recharged by a dc source connected to the dc busbars. The conventional traction drive and its active BMS are replaced by the proposed MMC such that the traditional BMS is replaced by the control of the converter.

Each phase-leg of the converter consists of two arms of multiple SMs where each SM consists of bidirectional half bridge converters with floating electrochemical cell. The operating principle of the bidirectional half-bridge chopper cell is explained by the inset of the

schematic of Fig. 3.1. When the auxiliary switch S_a is turned on, the output voltage, v_o, is equal to the cell voltage, v_{cell}. If the main switch S_m is turned on instead, v_o is equal to zero. Table 3.1 shows the four possible switch states of the half bridge chopper cell [53].

Table 3.1:The switch states of the half bridge chopper module.

S_m	S_a	v_0	current direction	power path	cell's state
1	0	0	$i_0 > 0$	S_m	unchanged
1	0	0	$i_0 < 0$	S_m	unchanged
0	1	v_{cell}	$i_0 > 0$	S_a	discharging
0	1	v_{cell}	$i_0 < 0$	S_a	charging

The voltage of SMs is equal to the cell voltage and, hence, low voltage MosFETs can be used as power devices to reduce conduction and switching losses. The arms of the converter are connected by means of two uncoupled buffer inductors to limit the circulating currents due to voltage mismatch between the total voltages of the phase-legs [7], [80].

If the arm contains n SMs, the output line-to-line voltage has $n + 1$ levels. The two arms within the same leg are controlled in a complementary way in order to keep the voltage between the positive and the negative busbars constant, so that $n_{kt} + n_{kb} = n$, where n_{kt} and n_{kb} are the number of active SMs in the top and bottom arms respectively [81]. Therefore, the maximum voltage on each arm is nv_{cell}, being v_{cell} the nominal voltage of a single electrochemical cell.

The current through the arm, which includes one half of the load current and the circulating current within the converter phase-legs, flows through the cells when the corresponding SMs are connected to the phase-leg and the direction of the current affects the SOC of the cell.

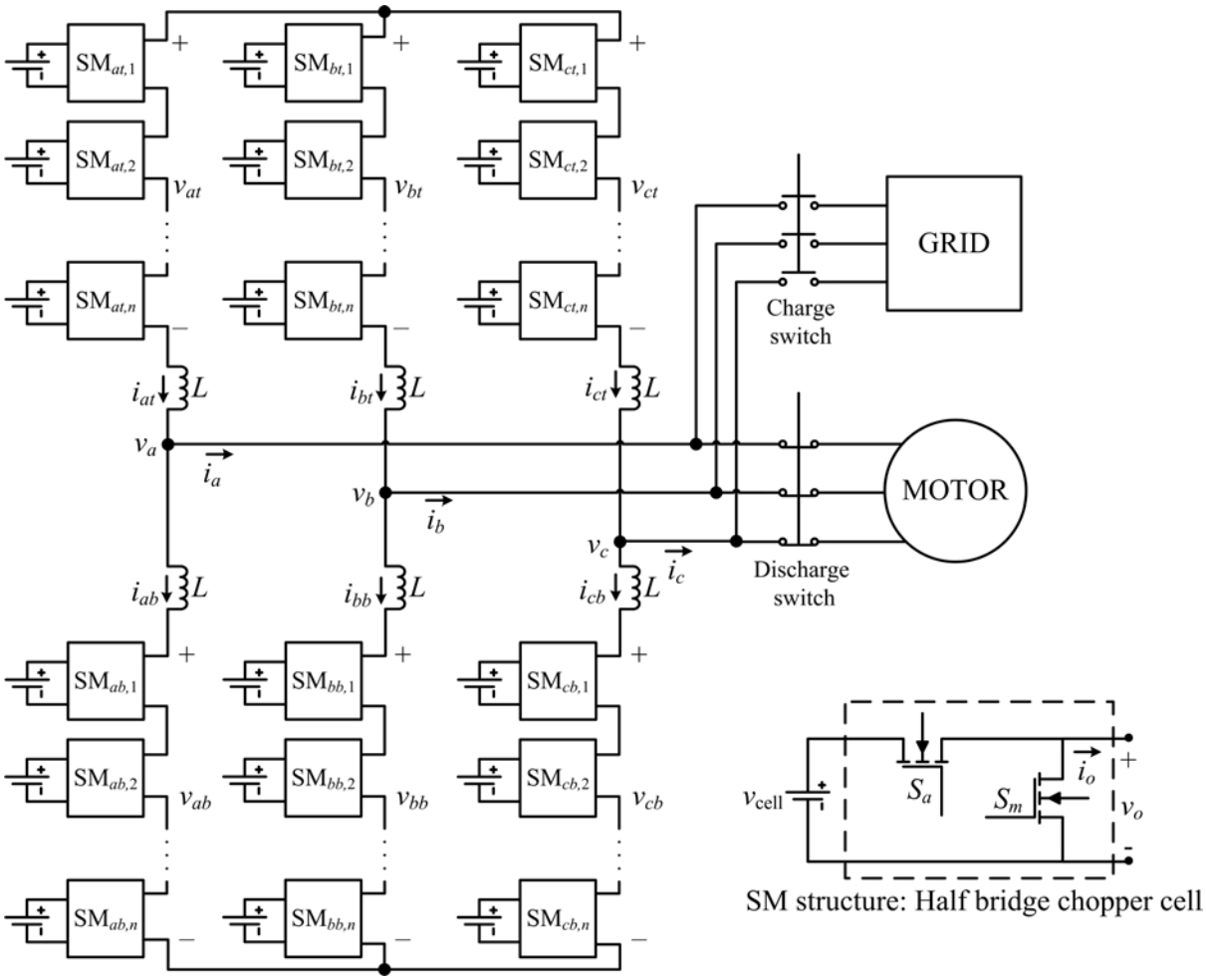


Fig. 3.1: Block diagram of the proposed power converter.

3.2 Converter mathematical model:

The top and bottom arm currents, i_{kt} and i_{kb}, of the phase k ($k = a, b, c$) can be expressed as [81]:

$$i_{kt} = i_{cir,k} + \frac{1}{2} i_k; \quad i_{kb} = i_{cir,k} - \frac{1}{2} i_k, \tag{3.1}$$

where i_k is the phase k current and $i_{cir,k}$ is the phase k circulating current which can be expressed as:

$$i_{cir,k} = \frac{i_{kt}}{2} + \frac{i_{kb}}{2}. \tag{3.2}$$

Using the single phase equivalent circuit of the converter in Fig 3.2, The voltage of the top and bottom arms, v_{kt} and v_{kb}, of the generic phase k, in the hypothesis of balanced cells, can be expressed as:

$$\begin{gathered} v_{kt} = \frac{nv_{\text{cell}}}{2} - v_k - v_{L,kt}; \quad v_{kb} = \frac{nv_{\text{cell}}}{2} + v_k - v_{L,kb} \\ -\frac{nv_{\text{cell}}}{2} \le v_k \le \frac{nv_{\text{cell}}}{2} \end{gathered}, \tag{3.3}$$

where v_k is the phase voltage of the phase k, and $v_{L,kt}$ and $v_{L,kb}$ are the voltage drop across top and bottom buffer inductors, L, which are given by:

$$v_{L,kt} = v_{L,cir,k} + v_{L,k} = L\frac{di_{cir,k}}{dt} + \frac{L}{2}\frac{di_k}{dt}; \quad v_{L,kb} = v_{L,cir,k} - v_{L,k} = L\frac{di_{cir,k}}{dt} - \frac{L}{2}\frac{di_k}{dt}. \tag{3.4}$$

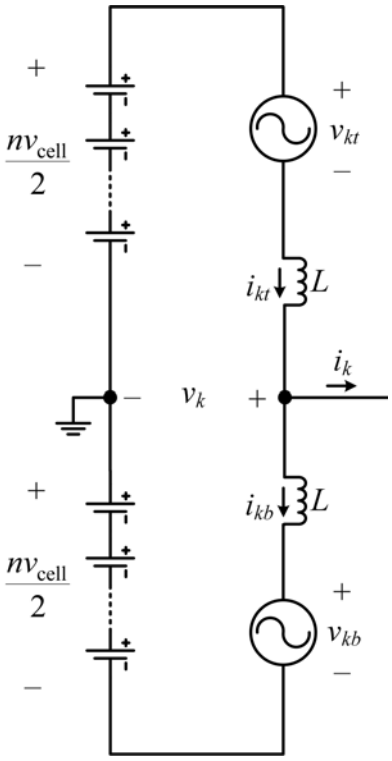


Fig. 3.2: Single phase equivalent circuit of the proposed converter.

Using (3.3) and (3.4), the mathematical model of the proposed MMC can be described by:

$$L\frac{di_{cir,k}}{dt}=\frac{nv_{\text{cell}}}{2}-\left(\frac{v_{kt}+v_{kb}}{2}\right);\quad v_k=\left(\frac{v_{kt}-v_{kb}}{2}\right)-\frac{1}{2}L\frac{di_k}{dt}. \tag{3.5}$$

3.3 Converter modulation techniques

The modulation techniques used for the proposed MMC are based on pulse width modulation and they can be classified into three schemes: carrier disposition-sinusoidal pulse width modulation (CD-SPWM), carrier disposition-third harmonic injection pulse width modulation (CD-THIPWM), and phase shifted carrier-sinusoidal pulse width modulation (PS-SPWM) schemes.

3.3.1 CD-SPWM

In order to produce a waveform with n + 1 levels, the CD-SPWM technique requires n in-phase carrier waveforms displaced symmetrically with the same carrier frequency f_c and amplitude, but with 2/n offset. Fig. 3.3 illustrates the CD-SPWM waveforms for n + 1 levels.

The sinusoidal reference waveforms, v_a^*, v_b^* and v_c^*, can be expressed as:

$$v_k^*=m\sin(\theta_k);\quad \begin{bmatrix}\theta_a & \theta_b & \theta_c\end{bmatrix}^T=\begin{bmatrix}\omega t & \omega t-2\pi/3 & \omega t+2\pi/3\end{bmatrix}^T, \tag{3.6}$$

where ω is the angular frequency of the modulating wave and m is the modulation index, which is defined for the proposed MMC as conventional multilevel inverters [82]-[84]:

$$m=\frac{2V_m}{nv_{\text{cell}}};\quad 0\le m\le 1, \tag{3.7}$$

where V_m is the amplitude of the phase voltage. Thus, the maximum rms value of line-to-line output voltage of the MMC, $V_{\max}$, is:

$$V_{\max}=\sqrt{\frac{3}{8}}nv_{\text{cell}}. \tag{3.8}$$

By comparing the sinusoidal reference waveforms with the n carrier waveforms, the voltage level at the ac-side of the MMC is determined [53]. It can be noticed by Fig. *3.3* that the CD-SPWM technique reduces the effective switching frequency per cell by the factor $1/n$, whereas the overall switching frequency is equal to the assigned carrier frequency.

Fig. 3.4 shows an illustration of the 'gear changing' of the switching frequency f_{sw} with the fundamental frequency. At low speeds, where the effect of the difference in the number of carrier cycles per each modulation cycle is small, asynchronous modulation is applied. At moderate and high speeds, the carrier signals and the modulating wave are synchronized and the modulation frequency decreases in steps as the frequency increases to prevent the introduction of undesirable sub-harmonics [85].

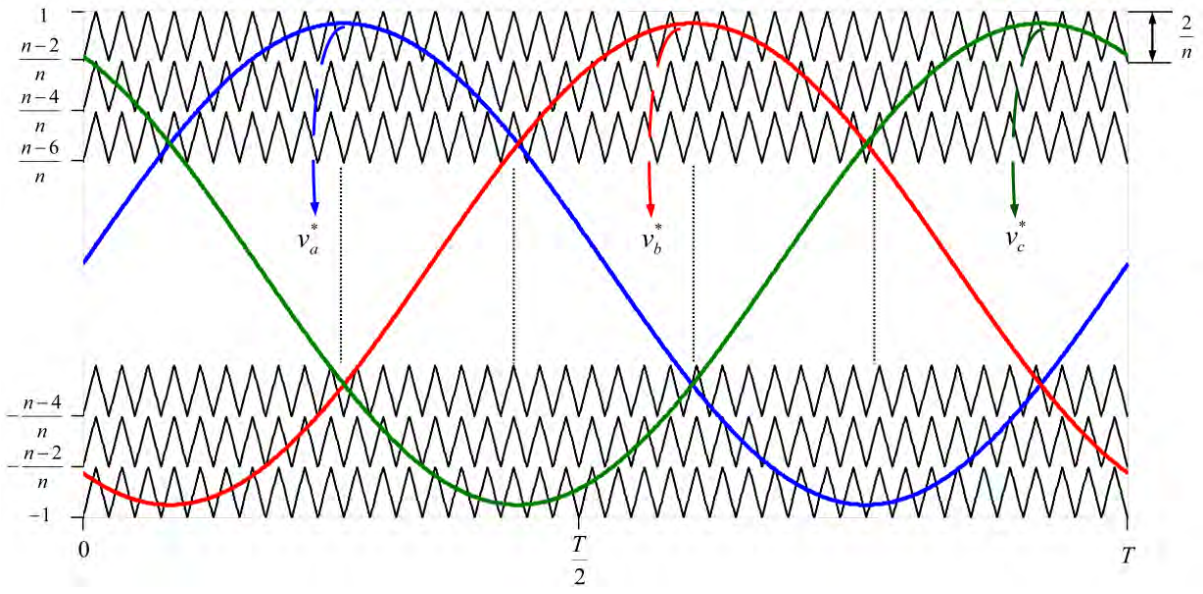


Fig. 3.3: The carrier disposition SPWM scheme.

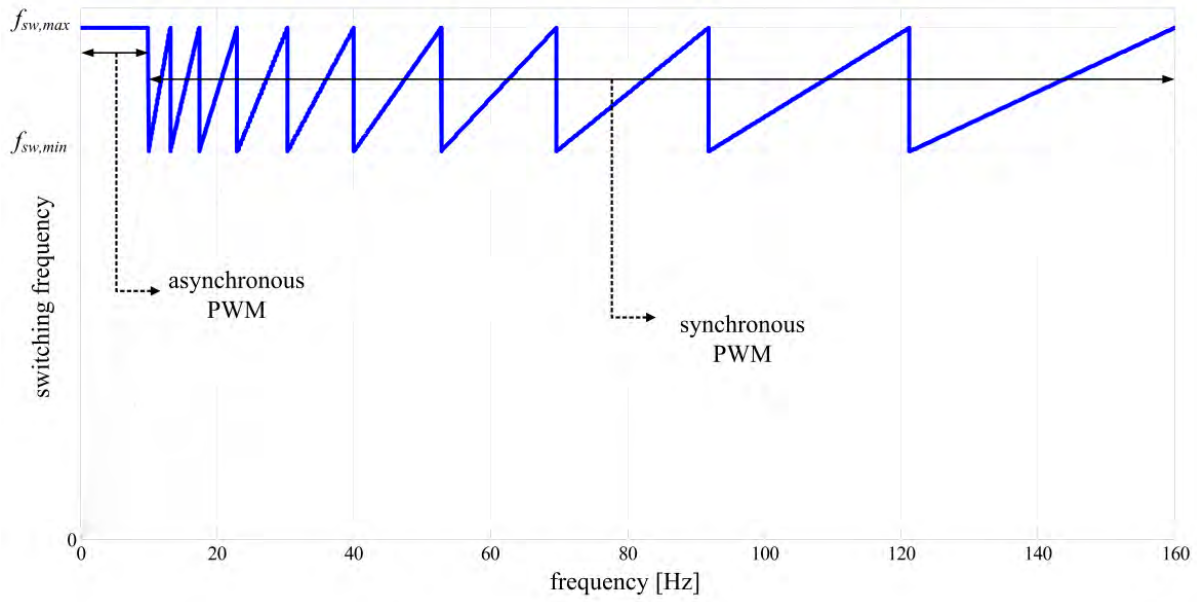


Fig. 3.4: Illustration of the 'gear changing' in SPWM.

3.3.2 CD-THIPWM

To extend the linear operating range of the SPWM strategy and increase the fundamental component of the ac-side line voltages of the MMC without causing over-modulation, a third-harmonic component can be included in the modulating reference signal, as shown in Fig. 3.5. In this case, the sinusoidal reference waveforms, v_a^*, v_b^* and v_c^*, are expressed as:

$$v_k^* = m[\sin(\theta_k) + h\sin(3\theta_k)]; \quad [\theta_a \quad \theta_b \quad \theta_c]^T = [\omega t \quad \omega t - 2\pi/3 \quad \omega t + 2\pi/3]^T, \quad (3.9)$$

where h is the proportion of the injected third harmonic component with respect to the fundamental.

The limit of a third-harmonic to avoid over-modulation can be calculated differentiating the sinusoidal reference waveform v_a^* in (3.9) with respect to θ_a and equalling to zero [86].

$$\frac{dv_a^*}{d\theta_a} = m[\cos(\theta_a) + 3h\cos(3\theta_a)] = 0, \quad (3.10)$$

This equation is satisfied when $\theta_a = \pi/3$, i.e. when the third harmonic crosses zero and this yields:

$$h = \frac{1}{6}. \tag{3.11}$$

Replacing (3.11) in (3.9) and considering that at $\theta_a = \pi/3$, the value of v_a^* has to be equal to the carrier maximum value, i.e., $v_a^*(\pi/3) = 1$, the following solution is obtained:

$$v_a^*\left(\frac{\pi}{3}\right) = m\left[\sin\left(\frac{\pi}{3}\right) + \frac{1}{6}\sin(\pi)\right] = 1 \Rightarrow m = \frac{2}{\sqrt{3}}. \tag{3.12}$$

In summary, the maximum value of the fundamental component of the reference can be increased by 16%, and the necessary third harmonic component will be 1/6. In this case, the CD-THIPWM strategy reduces the number of required SMs to generate the same voltage when the CD-SPWM used by a factor of 13.5 %. This will lead to reduction in the size, cost, switching and conduction losses of the proposed converter.

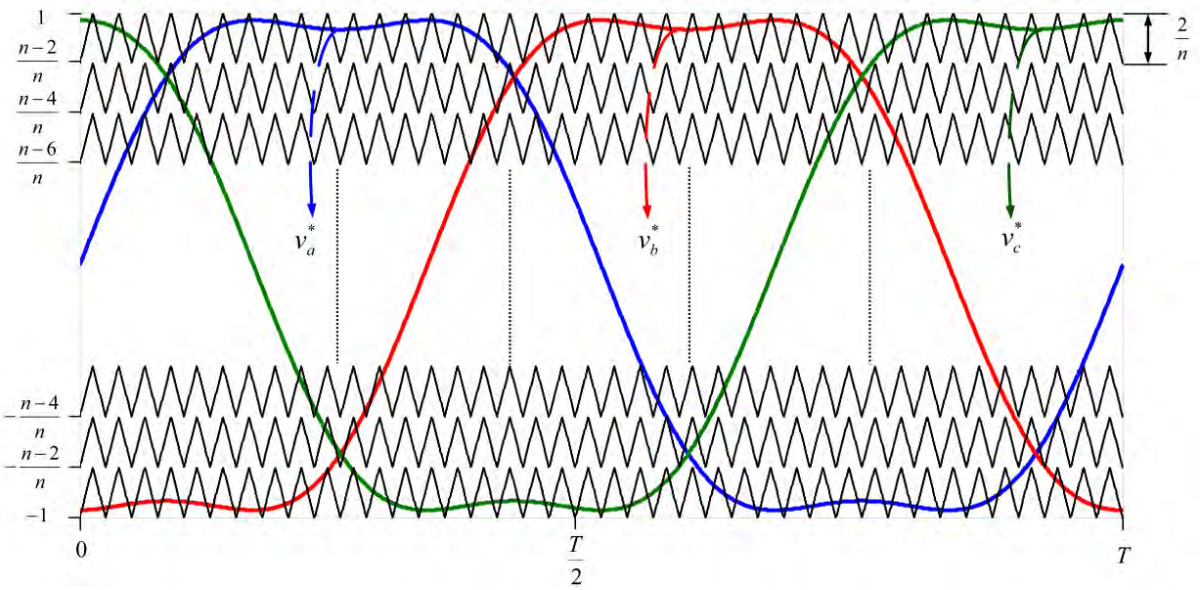


Fig. 3.5: Carrier disposition-third harmonic injection PWM scheme.

3.3.3 PSC-SPWM

The PSC-SPWM is a modulation technique used to separately control each arm of the MMC. In this modulation strategy, the sinusoidal reference waveforms are compared with triangular waveforms as shown in Fig. 3.6. The n chopper-cells per each arm have n triangular waveforms ($v_{c,1}$, $v_{c,2}$,… and $v_{c,n}$) with the same carrier frequency but a phase difference of $2\pi/n$ to achieve the harmonic cancellation and enhance current controllability because each SM has its own carrier signal and therefore it can be controlled independently from the other SMs in the same arm [85].

It can be noticed from Fig. 3.6 that the PSC-SPWM technique increases the switching frequency per each SM significantly, because the switching frequency of each SM is equal to the carrier frequency. Therefore, the overall switching frequency is increased by a factor $2n$, i.e. the overall switching frequency is equal to $2nf_c$. Consequently, the MMC switching losses increase by a factor $2n$ in comparison to the case of CD-SPWM.

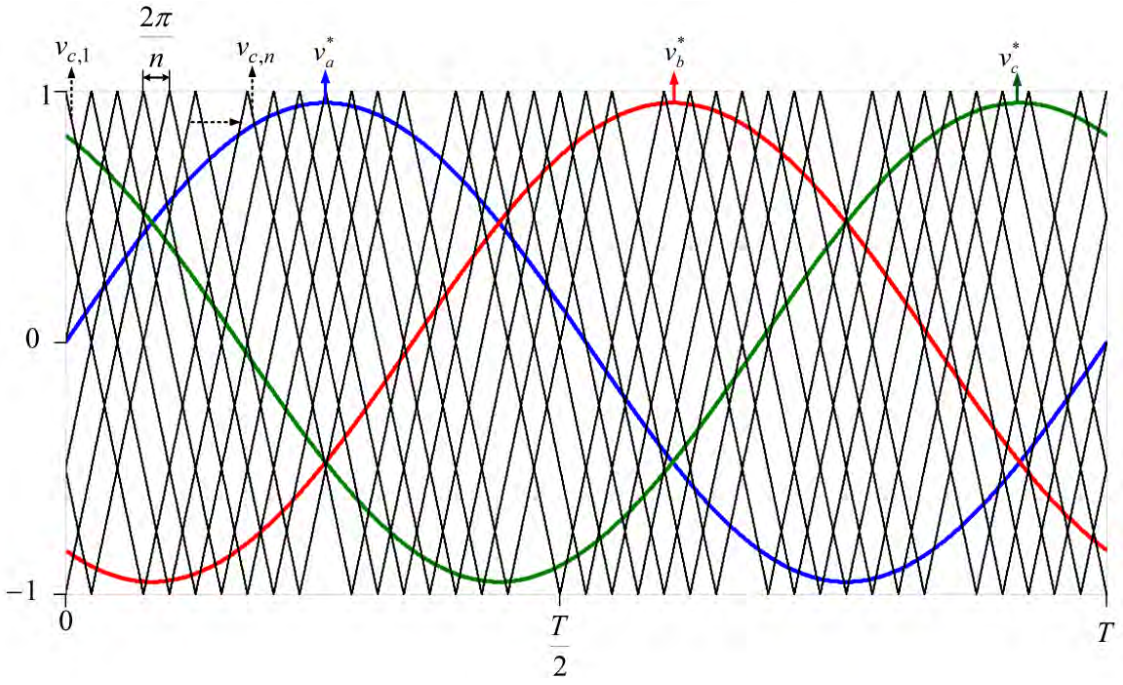


Fig. 3.6: Phase shifted carrier SPWM strategy.

3.4 Electrical model of battery cells

Li-ion batteries are commonly used in electric vehicles because of their high specific energy in comparison with other battery cells, such as nickel-cadmium, nickel metal hydrides and lead acid [87].

The state of charge of a battery is a quantity that is used to represent the residual electrical charge available from a battery. The SOC is expressed as a percentage of the maximum available capacity of the battery [88]:

$$\mathrm{SOC} = \frac{Q_{\mathrm{available}}}{Q}, \tag{3.13}$$

where $Q_{\mathrm{available}}$ is the available capacity of battery in [Ah] and Q is the maximum available capacity in [Ah].

The SOC of a battery can be estimated by integrating the battery current [106]:

$$\mathrm{SOC} = \frac{q_i - q}{Q} = \mathrm{SOC}_i - \frac{1}{3600Q}\int idt, \tag{3.14}$$

where q_i is the initial charge of battery in [Ah], q is the extracted capacity in [Ah], SOC_i is the initial state of charge in [%], and i is the current of the battery in [A].

In this thesis, the battery cells are modelled based on a dynamic model with parameters that are specific of the type of battery. Fig. 3.7 shows a typical discharge characteristic for a Li-ion cell. Following the approach of this theory, the mathematical model of a battery cell can be expressed by [89]:

$$\begin{aligned} V_{\mathrm{dis}} &= E_0 - Ri - K\frac{Q}{Q-q}i^* - K\frac{Q}{Q-q(t)}q + Ae^{-Bq}; \quad i^* > 0 \\ V_{\mathrm{ch}} &= E_0 - Ri - K\frac{Q}{0.1Q+q}i^* - K\frac{Q}{Q-q}q + Ae^{-Bq}; \quad i^* < 0 \end{aligned}, \tag{3.15}$$

where all quantities are defined in Table 3.2.

Table 3.2: Explanation of quantities of equation (3.15).

V_{dis}	V	Battery voltage during discharge process
V_{ch}	V	Battery voltage during charge process
E_0	V	Battery constant voltage
R	Ω	Battery internal resistance
i	A	Battery current
i^*	A	Low frequency current dynamics
K	V/Ah	Polarization constant
q	Ah	Extracted capacity
A	V	Exponential zone amplitude
B	Ah^{-1}	Exponential zone time constant inverse

The mathematical analysis is valid under the following conditions:

- the internal resistance of the cell is constant during the charge and discharge cycles and does not vary with the current;
- the temperature does not affect the model;
- the model parameters deduced from the discharge characteristic are valid also for the charge characteristic;
- the capacity of the battery does not change with the current;
- the self-discharge of the battery is not represented.

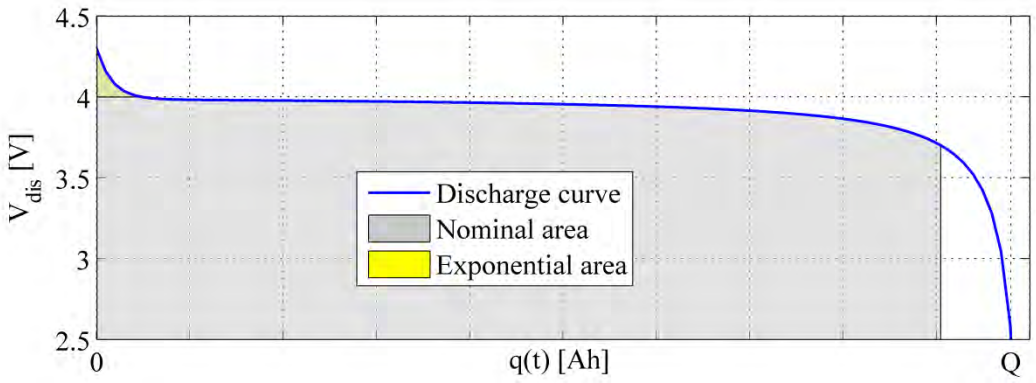


Fig. 3.7: The typical discharge curve of Li-Ion cell.

3.5 Analysis of reliability and availability

Traditional two-level inverters have six power devices that include a fully controlled switch and a freewheeling diode. When a fault occurs in one of the devices, the functionality of the converter is compromised, because the other device in the same leg cannot be operated to avoid the short circuit of the dc link. Therefore, the inverter must be stopped immediately and sent to maintenance. The probability of occurrence of a fault defines the reliability of the converter. In order to calculate the reliability, a simple mathematical model can be introduced. For simplicity, the controlled device and the diode are considered as one single element. Moreover, the devices are considered equal with the same individual reliability. Using these assumptions, the reliability of the two-level inverter is given by [77]:

$$R = p^6, \tag{3.16}$$

where p is the static reliability of a single device. Equation (3.16) is obtained from the consideration that all the six devices need to be healthy to have a working converter.

For the modular multilevel converter, the fault of a device does not compromise the entire converter, because the cell affected by the fault can be always connected or bypassed. If reference is made to the case when the cell is bypassed, the arm with the fault has $n - 1$ levels instead of n. Therefore, the converter can keep working with an unbalance of the output voltage. Alternatively, the converter can keep working with balanced output voltage but with a lower amplitude. This is because the voltages can be kept balanced by operating all the arms with $n - 1$ levels. Therefore, the reliability of the converter is a function of the power output required. In particular, if the nominal power of the converter is P_n and the power required is in the range [77]:

$$\frac{k-1}{n} P_n \leq P \leq \frac{k}{n} P_n, \tag{3.17}$$

at least k modules must be healthy in the arm. In order to have a module healthy, both the switches must be working properly. Therefore, the reliability of each module is p^2. The theory on partial redundancy gives the static reliability of the converter in this case [77]:

$$R = \left[\sum_{i=k}^{n} \binom{n}{i} \left(p^2\right)^i \left(1 - p^2\right)^{n-i} \right]^6. \tag{3.18}$$

The two reliabilities have been compared to understand the effect of the presence of redundancies in modular multilevel converters, selecting a number of level $n = 45$. The results are shown in Fig. 3.8 [77].

The figure clearly shows that the reliability of modular multilevel converters is greater than that of two-level inverters for a large range of the output power. When the full power is required, all the levels must be working and therefore the reliability of modular multilevel converter is lower, due to the higher number of devices. For a low value of device's reliability, modular multilevel converters are superior up to a power of 75% of the nominal power, whereas for a high value of device's reliability, they are superior up to a power of 93%. For two-level inverters the reliability of the converter is strongly affected by the reliability of the devices. For modular multilevel converters instead, the reliability is always the same irrespective of the value of p, at least for a large range of the output power [77].

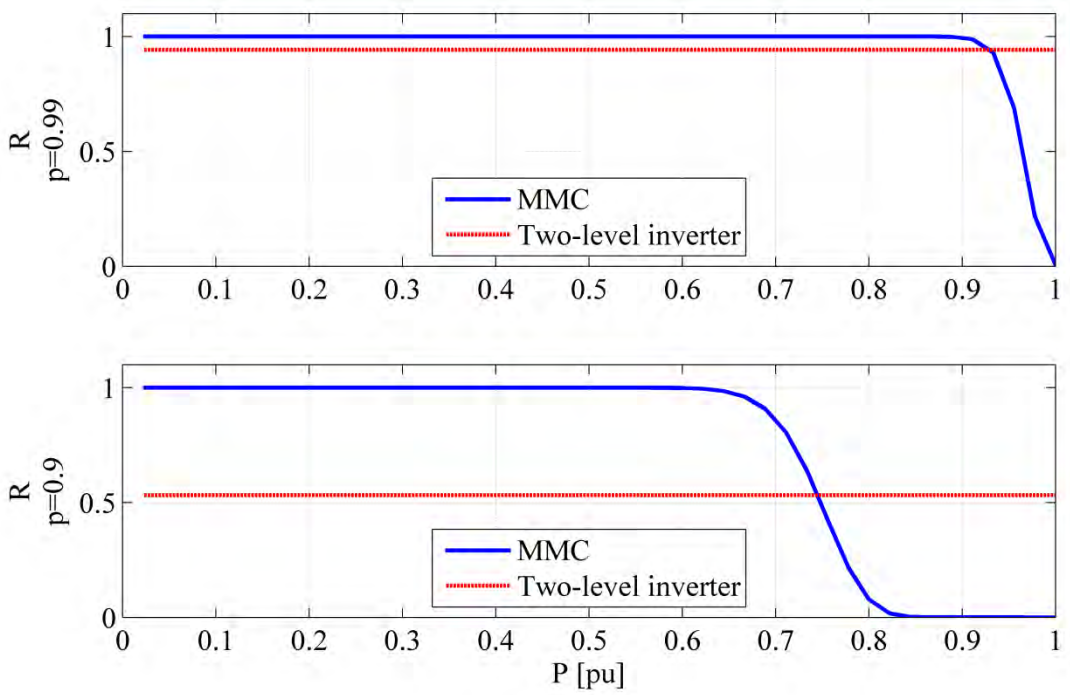


Fig. 3.8: The reliability of two-level and modular multilevel converters for $p = 0.99$ and $p = 0.9$ [77].

The comparison of the failure rates of the converters requires the selection of an appropriate model for the failure rate of the devices. However, power MosFETs are complicated semiconductor devices and an accurate estimation of the model is outside the scope of this research. However, it is possible to carry out an approximated analysis using the simple exponential model distribution. In this model, the failure rate is constant and, therefore, it neglects the ageing effects due to temperature stresses typical of power switches. Nevertheless, the exponential model allows some analytical calculations and it can give a starting point for further investigations. Therefore, the reliability of each switch is given by the following function of the time [90]:

$$p = e^{-\lambda t}, \tag{3.19}$$

where λ is the failure rate, supposed to be constant if the effect of temperature is neglected. The failure rate can be approximated by the following equation [90]:

$$\lambda = \left(C_1\pi_T + C_2\pi_E\right)\pi_Q\pi_L, \tag{3.20}$$

where λ is expressed in 10^{-6} [h^{-1}] and the meaning of the various coefficients are given in Table 3.3 [90]:

Table 3.3: The coefficients of failure rate.

Coefficients	Description	Switch for BEVs	Two-level inverter	MMC
C_1	Die complexity failure rate	MOS linear	0.01	0.01
C_2	Package failure rate	3 pin, surface mount technology	0.00092	0.00092
π_T	Temperature factor	MOS linear	58	5.2
π_E	Environmental factor	Ground, mobile	4	4
π_Q	Quality factor	Class B categories	1	1
π_L	Learning factor	> 2 year in production	1	1

The temperature factor can be calculated using the following formula [90]:

$$\pi_T = 0.1\exp\left[-7543.2\left(\frac{1}{T_j + 273} - \frac{1}{298}\right)\right], \tag{3.21}$$

where T_j is the worst case device junction temperature in [°C]. The equation shows that the device that allows operating at higher T_j, it will have higher temperature factor and then higher failure rate.

For the temperature factor, a junction temperature of 125ºC has been considered for the devices of the two-level inverter. However, the devices of the modular multilevel converter work with a different junction temperature due to the different switching frequency. Assuming a switching frequency equal to one tenth of that of the two-level inverter, the temperature rise of the MMC power switches due to switching and conduction losses is 55% of that of the two-level inverter. (A more accurate description on how to estimate the converter losses for both

topologies will be discussed later in chapter five). Assuming an ambient temperature of 25ºC, the junction temperature would be 80ºC. Using the coefficients of Table 3.3, the failure rates for the two level and modular multilevel inverters are respectively $\lambda_1 = 0.58\times10^{-6}$ [h^{-1}] and $\lambda_2 = 0.088\times10^{-6}$ [h^{-1}].

For the two-level inverter, the six power switches are connected in series from the reliability point of view, because all of them are necessary to let the converter working. The mean time between failures, MTBF, is then given by:

$$\mathrm{MTBF} = -\int_0^\infty t\frac{d}{dt}\left(e^{-6\lambda_1 t}\right)dt = \int_0^\infty \left(e^{-6\lambda_1 t}\right)dt = \frac{1}{6\lambda_1}. \tag{3.22}$$

For the modular multilevel converter, the MTBF is given by:

$$\begin{aligned}\mathrm{MTBF} &= -\int_0^\infty t\frac{d}{dt}\left[\sum_{i=k}^{n}\binom{n}{i}e^{-2i\lambda_2 t}\left(1-e^{-2\lambda_2 t}\right)^{n-i}\right]^6 dt \\ &= \int_0^\infty\left[\sum_{i=k}^{n}\binom{n}{i}e^{-2i\lambda_2 t}\left(1-e^{-2\lambda_2 t}\right)^{n-i}\right]^6 dt.\end{aligned} \tag{3.23}$$

Fig. 3.9 compares the MTBFs of the two converters. Due to the partial redundancy, the modular multilevel converter presents a longer MTBF up to 92% of the converter's nominal power. When higher power is required continuously, all the switches of the converter are needed at the same time and, therefore, a failure is expected early due to the larger number of components, though the stress on each component is smaller due to the lower switching frequency. However, electric vehicles are never running at full power all the time, so that the average output power is significantly lower than the nominal value. Moreover, the MTBF expresses the mean time before the first failure. Therefore, even if that time is shorter when the modular multilevel converter operates at full power, it is still possible to keep the converter in operation with a reduced output power.

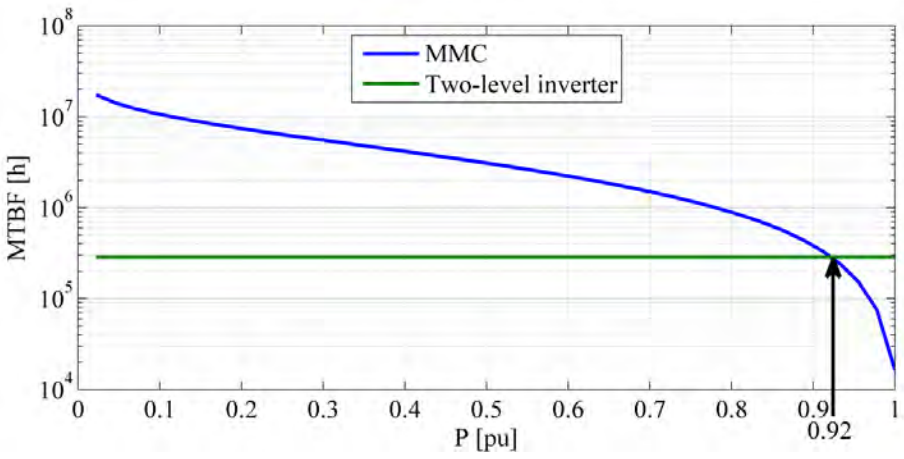


Fig. 3.9: Comparison of MTBFs of 2-level and modular multilevel converters.

In summary, the chapter introduced the topology of the new modular multilevel converter with embedded battery cells and its relevant characteristics. The converter is characterized by cascade connection of modular half bridge chopper cells with floating Li-Ion cells to form each arm. The converter allows to balance the battery cells at the same time of energy conversion. A mathematical model to depict and analyze the proposed MMC has been presented, the model includes the dynamic model of the Li-Ion battery cells. In this chapter, methods to modulate the proposed converter including CD-SPWM, CD-THIPWM, and PSC-SPWM schemes have been discussed, these modulation techniques allow the control of the proposed MMC. Finally, a detailed analysis of the converter reliability and availability in a comparison with the two-level inverter are discussed.

Chapter 4

Control Strategy of the Converter

This chapter describes the different sections of the converter controller. The main function of the control is to balance the SOC of the battery cells while the converter drives the traction motor or receives power from the grid for the recharge. This is achieved by the control of the circulating currents between the arms of the converter. The circulating current controller has the objective to balance the energy between the top and bottom arms for each leg and to balance the energy between the legs. Finally, the individual SOC controller balances the cells within an arm.

The motor is controlled by a standard vector control, whereas the recharge from the grid is based on a standard *dq* current control.

4.1 Circulating current control

The main target of the circulating current control is to achieve arm-energy balancing between the top and bottom arms for each leg and energy balancing between the converter legs. Fig. 4.1 shows the block diagram of the circulating current controller. The objective of the control is to use the circulating current to balance the energy between the arms and legs without affecting the output current.

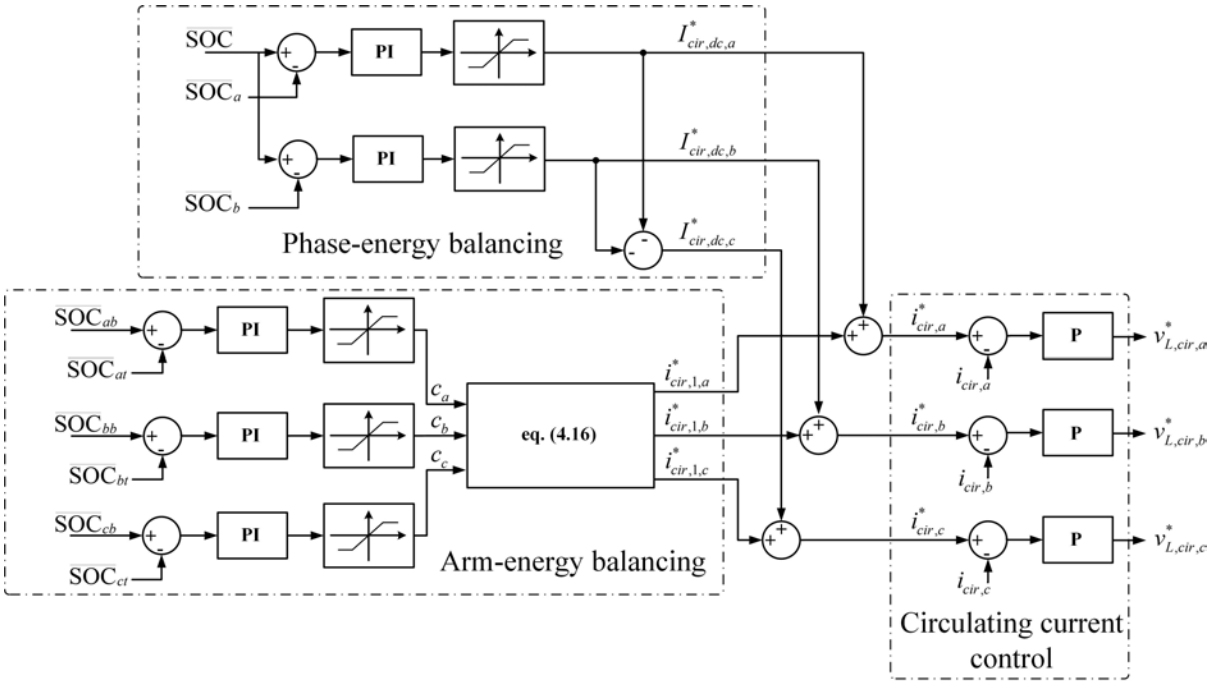


Fig. 4.1: The block diagram of circulating current controller.

4.1.1 Arm-energy balancing

The arm balancing control is needed to balance the energy stored between the top and bottom arms, i.e. reducing the difference of the energy stored between the converter arms. In order to achieve this, it is necessary to derive the relationships between the instantaneous power difference between the top and bottom arms and the converter circulating current.

The current flowing into any battery cell can be expressed in terms of the value of the cell SOC and capacity, as shown in (4.1) [77]:

$$i_{h,kt} = Q\frac{d\mathrm{SOC}_{h,kt}}{dt}; \quad i_{h,kb} = Q\frac{d\mathrm{SOC}_{h,kb}}{dt}; \quad h = 1,..., n, \tag{4.1}$$

where $\mathrm{SOC}_{h,kt}$ and $\mathrm{SOC}_{h,kb}$ are the SOCs of the h-th cell in the top and bottom arms, respectively.

Considering ideal switches, the instantaneous active power balancing on both sides of each sub-module of the top and bottom arms, in the hypothesis of balanced cells, yields [77]:

$$p_{h,kt} = v_{h,kt}\, i_{kt} = v_{\text{cell}}\, i_{h,kt} = \left(Q \frac{d\text{SOC}_{h,kt}}{dt} \right) v_{\text{cell}};$$
$$p_{h,kb} = v_{h,kb}\, i_{kb} = v_{\text{cell}}\, i_{h,kb} = \left(Q \frac{d\text{SOC}_{h,kb}}{dt} \right) v_{\text{cell}}, \tag{4.2}$$

where $v_{h,kt}$ and $v_{h,kb}$ are the h-th SM output voltages in the top and bottom arms, respectively. $i_{h,kt}$ and $i_{h,kb}$ are the h-th cell currents in the top and bottom arms, respectively.

The total instantaneous power of each arm is equal to the summation of the instantaneous active power of the individual SM of that arm [77]:

$$p_{kt} = \sum_{h=1}^{n} p_{h,kt} = i_{kt} \sum_{h=1}^{n} v_{h,kt} = \left(Q \sum_{h=1}^{n} \frac{d\text{SOC}_{h,kt}}{dt} \right) v_{\text{cell}}$$
$$p_{kb} = \sum_{h=1}^{n} p_{h,kb} = i_{kb} \sum_{h=1}^{n} v_{h,kb} = \left(Q \sum_{h=1}^{n} \frac{d\text{SOC}_{h,kb}}{dt} \right) v_{\text{cell}} \tag{4.3}$$

The instantaneous power of each arm can be also expressed as a function of the average SOC for the top and bottom arm of phase k as shown in (4.4) [77]:

$$p_{kt} = i_{kt} v_{kt} = nQ v_{\text{cell}} \frac{d\overline{\text{SOC}}_{kt}}{dt}; \quad p_{kb} = i_{kb} v_{kb} = nQ v_{\text{cell}} \frac{d\overline{\text{SOC}}_{kb}}{dt}, \tag{4.4}$$

where $\overline{\text{SOC}}_{kt}$ and $\overline{\text{SOC}}_{kb}$ are the average SOCs of top and bottom arms of phase k, respectively, which are given by [77]:

$$\overline{\text{SOC}}_{kt} = \frac{1}{n} \sum_{h=1}^{n} \text{SOC}_{h,kt}; \quad \overline{\text{SOC}}_{kb} = \frac{1}{n} \sum_{h=1}^{n} \text{SOC}_{h,kb}. \tag{4.5}$$

By ignoring the switching losses and considering the voltage drop across buffer inductors, the instantaneous power of each arm can be further written as:

$$p_{kt} = \underbrace{\left(\frac{nv_{\text{cell}}}{2} - v_k - L \frac{di_{kt}}{dt} \right)}_{v_{kt}} i_{kt}; \quad p_{kb} = \underbrace{\left(\frac{nv_{\text{cell}}}{2} + v_k - L \frac{di_{kb}}{dt} \right)}_{v_{kb}} i_{kb}. \tag{4.6}$$

The differential instantaneous power p_k^{Δ} of each phase-leg is given by [52]:

$$p_k^{\Delta} = p_{kt} - p_{kb}. \tag{4.7}$$

By substituting equations (4.4) and (4.6) in (4.7):

$$p_k^{\Delta} = nQv_{\text{cell}} \frac{d}{dt}\left[\overline{\text{SOC}}_{kt} - \overline{\text{SOC}}_{kb}\right] = -\frac{1}{2} n v_{\text{cell}} i_k - 2v_k i_{cir,k} - L\frac{d}{dt}(i_k i_{cir,k}). \tag{4.8}$$

Since the inductors of each phase-leg are used to filter the switching frequency harmonics, the voltage and current of the ac side of MMC can be assumed to be sinusoidal as expressed in (4.9).

$$\begin{aligned} &p_k^{\Delta} = p_{kt} - p_{kb}.v_k = V_m \sin(\theta_k); \quad i_k = I_m \sin(\theta_k - \varphi); \\ &[\theta_a \quad \theta_b \quad \theta_c]^T = [\omega t \quad \omega t - 2\pi/3 \quad \omega t + 2\pi/3]^T, \end{aligned} \tag{4.9}$$

where I_m is the peak values of the load current and φ is the phase angle. Expanding the circulating current with the Fourier series:

$$i_{cir,k} = I_{cir,dc,k} + \sum_{i=1}^{\infty} i_{cir,i,k} = I_{cir,dc,k} + \sum_{i=1}^{\infty} I_{cir,i,k} \sin(i\omega t + \gamma_{i,k}), \tag{4.10}$$

where $I_{cir,i,k}$ is the magnitude of the i-th harmonic of phase-k circulating current and $\gamma_{i,k}$ is the phase angle of that harmonic. By substituting (4.9) and (4.10) in (4.8) and ignoring the ripples due to the ac components, the difference of the powers generated by the battery cells of the top and bottom arms, p_k^{Δ}, depends only on the fundamental component of circulating current (see Appendix B.1):

$$p_k^{\Delta} = nQv_{\text{cell}} \frac{d}{dt}(\overline{\text{SOC}}_{kt} - \overline{\text{SOC}}_{kb}) \approx -V_m c_k; \quad c_k = I_{cir,1,k} \cos\gamma_{1,k}, \tag{4.11}$$

and the differential energy, E_k^{Δ}, can be calculated as:

$$E_k^{\Delta} = \int p_k^{\Delta} dt = E_{k,i}^{\Delta} + nQv_{\text{cell}}\left[\overline{\text{SOC}}_{kt} - \overline{\text{SOC}}_{kb}\right], \tag{4.12}$$

where $E_{k,i}^{\Delta}$ is the initial differential energy.

It can be noticed from (4.11) that the dc and high order components of the circulating current have no impact on the energy balance between the top and bottom arms as long as the ac voltage and current are sinusoidal without dc offset. From (4.11), it is easy to find that there are linear relationships between p_k^{Δ} and c_k at steady-state. Hence, the variable c_k can be regarded as the output of the differential energy balance controller, as shown in Fig. 4.1. Since the proposed converter has no external dc-link, the zero sequence of the reference circulating currents has to be eliminated and this can be done by adjusting $I_{cir,1,k}$ and $\gamma_{1,k}$:

$$\sum_{k=a,b,c} i_{cir,1,k} = 0 \Rightarrow \sum_{k=a,b,c} I_{cir,1,k} \sin(\omega t + \gamma_{1,k}) = 0. \tag{4.13}$$

Using sum-difference trigonometric identities, (4.13) can be re-written as:

$$\sum_{k=a,b,c} I_{cir,1,k} \cos(\gamma_{1,k}) = 0; \quad \sum_{k=a,b,c} I_{cir,1,k} \sin(\gamma_{1,k}) = 0. \tag{4.14}$$

Recalling that the output of the differential energy balance controller is:

$$c_k = I_{cir,1,k} \cos(\gamma_{1,k}). \tag{4.15}$$

To simplify the computational effort, one of the circulating current phases, say $\gamma_{1,a}$, has been set to zero and then, the previous equations can be solved for $\gamma_{1,b}$, $\gamma_{1,c}$, $I_{cir,1,a}$, $I_{cir,1,b}$, and $I_{cir,1,c}$:

$$\begin{gathered} \gamma_{1,b} = \tan^{-1}\left(\frac{c_a + c_b - 2c_c}{\sqrt{3}c_c}\right); \quad \gamma_{1,c} = \tan^{-1}\left(-\frac{c_a - 2c_b + c_c}{\sqrt{3}c_b}\right) \\ I_{cir,1,a} = c_a; \quad I_{cir,1,b} = \frac{c_b}{\cos(\gamma_{1,b})}; \quad I_{cir,1,c} = \frac{c_c}{\cos(\gamma_{1,c})} \end{gathered} . \tag{4.16}$$

4.1.2 Leg-energy balancing

The leg-energy control is also needed to balance energy stored across the three legs of the converter. The total instantaneous power p_k^{Σ} of each phase-leg is given by [52]:

$$p_k^{\Sigma} = p_{kt} + p_{kb}. \tag{4.17}$$

By substituting equations (4.4) and (4.6) in (4.17):

$$p_k^{\Sigma} = 2nQv_{\text{cell}}\frac{d\overline{\text{SOC}}_k}{dt} = -v_k i_k + nv_{\text{cell}} i_{cir,k} - L\left(i_{kt}\frac{di_{kt}}{dt} + i_{kb}\frac{di_{kb}}{dt}\right), \tag{4.18}$$

where $\overline{\text{SOC}}_k$ is the moving average SOC of phase k that can be calculated as:

$$\overline{\text{SOC}}_k = \frac{\overline{\text{SOC}}_{kt} + \overline{\text{SOC}}_{kb}}{2}. \tag{4.19}$$

Substituting (4.9) and (4.10) in (4.18), the total power flowing from/into the cells of each phase-leg will consist of several parts: a dc component and some ac components at low frequencies. Ignoring the ripples due to the ac components, the total power of the battery cell of each phase p_k^{Σ} depends on the dc component of the circulating current (see Appendix B.2):

$$p_k^{\Sigma} = 2nQv_{\text{cell}}\frac{d\overline{\text{SOC}}_k}{dt} \cong \underbrace{nv_{\text{cell}} I_{cir,dc,k}}_{P_{cir,k}} - \underbrace{\frac{1}{2}V_m I_m \cos\varphi}_{P_{\text{load}}}, \tag{4.20}$$

and the total energy stored in the cells of each phase, E_k^{Σ}, can be calculated as:

$$E_k^{\Sigma} = \int p_k^{\Sigma} dt = E_{k,i}^{\Sigma} + 2nQv_{\text{cell}}\overline{\text{SOC}}_k, \tag{4.21}$$

where $E_{k,i}^{\Sigma}$ is the initial total energy. The relation in (4.20) indicates that the energy balance between phases can be controlled by adding the component $I_{cir,dc,k}$ to the converter circulating currents.

Both leg and energy balancing controllers are decoupled and can be implemented in two separate and independent regulators. The control scheme in this thesis is based on saturated PI regulators for both the balancing functions. Since the control system is implemented in a digital manner using a field programmable gate array (FPGA), a discrete-time model is more useful for the design of the various controllers. Based on the equations (4.11) and (4.20), the terms $\overline{\text{SOC}}_{kt} - \overline{\text{SOC}}_{kb}$, $\overline{\text{SOC}}_k$, and $i_{cir,k}$ can be represented in z-domain as (see Appendices A.1, A.2 and A.3):

$$
\begin{aligned}
&\overline{\mathrm{SOC}}_k(z) = \frac{1}{2Q}\frac{T_s}{2}\frac{z+1}{z-1}\left[I_{cir,dc,k} - D(z)\right], \quad D(z) = \frac{1}{4}mI_m\cos\varphi; \\
&\overline{\mathrm{SOC}}_{kt}(z) - \overline{\mathrm{SOC}}_{kb}(z) = -\frac{m}{2Q}\frac{T_s}{2}\frac{z+1}{z-1}C_k(z); \qquad , \\
&I_{cir,k}(z) = \frac{1}{L}\frac{T_s}{2}\frac{z+1}{z-1}V_{L,cir,k}(z),
\end{aligned}
\tag{4.22}
$$

where T_s denotes the sampling period of the digital system. The transfer functions of the control of the MMC in the discrete-time domain are presented in Fig. 4.2, which include the leg-energy control, the arm-energy control, and the circulating current control. The closed-loop transfer functions can be represented as:

$$
\begin{aligned}
&\overline{\mathrm{SOC}}_k(z) = K_1\frac{(z+1)(z-\alpha_1)}{a_1z^2+b_1z+c_1}\overline{\mathrm{SOC}}(z) - K_2\frac{(z+1)(z-1)}{a_2z^2+b_2z+c_2}\mathrm{D}(z); \\
&\frac{\overline{\mathrm{SOC}}_{kt}(z) - \overline{\mathrm{SOC}}_{kb}(z)}{\overline{\mathrm{SOC}}^*_{kt}(z) - \overline{\mathrm{SOC}}^*_{kb}(z)} = K_3\frac{(z+1)(z-\alpha_3)}{a_3z^2+b_3z+c_3}; \\
&\frac{I_{cir,k}(z)}{I^*_{cir,k}(z)} = K_4\frac{z+1}{z+c_4},
\end{aligned}
\tag{4.23}
$$

and the relation between the control parameters in (4.23) and the control gains of Fig. 4.2 are given in Appendix A.4.

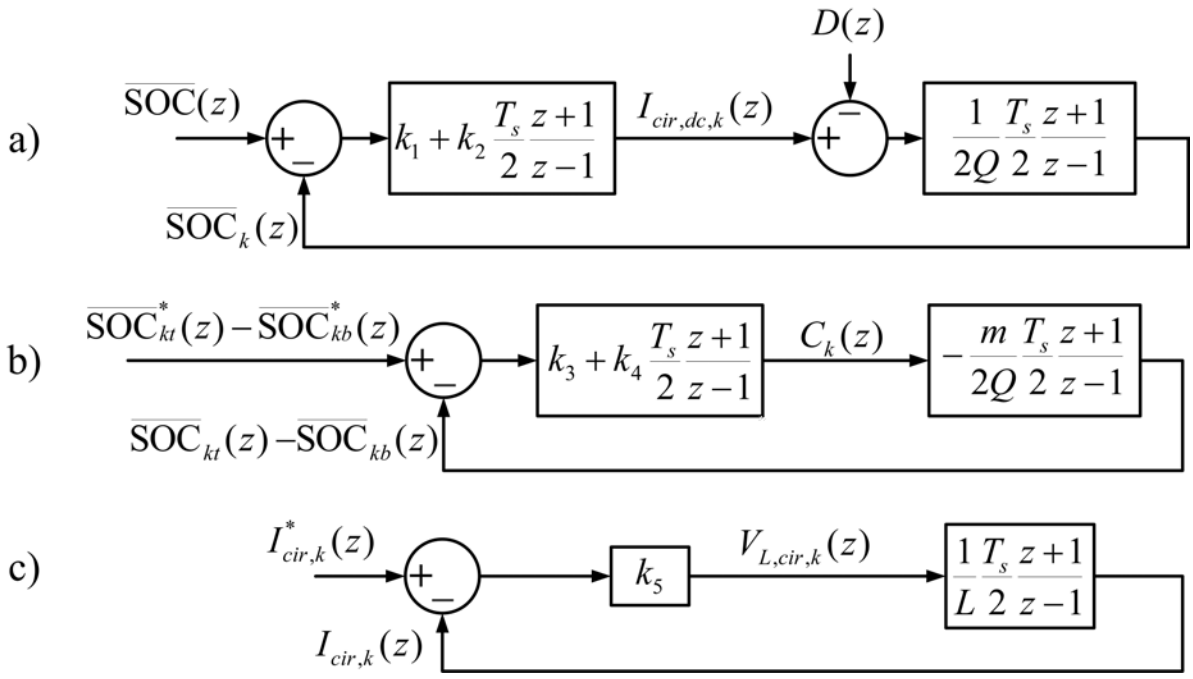


Fig. 4.2: a) Leg-energy balance control system. b) Arm-energy balance control system. c) Circulating current control system.

4.2 Static RL-load current control

If a static RL-load is connected to the MMC, the converter output voltages can be expressed as:

$$v_k = R_l i_k + L_l \frac{di_k}{dt}, \tag{4.24}$$

where R_l and L_l are the static load resistance and inductance, respectively. In this case, the voltage of the top and bottom arms can be expressed as:

$$\begin{aligned} v_{kt} &= \frac{nv_{\text{cell}}}{2} - \underbrace{[R_l i_k + (L_l + L/2)\frac{di_k}{dt}]}_{u_k} - v_{L,cir,k}; \\ v_{kb} &= \frac{nv_{\text{cell}}}{2} + \underbrace{[R_l i_k + (L_l + L/2)\frac{di_k}{dt}]}_{u_k} - v_{L,cir,k}, \end{aligned} \tag{4.25}$$

The term u_k in equation (4.25) can be used for the design of load current controller. The set of three phase voltages; u_{abc}, can be expresses in the stationary reference frame as:

$$u_{\alpha\beta} = \mathrm{C}.u_{abc}, \quad \mathrm{C} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix}, \tag{4.26}$$

where $u_{\alpha\beta} = [u_\alpha \;\; u_\beta]^T$, $u_{abc} = [u_a \;\; u_b \;\; u_c]^T$, and C is the Clarke transformation matrix. The space vector, $u_{\alpha\beta}$, can be further represented in the rotating reference frame as:

$$u_{dq} = \Gamma(\theta).u_{\alpha\beta}, \quad \Gamma(\theta) = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix}, \tag{4.27}$$

where $\theta = \omega t$, $u_{dq} = [u_d \;\; u_q]^T$, and $\Gamma(\theta)$ is the rotational matrix. By using the inverse of the rotating transformation matrix, the rotating frame voltages can be express in terms of the stationary frame quantities as:

$$u_{\alpha\beta} = \Gamma^{-1}(\theta).u_{dq}, \quad \Gamma^{-1}(\theta) = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix}, \tag{4.28}$$

where $\Gamma^{-1}(\theta)$ is the inverse of the rotational matrix.

The voltage u_k can be represented in the stationary reference frame as:

$$u_{\alpha\beta} = R_l i_{\alpha\beta} + L_{eq}\frac{di_{\alpha\beta}}{dt}; \quad L_{eq} = L_l + L/2, \tag{4.29}$$

which can be converted into the rotating reference frame by using the inverse of the rotating transformation matrix:

$$\Gamma^{-1}(\theta).u_{dq} = R_l\Gamma^{-1}(\theta).i_{dq} + L_{eq}\frac{d(\Gamma^{-1}(\theta).i_{dq})}{dt}, \tag{4.30}$$

multiplying (4.30) by $\Gamma(\theta)$, we get

$$
\begin{aligned}
u_{dq} &= R_l\, i_{dq} + L_{eq}\Gamma(\theta).\frac{d(\Gamma^{-1}(\theta).i_{dq})}{dt} \\
&= R_l\, i_{dq} + L_{eq}\left(\Gamma(\theta).\frac{d\,\Gamma^{-1}(\theta)}{dt}.i_{dq} + \Gamma(\theta).\Gamma^{-1}(\theta).\frac{di_{dq}}{dt}\right) \\
&= R_l\, i_{dq} + L_{eq}\left(\Gamma(\theta).\frac{d\,\Gamma^{-1}(\theta)}{dt}.i_{dq} + I\,\frac{di_{dq}}{dt}\right) \\
&= R_l\, i_{dq} + \omega L_{eq}\begin{bmatrix}\cos(\theta) & -\sin(\theta)\\ \sin(\theta) & \cos(\theta)\end{bmatrix}.\begin{bmatrix}-\sin(\theta) & \cos(\theta)\\ -\cos(\theta) & -\sin(\theta)\end{bmatrix}.i_{dq} + L_{eq}\,\frac{di_{dq}}{dt} \\
&= R_l\, i_{dq} + \omega L_{eq}\begin{bmatrix}0 & 1\\ -1 & 0\end{bmatrix}.i_{dq} + L_{eq}\,\frac{di_{dq}}{dt}.
\end{aligned}
\tag{4.31}
$$

As a result, the direct and quadrature components of the term u_k can be expressed by:

$$
u_d = R_l\, i_d + \omega L_{eq} i_q + L_{eq}\,\frac{di_d}{dt}; \quad u_q = R_l\, i_q - \omega\, L_{eq} i_d + L_{eq}\,\frac{di_q}{dt}. \tag{4.32}
$$

This equation can be used for the design of a current controller in the rotating reference frame, using the reference currents i^*_d and i^*_q. However, it is impossible to independently control both i_d and i_q since the static load power factor is always constant. Fig. 4.3 shows the block diagram of the static load current control where the linearized model can be described by Fig. 4.4. The current regulators of the load will produce the references for the three-phase voltages v_k^*. These references are used by the CD-THIPWM modulator to generate the pulses for the devices of the SMs.

The transfer function of closed loop system can be represented as:

$$
\frac{I_d(z)}{I_d^*(z)} = \frac{I_q(z)}{I_q^*(z)} = K_5\,\frac{(z+1)(z-\alpha_5)}{a_5 z^2 + b_5 z + c_5}, \tag{4.33}
$$

where the relation between the control parameters in (4.33) and the control gains in the block diagram are given in Appendix A.5.

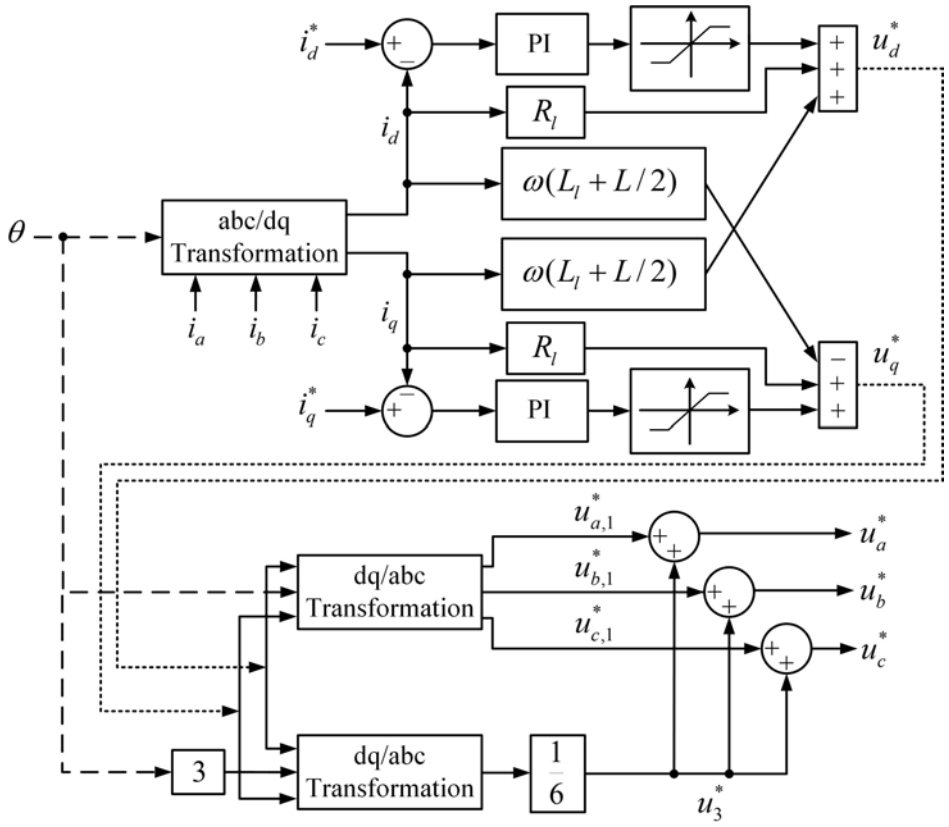


Fig. 4.3: The block diagram of RL current controller.

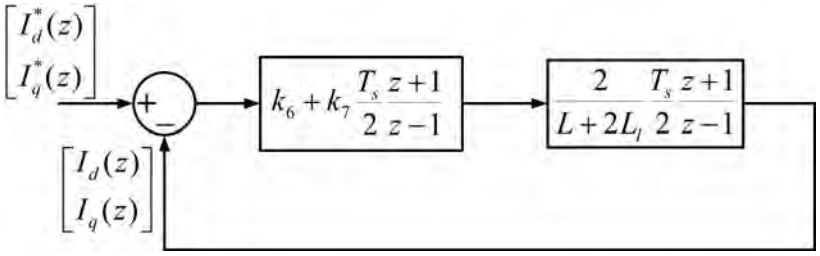


Fig. 4.4: Static load current control system.

4.3 Individual SOC balancing control

The individual SOC controller balances the cells within each arm of the converter. When the arm current is positive according to the direction of the arm current in Fig. 3.1, the cell is

charged if the SM is on and, hence, its SOC increases. When the arm current is negative and the SM is on, the cell is discharged and its SOC decreases.

In order balance the SOCs of the cells, the following algorithm is applied for each arm:

1. The arm current is measured using a current sensor.
2. The current flowing in each cell is calculated from the measured arm current and the switching function of the main switch of the half bridge converter S_m:

$$i_{h,kt} = i_{kt}\, S_m; \quad i_{h,kb} = i_{kb}\, S_m, \tag{4.34}$$

where S_m is 1 when the switch is on and 0 when it is off.

3. The SOCs of the cells are estimated every millisecond using a classical Coulomb counting method [44], [91].
4. The cells are sorted according to their SOC in descending order.
5. In case of positive arm current, the cells with the lowest SOCs are activated switching on the main switch.
6. In case of negative arm current, the cells with the highest SOCs are activated switching on the main switch.

This method produces a step-by-step balancing of the SOCs within the arm. The procedure to implement the individual SOC balancing strategy is summarised in the diagram of Fig. 4.5 [99].

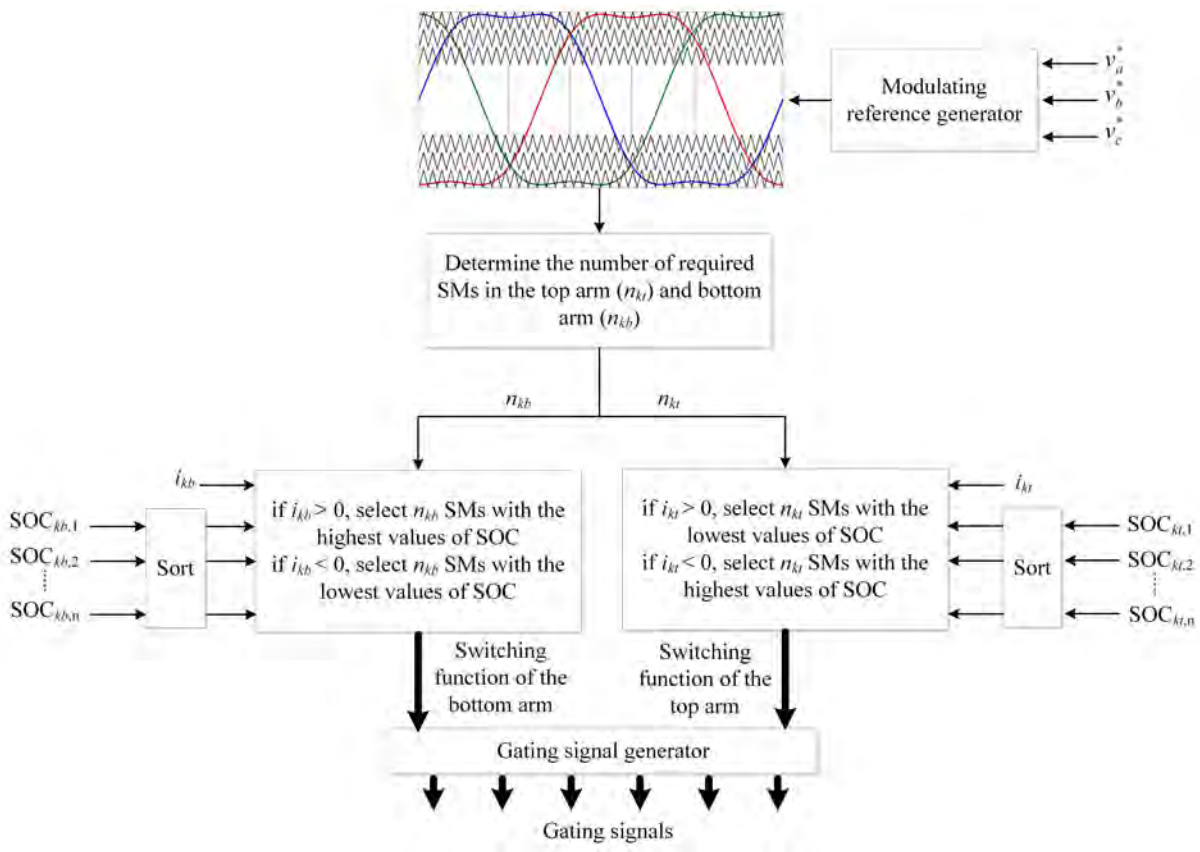


Fig. 4.5: The block diagram of the individual SOC balancing controller.

In practice, the Coulomb counting method can be affected by the coulombic efficiency of the recharge process, the internal temperature of the cell, the self-discharge due to the cell leakage current, aging, etc. In this case, the estimation of the SOC based only on the current integration method can lead to incorrect results. The proposed controller takes into account these phenomena modifying equation (3.14) as follows [77]:

1) the initial SOC values are updated by measuring the open circuit voltage (OCV) of the cell when the electric vehicle is not in use or the correspond SM is not active (; the relation between the OCV and SOC can be preliminary estimated according to in [92].
2) the energy loss occurring during charging needs to be compensated taking into account the coulombic efficiency, which is typically between 0.98-1. A more accurate description on

how to estimate the coulombic efficiency is discussed in [93], [94].

3) the maximum available capacity needs to be changed as a function of cell's temperature in order to consider the effect of capacity losses due to changes of the thermodynamic and kinetic aspects of the electrochemical processes [94]. A more accurate description on how to estimate capacity loss is also discussed in [93], [94].

The individual controller is flexible and can be improved by adding a thermal management system (TMS), which is essential when the converter has to be fitted in a real battery EV. The TMS can cool/heat battery cells timely and selectively on the basis of the temperature of battery cells and achieve more efficient and reliable operations for the proposed MMC.

The source of heat from each battery cell is due to the power dissipated by the cell's internal resistance, Q_d. Some part of generated heat is absorbed into the cell materials and the remaining heat is released on the surface of the cell. The equation for the calculation of Q_d is given by [95]:

$$Q_d = R_{\text{int}} I_c^2 = C_c \frac{dT_c}{dt} + Ah(T_c - T_{amb}), \tag{4.35}$$

where R_{int} is the cell's internal resistance, I_c is the cell current, C_c is the heat capacity, T_c is the cell temperature, A is the cell surface area, h is the heat transfer coefficient, and T_{amb} is the ambient temperature which is affected by the temperature of thermal fins, T_f. Solving (4.35) for T_c gives:

$$T_c(t + \Delta t) = T_c(t) + \Delta t \left[\frac{R_{\text{int}}}{C_c} I_c^2 - \frac{Ah}{C_c}(T_c(t) - T_{amb}) \right]. \tag{4.36}$$

During the operation cycle of the cell from the unity SOC to zero SOC, a rise of cell temperature increases the mobility of cell charges and chemical reactions in the cell, and therefore temporarily reduces the internal resistance of the cell and increases its capacity. The

relation between the internal resistance and the cell temperature during the operation cycle of the cell is given by [95]:

$$R_{\text{int}} = a_0 + a_1 T_c + a_2 T_c^2 + a_3 T_c^3. \tag{4.37}$$

The proposed MMC should guarantee delivery of the required power within the cell voltage range. However, a decrease in the cell temperature increases the cell internal resistance and it may cause a higher voltage drop for the same current. In this case, the converter output voltage drops below the applicable voltage and making the MMC unable to provide the required power to the traction motor. On the other hand, a further increase in the temperature potentially results in thermal runaway and may cause an explosion of the battery cells, because of material decomposition. Therefore, the thermal stability of battery cells should be maintained. To protect the battery cells from the thermal runaway and the malfunction at low temperature, the cell temperature should be kept within its minimum and maximum limits (e.g. $T_{min}<T_c<T_{max}$) [95].

Fig. 4.6 shows the flowchart of the proposed TMS. The BMS estimates continuously the cell SOC by measuring the cell voltage and current. Using the measurement of V_c and I_c, the equivalent R_{int} can be calculated as:

$$R_{\text{int}} = \frac{V_{oc} - V_c}{I_c}, \tag{4.38}$$

where V_{oc} is the open circuit voltage and the relation between V_{oc} and SOC can be made by using the curve given in [93]. Using equation (4.37), we can calculate the desirable cell temperatures. The cells whose temperature is higher than the upper limit need to be cooled in order to maintain thermal stability. On the other hand, equation (4.36) gives the desirable ambient temperatures for cells whose temperature is lower than the upper limit. Based on the temperature distribution, we can obtain thermal fins' temperatures that achieve the target

ambient temperature and then determine whether each cell needs to be heated or cooled. In order to do that, cooling and heating channels are connected to the radiator/heater; these channels are connected to thermal fins for each cell through coolant flow valves.

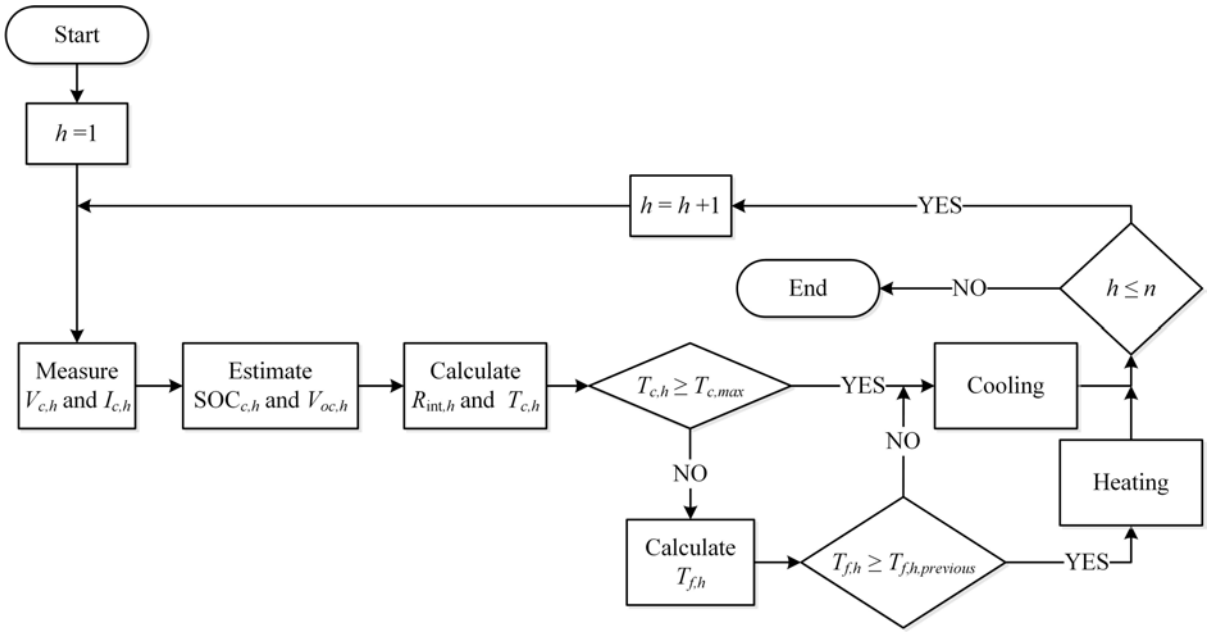


Fig. 4.6: Flowchart of the proposed TMS.

4.4 Induction motor vector control

For an induction motor, the stator voltage and the rotor flux linkage equations can be expressed in the rotating reference frame synchronous with the rotor flux Φ_r as [96]:

$$\begin{aligned} v_{qs} &= R_s i_{qs} + \sigma L_s \frac{di_{qs}}{dt} + \sigma L_s p\omega_r i_{ds} + \frac{L_m}{L'_r} p\omega_r \Phi_{dr}; \\ v_{ds} &= R_s i_{ds} + \sigma L_s \frac{di_{ds}}{dt} - \sigma L_s p\omega_r i_{qs} + \frac{L_m}{L'_r} \frac{d\Phi_{dr}}{dt}; \end{aligned} \tag{4.39}$$

$$\Phi_{qr} = 0 = L'_r \, i'_{qr} + L_m \, i_{qs}; \qquad \Phi_{dr} = \Phi_r = L'_r \, i'_{dr} + L_m \, i_{ds}, \tag{4.40}$$

where v_{qs}, v_{ds}, i_{qs}, i_{ds} are the q-axis and d-axis components of the stator voltage and current, respectively; Φ_{qr}, Φ_{dr} are the q-axis and d-axis components of the rotor flux, R_s and L_s are resistance and total self-inductance of the stator winding, L'_r is the total self-inductance of the

rotor winding referred to a stator phase winding, L_m is the mutual inductance, $\sigma = 1 - L_m^2 / (L_r L_s)$ is the total leakage factor, p is the number of machine pole pairs, and ω_r is the mechanical speed.

The equation of the rotor flux, torque and slip frequency are [96]:

$$\frac{L'_r}{R'_r}\frac{d\Phi_r}{dt} + \Phi_r = L_m\, i_{ds}, \tag{4.41}$$

$$T_{el} = \frac{p\, L_m \Phi_r}{L'_r} i_{qs}, \tag{4.42}$$

$$\omega_\sigma = \frac{R'_r\, L_m}{L'_r\, \Phi_r} i_{qs}, \tag{4.43}$$

where R'_r is the resistance of rotor windings referred to a stator phase winding,

For the indirect vector control, the rotor flux angle, ψ, is calculated by integrating the sum of rotor speed and the calculated slip frequency. The flux is constant up to the base speed and then above the nominal speed, the flux decreases with an inverse law of motor speed.

Fig. 4.7 shows the block diagram of the indirect vector control where the difference between the speed reference, ω_r^*, and the speed feedback, ω_r, produces the speed error for the PI speed regulator, which produces the torque reference T_{el}^*. The flux is kept constant at the rated value, unless field-weakening is necessary to achieve speeds above the rated. The reference rotor flux Φ_r^* and the estimated flux provide the flux error for the PI flux regulator, which produces the reference value of i_{ds}^* based on (4.41). Therefore, i_{qs}^* can be calculated from the torque reference and the flux reference using (4.42). From (4.43), the required slip reference, ω_σ^*, can be finally calculated.

The current regulators of the motor produce the voltage references for the three-phase voltages v_k^*. These references are used by the CD-THIPWM modulator to generate the pulses

for the devices of the SMs [97]. Equation (4.39) can be used for the design of the motor current controller in the rotating reference frame using the reference currents i_{dq}^{*}.

The linearized model of the motor speed, flux, and current controllers can be described according to Fig. 4.8 (a), (b), and (c), respectively, and the transfer functions are given by:

$$\begin{aligned}
\Omega_r(z) &= K_6 \frac{(z+1)(z-\alpha_1)}{a_6 z^2 + b_6 z + c_6} \Omega_r^*(z) - K_7 \frac{(z+1)(z-1)}{a_7 z^2 + b_7 z + c_7} T_L(z) \\
\frac{\Phi_r(z)}{\Phi_r^*(z)} &= K_8 \frac{(z+1)(z-\alpha_8)}{a_8 z^2 + b_8 z + c_8} \\
\frac{I_{ds}(z)}{I_{ds}^*(z)} &= \frac{I_{qs}(z)}{I_{qs}^*(z)} = K_9 \frac{(z+1)(z-\alpha_9)}{a_9 z^2 + b_9 z + c_9}
\end{aligned} \quad , \qquad (4.44)$$

where the relation between the control parameters in (4.44) and the control gains in the block diagram are given in Appendix A.6.

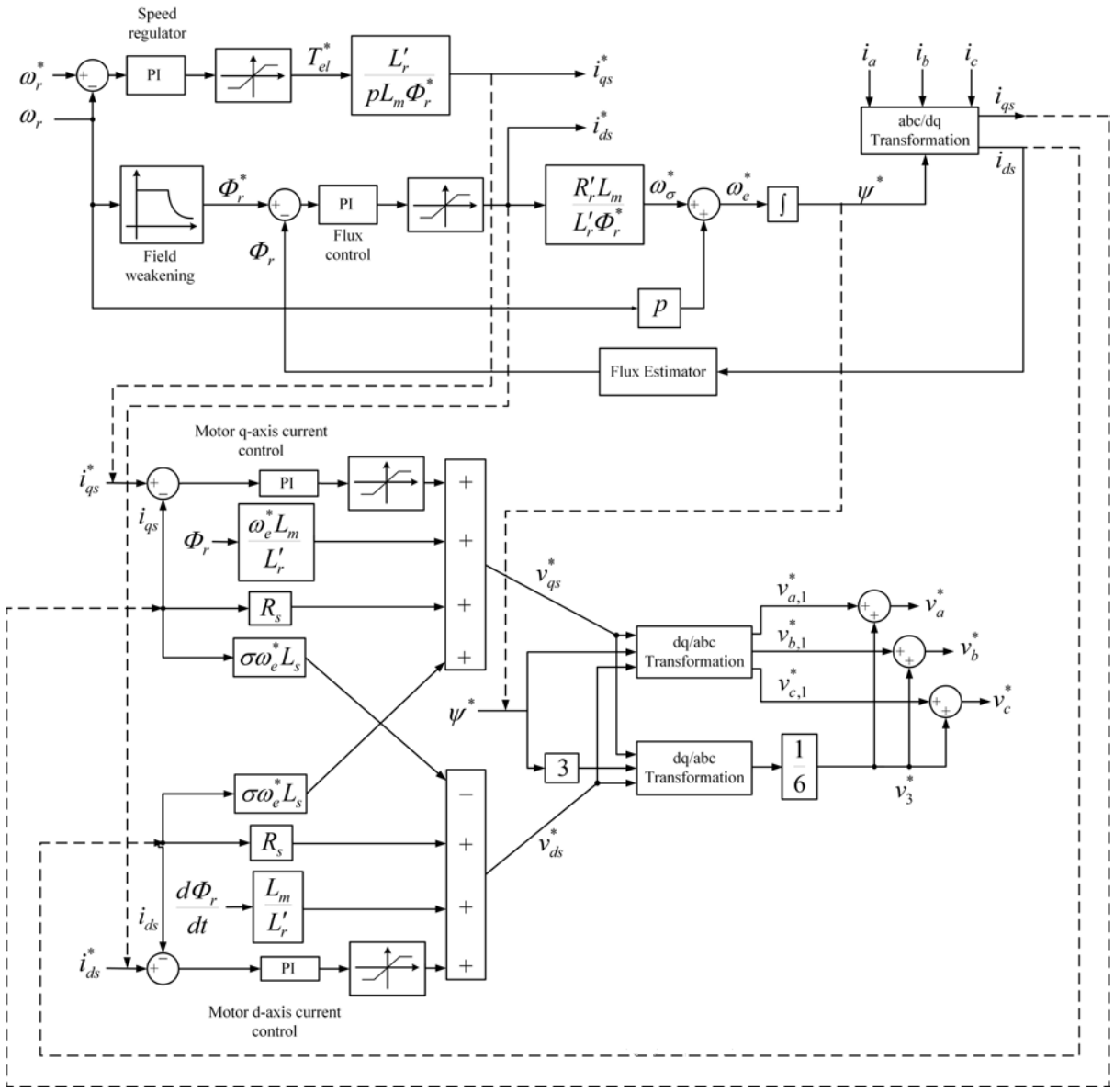


Fig. 4.7: The block diagram of indirect vector control.

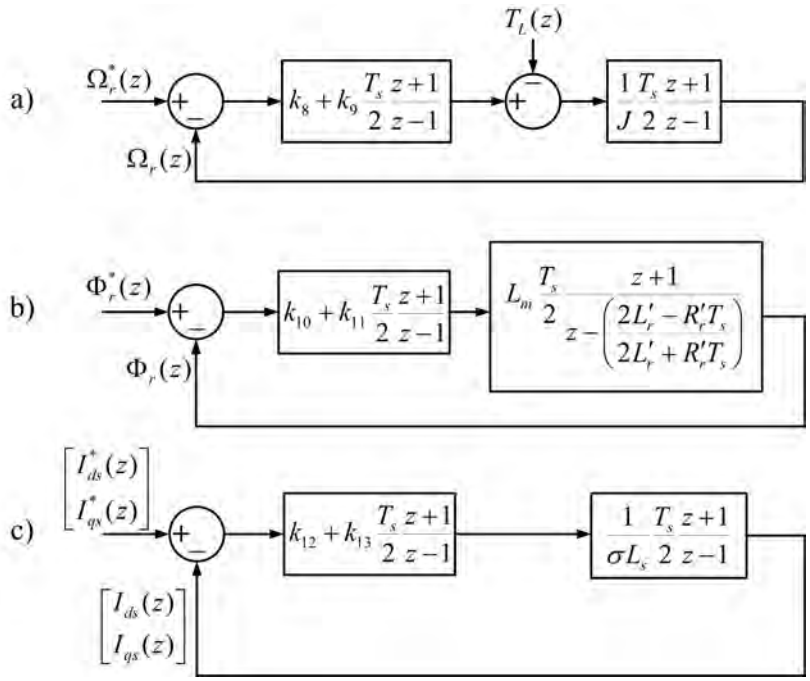


Fig. 4.8: a) Motor speed control system. b) Motor flux control system. c) Motor current control system.

4.5 Battery charging with the proposed MMC

This section provides the analyses of control for the stationary recharging of the battery cells. The proposed converter can be used to charge the batteries from three phase and a single phase ac sources and from dc sources. The recharge from dc sources and single-phase ac sources are not considered in this thesis.

In order to recharge the battery cells with the maximum efficiency, the current drawn from the external three-phase source must have a (nearly) unity input power factor. The connection to the grid requires a phase-locked loop (PLL) and a proper current controller. The control algorithm of grid current control system is shown in Fig. 4.9 [98].

4.5.1 PLL

The grid voltage is measured by voltage sensors and the phase-locked loop algorithm yields

the phase angle $\hat{\theta}$ and the direct component of the grid voltage The three-phase voltages of the grid can be expressed as [98]:

$$v_{abc} = [v_a \quad v_b \quad v_c]^T = V_m[\cos(\theta) \quad \cos(\theta - 2\pi/3) \quad \cos(\theta + 2\pi/3)]^T; \quad \theta = \int \omega \, dt, \tag{4.45}$$

where ω is the actual grid frequency. Under the assumption of balanced grid voltages, the three-phase voltages can be expressed in the rotating reference frame as [98]:

$$v_{dq} = [v_d \quad v_q]^T = \Gamma(\hat{\theta}).\mathrm{C}.v_{abc}, \tag{4.46}$$

where v_d and v_q are the direct and quadrature components of the grid phase voltages, respectively. By substituting the phase voltages in (4.45) into (4.46), the direct and quadrature components of the grid phase voltages are expressed as [98]:

$$v_d = \sqrt{\frac{3}{2}} V_m \sin(\theta_e); \qquad v_q = \sqrt{\frac{3}{2}} V_m \cos(\theta_e); \qquad \theta_e = \hat{\theta} - \theta. \tag{4.47}$$

If it is assumed that the phase difference θ_e is very small, (4.47) can be linearized as [98]:

$$v_d \approx \sqrt{\frac{3}{2}} V_m \theta_e; \qquad v_q \approx \sqrt{\frac{3}{2}} V_m. \tag{4.48}$$

Hence, the direct component can be used to track the grid frequency and phase angle, by a proper design of the PI controller. The linearized model of the three phase PLL system can be described by Fig. 4.10 (a) and the transfer function of the PLL closed loop system can be represented as:

$$\frac{\hat{\Theta}(z)}{\Theta(z)} = K_{10} \frac{(z+1)(z-\alpha_{10})}{a_{10}z^2 + b_{10}z + c_{10}}, \tag{4.49}$$

where the relation between the control parameters in (4.49) and the control gains in the block diagram are given in Appendix A.7.

4.5.2 Grid current control

The term $v_{L,k}$ in equation (3.4) can be used for the design of the grid current controller in the rotating reference frame, using the reference currents i^*_d and i^*_q. The voltage $v_{L,k}$ can be represented in the stationary reference frame as:

$$v_{L,\alpha\beta} = \frac{L}{2}\frac{di_{\alpha\beta}}{dt}, \tag{4.50}$$

which can be converted into the rotating reference frame by using the inverse of rotating transformation matrix:

$$\Gamma^{-1}(\theta).v_{L,dq} = \frac{L}{2}\frac{d(\Gamma^{-1}(\theta).i_{dq})}{dt}, \tag{4.51}$$

multiplying (4.51) by $\Gamma(\theta)$, we get:

$$\begin{aligned} v_{L,dq} &= \frac{L}{2}\Gamma(\theta).\frac{d(\Gamma^{-1}(\theta).i_{dq})}{dt} \\ &= \frac{L}{2}\left(\Gamma(\theta).\frac{d\,\Gamma^{-1}(\theta)}{dt}.i_{dq} + \Gamma(\theta).\Gamma^{-1}(\theta).\frac{di_{dq}}{dt}\right) \\ &= \frac{L}{2}\left(\Gamma(\theta).\frac{d\,\Gamma^{-1}(\theta)}{dt}.i_{dq} + I\frac{di_{dq}}{dt}\right) \\ &= \frac{\omega L}{2}\begin{bmatrix}\cos(\theta) & -\sin(\theta)\\ \sin(\theta) & \cos(\theta)\end{bmatrix}.\begin{bmatrix}-\sin(\theta) & \cos(\theta)\\ -\cos(\theta) & -\sin(\theta)\end{bmatrix}.i_{dq} + \frac{L}{2}\frac{di_{dq}}{dt} \\ &= \frac{\omega L}{2}\begin{bmatrix}0 & 1\\ -1 & 0\end{bmatrix}.i_{dq} + \frac{L}{2}\frac{di_{dq}}{dt}. \end{aligned} \tag{4.52}$$

As a result, the direct and quadrature components of the term $v_{L,k}$ can be expressed by:

$$v_{L,d} = \frac{\omega L}{2}i_q + \frac{L}{2}\frac{di_d}{dt}; \quad v_{L,q} = -\frac{\omega L}{2}i_d + \frac{L}{2}\frac{di_q}{dt}. \tag{4.53}$$

The instantaneous real power, p, and the instantaneous imaginary power, q, are given as [110]:

$$p = v_d i_d + v_q i_q = v_d i_d; \quad q = v_d i_q - v_q i_d = v_d i_q. \tag{4.54}$$

The d-axis current reference, i_d^*, and the q-axis current reference, i_q^*, are determined by a standard instantaneous power controller based on the real and imaginary powers as given in equation (4.54) and a block to decouple the direct and quadrature feedback loops. The active power reference is set according to the capability of the grid, whereas the imaginary power is set to zero ($q^* = 0$) in order to obtain a (nearly) unity input power factor [79]:

$$i_d^* = \frac{p^*}{v_d}; \quad i_q^* = \frac{q^*}{v_d} = 0. \tag{4.55}$$

The linearised model of the grid current controller can be described by Fig. 4.10 (b). The transfer function of closed loop system can be represented as:

$$\frac{I_d(z)}{I_d^*(z)} = \frac{I_q(z)}{I_q^*(z)} = K_{11} \frac{(z+1)(z-\alpha_{11})}{a_{11}z^2 + b_{11}z + c_{11}}, \tag{4.56}$$

where the relation between the control parameters in (4.56) and the control gains in the block diagram are given in Appendix A.7.

Fig. 4.11 shows the cell voltage, current and power over the time of recharging process. Starting from an initial low SOC, the recharge algorithm ensures a recharge of the cells with a constant current, up to a SOC near to unity. When the cell reaches the maximum level of the voltage given by the manufacturer, the current controller switches to a voltage controller that hold up the maximum voltage of each cell until the recharge is completed. This has been in practice implemented by a proper selection of the reference currents in the described controller given by (4.57), which is derived by equalising the power of battery cells and the active power drawn from the grid. For the constant current recharge phase, the reference for the direct current

comes from a current regulator that charges the cells at constant current. For the constant voltage phase, the reference direct current comes from a voltage regulator that keeps voltage of the cells at the maximum permissible value [79]. This can be written as:

$$i_d^* = \frac{1}{v_d}\sum_{j=1}^{6n} v_{cj} i_{cj}; \quad \begin{cases} v_{cj} i_{cj} = V_{c,\max} i_{cj}; & v_{cj} \geq V_{c,\max} \\ v_{cj} i_{cj} = v_{cj} I_{ch}; & v_{cj} < V_{c,\max} \end{cases} \tag{4.57}$$

where v_{cj} and i_{cj} are the measured voltage and current of the *j-the* cell, respectively, $V_{c,\max}$ is the maximum cell voltage (4.2 V), I_{ch} is the nominal cell charge current, which can be calculated in terms of maximum rechargeable power, $P_{\max}$, in the hypothesis of no loss as:

$$I_{ch} = \frac{P_{\max}}{6nV_{c,\max}}. \tag{4.58}$$

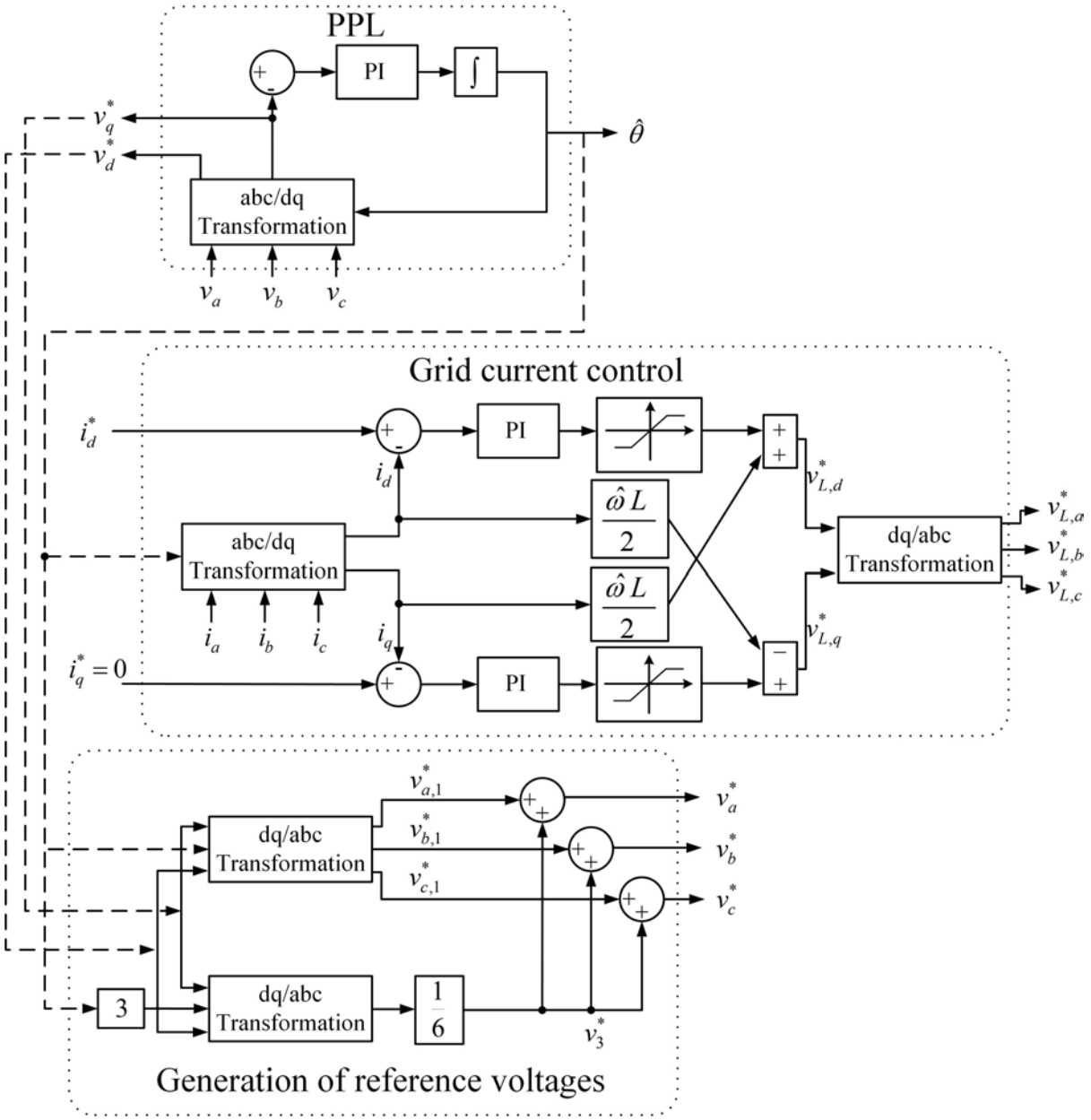


Fig. 4.9: Block diagram of PLL and the grid current control.

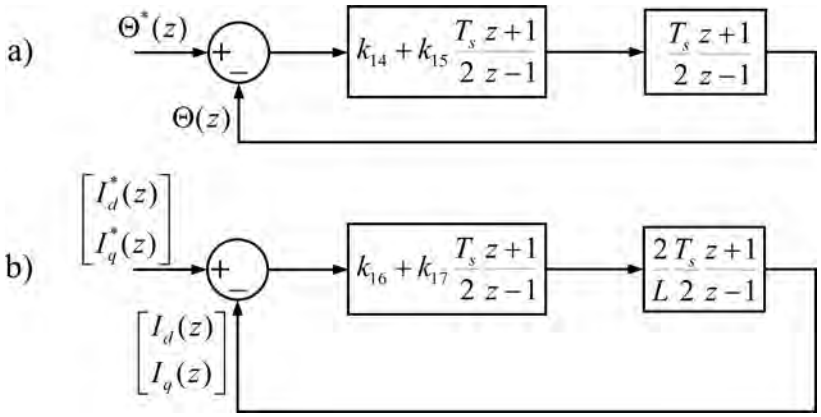


Fig. 4.10: a) PPL control system. b) Grid current control system.

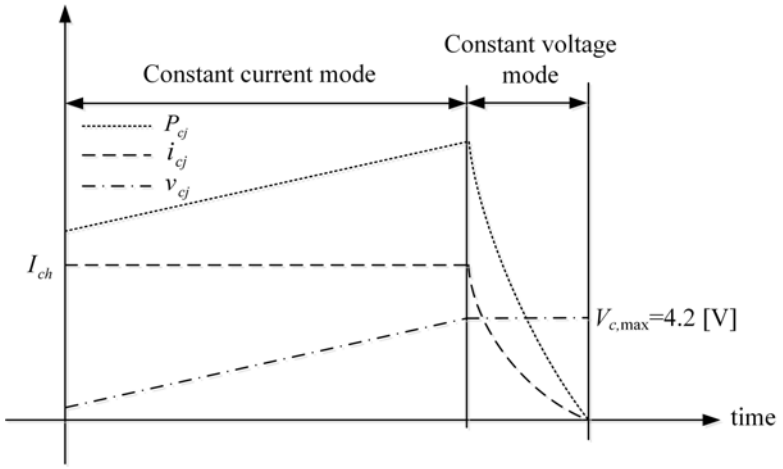


Fig. 4.11: Cell voltage, current and power curves during the recharge process.

In summary, the chapter presents control strategy of the proposed converter integrating the SOC balancing control scheme, the circulating current control scheme, the traction motor vector control, and grid ac current control scheme. This chapter has analysed further this converter configuration with reference to the stationary recharge from the AC grid. The recharge of the cells is based on a double stage process: the constant current stage recharges the electrochemical cells up to their maximum voltage; the constant voltage stage recharges the cells up to their unity state of charge. The analysis of the phase-locked loop control system is also presented for the phase tracking system of the three phase utility interface MMC.

Chapter 5

Assessment of Converter Losses

The main cause of concern of MMCs for low voltage applications is the increased conduction losses due to the high number of devices conducting in series. On the other hand, MMC can benefit from the flexibility of using low voltage devices like MosFETs that have an equivalent resistance lower than IGBTs and low switching losses. Therefore, a detailed analysis of power losses of MMC for the different operating regions of battery EVs is necessary to assess the suitability of this converter for traction drives.

The power losses of the converter are divided into conduction losses and switching losses and, for simplicity, other losses like gate drivers, magnetics and auxiliaries are not considered in this thesis.

5.1 Conduction losses

The instantaneous conduction losses of a single power MosFET can be calculated approximating the device with its the drain-source on-state resistance $R_{ds,on}$ [100]:

$$p_{c,M} = v_{ds} i_d = R_{ds,on} i_d^2, \tag{5.1}$$

where v_{ds} and i_d are the drain-source voltage and the drain current of the MosFET, respectively.

Each SM of the converter includes two power MosFETs but, at each instant of time except during dead-times, the current flows through only one of them independently of the conduction state and the direction of the current itself. Thus, the number of MosFETs conducting across

each arm is equal to n. The instantaneous value of the conduction losses of the converter top and bottom arms, $p_{c,kt}$ and $p_{c,kb}$, can be expressed as [101]:

$$p_{c,kt} = nR_{ds,on}i_{kt}^2 = n\,R_{ds,on}\left(i_{cir,k} + \frac{1}{2}i_k\right)^2; \quad p_{c,kb} = nR_{ds,on}i_{kb}^2 = n\,R_{ds,on}\left(i_{cir,k} - \frac{1}{2}i_k\right)^2. \tag{5.2}$$

Thus the instantaneous value of conduction losses of each phase leg, $p_{c,k}$, results in [101]:

$$p_{c,k} = p_{c,kt} + p_{c,kb} = 2\,nR_{ds,on}\left(i_{cir,k}^2 + \frac{1}{4}i_k^2\right). \tag{5.3}$$

Since the circulating current is normally few percent of the nominal current and is present only during cell balancing, its contribution to the conduction losses is negligible. Therefore, (5.3) can be approximated by [101]:

$$p_{c,k} = \frac{1}{2}nR_{ds,on}i_k^2. \tag{5.4}$$

Assuming the load current has only the fundamental component I_m, the average phase losses $P_{c,k}$ can be calculated as [101]:

$$P_{c,k} = \frac{1}{T}\int_0^T p_{c,k}dt = \frac{1}{4}n\,I_m^2R_{ds,on}. \tag{5.5}$$

Therefore, the total MMC conduction losses are independent from the modulation index and the load power factor and are given by [101]:

$$P_c = 3P_{c,k} = \frac{3}{4}nI_m^2R_{ds,on}. \tag{5.6}$$

5.2 Switching losses

For the calculation of the switching losses, a linear approximation of the MosFET switching process has been assumed. Thus, the turn-on and turn-off switching energy losses for a single MosFET, $E_{sw,on}$ and $E_{sw,off}$, are given by [100]:

$$E_{sw,on} = \frac{1}{2} v_{\text{cell}} i_d (t_{ri} + t_{fv}) = \frac{1}{2} v_{\text{cell}} i_d t_{on}; \quad E_{sw,off} = \frac{1}{2} v_{\text{cell}} i_d (t_{fi} + t_{rv}) = \frac{1}{2} v_{\text{cell}} i_d t_{off}, \quad (5.7)$$

where t_{ri} and t_{fi} are the current rise and fall times, t_{rv} and t_{fv} are the voltage rise and fall times. In (5.7), v_{cell} and i_d are considered at the initial instant of switching. Each change of the conduction state of a cell corresponds to the turn-on of one MosFET and the simultaneous turn-off of the other MosFET of the same SM. Thus, at each change of the conduction state of the SM, the energy dissipated is equal to [101]:

$$E_{sw} = E_{sw,on} + E_{sw,off} = \frac{1}{2} v_{cell} i_d (t_{on} + t_{off}). \quad (5.8)$$

If for simplicity the switching events are supposed to be regularly spaced, each arm is switching at T_{sw}, $2T_{sw}$, $3T_{sw}$ … zT_{sw}, where z is the total number of arm switching events in a fundamental period, T, which is given by [101]:

$$z = \frac{T}{T_{sw}} = \frac{f_{sw}}{f}. \quad (5.9)$$

If z_h denotes the number of switching events of a SM in the fundamental period T, the number z is split across the SMs of the arm, i.e. $z = z_1 + z_2 + \ldots + z_n$. Fig. 5.1 shows an example of waveforms for the currents flowing into the SMs of a converter arm in the case of 4 SMs/arm.

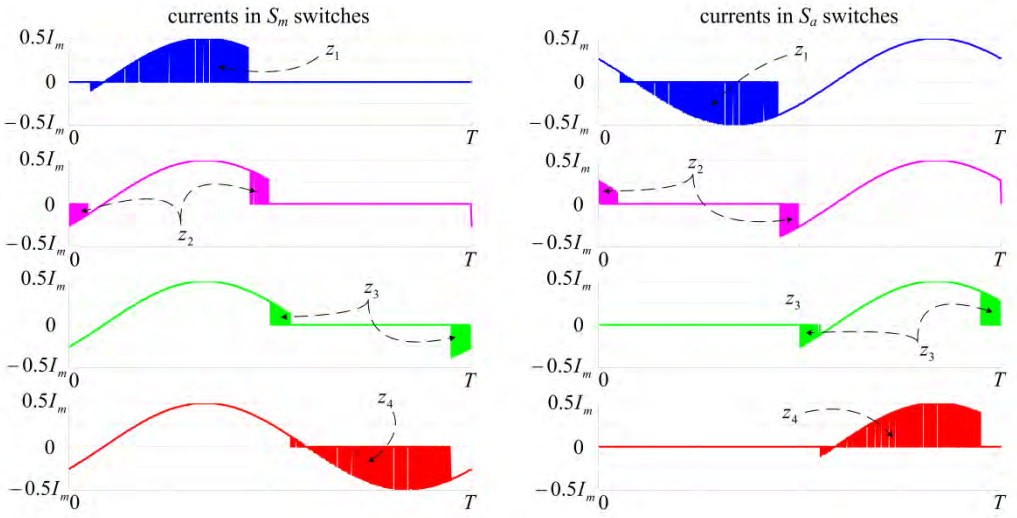


Fig. 5.1: Currents flowing into all switches within one arm ($n = 4$).

Supposing that the h-th SM is switching at $z_{h1}T_{sw}$, $z_{h2}T_{sw}$, $z_{h3}T_{sw}$ …, $z_{hzh}T_{sw}$, where z_{h1}, z_{h2}, z_{h3} …, z_{hzh} are unequal integer numbers, the others $n - 1$ SMs will remain in a constant switching state as long as THI-SPWM scheme is used. In this case, the h-th SM currents at instant of switching are [101]:

$$\left\{\frac{1}{2}I_m\left|\sin(z_{h1}\omega T_{sw})\right|,\quad \frac{1}{2}I_m\left|\sin(z_{h2}\omega T_{sw})\right|,\quad \frac{1}{2}I_m\left|\sin(z_{h3}\omega T_{sw})\right|,\quad \cdots\quad \frac{1}{2}I_m\left|\sin(z_{hz_h}\omega T_{sw})\right|\right\} \tag{5.10}$$

As a result, the switching energy $E_{sw,h}$ dissipated by a SM during a fundamental period can be expressed as [101]:

$$E_{sw,h} = E_{sw}^*\sum_{j=1}^{z_h}\left|\sin(z_{hj}\omega T_{sw})\right|;\qquad E_{sw}^* = \frac{1}{2}v_{\text{cell}}I_m(t_{on}+t_{off}), \tag{5.11}$$

and the switching energy $E_{sw,arm}$ dissipated by one arm during a fundamental period can be expressed as [101]:

$$\begin{aligned} E_{sw,arm} &= E_{sw}^*\left(\sum_{j=1}^{z_1}\left|\sin(z_{1j}\omega T_{sw})\right| + \sum_{j=1}^{z_2}\left|\sin(z_{2j}\omega T_{sw})\right| + \cdots + \sum_{j=1}^{z_n}\left|\sin(z_{nj}\omega T_{sw})\right|\right) \\ &= E_{sw}^*\sum_{i=1}^{z}\left|\sin(i\omega T_{sw})\right| = E_{sw}^*\sum_{i=1}^{z}\left|\sin(2\pi i/z)\right|, \end{aligned} \tag{5.12}$$

which can be further represented by the following closed form expression (see Appendix B.3) [101]:

$$E_{sw,arm} = E_{sw}^{*} \cot\left(\frac{\pi}{2z}\right) \approx E_{sw}^{*}\left(\frac{2z}{\pi} - \frac{\pi}{6z}\right). \tag{5.13}$$

Finally, the power dissipated by the converter due to switching losses can be calculated as [101]:

$$P_{sw} = 6fE_{sw,arm} \approx E_{sw}^{*}\left(\frac{12f_{sw}}{\pi} - \frac{\pi f^2}{f_{sw}}\right). \tag{5.14}$$

The total MMC losses P_l, are the sum of the conduction and switching losses [101]:

$$P_l = P_c + P_{sw} \approx v_{\text{cell}} I_m \left(\frac{6f_{sw}}{\pi} - \frac{\pi f^2}{2f_{sw}}\right)(t_{on} + t_{off}) + \frac{3}{4} n I_m^2 R_{ds,on}. \tag{5.15}$$

5.3 Comparison with a 2-level inverter

In order to assess the suitability of MMCs for traction drives, the MMC efficiency has been compared with a traditional two-level IGBT inverter. In order to penalise the MMC, the losses due to the cell balancing are not considered for the two-level inverter and are instead included in the MMC. As a further penalisation, the efficiency of the motor is considered equal for both the two-level inverter and the MMC [101]. Both converters are driven by THI-SPWM strategy and connected to a 220 V, 250 A, 50 Hz, 80 kW machine [101]. Equal semiconductor ratings have been applied for both converter types using FZ300R12KE3G IGBTs [103] for the two-level inverter and AUIRFS8409-7P power MosFETs [104] for the MMC. According to the technical literature, the conduction and switching losses of an IGBT-based two-level inverter are given by [102]:

$$P_{c,2-\text{level}} = \frac{3}{\pi} I_m (V_{ce,0} + V_{f,0}) + \frac{3}{4} I_m^2 (R_c + R_d) + \frac{3}{4} (V_{ce,0} - V_{f,0}) I_m m \cos(\varphi) + \frac{2}{\pi} (R_c - R_d) I_m^2 m \cos(\varphi); \quad (5.16)$$

$$P_{sw,2-\text{level}} = \frac{6}{T} \sum_{l=1}^{p} E_{IGBT,on}(i_i) + E_{IGBT,off}(i_i) + E_{IGBT,rec}(i_i); \qquad i_i = \left| I_m \sin(2\pi i / z) \right|,$$

The definition of the symbols and their corresponding values for the numerical simulations are reported in Table 5.1. $E_{IGBT,on}$ and $E_{IGBT,off}$ are given in the data sheet and can be described as a polynomial function of current i_l. Furthermore, Table 5.1 summarizes the main data of the two-level inverter and MMC parameters used for simulation. Fig. 5.2 shows the 'gear changing' used for the comparative case. The two converters are operated at a maximum switching frequency of 2 kHz and 20 kHz.

Table 5.1: Main data of the simulated converters [101].

	Variable	Description	Values
2-level inverter	$V_{ce,0}$	IGBT on-state zero-current collector-emitter voltage	0.921057 [V]
	$V_{ce,}$	IGBT maximum collector-emitter voltage	1200 [V]
	R_c	IGBT collector-emitter on-state resistance	3.59 [mΩ]
	$E_{IGBT,on}$	IGBT turn-on energy	$5.3\times10^{-3} + 2.9\times10^{-5}\, i_l + 1.2\times10^{-7}\, i_l^2$ [J]
	$E_{IGBT,off}$	IGBT turn-off energy	$2.4\times10^{-3} + 1.4\times10^{-4}\, i_l$ [J]
	$V_{f,0}$	Diode on-state zero-current forward voltage	1.03562 [V]
	R_d	Diode forward on-state resistance	2.09 [mΩ]
	$E_{Diode,rec}$	Diode recovery energy	$6.8\times10^{-3} + 9.1\times10^{-5}\, i_l - 9.1\times10^{-8}\, i_l^2$ [J]
MMC	n	Number of SMs/arm	84
	v_{cell}	Cell voltage	3.2-4.2 [V]
	L	Arm inductor	50 [μH]
	V_{ds}	MosFET drain-source maximum voltage	40 [V]
	$R_{ds,on}$	MosFET drain-source on-state resistance	0.55 [mΩ]
	t_{ri}	MosFET current rise time	43 [ns]
	t_{fi}	MosFET current fall time	72 [ns]
	t_{rv}	MosFET voltage rise time	0.85 [ns]
	t_{fv}	MosFET voltage fall time	6.24 [ns]

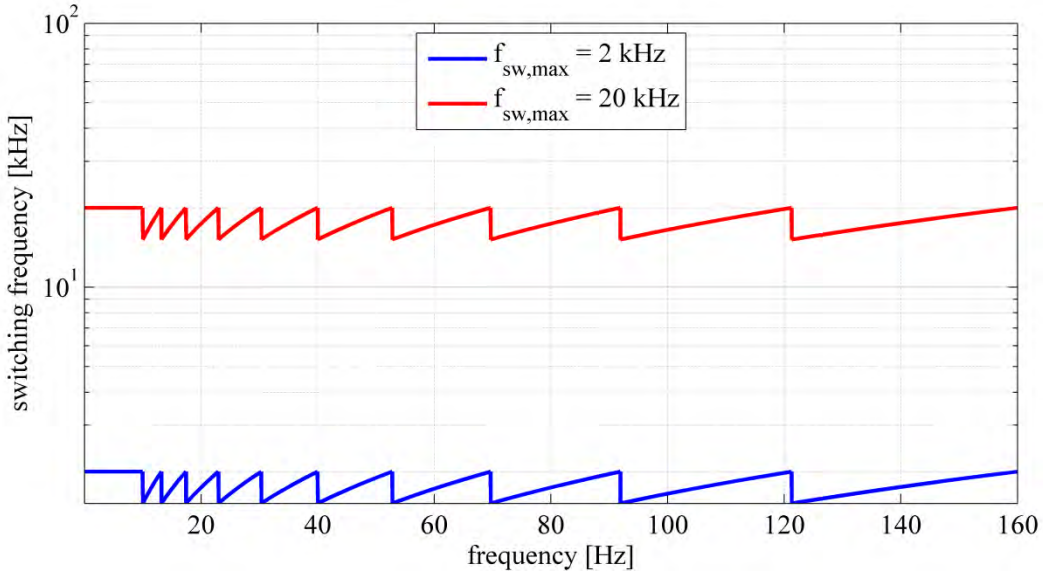


Fig. 5.2: Illustration of 'gear changing' used for the comparison.

Fig. 5.3 shows the efficiency for both topologies versus fundamental frequency when the motor is drawing half of the nominal current. It is evident that for the MMC the efficiency does not change in an appreciable way with the maximum switching frequency. At maximum switching frequency of 20 kHz, the MMC efficiency is higher than the inverter efficiency by 3-5% in the constant torque region, and by 0.5-1% in the constant power region. At maximum switching frequency of 2 kHz, the MMC efficiency is lower than the inverter efficiency by 1-4% in the constant torque region, and by 1% in the constant power region [101].

Fig. 5.4 shows the efficiency for both topologies versus frequency when the motor is drawing the nominal current with the same maximum switching frequencies of the previous example. At maximum switching frequency of 20 kHz, the MMC efficiency is lower than the inverter efficiency by 1-4% in the constant torque region, and by 1-2% in the constant power region. At maximum switching frequency of 2 kHz, the MMC efficiency is lower than the inverter efficiency by 3-12% in the constant torque region, and by 3% in the constant power region. It can be also noticed that the efficiency of the MMC increases when the load current decreases;

conversely, the efficiency of the two-level inverter increases when the current increases. This reflects the fact that conduction losses changes with the load and are prevalent for the MMC; switching losses do not change substantially with the load and are prevalent for the two-level inverter [101].

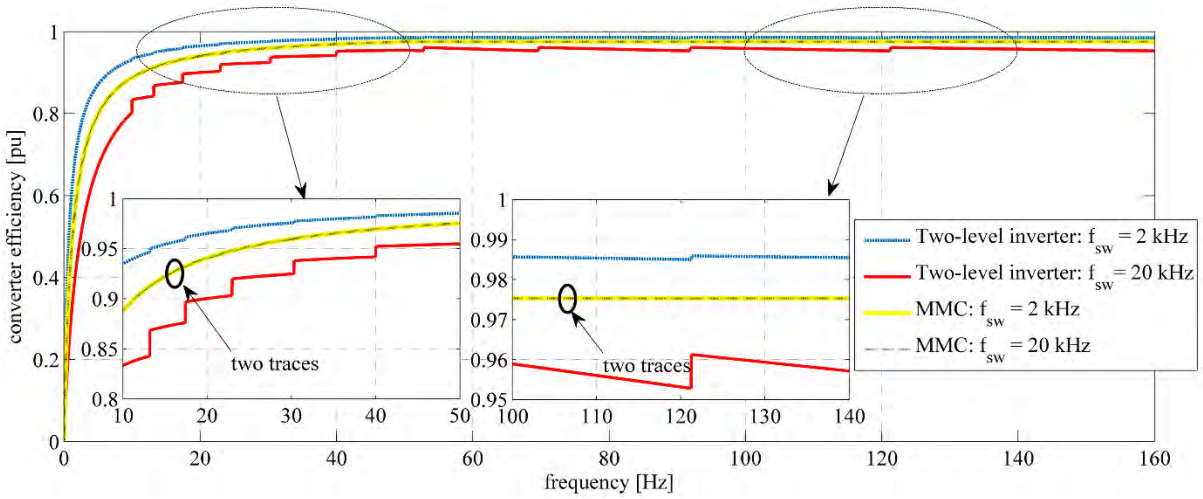


Fig. 5.3: The efficiency for both topologies versus frequency at half full-load current [101].

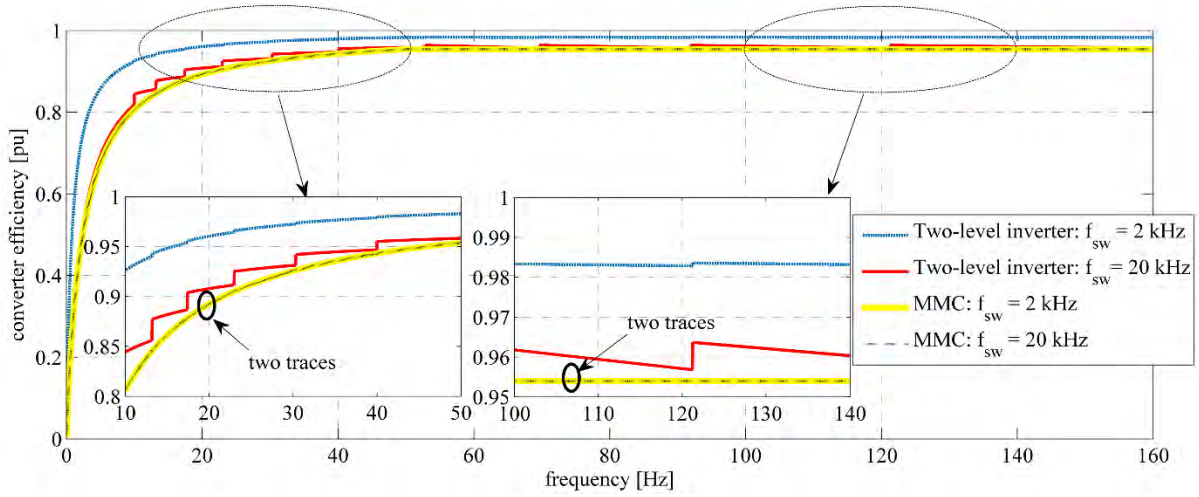


Fig. 5.4: The efficiency for both topologies versus frequency at full-load current [101].

In summary, using a proper modulation strategy, the switching losses of the MMC are much lower than those of traditional inverters and the global efficiency is comparable and even higher

in some cases. The comparison does not consider the power losses of the cell balancing converter used for the traditional inverter and the variation of the efficiency of the traction motor, so the MMC is penalised. Moreover, the global efficiency remains almost constant also at low speed/voltage and light loads, whereas the efficiency of traditional inverters drastically decreases. When the speed and the load of the traction drive is reduced for most of the time, like the case of urban cycles, MMC traction drives operate with higher efficiency with consequent benefits for the vehicle range [101].

Chapter 6

Simulation Results

This chapter describes the operating characteristics of the proposed MMC with embedded battery cells by means of numerical simulations obtained from Matlab/ Simulink (SimPower System Library). The simulation includes results for static and dynamic load and the recharge of the battery cells from the grid, assuming lossless switches.

The chapter also includes a comparison between the level-shift and phase-shift modulation techniques in terms of the harmonic content of the output waveforms and comparative study of the cell equalising time between the proposed converter and a standard active BMS.

6.1 Comparison between CD-SPWM & PSC-SPWM

Fig. 6.1 shows the simulated line-to-line voltages obtained using CD-SPWM and PSC-SPWM for different number of levels of the converter arm. The carrier frequency is set to 5 kHz, the modulation index is set to 0.95, the frequency of the modulating wave is set to 50 Hz and the battery cells have a constant dc voltage equal to 3.7 V. Table 6.1 and Fig. 6.2 summarise the values of the THD for each modulation technique and for a different number of levels. It can be observed that the CD-SPWM scheme produces a level of harmonic distortion of the line-to-line voltages lower than that of the PSC-SPWM technique for every n. Therefore, the CD-SPWM technique has been chosen in the following for the modulation of the voltage waveforms.

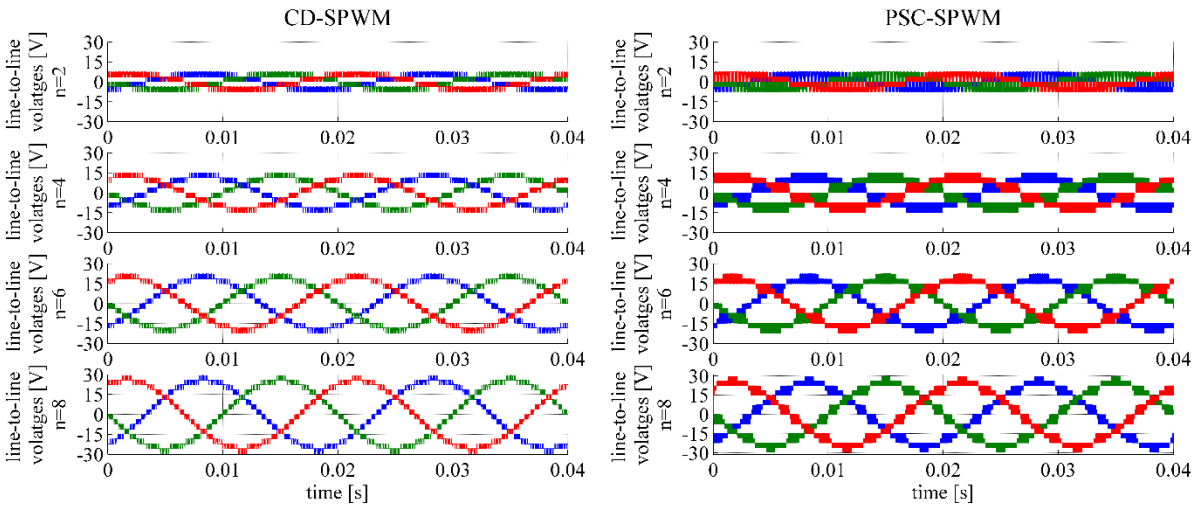


Fig. 6.1: The simulated line-line voltages when the CD-SPWM and PSC-SPWM are applied.

Table 6.1: The THD of line-line voltage

	CD-SPWM	PSC-SPWM
n	THD [%]	THD [%]
2	37.39	46.89
4	17.23	27.36
6	11.55	18.27
8	9.05	12.5

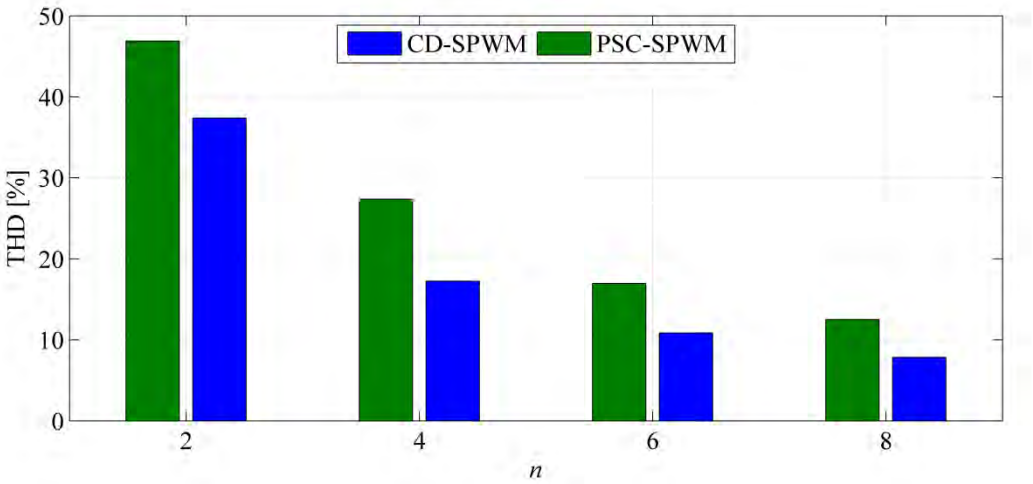


Fig. 6.2: THD versus *n*.

6.2 MMC with a static RL load

The proposed MMC has been initially simulated with a static RL load. Table 6.2 and Table 6.3 summarise the circuit parameters and the control gains used for the simulation. In this example, the converter has 38 Li-ion cells per arm and is controlled with the CD-THIPWM scheme switching frequency of 2 kHz. Since the nominal voltage of a single cell is equal to 3.7 V, the maximum rms value of the line-to-line output voltage is 100 V. The battery cells have been discharged with two different current, at the nominal load current and half of the nominal current. Fig. 6.3 shows the *dq*-axis components of the load current and the active/reactive power drawn by the inductive load.

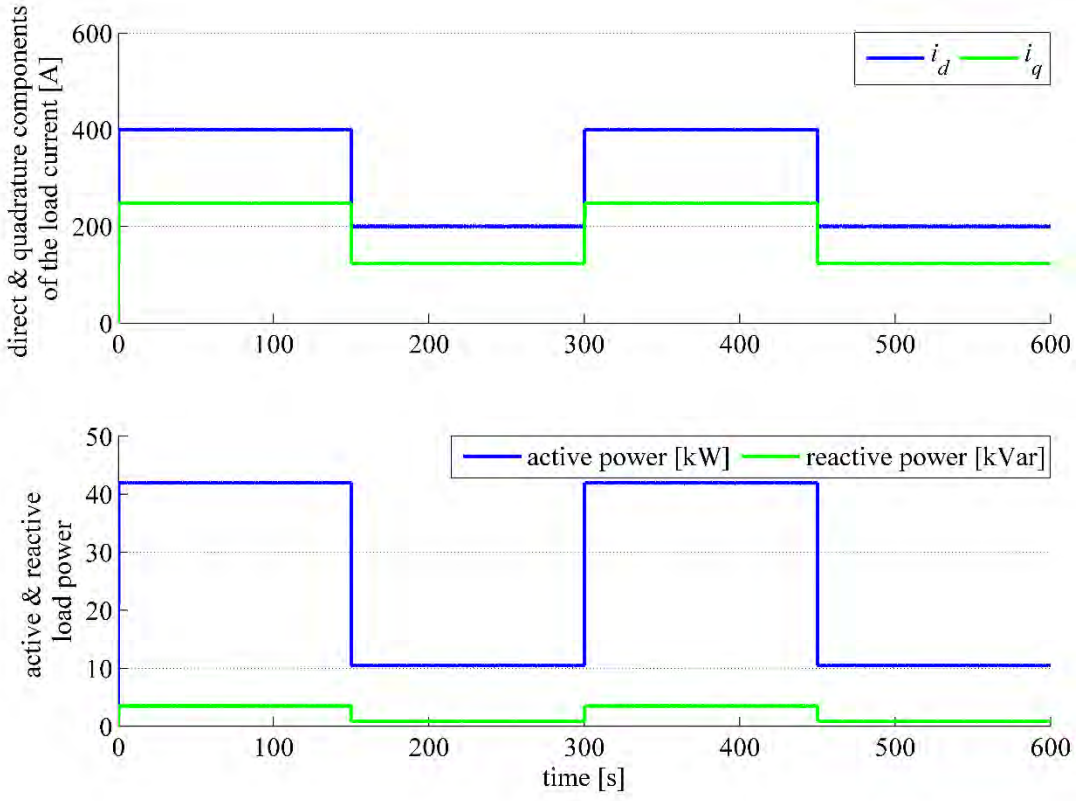


Fig. 6.3: The *dq*-components of load current, active, and reactive load power.

In order to verify the capability of the control algorithm of balancing the SOC of the cells, the simulation starts from an unbalanced condition of the cells. The initial state of charge of the cells has been randomly chosen between 70% and 100%. The battery cells have been modelled using equation (3.15). Table 6.4 summarises the data of the simulated Li-ion battery cell.

Table 6.2: Circuit Parameters used for Simulation

Load active power	P	40 kW
Load power factor	$\cos\varphi$	0.85
Nominal line-line rms voltage	V_n	100 V
Nominal rms current	I_n	270 A
Nominal frequency	f_n	50 Hz
Switching frequency	f_{sw}	2 kHz
Arm inductor	L	50 µH
Nominal cell capacity	Q	12.8 Ah
Nominal cell voltage	V_c	3.7 V
Control time step	T_s	50 µs
Number of cells per each arm	n	38

Table 6.3: Control gains used for simulation.

f_n = 0.004 Hz	Proportional gain of leg-energy control	k_1	8.2339×10^4 A
ζ = 35.3553	Integral gain of leg-energy control	k_2	29.2658 A/s
f_n = 0.002 Hz	Proportional gain of arm-energy control	k_3	-8.2339×10^4 A
ζ = 35.3553	Integral gain of arm-energy control	k_4	-14.6329 A/(s)
T = 0.11254 ms	Proportional gain of circulating current control	k_5	4.7445 Ω
f_n = 1 kHz	Proportional gain of load current control	k_6	3.3883 Ω
ζ = 0.707	Integral gain of load current control	k_7	1.5054×10^4 Ω/s

Note: The relations between the control gains and the closed loop natural frequency f_n, the time constant T, and the damping ratio ζ are given in Appendix C.

Table 6.4: Data of the simulated Li-ion cell

E_0 [V]	K [V/(Ah)]	R [mΩ]	A [V]	B [Ah^{-1}]	Q [Ah]
4.0252	0.00026633	0.14375	0.29595	4.7445	12.87

The diagram of the SOC of all the cells of the converter is reported in Fig. 6.4 when the battery cells have been discharged with two different current, at the nominal load current and half of the nominal current. In the first part of the cycle, the cells with higher SOC are

discharged quicker, while the cells with lower SOC are recharged until all the cells have the same SOC after about 420 s. The arm and circulating currents are also presented in Fig. 6.4 at t = 10 s and t = 420 s, respectively. The arm currents consist of two components, the load current and the circulating current, the load currents are not affected by the SOC balancing control and the circulating currents are used to balance the converter arms and legs. The circulating currents have been calculated using (3.2). At t = 10 s, the arm currents are not balanced because of the circulating currents generated by the phase-leg and arm energy controllers. It is worth noting that both controllers have been saturated with an anti-windup so the arm current is limited to 105% of the nominal load current. When the battery cells have been totally balanced at t = 410 s, the converter arm currents become balanced and the circulating currents become very small.

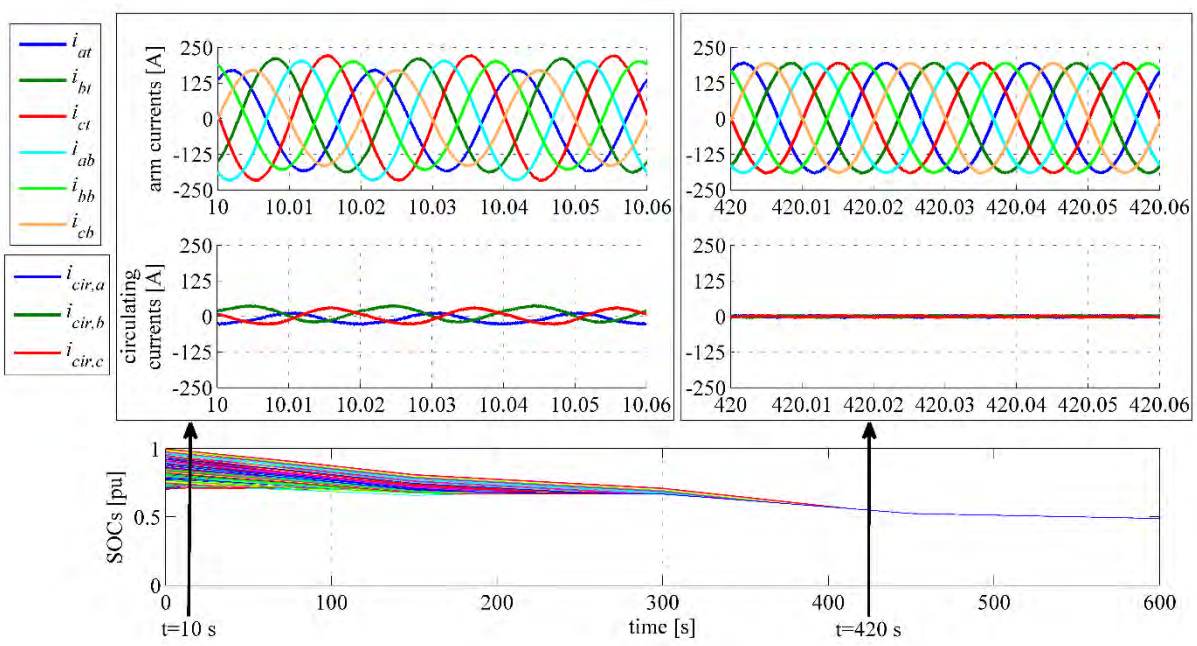


Fig. 6.4: SOCs of the 228 battery cells, arm and circulating currents at 10 s and 420 s.

Fig. 6.5 (a) and (b) show the line voltage and current when the battery cells are discharged at nominal and half nominal load current, respectively. It is clear that they are not affected by

the SOC balancing control and that the MMC produces very high quality voltage with very small THD and negligible distortion of load current even at high power factors. Table 6.5 summarises the THD of both line voltage and current when the cells were discharged at nominal and half nominal load currents.

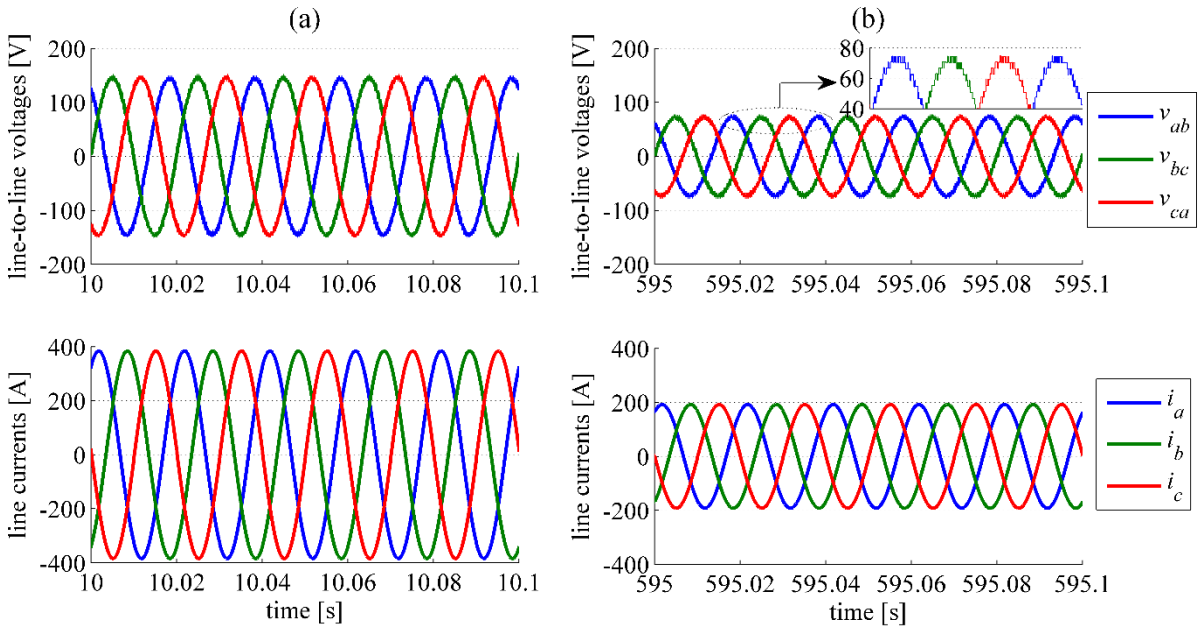


Fig. 6.5: Steady state line-to-line voltages and line currents: (a) Nominal load current. (b) Half nominal load current.

Table 6.5: The THD of line voltage and current.

I_n [A]	THD of the line voltage [%]	THD of the line current [%]
270	1.44	0.03
135	2.72	0.07

Fig. 6.6 (a) shows the transient waveforms for the discharge operation from the nominal load current to the half nominal load current with a step change of the reference load current from 270 A to 135 A, while Fig. 6.6 (b) shows the transient waveforms for the step change of the reference load current from 135 A to 270 A. These waveforms confirm stable operations of the MMC for step-changes of the load conditions.

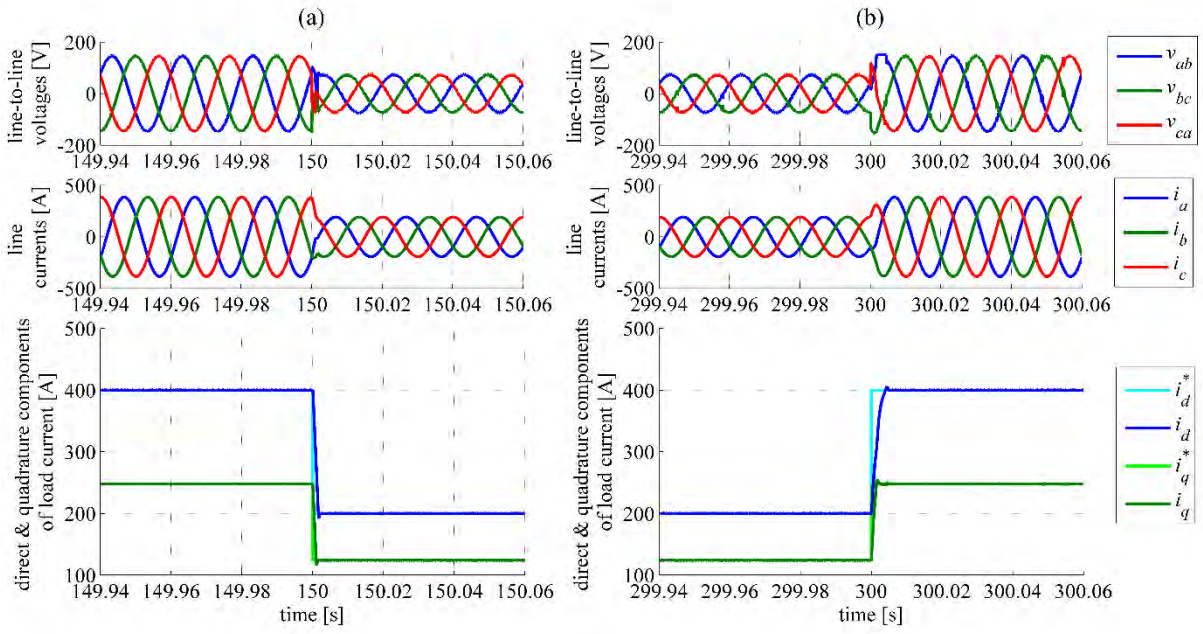


Fig. 6.6: Step-change of the load: (a) load current changed from 270 A to 135 A. (b) load current changed from 135 A to 270 A.

6.3 MMC driving an induction motor

The proposed converter has been simulated as part of the electric drive of a battery EV. In order to obtain realistic results, the public data of an existing electric car (Nissan Leaf) have been used for the simulation [105] and reported in Table 6.7. Table 6.6 summarises the parameters of the converter, whereas Table 6.8 indicates the motor data. In this simulation, the MMC has 84 cells (4.2 V / 12.8 Ah) per arm, with a maximum line voltage of 220 V rms. The initial imbalance of the SOC of the cells has been assumed equal to 40%. The battery cells have been modelled using equation (3.15) and the cells data are reported in Table 6.4. The converter is controlled with a CD-THISPWM scheme with a switching frequency of 4 kHz. The electromagnetic torque, T_{el}, developed by the machine is given by:

$$T_{el} = T_L + (J_m + J_{eq})\frac{d\omega_r}{dt}; \quad T_L = d_1\omega_r + d_2\omega_r^2 + d_3\omega_r^3, \tag{6.1}$$

where T_L is the load torque of the machine, d_1, d_2, and d_3 are three constants depending on the aerodynamic and friction of the car, J_m is the inertia of the machine and J_{eq} is the equivalent vehicle inertia referred to the machine shaft, which can be calculated as (see Appendix B.4):

$$J_{eq} = \frac{1}{4} m_v \left(\frac{D}{\tau} \right)^2, \tag{6.2}$$

where m_v is the vehicle weight in [kg], D is the wheel diameter in [m], and τ is the transmission ratio. Table 6.9 summarises all parameters used for the mechanical model and Table 6.10 summarises the control gains used for simulation.

Table 6.6: Converter Parameters used for Simulation.

Arm inductor	L	50 µH
Nominal cell capacity	Q	12.8 Ah
Nominal cell voltage	V_c	3.7 V
Control time step	T_s	20 µs
Number of cells per each arm	n	84
Switching frequency	f_{sw}	4 kHz

Table 6.7: Main data of the simulated vehicle

Transmission ratio	Battery capacity [kWh]	Wheelbase [m]	Curb weight [kg]	Maximum vehicle speed [km/h]
7.94:1	24	2.7	1525	143

Table 6.8: Motor electric data

Nominal power [kW]	Nominal voltage [V]	Pole pairs	Base speed [rpm]	Nominal Current [A]	Base frequency [Hz]
80	220	1	2730	260	50

Table 6.9: Parameters used for the mechanical model.

d_1 [N.m.s]	d_2 [N.m.s^2]	d_3 [N.m.s^3]	J_{eq} [kg.m^2]	J_m [kg.m^2]
1.81×10^{-2}	2.2453×10^{-5}	9.4852×10^{-9}	2.034	0.32

Table 6.10: Control gains of energy balance control, circulating current control, motor speed control, motor current control and motor flux control used for simulation.

f_n = 0.0004 Hz	Proportional gain of leg-energy control	k_1	8.2339×10^3 A
ζ = 35.3553	Integral gain of leg-energy control	k_2	0.2927 A/s
f_n = 0.0002 Hz	Proportional gain of arm-energy control	k_3	-8.2339×10^3 A
ζ = 35.3553	Integral gain of arm-energy control	k_4	-0.1463 A/s
T =0.11254 ms	Proportional gain of circulating current control	k_5	0.4443 Ω
f_n = 50 Hz	Proportional gain of motor speed control	k_8	1.0459×10^3 kg m^2 s
ζ = 0.707	Integral gain of motor speed control	k_9	2.3233×10^5 kg m^2
f_n = 300 Hz	Proportional gain of motor current control	k_{10}	0.6807 Ω
ζ = 0.707	Integral gain of motor current control	k_{11}	907.2383 (V s)/A
f_n = 5 Hz	Proportional gain of motor flux control	k_{12}	9.5647×10^2 A/wb
ζ = 0.707	Integral gain of motor flux control	k_{13}	2.4101×10^4 A s wb

Note: The relations between the control gains and the closed loop natural frequency f_n, the time constant T, and the damping ratio ζ are given in Appendix C.

Fig. 6.7 shows the motor speed, torque, mechanical power, and flux when the vehicle accelerates from 0 to 100 km/h. In the constant torque region, the machine operates at the rated value of the air-gap flux to produce a maximum torque of 280 Nm. In the constant power region, the machine flux and the torque decrease with an inverse law of the motor speed to produce a maximum mechanical power of 80 kW. The time to accelerate the vehicle from 0 to 100 km/h is about 11.9 s in agreement with the data of the manufacturer [105].

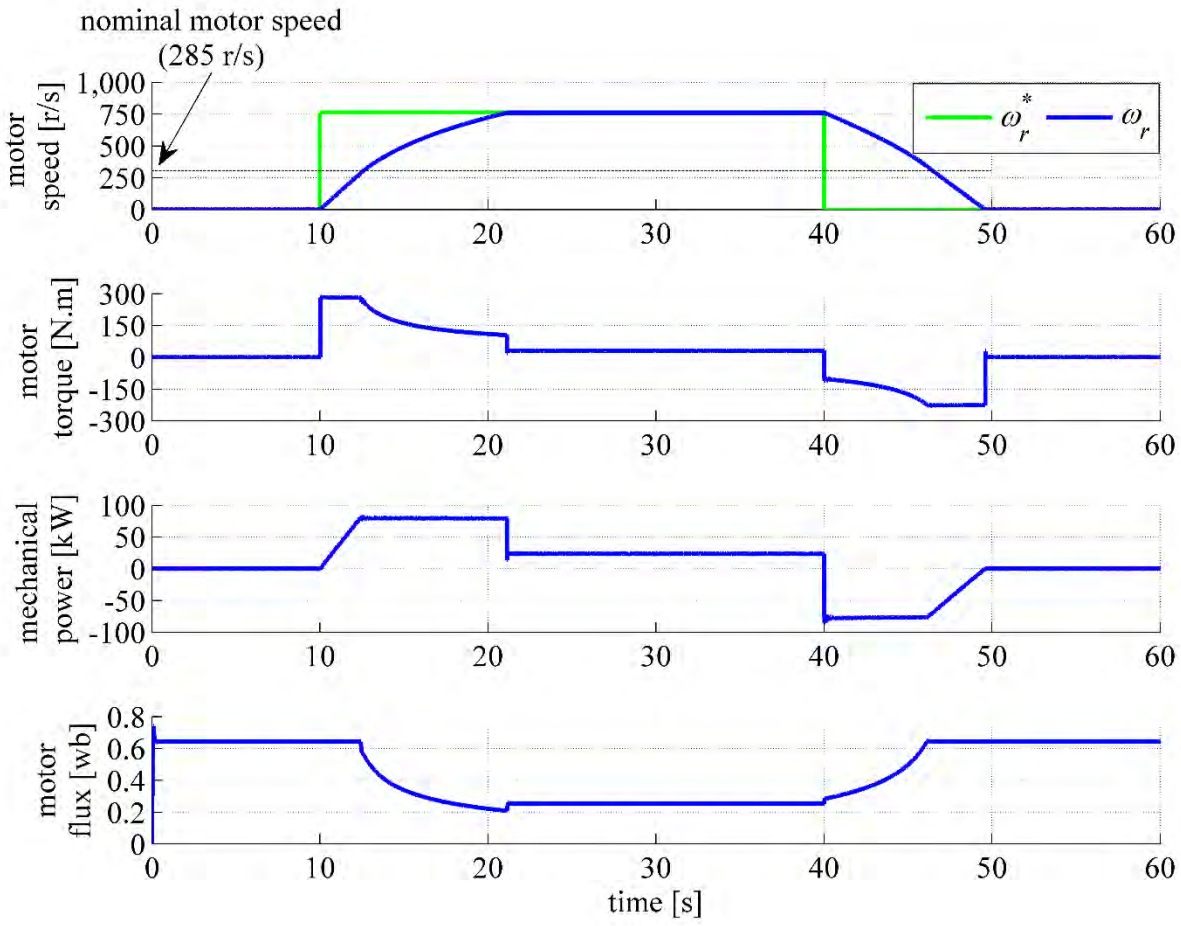


Fig. 6.7: The machine speed, torque, power, and flux.

The balancing capabilities of the converter have been tested supposing that the vehicle travels on the New European Driving Cycle (NEDC), shown in Fig. 6.8. The NEDC combines the Urban Driving Cycle (UDC), which is repeated four consecutive times, and the Extra-Urban Driving Cycle (EUDC), which has a maximum speed of 120 km/h [107].

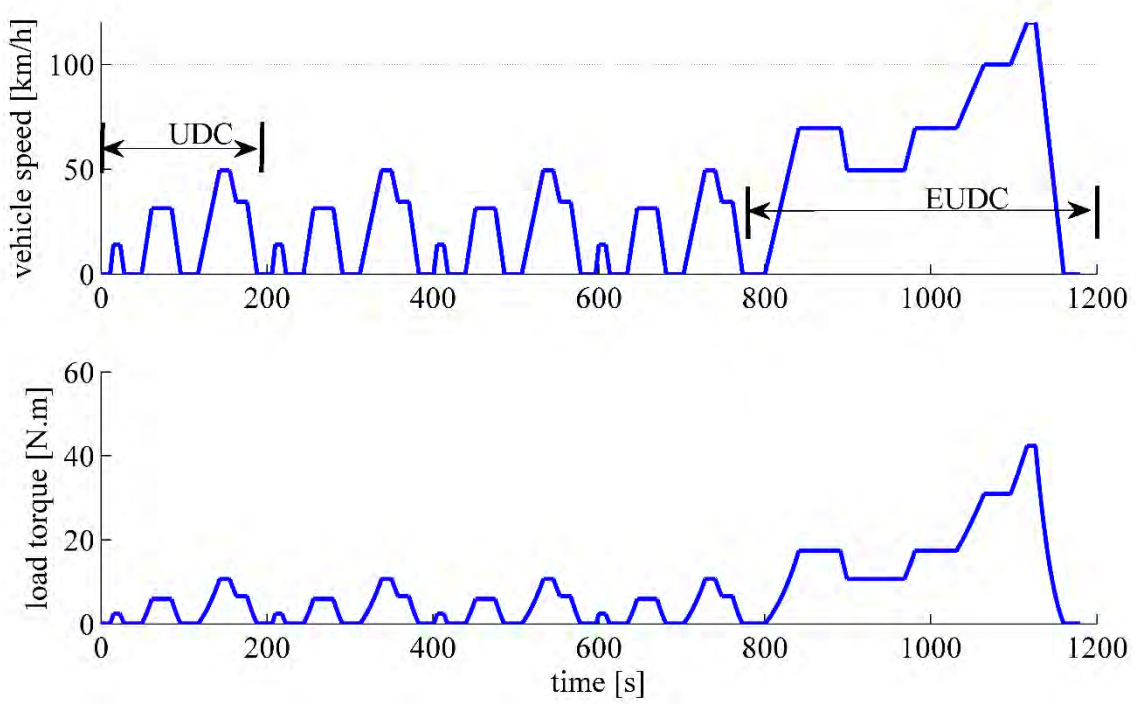


Fig. 6.8: The NEDC and the load torque.

Fig. 6.9 shows the motor line voltages and line currents when the vehicle accelerates from standstill to a speed of 15 km/h in 4 seconds. The simulation shows that the converter produces the required torque at low speed without any overcurrent. This is because the power is generated within the sub-modules, so this MMC does not suffer from the high voltage ripple on the dc-link of the SMs in traditional MMCs.

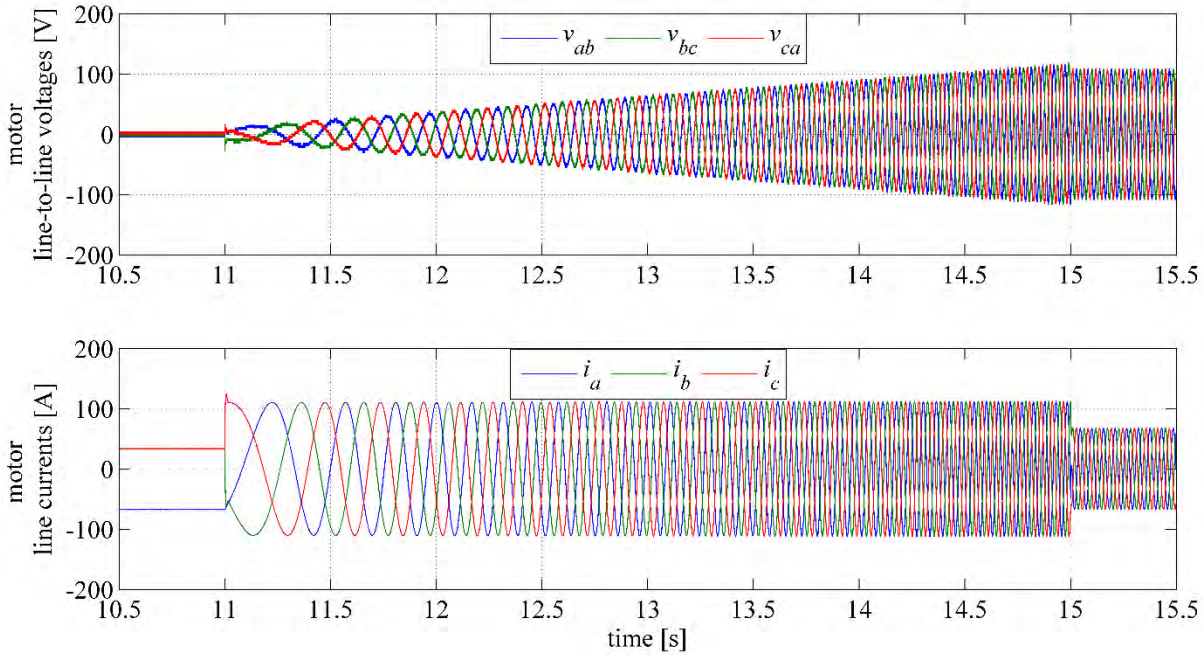


Fig. 6.9: Motor line-to-line voltages and currents when the vehicle accelerates from 0 to 15 km/h.

Fig. 6.10 shows the motor speed and cells' SOC. This result shows that a proper speed of the motor is obtainable for the whole driving cycle. Moreover, the SOC balancing control works appropriately and all the cells are completely balanced after 887 seconds.

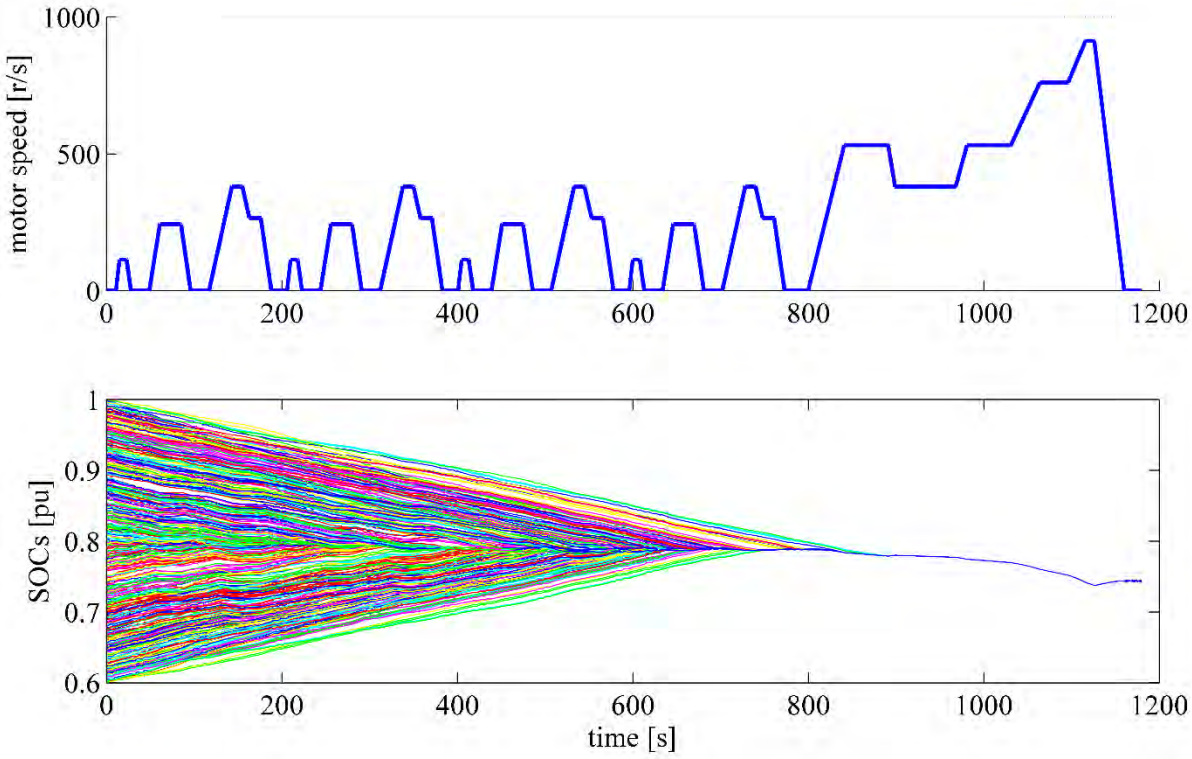


Fig. 6.10: The motor speed and SOCs of battery cells [101].

The effect of SOC balancing control on the arm currents, circulating currents, motor line-to-line voltages and motor line currents are measured during and after the balancing at t = 14 s and t = 887 s. Fig. 6.11 shows the converter arm and circulating currents whereas Fig. 6.12 shows the motor line-to-line voltages and line currents. The circulating currents are dependent on the energy arm/leg unbalancing of converter. Since the converter legs and arms have different initial energy, the leg-energy balance controllers inject dc and fundamental components to the circulating currents in order to balance the cells. When the balancing is complete, the converter legs and arms are balanced and the circulating currents decrease to zero. It is worth noting that the load currents are always balanced regardless of the SOC imbalance of the cells, as illustrated in Fig. 6.12.

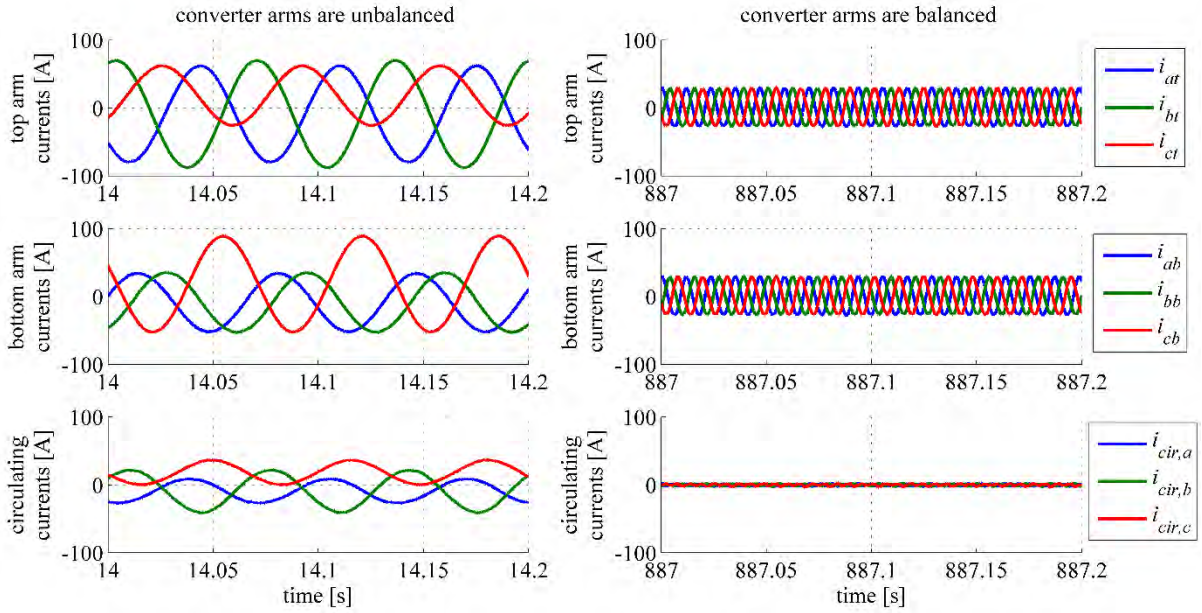


Fig. 6.11: The converter arm and circulating currents at t = 14 s and t = 887 s.

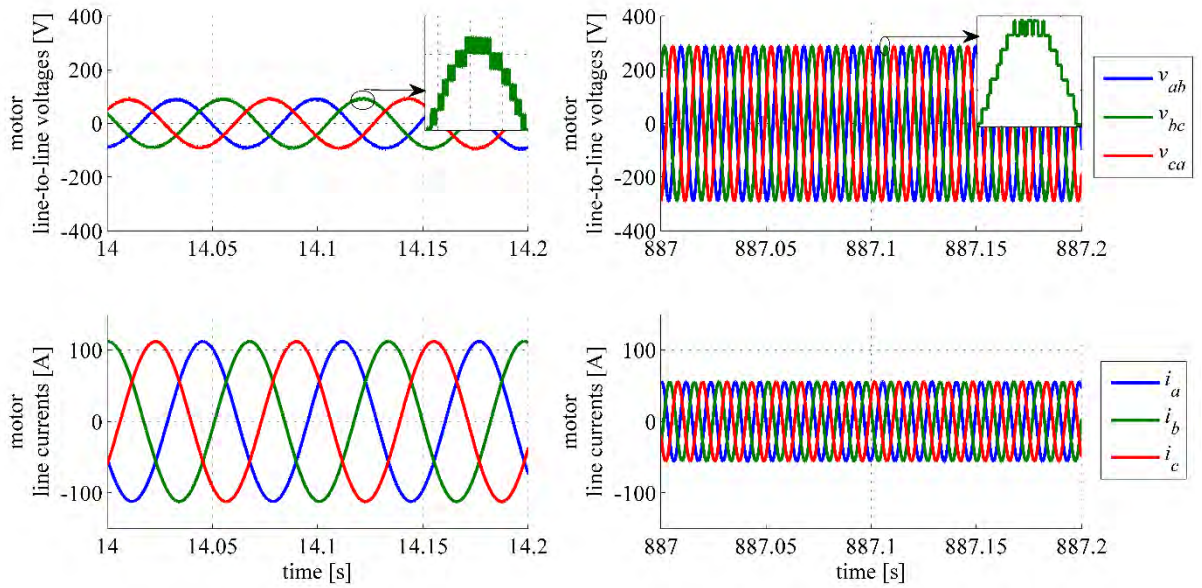


Fig. 6.12: The motor line-to-line voltages and line currents at t = 14 s and t = 887 s.

Fig. 6.13 shows the q-axis component of the stator current and the machine torque, while Fig. 6.14 shows the d-axis component of the stator current and the magnitude of rotor flux.

These figures confirm that the vector control can be achieved for the full frequency range of the motor.

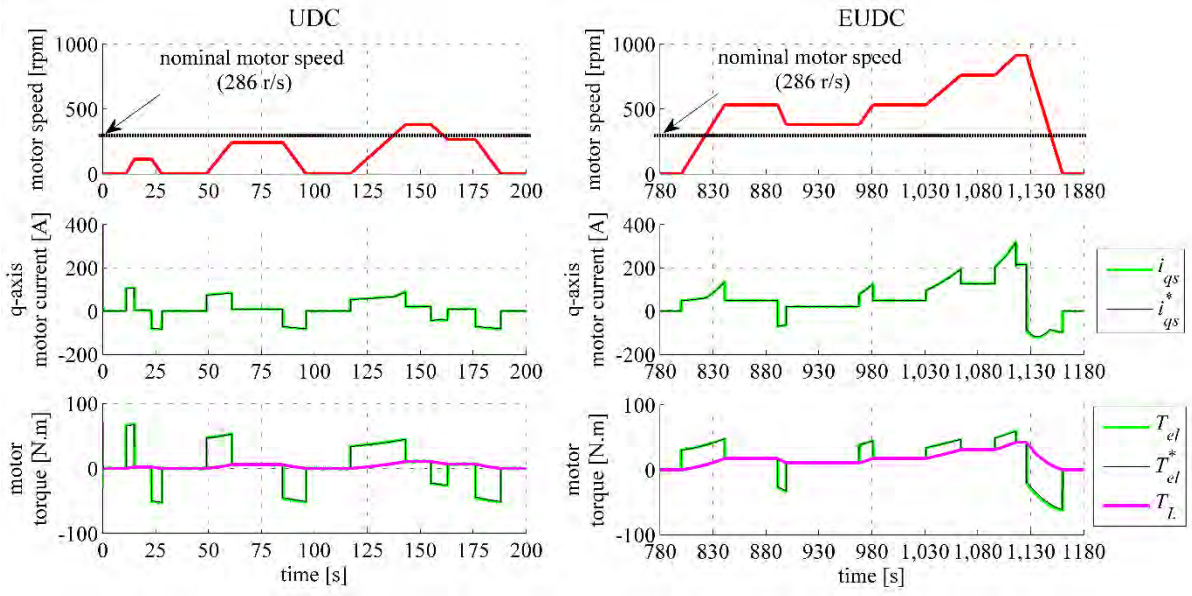


Fig. 6.13: The *q*-axis component of stator current and the machine torque.

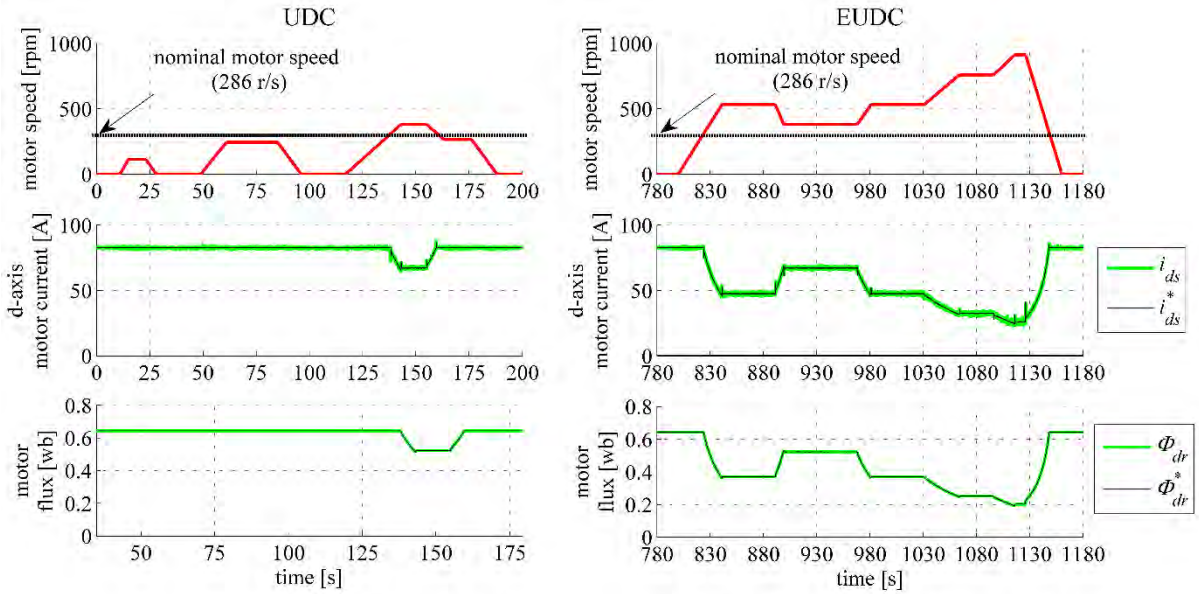


Fig. 6.14: The *d*-axis component of stator current and the magnitude of rotor flux.

Fig. 6.15 shows the motor electric power, electric frequency and the rms value of motor voltage and current respectively. Using equations (5.15) and (5.16), the switching and

conduction losses are calculated for the NEDC to estimate the converter efficiency of the proposed MMC and compare the result with the efficiency of a two-level inverter. The result of the comparison is illustrated in Fig. 6.16. The left part of Fig. 6.16 shows the vehicle speed, the estimated switching and condition losses, and the efficiency for both topologies during one consecutive time of the UDC, while the right part of the figure shows the vehicle speed, the estimated switching and condition losses, and the efficiency for both topologies during the EUDC. The results show that MMC has most of the time a better efficiency. This result is in agreement with the conclusion of chapter 5, because for a urban cycle or a predominantly urban cycle, the drive works for most of the time with a power lower than the maximum value. Therefore, the MMC is particularly suitable for battery EV, where the average efficiency of the drive across a wide power range is more important than the peak efficiency.

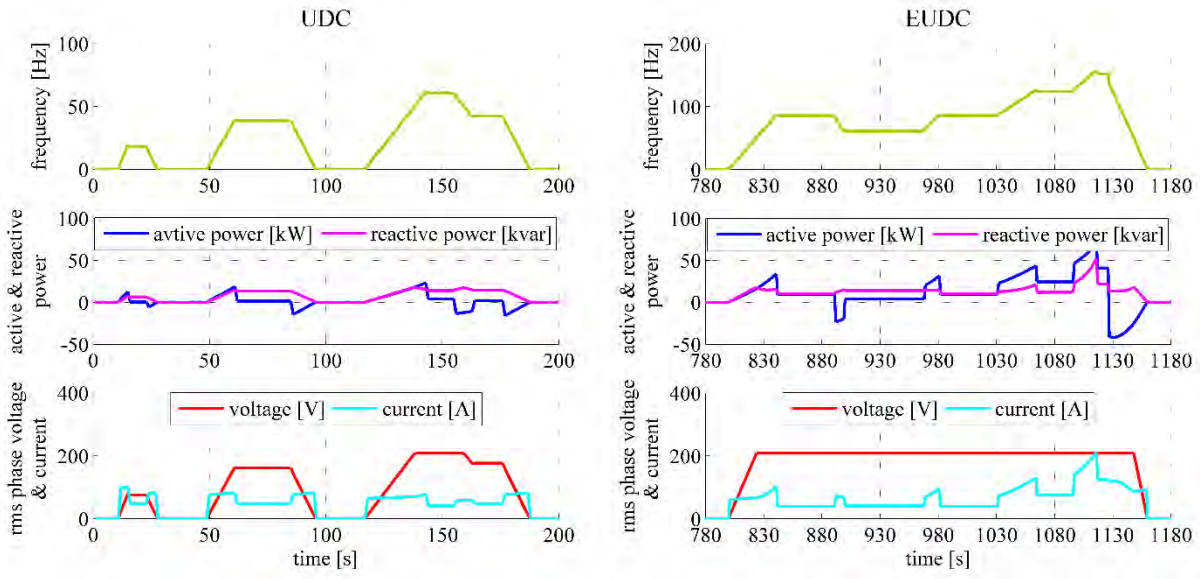


Fig. 6.15: The motor electric power, frequency, voltage and current [101].

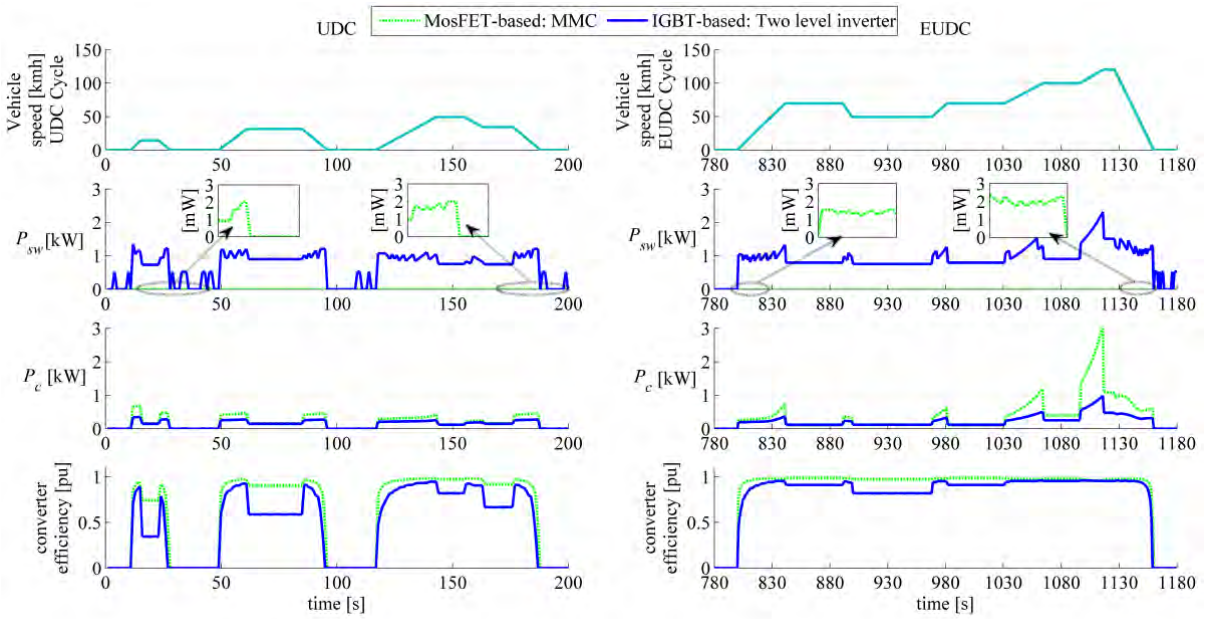


Fig. 6.16: The converter efficiency, switching and conductions losses [101].

6.4 MMC recharging battery cells from the grid

6.4.1 PLL for a three-phase utility interface

A closed loop PLL algorithm has been developed to interface the MMC with a three-phase grid. Fig. 6.17 shows the response of the PLL when the closed loop natural frequency f_n is equal to 50 Hz, 100 Hz and 1 kHz, respectively. In this simulation, the damping ratio ζ is set to 0.707 and the peak of the grid phase voltage is 311 V. The gains of the loop filter are k_{14} = 2.4734, 4.9467, and 49.4673 and k_{15} = 549.4431, 2.1978×10^3, and 2.1978×10^5, respectively. As expected from theory, the designed PLL is capable of reconstructing the phase and frequency information of the grid for all cases and higher bandwidth of the controller gives a faster dynamic response.

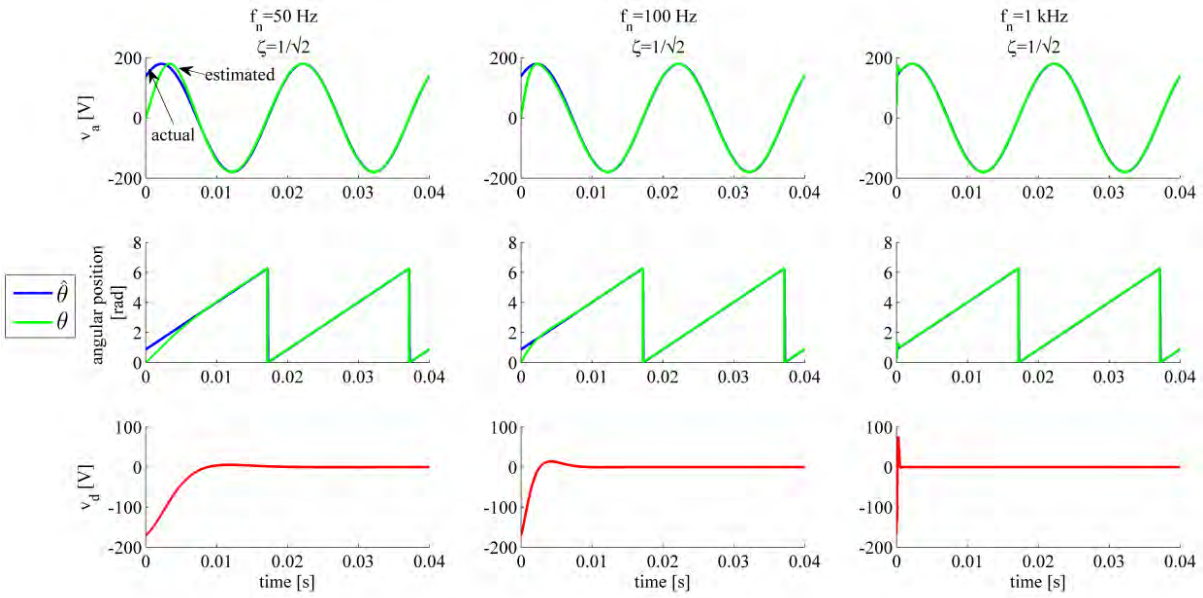


Fig. 6.17: Simulated results of three-phase PLL system: actual and estimated grid phase voltages, angular position, and the d-axis components of grid voltage.

6.4.2 Stationary charge/discharge of the batteries

In order to prove the possibilities for stationary charge/discharge of the battery cells, the proposed MMC has been connected to a three-phase grid. In this simulation, the MMC has 84 cells (4.2 V / 12.8 Ah) per arm, with a maximum line voltage of 220 V rms. The battery cells have been modelled using equation (3.15) and the data of the Li-Ion cell are given in Table 6.4. In order to obtain a linear modulation, the MMC is connected to a 220 V, 50 Hz ideal three-phase voltage source with a standard maximum charge power of 44 kW. It has been assumed that the grid frequency randomly changes within the limits specified by the electricity supply regulations (i.e. ±1% of nominal grid frequency). The control of the converter is based on a sampling time of 50 μs and the control gains of both PLL and current controllers are summarised in Table 6.11. In order to show the balancing capability of the proposed converter, the initial SOCs of battery cells have been set to random values between 30% and 60% and

then repetitively charged and discharged at the rated power of 44 kW.

Table 6.11: Control gains of energy balance control, circulating current control, PLL and the grid current control used for simulation.

f_n = 0.0004 Hz	Proportional gain of leg-energy control	k_1	8.2339×10^3 A
ζ = 35.3553	Integral gain of leg-energy control	k_2	0.2927 A/s
f_n = 0.0002 Hz	Proportional gain of arm-energy control	k_3	-8.2339×10^3 A
ζ = 35.3553	Integral gain of arm-energy control	k_4	-0.1463 A/s
T = 0.11254 ms	Proportional gain of circulating current control	k_5	0.4443 Ω
f_n = 1.5 kHz	Proportional gain of PLL control	k_{14}	4.9467 rad/(V s)
ζ = 0.707	Integral gain of PLL control	k_{15}	2.1978×10^3 rad/(V s^2)
f_n = 1 kHz	Proportional gain of grid current control	k_{16}	0.2221 Ω
ζ = 0.707	Integral gain of grid current control	k_{17}	986.9604 (V s)/A

Note: The relations between the control gains and the closed loop natural frequency f_n, the time constant T, and the damping ratio ζ are given in Appendix C.

The response of the PLL is presented in Fig. 6.18. A low closed-loop bandwidth of 100 Hz with damping ratio equal to 0.707 has been chosen to reduce the tracking errors due to distorted utility conditions, such as the phase unbalancing, harmonics, offset caused by nonlinear loads and measurement errors [98].

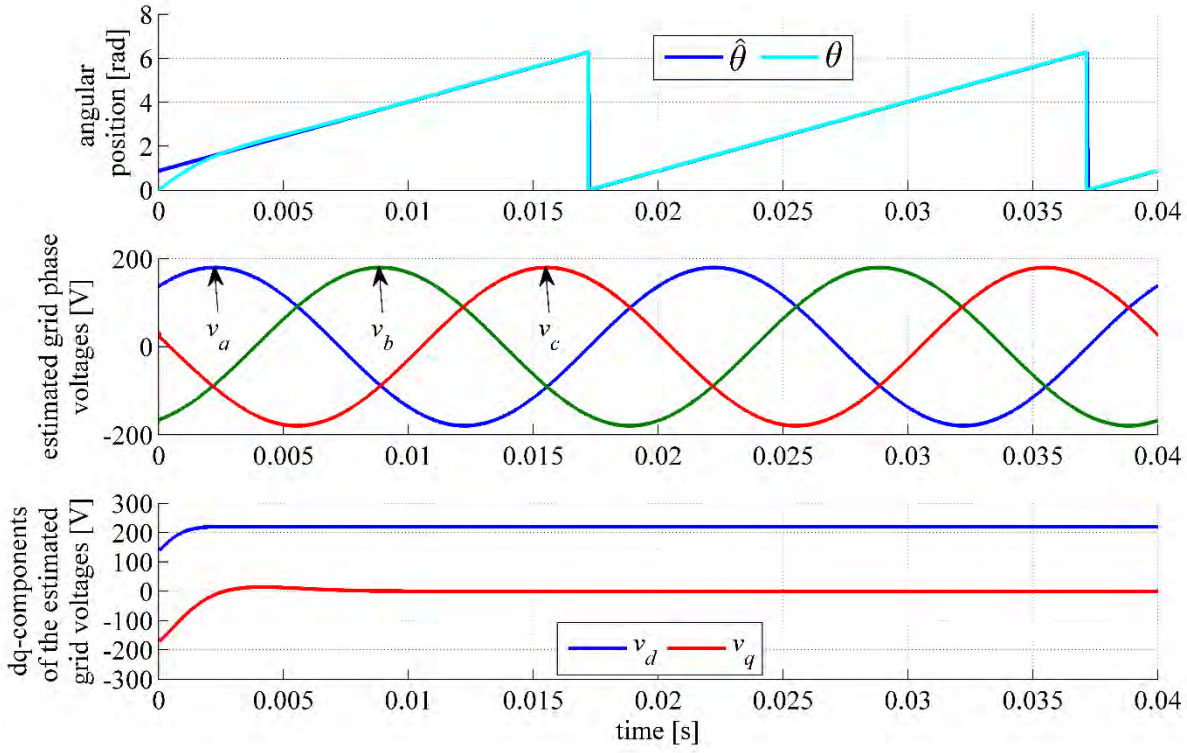


Fig. 6.18: Simulation of the three-phase PLL: angular position, actual and estimated grid phase voltages and *dq*-axis components of the grid voltage.

Fig. 6.19 shows the grid active and reactive powers, the *d*-axis and *q*-axis components of the line current and the SOC of the battery cells. The SOC-balancing control is effective also for the recharge and is completed within 15 minutes.

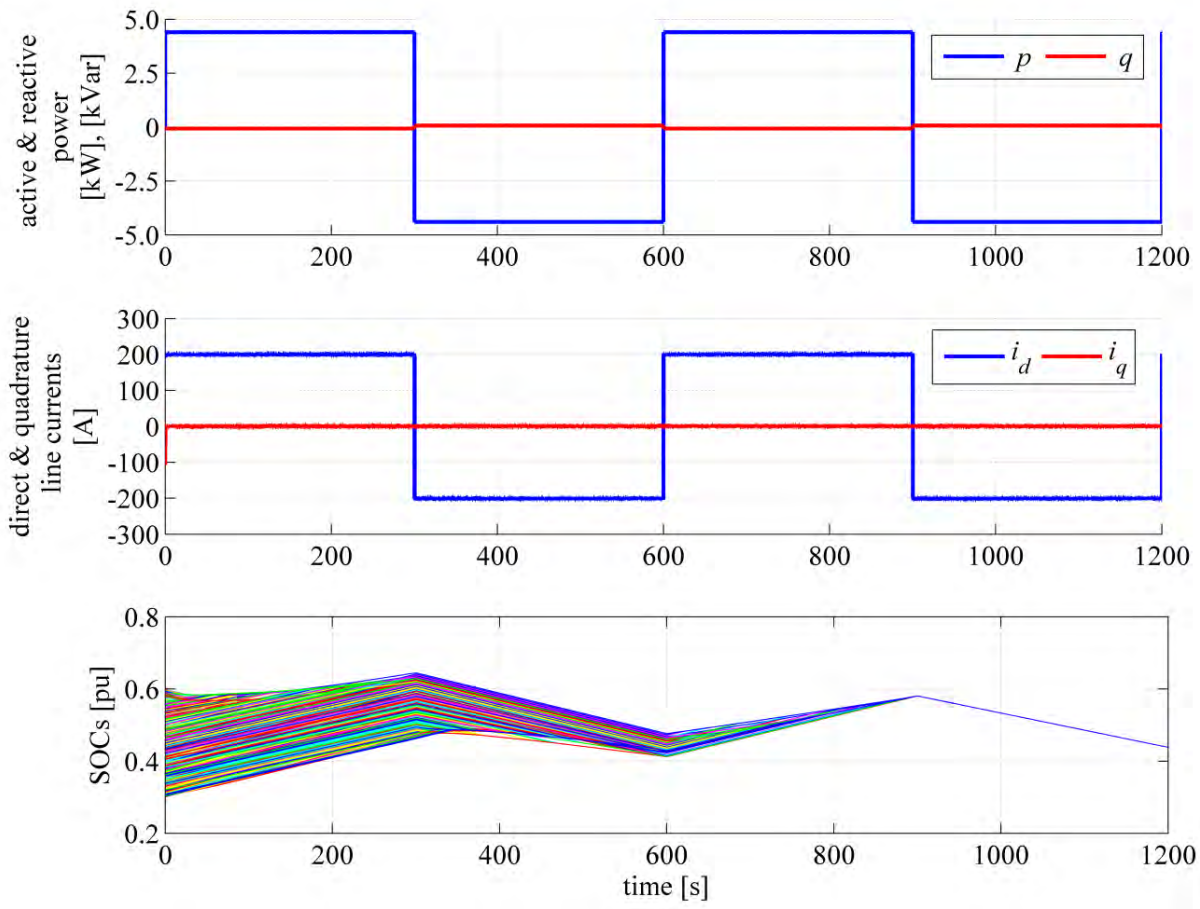


Fig. 6.19: Simulated waveforms with repetitive charging and discharging of the battery cells.

Fig. 6.20 shows the converter arm and circulating currents, during charging at 44 kW (a) and discharging at 44 kW (b). Since the converter legs and arms have different initial energy, the leg-energy balance controllers inject the dc and the fundamental components to the circulating currents in order to achieve energy arm/leg balance, as shown in Fig. 6.20 (a). When the balancing is complete, the converter legs and arms are balanced and then the circulating currents decrease to zero, as shown in Fig. 6.20 (b).

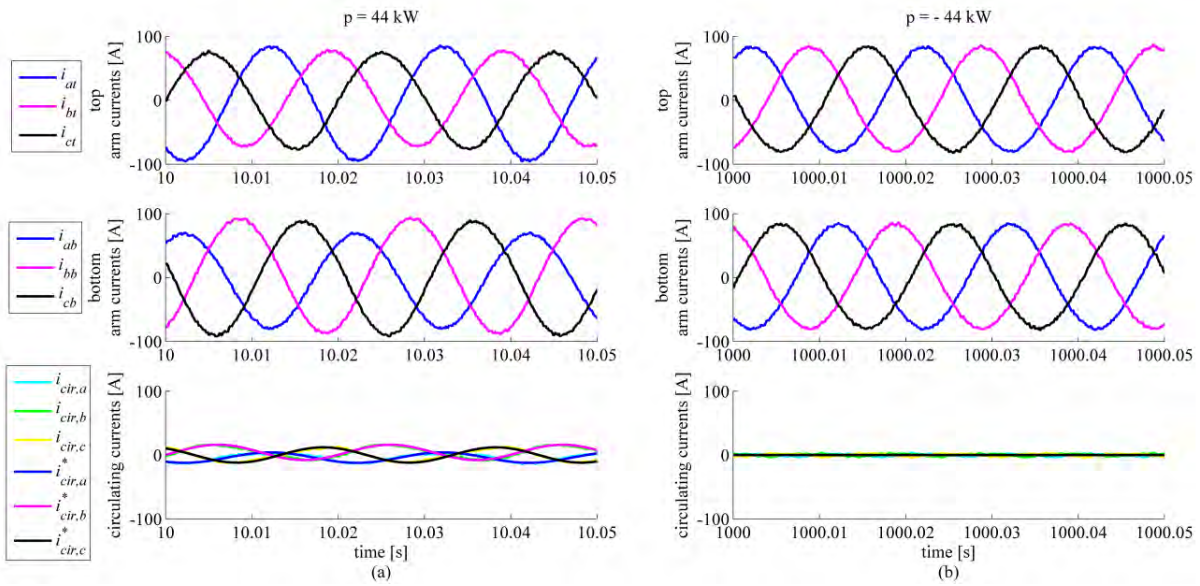


Fig. 6.20: Converter arm and circulating currents.

Fig. 6.21 shows the simulated arm voltages, grid phase voltages and line currents during the recharge at 44 kW (a) and the discharge at 44 kW (b). When the battery cells are recharged, the waveforms v_k and i_k are in phase showing that the converter operates at (nearly) unity power factor. The same applies when the battery cells are discharged and v_k and i_k are out of phase of 180˚.

It is worth noting that unlike traditional two-level converters, the MMC produces a high quality line current with a THD of 1.1% without any additional external filter.

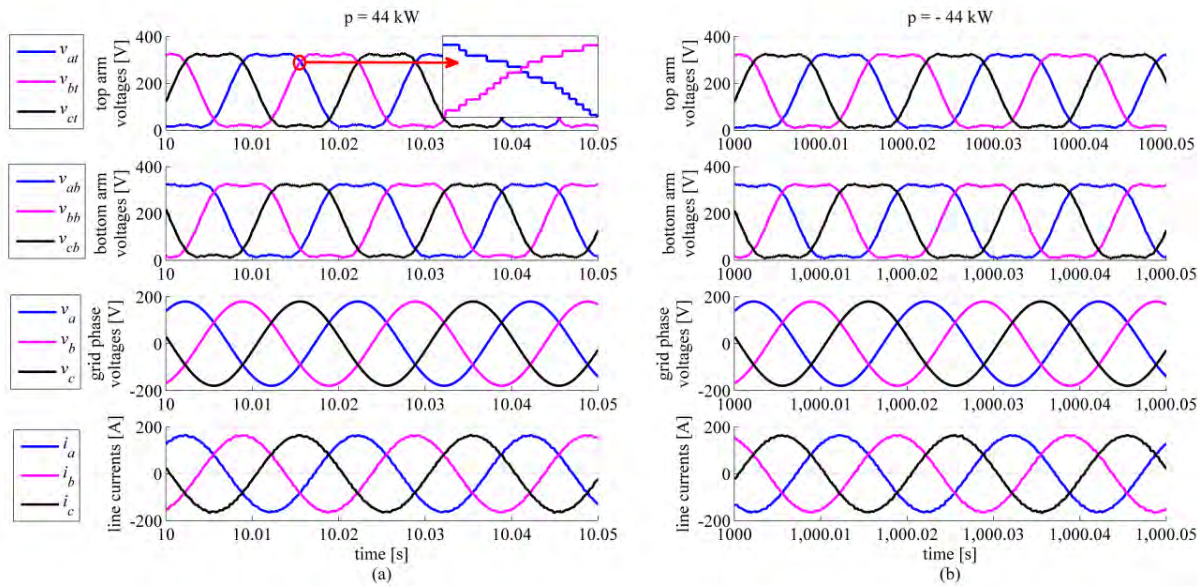


Fig. 6.21: Converter top/bottom arm voltages, grid phase voltages, and line currents.

6.4.3 Stationary recharge of battery cells

The MMC is the same as the previous section and the battery cells have been recharged up to 100% starting from an initial SOC of 10%, supposed to be the same for all the battery cells. The MMC is connected to a 220 V, 50 Hz ideal three-phase voltage source with a standard maximum charge power of 44 kW.

In order to preserve the life of battery cells, the recharge current is constant until the cells reach their maximum voltage. Thereafter, the voltage is maintained constant until the recharge is complete. The quadrature component of the grid current is set to 0 to have a recharge at (nearly) unity power factor. The direct component of the grid current is set according to equation (4.55).

The SOC, current and voltage of one cell are reported during the recharge process in Fig. 6.22. The cell is initially recharged with a constant current until it reaches its maximum voltage, then it is charged with a constant maximum voltage until the current declines to zero for unity SOC.

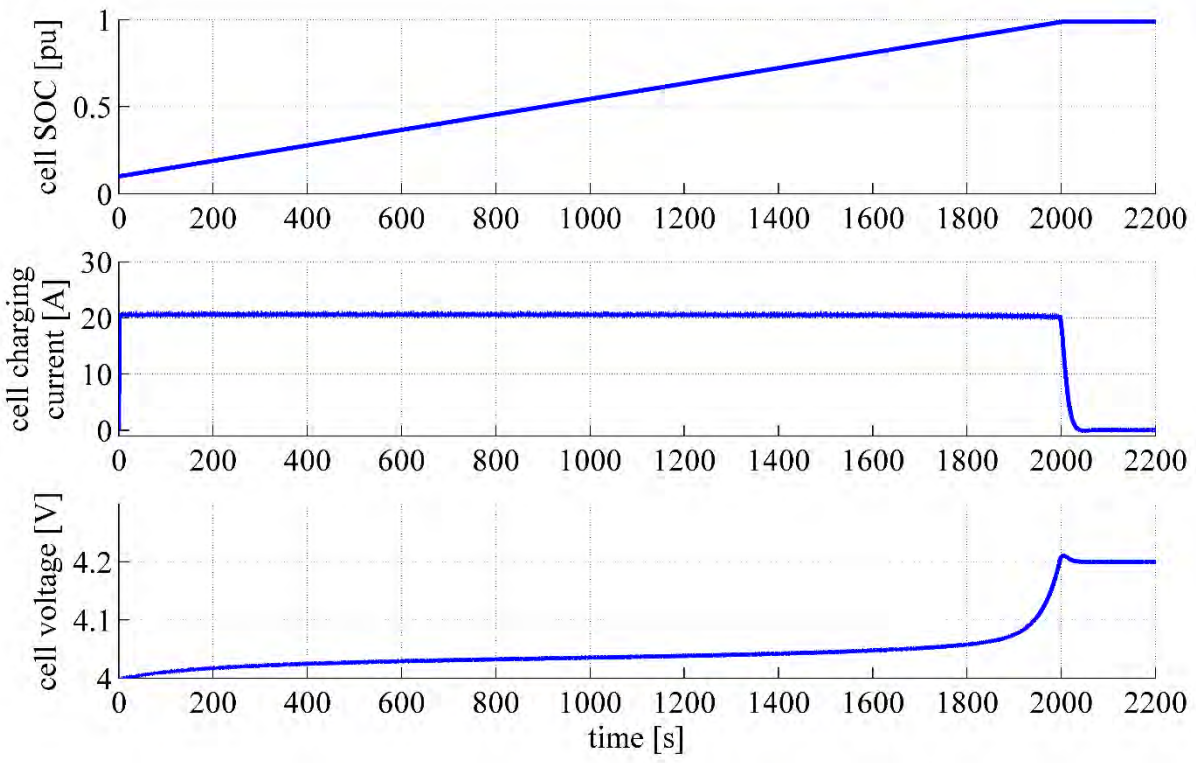


Fig. 6.22: Cell SOC, voltage, and current.

The top figure of Fig. 6.23 shows the line currents drawn by the MMC, the middle figure shows the *d*-axis and *q*-axis components of the line currents and the bottom figure shows the power drawn by the grid during the recharge process. The grid current is almost sinusoidal during the whole recharge process. In the constant current region, the power drawn by the grid is linearly proportional to the cell voltage and increases from 42 kW to 44 kW. When the SOC approaches the full charge, the power goes down to zero for unity SOC. The battery cells are completely recharged in about 34 minutes, in agreement with the figures given by the manufacturers of commercial vehicles [109].

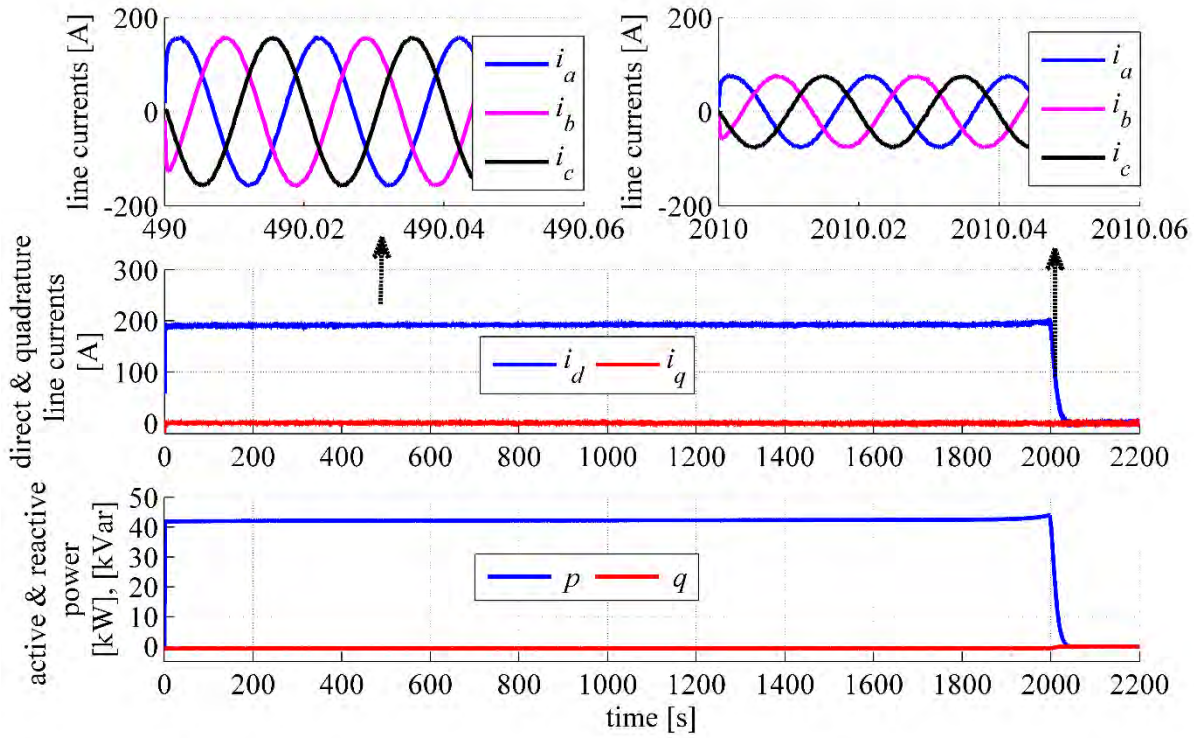


Fig. 6.23: Line currents drawn by the MMC, *d*-axis and *q*-axis components of the line currents, and powers drawn by the grid.

6.4.4 Effectiveness of the SOC balancing control

In order to show the balancing capability of the proposed converter during the recharge process, the SOC of the battery cells have been selected with a maximum imbalance of 20% and an initial SOC between 10% and 30%.

Fig. 6.24 shows that the SOC of all battery cells is balanced within 20 minutes, while the cells are completely recharged within 30 minutes.

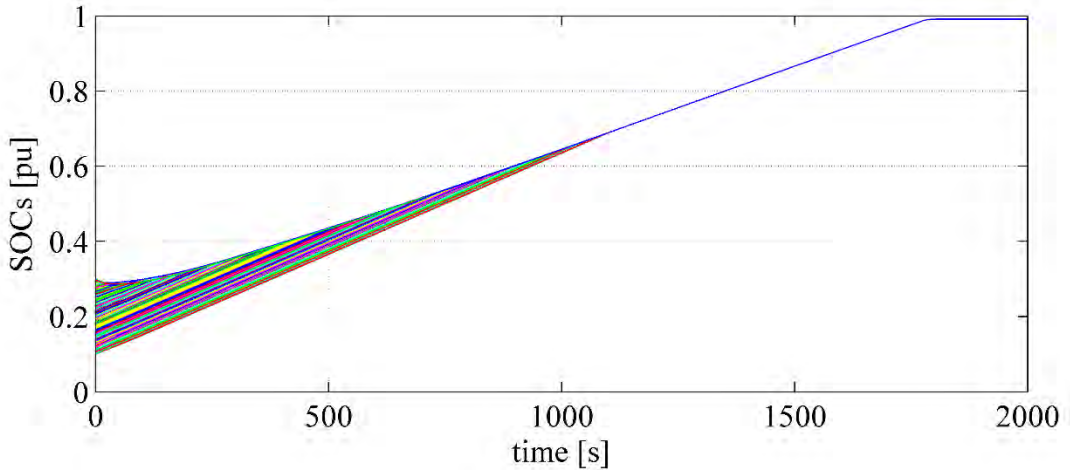


Fig. 6.24: The SOCs of cells.

The detail of the voltage, current, and SOC of three representative cells within one arm are reported in Fig. 6.25. The cells have initially SOC of 10%, 20%, and 30%. When the SOC-balancing control is started, the cell with the highest SOC is charged slower than the cell with the lowest SOC, as confirmed by the diagrams of the recharge currents.

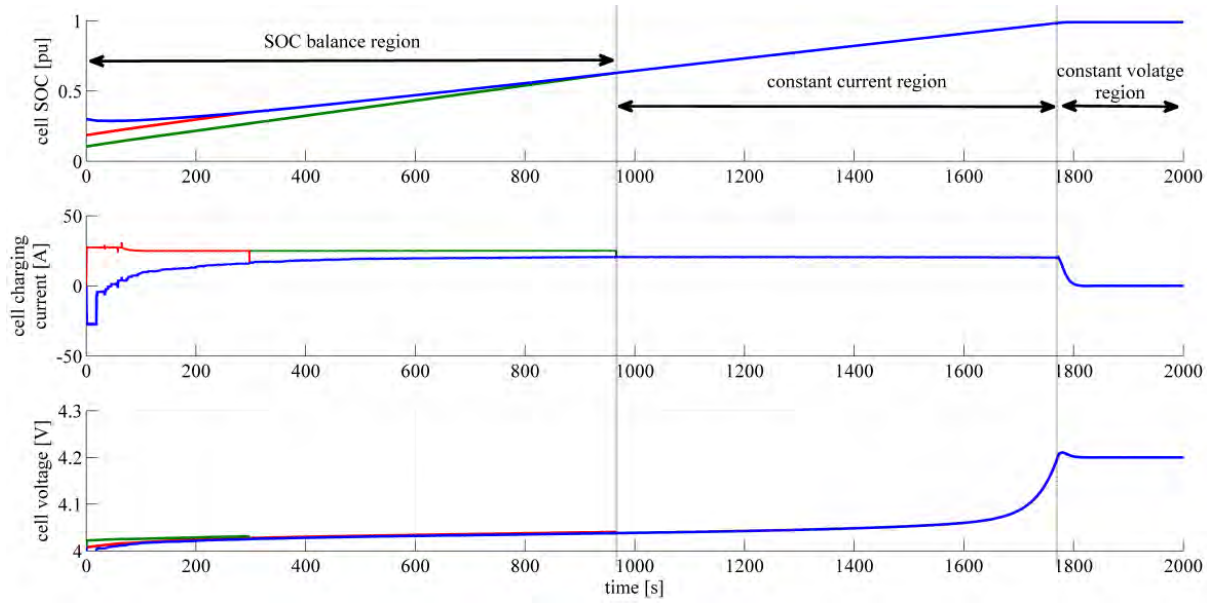


Fig. 6.25: Cell SOC, current, voltage.

The arm current, circulating current, grid current and active and reactive powers have diagrams very similar to the case presented in section 6.4.3.

6.5 Comparison with other battery management systems

The proposed MMC has been compared with the active BMS topologies reviewed in chapter two. Table 6.12 shows the number of elements required by the different BMSs and provides a comparison in terms of size, cost, equalising time and efficiency. Capacitor base methods have smaller energy losses in comparison with inductor/transformer and converter base methods, but longer equalisation time. The SSC has the smallest energy losses and acceptable equalisation time when compared with the SC, DTSC, and MSC [77].

On the other hand, MWT and MSI have an equalisation time smaller than that of capacitor base methods, but they are not suitable for Li-ion batteries because they are based on the voltage differences between cells, which are not so evident in Li-Ion batteries. MWT and MSI use high number of inductors and iron cores, so they have the largest sizes and the highest losses due to the magnetic cores. SWT and SSI have fast equalisation speed and low additional core losses, but they require a complex control. For SWT, the core must be changed to add one or more cells. Filtering capacitors are needed for SSI when a high switching frequency is used. BBC topology has the smallest equalisation time with acceptable energy losses if compared to FbC, CC, and RC methods [14], [77].

Unlike traditional BMSs, the proposed MMC uses the load current to balance the battery cells. Therefore, the cells can be quickly balanced without the losses of the extra hardware required by other BMS. None of the devices used in the proposed topology has high voltage stress issues, reducing the hardware costs. In the practical design, the half-bridge converters and their drivers are mounted on the battery cells and, hence, the power cables and sensing wires are very short and light. As a result, the MMC has the smallest equalisation time and energy losses with acceptable size and cost in comparisons with all aforementioned BMSs [77].

Table 6.12: Comparison of the proposed MMC with different BMSs [77].

Topology	L	C	SW	D	IC	Size	Cost	Equalizing Time	Efficiency
SC	0	$N-1$	$2N$	0	0	+	+	±	+++
DTSC	0	$(3N-3)/2$	$2N$	0	0	+	+	++	+++
SSC	0	1	$N+5$	0	0	++	++	+	+++
MSC	0	$N-1$	$2N+2m$	0	0	+	+	+	+++
MSI	$N-1$	0	$2N-2$	0	0	+	+	++	++
SSI	1	0	$2N$	$2N-2$	0	+	+	++	++
SWT	2	0	$N+6$	0	1	+	±	+	+
MWT	$N+1$	0	2	0	1	±	±	+	+
BBC	1	1	$N+7$	0	0	+	+	+++	+++
CC	$2N-2$	$N-1$	$2N-2$	0	0	+	+	++	++
FbC	$2N$	1	$2N$	0	N	±	±	+	+
RC	$N/2$	N	N	N	1	±	±	+	+
MMC	**6**	**0**	**2*N***	**0**	**0**	**+**	**+**	**+++**	**+++**

L: Inductor, C: Capacitor, SW: Switch, D: Diode, IC: Iron Core,
N: number of cells, m: number of modules,
+++: Excellent, ++: Very good, +: Good, ±: Satisfactory, and – –: Poor.

The equalising time of the proposed MMC has been compared to the standard active cell balancing proposed in [108]. For the purpose of the comparison, the proposed converter has been tested with 8 Li-ion batteries (4.2 V / 10 Ah) per arm with a highly inductive load of 10 A. In agreement with [108], the highest voltage of cell C1 has initial voltage of 4.17 V, the lowest voltage of cell C8 has initial voltage of 3.17 V and the voltages of the remaining cells (C2 ~ C7) are ~ 3.67 V [77].

Fig. 6.26 shows that the voltage difference between cell 1 and cell 8 decreases from 1.0 V to 0.5 V in 46 minutes compared to 180 min necessary for the BMS proposed in [108]. The reason of the very low equalisation time of the proposed circuit is because the balancing current can be up to the full load current of the traction converter, without the limitations of the low-power balancing circuits of standard BMSs (equal to 6 A for the circuit in [108]). In the proposed converter, the circulating current can be designed according to the desired recharge current of the battery cells and the equalising time. Fig. 6.27 shows that the proposed controller equalises the SOCs of all battery cells without affecting the load voltages and currents [77].

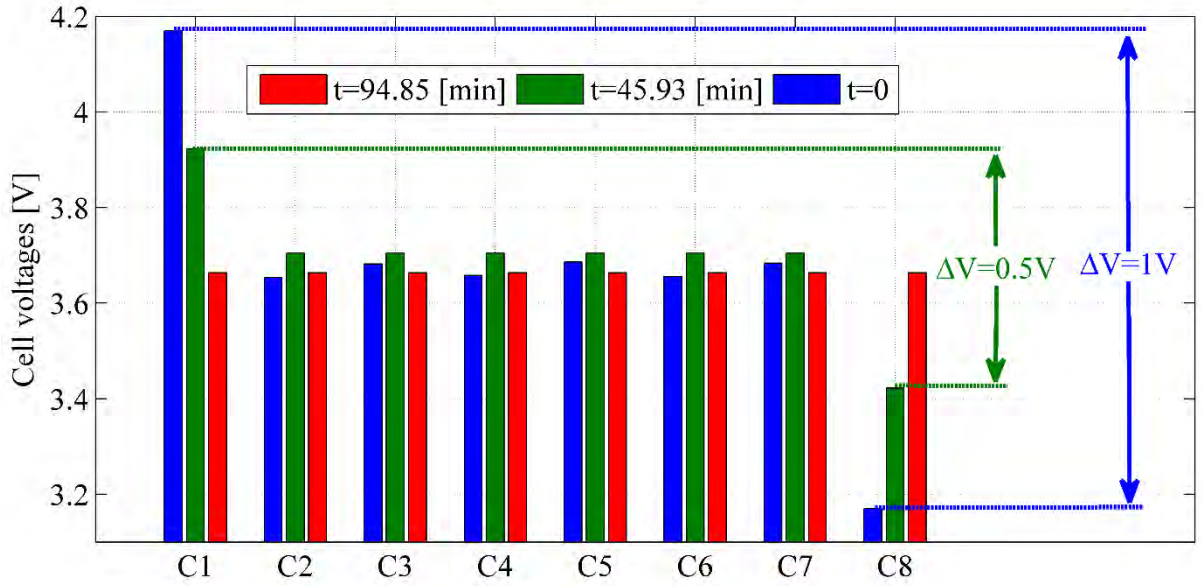


Fig. 6.26: Measured cell voltages at balancing time=0, 46 min and 95 min [77].

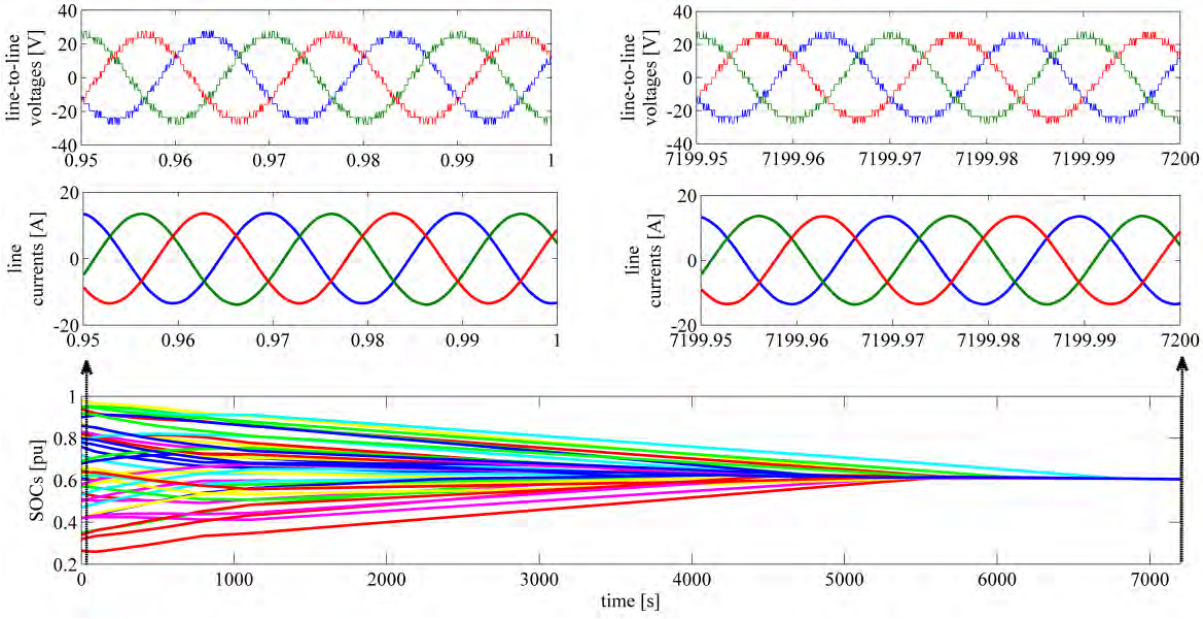


Fig. 6.27: SOCs of 48 cells, transient and steady state load voltages and currents [77].

It is worth to note that the high-frequency pulsed currents in battery cells, during either charging or discharging the cells, are not useful for the power transfer and can affect the lifetime of battery cells. However, the effect of high-frequency pulsed currents is similar for

both two-level inverters and MMCs. For two-level inverters, the situation is even worse, because the switching frequency is much higher than that of MMCs. The analysis of ageing effects of pulsed current involves different ageing phenomena such as:

- Movement of additional electric charge;
- Increase of the operating temperature;
- Variation of the operating voltage.

Some of the authors are currently studying ageing phenomena of lithium batteries [111], but the analysis is complex and there is still a significant gap on this subject in the technical literature. On the other hand, the proposed MMC has 84 SMs per each arm to generate a maximum line voltage of 220 V rms as explained in the simulation part. Therefore, the THD of the converter output voltages is very small (THD < 1 %) even if the SMs are switched at low value of maximum switching frequency. Therefore, the carrier frequency can be set to equal the motor electric frequency in order to eliminate the effect of the high-frequency pulsed currents in battery cells.

In summary, a set of simulation studies in the Matlab/ Simulink environment are presented in this chapter to confirm the validity of the converter control strategy as well as the theory developed. The simulation includes results for static and dynamic load and the recharge of the battery cells from the grid, using a model of a commercially available city car. The simulation results demonstrate that the proposed MMC can effectively provide SOC balancing for the cells under both steady and dynamic operating state. The chapter has also demonstrated that the proposed converter can effectively ensure the balance of cells during the recharge, even in the worst case scenario where an inhomogeneous distribution of the state of charge is assumed as initial condition.

Chapter 7

Prototype Design of MMC for Traction Drives

This chapter describes the design of all the hardware and software components of the proposed MMC and the practical implementation of a small-scale laboratory prototype with four sub-modules per arm.

7.1 Hardware components of the MMC

7.1.1 MosFETs

MosFETs are the devices of choice for low voltage applications due to their low on-state losses, fast switching speeds and high gate impedance. For a gate voltage below the threshold value, typically in a range of 2-4 V, MosFETs are completely off. Above the threshold value, the drain current depends on the gate voltage and the rated value is obtained when the gate voltage reaches approximately 15 V. The internal capacitances of MosFETs affect the turn-on and turn-off times, but they have no effect at steady-state [112], [113]. Two power MosFETs with a part number of IRF1324S-7PPbF, manufactured by International Rectifier, are used for the experimental implementation of each SM power circuit.

7.1.2 Gate drivers

A gate driver circuit has to be designed to drive the MosFETs according to the required switching times [114] and it is shown in Fig. 7.1. The function of gate drive is to supply/sink a current sufficient to charge/discharge the MosFET input capacitor. In order to achieve switching speeds of 100 ns or less, the gate drive circuit has a low-output impedance and capability to supply/sink relatively large currents [114].

The drive circuit is shown in Fig. 7.1 and generates two pulse signals, $v_{\text{drive},a}$ and $v_{\text{drive},m}$ to drive one SM of the MMC. The pulse signals are shifted to respect the switching sequence of the SM. The dead time between the two pulse signals is generated by the gate drive to avoid any short circuit across the battery cell. Since both logic pulse signals have a common terminal, c, the control signal $v_{drive,a}$ needs to be referenced to the potential V_o at the source terminal of MosFET S_a. This implies that $v_{drive,a}$ has to be shifted by V_o. Therefore, there is a need for isolating the pulse signals with interface circuits between the logic circuit and the MosFETs in order to achieve the appropriate level shifting. In a MMC, also the MosFET S_m cannot be gated without isolation because of the multiple series connected SMs [113]. This can be done by adding isolated DC-DC converters to the drive circuit as shown in Fig. 7.1. A gate drive with a part number of L6384, manufactured by STMicroelectronics, is used for the experimental implementation of each SM drive circuit and two isolated DC-DC converters with a part numbers of ISF0515A, manufactured by XP Power, are added to the drive circuit.

7.1.3 Optocouplers

An optocoupler is used to interface the logic circuit with the MosFET gate terminals in order to obtain the required level shifting. It combines an infrared light-emitting diode (ILED) and a silicon phototransistor. The input signal is applied to the ILED and the output is taken from the

phototransistor. The typical rise and fall times of phototransistors are 2-5 μs. The phototransistors require a separate power supply that increases the complexity, cost, and weight of the drive circuits [113]. Two optocouplers with a part number of FOD3180, manufactured by Fairchild Semiconductor, are used for the experimental implementation of each SM drive circuit.

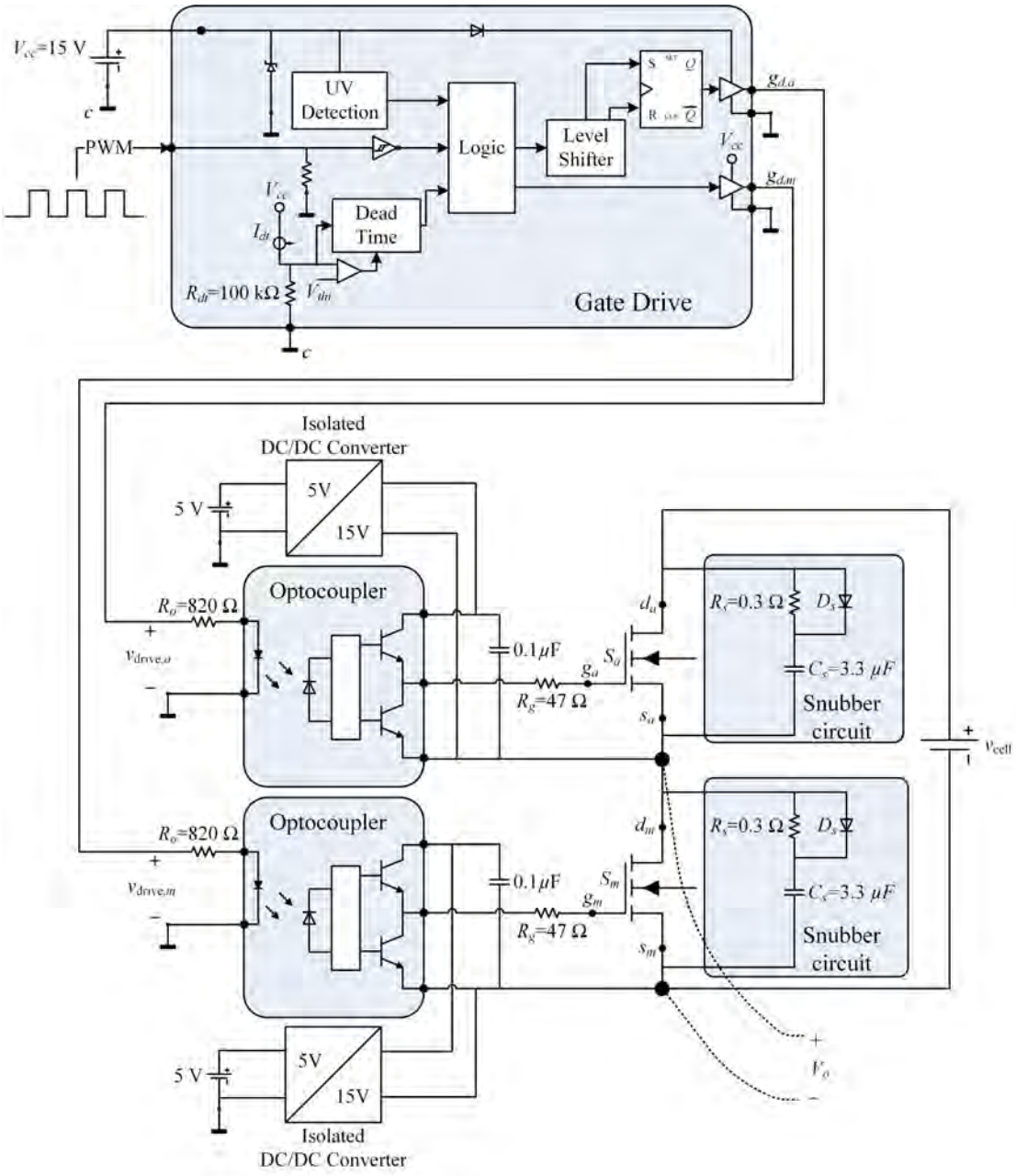


Fig. 7.1: Layout of one SM and its drive circuit.

7.1.4 *RC*-Snubber circuit

The function of the snubber circuit is to limit the *dv/dt* across the devices to reduce the switching losses [113]. Fig. 7.1 shows the turn-off snubber circuit, consisting of a capacitor, a diode, and a resistor connected across the drain and source terminals of the MosFET. At the device turn-off, the current is diverted into the snubber capacitor C_s through the diode D_s. The device voltage is clamped to the capacitor voltage, which is initially zero. The larger the capacitor, the slower the rise of the device voltage for a given load current.

Fig. 7.2 (a) shows the turn-off device voltage v_{sw} and current i_{sw}, where it has been assumed that the voltage rise time is short compared with the current fall time, given by the following equation [115]:

$$i_{sw} = i_m (1 - t / t_{fi}). \tag{7.1}$$

Fig. 7.2 (b) shows the turn-off switch voltage for different values of snubber capacitance. The MosFET tail current has been neglected. For low capacitance values, the snubber capacitor may charge to v_{cell} before the drain current has fallen to zero. For larger capacitance, the drain current reaches zero before the capacitor has charged to v_{cell} [115].

For analysis, the voltage rise time for an unaided switch is assumed zero. The device switch-off energy losses without a snubber, as shown in Fig. 7.2 (a), are given by [115].

$$E = \frac{1}{2} v_{\text{cell}} i_m t_{fi}. \tag{7.2}$$

When a snubber circuit is used, switching losses decrease as shown in Fig. 7.2 (c), but snubber losses increase. After the turn-off, the capacitor is charged to the cell voltage v_{cell}. The energy stored in the capacitor is equal to:

$$E_C = \frac{1}{2} C_s v_{\text{cell}}^2. \tag{7.3}$$

This stored energy is subsequently dissipated across the snubber circuit resistor at the next turn-on of the device [115].

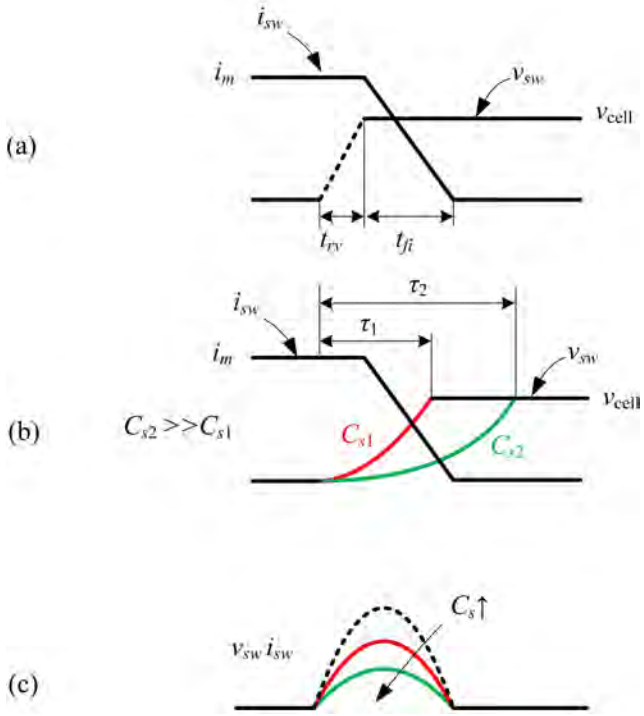


Fig. 7.2: Switch turn-off waveforms: (a) Turn-off without snubber circuit (b) Turn-off with small and large snubber capacitances (c) Switch power losses.

7.1.5 NI CompactRIO

A NI CompactRIO has been used for the measurement, signal processing and control of the converter. The NI CompactRIO is a reconfigurable embedded control and acquisition system. It consists of I/O modules, a reconfigurable field programmable gate array (FPGA) chassis, and an embedded controller. CompactRIO is programmed with NI LabVIEW [116].

Fig. 7.3 shows the block diagram of the control system used for the prototype built for this thesis. The top and bottom arm currents are measured as analogue input signals using the ADC blocks. When the converter is operated as a drive, the motor speed is also measured as analogue

input signal. When instead the converter is used as battery charger, the grid voltages are measured as analogue input signals.

The FPGA unit has the following functions [77]:

- generation of the voltage commands v^*_k;
- generation of the carrier signals with the carrier disposition SPWM technique;
- comparison of v^*_k with the corresponding triangular carrier signals to determine the number of active SMs;
- perform the SOC balancing control algorithm.

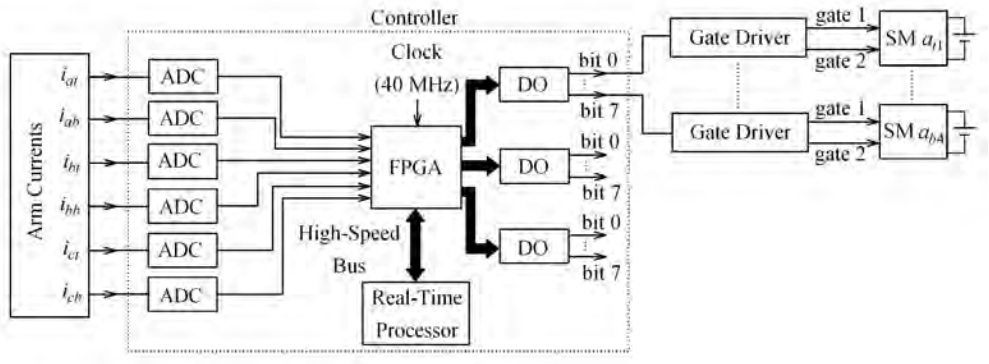


Fig. 7.3: Control system used for the experiments.

7.2 Design of support circuitry and the buffer inductors

7.2.1 Gate resistor design

The gate resistor R_g has been designed from the specification of the low peak value of the optocoupler output current and the MosFET. Assuming ideal voltage from the optocoupler, the gate resistance must satisfy the following inequality:

$$R_g \geq \frac{V_{cc} - V_{OL}}{I_{OL}}, \tag{7.4}$$

where I_{OL} is the low peak value of the optocoupler output current, V_{cc} is the supply voltage and V_{OL} is low level value of the optocoupler output voltage. From the datasheet of the optocoupler it is V_{cc} = 15 V, V_{OL} = 1 V, and I_{OL} = 0.4 A, leading to a gate resistance:

$$R_g = \frac{15-1}{0.4} = 35\,\Omega \Rightarrow R_g = 47\,\Omega. \tag{7.5}$$

7.2.2 Optocoupler input resistor design

In order to limit the optocoupler input current, a resistor R_o must be added between the logic driver and the optocoupler. According to the datasheet of the optocoupler, the maximum average input current $I_{\max}$ of the optocoupler is 20 mA. To protect the optocoupler, 90 % of $I_{\max}$ has been considered for the design of R_o and hence:

$$R_o = \frac{V_{\text{drive,max}}}{I_{\max}}, \tag{7.6}$$

where $V_{\text{drive,max}}$ is the maximum average output voltage of the logic driver circuit, which can be calculated as:

$$V_{\text{drive,max}} = \delta_{\max} V_{DH}, \tag{7.7}$$

being $\delta_{\max}$ is the maximum duty cycle and V_{DH} is the high peak output voltage from logic driver circuit. From the datasheet of the gate driver, V_{DH} = 15 V and $\delta_{\max}$ = 95 %. By substituting these values into (7.7), the value of $V_{\text{drive, max}}$ is 14.25 V and R_o is:

$$R_o = \frac{14.25}{0.018} = 792\,\Omega \Rightarrow R_o = 820\,\Omega. \tag{7.8}$$

7.2.3 Snubber circuit design

The snubber circuit can be designed using the capacitor characteristic equation:

$$i_{sw} = C_s \frac{dv_{sw}}{dt} = C_s \frac{v_{\text{cell}}}{t_{fi}}. \tag{7.9}$$

Each arm of the converter is designed to carry a maximum current of 25 A. Therefore, the device current is assumed to be 25 A and the turn-off linear current time has been measured without considering the snubber circuit (t_{fi} = 400 ns). Substitution these values in (7.10), the snubber capacitance is calculated as:

$$C_s = (25\text{ A})(400\text{ ns})/(3.7\text{ V}) = 2.703\,\mu\text{F} \Rightarrow C_s = 3.3\,\mu\text{F}. \tag{7.10}$$

The snubber capacitor is discharged at switch turn-on and must be discharged within the switch minimum on-time, $t_{on,\min}$. This means that the time constant of the *RC*-snubber circuit must be much smaller than $t_{on,\min}$.

$$R_s C_s <<< t_{on,\min}. \tag{7.11}$$

Assuming a minimum duty cycle of 5% ($\delta_{\min}$ = 5%.), a maximum switching frequency of 10 kHz and considering that the value of $t_{on,\min}$ is approximately five times R_sC_s, the snubber resistance is:

$$t_{on,\min} = \frac{\delta_{\min}}{f_{sw}} = 5R_sC_s \Rightarrow \frac{0.05}{10000} = 5R_s(3.3\times10^{-6}) \Rightarrow R_s = 0.3\,\Omega. \tag{7.12}$$

The discharge resistor power rating, $P_{0.3\Omega}$, is independent on the resistance and it is given by:

$$P_{0\,3\Omega} = \frac{1}{2}C_s v_{cell}^2 f_{sw} = \frac{1}{2}(3.3\,\mu\text{F})(3.7)^2(10\text{ kHz}) = 225.885\text{ mW}. \tag{7.13}$$

7.2.4 Design of the buffer inductors

The buffer inductors have the functions to absorb the instantaneous voltage difference between the converter arms and filter the circulating currents. The current flowing through an arm inductor is equal to the arm current. Therefore, the steady-state magnitude of the voltage drop across the inductor $|\Delta v_L|$ can be calculated as:

$$|\Delta v_L| = \omega L |I_{\text{arm}}|, \tag{7.14}$$

where $|I_{\text{arm}}|$ is the steady state magnitude of the arm current, which depends on the peak of both load current and the injected circulating current during cell balancing. The maximum value of the steady state magnitude of the arm current, $|I_{\text{arm}}|_{\max}$, can be calculated as:

$$\left|I_{\text{arm}}\right|_{\max} = \frac{1}{2} I_{mn} + I_{cir,1,\max}, \tag{7.15}$$

where I_{mn} is the nominal peak value of the load current ($I_{mn} = \sqrt{2} \times 50$ A) and $I_{cir,1,\max}$ is the maximum peak value of the injected circulating current during cell balancing, which has been set to 5% of I_{mn}. With these assumptions, the maximum steady-state magnitude of the voltage drop across the inductor, $|\Delta v_L|_{\max}$, is equal to:

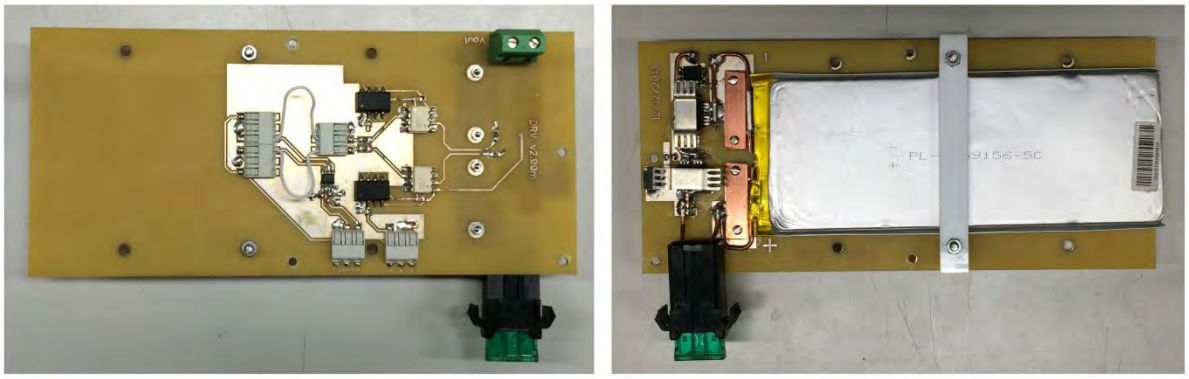
$$\left|\Delta v_L\right|_{\max} = \omega L \left|I_{\text{arm}}\right|_{\max} = 0.55\,\omega L\, I_{mn}. \tag{7.16}$$

Assuming that this voltage drop is 8% of the nominal peak value of the load voltage V_{mn} and that the maximum operating frequency of the converter is two times the nominal motor frequency (2×50 Hz), the buffer inductor is:

$$L \le \frac{8\% \times V_{mn}}{0.55\omega I_{mn}} = \frac{0.08 \times (nV_{cn}/2)}{0.55 \times \omega I_{mn}} = \frac{0.08 \times 7.4}{0.55 \times 2\pi \times 100 \times 50\sqrt{2}} = 24.3\,\mu\text{H} \Rightarrow L = 22\,\mu\text{H}. \tag{7.17}$$

7.3 Circuit implementation

A complete small-scale prototype of the proposed MMC with four sub-modules per arm has been built in the laboratory. The practical design of a complete SM with a Li-ion battery cell, the MosFET based half-bridge and the drive circuit is shown in Fig. 7.4. The complete prototype is shown in Fig. 7.5.



(a) (b)

Fig. 7.4: Experimental implementation of one SM: (a) Drive circuit. (b) Power circuit.

Fig. 7.5: Prototype of a 5-level MMC with embedded lithium-ion batteries.

In summary, this chapter gives an overall review of all the hardware and software components (i.e. MosFETs, gate drives, optocouplers, *RC*-snubber circuits, and NI CompactRIO) of the proposed MMC. The chapter also provides guidelines for the design of the converter support circuitry and the buffer inductor. Finally, it shows the experimental implementation of the small-scale prototype of the proposed MMC with four sub-modules per arm.

Chapter 8

Experimental Results

In this chapter, the simulation work has been experimentally verified with the lab prototype of MMC with 4 SMs per arm. The experimental tests have been focussed on the viability of the proposed converter for traction application, the effectiveness of the cell balancing control and the validation of the power loss model. Finally, the chapter shows experimental results for the recharge control algorithm from the three-phase utility grid at (nearly) unity power.

8.1 Preliminary tests on dead time, level shifting and snubber circuits

The dead time between the output signals of the high voltage and low voltage gate drivers can be set connecting a dead time resistor R_{dt} between pin 3 and pin 4 (ground) of the logic driver, as shown in Fig. 8.1. The value of R_{dt} determines the value of the dead time and the relationship between the value of R_{dt} and the dead time is shown in Fig. 8.1. A dead time resistor of 100 kΩ has been chosen, leading to a dead time of 1 μs, as confirmed by the gate signals shown in Fig. 8.2.

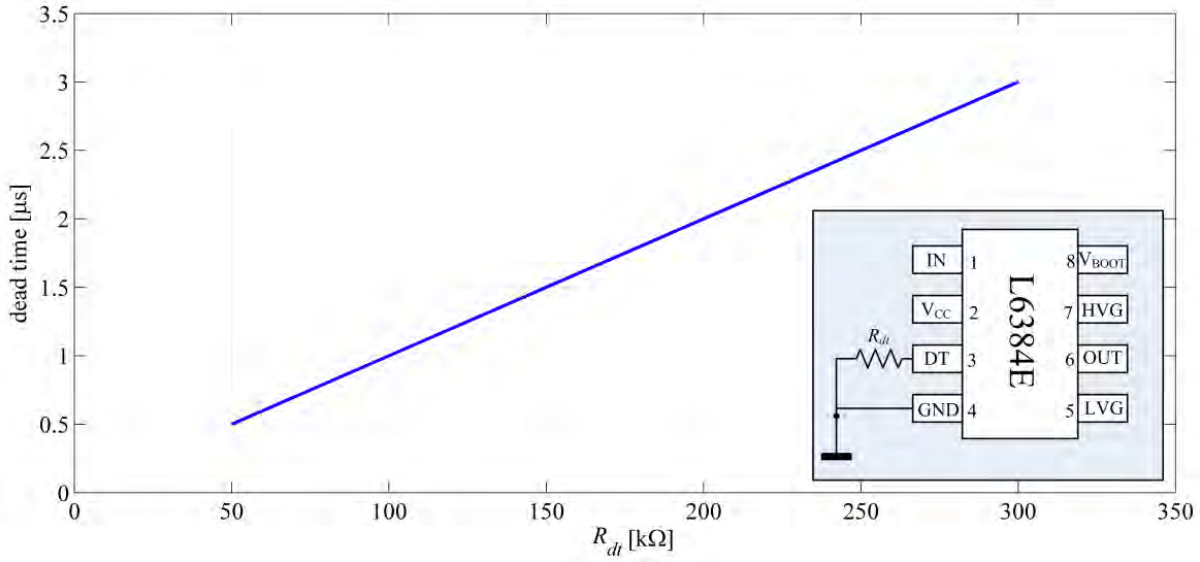


Fig. 8.1: Dead time versus R_{dt} and connection of dead time resistor (inset).

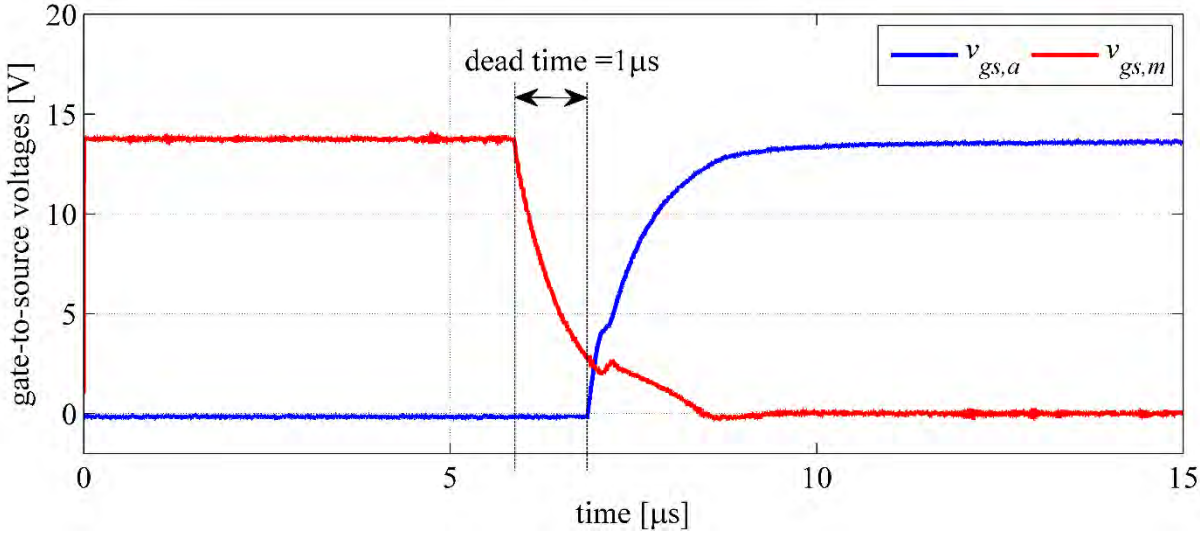


Fig. 8.2: Dead time test.

In order to check the level shifting between the gate signals, both gate signals have been measured with respect to the source terminal of the MosFET S_m and the results are shown in Fig. 8.3. It can be noticed that $v_{g,a}$ is shifted by 3.7 V, which is the SM output voltage. This confirms that the required level shifting and isolation of gate signal with respect to the ground has been obtained by the optocouplers.

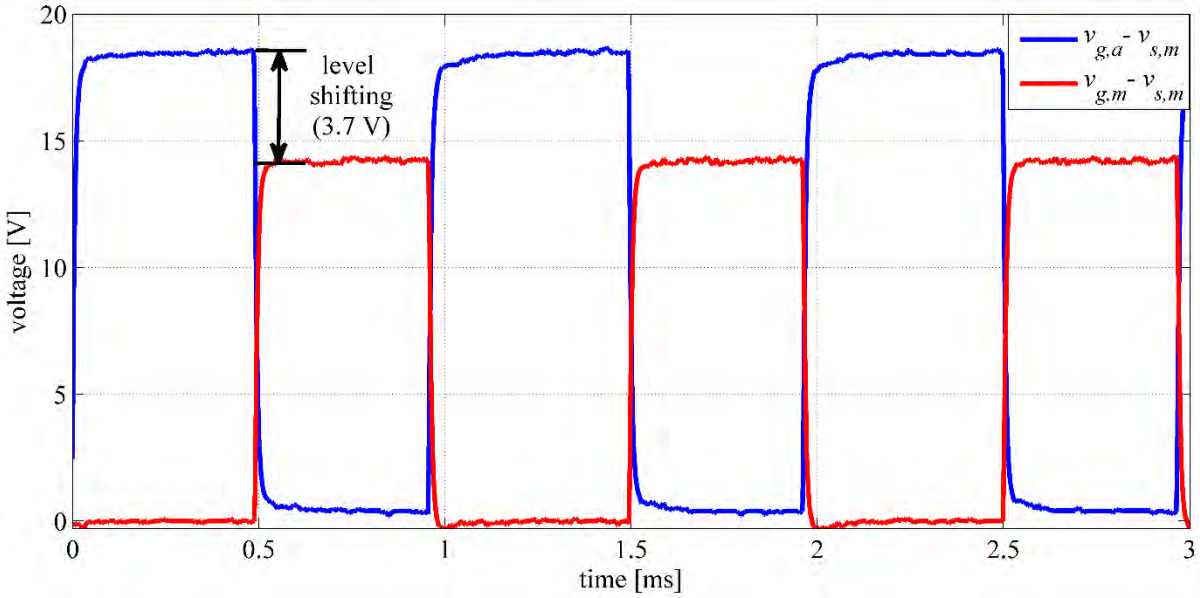


Fig. 8.3: Level shifting test.

Fig. 8.4 illustrates the turn-off voltage, current, and energy associated to a MosFETs in one of the SMs with/without connecting the snubber circuit. It is clear that at the switching instant there is a significant spike and ringing of the voltage across the MosFET when the snubber circuit is not connected. The ringing causes a significant increase of the switching losses and of the electromagnetic interference (EMI) noise, which may affect the normal operation of the SM. In addition, a higher voltage stress requires a higher voltage rating for the MosFET, which results in higher conduction losses due to the higher on-state resistance. On the other hand, it is clear that the snubber circuit eliminates both the spikes and the ringing, with consequent benefits on the reduction of switching losses.

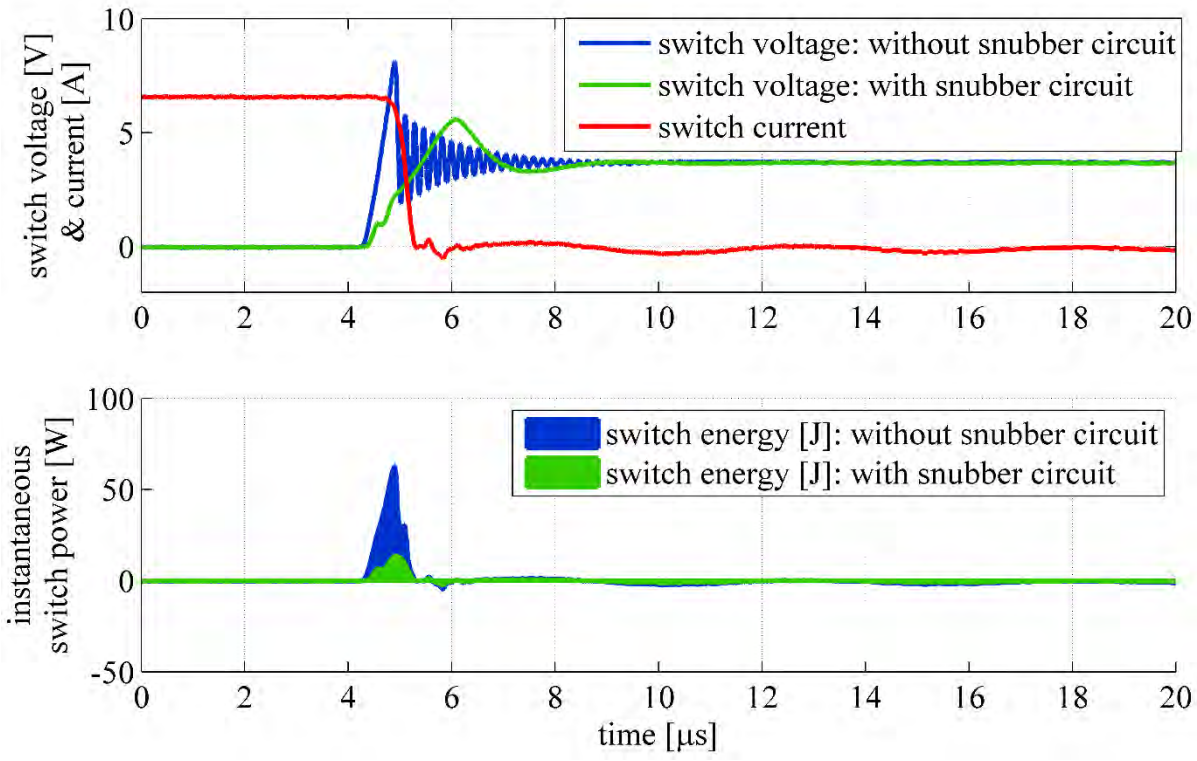


Fig. 8.4: Snubber circuit test. (The area under the instantaneous switch power curve represents the switch energy losses)

8.2 Converter test under no load conditions

The converter is designed to drive a traction motor and, hence, the number of active levels is dependent on the voltage amplitude required at the output terminals. Due to the modular design of the converter, the number of levels can be adjusted by changing the modulation index and the output voltage is regulated through the SPWM of the last level. When a variable frequency is required, this control allows a quick variation of the voltage level in a way completely similar to traditional two-level inverters. In order to verify the experimental response of the converter to a variation of the output voltage and frequency, the tests have been made with a Volt/Hertz constant control at four modulation indices and frequencies with a constant modulation frequency ratio of 21. The experimental tests have also been compared

with the simulations. Fig. 8.5 shows both simulated and experimental line-to-line voltages for the different output frequencies and voltages: The larger the number of levels, the smaller THD of output voltage. Table 8.1 compares the results between the simulation and the experiment based on the THD and the peak value of the fundamental component, $V_{1,peak}$. Both results show a close agreement and highlight the small distortion of the voltage generated by the proposed MMC. Therefore, it is expected that the losses of the traction motor are also significantly reduced. In order to quantify the improvement of motor efficiency with a higher number of levels, a simulation has been carried out supplying the induction motor with the same voltage amplitude and frequency and with the same output torque. The result is shown in Fig. 8.6 where it is evident that an increment of the efficiency of about 0.8% has to be expected, with a significant impact on the driving efficiency of the battery EV [77]. It is worth noting that the motor core losses (eddy currents and hysteresis losses) have not been included when the machine efficiency has been calculated.

Table 8.1: The THDs of line-to-line voltages [77].

			practical results		simulation results	
m	f	n-level	THD[%]	$V_{1,peak}$ [V]	THD[%]	$V_{1,peak}$ [V]
0.25	12.5	2	70.49	3.221	68.57	3.213
0.5	25	3	37.72	6.420	35.35	6.417
0.75	37.5	4	23.37	9.866	23.33	9.592
1	50	5	17.28	13.200	17.08	12.840

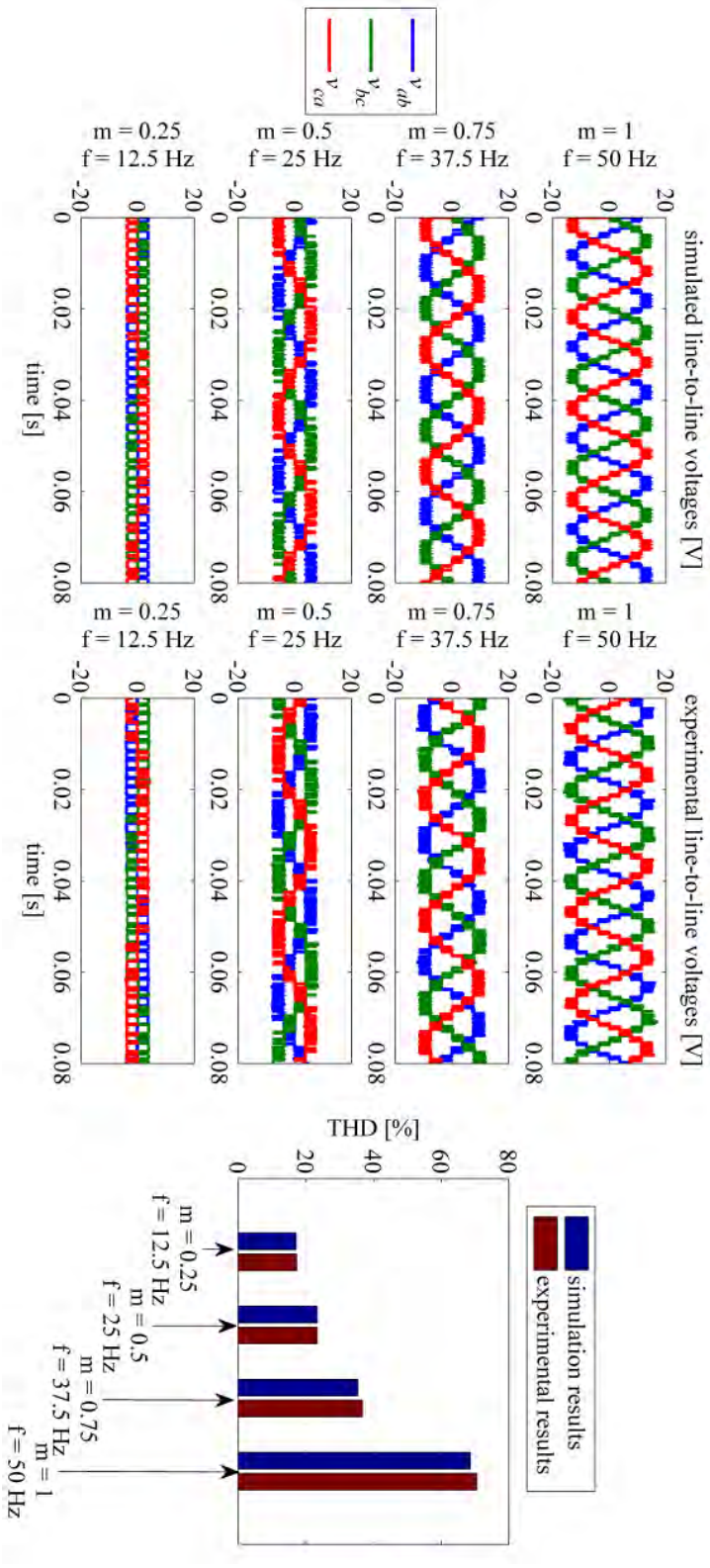


Fig. 8.5: Line-to-line voltage waveforms [77].

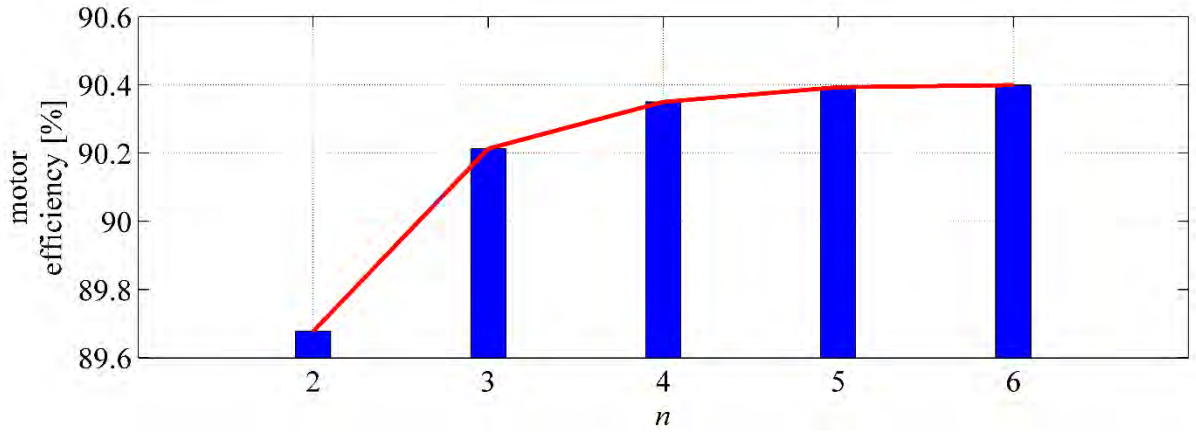


Fig. 8.6: Motor efficiency for different number of converter levels. Note: in all conditions the motor power is 4 kW, the voltage is 400 V, the frequency is 50 Hz, the speed is 1430 rpm [77].

8.3 Experimental tests with a static load

8.3.1 Resistive load

The MMC prototype has been operated with a static resistive load to verify the effectiveness of cell balancing. In this experiment, the converter is controlled using SPWM with a 1.05 kHz switching frequency. Table 8.2 summarises the circuit parameters used for this experiment. For comparison purposes, numerical simulations have been carried out based on the circuit parameters used for the experiments.

Fig. 8.7 shows both simulated and experimental waveforms of the load voltages and currents that confirm the correct operations of the converter. The figures also show that, although the MMC has only four cells per arm, the distortion of the current is small even for a resistive load, as predicted by the simulations.

To demonstrate the correct operations of the SOC balancing algorithm, the 24 Li-ion cells have been initially charged to different SOC values with a maximum SOC unbalancing of around 4.5%. The SOC of each cell has been estimated by using Coulomb counting method according to equation (3.14). The result in Fig. 8.8 shows a good agreement between simulated and experimental SOCs of all the battery cells. With the proposed controller, the SOCs of battery cells converge toward the same level and are balanced after about 1200 seconds.

Table 8.2: Circuit parameters used for experiment.

Load active power	P	0.9 kW
Load power factor	cosφ	1.0
Nominal line-line rms voltage	V_n	10 V
Nominal rms current	I_n	50 A
Nominal frequency	f_n	50 Hz
Arm inductor	L	22 µH
Nominal battery capacity	Q	10 Ah
Nominal battery voltage	V_{cn}	3.7 V
Switching frequency	f_s	1.05 kHz
Number of cells per each arm	n	4

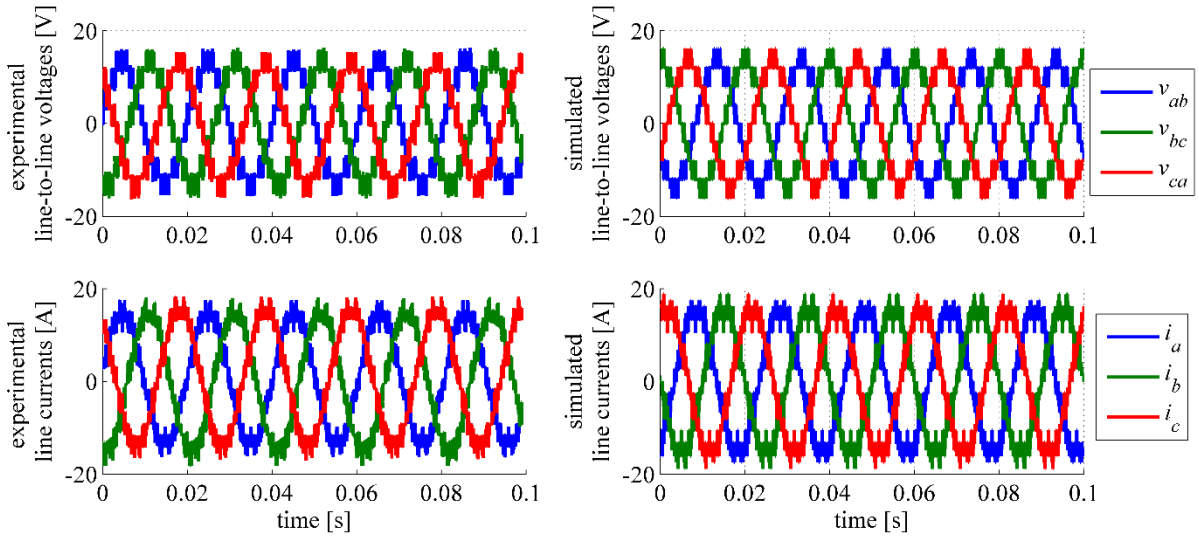


Fig. 8.7: Load voltages and currents

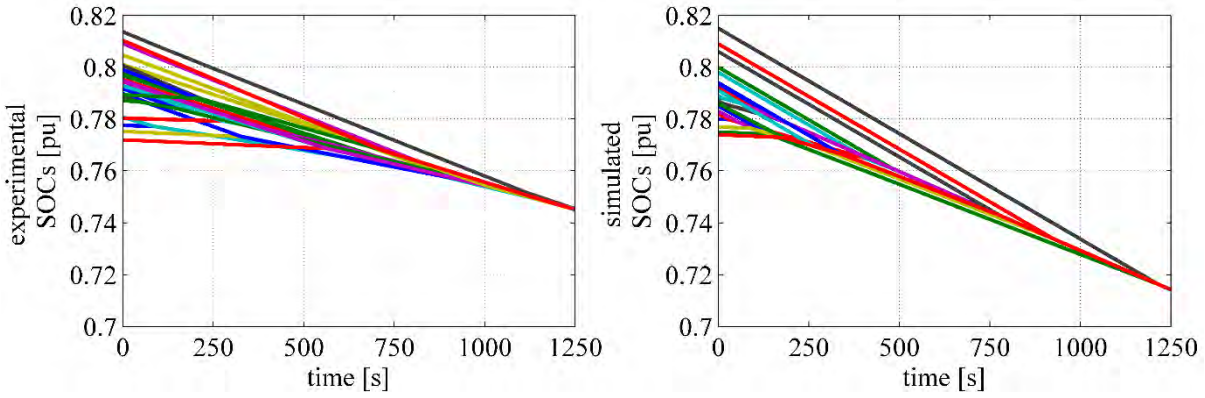


Fig. 8.8: Experimental and simulated SOCs of the battery cells of the proposed MMC.

8.4 Experimental tests with an induction motor

The MMC has been experimentally tested with an induction motor, whose data are given in Table 8.3. A 10V/400V, 1.2 kVA three-phase transformer has been used to boost the converter voltage to the level suitable for the motor. Table 8.4 summarises the circuit and battery parameters used for experiment. Fig. 8.9 shows the experimental implementation of the proposed converter driving the induction motor.

Table 8.3: Main characteristic of the induction motor.

Nominal power	Nominal voltage	Nominal motor current	Pole Pairs	Nominal Speed	Connection	Machine class
0.55 kW	400 V	1.34 A	2	1435 rpm	Y	B

Table 8.4: converter parameters used for experiment (dynamic load test).

Nominal battery capacity	Nominal battery voltage	Nominal converter current	Arm inductor	Switching frequency
10 Ah	3.7 V	50 A	22 µH	1.05 kHz

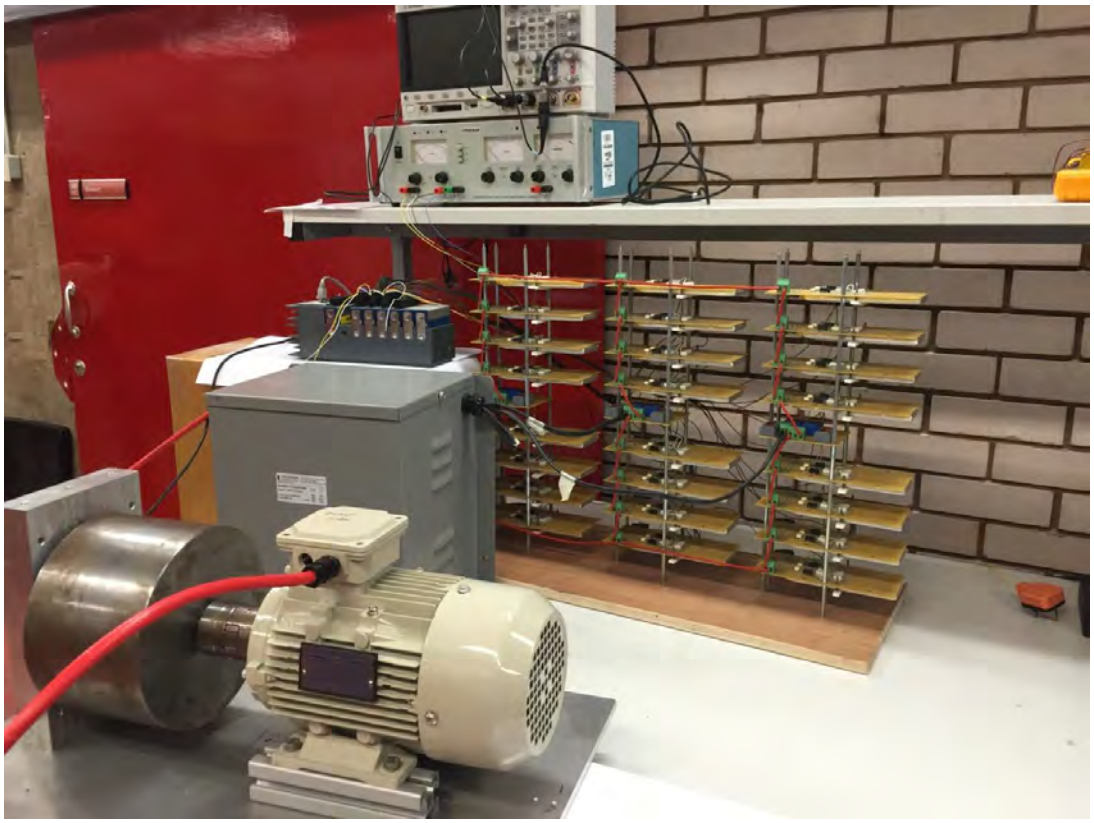


Fig. 8.9: Prototype of the 5-level MMC with embedded lithium-ion batteries driving a three-phase induction motor.

8.4.1 Estimation of the induction motor parameters

The induction motor parameters have been estimated using the typical tests based on dc measurements, no-load and locked rotor conditions. Table 8.5 summarises the results of the three tests.

Table 8.5: the results of DC, no-load and locked rotor conditions.

	Voltage [V]	Current [A]	Power factor angle [deg]
DC-test	23.288	1.34	-
locked rotor test	73.1	1.34	69
no-load test	400	0.82	-

In the dc-test, two terminals of the motor stator windings are connected to a variable dc power supply. The current is increased up to the nominal value and then the voltage across the windings is measured. The stator resistance is then calculated as:

$$R_s = \frac{V_{dc}}{2I_{dc}} = \frac{23.288}{2 \times 1.348} = 8.64\,\Omega. \tag{8.1}$$

The value of R_s needs to be referred to a frequency of 50 Hz considering the skin effect and the conventional temperature of 75 °C.

In the locked rotor test, a variable three-phase voltage source supplies the stator windings until the nominal current is reached. The values that are measured during this test are the voltage and the power factor. In this case, the magnitude of the sum of the stator and rotor impedances, $|Z_{\text{eq}}|$, is calculated as:

$$\left|Z_{\text{eq}}\right| = \frac{98}{1.34\sqrt{3}} = 42.29\,\Omega, \tag{8.2}$$

and the sum of the stator and rotor resistances and reactances, R_{eq} and X_{eq}, are calculated as:

$$R_{eq} = R_s + R'_r = \left|Z_{eq}\right|\cos(\varphi) = 42.3\cos(69°) = 15.15\,\Omega; \tag{8.3}$$

where φ is the measured power factor angle. With this information, the rotor resistance referred to the stator windings is determined since the stator resistance has been already estimated by (8.1). Neglecting the skin effect and using the dc resistance test, the value of R'_r is calculated as:

$$\begin{aligned} R'_r &= R_{eq} - R_s \\ &= 15.15 - 8.63798 = 6.52\,\Omega. \end{aligned} \tag{8.4}$$

The sum of the stator and rotor reactances, X_{eq}, is calculated as shown below:

$$\begin{aligned} X_{eq} &= X_s + X'_r = \left|Z_{eq}\right|\sin(\varphi) \\ &= 42.3\sin(69°) = 39.48\,\Omega, \end{aligned} \tag{8.5}$$

where X_s is the total leakage reactance of stator windings and X'_r is the total leakage reactance of rotor windings referred to the stator phase winding.

Since the machine class is B type, the relation between X_s and X'_r is given by the national electrical manufacturers association (NEMA) as:

$$X_s = \frac{2}{3} X'_r. \tag{8.6}$$

Solving (8.5) and (8.6) yields:

$$X_s = 15.79\,\Omega; \quad X'_r = 23.69\,\Omega. \tag{8.7}$$

In the no-load test a three-phase source supplies nominal voltage to the stator windings at the motor nominal frequency and the machine rotates without any load close to synchronous speed. The current is measured during this test. Neglecting the equivalent resistance representing the losses due to eddy current and hysteresis, the sum of the magnetising and stator reactances, X_{nl}, is calculated as:

$$X_{nl} = X_m + X_s = \frac{V_{nl}}{I_{nl}} = \frac{400}{\sqrt{3} \times 0.82} = 278.11\,\Omega, \tag{8.8}$$

where V_{nl} and I_{nl} are the measured voltage and current under no-load conditions, respectively, and X_m is the machine self-reactance. With this equation X_m can be determined, since the stator reactance has been already calculated in (8.7) using the locked rotor test. The value of X_m is calculated as:

$$\begin{aligned} X_m &= X_{nl} - X_s \\ &= 278.1 - 15.8 = 262.32\,\Omega. \end{aligned} \tag{8.9}$$

Table 8.6 summarises the estimated induction motor parameters referred to 50 Hz considering the skin effect and the conventional temperature of 75 °C. The motor inductances are calculated from the estimated reactances dividing by the radian frequency.

Table 8.6: Induction motor parameters for experiment.

R_s	L_s	R'_r	L'_r	L_m
8.64 Ω +10 %	50.27 mH	6.52 Ω	75.4 mH	835 mH

8.4.2 Operations at constant speed

The SOC balance capability of the proposed MMC has been validated again when the converter drives the motor, using an initial SOC imbalance of 44%. The motor rotates at nominal speed during the whole SOC balancing time. Fig. 8.10 shows the output voltages and currents at nominal motor speed. It is clear that the MMC produces output currents with a very small THD, due to the filtering effect of the motor. The small imbalance of the current is due to the asymmetry of the windings of the induction motor. Fig. *8.11* shows that the SOCs of all battery cells converge to a common value, validating the SOC balancing strategy even for a large initial imbalance of the cells [77]. Moreover, the converter output voltages and currents have been measured at t = 950 s and t = 1900 s in order to demonstrate that they are not affected by the balancing control.

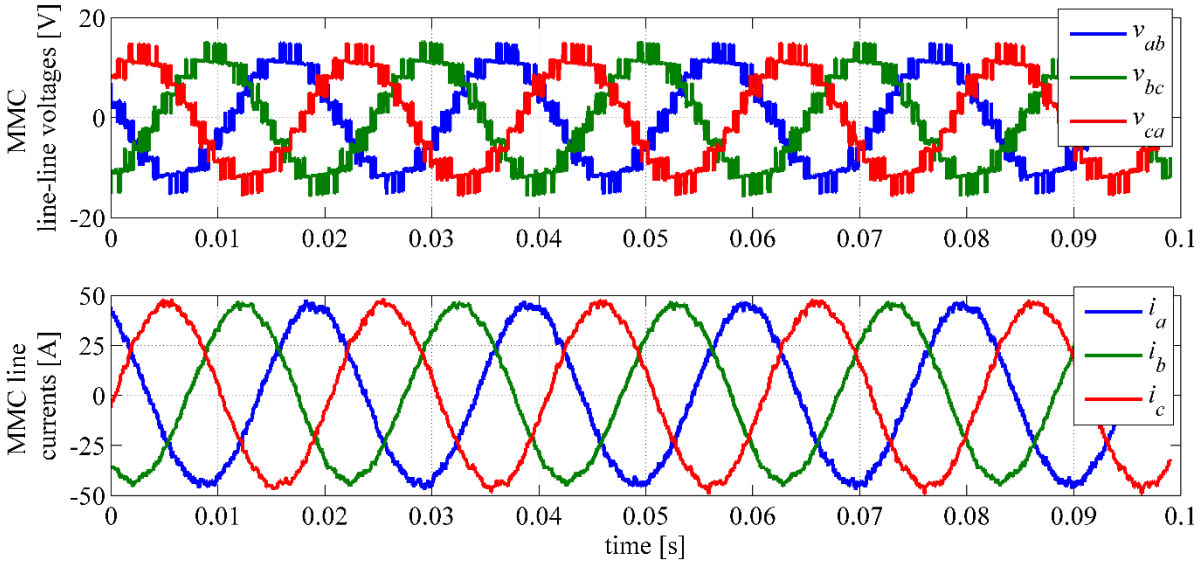


Fig. 8.10: Converter output voltages and currents [77].

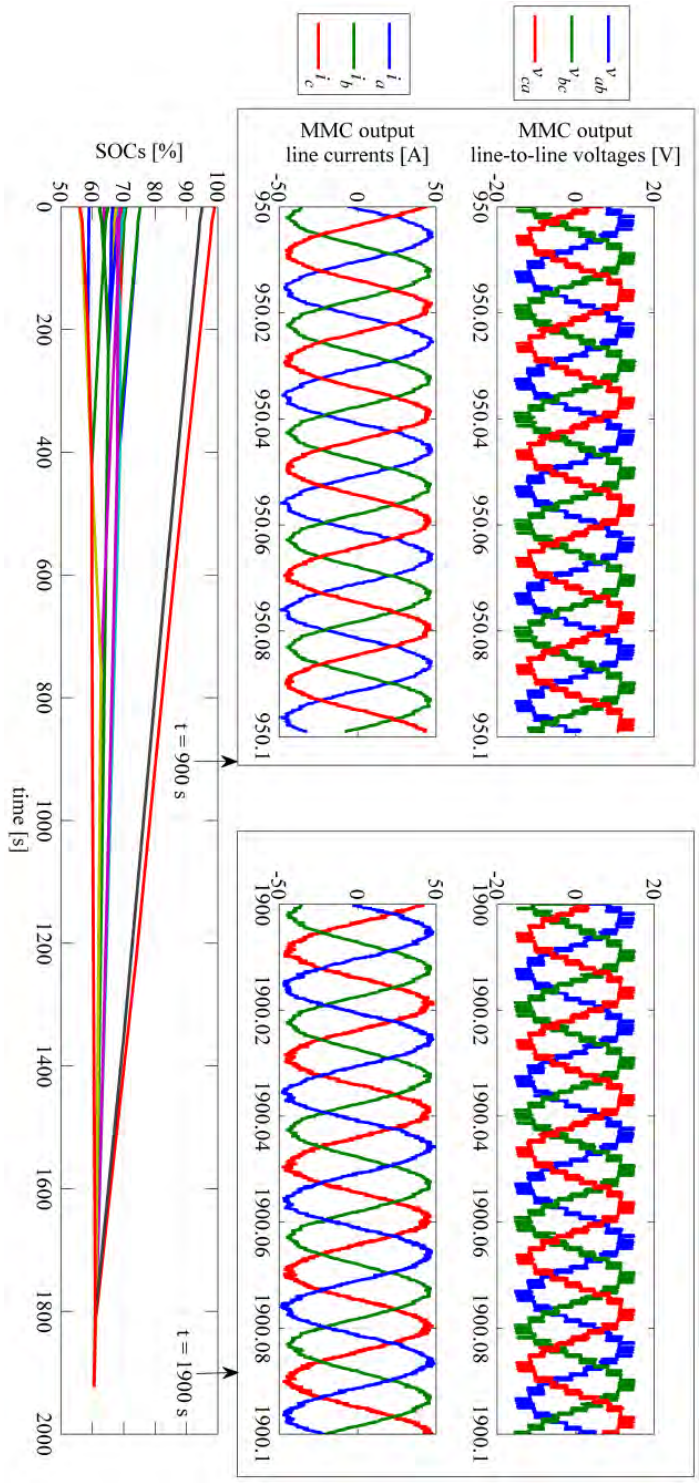


Fig. 8.11: The SOCs of the 24 battery cells, output voltages and currents at 950 s and 1900 s, as taken from [77].

8.4.3 Operations with variable speed

The 24 Li-ion cells have been charged to different initial SOC values in order to test the SOC balancing during a drive cycle of the induction motor. The maximum SOC unbalancing between the cells is around 40% and the NEDC has been used as the reference speed for the induction motor. Table 8.7 summarises the control gains used for experiment and Fig. 8.12 shows the illustration of the 'gear changing' of the switching frequency with the fundamental frequency used for the experiment.

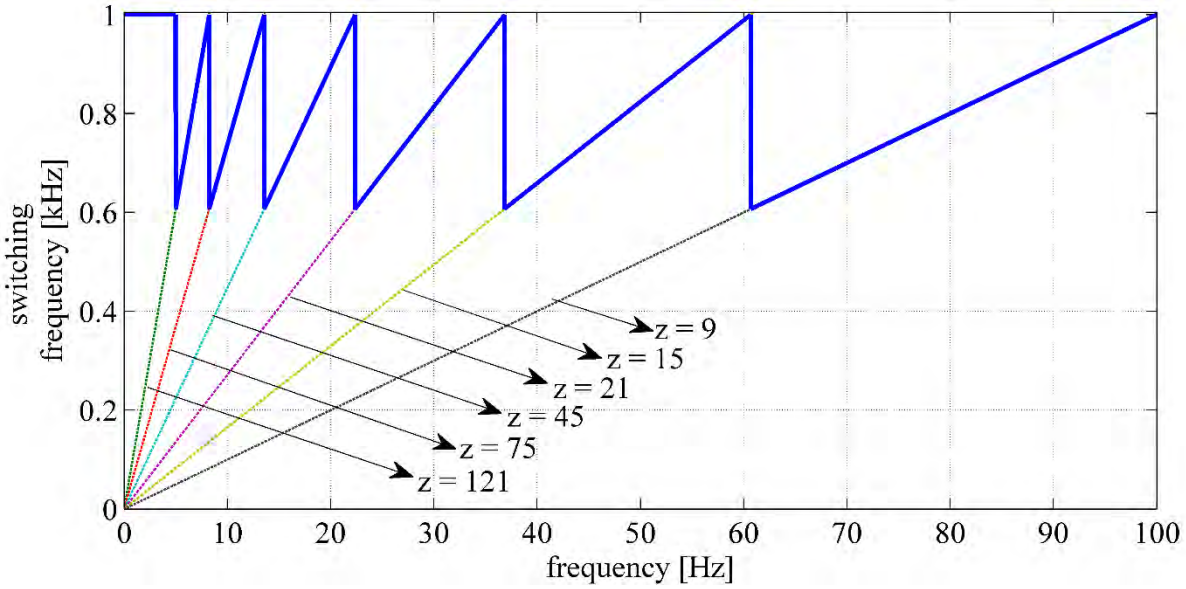


Fig. 8.12: The gear changing used for experiment.

Table 8.7: Control gains used for experiment.

f_n = 0.0004 Hz	Proportional gain of leg-energy control	k_1	6.3978×10^3 A
ζ = 35.3553	Integral gain of leg-energy control	k_2	0.2247 A/(s)
f_n = 0.0002 Hz	Proportional gain of arm-energy control	k_3	-6.3978×10^3 A
ζ = 35.3553	Integral gain of arm-energy control	k_4	-0.1137 A/(s)
T =0.11254 ms	Proportional gain of circulating current control	k_5	0.1955 Ω
f_n = 0.2345Hz	Proportional gain of motor speed control	k_8	0.6572 kg m^2 s
ζ = 4.6942	Integral gain of motor speed control	k_9	0.41264 kg m^2
f_n = 3.2565 Hz	Proportional gain of motor current control	k_{10}	50 Ω
ζ = 40.9229	Integral gain of motor current control	k_{11}	50 Ω s

Note: The relations between the control gains and the closed loop natural frequency f_n, the time constant T, and the damping ratio ζ are given in Appendix C.

The results shown in Fig. 8.13 from the top to the bottom are the motor reference speed and the measured motor speed, the converter output voltage and current measured at different motor speeds during the SOC balancing process, and the SOCs of all the battery cells. It is clear that the SOCs of all the battery cells of the converter converge toward the same level and are balanced after about 2,636 seconds. This result is in agreement with those of the simulation reported in Fig. 6.10, since the nominal current of the prototype is about 5 times smaller than that used for the simulations. The waveforms also confirm that the current is almost sinusoidal for all the operating conditions of the motor.

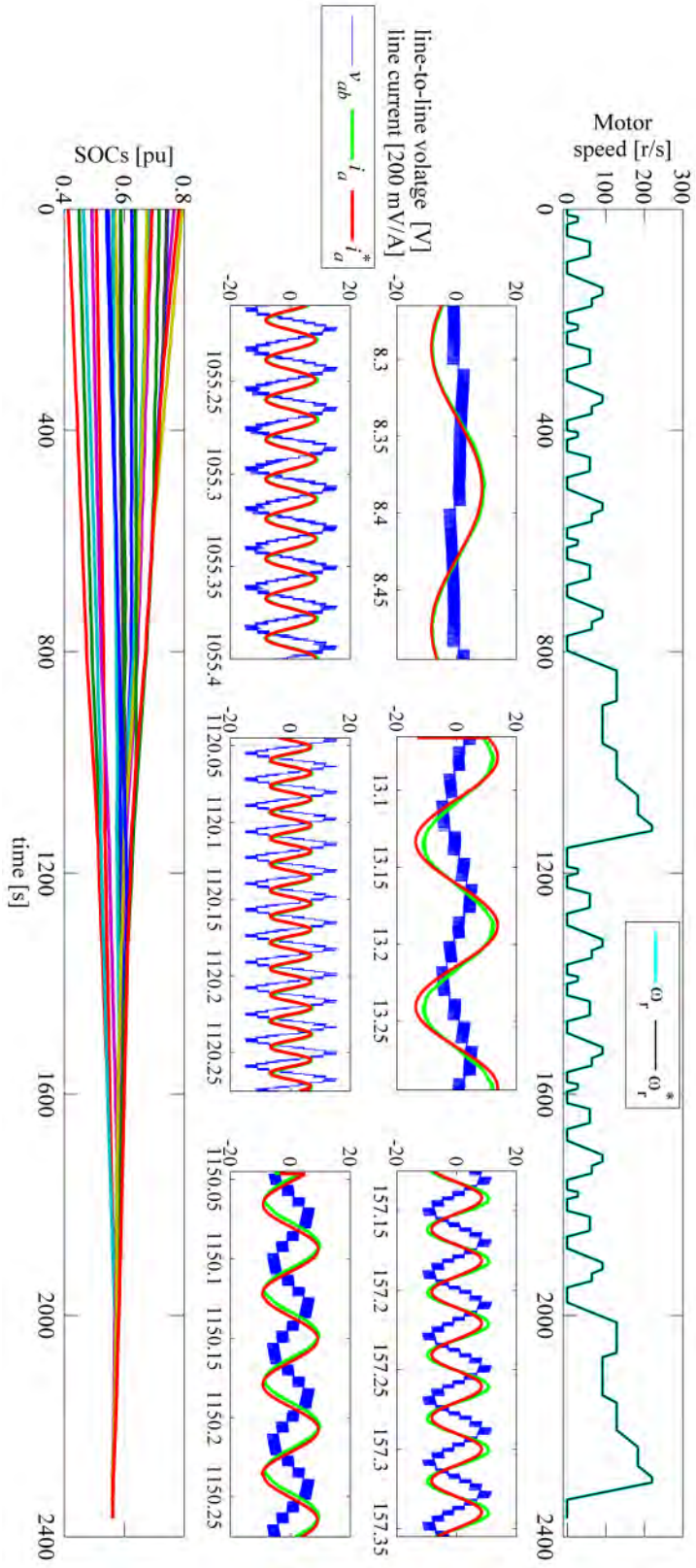


Fig. 8.13: Motor speed, output voltage and current and SOCs of the battery cells [101].

8.4.4 Validation of the loss calculation method

In order to validate the efficiency of the proposed MMC, the switching and conduction losses have been measured for one SM at different motor speeds during the whole NEDC. All cells have been charged to the same initial SOC value. In this case, the estimated efficiency of one SM is approximately equal to the MMC efficiency, since the converter has identical SMs. The drain-source on-state resistance for the power MosFET of the prototype is 0.8 mΩ and its rated drain-source voltage is 20 V while the MosFET current and rise times are 240 ns and 93 ns, respectively [101].

The experimental switching waveforms of one MosFET are presented in Fig. 8.14, where the upper part shows the waveforms of the drain-source voltage and the drain current and the lower part shows the measured losses, with an ideal splitting between switching and conduction losses [101].

Fig. 8.15 shows the converter output line voltage and current, the instantaneous power supplied by one batter cell and the instantaneous power losses of the SM at different motor speeds. The average input power and average power losses of the experiments are summarised in Table 8.8 and compared with the simulations. Both simulated and experimental efficiencies at different motor speeds show a close agreement, although the experimental MMC efficiency is slightly lower than the simulated efficiency by 1-2 % because of the dead time losses, which have not been included in the simulations [101].

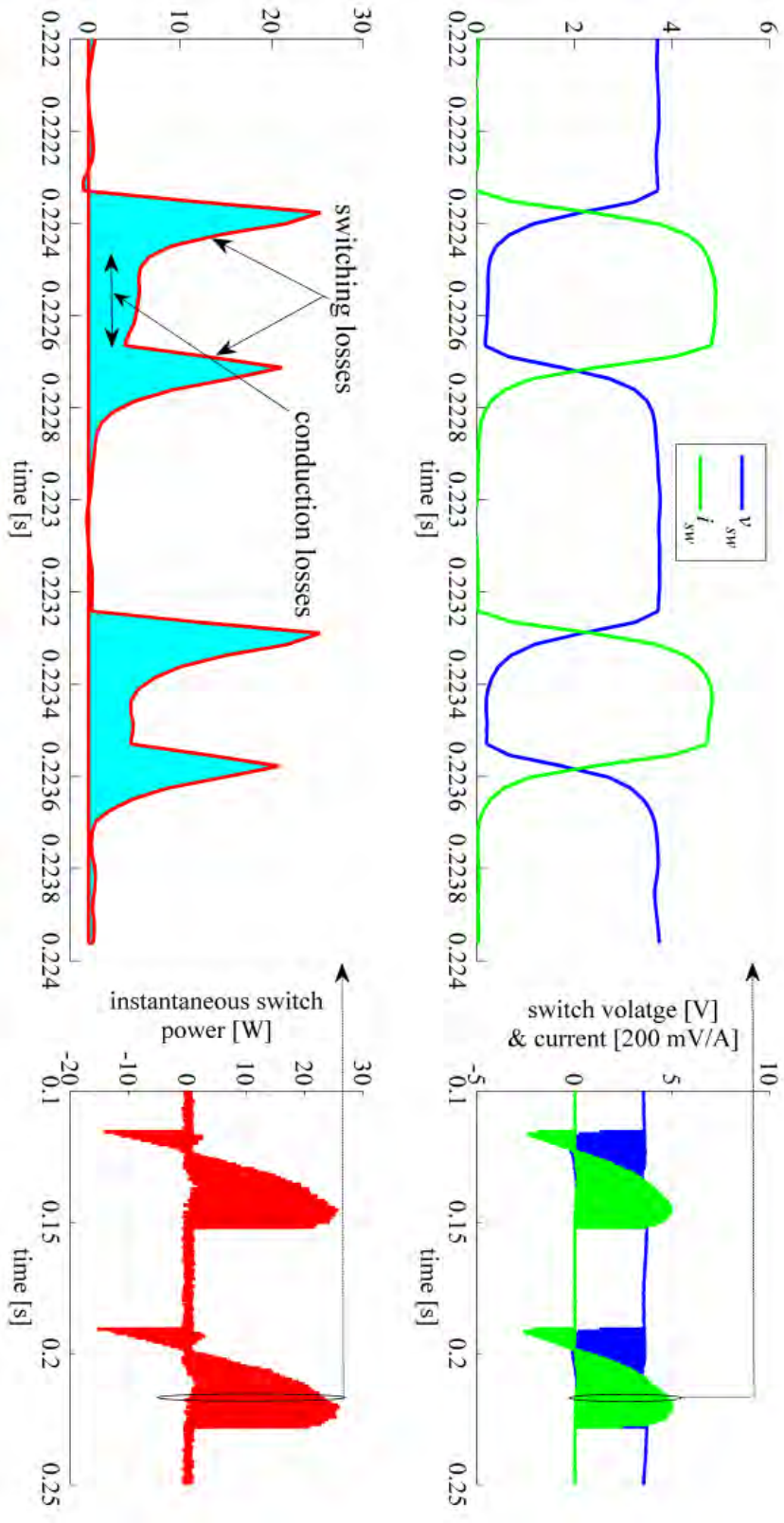


Fig. 8.14: The experimental switching process of one power MosFET [101].

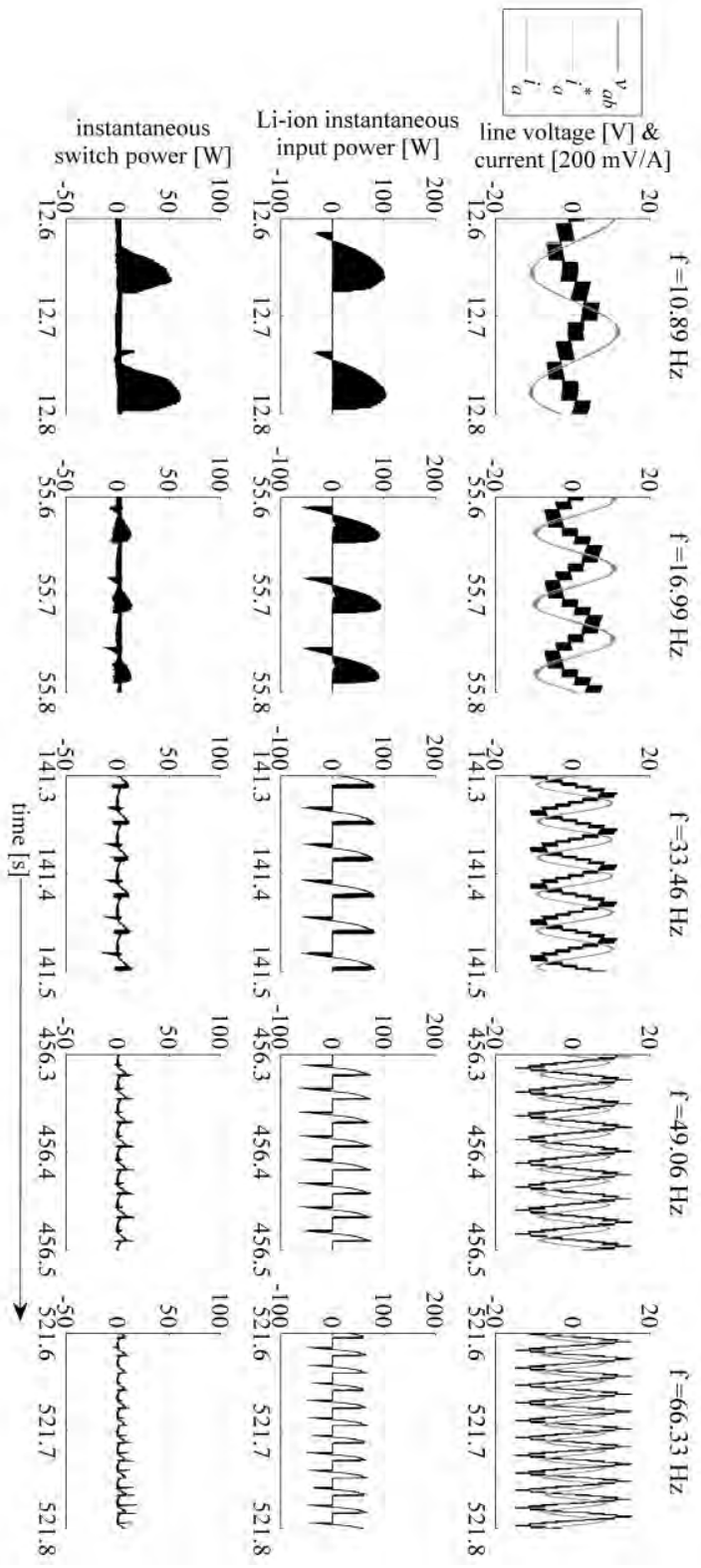


Fig. 8.15: Converter line voltage and current, instantaneous power of a Li-ion cell and instantaneous losses of a SM at different motor speeds [101].

Table 8.8: Average power of a Li-ion cell, average power losses and efficiency of one SM [101].

Electric frequency [Hz]	Average power of a Li-ion cell [W]	Power losses of one SM [W]	Experimental efficiency of the SM [%]	Simulated efficiency of the SM [%]
10.89	19.00	4.19	77.95	78.85
16.99	15.60	2.42	84.49	85.14
32.46	15.33	2.52	83.35	84.98
49.06	12.11	2.32	80.84	82.04
66.23	12.96	2.15	83.41	84.53

8.5 Stationary recharge from a three-phase grid

The recharge of battery cells has been verified connecting the implemented MMC to a 400 V, 50 Hz three-phase grid. A 400 V/10 V, 1.2 kVA three-phase transformer is used to step down the grid voltage to the level suitable for the converter. In this experiment, the converter is controlled using SPWM with a 2.25 kHz switching frequency. Fig. 8.16 shows the experimental implementation of the proposed converter when it is connected to the grid.

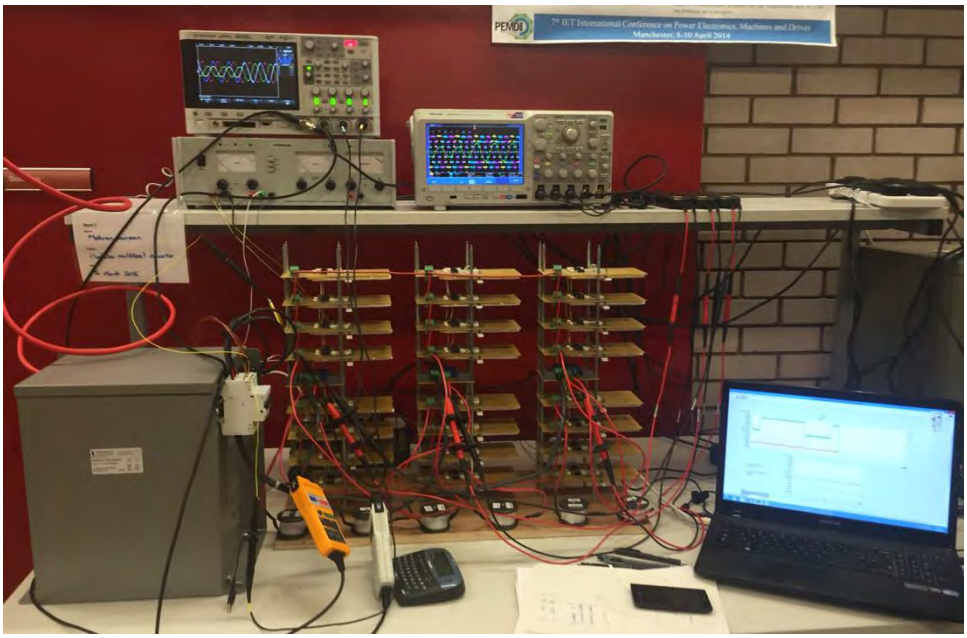


Fig. 8.16: Prototype of the 5-level grid-connected MMC with embedded lithium-ion batteries.

8.5.1 Implementation of the PLL for three-phase utility grid

A three phase PLL has been designed and implemented in the NI CompactRIO to verify the simulated results. Fig. 8.17, Fig. 8.18, and Fig. 8.19 show the responses of the PLL system when the damping ratio is set to 0.707 and the closed-loop natural frequency is chosen equal to 50 Hz, 100 Hz, and 1 kHz, respectively. The grid line voltage is 400 V and the transformer output line voltage is 10 V. Under these conditions, the gains of the loop filter are $k_{12} = 54.414$, 108.828, and 1.0883×10^3, and $k_{13} = 1.2088\times10^4$, 4.8351×10^4, and 4.8351×10^6, respectively. The tests confirm that the designed PLL work according to the simulations shown in Fig. 6.17, with a faster dynamic response for a larger bandwidth of the controller.

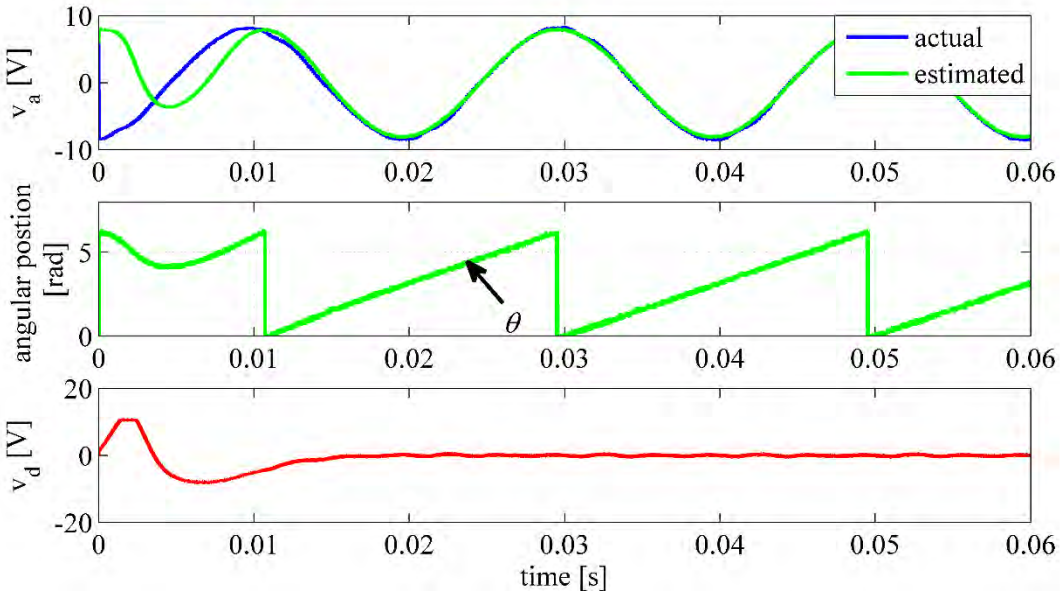


Fig. 8.17: Experimental results of three phase PLL system: actual and estimated grid phase voltages, phase angle, and the *d*-axis component of the grid voltage ($\zeta = 0.707$, $f_n = 50$ Hz).

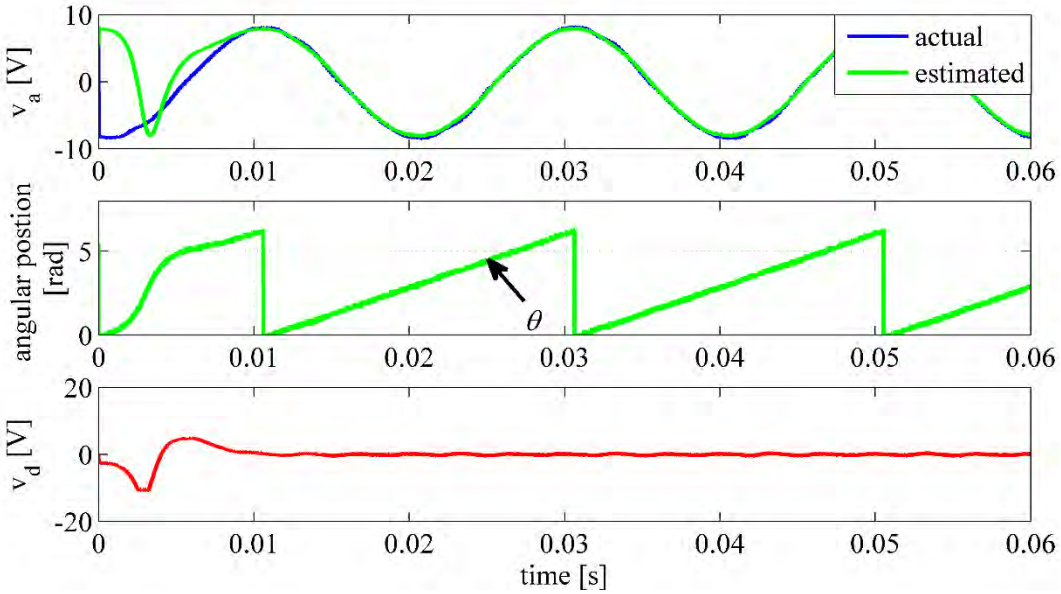


Fig. 8.18: Experimental results of three phase PLL system: actual and estimated grid phase voltages, angular position, and the *d*-axis components of grid voltage ($\zeta = 0.707$, $f_n = 100$ Hz).

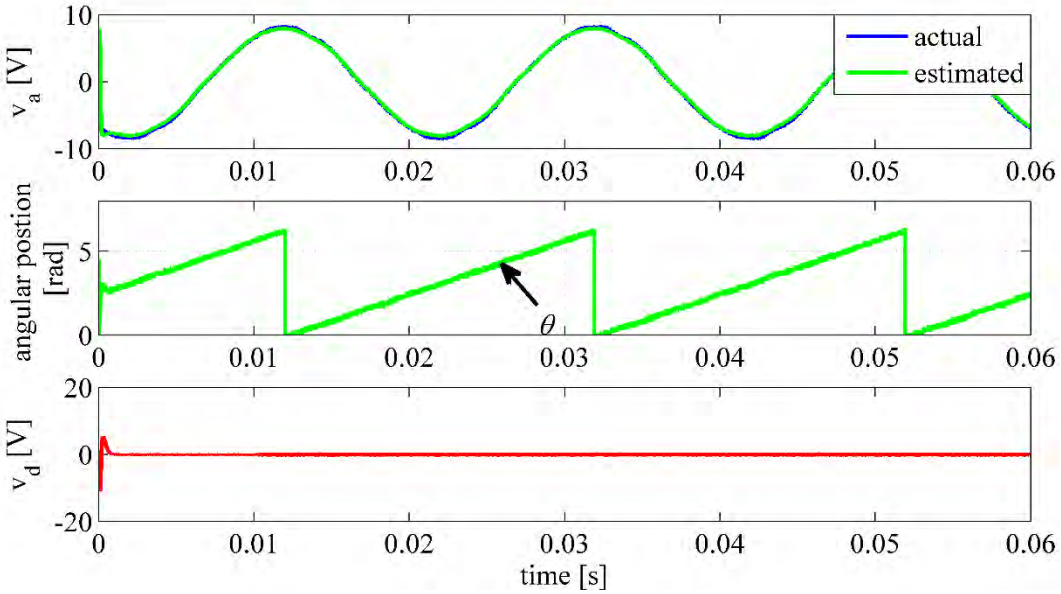


Fig. 8.19: Experimental results of three phase PLL system: actual and estimated grid phase voltages, angular position, and the *d*-axis components of grid voltage ($\zeta = 0.707$, $f_n = 1$ kHz).

8.5.2 Grid current control test

In order to verify the response of the grid current controller, different step changes of the reference direct-axis component of the grid current have been applied, as shown in Fig. 8.20, while the reference quadrature component has been set to zero in order to obtain a (nearly) unity power factor during the recharge process of cells. The converter shows a good capability of tracking the reference components of the current. Fig. 8.20 also shows the experimental phase voltage at the output of the transformer, the phase current of the MMC and the converter line-to-line voltages measured at i_d equal to 0 A, 10 A, 20 A and 30 A. Table 8.9 summarises the correspondent calculated distortion, displacement, and power factors. It is clear from the results that the grid current is almost sinusoidal for all the conditions shown in the figures and the converter recharges the cells at (nearly) unity power factor. The distortion factor is slightly lower for low grid current because the grid voltages are not symmetrical. Therefore, when the current drawn by the converter increases, the power factor is closer to unity because the distortion factor decreases.

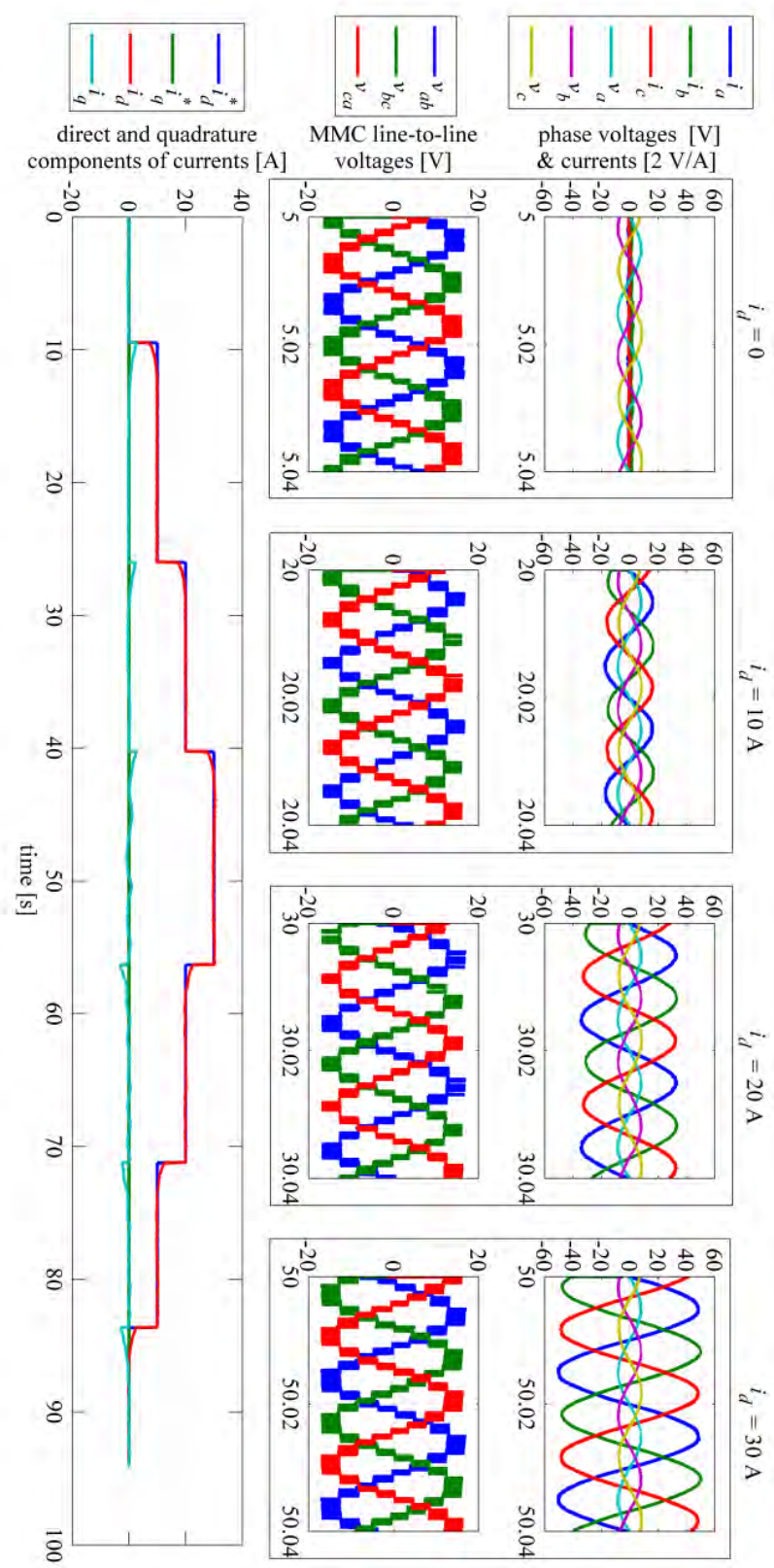


Fig. 8.20: Experimental results of the grid current controller.

Table 8.9: The estimated power factor.

I_d[A]	Distortion factor	Displacement factor	Input power factor
10	0.9978	0.9998	0.9976
20	0.9992	0.9999	0.9991
30	0.9996	0.9999	0.9995

Fig. 8.21 shows the experimental transient waveforms for the charge operation when a step change in the reference direct-axis current is applied from 10 A to 20 A and the reference quadrature component is maintained to 0. These waveforms confirm stable operations of MMC and good decoupling of the direct and quadrature current controllers.

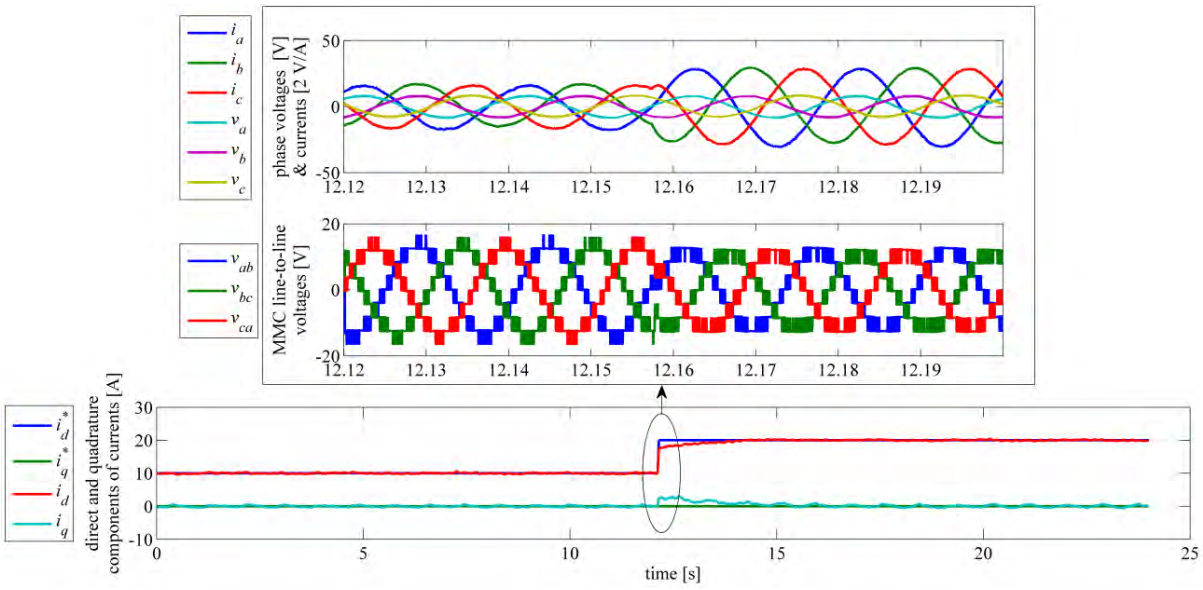


Fig. 8.21: Experimental transient waveforms for a step change in i_d.

8.5.3 SOC balancing during the recharge process

For this test, the 24 Li-ion cells have been initially discharged to different SOC values in order to test the SOC balancing algorithm during the recharge process. The maximum SOC unbalancing between the cells has been set to 35%. The cells have been charged at constant grid current of 20 A peak and the carrier frequency is set to 2.25 kHz. Table 8.10 summarises the control gains used for the experiment for the PLL and the grid current control systems.

Table 8.10: Control gains used for experiment during the charge process.

f_n = 1 kHz	Proportional gain of PLL control	k_{12}	1.0883×10^3 rad/(V s)
ζ = 0.707	Integral gain of PLL control	k_{13}	4.8351×10^6 rad/(V s^2)
f_n = 339.3195 Hz	Proportional gain of grid current control	k_{14}	1 Ω
ζ = 85.2803	Integral gain of grid current control	k_{15}	25 Ω s

Note: The relations between the control gains and the closed loop natural frequency f_n and the damping ratio ζ are given in Appendix C.

Fig. 8.22 shows that the balancing controller equalises the SOCs of all the battery cells towards the same level within the first 48 minutes of the recharge process. Fig. 8.22 shows also the converter line-to-line voltages, the phase grid voltage at the output of the transformer and the grid current, measured at t = 200 s and t = 2900 s in order to demonstrate that they are not affected by the balancing control. The grid current is almost sinusoidal in both conditions and the converter recharges the cells at unity power factor.

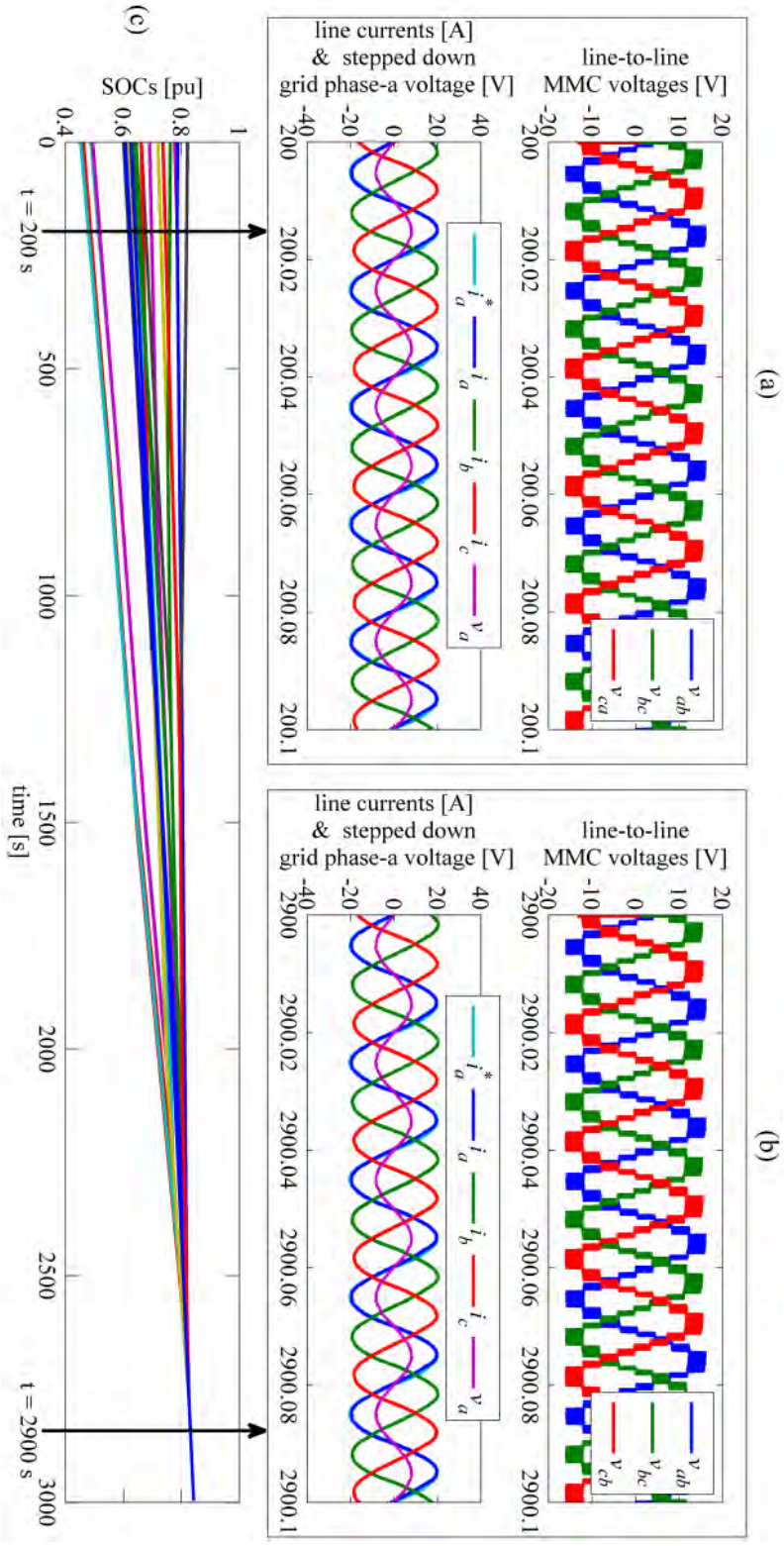


Fig. 8.22: Experimental results during the recharge process: (a) waveforms measured at 200 s. (b) waveforms measured at 2900 s, (c) SOCs of the 24 battery cells.

In summary, the chapter has experimentally verified the simulation work with the lab prototype of MMC with 4 SMs per arm. The experimental tests include preliminary tests on dead time, level shifting and sunbber circuit of each SM and then experimental tests of the converter under no load and static load conditions. The experimental results obtained from the laboratory model using 24 Li-Ion battery units have verified the effectiveness of the proposed SOC control method and confirmed the technical features of the converter's topology presented.

The proposed converter has been also tested with experiments under dynamic load conditions to balance the battery cells and follow the new European driving cycle, showing a good capability of achieving cell balancing and tracking the reference speed even during the cell balancing. The experimental efficiency of a SM has been also compared with the simulations carried out for the same number of SMs at different motor speeds. Both simulated and experimental efficiencies show a close agreement.

Finally, the chapter shows experimental results for the implemented PLL, the test of grid current controller, and the recharge control algorithm from the three-phase utility grid at (nearly) unity power. The results confirm that the designed PLL has a good capability of tracking the grid phase angle and the grid current controller has a good capability of tracking the reference components of the current, the results also show that the balancing controller equalises the SOCs of all the battery cells towards the same level during the recharge process.

Chapter 9

Conclusion and Future Work

9.1 Conclusions

This thesis has presented a new traction converter for battery electric vehicles based on the topology of modular multilevel converters with embedded battery cells. This topology integrates the functions of the battery management system in the power converter, without the need of external balancing circuits. The selected converter topology enables a large flexibility on the design of power devices. Since the battery cells are directly connected to the dc-link of the submodules, the proposed MMC uses low-voltage MosFETs to take advantage of their low on-state resistance. The state of charge of the battery cells is balanced using a dedicated controller that balances the energy of the leg, arm, and cells of the converter and does not affect the waveforms of the output current. The proposed converter produces an extremely low distortion of the output current, with direct benefits for the operations as a drive and as a battery charger. In the first case, the motor efficiency increases with benefits on the fuel economy of the electric vehicle. In the second case, the grid filter can be eliminated with benefits on the hardware costs.

The high number of devices can pose concerns on the proposed MMC in terms of conversion efficiency, but this matter has not received enough attention in the technical literature. Therefore, this thesis has presented an analytical method for the calculation of power losses of the MosFET-based MMC. The losses of the proposed converter have been compared with those

of a traditional two-level converters and the result has shown that the proposed converter presents better efficiencies at light loads, since losses are predominantly given by conduction losses. This suggests that the converter fits better than two-level inverter for urban use, where the motor is used below its full power for most of the time.

The thesis has also investigated the stationary recharge from a three-phase ac grid. The recharge of the cells has been divided into a phase at constant current up to the maximum voltage and a phase at constant voltage up to the completion of the recharge process. The results show that the modular multilevel converter topology can effectively ensure the active balancing of the cells during the recharge without any auxiliary balancing circuit.

The proposed converter has been tested with simulations and validated by experiments on a converter prototype with 4 sub-modules per arm, having line voltage of 10 V and line current of 50 A. The tests have demonstrated the correct operations of the converter to drive both a static load and an induction motor and as a battery charger. For all the different tasks, the SOC balancing control has been successfully verified. When the motor is set to follow the new European driving cycle, which is the reference cycle of electric cars, the battery cells have been balanced in 800 seconds starting from a 40% initial imbalance. The loss model has been also fully validated and has shown a converter efficiency of the experimental setup of 85% in a wide range of frequencies.

The proposed converter enables a new concept of battery cells directly embedded in the power converter and, from the assessment of its performance and characteristics, it is a suitable candidate to eliminate the balancing circuits of the battery pack and improve the output waveforms of traditional inverters.

9.2 Future work

The work of this thesis on modular multilevel converter with embedded battery cells for electric vehicles presents several opportunities for further research. The main avenues of future investigation are the following:

- reduce the number of SMs per arm using a boost dc-dc converter to increase the voltage of the battery cell and evaluate the impact in terms of the additional weight of the boost inductors.
- optimise the prototype to fit into a real car. This includes a more advanced cooling system and a thermal management of the cells. The thermal management can be easily included in the proposed controller, because the cells can be individually connected or disconnected using the half-bridge converters and keep the temperature within the optimal range.
- analyse the proposed MMC with faulty operations. This includes the analysis of the converter with one module open or short-circuited; the evaluation of performance with a reduced number of working modules; the selection of proper algorithms for the fault determination and isolation; and the determination of the relationship between the type of fault, the number of faulty modules and the THD of the output currents.
- add a voltage regulator in the controller to charge the cells at constant voltage up to their unity SOC when the voltage becomes equal to the maximum cell's voltage.
- develop a recharge algorithm for a single-phase ac supply and a dc supply using the same approach proposed converter. This requires the development of a new SOC balancing algorithm that can be derived from the proposed control valid for three-phase ac supply. For the single-phase ac supply, this requires also the adaptation of the PLL.

This new additional recharge mode will then require the development of a Simulink model and the experimental verification on a modified version of the test rig.

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Appendices

Appendix A Equations of Control Parameters

A.1 Derivation of the term $\overline{\mathbf{SOC}}_{kt}(z) - \overline{\mathbf{SOC}}_{kb}(z)$ in (4.12)

Solving (4.11) for $d(\overline{\mathrm{SOC}}_{kt} - \overline{\mathrm{SOC}}_{kb})/dt$ gives:

$$\frac{d}{dt}(\overline{\mathrm{SOC}}_{kt} - \overline{\mathrm{SOC}}_{kb}) = -\frac{V_m}{nQv_{\mathrm{cell}}} c_k . \tag{A.1}$$

Substituting (3.7) in (A.1) gives:

$$\frac{d}{dt}(\overline{\mathrm{SOC}}_{kt} - \overline{\mathrm{SOC}}_{kb}) = -\frac{\frac{1}{2}mnv_{\mathrm{cell}}}{nQv_{\mathrm{cell}}} c_k \Rightarrow \frac{d}{dt}(\overline{\mathrm{SOC}}_{kt} - \overline{\mathrm{SOC}}_{kb}) = -\frac{m}{2Q} c_k , \tag{A.2}$$

which can be represented in z-domain as:

$$\overline{\mathrm{SOC}}_{kt}(z) - \overline{\mathrm{SOC}}_{kb}(z) = -\frac{m}{2Q}\frac{T_s}{2}\frac{z+1}{z-1} C_k(z). \tag{A.3}$$

A.2 Derivation of the term $\overline{\mathbf{SOC}}_{k}(z)$ in (4.12)

Solving (4.20) for $d\overline{\mathrm{SOC}}_k/dt$ gives:

$$\frac{d\overline{\mathrm{SOC}}_k}{dt} = \frac{1}{2Q}\left[I_{cir,dc,k} - \frac{V_m I_m \cos\varphi}{2n v_{\mathrm{cell}}} \right]. \tag{A.4}$$

Substituting (3.7) in (A.4) gives:

$$\frac{d\overline{\mathrm{SOC}}_k}{dt} = \frac{1}{2Q}\left[I_{cir,dc,k} - \frac{\frac{1}{2}mnv_{\mathrm{cell}} I_m \cos\varphi}{2n v_{\mathrm{cell}}} \right] \Rightarrow \frac{d\overline{\mathrm{SOC}}_k}{dt} = \frac{1}{2Q}\left[I_{cir,dc,k} - \frac{1}{4} mI_m \cos\varphi \right], \tag{A.5}$$

which can be represented in z-domain as:

$$\overline{\mathrm{SOC}}_k(z) = \frac{1}{2Q}\frac{T_s}{2}\frac{z+1}{z-1}\left[I_{cir,dc,k} - D(z)\right], \quad D(z) = \frac{1}{4}mI_m\cos\varphi. \tag{A.6}$$

A.3 Derivation of the term $I_{cir,k}(z)$ in (4.12)

The voltage drop across the buffer inductor, $v_{L,cir,k}$, due to the circulating current, $i_{cir,k}$, is given by:

$$v_{L,cir,k} = L\frac{di_{cir,k}}{dt} \tag{A.7}$$

Solving (A.7) for $di_{cir,k}/dt$ gives:

$$\frac{di_{cir,k}}{dt} = \frac{1}{L}v_{L,cir,k} \tag{A.4}$$

which can be represented in z-domain as:

$$I_{cir,k}(z) = \frac{1}{L}\frac{T_s}{2}\frac{z+1}{z-1}V_{L,cir,k}(z) \tag{A.5}$$

A.4 Control parameters in (4.23)

$$K_1 = \frac{1}{T_sQ}k_1 + \frac{1}{2Q}k_2; \quad K_2 = \frac{1}{T_sQ}; \quad K_3 = -\frac{m}{T_sQ}k_3 - \frac{m}{2Q}k_4; \quad K_4 = \frac{T_s}{2L}k_5. \tag{A.6}$$

$$a_1 = a_2 = \frac{1}{T_sQ}k_1 + \frac{1}{2Q}k_2 + \frac{4}{T_s^2}; \quad a_3 = -\frac{m}{T_sQ}k_3 - \frac{m}{2Q}k_4 + \frac{4}{T_s^2}. \tag{A.7}$$

$$b_1 = b_2 = \frac{1}{Q}k_2 - \frac{8}{T_s^2}; \quad b_3 = -\frac{m}{Q}k_4 - \frac{8}{T_s^2}. \tag{A.8}$$

$$c_1 = c_2 = -\frac{1}{T_sQ}k_1 + \frac{1}{2Q}k_2 + \frac{4}{T_s^2}; \quad c_3 = \frac{m}{T_sQ}k_3 - \frac{m}{2Q}k_4 + \frac{4}{T_s^2}; \quad c_4 = \frac{T_s}{2L}k_5 - 1. \tag{A.9}$$

$$\alpha_1 = \frac{2k_1 - T_sk_2}{2k_1 + T_sk_2}; \quad \alpha_2 = \frac{2k_3 - T_sk_4}{2k_3 + T_sk_4}. \tag{A.10}$$

A.5 Control parameters in (4.33)

$$K_5 = \frac{2}{T_s L_{eq}} k_6 + \frac{1}{L_{eq}} k_7. \tag{A.11}$$

$$a_5 = \frac{2}{T_s L_{eq}} k_6 + \frac{1}{L_{eq}} k_7 + \frac{4}{T_s^2}. \tag{A.12}$$

$$b_5 = \frac{2}{L_{eq}} k_7 - \frac{8}{T_s^2}. \tag{A.13}$$

$$c_5 = -\frac{2}{T_s L_{eq}} k_6 + \frac{1}{L_{eq}} k_7 + \frac{4}{T_s^2}. \tag{A.14}$$

$$\alpha_5 = \frac{2k_6 - T_s k_7}{2k_1 + T_s k_2}. \tag{A.15}$$

A.6 Control parameters in (4.44)

$$\begin{aligned} &K_6 = \frac{2}{T_s J} k_8 + \frac{1}{J} k_9; \quad K_7 = \frac{2}{T_s J}; \\ &K_8 = \frac{2}{T_s} \frac{L_m R_r'}{L_r'} k_{10} + \frac{L_m R_r'}{L_r'} k_{11}; \quad K_9 = \frac{2}{T_s} \frac{1}{\sigma L_s} k_{12} + \frac{1}{\sigma L_s} k_{13}. \end{aligned} \tag{A.16}$$

$$\begin{aligned} &a_6 = a_7 = \frac{2}{T_s J} k_8 + \frac{1}{J} k_9 + \frac{4}{T_s^2}; \\ &a_8 = \left(\frac{2R_r'}{T_s L_r'} + \frac{2L_m R_r'}{T_s L_r'} \right) k_{10} + \frac{L_m R_r'}{L_r'} k_{11} + \frac{4}{T_s^2}; \quad a_9 = \frac{1}{\sigma L_s} k_{12} + \frac{2}{\sigma L_s T_s} k_{13} + \frac{4}{T_s^2}. \end{aligned} \tag{A.17}$$

$$b_6 = b_7 = \frac{1}{Q} k_9 - \frac{8}{T_s^2}; \quad b_8 = \frac{2L_m R_r'}{L_r'} k_{11} - \frac{8}{T_s^2}; \quad b_9 = \frac{2}{\sigma L_s} k_{13} - \frac{8}{T_s^2} \tag{A.18}$$

$$\begin{aligned} &c_6 = c_7 = -\frac{2}{T_s J} k_8 + \frac{1}{J} k_9 + \frac{4}{T_s^2}; \\ &c_8 = -\left(\frac{2R_r'}{T_s L_r'} + \frac{2L_m R_r'}{T_s L_r'} \right) k_{10} + \frac{L_m R_r'}{L_r'} k_{11} + \frac{4}{T_s^2}; \quad c_9 = \frac{1}{\sigma L_s} k_{13} - \frac{2}{\sigma L_s T_s} k_{12} + \frac{4}{T_s^2}. \end{aligned} \tag{A.19}$$

$$\alpha_6 = \frac{2k_8 - T_s k_9}{2k_8 + T_s k_9}; \quad \alpha_7 = \frac{2k_{10} - T_s k_{11}}{2k_{10} + T_s k_{11}}; \quad \alpha_8 = \frac{2k_{12} - T_s k_{13}}{2k_{12} + T_s k_{13}} \tag{A.20}$$

A.7 Control parameters in (4.49) & (4.56)

$$K_{10} = \frac{2}{T_s} k_{14} + k_{15}; \quad K_{11} = \frac{4}{T_s L} k_{16} + \frac{2}{L} k_{17}. \tag{A.21}$$

$$a_{10} = \frac{2}{T_s} k_{14} + k_{15} + \frac{4}{T_s^2}; \quad a_{11} = \frac{4}{T_s L} k_{16} + \frac{2}{L} k_{17} + \frac{4}{T_s^2}. \tag{A.22}$$

$$b_{10} = 2k_{15} - \frac{8}{T_s^2}; \quad b_{11} = \frac{4}{L} k_{17} + -\frac{8}{T_s^2}. \tag{A.23}$$

$$c_{10} = -\frac{2}{T_s} k_{14} + k_{15} + \frac{4}{T_s^2}; \quad c_{11} = -\frac{4}{T_s L} k_{16} + \frac{2}{L} k_{17} + \frac{4}{T_s^2}. \tag{A.24}$$

$$\alpha_{10} = \frac{2k_{14} - T_s k_{15}}{2k_{14} + T_s k_{15}}; \quad \alpha_{11} = \frac{2k_{16} - T_s k_{17}}{2k_{16} + T_s k_{17}}. \tag{A.25}$$

Appendix B Derivations

B.1 Derivation of equation (4.4)

$$
\begin{aligned}
&p_k^{\Delta} = -\frac{1}{2} n v_{\text{cell}} i_k - 2 v_k i_{cir,k} - L \frac{d}{dt}(i_k i_{cir,k}) = \\
&= -\frac{1}{2} n v_{\text{cell}} I_m \sin(\theta_k - \varphi) - 2\left(V_m \sin(\theta_k)\right)\left(I_{cir,dc,k} + \sum_{i=1}^{\infty} I_{cir,i,k} \sin(\beta_{i,k}) \right) + \\
&- L \frac{d}{dt}\left[\left(I_m \sin(\theta_k - \varphi)\right)\left(I_{cir,dc,k} + \sum_{i=1}^{\infty} I_{cir,i,k} \sin(\beta_{i,k}) \right) \right] = \\
&\approx -2 V_m \sin(\theta_k) \sum_{i=1}^{\infty} I_{cir,i,k} \sin(\beta_{i,k}) + \\
&- \omega L I_m \cos(\theta_k - \varphi) \sum_{i=1}^{\infty} I_{cir,i,k} \sin(\beta_{i,k}) - \omega L I_m \sin(\theta_k - \varphi) \sum_{i=1}^{\infty} i I_{cir,i,k} \cos(\beta_{i,k}) = \\
&= -\sum_{i=1}^{\infty} V_m I_{cir,i,k} \left[\cos(\theta_k - \beta_{i,k}) - \cos(\theta_k + \beta_{i,k}) \right] + \\
&- \frac{1}{2} \omega L \sum_{i=1}^{\infty} I_m I_{cir,i,k} \left[\sin(\theta_k + \beta_{i,k} - \varphi) - \sin(\theta_k - \beta_{i,k} - \varphi) \right] + \\
&- \frac{1}{2} \omega L \sum_{i=1}^{\infty} i I_m I_{cir,i,k} \left[\sin(\theta_k + \beta_{i,k} - \varphi) + \sin(\theta_k - \beta_{i,k} - \varphi) \right] \approx \\
&= -\sum_{i=1}^{\infty} V_m I_{cir,i,k} \cos(\theta_k - \beta_{i,k}) + \\
&+ \frac{1}{2} \omega L \sum_{i=1}^{\infty} I_m I_{cir,i,k} \sin(\theta_k - \beta_{i,k} - \varphi) + \\
&- \frac{1}{2} \omega L \sum_{i=1}^{\infty} i I_m I_{cir,i,k} \sin(\theta_k - \beta_{i,k} - \varphi) \approx \\
&\approx -V_m I_{cir,1,k} \cos(\theta_k - \beta_{1,k}) + \\
&+ \frac{1}{2} \omega L I_m I_{cir,1,k} \sin(\theta_k - \beta_{1,k} - \varphi) - \frac{1}{2} \omega L I_m I_{cir,1,k} \sin(\theta_k - \beta_{1,k} - \varphi) = \\
&= -V_m I_{cir,1,k} \cos(\theta_k - \beta_{1,k}) = -V_m I_{cir,1,k} \cos \gamma_{1,k}
\end{aligned}
\tag{B.1}
$$

B.2 Derivation of equation (4.20)

$$
\begin{aligned}
p_k^{\Sigma} &= -v_k i_k + n v_{\text{cell}} i_{cir,k} - L\left(i_{kt} \frac{di_{kt}}{dt} + i_{kb} \frac{di_{kb}}{dt} \right) = \\
&= -V_m \sin(\theta_k) I_m \sin(\theta_k - \varphi) + n v_{\text{cell}} \left[I_{cir,dc,k} + \sum_{i=1}^{\infty} I_{cir,i,k} \sin(\beta_{i,k}) \right] \\
&- L\left(\left(i_{cir,k} + \frac{1}{2} i_k \right) \frac{d}{dt} \left(i_{cir,k} + \frac{1}{2} i_k \right) + \left(i_{cir,k} - \frac{1}{2} i_k \right) \frac{d}{dt} \left(i_{cir,k} - \frac{1}{2} i_k \right) \right) = \\
&= -V_m \sin(\theta_k) I_m \sin(\theta_k - \varphi) + n v_{\text{cell}} \left[I_{cir,dc,k} + \sum_{i=1}^{\infty} I_{cir,i,k} \sin(\beta_{i,k}) \right] + \\
&- L\left(i_{cir,k} \frac{di_{cir,k}}{dt} + \frac{1}{2} i_{cir,k} \frac{di_k}{dt} + \frac{1}{4} i_k \frac{di_k}{dt} + \frac{1}{2} i_k \frac{di_{cir,k}}{dt} \right) + \\
&- L\left(i_{cir,k} \frac{di_{cir,k}}{dt} - \frac{1}{2} i_{cir,k} \frac{di_k}{dt} + \frac{1}{4} i_k \frac{di_k}{dt} - \frac{1}{2} i_k \frac{di_{cir,k}}{dt} \right) = \\
&= -V_m \sin(\theta_k) I_m \sin(\theta_k - \varphi) + n v_{\text{cell}} \left[I_{cir,dc,k} + \sum_{i=1}^{\infty} I_{cir,i,k} \sin(\beta_{i,k}) \right] + \\
&- L\left(2 i_{cir,k} \frac{di_{cir,k}}{dt} + \frac{1}{2} i_k \frac{di_k}{dt} \right) = \\
&= -V_m \sin(\theta_k) I_m \sin(\theta_k - \varphi) + n v_{\text{cell}} \left[I_{cir,dc,k} + \sum_{i=1}^{\infty} I_{cir,i,k} \sin(\beta_{i,k}) \right] + \\
&- 2\omega L \left(\left[\left(I_{cir,dc,k} + \sum_{i=1}^{\infty} I_{cir,i,k} \sin(\beta_{i,k}) \right) \right] \left[\left(\sum_{i=1}^{\infty} i I_{cir,i,k} \cos(\beta_{i,k}) \right) \right] \right) + \\
&- 2\omega L \left(\left[\frac{1}{4} I_m^2 \sin(\theta_k - \varphi) \cos(\theta_k - \varphi) \right] \right) \approx \\
&\approx -V_m I_m \sin(\theta_k) \sin(\theta_k - \varphi) + n v_{\text{cell}} I_{cir,dc,k} = \\
&= -\frac{1}{2} V_m I_m \cos(\theta_k) + \frac{1}{2} V_m I_m \cos(2\theta_k - \varphi) + n v_{\text{cell}} I_{cir,dc,k} \approx \\
&\approx -\frac{1}{2} V_m I_m \cos(\varphi) + n v_{\text{cell}} I_{cir,dc,k}
\end{aligned}
\tag{B.2}
$$

B.3 Derivation of equation (5.13)

To eliminate the tripled harmonics from the MMC output waveforms, the modulation frequency should be adjusted to be an odd number multiplied by 3. This means z is odd number and therefore (5.12) can be represented as:

$$E_{sw,arm} = E_{sw}^{*} \sum_{i=1}^{z} \left|\sin(2\pi i / z)\right| = 2E_{sw}^{*} \underbrace{\sum_{i=1}^{(z-1)/2} \sin(2\pi i / z)}_{y} \tag{B.3}$$

Using the Euler's formula and some trigonometric identities, the summation term, y, can be represented using a closed form expression as shown in (B.4)

$$y=\sum_{i=1}^{(z-1)/2}\sin(2\pi i/z)=\sum_{i=1}^{(z-1)/2}\mathrm{Im}\left\{e^{j(2\pi i/z)}\right\}$$

$$=\mathrm{Im}\left\{\underbrace{1+e^{j(2\pi/z)}+e^{j2(2\pi/z)}\ldots+e^{j\left(\frac{z-1}{2}\right)\left(\frac{2\pi}{z}\right)}}_{S}\right\}$$

$$S=1+e^{j\left(\frac{2\pi}{z}\right)}+e^{j2\left(\frac{2\pi}{z}\right)}\ldots+e^{j\left(\frac{z-1}{2}\right)\left(\frac{2\pi}{z}\right)}$$

$$Se^{j\left(\frac{2\pi}{z}\right)}=\left[1+e^{j\left(\frac{2\pi}{z}\right)}+e^{j2\left(\frac{2\pi}{z}\right)}\ldots+e^{j\left(\frac{z-1}{2}\right)\left(\frac{2\pi}{z}\right)}\right]e^{j\left(\frac{2\pi}{z}\right)}$$

$$Se^{j\left(\frac{2\pi}{z}\right)}=\underbrace{e^{j\left(\frac{2\pi}{z}\right)}+e^{j2\left(\frac{2\pi}{z}\right)}+e^{j3\left(\frac{2\pi}{z}\right)}\ldots+e^{j\left(\frac{z-1}{2}\right)\left(\frac{2\pi}{z}\right)}}_{S-1}+e^{j\left(\frac{z+1}{2}\right)\left(\frac{2\pi}{z}\right)}$$

$$Se^{j\left(\frac{2\pi}{z}\right)}=S-1+e^{j\pi\left(\frac{z+1}{z}\right)}\Rightarrow S=\frac{e^{j\pi\left(\frac{z+1}{z}\right)}-1}{e^{j(2\pi/z)}-1}=\left(\frac{e^{j\pi\left(\frac{z+1}{z}\right)}-1}{e^{j\left(\frac{2\pi}{z}\right)}-1}\right)\left(\frac{e^{-j\left(\frac{\pi}{z}\right)}}{e^{-j\left(\frac{\pi}{z}\right)}}\right)\left(\frac{2j}{2j}\right)=$$

$$=\frac{1}{2j}\frac{-1-e^{j\left(\frac{\pi}{z}\right)}}{\left(\frac{e^{j\left(\frac{\pi}{z}\right)}-e^{-j\left(\frac{\pi}{z}\right)}}{2j}\right)}=\frac{j}{2}\frac{e^{j\left(\frac{\pi}{z}\right)}+1}{\sin\left(\frac{\pi}{z}\right)}=\frac{1}{2}\frac{e^{j\left(\frac{\pi}{z}+\frac{\pi}{2}\right)}+e^{j\frac{\pi}{2}}}{\sin\left(\frac{\pi}{z}\right)}$$

$$y=\mathrm{Im}\{S\}=\frac{\sin\left(\frac{\pi}{2}\right)+\sin\left(\frac{\pi}{z}+\frac{\pi}{2}\right)}{2\sin\left(\frac{\pi}{z}\right)}=\frac{1+\cos\left(\frac{\pi}{z}\right)}{2\sin\left(\frac{\pi}{z}\right)}=\frac{1}{2}\cot\left(\frac{\pi}{2z}\right) \tag{B.4}$$

Using the Taylor expansion of cotangent with ignoring the high order terms gives:

$$y=\frac{1}{2}\cot\left(\frac{\pi}{2z}\right)\approx\left(\frac{z}{\pi}-\frac{\pi}{12z}\right). \tag{B.5}$$

By substituting into (B.4), the arm switching losses can be expressed as:

$$E_{sw,arm}\approx\left(\frac{2z}{\pi}-\frac{\pi}{6z}\right) \tag{B.6}$$

B.4 Derivation of equation (6.2)

The total kinetic energy stored in the vehicle, *E*, is given by:

$$E = \frac{1}{2} m_v v_v^2 \tag{B.7}$$

where v_v is the linear speed of the EV in [m/s], which can be expressed in terms of angular velocity of a flywheel, ω_f, as:

$$v_v = \frac{1}{2} \omega_f D \tag{B.8}$$

The relation between the motor speed and the flywheel speed is given by:

$$\omega_f = \frac{\omega_r}{\tau} \tag{B.9}$$

By substituting (B.8) & (B.9) in (B.7), the kinetic energy stored in the vehicle can be calculated as:

$$E = \frac{1}{2} m_v \left(\frac{D}{2\tau} \omega_r \right)^2 = \frac{1}{2} \underbrace{\left[\frac{1}{4} m_v \left(\frac{D}{\tau} \right)^2 \right]}_{J_{eq}} \omega_r^2 \tag{B.10}$$

Thus, the equivalent inertia referred to the machine shaft is given by:

$$J_{eq} = \frac{1}{4} m_v \left(\frac{D}{\tau} \right)^2 \tag{B.11}$$

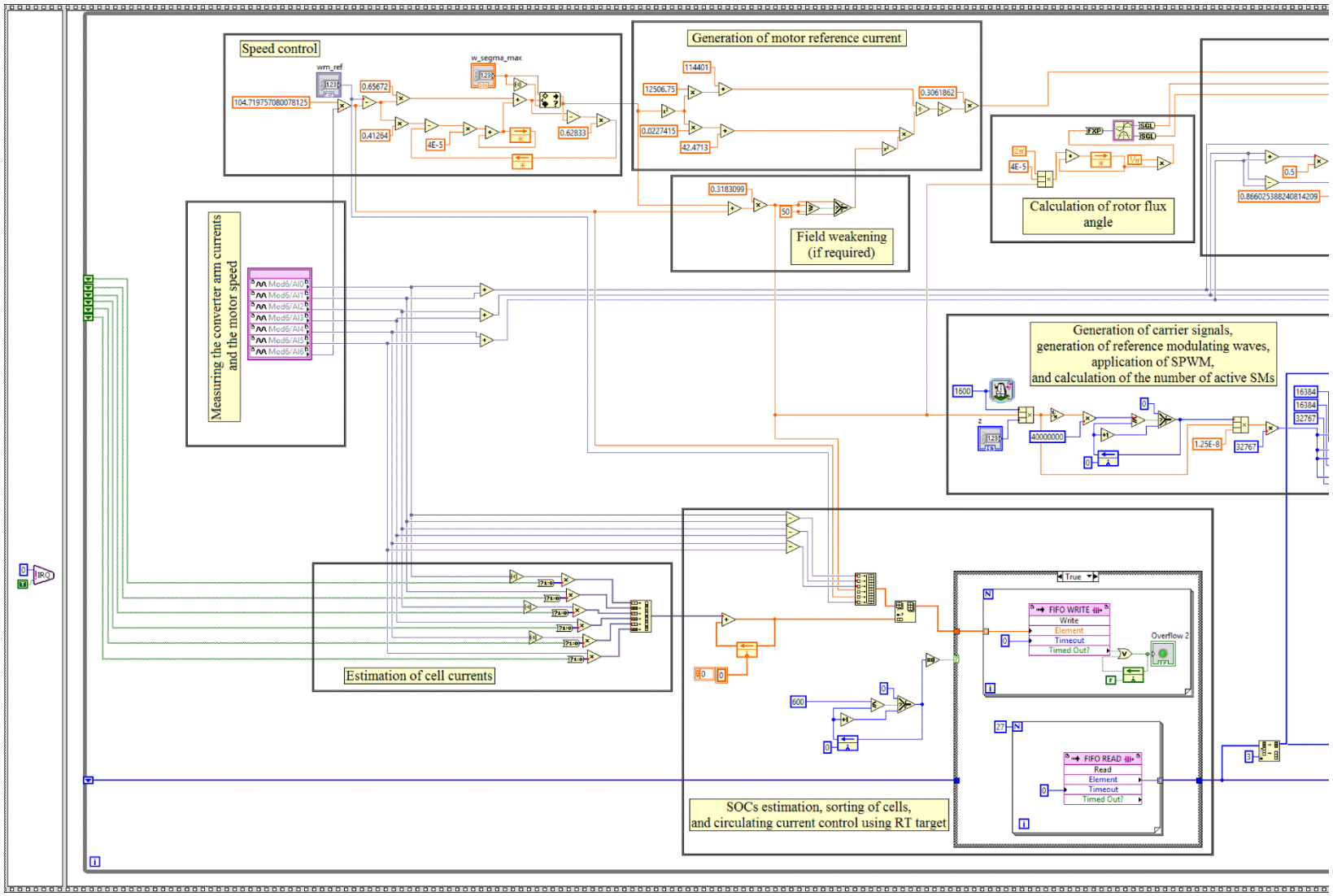
Appendix C Closed Loop Control Gains

$$
\begin{aligned}
&k_1 = 28800\,\pi Q f_n \zeta; \quad k_2 = 28800\,\pi^2 Q f_n^2 \\
&k_3 = -28800\,\pi \frac{Q}{m} f_n \zeta; \quad k_4 = -28800\,\pi^2 \frac{Q}{m} f_n^2 \\
&k_5 = \frac{L}{T} \\
&k_6 = 4\pi L_{eq} f_n \zeta; \quad k_7 = 4\pi^2 L_{eq} f_n^2 \\
&k_8 = 4\pi J f_n \zeta; \quad k_9 = 4\pi^2 J f_n^2 \\
&k_{10} = 4\pi f_n \zeta \frac{L_r'}{R_r' L_m} - \frac{1}{L_m}; \quad k_{11} = 4\pi^2 \frac{L_r'}{R_r' L_m} f_n^2 \\
&k_{12} = 4\pi\sigma L_s f_n \zeta; \quad k_{13} = 4\pi^2 \sigma L_s f_n^2 \\
&k_{14} = 4\pi \frac{f_n \zeta}{V_m}; \quad k_{15} = 4\pi^2 \frac{f_n^2}{V_m} \\
&k_{16} = 2\pi L f_n \zeta; \quad k_{17} = 2\pi^2 L f_n^2
\end{aligned}
\qquad . \qquad (C.1)
$$

Appendix D LabVIEW FPGA Programs

Fig. D. 1 shows the LabVIEW FPGA program that has been used to drive the induction motor using the proposed converter and the cell balancing control while Fig. D. 2 shows the LabVIEW FPGA programs of the charge process control system including both grid current and cell balancing control systems. Fig. D. 1 shows the case structures that have been used for the individual SOC cell balance.

Some data has been transferred between the FPGA and the real-time processor within the CompactRIO embedded system for real-time (RT) control, analysis, and data logging (i.e. sorting the cells according to their SOC in descending order and the data logging of SOCs) as shown in Fig. D. 4 and Fig. D. 5.


Speed control
wm_ref
w_segma_max
104.719757080078125
0.65672
0.41264
4E-5
0.62833
Generation of motor reference current
114401
12506.75
0.0227415
42.4713
0.3061862
0.3183099
50
Field weakening
(if required)
Calculation of rotor flux
angle
0.5
0.866025388240814209
Measuring the converter arm currents
and the motor speed
Mod6/AI0
Mod6/AI1
Mod6/AI2
Mod6/AI3
Mod6/AI4
Mod6/AI5
Mod6/AI6
Generation of carrier signals,
generation of reference modulating waves,
application of SPWM,
and calculation of the number of active SMs
1600
40000000
1.25E-8
32767
16384
16384
32767
Estimation of cell currents
600
True
FIFO WRITE
Write
Element
Timeout
Timed Out?
Overflow 2
27
FIFO READ
Read
Element
Timeout
Timed Out?
SOCs estimation, sorting of cells,
and circulating current control using RT target

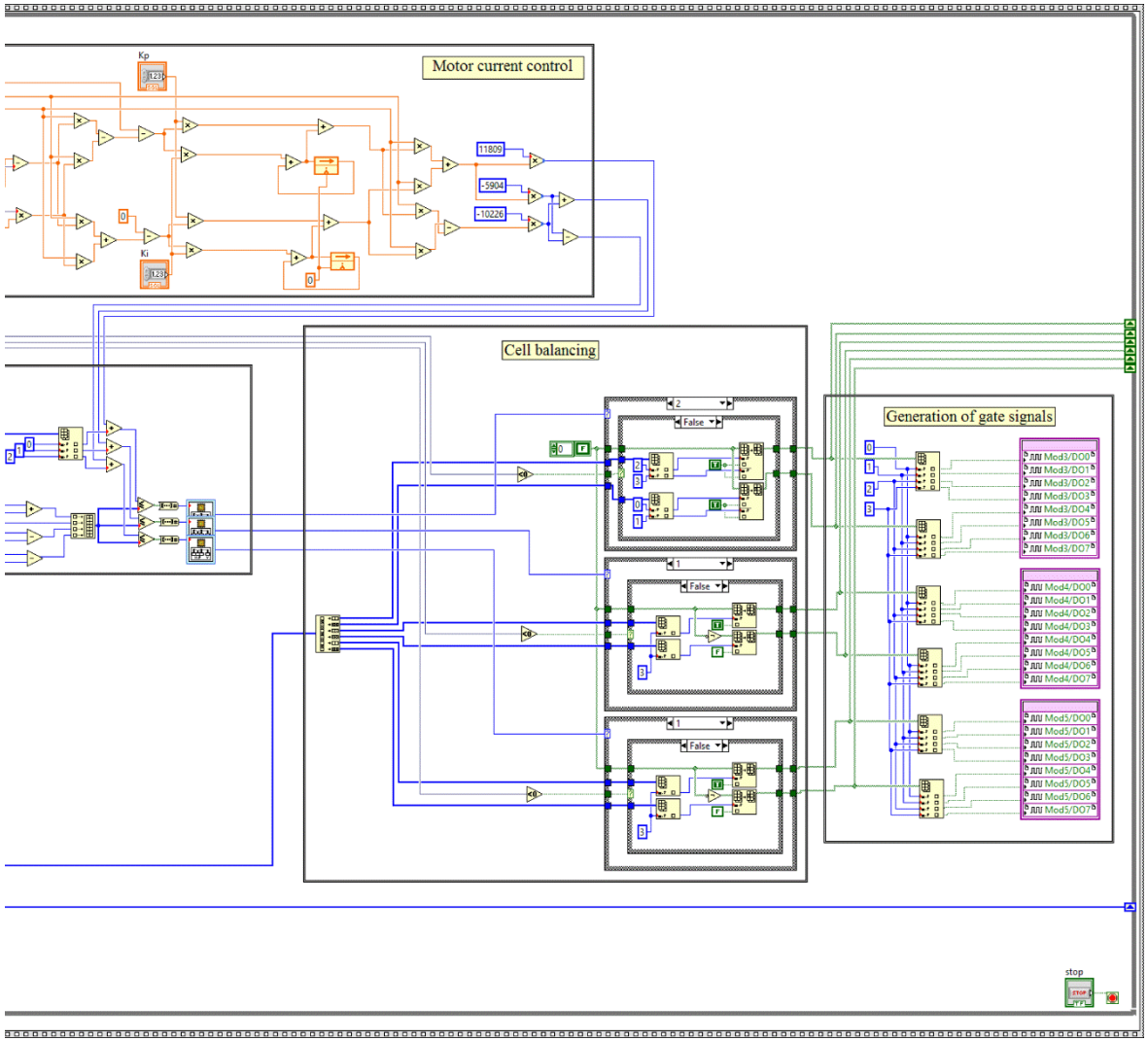


Fig. D. 1: LabVIEW FPGA program of the induction motor drive.

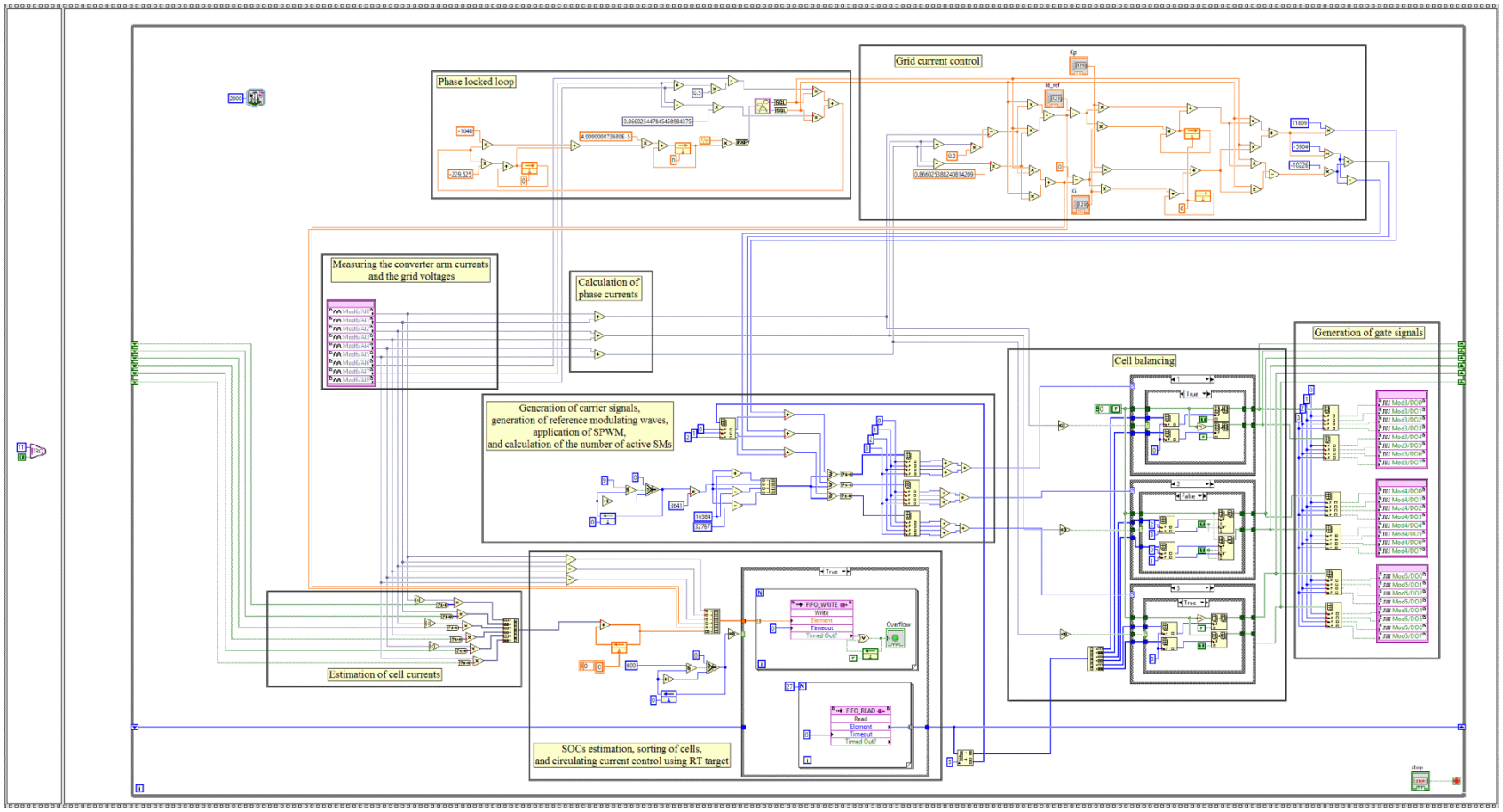


Fig. D. 2: LabVIEW FPGA program of the charge process control.

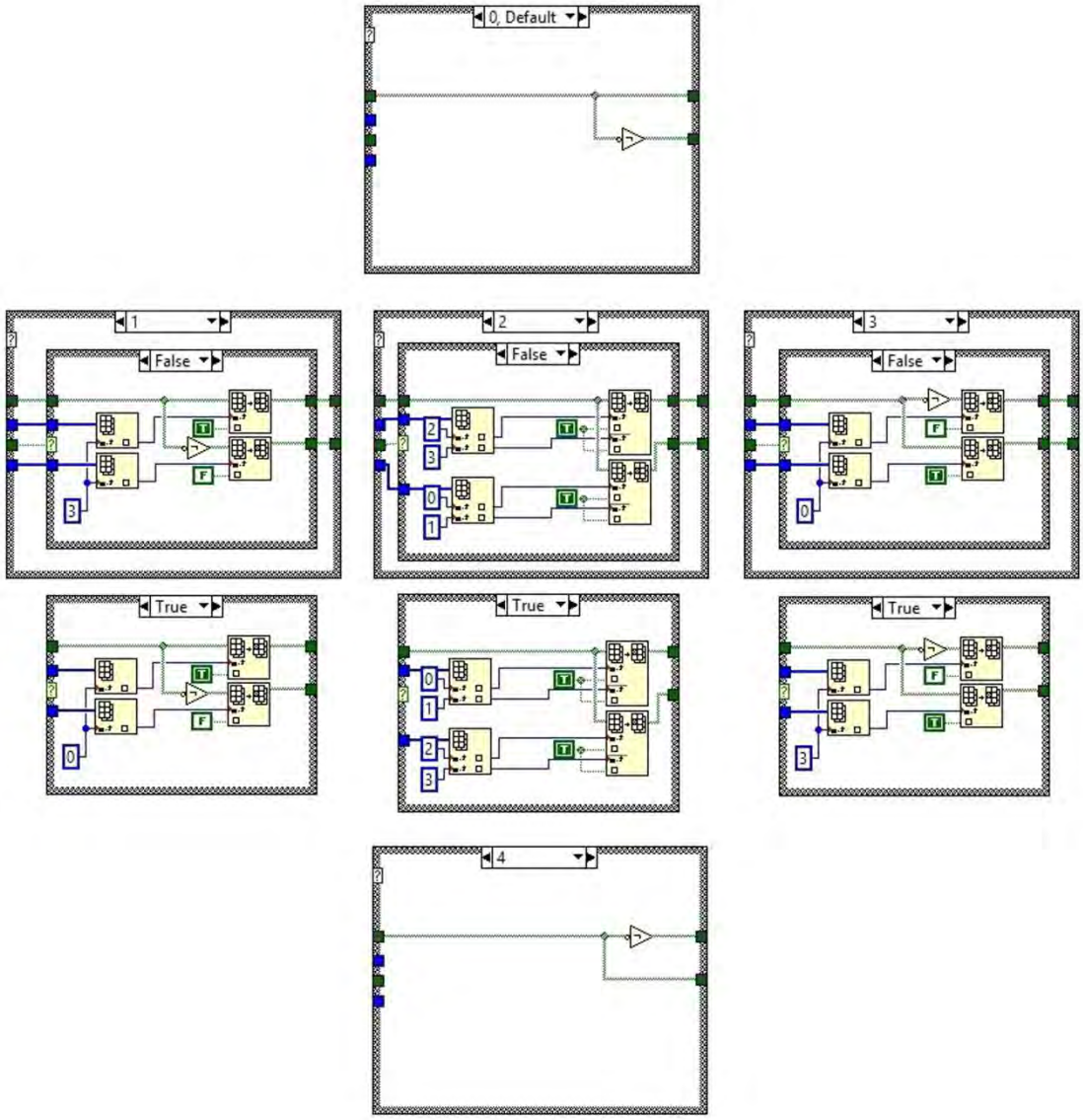


Fig. D. 3: Case structures of the cell balance control system.

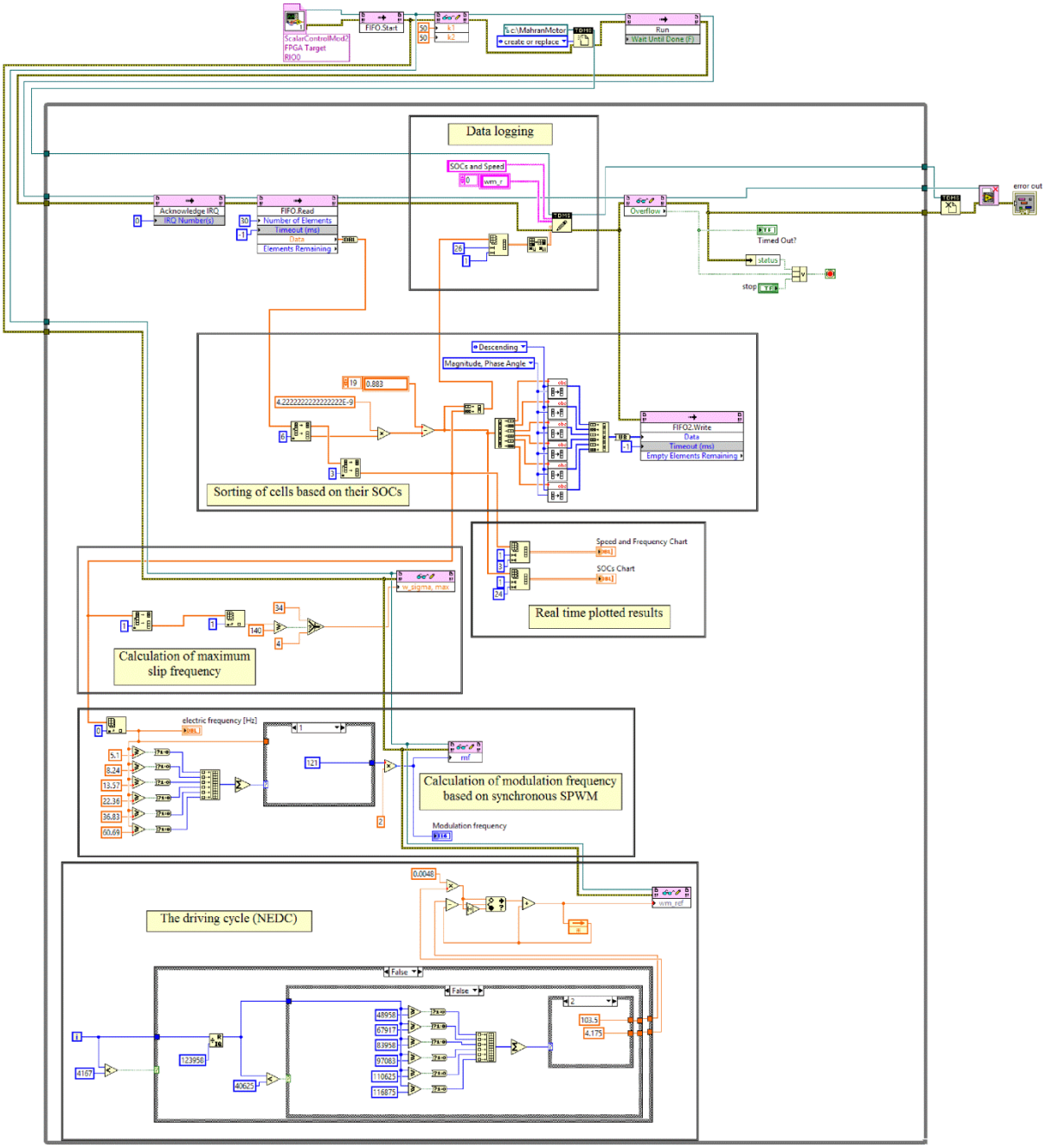


Fig. D. 4: LabVIEW program of the induction motor drive (RT target).

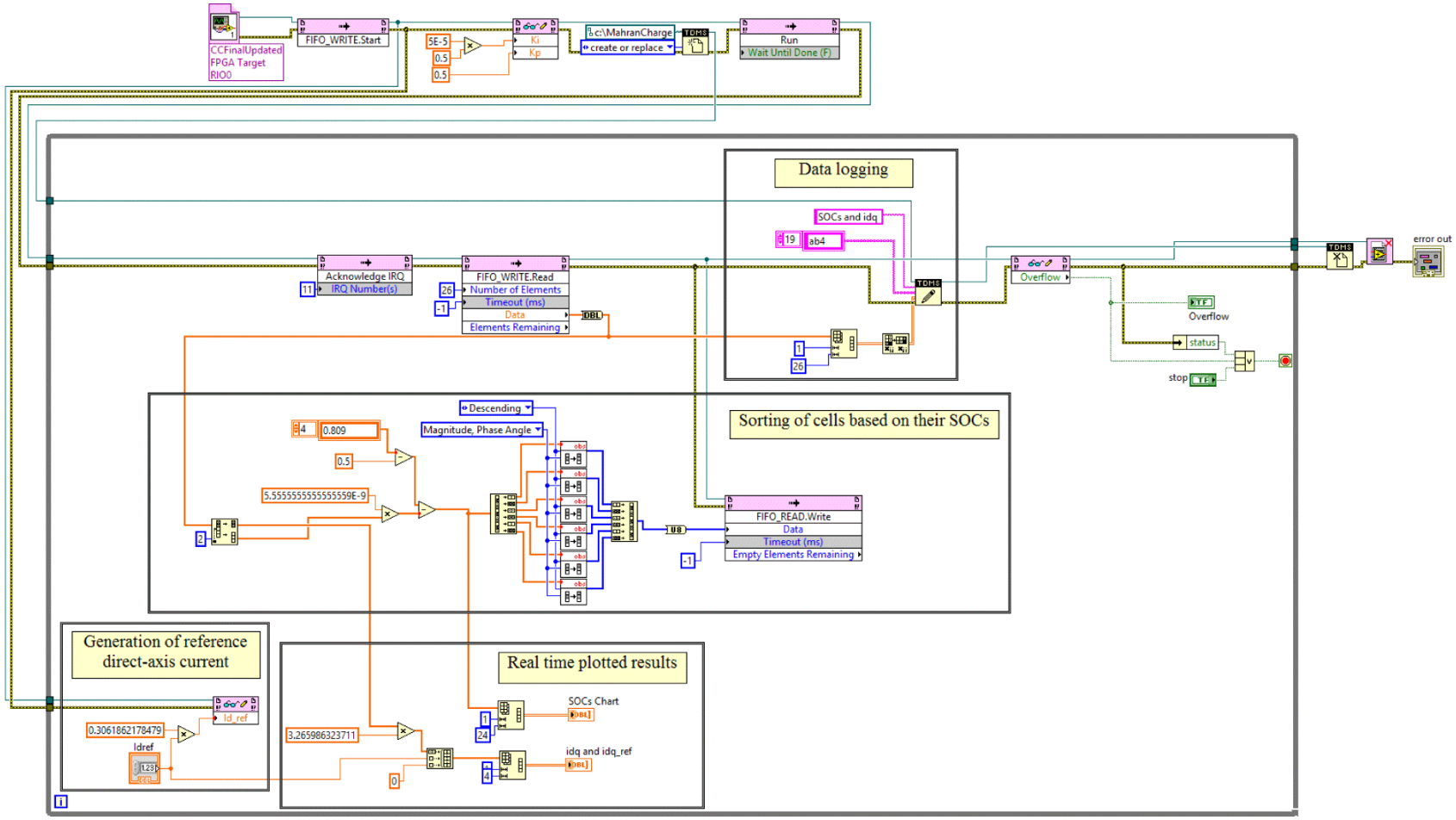


Fig. D. 5: LabVIEW program of the charge process control (RT target).