Modular Multilevel Converters for Power Transmission Systems

by

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Abstract

In this research, novel Modular Multilevel Converters (MMCs) intended for various type of power transmission systems are studied. Currently, the MMC, which is built based upon stack of identical half- or full-bridge submodules (SMs), is the dominant Voltage Source Converter (VSC) topology for power transmission systems, because of its salient features including (i) scalability/modularity to meet any voltage/power-level requirements, (ii) excellent harmonic performance, (iii) very high efficiency, and (iv) redundancy in the converter configuration. The application of power converters could be extended to novel transmission schemes that might be under research, such as High-frequency Half-Wavelength (HFHW) Transmission Line. Therefore, introducing suitable power converter topologies not only improves the developed technologies, but also facilitates the implementations of novel related ideas.

This research introduces three topologies of MMCs optimized for various type of power transmission systems. The first two topologies are intended for AC/AC applications such as HFHW system and the third converter is proposed for HVDC systems. Compared to conventional MMC, the proposed converters have fewer power switches with a major portion of them operating in soft-switching mode. Beside the theoretical studies, the viability of the proposed topologies, as well as the effectiveness of the control strategy are confirmed by both simulation and experimental results.

Furthermore, the economical aspect of HFHW power system is discussed and it is shown that this system can benefit from employing the proposed AC/AC converters.

Preface

Chapter 2 of this thesis has been published as R. Alaei, S. A. Khajehoddin and W. Xu, "Sparse AC/AC Modular Multilevel Converter," *IEEE Transactions on Power Delivery*, vol. 31, no. 3, pp. 1195-1202, June 2016. and, R. Alaei, S. A. Khajehoddin and W. Xu, "Control and Experiment of AC/AC Sparse Modular Multilevel Converter," *IEEE Transactions on Power Delivery*, (Early Access DOI: 10.1109/T-PWRD.2016.2618935). I was responsible for proposing the topology, simulation and experimental analysis as well as the manuscript composition. Drs. Khajehoddin and Xu contributed to the manuscript edits.

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Acronyms

B2B	Back-to-Back
CHBC	Cascaded H-Bridge Converter
DCC	Diode-Clamped Converter
DMC	Direct Matrix Converter
FACTS	Flexible AC Transmission System
FB	Full-Bridge
FBA	Full-Bridge Arm
FBSM	Full-Bridge Sub-Module
FBU	Full-Bridge Unfolder
FCC	Flying Capacitor Converter
FFTS	Fractional Frequency Transmission System
HB	Half-Bridge
HBA	Half-Bridge Arm
HBSM	Half-Bridge Sub-Module
HBU	Half-Bridge Unfolder
HF	High Frequency
HFHW	High Frequency Half-Wavelength
HVAC	High Voltage Alternating Current

HVDC	High Voltage Direct Current
HWTL	Half-Wavelength Transmission Line
IGBT	Insulated-Gate Bipolar Transistor
ILMC	Inverting Link Matrix Converter
IMC	Indirect Matrix Converter
MC	Matrix Converter
MMC	Modular Multilevel Converter
MMMC	MinMax Multilevel Converter
NLC	Nearest Level Control
NPCC	Neutral-Point Clamped Converter
PHMMC	Parallel Hybrid Modular Multilevel Converter
PLL	Phase-Locked Loop
PWM	Pulse-Width Modulation
RMS	Root-Mean-Square
SHE	Selective Harmonic Elimination
SHMMC	Series Hybrid Modular Multilevel Converter
SIL	Surge Impedence Loading
SM	Sub-Module
SMC	Sparse Matrix Converter
SMMC	Sparse Modular Multilevel Converter
SPWM	Sinusoidal Pulse-Width Modulation
SVM	Space Vector Modulation
THG	Third Harmonic Generator
THIL	Third Harmonic Injected Line

TOC	Total Owing Cost
USMC	Ultra Sparse Matrix Converter
VSC	Voltage Source Converter
VSI	Voltage Source Inverter
VSMC	Very Sparse Matrix Converter
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Chapter 1

Introduction

High power Voltage Source Converters (VSCs) have been the focus of research and development for a few decades and have found many industrial applications such as renewable energy resource interfaces, Flexible AC Transmission System (FACTS) devices and High Voltage Direct Current (HVDC) lines. The application of high power converters could be also extended to novel transmission schemes such as High Frequency Half-Wavelength (HFHW) power transmission [1]. In order to achieve high power ratings and high voltage levels, a single semiconductor device would be insufficient. Therefore, to increase the power capability, a number of semiconductors are paralleled to increase the current capability or series-connected to increase the voltage ratings. When power semiconductors are connected in series for high-voltage operation, both steady-state and transient voltages must be shared equally among the individual series devices which is often challenging and costly. As a result, multilevel VSC topologies can be used in high power and high voltage applications, as they reach higher voltages by utilizing low voltage power semiconductor switches, while both steady-state and transient voltage sharing are guaranteed. Multilevel VSCs offer

very low harmonic distortion and does not require bulk AC-side filters.

Currently, the Modular Multilevel Converter (MMC), which is built based upon stack of identical half- or full-bridge submodules (SMs), is the dominant VSC topology for power transmission systems, because of its salient features including (i) scalability/modularity to meet any voltage/power-level requirements, (ii) excellent harmonic performance, (iii) very high efficiency, and (iv) redundancy in the converter configuration [2–4].

This thesis focuses on introducing novel topologies of MMCs which offer the same advantages as conventional MMC with additional benefits such as lower switching losses and lower number of semiconductors. These converters are intended to operate in AC/AC transmission system such as HFHW and AC/DC systems such as HVDC lines. In total, three novel topologies are presented which their major portion of semiconductor devices operate in Zero Voltage Switching (ZVS) mode.

1.1 High Frequency Half-Wavelength Transmission Line

In this section, the HFHW system is briefly introduced. In a Half-Wavelength Transmission Line (HWTL), the line length between the sending and receiving ends is about half of the wavelength of the AC current carried by the line. Power transmission at this distance has one very attractive feature that the total line impedance becomes virtually zero (for lossless line). As a result, the sending end can be considered at close distance of the receiving end [5]. In recent years, the HWTL scheme regained the interest of industry and academia due to increasing construction of longer transmission lines [6–10]. In a 60 Hz power network, the half-wavelength will be a fixed length of

2500 km, which is too long and inflexible for practical use. In order to overcome this impediment, it is proposed to generate and transfer power at higher frequencies to shorten the half-wavelength distance, and interconnect the high-frequency portion to the rest of the power system using newly developed high power converters [1]. This scheme is called HFHW and is shown in Fig. 1.1. Unlike HVDC line which has one converter station at each end, the HFHW scheme requires only one converter station at the receiving end.
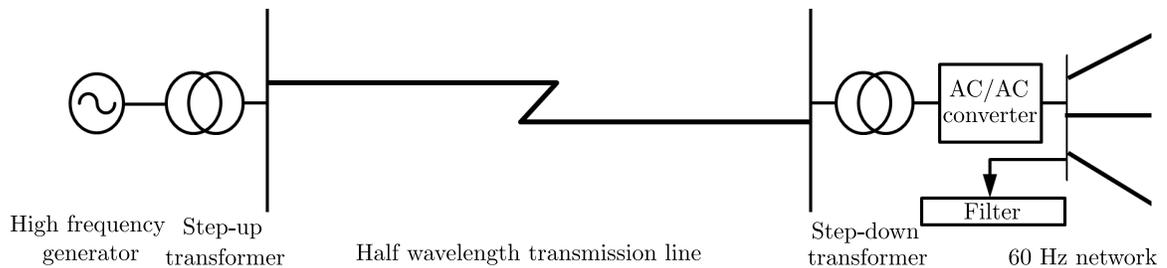
Figure 1.1. Schematic diagram of high-frequency half-wavelength line

1.2 Existing High Power Voltage Source Converters

In this section, different types of high power VSC topologies are reviewed. At the end, MMC is thoroughly discussed as one of the emerging viable options for high power applications.

1.2.1 Two-Level Voltage Source Converter

The schematic diagram of simplified 2-level Voltage Source Inverter (VSI) intended for high power applications is shown in Fig. 1.2. The inverter is composed of six groups of power electronic switches, with a free-wheeling diode in parallel with each switch. There are two ways to increase the power rating of the inverter: *i*) parallel connection of semiconductor switches to increase the current capability or *ii*) series

connection of switching to increase the voltage ratings. In both approaches, equal sharing of currents or voltages among devices is crucial. The importance and challenges of voltage sharing problem in series-connected switches in existing approaches are studied in Appendix A.
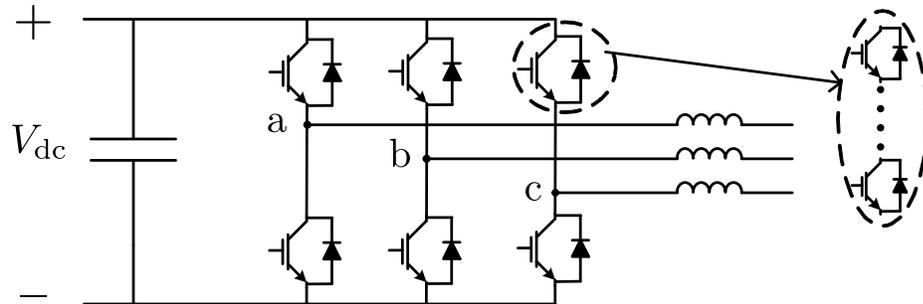
Figure 1.2. Schematic diagram of a 2-level high power voltage source inverter.

In order to decrease the harmonic distortion in a 2-level VSC, the electronic switches must be able to operate at a high switching frequency using Pulse-Width Modulation (PWM). Such high frequency switching current should be filtered before injected to AC-side using bulky filters on the AC-side. It must be added that for AC/AC applications, the Back-to-Back (B2B) version of this converter could be used with employing a DC-link to connect two AC sources [11]. Several topologies are proposed to reduce the component count of the this converter, yet they face limitations in the modes of operation and may require complex control systems [12–14].

1.2.2 Matrix Converter

Matrix Converters (MCs) are able to connect two AC sources with different frequencies without using a DC link. They are further divided into two groups of classical Direct Matrix Converter (DMC) and Indirect Matrix Converter (IMC) with fictitious DC link. A conventional DMC is an array of nine bidirectional switches that allows

any load phase to be connected to any source phase as shown in Fig. 1.3. The major advantage of MC is the absence of the DC link capacitor which could lead to a more compact design. However, the higher cost of the bidirectional switches and complex control have made this topology less attractive for industrial applications. Besides the high number of components, MCs have some difficulties to reach high voltages due to the limited availability of high voltage semiconductor switches.
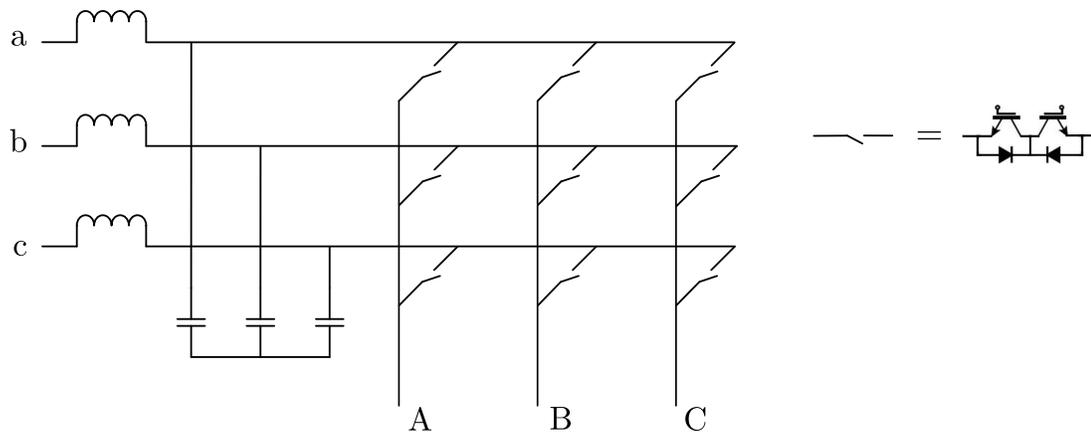
Figure 1.3. Conventional Direct Matrix Converter.

Figure 1.4 shows a conventional IMC which is obtained from the classical DMC structure. In 2002, a novel IMC is proposed called Sparse Matrix Converter (SMC) [15] which reduced the number of switches in conventional IMC. Later on, several other topologies are derived from SMC, such as Very Sparse Matrix Converter (VSMC), Ultra Sparse Matrix Converter (USMC) and Inverting Link Matrix Converter (ILMC) where in each iteration it is attempted to reduce the number of semiconductors [16].
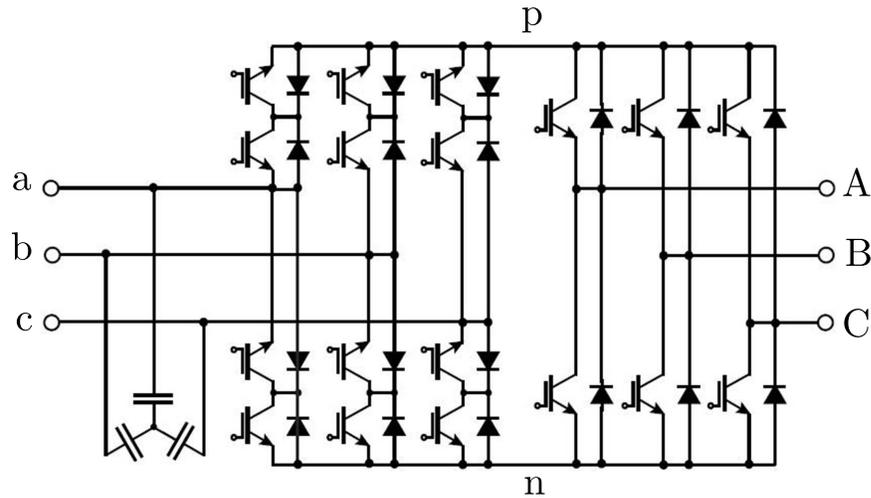
Figure 1.4. Conventional Indirect Matrix Converter.

1.2.3 Conventional Multilevel Voltage Source Converters

For higher power and voltage levels, multilevel converters are normally used as they can provide high voltage output with extremely low distortion and lower dv/dt, while the semiconductor devices only have to tolerate a portion of the DC voltage [17–20]. Multilevel converters use an array of electronic switches to achieve the desired high voltage from a number of available DC voltage levels which may be implemented using capacitors. A voltage balancing strategy is needed to insure that the capacitor voltage maintains at the desired value. Conventional multilevel VSCs can be generally divided into the following three main categories:

1.2.3.1 Diode-Clamped Converter

Diode-Clamped Converter (DCC) employs clamping diodes and cascaded DC capacitors to produce AC voltage waveforms with multiple levels. However, in practice, only the 3-level inverter, often known as Neutral-Point Clamped Converter (NPCC) shown in Fig. 1.5(a), has found industrial applications due to the unequal distribution

of losses among the switches and challenging capacitor voltage balancing for higher number of levels [17, 21–23]. It must be mentioned that, the complexity of the capacitor voltage balancing in DCC is solved in a B2B topology [24], yet it still suffers from high number of components.

(a) Neutral-Point Clamped   (b) Flying Capacitor   (c) Cascaded H-Bridge
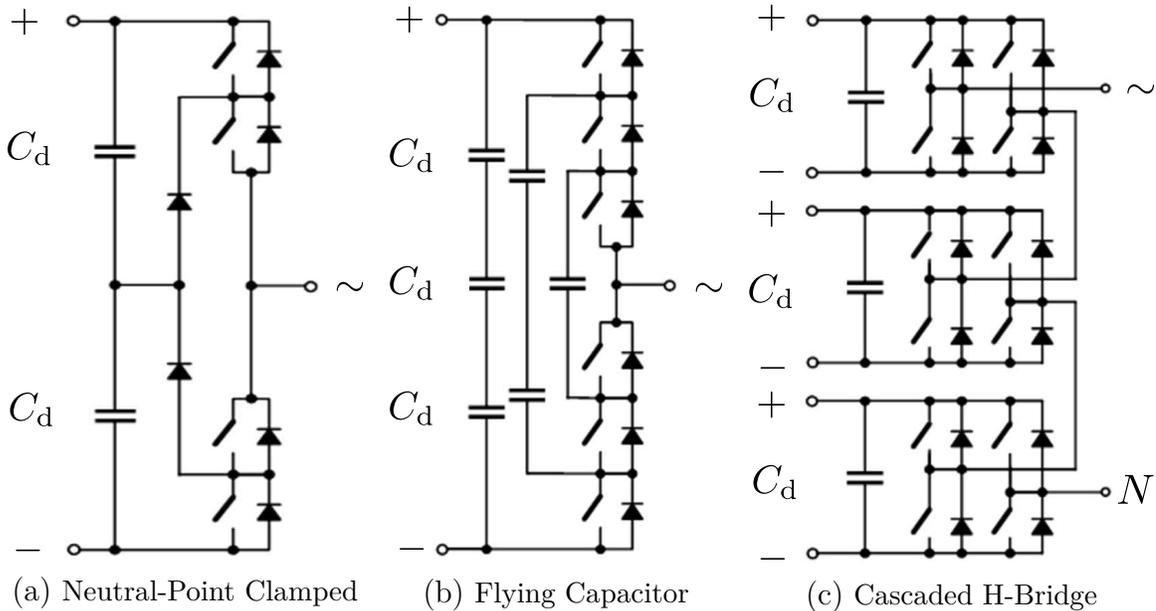
Figure 1.5. Different types of conventional multilevel converters.

1.2.3.2   Flying Capacitor Converter

Flying Capacitor Converter (FCC) consists of multiple pair of switches and capacitors. The schematic diagram of a 4-level FCC is shown in Fig. 1.5(b). All the capacitors are charged at the same voltage. Beside the difficulty of voltage balancing, FCC requires high number of capacitors, since as the number of levels increases, the number of capacitors increases rapidly [17].

1.2.3.3 Cascaded H-Bridge Converter

Cascaded H-Bridge Converter (CHBC) is composed of multiple cascaded H-bridge cells to achieve high voltage levels. The schematic diagram of a 4-level CHBC is shown in Fig. 1.5(c). In order to feed these H-bridge cells, the same number of isolated DC supplies are required which may be obtained from multipulse diode rectifiers. The modularity of CHBC not only makes it more cost-effective, but also facilitates reaching very high voltages. One drawback of this topology is the high number of isolated DC supplies for higher levels of CHBCs [25].

1.2.4 Modular Multilevel Converter

The Modular Multilevel Converter (MMC) is a newer generation of multilevel VSCs which was proposed for in 2003 by Marquardt [26] and first used commercially in the Trans Bay Cable project in San Francisco [27].

1.2.4.1 Principle of Operation

A traditional B2B-MMC is shown in Fig. 1.6 that consists of a number of series Sub-Modules (SMs) with DC capacitors. AC-side voltages are adjusted by changing the number of inserted SMs. The SM insertion/bypassing must be done so that the DC-link voltage remains constant and the capacitor voltages stay close to their desired values. Half-Bridge Sub-Module (HBSM) and Full-Bridge Sub-Module (FBSM) are the most popular SMs shown in Fig. 1.6. Unlike HBSM which only generates 0 and V_{C}, FBSM can produce $-V_{\mathrm{C}}$ as well. Due to the SM capacitor voltage variation and switching transients, the three parallel connected phase units may have different voltages. Thus, for any SM insertion in each arm of the MMC, there must be a SM bypassing in the other arm of the leg simultaneously, so the leg voltage remains

constant. Due to switching transients, the insertion and the bypassing may not happen at the same exact time which results in an increase/decrease in the leg voltage. Therefore, the three parallel connected legs may end up having different voltages. This leads to a circulating current which can flow between the three legs of the converter without affecting the AC-side voltages and currents. The circulating current needs to be minimized in order to reduce the branch losses which can be done by installing a small inductor of proper value in each arm. The details of the design procedure for different components of MMC are discussed in [28].

To sum up, MMC is increasingly attracting attention in different high power applications mainly due to its unique modular structure which can be built up into several hundred levels [27]. Although with such high number of levels, MMC offers
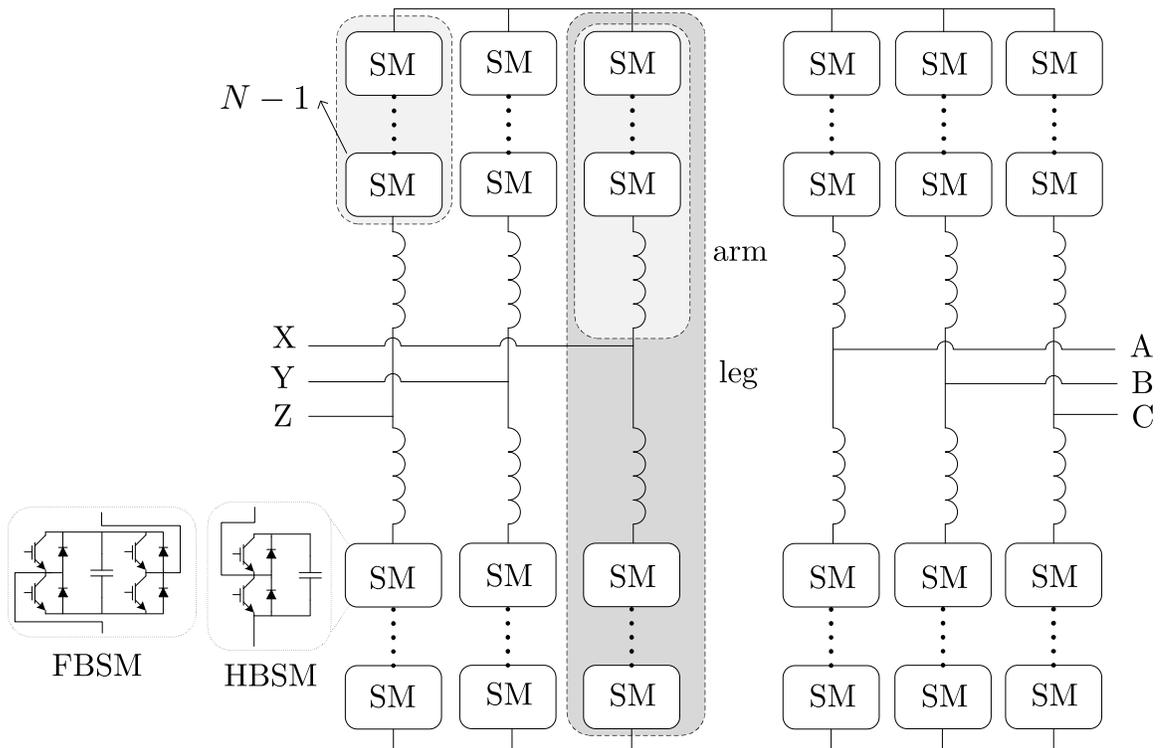
Figure 1.6. Three phase conventional B2B-MMC.

very low-harmonic voltage distortion on its output, yet it requires high number of hard-switched PWM-driven electronic switches. This thesis proposes a number of alternative topologies which offer the same advantages, but they require fewer electronic switches. In addition, the major portion of these switches operate in soft-switching mode.

1.2.4.2   Modulation Techniques

Several modulation techniques have been proposed for multilevel inverters [29]. The high number of switches in an MMC compared to a 2-level VSC, leads to a higher number of possible modulation schemes and more complicated modulation techniques. Modulation techniques for a MMC could be classified in two groups according to their switching frequency as shown in Fig. 1.7:

- Fundamental switching frequency, where each switch has only one commutation per cycle, such as multilevel Selective Harmonic Elimination (SHE), nearest voltage level and nearest vector control methods;

- High switching frequency, where each switch has several commutations per cycle, such as multilevel PWM and Space Vector Modulation (SVM) methods.

   Among different techniques of multilevel converter modulation, multicarrier PWM and Nearest Level Control (NLC) are explained here due to their popularity in multilevel converter modulation.

Multicarrier Pulse Width modulations

   There are two common multicarrier modulations applied to multilevel converters as shown in Fig. 1.7. Phase-shifted PWM is the most commonly used modulation for cascaded multilevel converters as it offers an evenly power distribution among
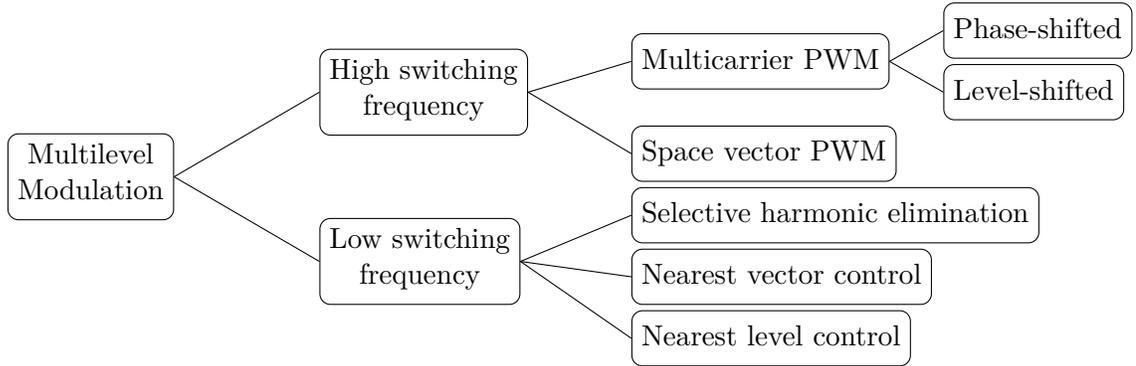
Figure 1.7. Classification of multilevel converter modulation techniques.

cells. This modulation technique shifts the phase of each carrier in a proper angle to reduce the harmonic content of the output voltage. Figure 1.8 shows the modulation waveforms for a MMC arm with three FBSMs.

Nearest Level Control

In NLC technique [30], the nearest voltage level to the desired voltage reference that can be generated by the converter leg would be selected as below:

$$v_\mathrm{a} = \mathrm{round}\left(\frac{v_\mathrm{ref}}{E}\right) \times E. \tag{1.1}$$

The output synthesized voltage is shown in Fig. 1.9. The main advantage of NLC technique is its easier implementation compared to other multilevel modulation techniques. This method is suitable for converters with a high number of levels, since the approximation error becomes significant for converters with a low number of levels which can lead to low-order harmonics at the AC-side.

1.2.4.3 Capacitor Voltage Balancing

In MMC, SMs are constantly inserted into or bypassed out of the phase arms. In order to keep the capacitor voltages as evenly distributed as possible, the proper
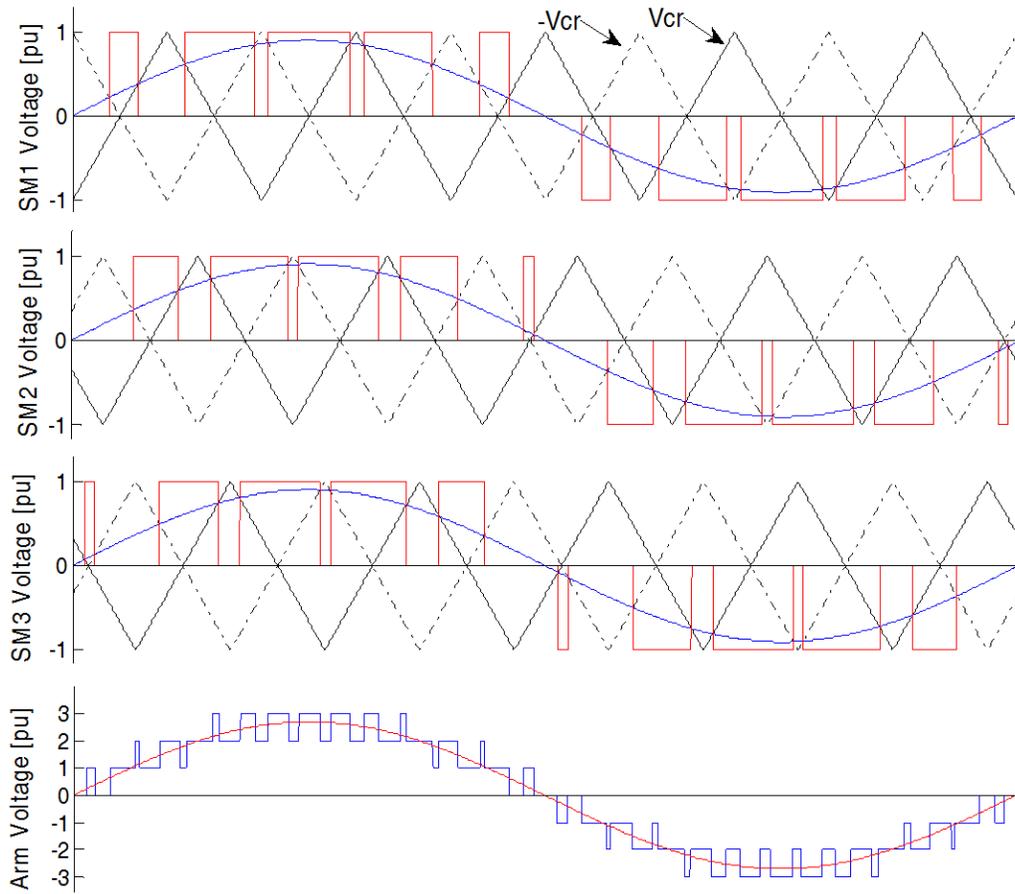
Figure 1.8. Multilevel phase-shifted carrier-based technique.
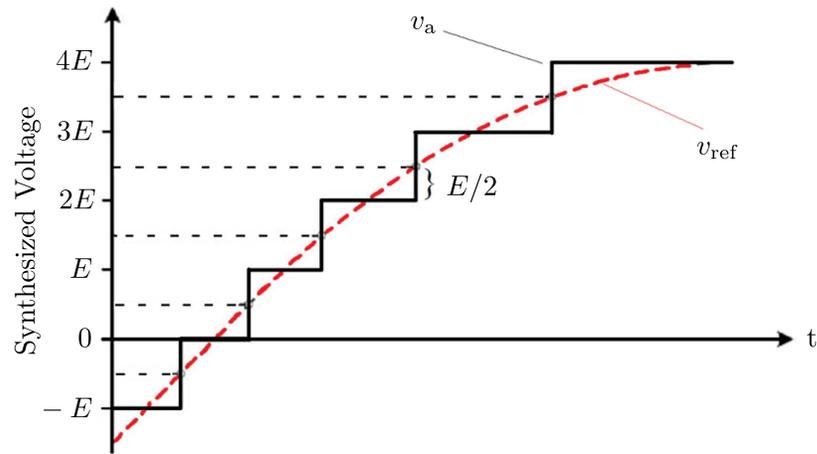
Figure 1.9. Nearest level control technique.

SMs must be selected to operate at any given time. Failure to adequately balance the voltages not only distorts the output voltage but also can result in equipment damage if individual SM voltages fluctuate outside of the rated values of the equipment. The change of a given SM's capacitor voltage is dependent on its inserted/bypassed state, as well as the magnitude and direction of the arm current. When the SM is inserted, the capacitor voltage increases (decreases) if the current is flowing into (out of) the SM. On the other hand, if the SM is bypassed, the capacitor voltage remains unchanged. This fact is shown for both HBSM and FBSM in Figs. 1.10 and 1.11, respectively.
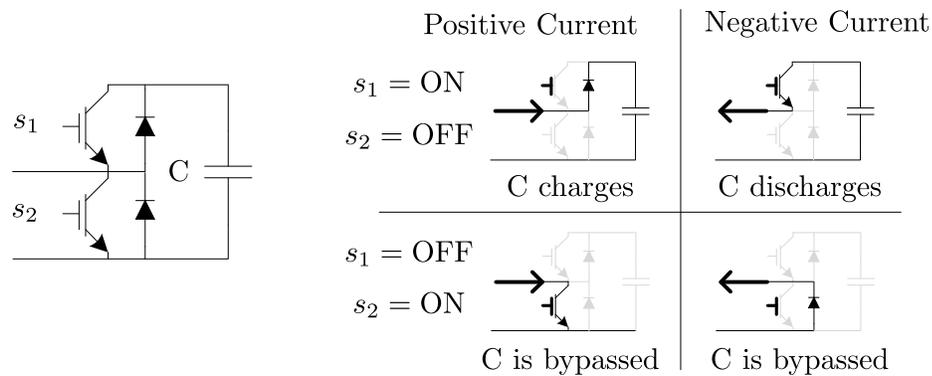
Figure 1.10. Capacitor charging/discharging based on HBSM's status.

The capacitor voltage sorting method in each arm remains the most popular technique for capacitor voltage balancing in MMCs [26, 28, 31]. In this method, first, all capacitor voltages in each arm are sorted and the sign of the arm current is detected. Then, if the arm current is charging the SM capacitors, the SMs with the lowest capacitor voltages are selected to be inserted. Otherwise, if the arm current is discharging the SM capacitors, the SMs with the highest capacitor voltages are selected to be inserted. In other words, by generating a sorted list of SM capacitor
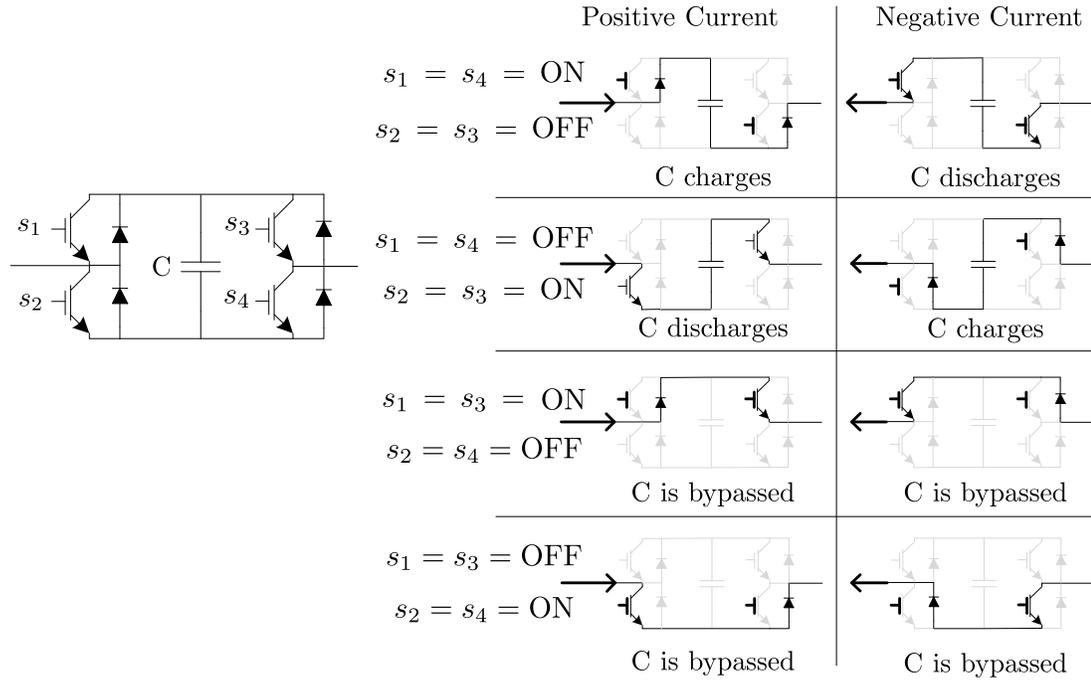
Figure 1.11. Capacitor charging/discharging based on FBSM's status.

voltages and the arm current direction at any time, the ideal SMs to be inserted or bypassed would be identified.

1.3   Description of the Proposed Converters

This dissertation intends to propose a number of novel MMCs for various power transmission systems. These MMCs will offer reduced number of components and increased efficiency, as a major portion of the power switches operate in ZVS mode. Figure 1.12 presents a single-phase version of the first proposed topology called Sparse Modular Multilevel Converter (SMMC) which is intended for HFHW transmission system.

The main leg synthesizes two rectified AC-voltages using its PWM-driven HBSMs and FBSMs, located in Half-Bridge Arm (HBA) and Full-Bridge Arm (FBA), respectively. The frequency of these voltages (v_H & v_F), are independent from each other.
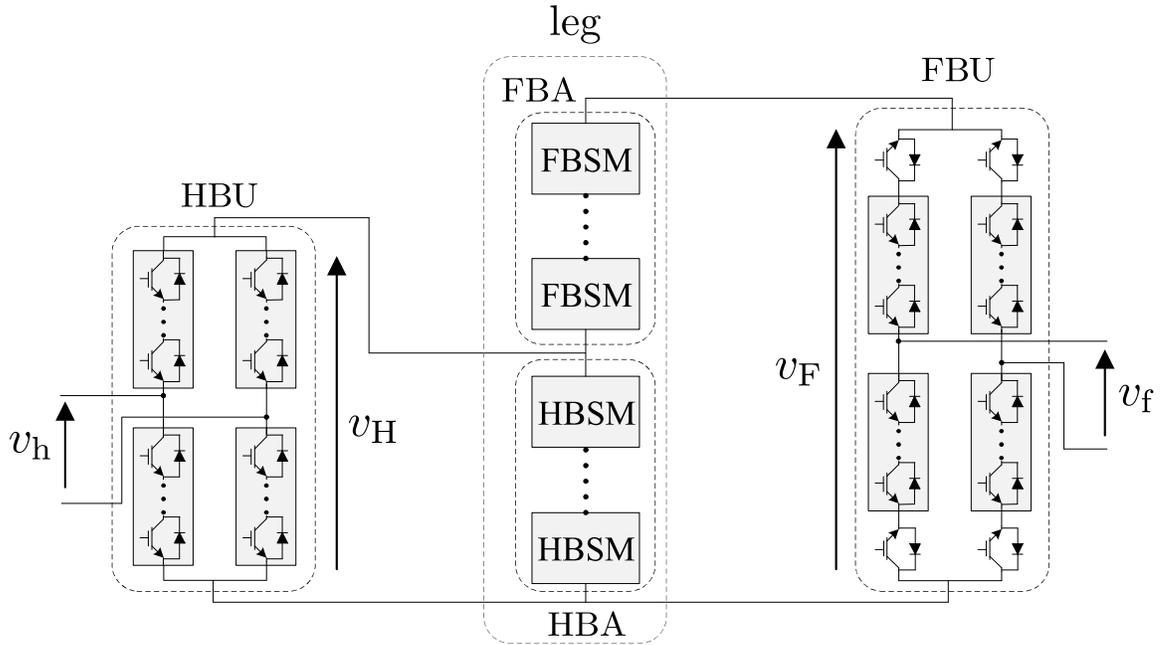
Figure 1.12. Single-phase sparse modular multilevel converter.

Later, two low-frequency and soft-switched unfolders on the converter's sides (Half-Bridge Unfolder (HBU) and Full-Bridge Unfolder (FBU)), would unfold the rectified waveforms every half-cycle, so the full-wave sinusoidal AC-voltages v_h & v_f are constructed in the outputs. It will be shown in Chapter 2 that the proposed SMMC topology is less expensive and less lossy compared to a B2B-MMC. Also, an effective control strategy is proposed for capacitor voltage balancing which is later validated by both simulation and experiment.

The second proposed converter called MinMax Multilevel Converter (MMMC) is also suitable for AC/AC systems such as HFHW. The MMMC further reduces the number of hard-switched power switches by employing an additional soft-switched unfolder. In Chapter 3, this topology is studied in detail. In Chapter 4, the economical aspect of HFHW system is discussed and it is shown that this transmission system

can benefit from employing the proposed converters. Finally, in Chapter 5, a high-gain MMC called Series Hybrid Modular Multilevel Converter (SHMMC) is proposed for HVDC systems. Similar to the other proposed converters, a major portion of the power switches in SHMMC operate in low-frequency and soft-switching mode.

1.4 Thesis Objectives

The main objective of this thesis is to introduce suitable MMC topologies for various power transmission systems. In these converters, the number of power switches are reduced and the major portion of them operate in soft-switching mode. Beside the theoretical studies, the viability of the proposed topologies, as well as the effectiveness of the control strategy will be confirmed by both simulation and experiment. Briefly, the dissertation's objectives are:

(i) To propose a novel AC/AC MMC for HFHW transmission system, which utilizes fewer power switches compared to conventional MMC and to have switches operating in soft-switching mode;

(ii) To propose another AC/AC MMC for HFHW system, which achieves more switches operating in soft-switching mode;

(iii) To propose a high-gain MMC for HVDC systems, which requires fewer power switches compared to MMC and similar to other proposed converters, the majority of its switches operate in soft-switching mode;

(iv) To propose control strategies for the proposed topologies which regulate the AC-sides active and reactive powers and also guarantee the capacitor voltage balancing in both steady-state and transient conditions;

(v) To study the economical aspect of HFHW power transmission system and compare the utilization of the proposed topologies with conventional approaches.

(vi) To experimentally test the proposed topologies and their associated control strategies.

1.5   Thesis Outline

Based on flow of the contribution and number of the proposed converters, this dissertation is divided into six chapters as follows:

Chapter 2 introduces a new topology of AC/AC converters called SMMC suitable for the HFHW transmission system. The advantages of SMMC compared to conventional MMC and its control strategy are then presented. At the end, the feasibility of SMMC is validated by simulation and experimental results.

Chapter 3 presents another novel topology of MMCs intended for AC/AC power transmission systems such as the HFHW system. The proposed topology further reduces the number of PWM-driven power switches and replace them with low-frequency soft-switched switches, and it is called MMMC. A control strategy is designed to ensure the capacitor voltage balancing of the converter. At the end, the feasibility of MMMC is validated by simulation and experimental results.

Chapter 4 discusses the economical aspects of the HFHW power transmission system. It is shown how the HFHW system could benefit from uitlizing the proposed AC/AC topologies.

Chapter 5 proposes a high-gain MMC called SHMMC which is intended for HVDC systems. The SHMMC provides a DC-link voltage almost 3.33 higher than AC-side Root-Mean-Square (RMS)-voltage which makes it very attractive for HVDC

applications. The feasibility of SHMMC, as well as the effectiveness of the control strategy are validated by simulation and experimental results.

Chapter 6 summarizes the work that is presented and suggests topics for future research.

Chapter 2

Sparse Modular Multilevel Converter

2.1   Introduction

In this chapter, a novel topology of MMCs is introduced for high power AC/AC systems. The Fractional Frequency Transmission System (FFTS) is an example that uses lower frequency ($50/3$ Hz) to reduce the line reactance, and thus to increase its capacity. This transmission system has been used in European railway electrification systems for almost a century [32, 33]. In the last few decades, novel static AC/AC frequency converters are proposed to reduce the weight and losses in traction propulsion systems which has resulted in a lower cost and more efficient system [34–36]. Another example is the HFHW power system which transfers the power in a higher

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frequency and requires an AC/AC converter at its receiving-end to connect to the 60 Hz power grid [1].

The proposed converter in this chapter has fewer power switches and capacitors compared to a B2B-MMC, and in addition, 57% of the switches operate in soft switching mode, which considerably decreases the converter losses. Moreover, a control strategy is developed and evaluated with both simulations and experiment which guarantees the capacitor voltage balancing for this converter.

2.2 Principle of Operation

Figures 2.1 and 2.2 show the schematic diagram of single-phase and 3-phase versions of the proposed topology.
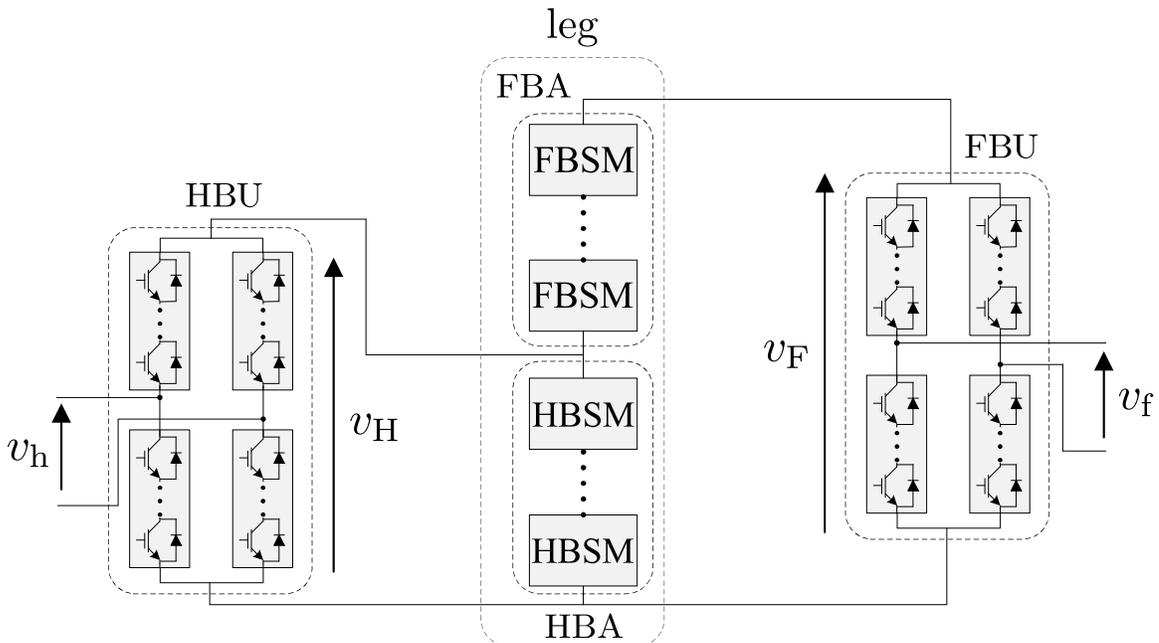
Figure 2.1. Schematic diagram of a single-phase n-level SMMC.

Compared to a B2B-MMC (see Fig. 1.6), this topology consists of a reduced number of components and therefore, it is called Sparse Modular Multilevel Converter
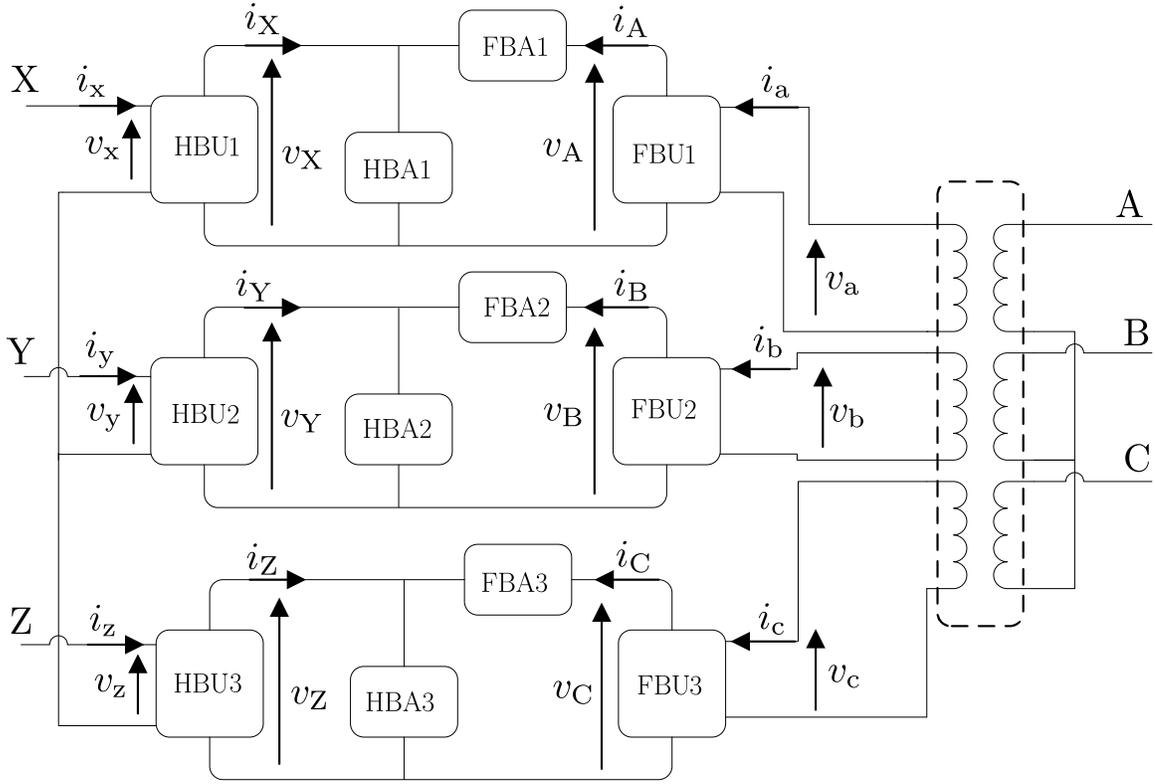
Figure 2.2. Schematic diagram of a three-phase SMMC.

(SMMC). The SMMC consists of three separate stages including Half-Bridge Unfolder (HBU) and Full-Bridge Unfolder (FBU) on the sides and one main leg. The main leg consists of Half-Bridge Arm (HBA) and Full-Bridge Arm (FBA) which are built by a number of cascaded HBSMs and FBSMs, respectively. By inserting/by-passing the proper number of SMs in HBA and FBA, the desired voltage on both sides of the converter can be achieved. The unfolders are employed to apply the arm voltage or its reverse to v_f or v_h. Therefore, the absolute value of AC-side voltages are provided by operating the desired number of SMs, while their polarity are controlled by the unfolders in both sides. In the 3-phase SMMC, utilizing an isolating 3-phase transformer is essential, otherwise, SM capacitors might get shorted in some switching states (as an example, see Fig. 2.3). In Fig. 2.1, the Half-Bridge (HB)-side voltage v_H
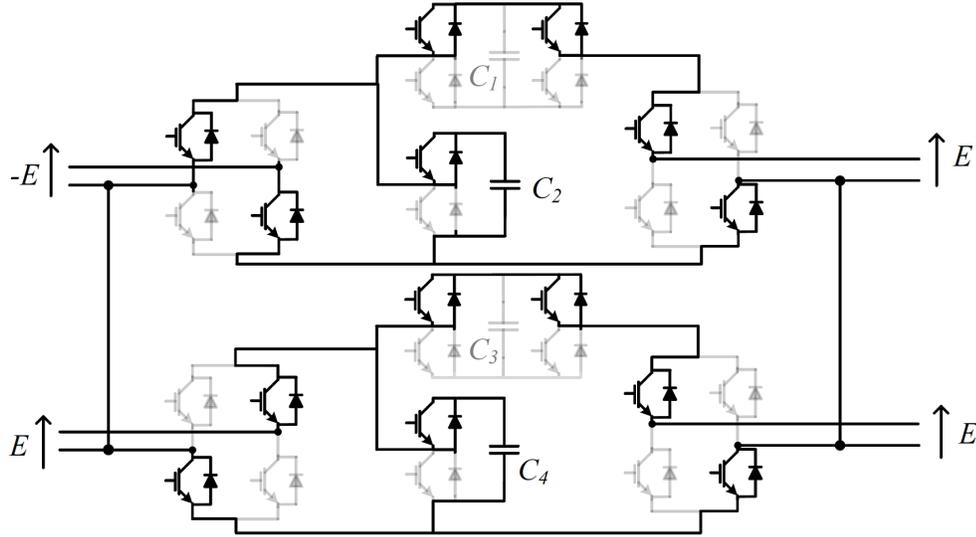
Figure 2.3. Shorting capacitor C_2 without using isolating transformer.

is the summation of inserted HBSMs in HBA which is a non-negative value as well as independent from FBA voltage. However, the Full-Bridge (FB)-side voltage v_F is the summation of both HBA and FBA voltages. When $v_\text{H} \neq v_\text{F}$, a proper number of inserted FBSMs would generate the voltage difference. In an n-level SMMC, the number of HBSMs and FBSMs are equal to $(n-1)/2$; so that all desired non-negative values of v_H and v_F can be generated.

Unlike MMC, there is no circulating current between different legs (phases) of SMMC, as they are isolated from each other by a 3-phase transformer. However, it is inherently possible for current to circulate inside one phase of the SMMC. This current is not continuous and only may flow when v_F crosses zero, and so it is called zero-crossing circulating current. For example, in Fig. 2.4, if $V_\text{C3} + V_\text{C4}$ is slightly smaller than $V_\text{C1} + V_\text{C2}$, it causes v_F to become a small negative value (when $v_\text{F} = 0$ is required). In addition, due to switching transients, the SM insertion/bypassing may not occur simultaneously. This leads to one extra level decrease/increase in v_F for a short period of time. An extra level decrease in v_F (when $v_\text{F} = 0$ is required), could
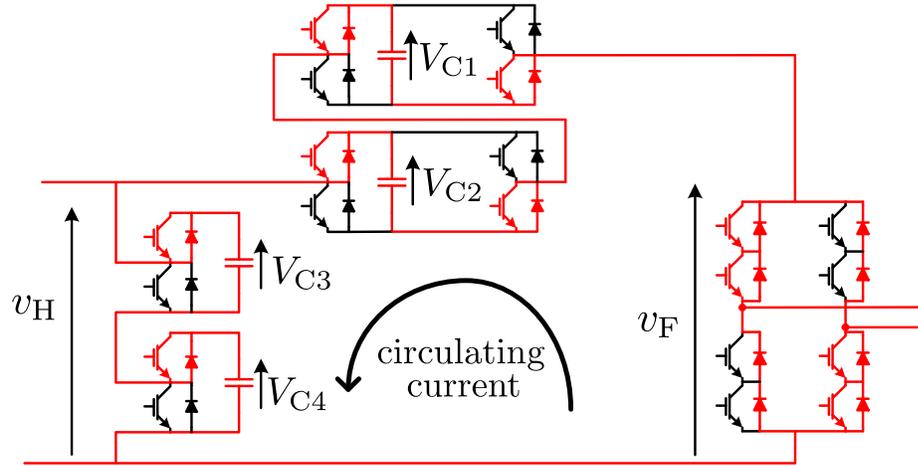
Figure 2.4. Zero-crossing circulating current in 5-level SMMC.
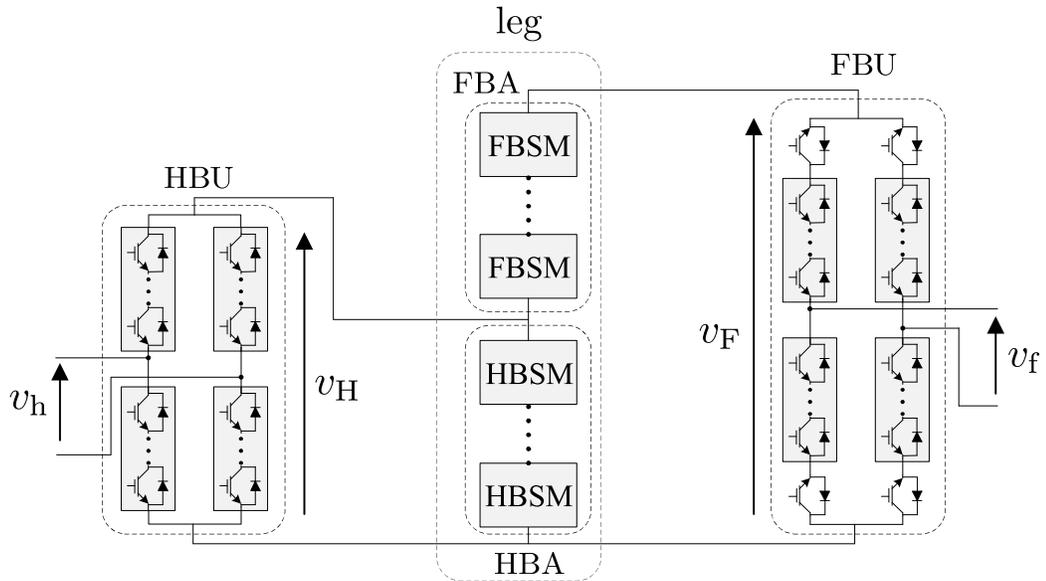
Figure 2.5. Schematic diagram of SMMC with modified FBU.

make v_F negative. This negative voltage turns on the unfolder's anti-parallel diodes and current circulates through the leg.

Adding one reversed Insulated-Gate Bipolar Transistor (IGBT) in each arm of the FBU as shown in Fig. 2.5, could block the possible small negative v_F. The HBU remains intact. It should be noticed that the maximum voltage-drop across

the reversed IGBT occurs, when HBA and FBA capacitors are in their lowest and highest acceptable voltages, respectively. Therefore, this IGBT must withstand the predefined capacitor voltage ripple, ΔV_{ripp} multiplied by the number of HBSMs (or FBSMs) which equals to $(n-1)/2 \times \Delta V_{\text{ripp}}$. This implies that in case of high number of levels, more than one reversed IGBT might be required. Figure 2.6 demonstrates FBU's principle of operation at voltage zero-crossing transition for both cases of leading and lagging currents. Note that here only the right leg of the unfolder is shown. It can be seen that at any stage of unfolding transition, there is at least one reversed IGBT blocking the zero-crossing circulating current.

Table 2.1 compares an n-level B2B-MMC with the alternative SMMC based on the number of main components. The multiple number of IGBTs for the unfolder valves is taken into account in the calculation. This converter also offers ZVS for more than half of its semiconductors which later on will be used for voltage sharing of series-connected semiconductors.

Table 2.1.
COMPARISON OF MMC AND SMMC COMPONENT COUNT

	1-Phase		3-Phase	
Quantity	MMC	SMMC	MMC	SMMC
Capacitor	$8(n-1)$	$(n-1)$	$12(n-1)$	$3(n-1)$
Inductor	8	0	12	0
High-frequency & hard-switched IGBT	$16(n-1)$	$3(n-1)$	$24(n-1)$	$9(n-1)$
Line-frequency & soft-switched IGBT	0	$4n$	0	$12n$

2.2.1 Demonstration of a Single-phase 5-Level SMMC

The main leg of a 5-level SMMC is shown in Fig. 2.7 to be studied in detail. For the sake of simplicity, all capacitor voltages are assumed to be regulated at voltage E. Switching function $d_i(i = 11, 12, 21, 22, 3, 4)$ is defined so that $d_i = 1$, when upper

Table 2.2.
VALID SWITCHING STATES OF A 5-LEVEL SMMC

Switching state	d_{11}	d_{12}	d_{21}	d_{22}	d_3	d_4	V_1	V_2
1	0	0	0	0	0	0	0	0
	0	0	1	1	0	0		
	1	1	0	0	0	0		
	1	1	1	1	0	0		
2	1	0	0	0	0	0	E	0
	1	0	1	1	0	0		
	0	0	1	0	0	0		
	1	1	1	0	0	0		
3	1	0	1	0	0	0	$2E$	0
4	0	1	0	0	1	0	0	E
	0	1	1	1	1	0		
	0	0	0	0	1	0		
	1	1	1	1	1	0		
	0	1	0	0	0	1		
	0	1	1	1	0	1		
	0	0	0	0	0	1		
	1	1	1	1	0	1		
5	0	0	0	0	1	0	E	E
	0	0	1	1	1	0		
	1	1	0	0	1	0		
	1	1	1	1	1	0		
	0	0	0	0	0	1		
	0	0	1	1	0	1		
	1	1	0	0	0	1		
	1	1	1	1	0	1		
6	1	0	0	0	1	0	$2E$	E
	1	0	1	1	1	0		
	0	0	1	0	1	0		
	1	1	1	0	1	0		
	1	0	0	0	0	1		
	1	0	1	1	0	1		
	0	0	1	0	0	1		
	1	1	1	0	0	1		
7	0	1	0	1	1	1	0	$2E$
8	0	1	0	0	1	1	E	$2E$
	0	1	1	1	1	1		
	0	0	0	1	1	1		
	1	1	0	1	1	1		
9	0	0	0	0	1	1	$2E$	$2E$
	0	0	1	1	1	1		
	1	1	0	0	1	1		
	1	1	1	1	1	1		
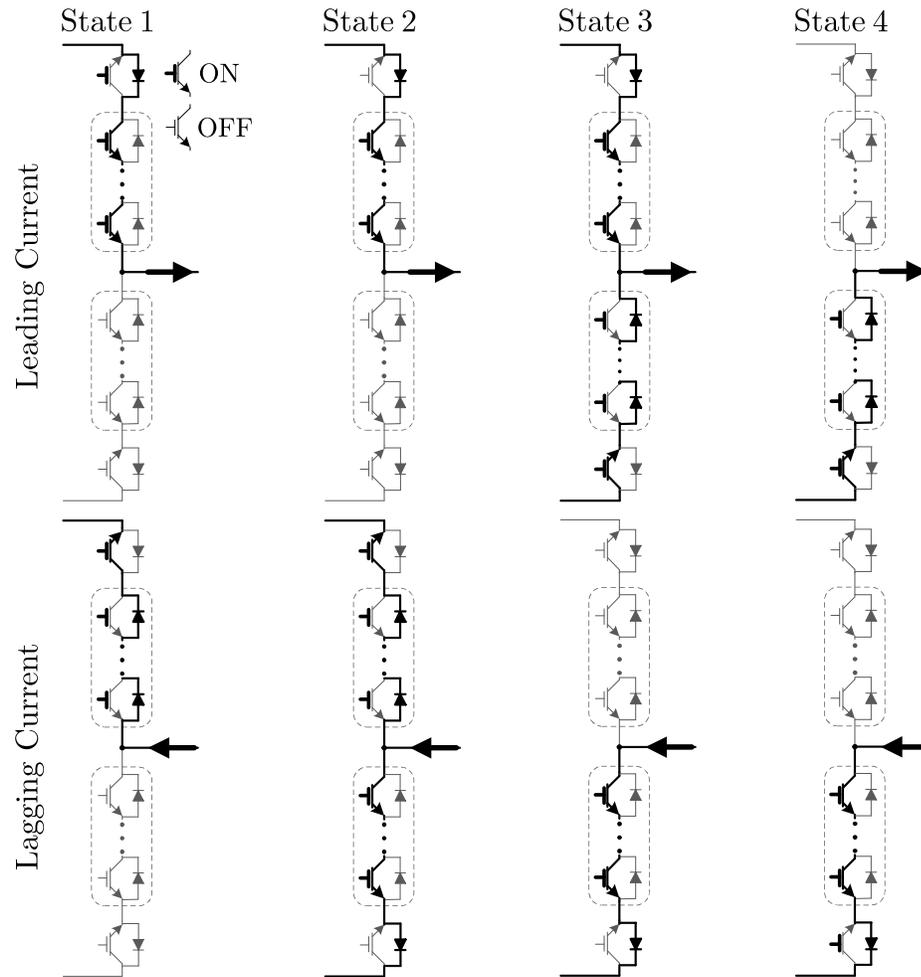
Figure 2.6. Description of zero-crossing transition in FBU.

switch of the SM is ON and the lower switch is OFF and $d_i = 0$, for the reverse case. Table 2.2 lists all the valid switching states for the main leg of 5-level SMMC. Note that for many of these states, there are several redundancies and also all desired voltages for V_1 and V_2 could be provided independent from each other. As an example, the switching states 4-6 are illustrated in Fig. 2.8.

2.2.2 ZVS of SMMC Unfolders

Since the HBA and FBA arms operate with a voltage higher than the available switch ratings, several switches are connected in series to tolerate the desired voltage. Thus, steady-state and transient voltage sharing between the series switches need to be ensured, since most power semiconductors do not hold voltages above their rating and their recovery characteristics differ even within the same type and manufacturer. The steady-state voltage sharing can be achieved by installing high-value parallel resistors. Generally, additional circuitry has to be provided to ensure equal transient voltage sharing. Here, there is no need for extra components, since all the switchings in the unfolders occur in ZVS regardless of the operating condition. Figure 2.9 shows the HBU switching transition.

In case of lagging current, shown in Fig. 2.10(a), the turn on gate signals are set for S_{1a} and S_{4a} at time instant of t_0. However, they will not start conducting until
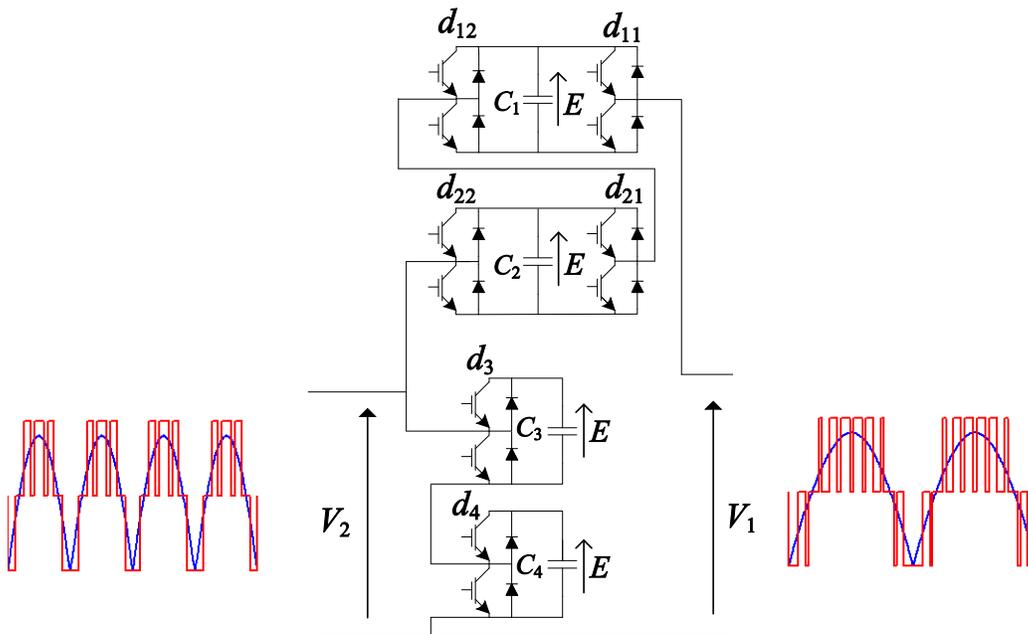
Figure 2.7. Schematic diagram of a 5-level SMMC leg.

(a) state #4: $V_1 = 0, V_2 = E$

(b) state #5: $V_1 = V_2 = E$

(c) state #6: $V_1 = 2E, V_2 = E$
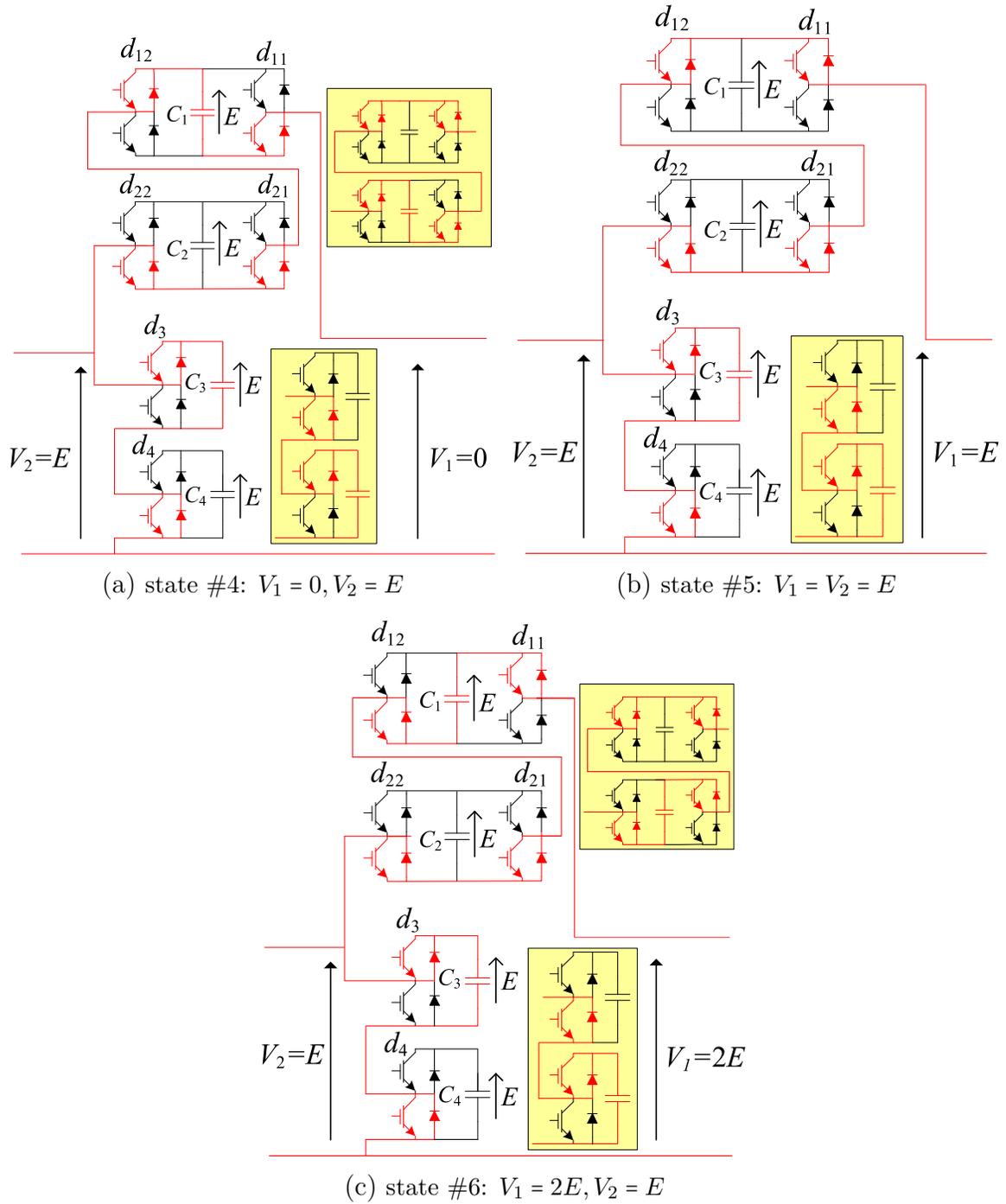
Figure 2.8. Illustration of switching states 4-6 in a 5-level SMMC
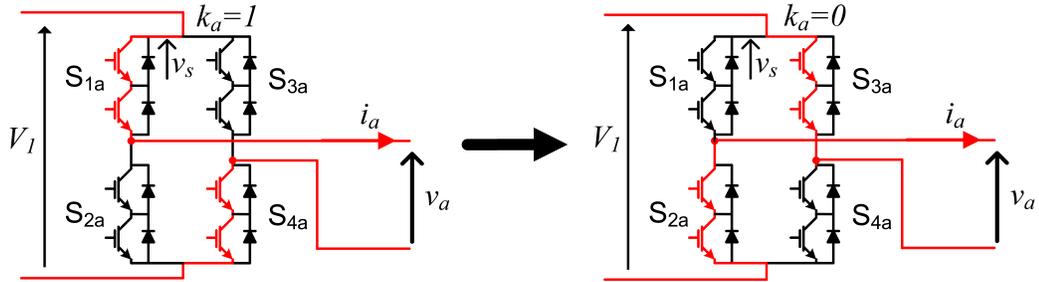
Figure 2.9. Schematic diagram of HBU switching transition.
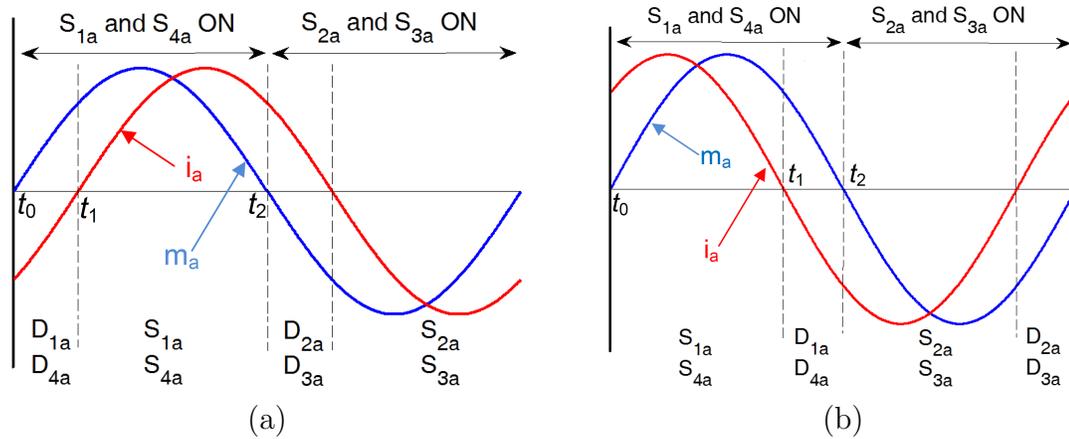
Figure 2.10. Unfolder transition (a) lagging current (b) leading current.

the current i_a crosses zero and becomes positive at time instant of t_1 causing a Zero Current Switching (ZCS). From t_0 to t_1, D_{1a} and D_{4a} are ON which forces the voltage across S_{1a} and S_{4a} to be close to zero before turning on causing a ZVS. Thus, S_{1a} and S_{4a} are experiencing both ZVS and ZCS at turn on in case of lagging current. At time instant of t_2, the turn off gate signals are set for S_{1a} and S_{4a}, however due to their different gating characteristics, they may not turn off at the exact same time. In this situation, in a valve including n series IGBTs, the one which turns off first, will experience the full voltage of the series string. Here, this voltage is $n \times v_{\text{IGBT-ON}}$, since the current i_a is commutating from S_{1a} and S_{4a} to D_{2a} and D_{3a}. Because this voltage is still negligible compared to an IGBT's blocking voltage, it can be concluded that

S_{1a} and S_{4a} are experiencing ZVS at turn off in case of lagging current. Similarly, S_{2a} and S_{3a} are experiencing both ZVS and ZCS at turn on and ZVS at turn off when the current is lagging.

In case of a leading current (see Fig. 2.10(b)), the turn on gate signals are set for S_{1a} and S_{4a} at time instant of t_0. However, due to their different gating characteristics, they may not turn simultaneously. In this case, in a string of n series IGBTs, the one which turns on last will experience the full voltage of the string. Here, this voltage is $n \times v_{D-ON}$, since the current i_a is commutating from D_{2a} and D_{3a} to S_{1a} and S_{4a}. Because this voltage is still negligible compared to an IGBT's blocking voltage, it can be concluded that S_{1a} and S_{4a} are experiencing ZVS at turn on in case of a leading current. At time instant of t_2, the turn off gate signals are set for S_{1a} and S_{4a}. As the current i_a becomes negative and flows through D_{1a} and D_{4a} at time instant of t_1, S_{1a} and S_{4a} are experiencing both ZVS and ZCS at turn off in case of a lagging current. Similarly, S_{2a} and S_{3a} are experiencing ZVS at turn on and both ZVS and ZCS at turn off when the current is lagging.

Since ZVS occurs in the unfolders for all operating conditions, voltage across the valve is small when gate pulses are applied and even if the gate pulses come at different times, maximum voltage during transient will not exceed the device rating. Therefore, without any extra circuitry, a limited maximum transient voltage sharing is achieved in the unfolders.

2.2.3 Unidirectional SMMC

Figure 2.11 shows a HFHW system operating in 180 Hz. It must be noted that this system is unidirectional and the active power always flow from the high-frequency generator to the 60 Hz grid. Thus, the proposed converter could be modified to

operate in unidirectional mode. This unidirectional SMMC is derived from the original SMMC by using diode-bridge front unfolder as shown in Figure 2.12. Table 2.3 presents the comparison of these two AC/AC converters in terms of the number of different components.
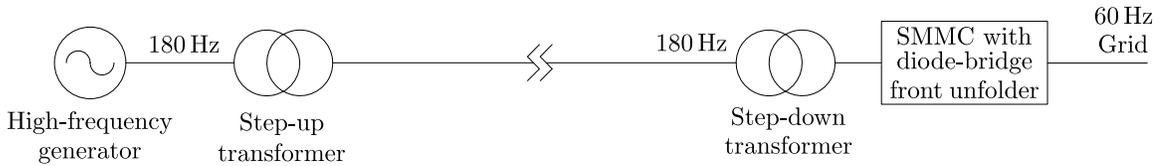
Figure 2.11. High frequency half-wavelength transmission scheme with unidirectional SMMC.
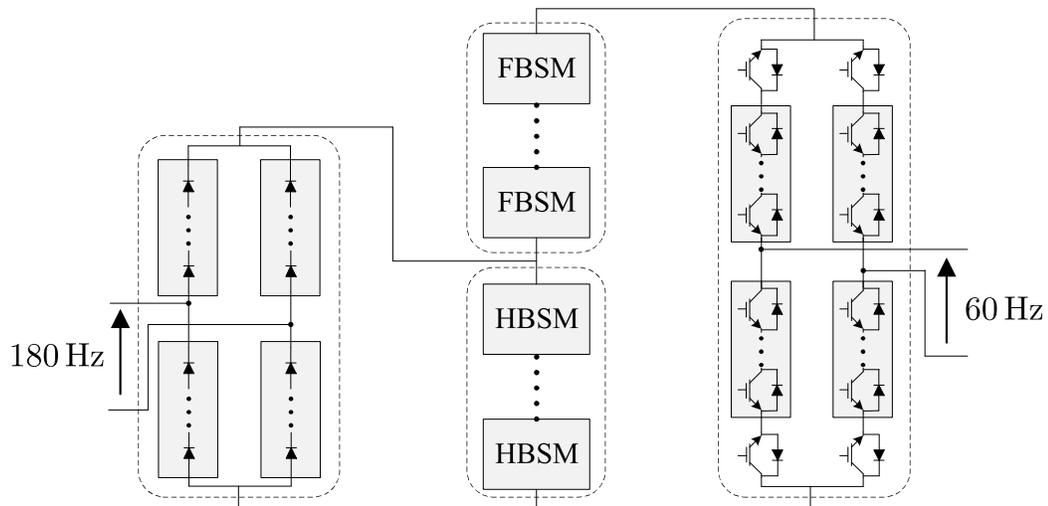
Figure 2.12. One phase of unidirectional SMMC with diode-bridge front unfolder.

In must be noted that although, the modified SMMC utilizes a diode-bridge in the front-end, it does not inject any harmonic to the AC-side. To compare this topology with alternative MMC-based converter, a HFHW system operating in 180 Hz is presented in Fig. 2.13. Table 2.3 presents the comparison of these two AC/AC converters in terms of the number of different components.
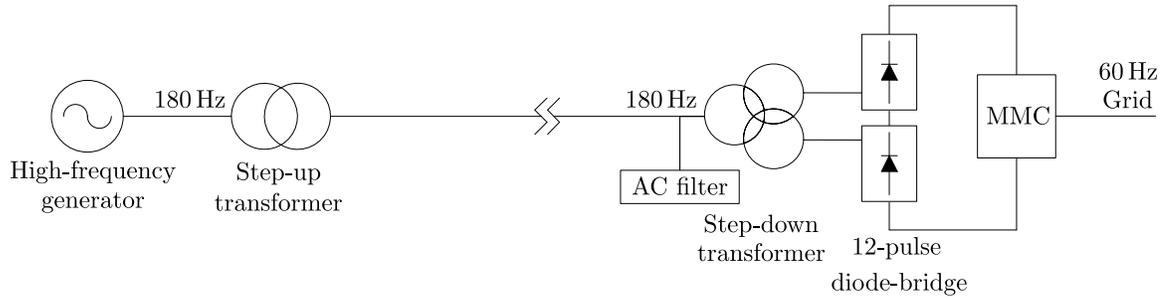
Figure 2.13. High frequency half-wavelength transmission scheme with MMC.

Table 2.3.
COMPONENT COUNT OF TWO CONVERTERS FOR HFHW SCHEME.

	Diode-bridge Rectifier + MMC	SMMC with diode-bridge front-end
Diode	$6(n-1)$	$6(n-1)$
IGBT[†]	$12(n-1)$	$9(n-1)$
IGBT[‡]	0	$6(n+1)$
Capacitor	$6(n-1)$	$3(n-1)$
AC filter	Required	Not Required
Step-down transformer	Special	Conventional

[†] High-frequency & hard-switched
[‡] Line-frequency & soft-switched

2.3   Capacitor Voltage Balancing

Figure 2.14 shows the simplified schematic diagram of a single-phase SMMC.
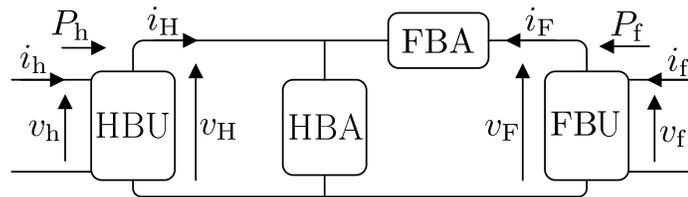
Figure 2.14. Simplified schematic diagram of a single-phase SMMC.

The voltages and currents on FB- and HB-sides of the converter can be represented as:

$$\begin{cases} v_{\mathrm{f}} = V_{\mathrm{mf}}\sin(\omega_{\mathrm{f}}t) \quad, \quad v_{\mathrm{F}} = \lambda_{\mathrm{f}}.v_{\mathrm{f}} \\[2mm] i_{\mathrm{f}} = I_{\mathrm{mf}}\sin(\omega_{\mathrm{f}}t - \varphi_{\mathrm{f}}) \quad, \quad i_{\mathrm{F}} = \lambda_{\mathrm{f}}.i_{\mathrm{f}} \\[2mm] \lambda_{\mathrm{f}} = \mathrm{sign}(v_{\mathrm{f}}) = \mathrm{sign}(\sin(\omega_{\mathrm{f}}t)) \end{cases} \tag{2.1}$$

$$\begin{cases} v_{\mathrm{h}} = V_{\mathrm{mh}}\sin(\omega_{\mathrm{h}}t + \theta_{\mathrm{h}}) \quad, \quad v_{\mathrm{H}} = \lambda_{\mathrm{h}}.v_{\mathrm{h}} \\[2mm] i_{\mathrm{h}} = I_{\mathrm{mh}}\sin(\omega_{\mathrm{h}}t + \theta_{\mathrm{h}} - \varphi_{\mathrm{h}}) \quad, \quad i_{\mathrm{H}} = \lambda_{\mathrm{h}}.i_{\mathrm{h}} \\[2mm] \lambda_{\mathrm{h}} = \mathrm{sign}(v_{\mathrm{h}}) = \mathrm{sign}(\sin(\omega_{\mathrm{h}}t + \theta_{\mathrm{h}})). \end{cases} \tag{2.2}$$

The instantaneous power going through FBA and HBA are calculated as:

$$p_{\mathrm{HB}}(t) = (i_{\mathrm{F}} + i_{\mathrm{H}}) \times v_{\mathrm{H}} \quad, \quad p_{\mathrm{FB}}(t) = i_{\mathrm{F}} \times (v_{\mathrm{F}} - v_{\mathrm{H}}). \tag{2.3}$$

In the steady state condition, the stored energy of FBA and HBA must be constant, so the capacitor voltages remain unchanged. This leads to the following equations:

$$\int_{T} p_{\mathrm{HB}}(t).dt = 0 \quad, \quad \int_{T} p_{\mathrm{FB}}(t).dt = 0. \tag{2.4}$$

The above equation can be rewritten as below voltage balancing criteria:

$$\left. \begin{array}{r} \int_{T}\big(p_{\mathrm{FB}}(t) + p_{\mathrm{HB}}(t)\big).dt = 0 \\[3mm] \int_{T} p_{\mathrm{FB}}(t).dt = 0 \end{array} \right\} \text{voltage balancing criteria.} \tag{2.5}$$

The first criterion leads to the real power balance between the AC-sides as pre-sented below:

$$
\begin{aligned}
0 &= \int_T \Big(p_{\mathrm{FB}}(t) + p_{\mathrm{HB}}(t)\Big).dt \\
&= \int_T (i_{\mathrm{F}} \times v_{\mathrm{F}} + i_{\mathrm{H}} \times v_{\mathrm{H}}).dt \\
&= \frac{1}{2} V_{\mathrm{mf}} I_{\mathrm{mf}} \cos(\varphi_{\mathrm{f}}) + \frac{1}{2} V_{\mathrm{mh}} I_{\mathrm{mh}} \cos(\varphi_{\mathrm{f}}) \\
&\Rightarrow P_{\mathrm{f}} + P_{\mathrm{h}} = 0.
\end{aligned}
\tag{2.6}
$$

The second criterion is studied as:

$$
\begin{aligned}
0 &= \int_T p_{\mathrm{FB}}(t).dt \\
&= \int_T \{i_{\mathrm{F}} \times (v_{\mathrm{F}} - v_{\mathrm{H}})\}.dt \\
&= \frac{1}{2} V_{\mathrm{mf}} I_{\mathrm{mf}} \cos(\varphi_{\mathrm{f}}) - \int_T (i_{\mathrm{F}} \times v_{\mathrm{H}}).dt \\
&\Rightarrow \frac{1}{2} V_{\mathrm{mf}} I_{\mathrm{mf}} \cos(\varphi_{\mathrm{f}}) = V_{\mathrm{mh}} I_{\mathrm{mf}} \int_T \{\lambda_f \sin(\omega_f t - \varphi_{\mathrm{f}}) |\sin(\omega_{\mathrm{h}} t + \theta_{\mathrm{h}})|\}.dt
\end{aligned}
\tag{2.7}
$$

This can be rewritten as:

$$
\begin{aligned}
\mathrm{VG} &= \frac{V_{\mathrm{mf}}}{V_{\mathrm{mh}}} = \int_T \frac{2\lambda_{\mathrm{f}} \sin(\omega_f t - \varphi_{\mathrm{f}}) |\sin(\omega_{\mathrm{h}} t + \theta_{\mathrm{h}})|}{\cos(\varphi_{\mathrm{f}})}.dt \\
&= \int_T g(t).dt - \int_T h(t).dt, \\
g(t) &= 2 |\sin(\omega_f t) \sin(\omega_{\mathrm{h}} t + \theta_{\mathrm{h}})|, \\
h(t) &= 2\lambda_{\mathrm{f}} \cos(\omega_f t) \tan(\varphi_{\mathrm{f}}) |\sin(\omega_{\mathrm{h}} t + \theta_{\mathrm{h}})|.
\end{aligned}
\tag{2.8}
$$

There is no analytical solution for Eq. (2.8). However, its numerical solution can be approximated as:

$$G = \int_T g(t) \approx 0.81 + A_1 \cos(B.\theta_\mathrm{h}) \tag{2.9}$$

$$H = \int_T h(t) \approx A_2 \tan(\varphi_\mathrm{f}) \sin(B.\theta_\mathrm{h}), \tag{2.10}$$

where, A_1 and A_2 are positive real numbers which only depend on the frequency ratio $(\omega_\mathrm{h}/\omega_\mathrm{f})$ as shown in Fig. 2.15.
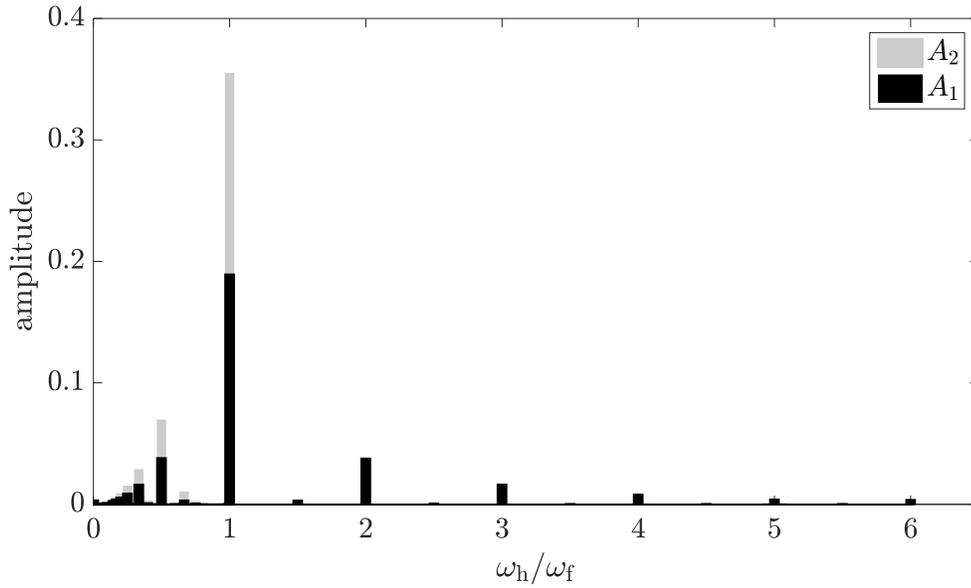
Figure 2.15. The value of A_1 and A_2 based on $\omega_\mathrm{h}/\omega_\mathrm{f}$.

By substituting Eqs. (2.9) and (2.10) in Eq. (2.8):

$$\mathrm{VG} = \frac{V_\mathrm{mf}}{V_\mathrm{mh}} = 0.81 + A_1 \cos(B\theta_\mathrm{h}) - A_2 \tan(\varphi_\mathrm{f}) \sin(B\theta_\mathrm{h}). \tag{2.11}$$

Finally, the voltage balancing criteria can be summarized as:

$$
\begin{cases}
P_\mathrm{f} + P_\mathrm{h} = 0 \\
\mathrm{VG} = \dfrac{V_\mathrm{mf}}{V_\mathrm{mh}} = 0.81 + A_1 \cos(B\theta_\mathrm{h}) - A_2 \tan(\varphi_\mathrm{f}) \sin(B\theta_\mathrm{h})
\end{cases}
\tag{2.12}
$$

2.3.1 The Impact of Frequency Ratio

Assume the AC-side frequencies are not an integer multiple of each other ($\omega_\mathrm{h}/\omega_\mathrm{f} \neq n$ or $1/n$ where n is an integer number). In this case, as it is shown in Fig. 2.15, A_1 and A_2 are constant and almost equal to 0. For instance, if the converter is working between two grids with the frequencies of 50 and 60 Hz, $A_1 = 0.00014$ and $A_2 = 0.00279$. Assuming that v_f side is not purely inductive, by substituting A_1 and A_2 in Eq. (2.11):

$$
M \approx 0 \Rightarrow \mathrm{VG} \approx 0.81.
\tag{2.13}
$$

Thus, VG is equal to 0.81 regardless of the frequency ratio. According to Eq. (2.11), even if the frequency ratio is a small integer number, the voltage gain would still be constant, but also could be affected by AC-sides power factor and phase-angle. In other words, if voltage balancing is achieved, the gain of the converter is always fixed. In the next section, third harmonic injection is proposed to regulate the converter gain, regardless of the frequency ratio.

2.3.2 Voltage Gain Adjustment

For many practical applications, voltage gain control is vital. For example, in grid-connected application, voltage gain can be used to adjust the reactive power exchange

with the AC networks. The AC-side voltages can be controlled by injecting harmonics, such that the ratio between the average rectified AC voltage and its fundamental component is adjusted. In this process, the unfolders are preferred to retain the soft switched operation. In general, both sides of the converter can contribute to the voltage gain control by admitting an infinite series of harmonics. However, the added harmonics should be chosen such that they are cancelled out in line-line voltages. In other words, only odd multiples of three harmonics $(3, 9, 15, 21, ..., \infty)$ can be used. As an example, the voltage control is performed using only third harmonic addition to transformer-side of the converter (see Fig. 2.2). Based on this strategy, the AC-side voltages in a 3-phase SMMC shown in Fig. 2.2 can be represented as:

$$
\begin{cases}
v_a = V_{mf} \sin(\omega_f t) + V_3 \sin(3\omega_f t + \beta) \\[2mm]
v_b = V_{mf} \sin(\omega_f t - 2\pi/3) + V_3 \sin(3\omega_f t + \beta) \\[2mm]
v_c = V_{mf} \sin(\omega_f t - 4\pi/3) + V_3 \sin(3\omega_f t + \beta) \\[2mm]
v_U = \lambda_u v_u \quad , \quad \lambda_u = \text{sign}(v_u) \quad , \quad u = a, b, c
\end{cases}
\tag{2.14}
$$

$$
\begin{cases}
v_x = V_{mh} \sin(\omega_h t + \theta_h) \\[2mm]
v_y = V_{mh} \sin(\omega_h t + \theta_h - 2\pi/3) \\[2mm]
v_z = V_{mh} \sin(\omega_h t + \theta_h - 4\pi/3) \\[2mm]
v_U = \lambda_u v_u \quad , \quad \lambda_u = \text{sign}(v_u) \quad , \quad u = x, y, z
\end{cases}
\tag{2.15}
$$

Now it is desired to develop voltage balancing equations for one phase of the SMMC (e.g. the phase between A and X). According to Fig. 2.2, the instantaneous power

going through FBA1 and HBA1 are:

$$p_{\mathrm{HB1}}(t) = (i_{\mathrm{A}} + i_{\mathrm{X}}) \times v_{\mathrm{X}} \quad , \quad p_{\mathrm{FB1}}(t) = i_{\mathrm{A}} \times (v_{\mathrm{A}} - v_{\mathrm{X}}). \tag{2.16}$$

Similar to the previous section, the capacitor voltage balancing criteria is defined as:

$$\left. \begin{array}{c} \int_T \Big(p_{\mathrm{FB1}}(t) + p_{\mathrm{HB1}}(t) \Big).dt = 0 \\[2mm] \int_T p_{\mathrm{FB1}}(t).dt = 0 \end{array} \right\} \text{balancing criteria.} \tag{2.17}$$

The neutral terminal of the transformer is not grounded, thus the added third harmonic voltage does not create current and cannot contribute to the power flow. As a result, similar to previous section, the first criterion of voltage balancing leads to the real power balance between the AC-sides. The second criterion of voltage balancing eqs. leads to:

$$\mathrm{VG} = \frac{V_{\mathrm{mf}}}{V_{\mathrm{mh}}} = \int_T \frac{2\lambda_{\mathrm{a}} \sin(\omega_{\mathrm{f}} t - \varphi_{\mathrm{f}}) \left| \sin(\omega_{\mathrm{h}} t + \theta_{\mathrm{h}}) \right|}{\cos(\varphi_{\mathrm{f}})} .dt. \tag{2.18}$$

The impact of phase angle θ_{h} and frequency ratio are studied before. Thus, for simplicity, in this section, it is assumed that $\theta_{\mathrm{h}} = 0$ and also the frequency ratio is not a small integer number. The ratio of AC-side voltages can be calculated as:

$$\mathrm{VG} = \frac{V_{\mathrm{mf}}}{V_{\mathrm{mh}}} = \int_T g(t) - 2\tan(\varphi_{\mathrm{f}}) \int_T s(t), \tag{2.19}$$

where, $g(t)$ and $s(t)$ are obtained as:

$$g(t) = 2\lambda_{\mathrm{a}} \sin(\omega_{\mathrm{f}} t) \left| \sin(\omega_{\mathrm{h}} t) \right| \quad , \quad s(t) = 2\lambda_{\mathrm{a}} \cos(\omega_{\mathrm{f}} t) \left| \sin(\omega_{\mathrm{h}} t) \right|. \tag{2.20}$$

λ_a may be represented as:

$$\begin{cases} \lambda_a = \text{sign}(V_{mf}\sin(\omega_f t) + V_3\sin(3\omega_f t + \beta)) = \text{sign}(\sin(\omega_f t) + \gamma\sin(3\omega_f t + \beta)) \\ \gamma = \dfrac{V_3}{V_{mf}} \quad, \quad -\pi \leq \beta \leq \pi. \end{cases} \quad (2.21)$$

Adding third harmonic voltage would appear as a phase-angle shift in λ_a, such that the zero-crossing point of the target AC voltage is shifted by δ (rad) without affecting the fundamental component as shown in Fig. 2.16. Different values of δ could be achieved by adjusting γ and β in Eq. (2.21) as shown in Fig. 2.17. The behavior of $\int g(t)$ and $\int s(t)$ regarding to different amount of third harmonic injection (γ, β) are illustrated in Fig. 2.18 and Fig. 2.19, respectively. By considering the impact of power factor in Eq. (2.19), the voltage gain of the converter is sketched for $\beta = -0.8\pi$ and $\beta = 0.8\pi$, as shown in Fig. 2.20 and Fig. 2.21, respectively.
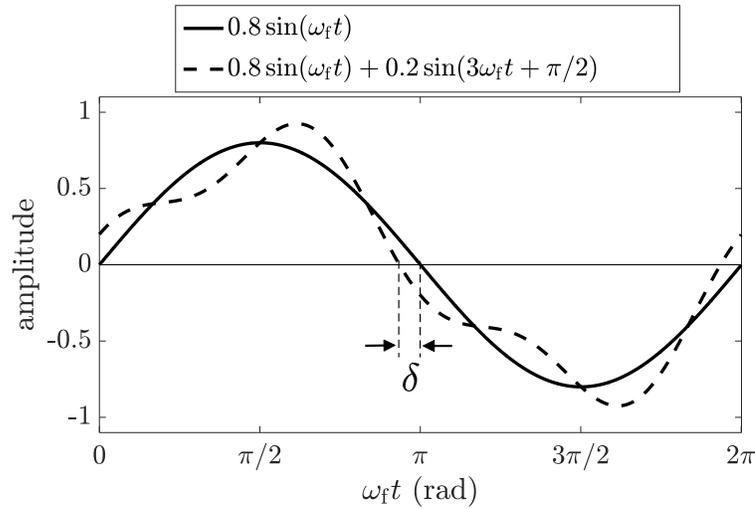
Figure 2.16. Adding third harmonic voltage shifts the zero-crossing point.
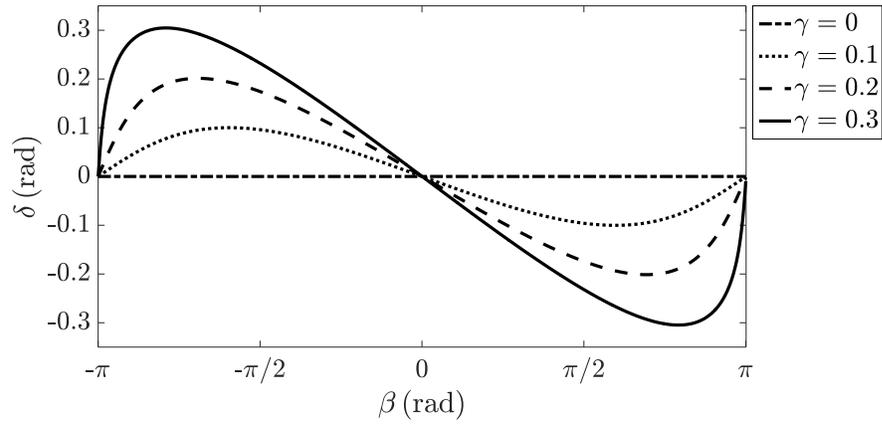
Figure 2.17. The value of δ in regards with β.
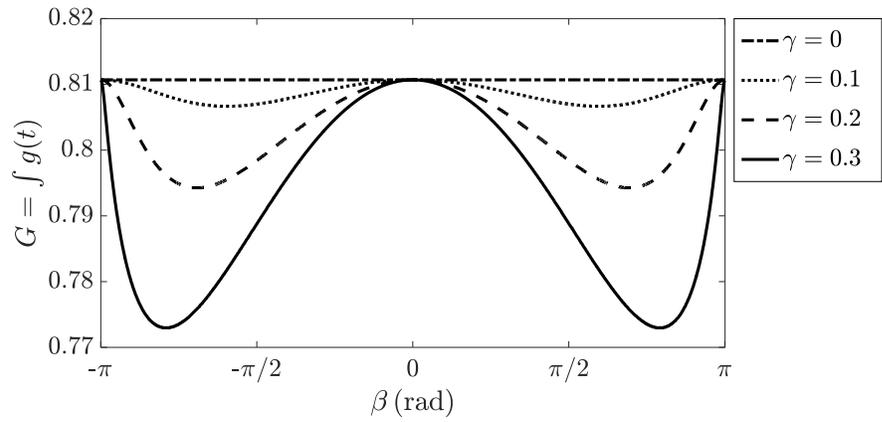
Figure 2.18. The impact of third harmonic injection on the function G.
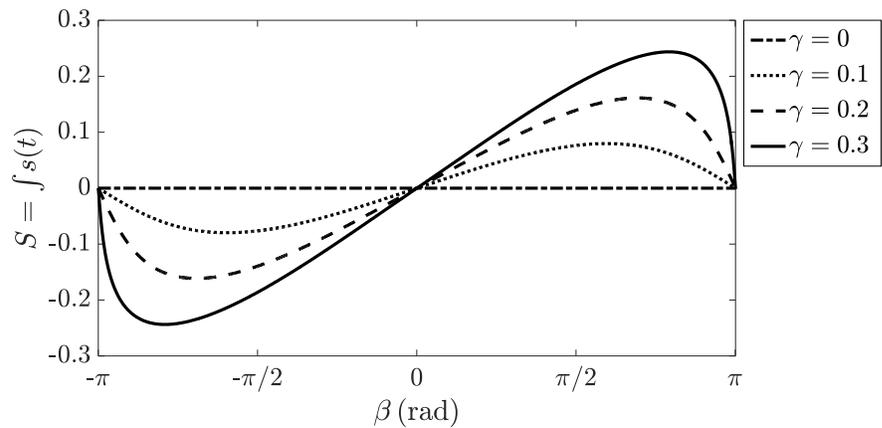
Figure 2.19. The impact of third harmonic injection on the function S.
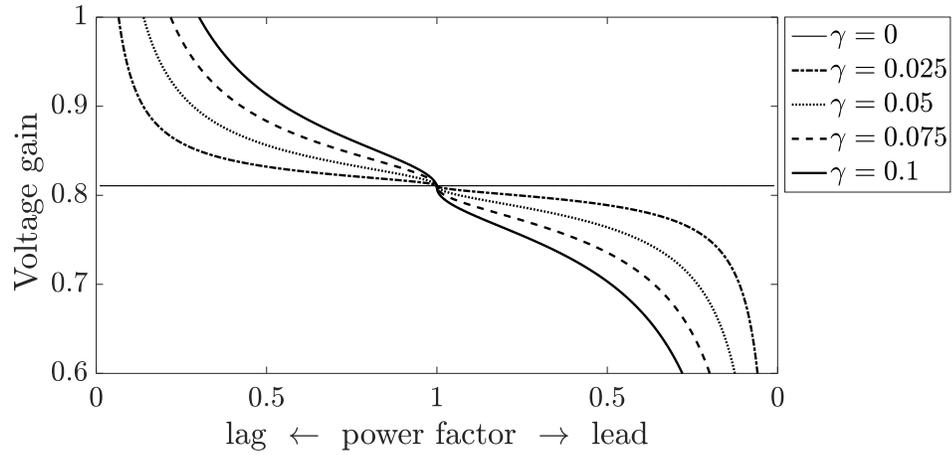
Figure 2.20. The voltage gain in regards with γ ($\beta = -0.8\pi$).
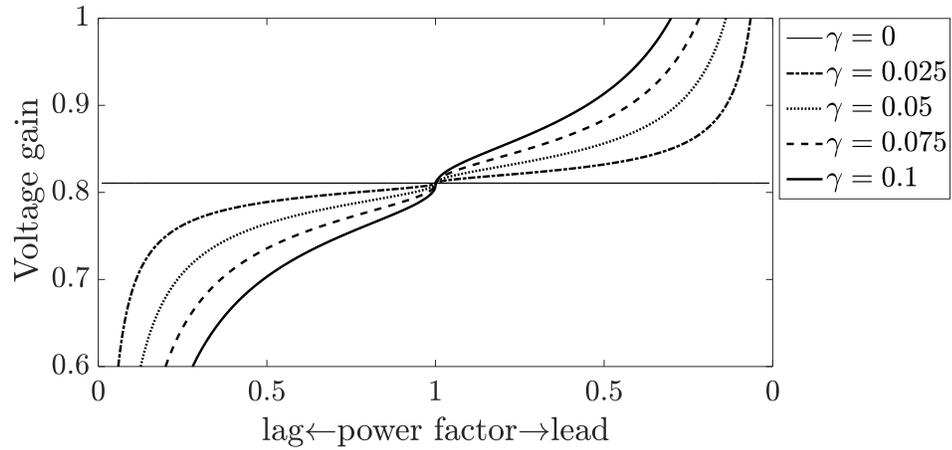
Figure 2.21. The voltage gain versus γ ($\beta = 0.8\pi$).
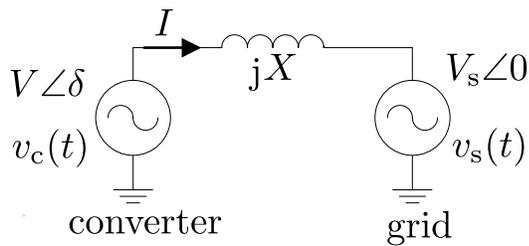
Figure 2.22. Simplified single-line diagram of converter-grid circuit.

2.3.3 The Power Capability of SMMC

Figure 2.22 shows the simplified single-line diagram of converter-grid circuit. The injected real and reactive powers to the grid are calculated as:

$$P = \frac{VV_{\mathrm{s}}}{X}\sin\delta \quad , \quad Q = \frac{V_{\mathrm{s}}^2 - VV_{\mathrm{s}}\cos\delta}{X}, \tag{2.22}$$

where, $V\angle\delta$ and $V_{\mathrm{s}}\angle 0$ are the voltage phasors of converter's AC-side and grid, respectively and X is the filter reactance. To study the impact of converter's gain, it is assumed that $V_{\mathrm{s}} = 1\,\mathrm{pu}$. From Eq. (2.22), the *PQ* diagram of the SMMC is both sketched regardless of the converter's limitation and also considering the maximum tolerable IGBT's current as magnified in Fig. 2.23.
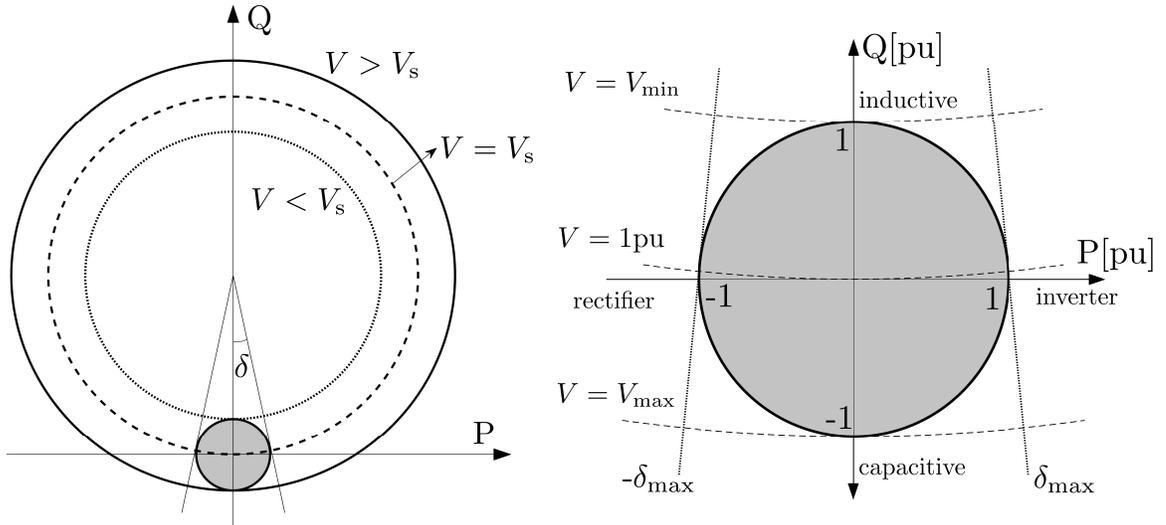
Figure 2.23. The power capability chart of SMMC.

The typical value of $0.05\,\mathrm{pu}$ is assumed for the filter reactance. Considering $Q = \pm1\,\mathrm{pu}$ in Eq. (2.22), the range of converter's output voltage is equal to $V_{\mathrm{min}} = 0.95$ and $V_{\mathrm{max}} = 1.05$ as shown in Fig. 2.24 for inverter mode. From the previous section,

the required injected third harmonic voltage for this SMMC is in the range of $-0.10 \leqslant$ $\gamma \leqslant 0.10$.
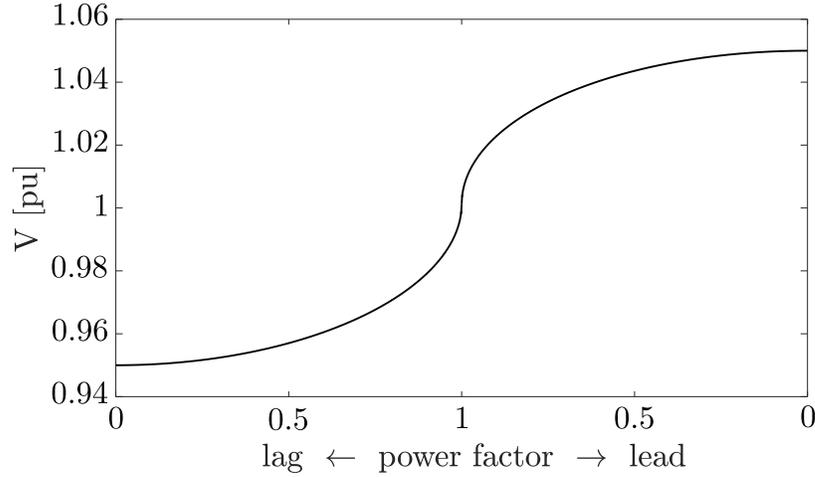
Figure 2.24. Required output voltage in different power factor (inverter mode).

2.4   Control Strategy

Figure 2.25 shows the schematic diagram of the proposed control system for a 3-phase SMMC. This controller operates by regulating AC-side currents in two separate *dq*-frames. This requires a synchronization mechanism that is achieved through a Phase-Locked Loop (PLL) on each side of the converter. Two reference generators are utilized to provide the reference ac currents for the next control stage. P_{fref} in grid F, determines the amount and direction of transferred real power, whilst the reactive power of both sides, Q_{fref} and Q_{href} are regulated to arbitrary values within the ratings of converter. On each side of the converter, a standard current controller in *dq*-frame depicted in Fig. 2.26, which provides the expected active and reactive power exchange with the grid.
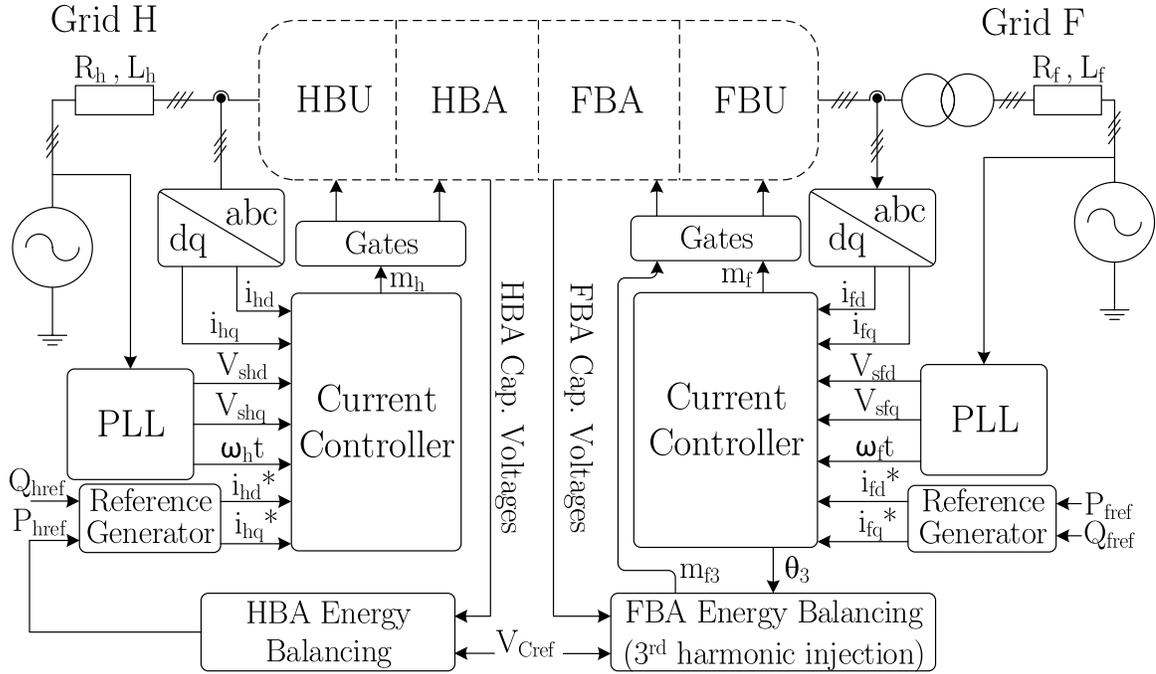
Figure 2.25. The schematic diagram of control strategy.
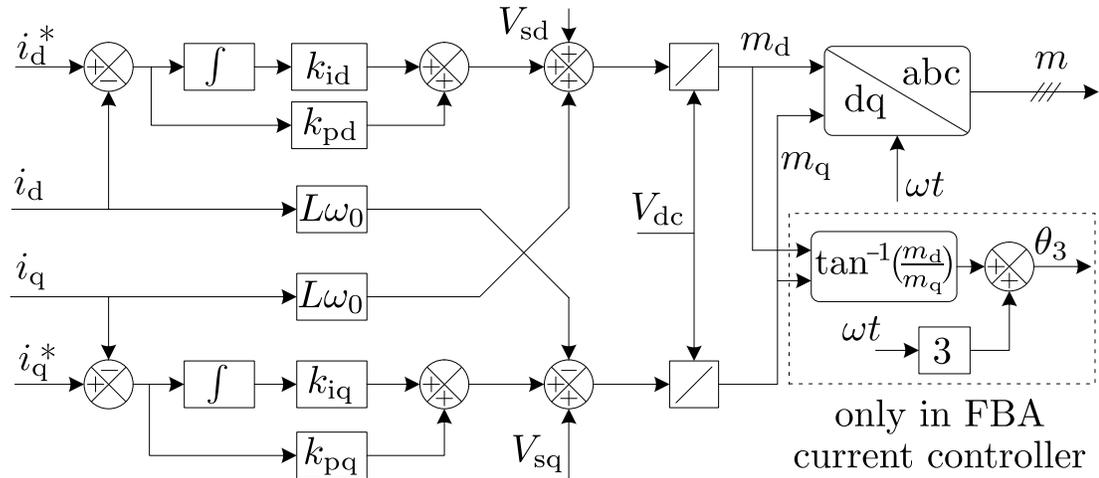
Figure 2.26. The schematic diagram of the current controller.

To ensure the power balance, a slow outer control loop is employed on each side of the converter, such that the total energy stored in the capacitors is effectively regulated at all time. To do so, the capacitor voltage reference (V_{Cref}) and also the measured value are squared and multiplied by the total number of SM in the arm, which provides the desired and measured energy stored in the arm. By adjusting the total energy stored in the arm capacitors, the balance between the arm power and the AC-side active power is maintained. For the HB-side, the internal control variable of P_{href} is provided according to the total energy stored in the HBAs as illustrated in Fig. 2.27. n_{C} is the total number of capacitors in each arm which is equal to $(n-1)/2$ in an n-level SMMC. For the FB-side, as mentioned in the previous section, the power flow could be controlled by injecting third harmonic voltage.
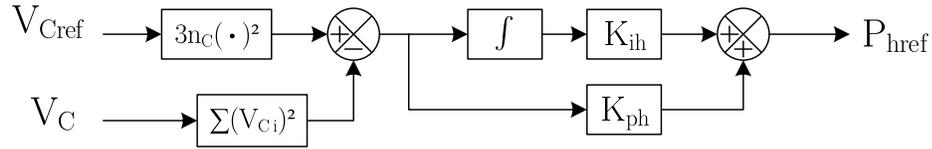
Figure 2.27. The schematic diagram of HBA Energy Balancing unit.
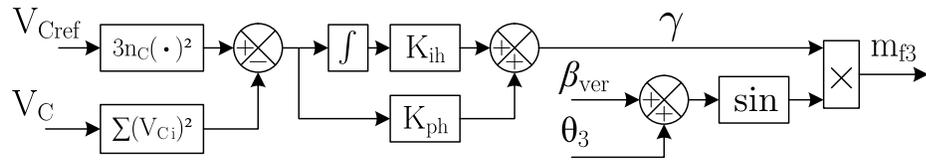
Figure 2.28. The schematic diagram of FBA Energy Balancing unit.

Figure 2.28 illustrates the process of providing γ which then is used to generate the third harmonic component. β_{ver} ($\approx 0.8\pi$ or -0.8π) is the phase angle that generates the highest/lowest voltage gain. It is also necessary to evenly distribute the arm energy between the capacitors by selecting the proper SMs at each time. This is done according to the sorted queue of capacitor voltages and arm current direction [26].

2.5 Simulation Results

The theoretical findings for a 3-phase SMMC shown in Fig. 2.2 are validated by simulation using MATLAB/Simulink software. In this simulation, the HB-side of the converter is connected to grid H with frequency of 60 Hz, while the other side is connected to grid F operating at 50 Hz. The converter is rated for 4 MVA and the capacitors' average voltage are regulated at 2 kV. Table 2.4 lists the main simulation parameters. A multi-carrier PWM is applied to the main leg such that the effective frequency of the output voltage is 1500 Hz. By having four SMs in each arm, the switching frequency of SM IGBTs is approximately 375 Hz, while the unfolder switches are operating at corresponding AC line frequency. In practice, the number of levels is higher according to the desired power and AC-side voltages. Thus, the waveform quality would improve and smaller AC filters could be installed.

Table 2.4.
SIMUALTION PARAMETERS

Parameter		Rating
Power rating	$S_{\text{conv.}}$	4 MVA
Grid F frequency	f_{f}	50 Hz
Grid F voltage (line-line rms)	V_{Sf}	7.3 kV
Grid H frequency	f_{h}	60 Hz
Grid H voltage (line-line rms)	V_{Sh}	9 kV
SM capacitor	C_{SM}	4 mF
No. of cells per arm	n_{C}	4
Mean cell capacitor voltage	E	2000 V
Filter+Grid inductance	L_{f}, L_{h}	5 mH
Filter+Grid resistance	R_{f}, R_{h}	10 mΩ

Figure 2.29 shows the steady-state converter voltages and currents. In this case, real power is flowing from grid F to grid H, while the power factor for both sides is unity. Therefore, the FB- and HB-sides of the converter are operating as a rectifier
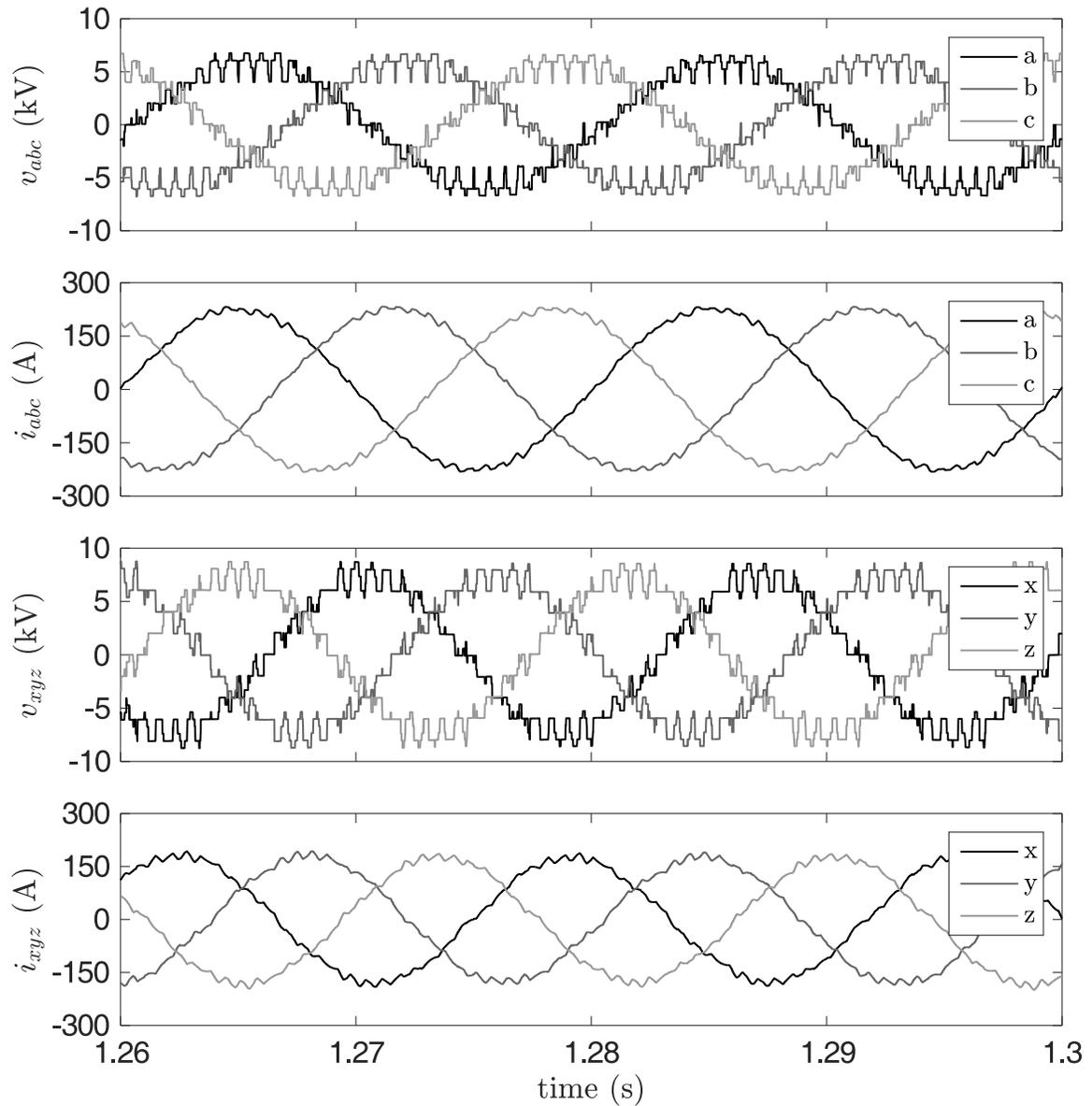
Figure 2.29. Voltage and current waveforms.

and an inverter, respectively. It can be seen that the third harmonic component of the AC-side voltages is canceled and the desired fundamental portion is well synthesized. It must be noticed that the voltages shown in Fig. 2.29 are considered as internal parameters of the converter and located before the AC-side filters. As mentioned in Section 2.4, on each side of the converter, a current controller is utilized to ensure an
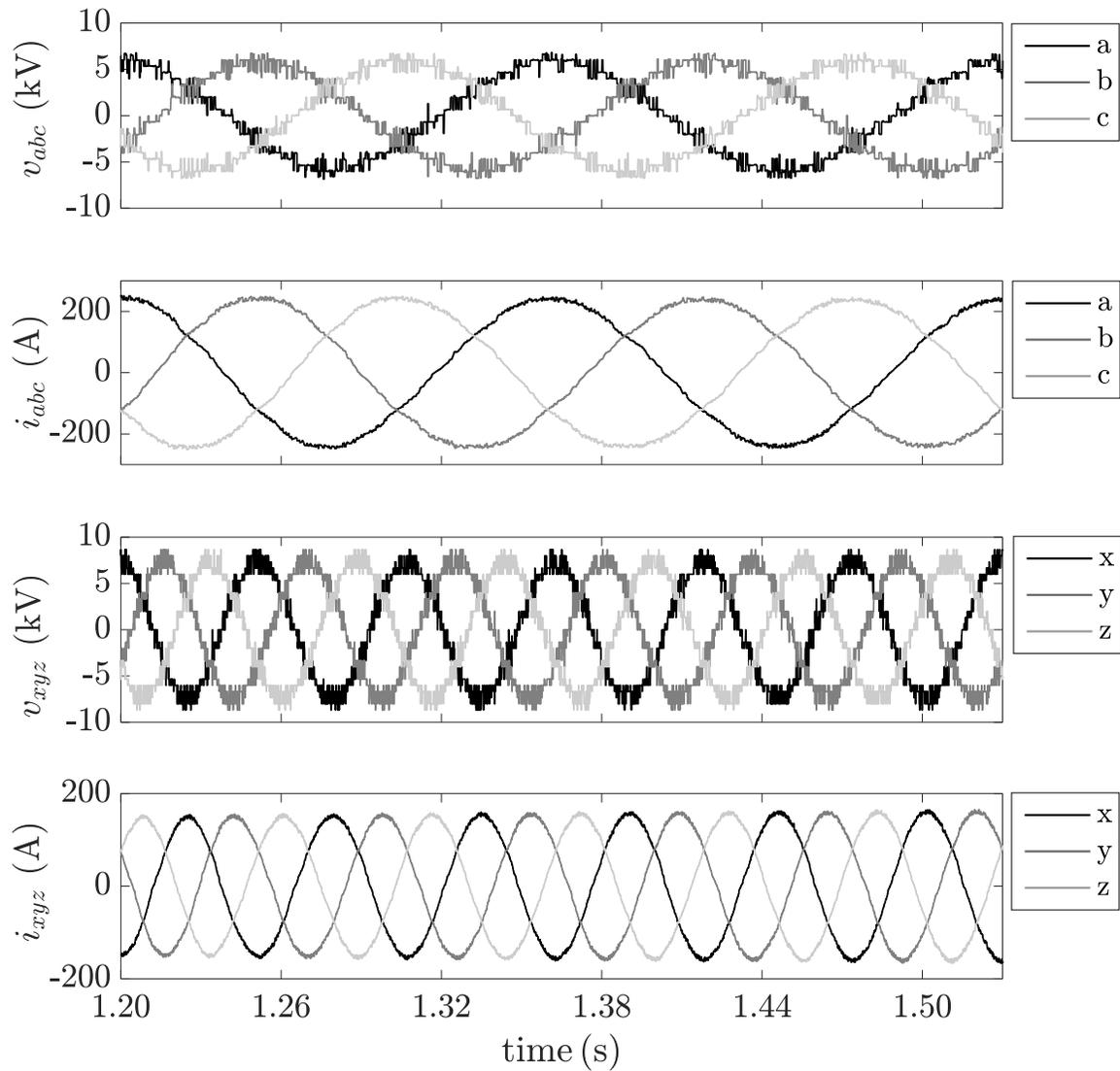
Figure 2.30. Voltage and current waveforms.

AC sinusoidal current with acceptable harmonic content (see Fig. 2.26). The current controller is fast enough to mitigate the impact of capacitor voltage ripple on the current by modifying the converter's AC-side voltage. As mentioned before, in a HFHW, an AC/AC converter connects the 60 Hz power grid to the HWTL which operates in a higher frequency. As an example, the steady-state results of the SMMC is also shown in Fig. 2.30 where it operates between a 60 Hz grid and 180 Hz line.
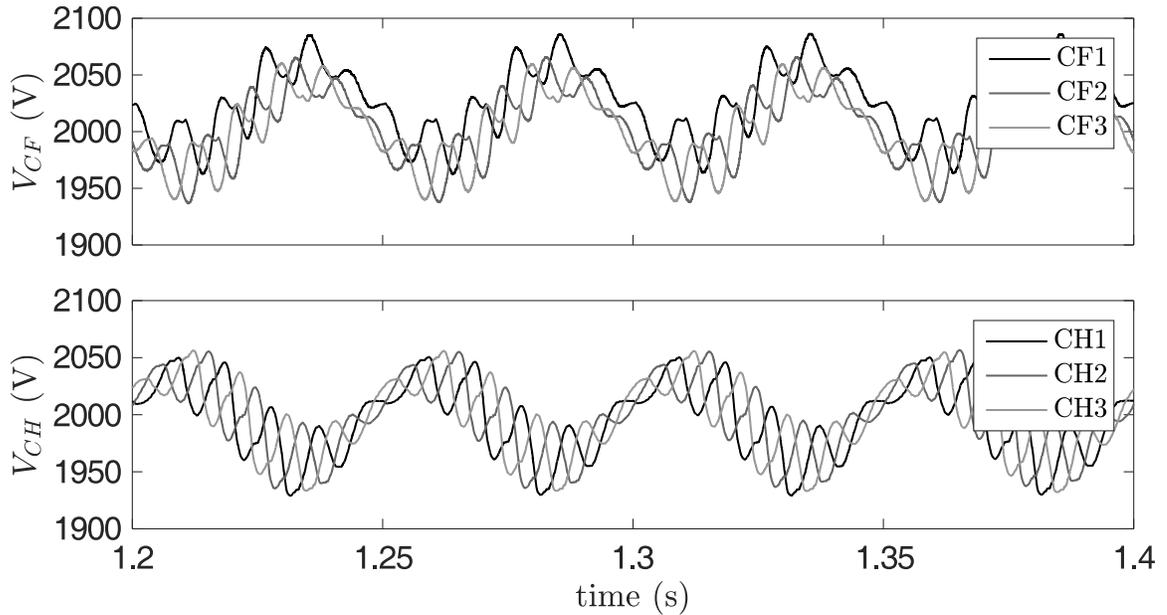
Figure 2.31. Average HBA and FBA capacitor voltages.

Figure 2.31 illustrates the behavior of the arm capacitor voltages in the steady-state conditions. In this case, the peak-to-peak ripple in the capacitor voltage is approximately 8% which may vary due to the operating point of active and reactive powers on both sides of the converter. Since the injected third-harmonic voltage does not create current, third-harmonic frequency does not appear in capacitor voltages. The 20 Hz ripple is caused by the converter's natural energy balancing cycle. Note that the frequency of the rectified AC-voltages (and consequently current) gets doubled (i.e. 100 Hz & 120 Hz) and afterwards, the greatest common factor (GCD) of the rectified currents' frequencies appears as the natural frequency of converter's energy balancing cycle (here, GCD(100, 120) = 20 Hz). To study the transient response of the converter, a few active and reactive power changes are applied on both sides as rising/falling ramp within 5 ms. As shown in Fig. 2.32, the desired operating point is properly controlled by its reference. During each transient, a small error may occur in the capacitor voltages which will be compensated in a few cycles.
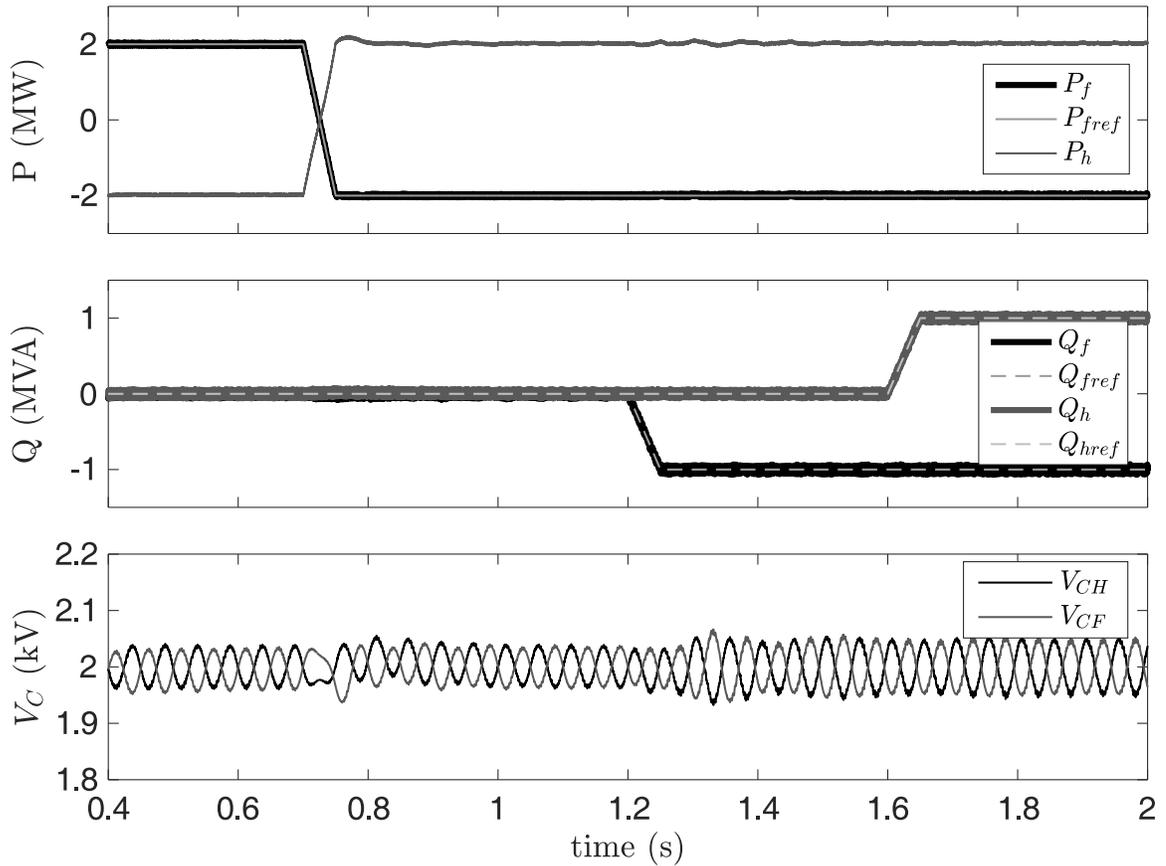
Figure 2.32. Converter transient waveforms during power variation.

2.6   Experimental Results

Although the simulation was performed on a 3-phase 4 MVA SMMC, due to limited resources in our laboratory, a low-voltage single-phase 5-level SMMC constructed using MOSFET devices as shown in (MTD6N15T4G)Figure 2.33. The control system is implemented on a dSPACE-MicroLabBox unit. The HB-side of the converter is connected to the grid (120 V & 60 Hz), while the FB-side feeds a resistive load operating in 98 V & 50 Hz.

The parameters of the experimental setup can be found in Table 2.5. Here, the switching frequency of 3 kHz is applied to the SM switches which could be reduced
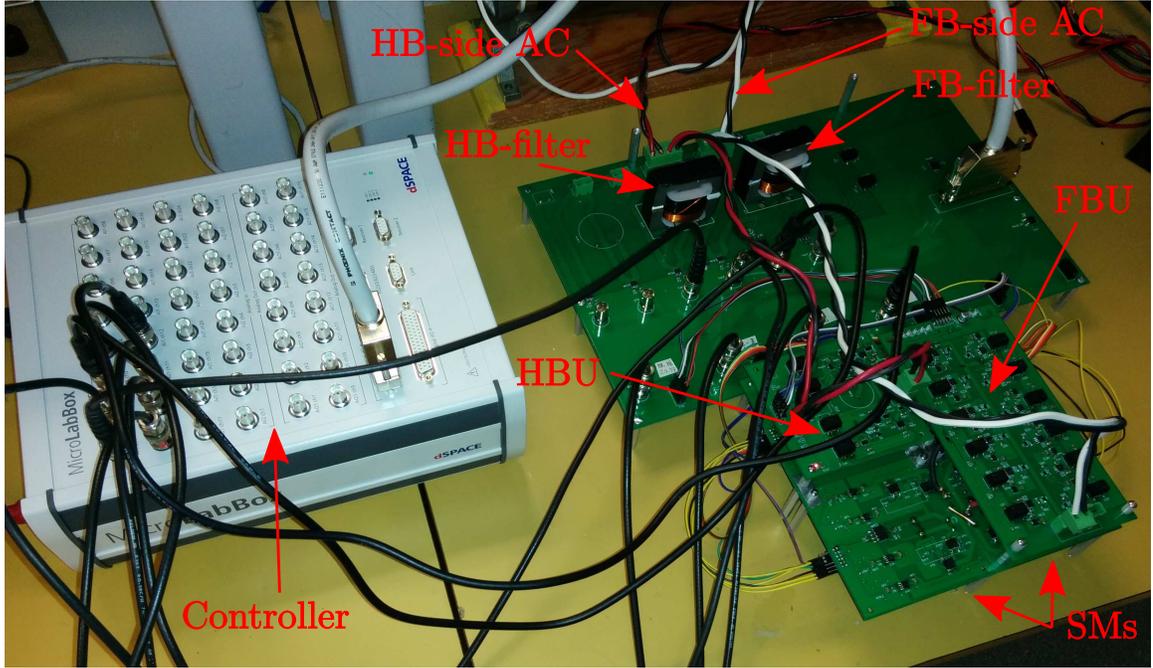
Figure 2.33. A view of the experimental setup.

Table 2.5.
EXPERIMENTAL PARAMETERS

Parameter		Rating
HB & FB sides' frequency	f_h, f_f	60 Hz, 50 Hz
HB & FB sides' AC voltage (rms)	$V_\mathrm{ac\_h}$, $V_\mathrm{ac\_f}$	120 V, 98 V
SM capacitor	C_SM	820 μF
Mean cell capacitor voltage	E	100 V
MOSFET maximum drain-source voltage	V_DS	150 V
MOSFET continuous drain current	I_D	6 A
MOSFET drain-source on-state resistance	$R_\mathrm{DS\text{-}ON}$	300 $m\Omega$
Filter inductance	$L_\mathrm{f}, L_\mathrm{s}$	5 mH

by utilizing higher number of SMs.

For a single-phase SMMC without third-harmonic injection and with frequency ratio of 60/50 = 1.2, the voltage gain is constant and almost equals $V_\mathrm{mf}/V_\mathrm{mh} \approx 0.81$. The reactive power on both sides are set to zero. With transferring only active power, in order to achieve power balance, the current ratio is expected to be $I_\mathrm{mf}/I_\mathrm{mh} \approx 1.23$.

The converter's HB- and FB-side waveforms in the steady-state condition are shown in Figs. 2.34 and 2.35, respectively. Both side currents are measured as they enter the converter and the voltages are measured before the AC-side filters (see Fig. 2.14). It can be seen that both side voltages are well synthesized with the expected amplitude and frequency.
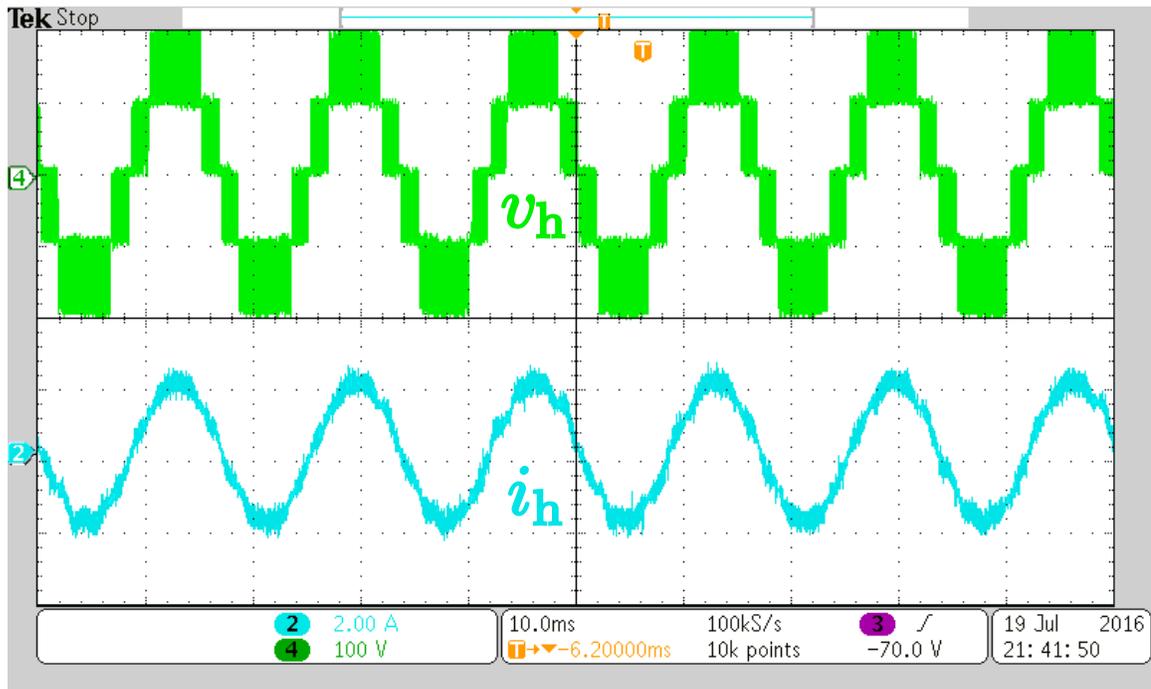
Figure 2.34. Converter's HB-side waveforms in steady-state condition.

In order to evaluate the dynamic response of the capacitor voltage balancing strategy, the load is suddenly doubled while the SM capacitor voltages are monitored. As shown in Fig. 2.36, a sudden increase in the load causes the capacitors to lose a small portion of their stored energy which would be detected by both HBA and FBA energy balancing units (see Figs. 2.27 and 2.28). Thus, the operation point will be upgraded and the capacitors' energy will be restored in less than 300 ms.
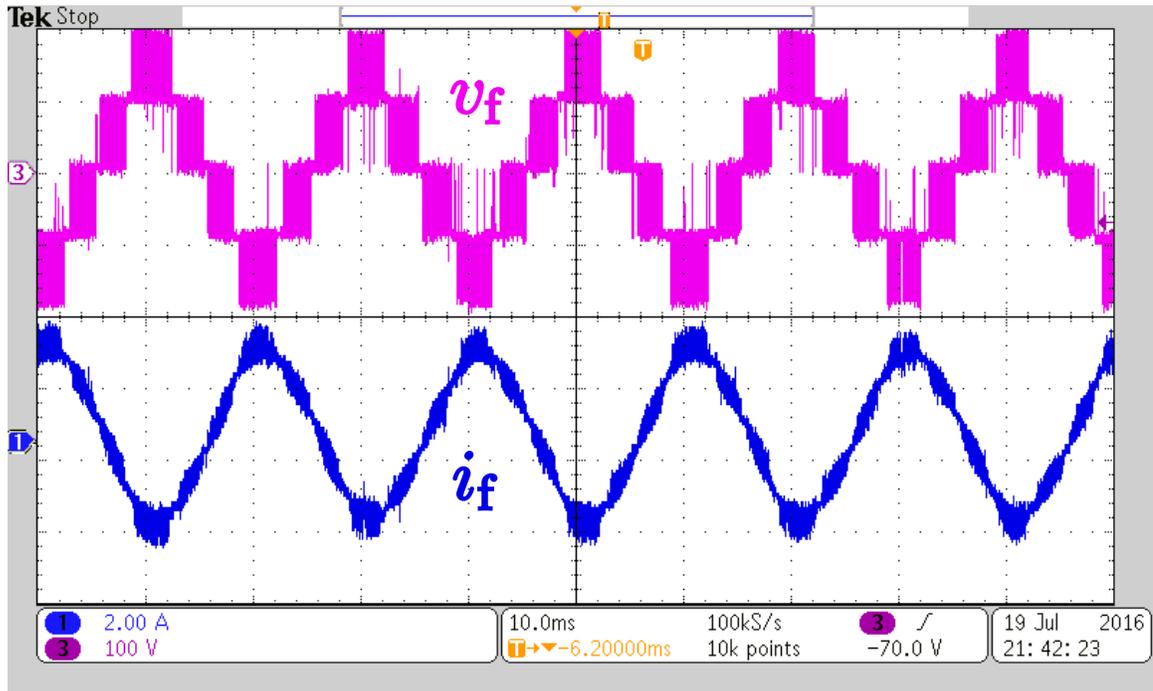
Figure 2.35. Converter's FB-side waveforms in steady-state condition.
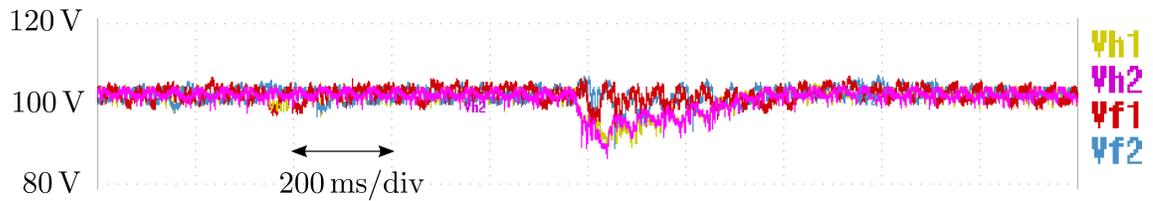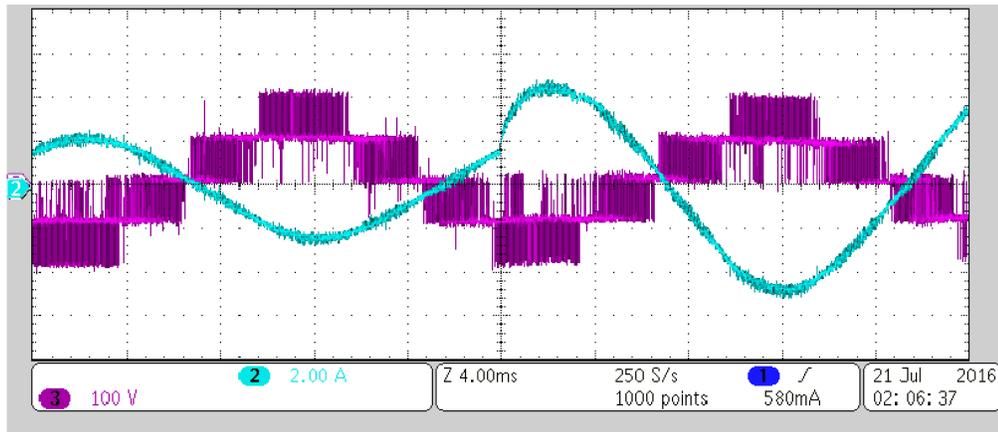
Figure 2.36. Dynamic response of the converter to the load change.

2.7   Summary

The SMMC topology for AC/AC power transmission system was studied in this chapter. It was shown that the SMMC requires fewer components compared to its alternatives and offers higher efficiency by utilizing more than half of the power switches in soft-switching mode. The proposed control strategy regulates the desired active/reactive power exchanged between the AC grids and it also ensures the capacitor voltage balancing of the converter. Both simulation and experimental results show that SMMC can fulfill the requirements of a bidirectional AC/AC converter.

Chapter 3

MinMax AC/AC Multilevel Converter

3.1 Introduction

This chapter presents another novel topology of bidirectional VSCs intended for High power AC/AC applications. The proposed topology further reduces the number of PWM-driven IGBTs and replace them with low-frequency soft-switched switches, and it is called MinMax Multilevel Converter (MMMC). It consists of a number of cascaded HBSMs in addition to nine soft-switched unfolders in a 3-phase version. Compared to MMC, MMMC does not inherit the internal unwanted circulating current which obviates the necessity of the arm inductors as well. The feasibility of the proposed converter, as well as the effectiveness of the control strategy are validated by simulation and experimental results.

R. Alaei, S. A. Khajehoddin and W. Xu, "MinMax AC/AC Multilevel Converter," *Power Electronics Letter*, (Under Review).

3.2 Principle of Operation

Figure 3.1 shows the single-phase version of the proposed converter. It consists of three separate stages that regulates the absolute AC voltages using the installed HBSM and pass them to each grid through a low frequency soft-switched unfolder. The proposed converter reduces the number of PWM-driven IGBTs and replace them with low-frequency and soft-switched switches, and it is called MMMC. For simplicity, all SM capacitors are assumed to be equally operating at voltage E and then, in the description of the control strategy, it will be shown how this is implemented. In Fig. 3.1, v_A and v_X are the rectified version of the AC-side voltages v_a and v_x, respectively. The lower HBSM-arm, i.e. LHBA provides the smaller absolute voltage, i.e. $\min(v_A, v_X)$, whilst, the upper HBSM-arm, i.e. UHBA generates the difference between the two, i.e. $|v_A - v_X|$. The middle unfolder, UFm relates these two synthesized voltages to the proper AC unfolders (UFa and UFx). In other words, the absolute
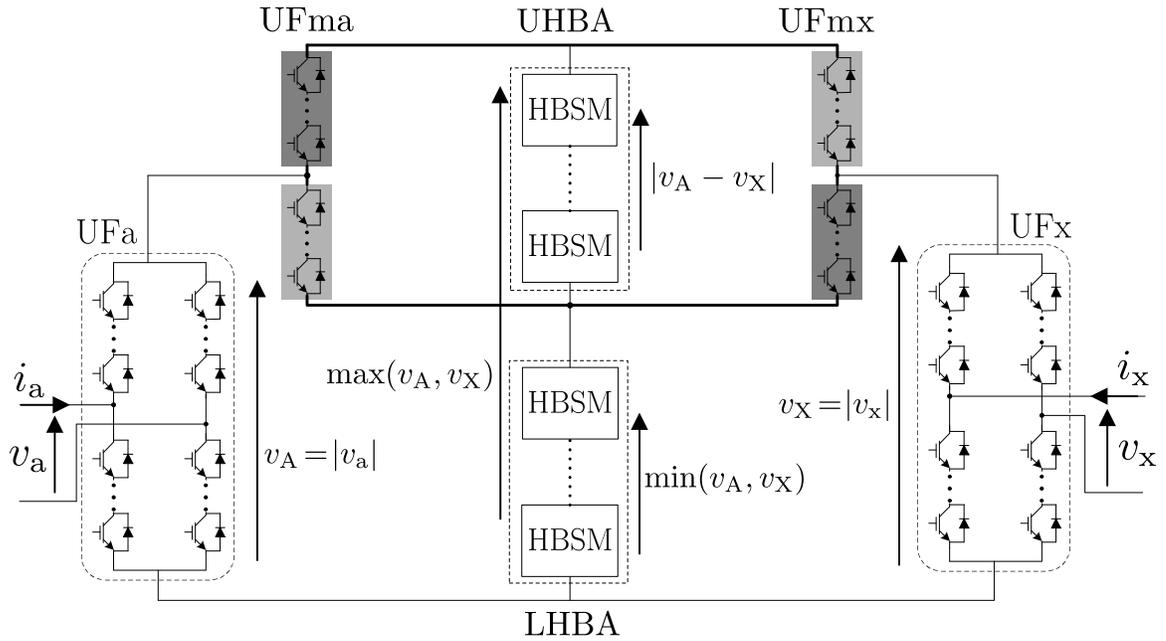
Figure 3.1. The schematic diagram of single-phase n-level MMMC.

value of AC voltage is synthesized by changing the number of inserted HBSMs, while the polarity is controlled by the corresponding unfolder.

In an n-level converter, the number of HBSMs in each arm is equal to $(n-1)/2$; so that all desired non-negative values of $v_{A,X}$ can be generated ($v_{A,X} = kE$, $k = 0, 1, \cdots, (n-1)/2$). Unlike MMC, there is no circulating current between different phases of this topology as the legs are isolated from each other by a 3-phase transformer as shown in Fig. 3.2.
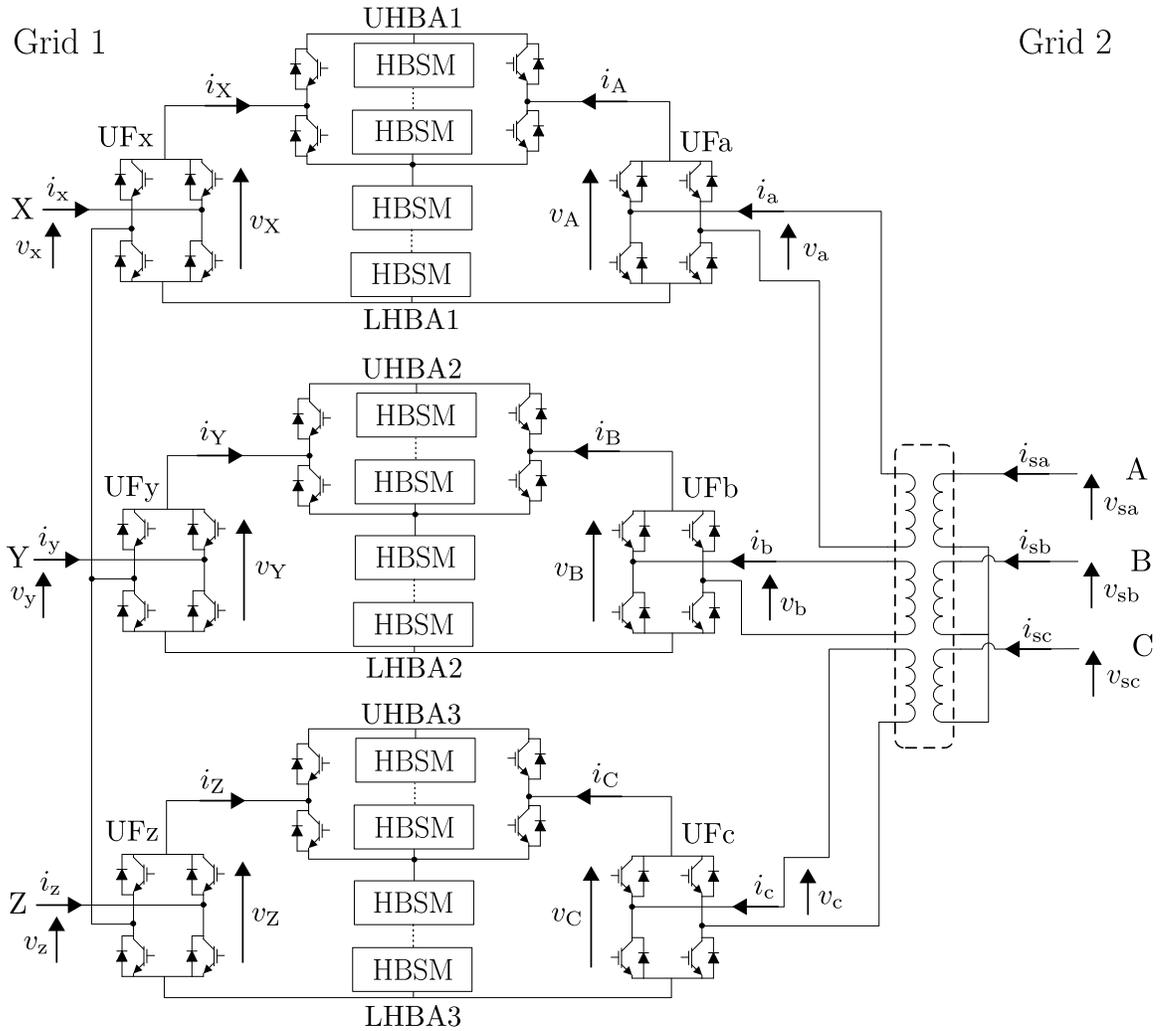
Figure 3.2. The schematic diagram of 3-phase MMMC.

Table 3.1 presents the component count comparison of the proposed MMMC with a B2B-MMC alternative. It can be seen that MMMC has fewer capacitors and 75% of the IGBTs operate is ZVS.

Table 3.1.
COMPARISON OF MMC AND MMMC COMPONENT COUNT

Quantity	1-Phase			3-Phase		
	MMC	SMMC	MMMC	MMC	SMMC	MMMC
Capacitor	$8(n-1)$	$(n-1)$	$(n-1)$	$12(n-1)$	$3(n-1)$	$3(n-1)$
Inductor	8	0	0	12	0	0
IGBT[†]	$16(n-1)$	$3(n-1)$	$2(n-1)$	$24(n-1)$	$9(n-1)$	$6(n-1)$
IGBT[‡]	0	$4n$	$6(n-1)$	0	$12n$	$18(n-1)$

[†] High-frequency & hard-switched
[‡] Line-frequency & soft-switched

As it can be seen from Table 3.1, the main difference between SMMC and MMMC is the number of hard-switched and soft-switched IGBTs. The MMMC has fewer hard-switched IGBTs which results in a higher efficiency, but the total number of IGBTs is increased which may result in higher device cost. Thus, it can be concluded that MMMC would be a wiser alternative, if efficiency is of higher importance. Also, SMMC would be more suitable, if the objective is to have the least total device cost.

3.2.1   Switching States of a 3-level Single-phase MMMC

As an example, a 3-level single-phase MMMC is sketched in Fig. 3.3. The switching function $d_i(i = 1, 2)$ is defined so that $d_i = 1$, when upper switch of the SM-leg is ON and the lower switch is OFF and $d_i = 0$, for the reverse case. In the AC-side unfolders, $k_j(j = a, x) = 1$ when $v_j \geqslant 0$ and $k_j = 0$ when $v_j < 0$. For the middle unfolder, $k_{m\_a} = 1$ & $k_{m\_x} = 0$ when $v_A \geqslant v_X$ and $k_{m\_a} = 0$ & $k_{m\_x} = 1$ when $v_A < v_X$. Table 3.2 shows all the possible switching states in a 3-level MMMC.
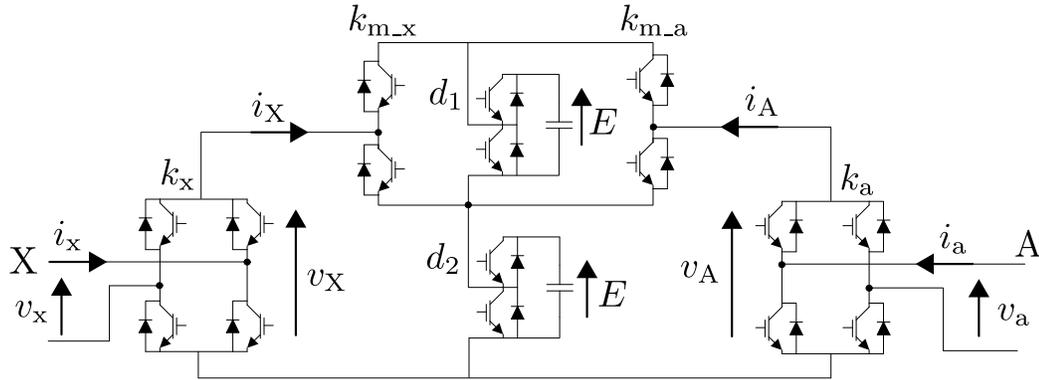
Figure 3.3. The schematic diagram of single-phase 3-level MMMC.

Table 3.2.
SWITCHING STATES OF A 3-LEVEL MMMC

#	d_1	d_2	k_a	k_x	k_{m_a}	k_{m_x}	v_A	v_X	v_a	v_x
1	0	1	0	0	1	0	E	E	$-E$	$-E$
2	1	0	0	1	1	0	E	0	$-E$	0
3	0	1	0	1	1	0	E	E	$-E$	E
4	1	0	1	0	0	1	0	E	0	$-E$
5	0	0	1	1	1	0	0	0	0	0
6	1	0	1	1	0	1	0	E	0	E
7	0	1	1	0	1	0	E	E	E	$-E$
8	1	0	1	1	1	0	E	0	E	0
9	0	1	1	1	1	0	E	E	E	E

3.3   Capacitor Voltage Balancing

Figure 3.4 shows the simplified schematic diagram of a single-phase MMMC.
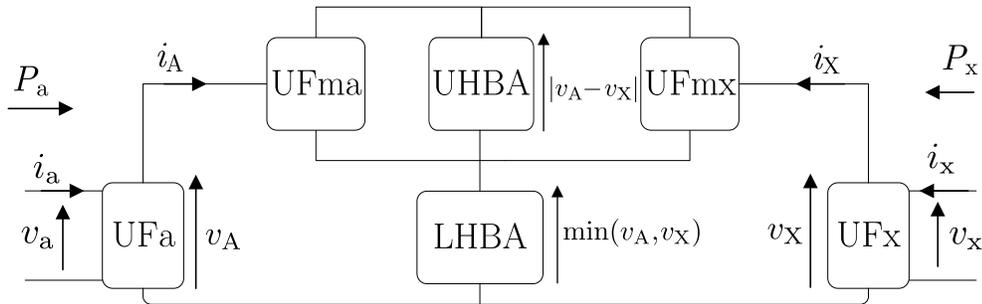
Figure 3.4. Simplified schematic diagram of a single-phase MMMC.

The phase A and X voltages and currents are represented as:

$$\begin{cases} v_{\mathrm{a}} = V_{\mathrm{ma}}\sin(\omega_{\mathrm{a}}t) \ , \ v_{\mathrm{A}} = \lambda_{\mathrm{a}}.v_{\mathrm{a}} \\[2mm] i_{\mathrm{a}} = I_{\mathrm{ma}}\sin(\omega_{\mathrm{a}}t - \varphi_{\mathrm{a}}) \ , \ i_{\mathrm{A}} = \lambda_{\mathrm{a}}.i_{\mathrm{a}}, \\[2mm] \lambda_{\mathrm{a}} = \mathrm{sign}(v_{\mathrm{a}}) = \mathrm{sign}(\sin(\omega_{\mathrm{a}}t)) \end{cases} \begin{cases} v_{\mathrm{x}} = V_{\mathrm{mx}}\sin(\omega_{\mathrm{x}}t + \theta) \ , \ v_{\mathrm{X}} = \lambda_{\mathrm{x}}.v_{\mathrm{x}} \\[2mm] i_{\mathrm{x}} = I_{\mathrm{mx}}\sin(\omega_{\mathrm{x}}t + \theta - \varphi_{\mathrm{x}}) \ , \ i_{\mathrm{X}} = \lambda_{\mathrm{x}}.i_{\mathrm{x}}, \\[2mm] \lambda_{\mathrm{x}} = \mathrm{sign}(v_{\mathrm{x}}) = \mathrm{sign}(\sin(\omega_{\mathrm{x}}t + \theta)) \end{cases} \quad (3.1)$$

The instantaneous power going through UHBA and LHBA are calculated as:

$$p_{\mathrm{U}}(t) = v_{\mathrm{U}} \times i_{\mathrm{U}} = \begin{cases} (v_{\mathrm{A}} - v_{\mathrm{X}}) \times i_{\mathrm{A}} & v_{\mathrm{A}} \geqslant v_{\mathrm{X}} \\[3mm] (v_{\mathrm{X}} - v_{\mathrm{A}}) \times i_{\mathrm{X}} & v_{\mathrm{A}} < v_{\mathrm{X}} \end{cases} \quad (3.2)$$

$$p_{\mathrm{L}}(t) = v_{\mathrm{L}} \times i_{\mathrm{L}} = \begin{cases} v_{\mathrm{X}} \times (i_{\mathrm{A}} + i_{\mathrm{X}}) & v_{\mathrm{A}} \geqslant v_{\mathrm{X}} \\[3mm] v_{\mathrm{A}} \times (i_{\mathrm{A}} + i_{\mathrm{X}}) & v_{\mathrm{A}} < v_{\mathrm{X}}. \end{cases} \quad (3.3)$$

In the steady-state condition, the stored energy of both arms must remain constant. This leads to the following equations:

$$\int_{T} p_{\mathrm{U}}(t).dt = 0, \quad \int_{T} p_{\mathrm{L}}(t).dt = 0. \quad (3.4)$$

The above equation can be rewritten as below voltage balancing criteria:

$$\left. \begin{array}{c} \int_{T}\{(p_{\mathrm{U}}(t) + p_{\mathrm{L}}(t)\}.dt = 0 \\[3mm] \int_{T} p_{\mathrm{L}}(t).dt = 0 \end{array} \right\} \text{voltage balancing criteria.} \quad (3.5)$$

The first criterion leads to the real power balance between the AC-sides as presented below:

$$
\begin{aligned}
0 &= \int_T \left(p_U(t) + p_L(t) \right).dt \\
&= \begin{cases}
\int_T [(v_A - v_X) \times i_A + v_X \times (i_A + i_X)].dt & v_A \geqslant v_X \\
\int_T [(v_X - v_A) \times i_X + v_A \times (i_A + i_X)].dt & v_A < v_X
\end{cases} \\
&= \int_T (v_A \times i_A + v_X \times i_X).dt = \frac{1}{2} V_{ma} I_{ma} \cos(\varphi_x) + \frac{1}{2} V_{mx} I_{mx} \cos(\varphi_a) \\
\Rightarrow\ & P_a + P_x = 0,
\end{aligned}
\tag{3.6}
$$

Thus, the summation of active power flowing into the converter must be equal to zero. The second criterion is studied as:

$$
\begin{aligned}
0 &= \int_T p_L(t).dt \\
&= \int_T \min(v_A, v_X) \times (i_A + i_X).dt \\
&= \frac{1}{2} \int_T (v_A + v_X - |v_A - v_X|) \times (i_A + i_X).dt \\
&= \int_T v_A \times i_X + v_X \times i_A - |v_A - v_X| \times (i_A + i_X).dt
\end{aligned}
\tag{3.7}
$$

which can be rewritten in detail as:

$$
\begin{aligned}
0 = \int_T\ & V_{ma} I_{mx} |\sin(\omega_a t)|.\sin(\omega_x t + \theta - \varphi_x).\mathrm{sign}(\sin(\omega_x t + \theta)) \\
&+ V_{mx} I_{ma} |\sin(\omega_x t + \theta)|.\sin(\omega_a t - \varphi_a).\mathrm{sign}(\sin(\omega_a t)) \\
&- \left| V_{ma} |\sin(\omega_a t)| - V_{mx} |\sin(\omega_x t + \theta)| \right| \\
&\times (I_{ma} \sin(\omega_a t - \varphi_a)\mathrm{sign}(\sin(\omega_a t)) + I_{mx} \sin(\omega_x t + \theta - \varphi_x)\mathrm{sign}(\sin(\omega_x t + \theta))).dt
\end{aligned}
\tag{3.8}
$$

There is no analytical solution for Eq. (3.8), however, it can be studied in different conditions as below:

a) The impact of frequency ratio $(\varphi_a = \varphi_x = \theta = 0)$

In this condition, Eq. (3.8) could be simplified as:

$$0 = \int_T (V_{ma}I_{mx} + V_{mx}I_{ma})|\sin(\omega_x t).\sin(\omega_a t)|$$
$$- \big|V_{ma}|\sin(\omega_a t)| - V_{mx}|\sin(\omega_x t)|\big| \times (I_{ma}|\sin(\omega_a t)| + I_{mx}|\sin(\omega_x t)|).dt \tag{3.9}$$

Also, from Eq. (3.6) could be concluded:

$$V_{ma}I_{ma} = -V_{mx}I_{mx} \Rightarrow \frac{V_{ma}}{V_{mx}} = -\frac{I_{mx}}{I_{ma}} = M \tag{3.10}$$

By substituting Eq. (3.10) in Eq. (3.9):

$$0 = \int_T (1 - M^2)|\sin(\omega_x t).\sin(\omega_a t)|$$
$$+ \big|M|\sin(\omega_a t)| - |\sin(\omega_x t)|\big| \times (M|\sin(\omega_x t)| - |\sin(\omega_a t)|).dt \tag{3.11}$$

The value of M depends on the frequency ratio and could be obtained as shown in Fig. 3.5.

b) The impact of phase angle shift θ $(\varphi_a = \varphi_x = 0)$

In this case, Eq. (3.11) could be rewritten as:

$$0 = \int_T (1 - M^2)|\sin(\omega_x t + \theta).\sin(\omega_a t)|$$
$$+ \big|M|\sin(\omega_a t)| - |\sin(\omega_x t + \theta)|\big| \times (M|\sin(\omega_x t + \theta)| - |\sin(\omega_a t)|).dt \tag{3.12}$$

The value of M in different phase angle shifts θ is shown in Fig. 3.6.

c) The impact of power factor φ_x $(\varphi_a = \theta = 0)$
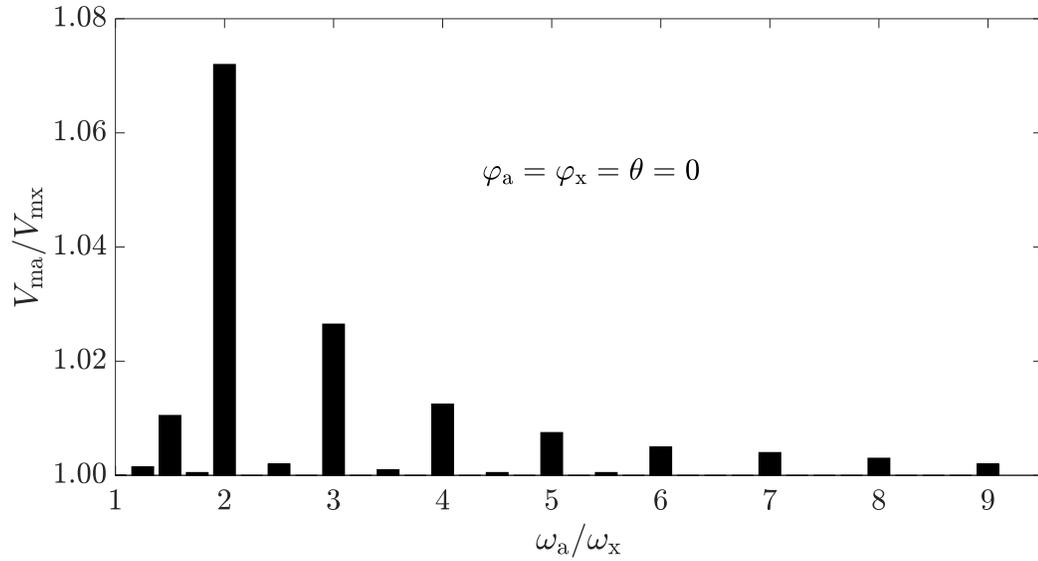
Figure 3.5. The voltage gain of MMMC versus frequency ratio.
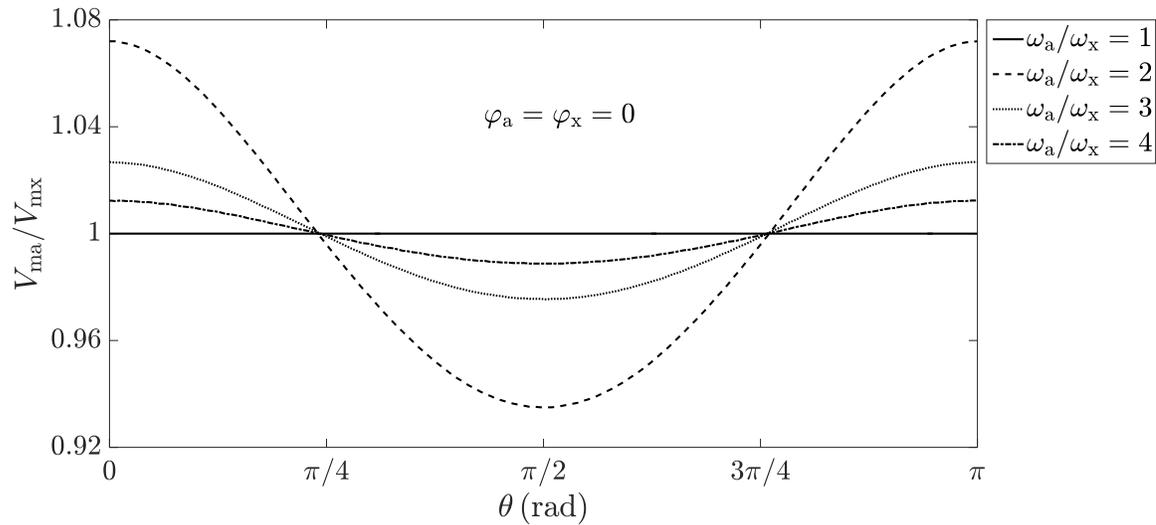
Figure 3.6. The voltage gain of MMMC versus θ (rad).

In this case, from Eq. (3.6) could be concluded:

$$\frac{1}{2}V_{\text{ma}}I_{\text{ma}}\cos(\varphi_{\text{a}}) + \frac{1}{2}V_{\text{mx}}I_{\text{mx}}\cos(\varphi_{\text{x}}) = 0$$

$$\Rightarrow V_{\text{ma}}I_{\text{ma}} = -V_{\text{mx}}I_{\text{mx}}\cos(\varphi_{\text{x}}) \Rightarrow \frac{V_{\text{ma}}}{V_{\text{mx}}} = -\frac{I_{\text{mx}}\cos(\varphi_{\text{x}})}{I_{\text{ma}}} = \text{M}$$

(3.13)

Thus, Eq. (3.8) could be rewritten as:

$$0 = \int_T \frac{-\text{M}^2}{\cos\varphi_{\text{x}}}|\sin(\omega_{\text{a}}t)|.\sin(\omega_{\text{x}}t - \varphi_{\text{x}}).\text{sign}(\sin(\omega_{\text{x}}t)) + |\sin(\omega_{\text{x}}t).\sin(\omega_{\text{a}}t)|$$

$$- \big|\text{M}|\sin(\omega_{\text{a}}t)| - |\sin(\omega_{\text{x}}t)|\big|$$

$$\times (|\sin(\omega_{\text{a}}t)| + \frac{-\text{M}}{\cos\varphi_{\text{x}}}\sin(\omega_{\text{x}}t - \varphi_{\text{x}}).\text{sign}(\sin(\omega_{\text{x}}t))).dt$$

(3.14)

$$= \int_T (1 - \text{M}^2)|\sin(\omega_{\text{x}}t).\sin(\omega_{\text{a}}t)|$$

$$+ \big|\text{M}|\sin(\omega_{\text{a}}t)| - |\sin(\omega_{\text{x}}t)|\big| \times (\text{M}|\sin(\omega_{\text{x}}t)| - |\sin(\omega_{\text{a}}t)|).dt + \int_T g(t).dt$$

where,

$$g(t) = \text{M}\tan\varphi_{\text{x}}.\cos(\omega_{\text{x}}t).\text{sign}(\sin(\omega_{\text{x}}t))$$

$$\times \big\{\text{M}|\sin(\omega_{\text{a}}t)| - \big|\text{M}|\sin(\omega_{\text{a}}t)| - |\sin(\omega_{\text{x}}t)|\big|\big\}$$

(3.15)

In the above equation, $g(t)$ is an odd function (i.e. $g(-t) = -g(t)$), which results in $\int_T g(t).dt = 0$. Therefore, Eq. (3.14) equals to what obtained in Eq. (3.11) and the power factor of phase X does not affect the capacitor voltage balancing. Similar calculations could be done for the power factor of phase A.

To sum up, the second criterion of voltage balancing in Eq. (3.5) implies that the voltage gain of the converter (i.e. $V_{\text{ma}}/V_{\text{mx}}$) depends on the frequency ratio and phase angle shift values.

3.3.1 Voltage Gain Adjustment

For many practical applications, voltage gain control is vital. For example, in grid-connected application, voltage gain can be used to adjust the reactive power exchange with the AC networks. Similar to Section 2.3.2, the voltage gain control is performed by injecting third harmonic voltage to the transformer-side of the converter. Thus, the AC-side voltages in a 3-phase MMMC can be represented as:

$$
\begin{cases}
v_{\mathrm{a}} = V_{\mathrm{m2}} \sin(\omega_2 t) + V_3 \sin(3\omega_2 t + \beta) \\[2mm]
v_{\mathrm{b}} = V_{\mathrm{m2}} \sin(\omega_2 t - 2\pi/3) + V_3 \sin(3\omega_2 t + \beta) \\[2mm]
v_{\mathrm{c}} = V_{\mathrm{m2}} \sin(\omega_2 t - 4\pi/3) + V_3 \sin(3\omega_2 t + \beta) \\[2mm]
v_{\mathrm{U}} = \lambda_{\mathrm{u}} v_{\mathrm{u}} \quad , \quad \lambda_{\mathrm{u}} = \mathrm{sign}(v_{\mathrm{u}}) \quad , \quad \mathrm{u = a, b, c}
\end{cases}
\tag{3.16}
$$

$$
\begin{cases}
v_{\mathrm{x}} = V_{\mathrm{m1}} \sin(\omega_1 t + \theta) \\[2mm]
v_{\mathrm{y}} = V_{\mathrm{m1}} \sin(\omega_1 t + \theta - 2\pi/3) \\[2mm]
v_{\mathrm{z}} = V_{\mathrm{m1}} \sin(\omega_1 t + \theta - 4\pi/3) \\[2mm]
v_{\mathrm{U}} = \lambda_{\mathrm{u}} v_{\mathrm{u}} \quad , \quad \lambda_{\mathrm{u}} = \mathrm{sign}(v_{\mathrm{u}}) \quad , \quad \mathrm{u = x, y, z}
\end{cases}
\tag{3.17}
$$

Now it is desired to develop voltage balancing equations for one phase of the MMMC (e.g. the phase between A and X). Similar to the previous section, the capacitor voltage balancing criteria is defined as:

$$
\left.
\begin{aligned}
\int_T \{p_{\mathrm{U1}}(t) + p_{\mathrm{L1}}(t)\}.dt = 0 \\[2mm]
\int_T p_{\mathrm{L1}}(t).dt = 0
\end{aligned}
\right\} \text{ voltage balancing criteria.}
\tag{3.18}
$$

The neutral terminal of the transformer is not grounded, thus the added third

harmonic voltage does not create current and cannot contribute to the power flow. As a result, similar to previous section, the first criterion of voltage balancing leads to the real power balance between the AC-sides.

The second criterion of voltage balancing eqs. leads to:

$$
\begin{aligned}
0 = \int_T & |V_{m2}\sin(\omega_2 t) + V_3\sin(3\omega_2 t + \beta)|.I_{m1}\sin(\omega_1 t + \theta - \varphi_1).\text{sign}(\sin(\omega_1 t + \theta)) \\
& + V_{m1}I_{m2}|\sin(\omega_1 t + \theta)|.\sin(\omega_2 t - \varphi_2).\text{sign}(\sin(\omega_2 t) + \frac{V_3}{V_{m2}}\sin(3\omega_2 t + \beta)) \\
& - \left\| |V_{m2}\sin(\omega_2 t) + V_3\sin(3\omega_2 t + \beta)| - V_{m1}|\sin(\omega_1 t + \theta)| \right\| \\
& \times \{ I_{m2}\sin(\omega_2 t - \varphi_2)\text{sign}(\sin(\omega_2 t) + \frac{V_3}{V_{m2}}\sin(3\omega_2 t + \beta)) \\
& + I_{m1}\sin(\omega_1 t + \theta - \varphi_1)\text{sign}(\sin(\omega_1 t + \theta)) \}.dt
\end{aligned}
\tag{3.19}
$$

The impact of phase angle shift θ and power factor are studied before. Thus, for simplicity, in this section, it is assumed that $\theta = \varphi_1 = \varphi_2 = 0$. Eq. (3.19) can be rewritten as:

$$
\begin{aligned}
0 = \int_T & |\sin(\omega_1 t)|.\sin(\omega_2 t).\text{sign}(\sin(\omega_2 t) + \gamma\sin(3\omega_2 t + \beta)) \\
& - M^2|\sin(\omega_2 t) + \gamma\sin(3\omega_2 t + \beta)|.|\sin(\omega_1 t)| \\
& + \left| M|\sin(\omega_2 t) + \gamma\sin(3\omega_2 t + \beta)| - |\sin(\omega_1 t)| \right| \\
& \times \{ M|\sin(\omega_1 t)| - \sin(\omega_2 t)\text{sign}(\sin(\omega_2 t) + \gamma\sin(3\omega_2 t + \beta)) \}.dt \\
& \text{where: } \gamma = \frac{V_3}{V_{m2}} \quad , \quad M = \frac{V_{m2}}{V_{m1}} = -\frac{I_{m1}}{I_{m2}}
\end{aligned}
\tag{3.20}
$$

First, the value of β is considered 0 and the impact of γ is studied:

$$
\begin{aligned}
0 = \int_T & |\sin(\omega_1 t)\sin(\omega_2 t)| - M^2|\sin(\omega_2 t) + \gamma\sin(3\omega_2 t)|.|\sin(\omega_1 t)| \\
& + \left| M|\sin(\omega_2 t) + \gamma\sin(3\omega_2 t)| - |\sin(\omega_1 t)| \right| \times \{ M|\sin(\omega_1 t)| - |\sin(\omega_2 t)| \}.dt
\end{aligned}
\tag{3.21}
$$

Figure 3.7 shows the impact of γ on the voltage gain($\beta = 0$).
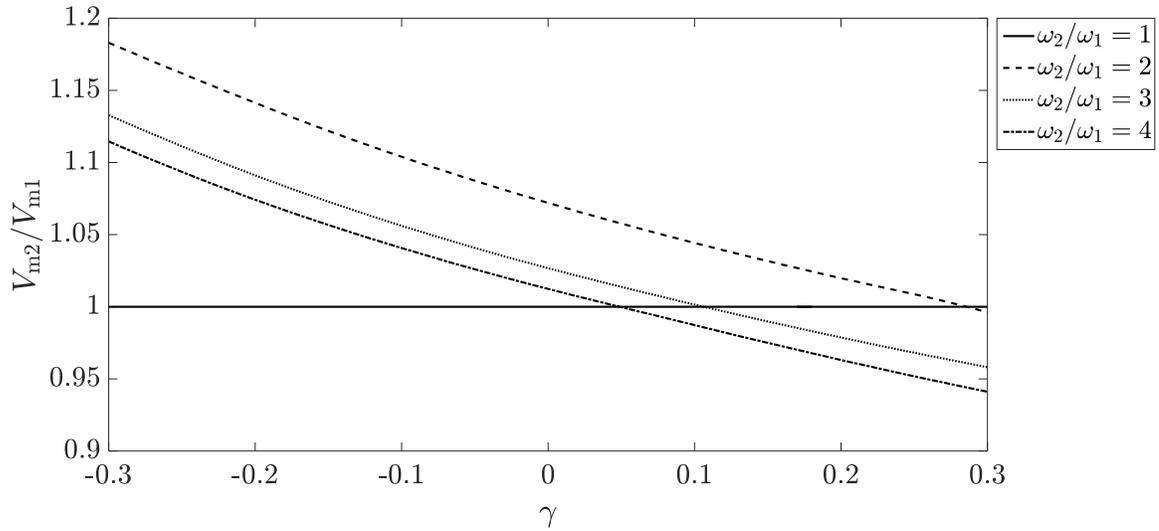
Figure 3.7. The voltage gain of MMMC versus γ.

Also, in Fig. 3.8, the value of γ is considered 0.3 and the impact of β on the voltage gain is presented.
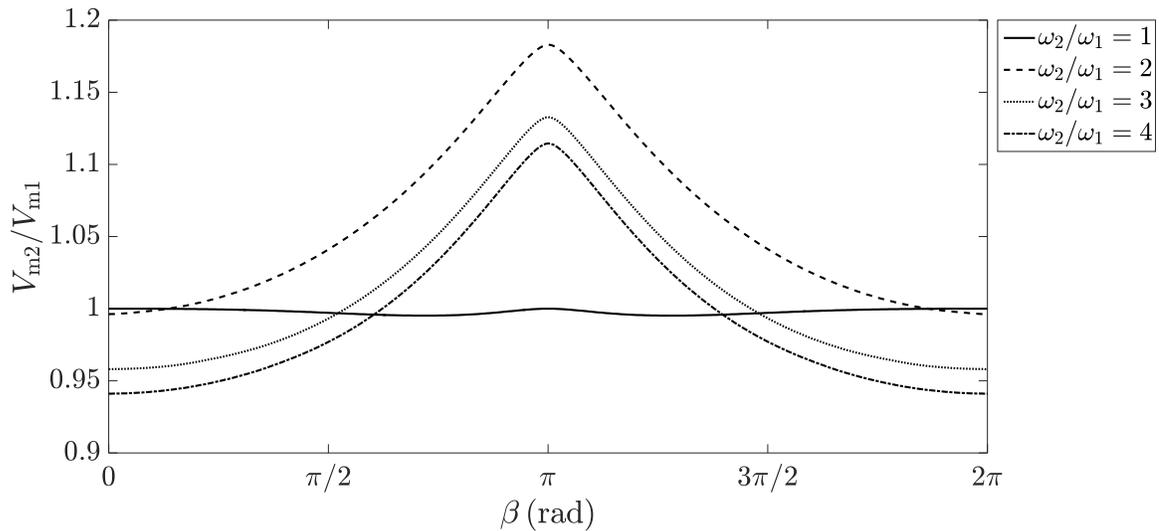
Figure 3.8. The voltage gain of MMMC versus β.

Thus, different values of voltage gain could be achieved by adjusting γ and β which must be included in design of the control strategy

3.4 Control Strategy
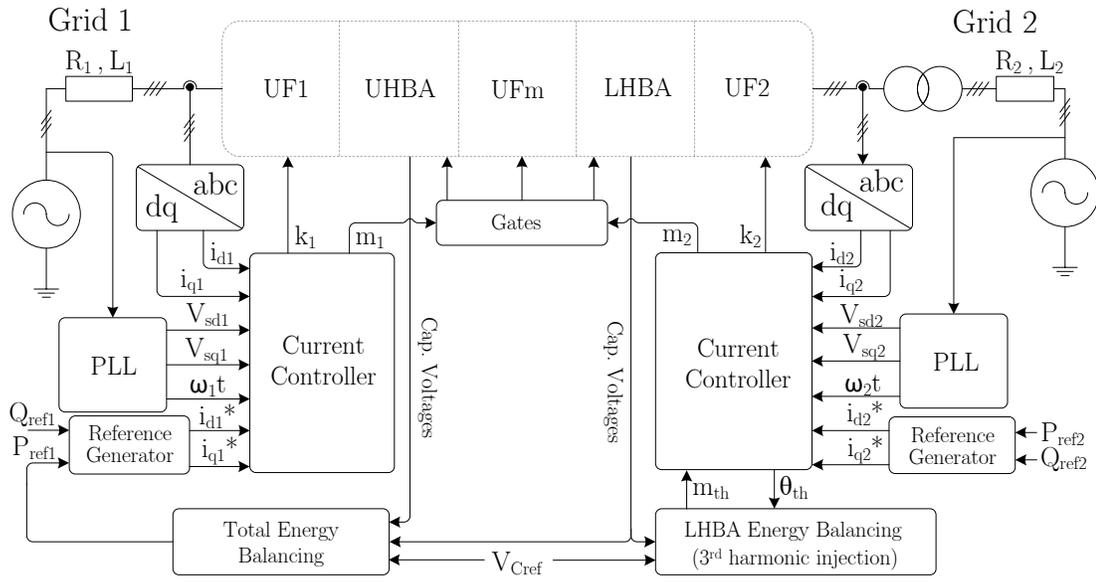
Figure 3.9. The schematic diagram of control strategy.
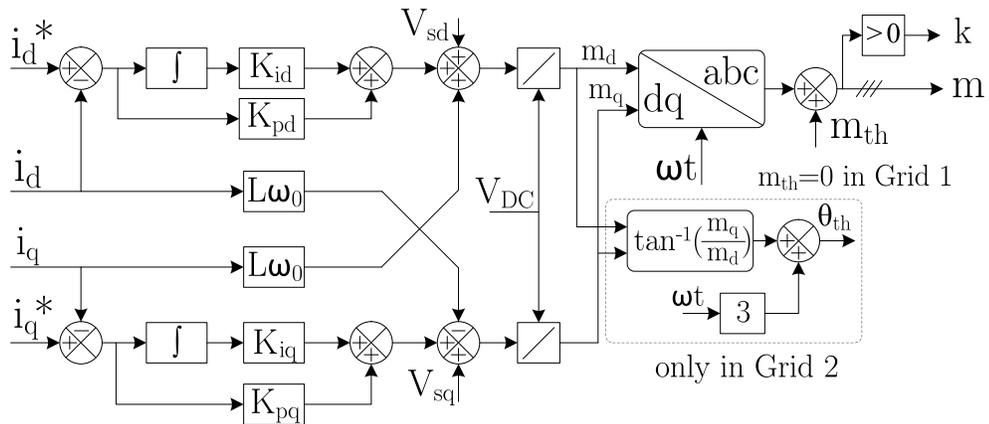
Figure 3.10. The schematic diagram of the current controller.
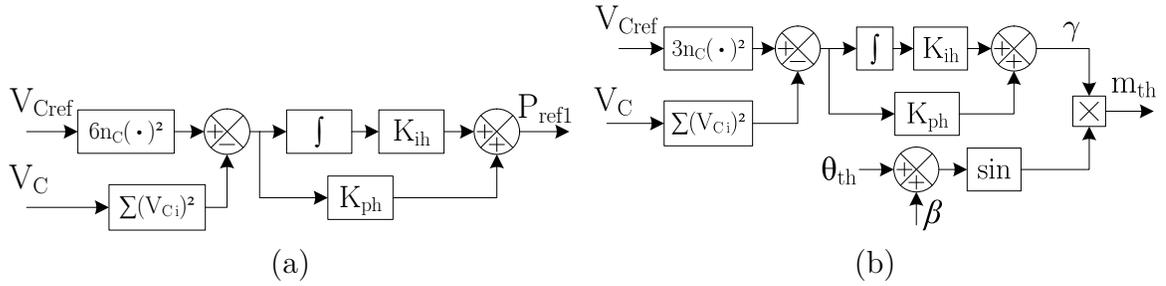
Figure 3.11. (a) Total energy balancing unit (b) LHBA energy balancing unit.

Figure 3.9 shows the schematic diagram of the control system for the proposed converter. On each side of the converter, a rotating dq-frame is utilized for controlling the AC current. This is done using a standard current controller depicted in Fig. 3.10, which provides the reference active and reactive powers exchanged with the grid. Here, P_{ref2} determines the amount and direction of transferred real power, whilst the reactive powers, Q_{ref1} and Q_{ref2} are regulated to arbitrary values within the converter rating. To ensure the power balance, a slow outer control loop shown in Fig. 3.11(a) is employed such that the total energy stored in the capacitors is effectively regulated at all time. In addition, a second energy balancing unit is utilized to distribute the stored energy equally in the arms. This is done by injecting third harmonic voltage on grid 2 side of the converter (see Fig. 3.11(b)). n_{C} is the total number of capacitors in each arm which is equal to $(n-1)/2$ in a n-level converter. It is also necessary to evenly distribute the arm energy between the HBSM capacitors by selecting the proper SMs at each time. This is done according to the sorted queue of capacitor voltages and arm current direction [26].

3.5   Simulation Results

The theoretical findings for a 3-phase converter shown in Fig. 3.2 are validated by simulation using MATLAB/Simulink software. The converter is rated for 4 MVA and

the transformer ratio is unity. The SM capacitors are operating in average voltage of 2 kV. Table 3.3 lists the main simulation parameters.

Table 3.3.
SIMULATION PARAMETERS

Parameter		Rating
Power rating	$S_{\text{conv.}}$	4 MVA
Grid 1 frequency	f_1	60 Hz
Grid 1 voltage (line-line rms)	V_{S1}	9 kV
Grid 2 frequency	f_2	50 Hz
Grid 2 voltage (line-line rms)	V_{S2}	9 kV
SM capacitor	C_{SM}	4 mF
No. of cells per arm	n_{C}	4
Mean capacitor voltage	E	2 kV
Filter+Grid inductance	$L_1,\ L_2$	10 mH
Filter+Grid resistance	$R_1,\ R_2$	10 mΩ

A multi-carrier PWM with effective frequency of 1800 Hz is applied to the main leg. By having four SMs in each arm, the switching frequency of SM IGBTs is 450 Hz, while the unfolder switches are operating at corresponding AC line frequency (60 Hz & 50 Hz). In practice, the number of levels is greater due to the higher grid voltage and power ratings. Figure 3.12 shows the steady state converter waveforms.

In this case, real power is flowing from the grid 2 to grid 1, while the power factor is unity. It can be seen that the third harmonic component of the voltage is canceled and the desired fundamental portion is well synthesized. The peak-to-peak ripple in the capacitor voltages shown in Fig. 3.13 is approximately 7% which may vary due to the *PQ* operating point of the converter.

To study the transient response of the converter, a few active and reactive power changes are applied as rising/falling ramps within 5 ms. As shown in Fig. 3.14, the desired operating point is properly controlled by its reference. During each transient,
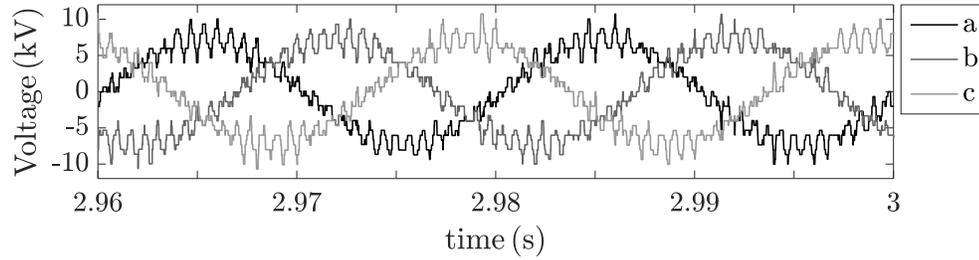
(a) Grid 1 phase voltages
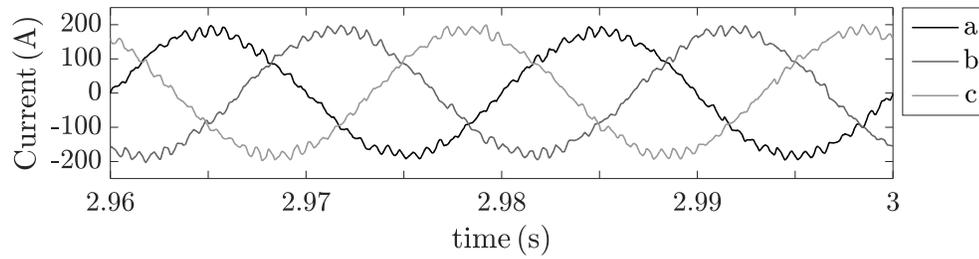
(b) Grid 1 line currents ($P = 2\,\text{MW}$, $Q = 0\,\text{MVAR}$)
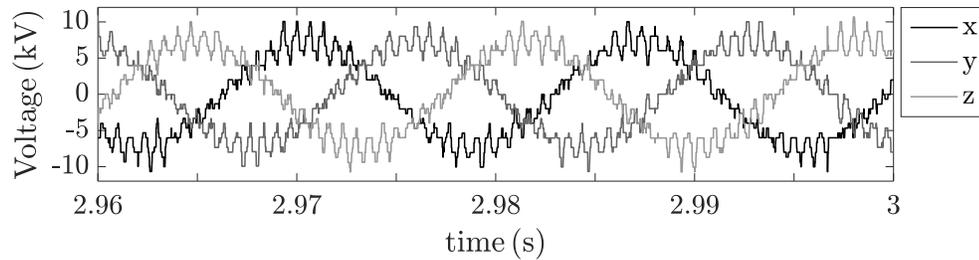
(c) Grid 2 phase voltages
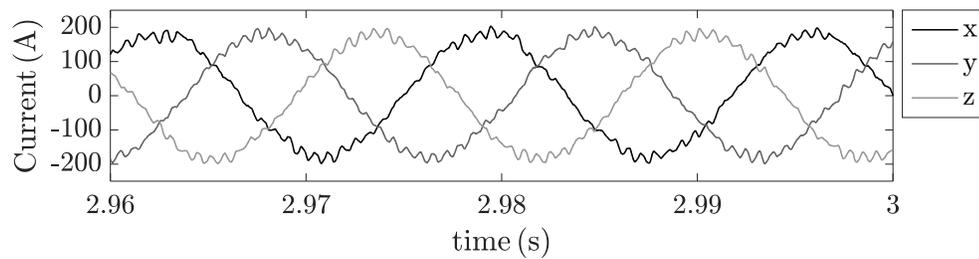
(d) Grid 2 line currents ($P = -2\,\text{MW}$, $Q = 0\,\text{MVAR}$)

Figure 3.12. Steady-state simulation results.
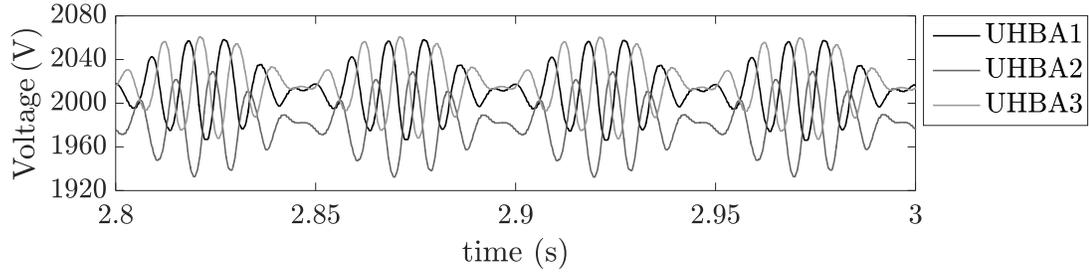
(a) Upper half-bridge arm capacitor voltages
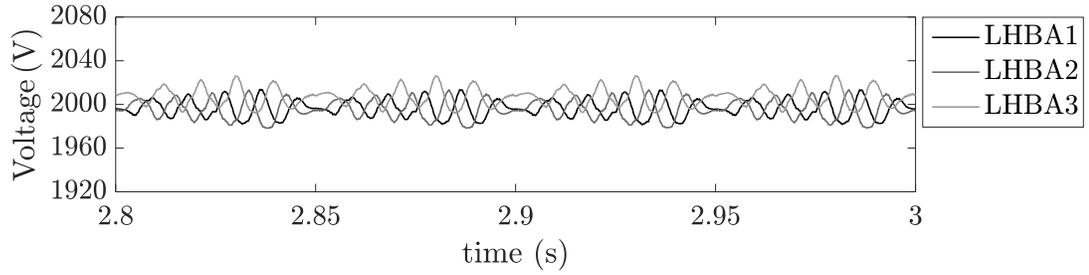
(b) Lower half-bridge arm capacitor voltages

Figure 3.13. Average arm capacitor voltages (steady state).

a small error may occur in the capacitor voltages which will be compensated in a few cycles.

3.6 Experimental Results

Although the simulation was performed on a 3-phase 4 MVA MMMC, due to limited resources in our laboratory, a low-voltage single-phase 5-level MMMC is constructed using MOSFET devices to perform experiments. The control system is implemented

Table 3.4.
EXPERIMENTAL PARAMETERS

Parameter		Rating
Supply side frequency	f_S	60 Hz
Load side frequency	f_L	50 Hz
SM capacitor	C_{SM}	820 μF
Mean SM-capacitor voltage	E	25 V
Filter inductance	L_S, L_L	5 mH
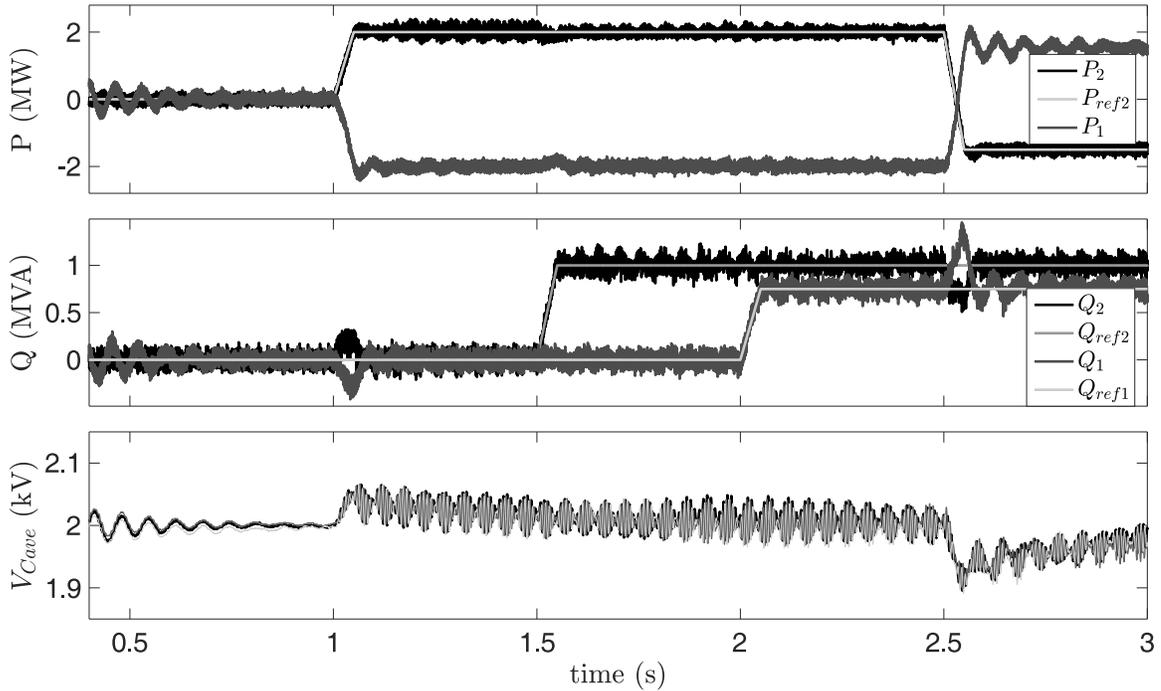
Figure 3.14. Converter transient response.

on a dSPACE-MicroLabBox unit. One side of the converter is connected to the AC voltage source (60 Hz), while the other side feeds a resistive load operating 50 Hz. The parameters of the experimental setup can be found in Table 3.4. Here, the switching frequency of 3 kHz is applied to the SM switches which could be reduced by utilizing higher number of SMs. The converter's AC-side waveforms in the steady-state condition are shown in Figs. 3.15 and 3.16, respectively. Both side currents are measured as they exit the converter and the voltages are measured before the AC-side filters. It can be seen that both side voltages are well synthesized with the expected amplitude and frequency. Figure 3.17 shows the measured SM capacitor voltages in the steady-state condition. They are well regulated around their desired average voltage which is 25 V.
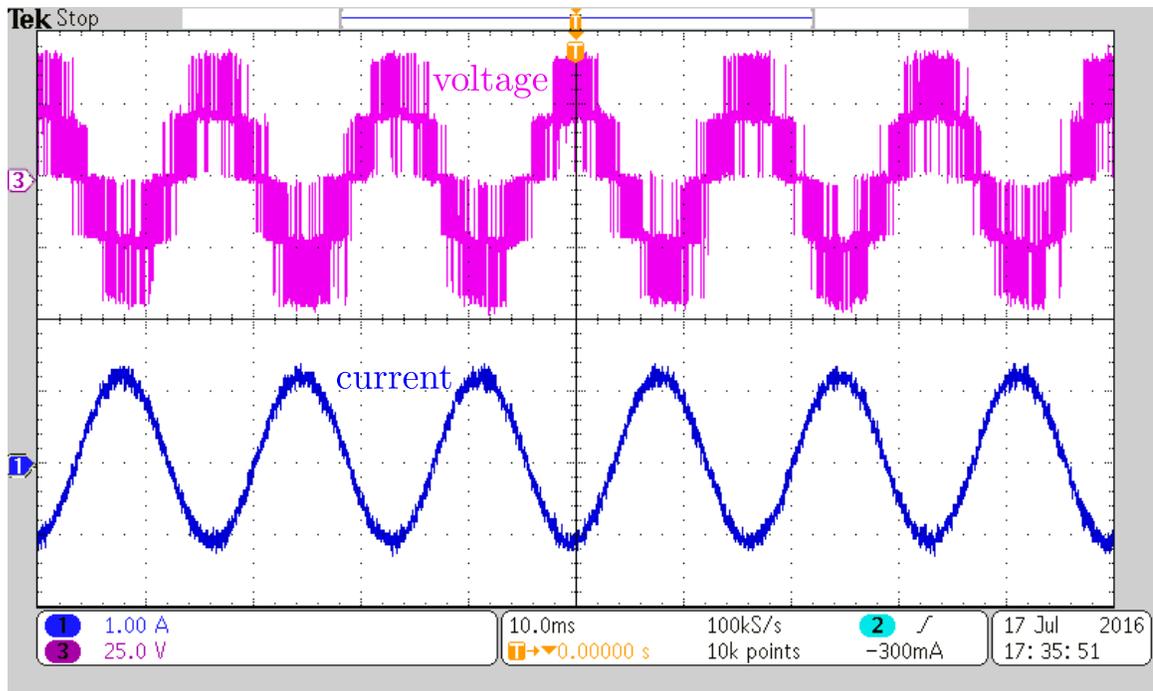
Figure 3.15. Converter's supply-side waveforms in steady-state condition.
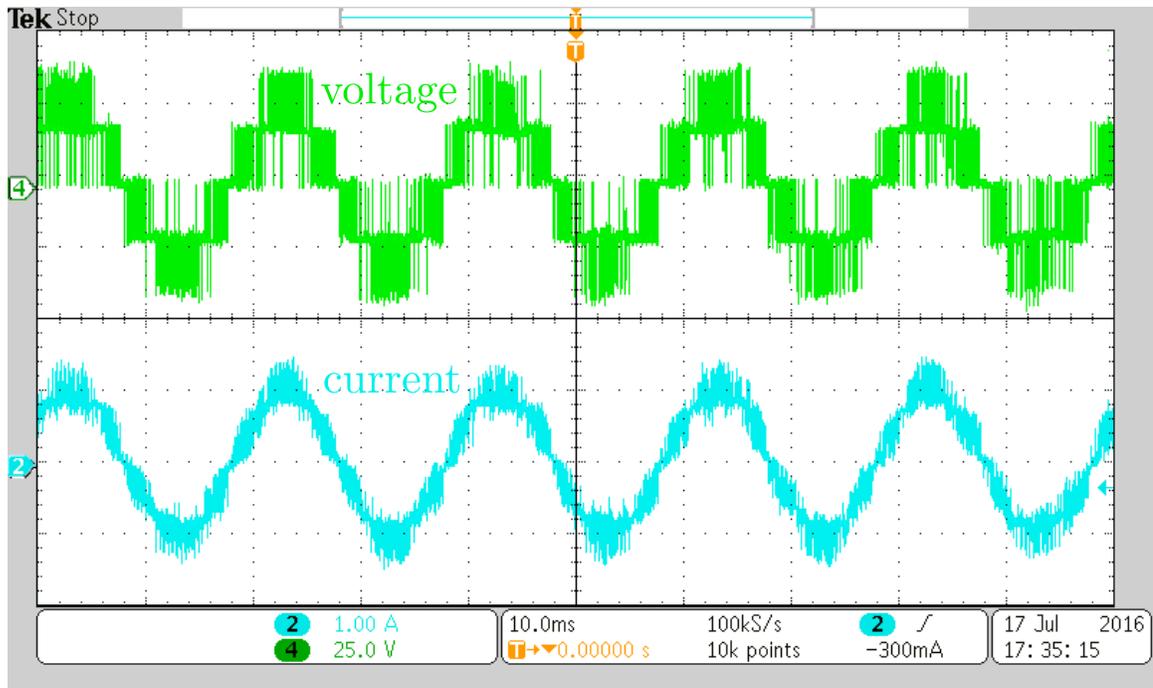
Figure 3.16. Converter's load-side waveforms in steady-state condition.
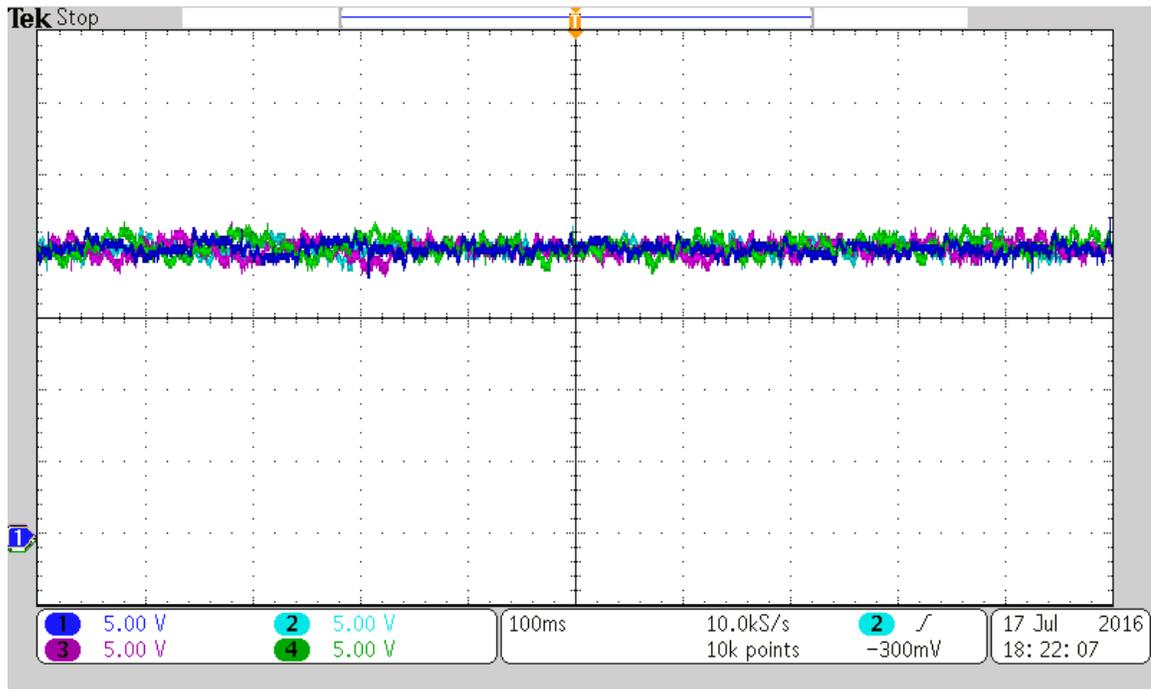
Figure 3.17. Capacitor voltages in steady-state condition.

3.7 Summary

In this chapter, another converter called MMMC intended for high power AC/AC applications such as the HFHW system was proposed. It was shown that the MMMC can further reduce the number of hard-switched IGBTs compared to the SMMC. Similar to the SMMC, a control strategy was developed to regulate the required active/reactive power exchanged between the AC grids and to guarantee the capacitor voltage balancing of the converter. Finally, the theoretical discussion was confirmed by both simulation and experimental results.

Chapter 4

High Frequency Half-Wavelength Transmission Line

4.1   Introduction

As mentioned in Chapter 1, in a HFHW system, it is proposed to generate and transfer power at higher frequencies to shorten the half-wavelength distance, and interconnect the high-frequency portion to the rest of the power system using a high power AC/AC converter [1]. In this chapter, the economical aspect of the HFHW system components including the AC/AC converter is studied.

4.2   Half-Wavelength Transmission Line

A long-distance transmission line can be approximated as a lossless line for transmission capacity studies. For such a line, the voltage and current at distance x from the

receiving end (V_x and I_x, respectively), can be determined as:

$$
\begin{bmatrix} V_x \\ I_x \end{bmatrix} = \begin{bmatrix} \cos(\alpha x) & jZ_c \sin(\alpha x) \\ j\sin(\alpha x)/Z_c & \cos(\alpha x) \end{bmatrix} \cdot \begin{bmatrix} V_r \\ I_r \end{bmatrix},
\tag{4.1}
$$

where, V_r and I_r are the voltage and current at the receiving end, respectively. Z_c is the surge impedance of the line which equals to $\sqrt{L_0/C_0}$ for a lossless line. Also, $\alpha = 2\pi/\lambda$ and λ is the wavelength.

For pu representation, Eq. (4.1) can be rewritten as:

$$
\begin{bmatrix} V_X \\ I_X \end{bmatrix} = \begin{bmatrix} \cos\left(\frac{2\pi x}{\lambda}\right) & j\sin\left(\frac{2\pi x}{\lambda}\right) \\ j\sin\left(\frac{2\pi x}{\lambda}\right) & \cos\left(\frac{2\pi x}{\lambda}\right) \end{bmatrix} \cdot \begin{bmatrix} V_R \\ I_R \end{bmatrix}.
\tag{4.2}
$$

In Eq. (4.2), all the voltage and current values are in terms of pu. For a HWTL, if the value of x equals to $\lambda/2$, then V_X and I_X represent the voltage and current of the sending end, respectively. Thus:

$$
\begin{bmatrix} V_S \\ I_S \end{bmatrix} = \begin{bmatrix} \cos\pi & j\sin\pi \\ j\sin\pi & \cos\pi \end{bmatrix} \cdot \begin{bmatrix} V_R \\ I_R \end{bmatrix} = \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \cdot \begin{bmatrix} V_R \\ I_R \end{bmatrix},
\tag{4.3}
$$

where, V_S and I_S are the voltage and current at the sending end, respectively. Equation (4.3) implies that there is zero impedance between the sending and receiving end of the line, as if the line did not exist. The line only changes the phase of the voltage and current. For implementation, the line shall be slightly longer than the $\lambda/2$ to avoid stability problems [5]. Some of the advantages of a HWTL are:

- The voltage magnitude in the sending and receiving ends of the line are very similar and do not depend on the load level;

- There is no stability concern;

- There is no Ferranti effect concern;

- There is no need for reactive power compensation, since the line inherently generates the absorbed reactive power, along its length.

In the HFHW system, the frequency of generation and transmission is chosen based on the distance between the generation site and 60 Hz grid, which is half of the wavelength. This is formulated as:

$$f = \frac{v}{\lambda_{\mathrm{f}}} = \frac{v/2}{\lambda_{\mathrm{f}}/2} = \frac{v}{2d_{\mathrm{line}}}, \tag{4.4}$$

where v is roughly equal to the speed of light, λ_{f} is the wavelength in frequency of f and d_{line} is the line length.

4.2.1 HWTL Voltage and Current Profiles

In this section, the impact of transferred power on the HWTL voltage and current behavior along the line is studied. The amount of transmitted power is defined as a factor of Surge Impedence Loading (SIL), or natural loading, being the power loading at which reactive power is neither produced nor absorbed. The SIL depends on the line geometry and is calculated as:

$$\mathrm{SIL} = P_{\mathrm{c}} = \frac{V_{\mathrm{r}}^2}{Z_{\mathrm{c}}} \rightarrow P_{\mathrm{C}} = 1\,\mathrm{pu}, \tag{4.5}$$

where, V_{r} is the line-to-line voltage measured at the receiving end of the transmission line. Here, it is assumed that the amplitude of sending end voltage is equal to 1 pu.

As obtained in Eq. (4.3), the amplitude of sending and receiving end voltages for a HWTL are equal, thus $|V_S| = |V_R| = 1$ pu. If the load is pure resistive and its impedance equals $Z_l = Z_c/k$, then the amount of load demand, P_r in terms of SIL can be presented as:

$$P_r = \frac{V_r^2}{Z_l} = k \times P_c \rightarrow P_R = k \text{ pu.} \tag{4.6}$$

Also the current at receiving end can be expressed as:

$$I_r = \frac{V_r}{Z_l} = \frac{kV_r}{Z_c} \rightarrow I_R = k \text{ pu.} \tag{4.7}$$

Substituting Eq. (4.7) in Eq. (4.2) gives:

$$\begin{cases} V_X = \cos\left(\dfrac{2\pi x}{\lambda}\right) + jk\sin\left(\dfrac{2\pi x}{\lambda}\right) \\ I_X = j\sin\left(\dfrac{2\pi x}{\lambda}\right) + k\cos\left(\dfrac{2\pi x}{\lambda}\right). \end{cases} \tag{4.8}$$

If $\theta = 2\pi x/\lambda$, then the amplitude of V_X and I_X can be expressed as:

$$\begin{cases} |V_X| = \sqrt{\cos^2\theta + k^2\sin^2\theta} = \sqrt{1 + (k^2 - 1)\sin^2\theta} \\ |I_X| = \sqrt{\sin^2\theta + k^2\cos^2\theta} = \sqrt{1 + (k^2 - 1)\cos^2\theta} \end{cases} \tag{4.9}$$

In the middle of the line, the voltage and current amplitude can be obtained as:

$$x = \frac{\lambda}{4} \rightarrow \theta = \frac{\pi}{2} \rightarrow \begin{cases} |V_M| = k \text{ pu} \\ |I_M| = 1 \text{ pu} \end{cases} \tag{4.10}$$

where, V_M and I_M are the voltage and current in the middle of the line. Thus, the voltage in the middle point of the HWTL is proportional to the transferred power,
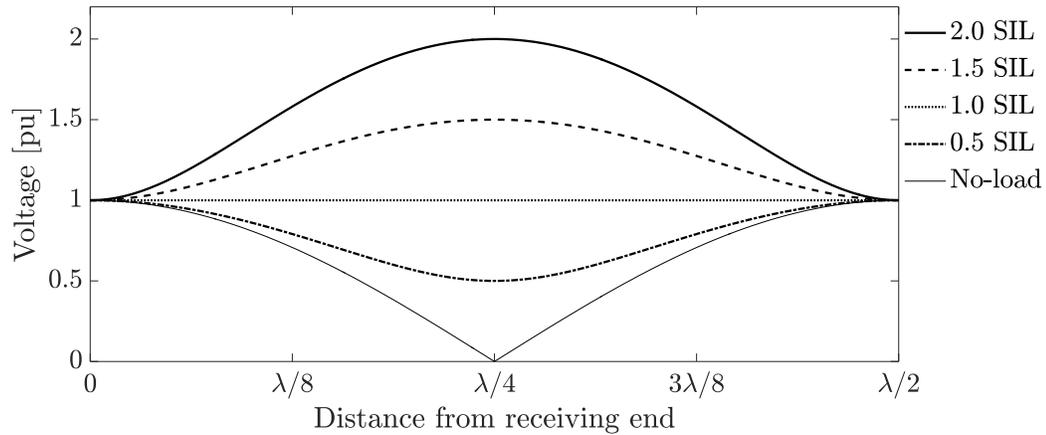
Figure 4.1. Voltage profile in HWTL in regards to different load levels.
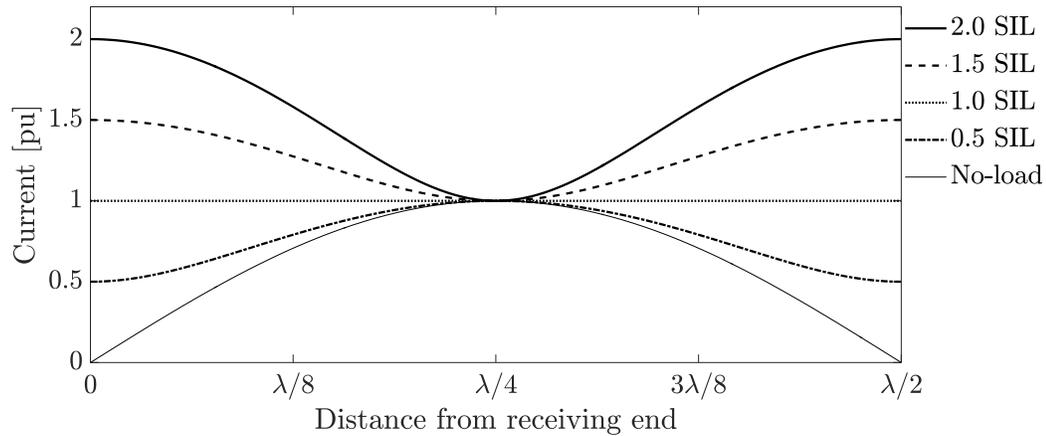
Figure 4.2. Current profile in HWTL in regards to different load levels.

while its current is constant and independent from the transferred power. Figures 4.1 and 4.2 show the pu voltage and current profiles across the line in regards to different load levels, respectively. It can be seen that the line middle-point voltage is one of the restrictions that must be considered in the HWTL utilization and thus, the amount of power transferred through HWTL cannot exceed 1 SIL (see Fig. 4.1). Since the line middle-point current is 1 pu at all conditions, for load levels not higher than 1 SIL, HWTL has the least conduction loss when the load equals to 1 SIL (see Fig. 4.2).

4.2.2 HWTL Loadability Limit

Generally, the loadability of a line is limited by the following constraints [37]:

- **Thermal limit:** For a short line, the heating of conductors due to line losses is considered as thermal limit.

- **Angular stability limit:** It is related to the ability of the power system and the individual generators to maintain synchronism after an operational disturbance.

- **Voltage stability limit:** It defines the theoretical maximum possible power transferred to the load.

- **Voltage quality limit:** It defines the practical maximum possible power transferred to the load.

In the proposed HFHW scheme, a long HWTL is connected between a generator and the power grid. Thus, the voltage in both sending and receiving ends is independent from the transferred power. Thus, following observations could be made:

- Thermal limit is not considered here, as the transmission line in the proposed scheme is very long.

- Angular stability limit is not a concern, since both ends of the HWTL are inherently in phase.

- Both voltage stability and quality limits are not considered here, as the receiving end voltage does not depend on the transmitted power.

Therefore, the only restriction for the loadability of HWTL is the middle-point voltage magnitude. As presented in Fig. 4.1, transmitting power higher than $1\,\mathrm{SIL}$ causes overvoltage in the middle-point. Therefore, the practical maximum possible active power which can be transmitted through the proposed HFHW is $1\,\mathrm{SIL}$.

4.2.3 Loadability of HWTL versus Conventional AC line

To have a fair comparison, a conventional long-distance High Voltage Alternating Current (HVAC) transmission line constructed between a generator and power grid is studied. Based on aforementioned discussion, the angular stability limit is the major loadability restriction in this case. Transmission line loadability curve, also known as St. Clair curve [38] is used here to analyze the line. This curve shows the loadability of transmission line in terms of its SIL regardless of its voltage level. First, SIL and surge impedance are defined as below:

$$\mathrm{SIL} = \frac{V_{\mathrm{rated}}^2}{Z_{\mathrm{Surge}}} \ , \ \ Z_{\mathrm{Surge}} = \sqrt{\frac{L_0}{C_0}} = \sqrt{\frac{X_0}{B_0}}, \tag{4.11}$$

where, L_0 and C_0 are inductance and capacitance per-unit-length of the line, respectively. Also, X_0 and B_0 are reactance and susceptance per-unit-length of the line, respectively. Note that the unit length of the line is $1\,\mathrm{km}$. It is well known that the per-unit line data which is normalized using SIL and Surge Impedance is constant, i.e. independent of line construction and voltage rating as follows:

$$X_{\mathrm{pu/km}} = \frac{X_0}{Z_{\mathrm{Surge}}} = \frac{X_0}{\sqrt{X_0/B_0}} = \sqrt{X_0 B_0} = \sqrt{L_0 C_0} = \frac{2\pi f}{v} \tag{4.12}$$

$$B_{\mathrm{pu/km}} = \frac{B_0}{1/Z_{\mathrm{Surge}}} = \frac{X_0}{\sqrt{B_0/X_0}} = \sqrt{X_0 B_0} = \sqrt{L_0 C_0} = \frac{2\pi f}{v}, \tag{4.13}$$

where, v is roughly equal to the speed of light $(300{,}000\,\text{km/s})$ and f is frequency of the voltage. As an example, using Eq. (4.12), per-unit line data for a $60\,\text{Hz}$ system can be determined as follows:

$$X_{\text{pu/km}} = B_{\text{pu/km}} = \frac{2\pi f}{v} = \frac{2\pi 60}{300000} = 0.00126\,\text{pu/km}. \tag{4.14}$$

Therefore, the total line reactance in pu can be obtained as:

$$X_{\text{pu}} = X_{\text{pu/km}} \times d = 0.00126 d\,\text{pu}, \tag{4.15}$$

where, d is the length of the line in km. The angular stability limit is determined as [37]:

$$P = \frac{VE}{X} \sin \delta, \tag{4.16}$$

where, V and E are receiving and sending voltage magnitudes, respectively. δ is the rotor angle and X is the line reactance. It is assumed that the magnitude of V and E are both equal to $1\,\text{pu}$. Also, the rotor angle $44°$ (the corresponding stability margin is 30%) is selected as the angular stability limit [39]. Using Eq. (4.15), Eq. (4.16) can be rewritten in pu as:

$$P_{\text{max-pu}} = \frac{1}{X_{\text{pu/km}} \times d} \sin 44° = \frac{555}{d}, \tag{4.17}$$

Note that Eq. (4.17) is valid for long transmission line, as in short line, thermal limit is the main restriction. Figure 4.3 shows the allowable line operational area without exceeding the thermal and angular stability limits.
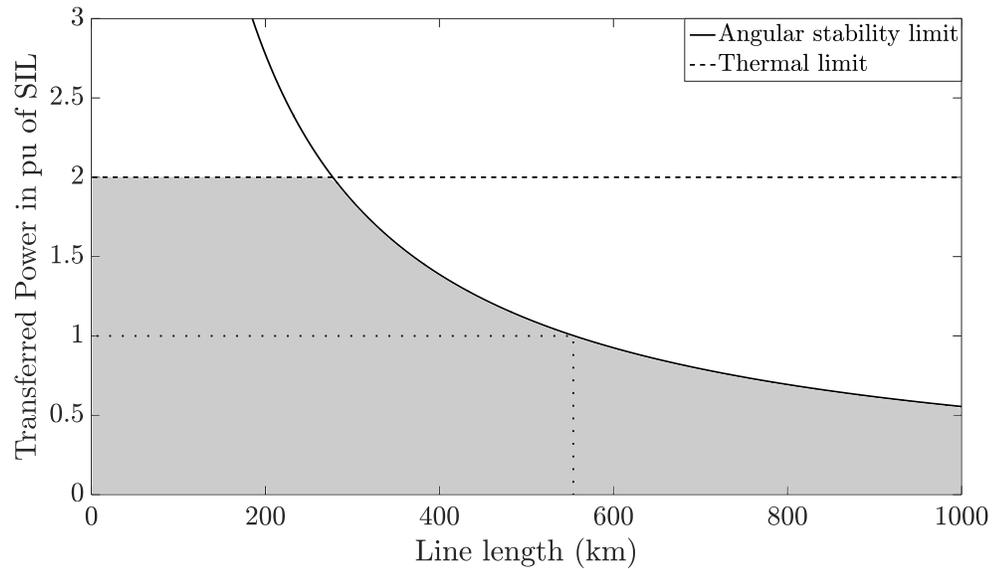
Figure 4.3. Loadability curves of AC transmission line.

Thermal limit is almost independent from the line length and it greatly depends on the type and size of the conductor as well as the number of bundles in the conductor. Here, as an example, a constant power limit of 2 pu of SIL is considered for thermal limit.

It can be concluded that for distances longer than 555 km, the proposed HFHW is capable of transmitting more power, as the loadability of HWTL is fixed and equal to 1 pu of SIL.

In the next section, other components of the HFHW scheme are studied.

4.3 Other System Components

4.3.1 High Frequency Generator

The rotation speed of an industrial steam turbine is quite flexible and can be as high as 20000 rpm. For example, steam turbine SST-600 produced by Siemens has

a speed range varying from 3000 to 18000 rpm, and has been widely used for power generation. Hence, High Frequency (HF) power generation is easy to implement. In fact, running a turbine at a higher speed has two benefits [40]:

- **Higher efficiency and lower cost:** Each steam turbine has its optimum rotation speed where the efficiency is the highest. Normally, this speed is higher than the generator's speed. Existing solutions to deal with this issue is to use a gearbox, which causes extra energy loss and requires cooling system. The proposed transmission scheme can increase the generator speed and hence the efficiency could be improved with the elimination of the gearbox

- **Turbine-set size:** The power developed at the turbine shaft is a function of the developed torque and its rotation speed. If the turbine speed increases, then a smaller diameter turbine would be required to maintain the same power, thus reducing the cost and size.

As for a hydro power unit, its rotation speed can be also increased through hydraulic design. Increasing the number of poles may not be an option since hydro generators usually have several poles. According to the relationship between the generator speed N_s and its pole number (P), $f = N_s \times P/120$, sample combinations of N_s and P to produce various half-wavelength as it is shown in Table 4.1.

Table 4.1.
LINE LENGTH REGARDING GENERATOR'S NUMBER OF POLE (P) & SPEED (N_s)

P \ N_s (rpm)	3600	7200	14400
2	**2500 km (60 Hz)**	**1250 km (120 Hz)**	**625 km (240 Hz)**
4	**833 km (180 Hz)**	417 km (360 Hz)	208 km (720 Hz)
6	417 km (360 Hz)	208 km (720 Hz)	104 km (1440 Hz)

4.3.2 High Frequency Transformer

Two custom-made HF transformers are needed for the scheme. At higher frequencies, a transformer can be implemented using a smaller size and weight for the same power level. It is worth mentioning that high voltage transformers are always custom-made even at 60 Hz. Therefore, the proposed scheme does not add excessive cost for the transformer procurement. The proposed HFHW scheme could be beneficial up to roughly 300 Hz. In [41], the design process of two transformers in 60 Hz and 180 Hz are studied.

4.3.3 Unidirectional AC/AC Converter

The proposed transmission scheme is unidirectional which means, the active power always flows from sending end to the receiving end. Thus, it requires a unidirectional AC/AC converter station at the receiving end terminal.

4.4 Economical Study

As concluded in Section 4.2.3, for distances longer than 555 km, the HFHW transmission scheme can carry more power compared to conventional HVAC line. However, the HFHW scheme requires an additional converter station and all the other components such as generator, line and transformers must be designed to operate at a higher frequency. To identify the most cost-efficient approach, this section studies the economical aspects of the HFHW scheme and compares them with conventional HVAC and HVDC alternatives. Based on the inherent characteristics of HFHW, HVAC and HVDC transmission systems, some initial observation could be made:

- In general, for the same power rating, the transformer designed to operate in a higher frequency is smaller, lighter and less-expensive [41].

- The terminal cost of HFHW is lower than HVDC alternative, as in the HVDC system, both terminals require a converter station.

- The terminal cost of HFHW is higher than HVAC alternative, as the HVAC system does not require converter station.

To have a more accurate cost assessment, all the major terminal components (generator, transformer and converter) must be studied in terms of their cost.

4.4.1 Converter Station

Figure 4.4 shows the the alternative HVDC transmission line with its converter station. As the power flow is unidirectional, a 12-pulse diode-bridge is used in the sending-end. Figures 4.5(a) and 4.5(b) illustrate the HFHW scheme using conventional MMC and unidirectional SMMC introduced in Chapter 2, respectively.
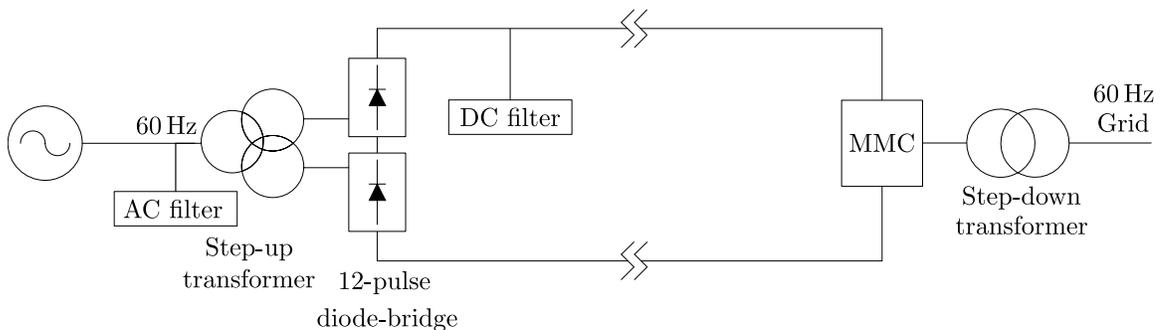
Figure 4.4. The unidirectional HVDC transmission scheme.

A typical cost structure for a B2B converter station (including converter transformer) is shown in Fig. 4.6 [42]. To compare the converter cost for different trans-

(a) HFHW scheme with MMC

(b) HFHW scheme with SMMC
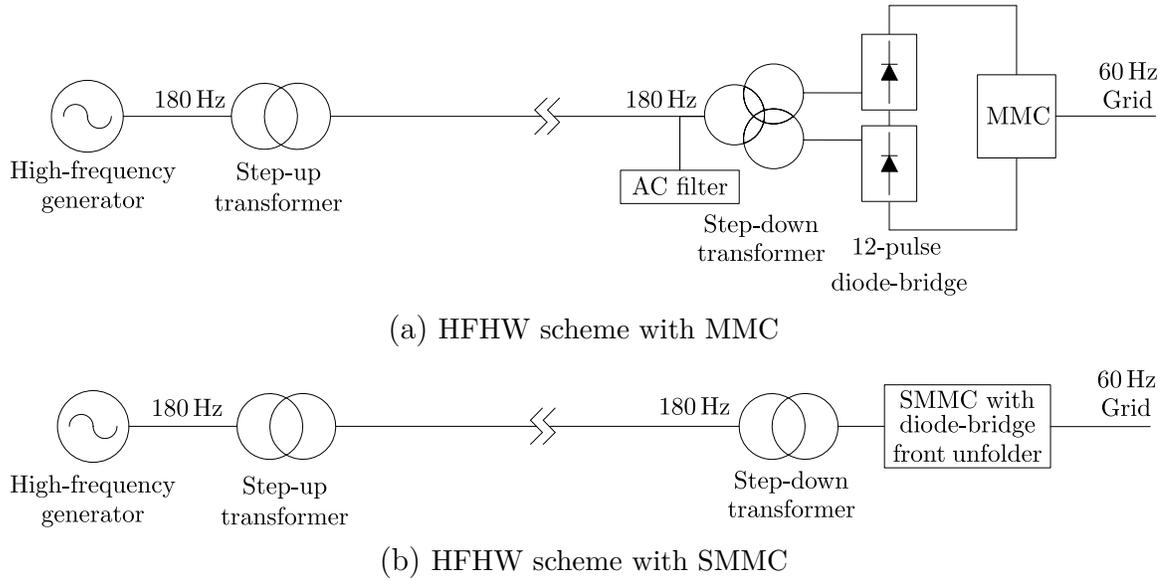
Figure 4.5. Different transmission lines with their converters.
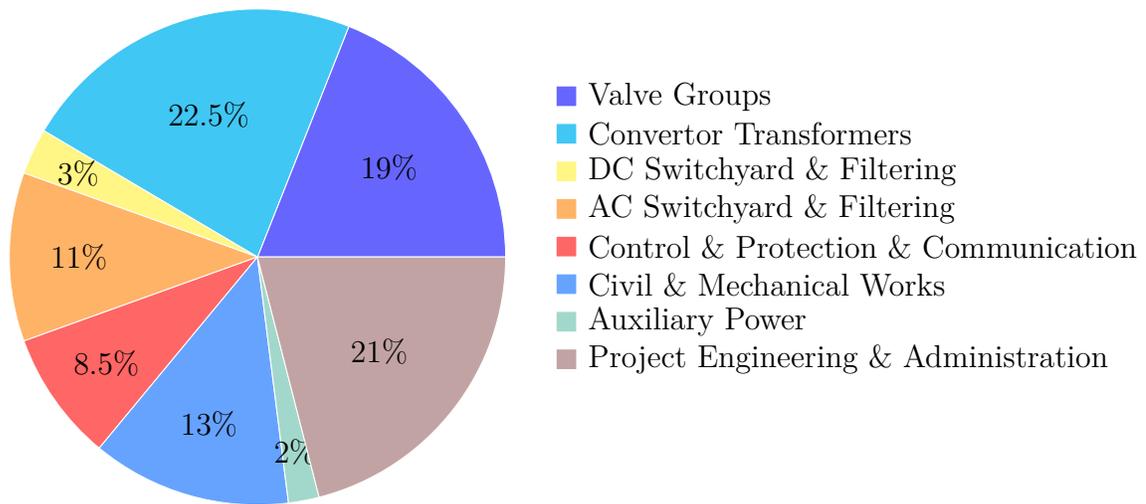
Figure 4.6. Cost structure of a back-to-back HVDC station.

mission lines, a few points must be made: i) Unlike the HVDC stations, the AC/AC converter in the HFHW scheme is placed in the low-voltage side and one location. The capital cost breakdown of MMC is not available in the literature, but as a rough estimation, for a given power the cost for the HFHW's converter is almost halved

[42], ii) The AC filter in MMC-based HFHW is smaller as it is designed to filter higher frequency harmonics. iii) Unlike HVDC and MMC-based HFHW, the SMMC topology does not require special converter transformer or filtering.

4.4.2 Power Plant

The turbine, generator and step-up transformer belong to a bigger system component which is the power plant. For example, in a combined-cycle power plant, the costs of gas turbine-set, steam turbine-set and electrical parts (mainly step-up transformer) are 32%, 8% and 9% of the total cost, respectively as shown in Fig. 4.7 [43].
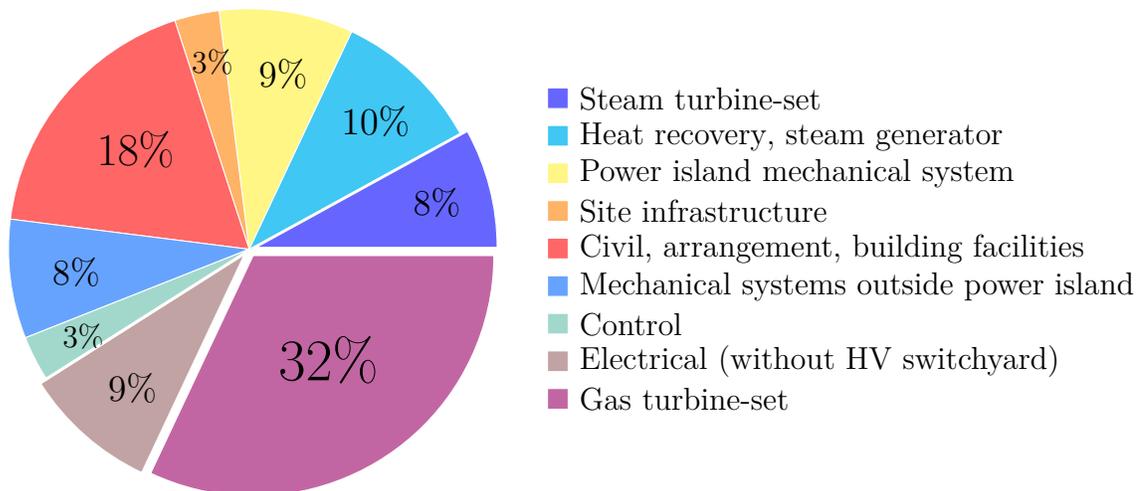
Figure 4.7. Breakdown of the capital cost for combined-cycle power plant.

In HFHW scheme, the power plant is designed to generate the electricity in a frequency higher than 60 Hz. With this approach, the following components must be redesigned and studied in term of their costs.

4.4.2.1 Turbine-Set

Turbine-set includes both turbine and the electrical generator. One of the parameters that can increase the turbine efficiency is to design in a higher speed of rotation. However, when high-speed turbines are used to drive generator, a gearbox must be incorporated to reduce the high speed of the turbine. The higher efficiency and lower cost of the high-speed turbine outweighs the additional cost of the gearbox as well at the losses caused by the speed reduction [40].

In this case study, the turbine's speed of rotation is assumed to be 10,800 rpm. In HFHW scheme there is no need for a reduction gearbox, since the generator operates at frequency of 180 Hz. However, in both HVDC and conventional HVAC schemes, a gearbox with reduction ratio of 3:1 is utilized. The efficiency of this gearbox is around 98% [44].

Although it can be expected that the turbine-set operating in 180 Hz is cheaper, however due to lack of information at this stage, the worst case scenario is considered. This means both turbine-sets (60 Hz and 180 Hz) cost the same.

4.4.2.2 Transformer

The cost of the step-up transformer is almost 9% of the total cost the power plant. To compare the transformer cost in different transmission approaches, two 750 kVA transformers are designed to operate in 60 Hz and 180 Hz frequencies [41]. Then, they are compared in terms of their Total Owing Cost (TOC). The TOC takes into account not only the initial transformer cost but also the cost to operate and maintain the transformer over its lifetime. Based on this comparison this comparison, the TOC for 750 kVA transformers in 60 Hz and 180 Hz is US$ 52934.42 and US$ 49040.88, respectively. Thus, the transformer in the higher frequency is 7.36% cheaper. Even

though, the step-up transformers used in the power plant are much bigger, yet these values could roughly estimate their cost comparison. Based on this information, the relative cost breakdown of the power plant for different transmission systems could be represented as shown in Fig. 4.8.
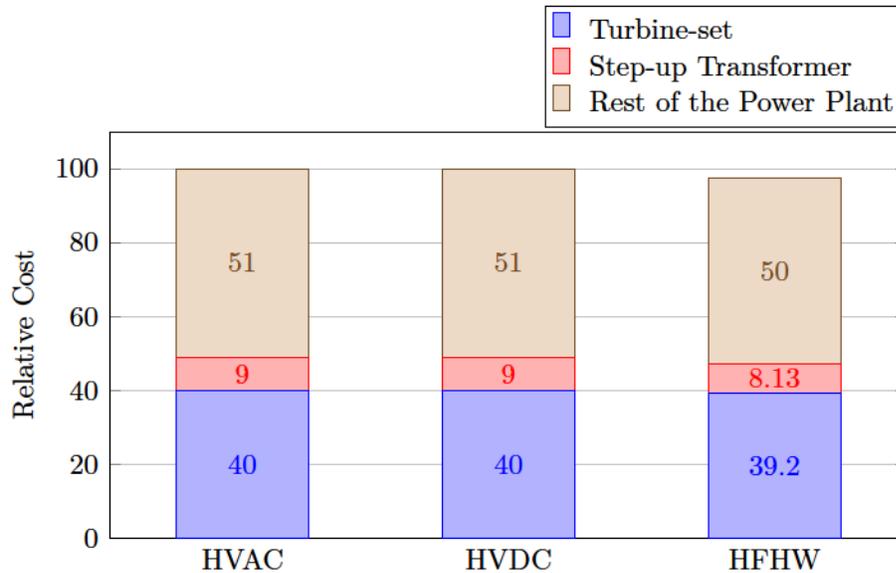
Figure 4.8. Relative power plant cost breakdown.

Based on the results from converter station and power plant for different transmission schemes, the relative terminal cost is summarized in Fig. 4.9.

4.4.3 Transmission Line

The transmission line used for conventional HVAC and HFHW systems are identical and thus they cost the same. However, they are 39% more expensive compared to HVDC line in terms of their yearly cost [45]. It must be noted that unlike HVAC line, the voltage level of HWTL and HVDC schemes does not depend on the line length. This is one of the key benefits of HWTL as the transmission voltage level increases discretely. Figure 4.10 represents the capability of AC and DC transmission lines in

different voltage levels and distances [46]. To observe the impact of discrete voltage level increase, the cost of different lines is compared for a 1000 MW case. As shown in Fig. 4.11, for an HVAC line longer than 555 km, a higher voltage level must be selected compared to HFHW scheme.

4.5 Summary

In this chapter, a cost comparative study was conducted to emphasize the economical opportunity of the HFHW transmission system. To do so, a case study of 180 Hz HFHW along with its conventional alternatives were compared in detail. The unidirectional SMMC was utilized at the receiving-end of the HFHW system as the required AC/AC converter. It was shown that the proposed AC/AC converter does not inject harmonic to the the line, and thus it does not require AC-filter or special transformer. It was also shown that the HFHW system costs less compared to
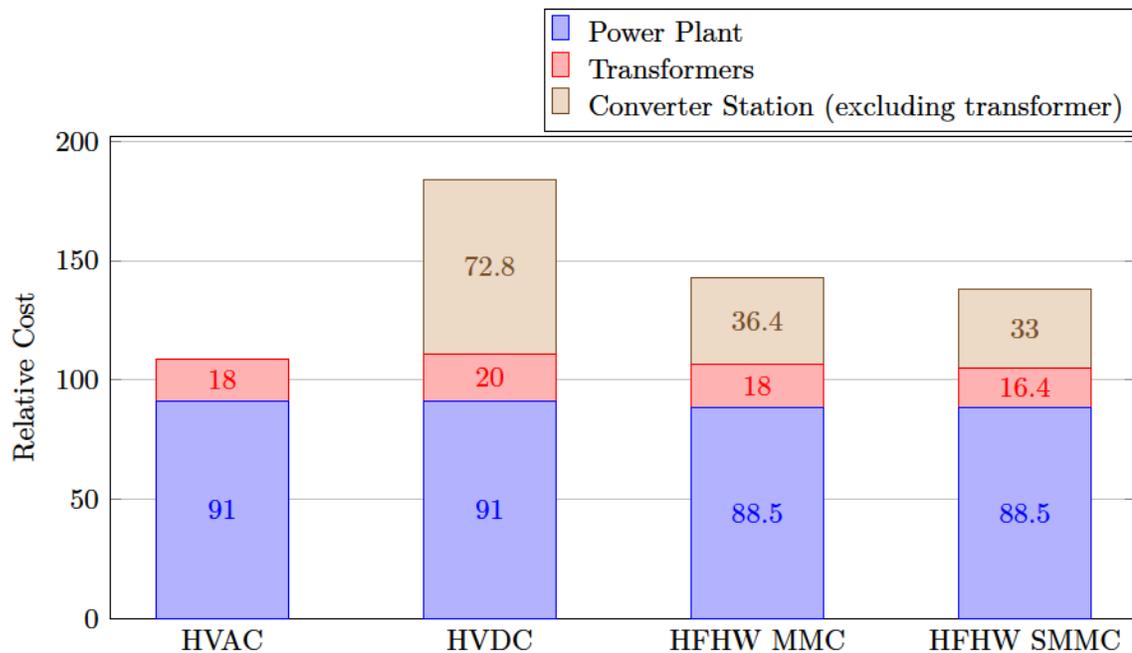
Figure 4.9. Relative terminal cost breakdown of different transmission systems.

Max Line Capability vs. Distance with 3000 A Ratings
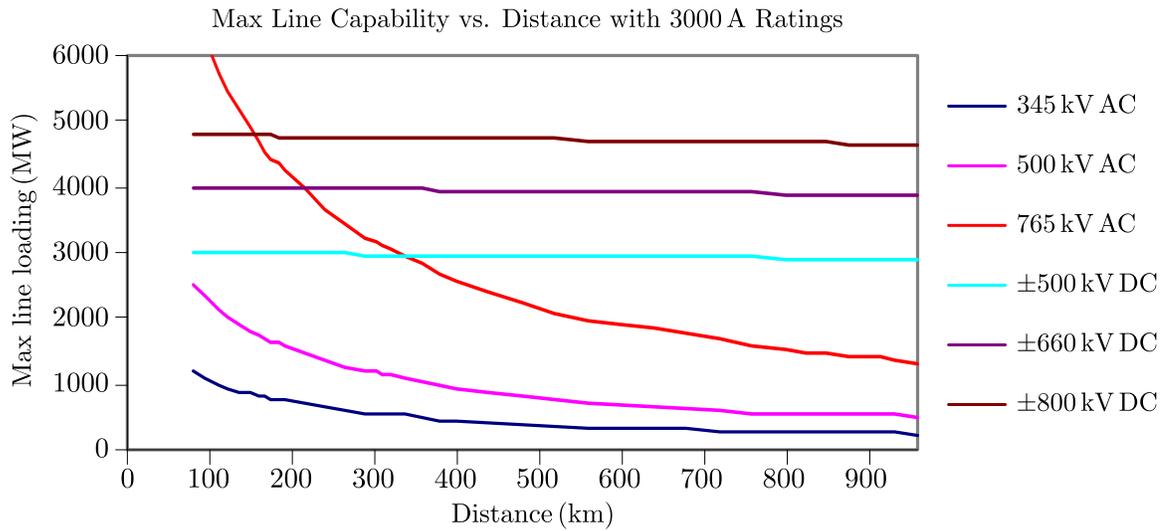
Figure 4.10. Transmission line capability versus distance.
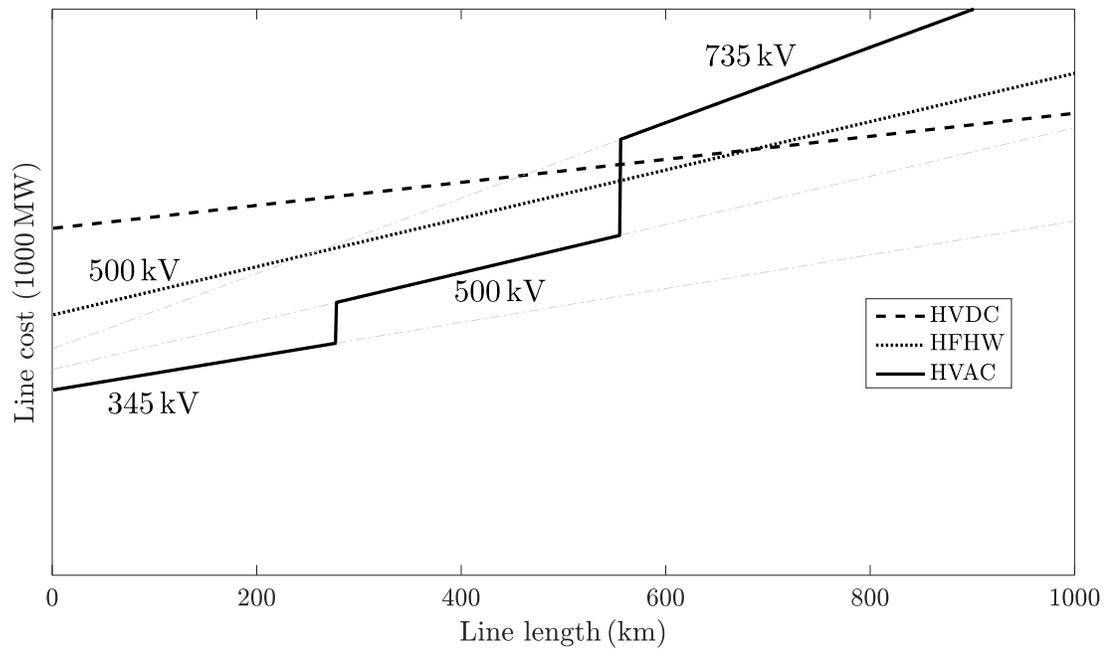
Figure 4.11. Transmission line capability versus distance.

conventional AC transmission system in distances longer than 550 km. This is very attractive as the cost breakthrough between HVAC and HVDC overhead lines occurs in longer distances.

Chapter 5

Series Hybrid Modular Multilevel Converter for HVDC System

5.1 Introduction

In Chapters 2 and 3, two power converters were introduced for AC/AC power systems. Afterwards, it was presented in Chapter 4 that the unidirectional version of SMMC could be employed in the HFHW transmission system. The HVDC line is another transmission system which could benefit from employing multilevel converters. The Parallel Hybrid MMC (PHMMC) is recently introduced for HVDC applications, but due to its circuit topology, inherits low-order harmonics on its DC-bus voltage and cannot fully regulate the DC voltage/power [47, 48]. In this chapter, a novel MMC for HVDC transmission system, called Series Hybrid Modular Multilevel Converter (SHMMC) is proposed. The SHMMC offers soft-switching operation for almost

66% of the power switches. In addition, it provides a DC-link voltage almost 3.33 times higher than AC-side rms voltage which makes it suitable for HVDC systems. The feasibility of the proposed converter, as well as the effectiveness of the control strategy are validated by simulation and experimental results.

5.2   Description of SHMMC

Figure 5.1 shows the schematic diagram of the proposed converter called SHMMC. It consists of two separate stages, a low frequency soft-switched unfolder on the AC-side and a Full-Bridge Arm (FBA) which includes a number of PWM-driven and hard-switched FBSMs for each phase of the converter. For simplicity, the voltage of FBSM-capacitors are assumed to be set at E and then, in the description of the

Figure 5.1. The schematic diagram of back-to-back SHMMC.

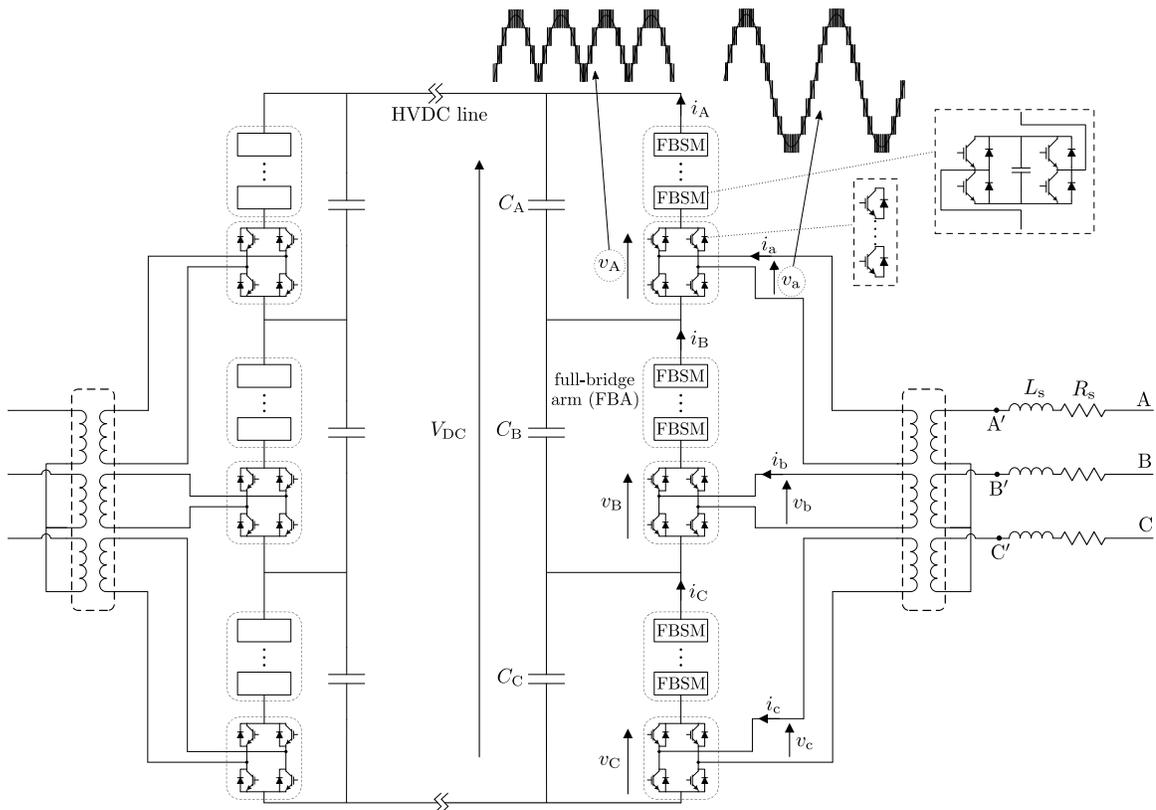control system, it will be shown how this is implemented. The voltage across the DC-link is set to $3(n-1)E/4$ which is equally distributed among the DC-link capacitors (i.e. C_A, C_B and C_C). n is the number of levels in the converter and can have the values of $4k + 1$, where k is the number of SMs in the FBA. By inserting the proper number of SMs in the FBAs, the absolute value of the phase voltages are synthesized across the unfolders (e.g. v_A for phase A). In an n-level converter, the number of FBSMs is equal to $(n-1)/4$; so that all desired non-negative values of $v_{A,B,C}$ can be generated $(v_{A,B,C} = mE, \ m = 0, 1, \cdots, (n-1)/2)$. The unfolders can further apply the absolute phase voltages or their reverse values to the AC-sides (e.g. v_a for phase A). In other words, the absolute value of phase voltages are synthesized by controlling the number of inserted FBSMs, while their polarities are controlled by the corresponding unfolders.

5.2.1 Zero-Crossing Circulating Current

Unlike MMC, there is no circulating current among different phases of the SHMMC as they are isolated from each other by a 3-phase transformer. However, it is inherently possible for current to circulate inside each phase of the converter. This current is not continuous and only may flow when phase voltages cross zero, and so it is called zero-crossing circulating current (i_{zcc}). For instance, the phase A of a 5-level converter is shown in Fig. 5.2, when $v_A = 0$ is required. In this switching state, if V_{CA} is slightly smaller than $V_{Ca1} + V_{Ca2}$, which can happen as a result of capacitor voltage variation, v_A becomes a small negative voltage. This negative voltage turns on the unfolder diodes, thus the current can circulate through the FBA. As studied in Section 2.2, adding one reversed IGBT in each arm of the unfolder could block the
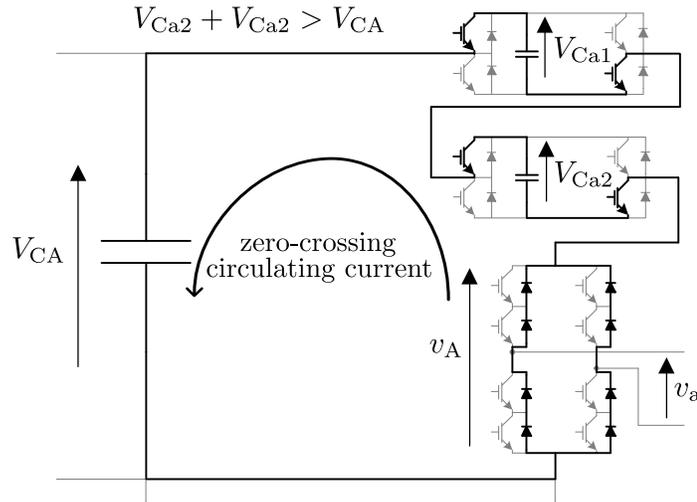
Figure 5.2. Zero-crossing circulating current in one phase of the converter.

possible i_{zcc}. Thus, at any stage of unfolding transition, there is at least one reversed IGBT blocking the zero-crossing circulating current (see Fig. 2.6).

5.2.2 Switching States of 5-level Single-phase SHMMC

The phase A of a 5-level SHMMC is shown in Fig. 5.3. The voltage of the DC-link and FBSM capacitors are both equal to E. The switching function $d_i(i = 1, 2)$ is defined so that $d_i = 1$, when upper switch of the SM leg is ON and the lower switch is OFF and $d_i = 0$, for the reverse case. In addition, $s_{\text{a}} = 1$ when $v_{\text{a}} \geqslant 0$ and $s_{\text{a}} = 0$ when $v_{\text{a}} < 0$. Therefore, v_{a} can take any of the values of 0, $\pm E$ or $\pm 2E$. Table 5.1 shows all the possible switching states in one phase of the converter. Similar tables could be developed for the other phases independent from each other.

5.2.3 Component Comparison with Alternative Converters

Table 5.2 presents the component count comparison of the proposed converter with MMC and Parallel Hybrid Modular Multilevel Converter (PHMMC) alternatives. It can be seen that both PHMMC and SHMMC have fewer components compared to
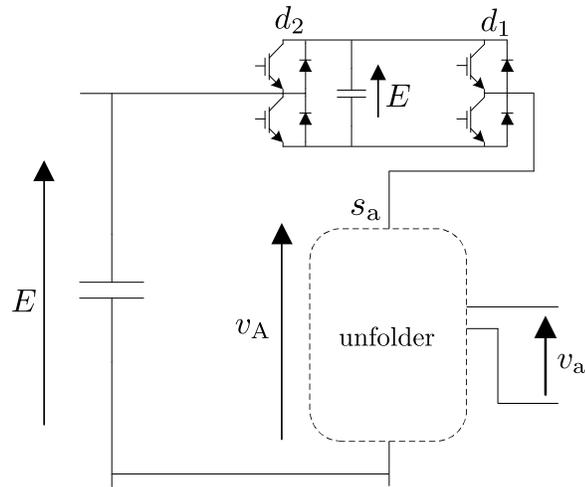
Figure 5.3. The schematic diagram of 5-level single-phase converter.

Table 5.1.
SWITCHING STATES OF A 5-LEVEL SHMMC

Switching state	d_1	d_2	s_a	v_A	v_a
1	0	1	0	0	0
2	0	0	1	E	$+E$
	1	1	1	E	$+E$
3	0	0	0	E	$-E$
	1	1	0	E	$-E$
4	1	0	1	$2E$	$+2E$
5	1	0	0	$2E$	$-2E$

Table 5.2.
COMPONENT COUNT COMPARISON (EQUAL DC-LINK VOLTAGE)

	MMC	PHMMC	SHMMC
Arm inductor	12	0	0
Capacitor	m	$0.26m$	$0.33m$
High-frequency & hard-switched IGBT	$2m$	$0.52m$	$0.67m$
Line-frequency & soft-switched IGBT	0	1.05m	$1.08m$
DC filter	×	✓	×
Voltage gain ($V_{\text{DC}}/V_{\text{AC\_rms}}$)	2.45	2.70	3.33

MMC. Although, SHMMC requires more capacitors and switches, but it provides a harmonic-free DC-link voltage which obviates the necessity of DC filter. Furthermore, SHMMC provides a DC-link voltage almost 3.33 times higher than AC-side phase-voltage. This is 23% higher than that of PHMMC and very attractive for HVDC applications.

5.2.4 Capacitor Voltage Balancing

The phase A voltage and current in Fig. 5.1 are represented as:

$$
\begin{cases}
v_{\mathrm{a}} = \sqrt{2}V\sin(\omega t) \ , \ v_{\mathrm{A}} = \lambda_{\mathrm{a}}.v_{\mathrm{a}} \ , \ \lambda_{\mathrm{a}} = \mathrm{sign}(v_{\mathrm{a}}) \\
i_{\mathrm{a}} = \sqrt{2}I\sin(\omega t - \varphi) \ , \ i_{\mathrm{A}} = \lambda_{\mathrm{a}}.i_{\mathrm{a}}.
\end{cases}
\tag{5.1}
$$

According to Fig. 5.1, the instantaneous power going through phase A's FBA, $p_{\mathrm{FA}}(t)$, is calculated as:

$$
p_{\mathrm{FA}}(t) = i_{\mathrm{A}} \times (v_{\mathrm{A}} - v_{\mathrm{CA}}),
\tag{5.2}
$$

where, v_{CA} is the voltage across the DC-link capacitor C_{A} and it is assumed to be equal to $V_{\mathrm{DC}}/3$. In the steady state condition, the stored energy of the FBA must be constant. This leads to the following equations to estimate the gain of the converter:

$$
\begin{aligned}
0 = \int_{T} p_{\mathrm{FA}}(t).dt &= \int_{T} i_{\mathrm{A}} \times (v_{\mathrm{A}} - \frac{V_{\mathrm{DC}}}{3}).dt \\
&= \int_{T}(i_{\mathrm{A}} \times v_{\mathrm{A}} - i_{\mathrm{A}} \times \frac{V_{\mathrm{DC}}}{3}).dt \\
&= VI\cos(\varphi) - \frac{2\sqrt{2}}{3\pi}V_{\mathrm{DC}}I\cos(\varphi) \\
&\Rightarrow \frac{V_{\mathrm{DC}}}{V} = 1.5\sqrt{2}\pi \approx 3.33.
\end{aligned}
\tag{5.3}
$$

Therefore, to achieve capacitor voltage balancing, the voltage gain of SHMMC must be constant and equal to 3.33. However, for any practical application, voltage gain control is required, especially, to adjust the reactive power exchange with the AC network. The AC-side voltage can be controlled by injecting harmonics, such that the ratio between the average rectified AC voltage and its fundamental component is regulated. Meanwhile, the unfolders are remained soft switched. The injected harmonics are required to be cancelled in line-to-line voltages and thus odd multiples of three harmonics $(3, 9, 15, 21, ..., \infty)$ are only accepted. In the simplest case, the voltage control is performed using only third harmonic addition. Based on this strategy, the AC-side voltages in a 3-phase converter shown in Fig. 5.1 can be represented as:

$$
\begin{cases}
v_{\mathrm{a}} = \sqrt{2}V \sin(\omega t) + \sqrt{2}V_3 \sin(3\omega t + \beta) \\[2mm]
v_{\mathrm{b}} = \sqrt{2}V \sin(\omega t - 2\pi/3) + \sqrt{2}V_3 \sin(3\omega t + \beta) \\[2mm]
v_{\mathrm{c}} = \sqrt{2}V \sin(\omega t - 4\pi/3) + \sqrt{2}V_3 \sin(3\omega t + \beta) \\[2mm]
v_{\mathrm{U}} = \lambda_{\mathrm{u}} v_{\mathrm{u}} \;\;, \;\; \lambda_{\mathrm{u}} = \mathrm{sign}(v_{\mathrm{u}}) \;\;, \;\; u = a, b, c.
\end{cases}
\tag{5.4}
$$

The neutral terminal of the transformer is not grounded, thus the added third harmonic voltage would not contribute to the power flow. Similar to the previous section, the capacitor voltage balancing criterion is studied as:

$$
0 = \int_T p_{\mathrm{FA}}(t).dt = VI\cos(\varphi) - \frac{\sqrt{2}V_{\mathrm{DC}}}{3} \int_T \lambda_{\mathrm{a}} I \sin(\omega t - \varphi)
\tag{5.5}
$$

$$
\Rightarrow \frac{V_{\mathrm{DC}}}{V} = \frac{3\cos(\varphi)}{\sqrt{2}\int_T \lambda_{\mathrm{a}} \sin(\omega t - \varphi)},
\tag{5.6}
$$

where, λ_a may be represented as:

$$
\begin{cases}
\lambda_a = \text{sign}(V \sin(\omega t) + V_3 \sin(3\omega t + \beta)) \\[2mm]
\quad\ = \text{sign}(\sin(\omega t) + \gamma \sin(3\omega t + \beta)) \\[2mm]
\gamma = \dfrac{V_3}{V} \quad , \quad -\pi \leq \beta \leq \pi.
\end{cases}
\tag{5.7}
$$

Adding third harmonic voltage appears as a phase-angle shift in λ_a, such that the zero-crossing point of the target AC voltage is shifted by δ without affecting the fundamental component (see Fig. 2.16 in Section 2.3.2). Different values of δ could be achieved by adjusting γ and β in Eq. (5.7) (see Fig. 2.17). Considering the impact of power factor in Eq. (5.6), the voltage gain of the converter is sketched versus β when $\gamma = 0.3$ and also versus power factor when when $\beta = 0.8\pi$ in Figs. 5.4 and 5.5, respectively.
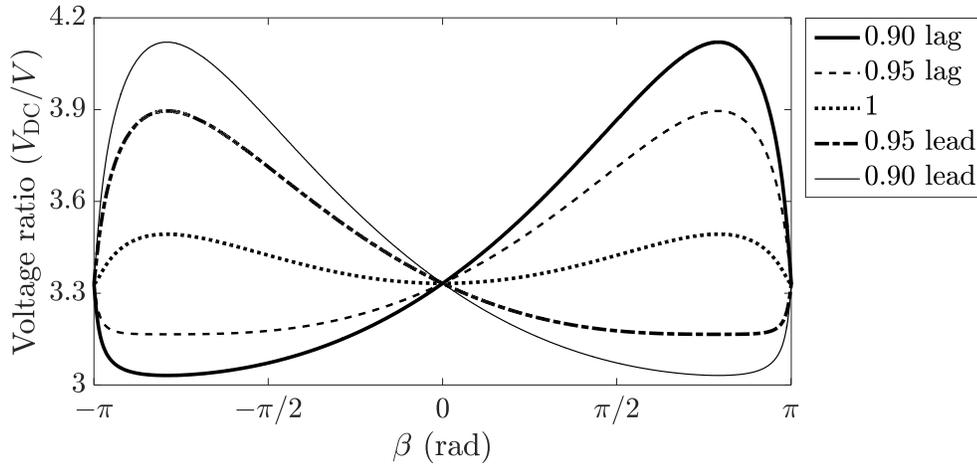

Figure 5.4. Voltage gain in terms of different β and power factor ($\gamma = 0.3$)
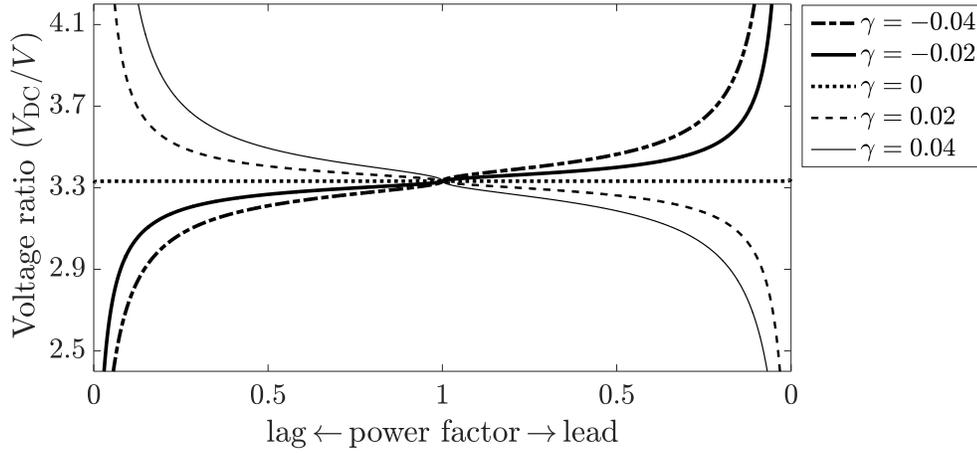
Figure 5.5. Voltage gain in terms of different γ and power factor $(\beta = 0.8\pi)$

5.3   Power Capability of the Proposed Converter

Figure 5.6 shows the simplified single-line diagram of the VSC-HVDC station connected to the AC grid.
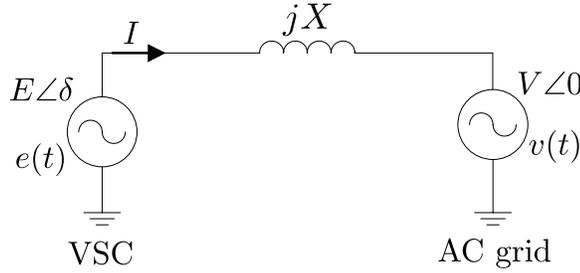
Figure 5.6. Simplified single-line diagram of converter-grid circuit.

The injected real and reactive powers to the grid are calculated as:

$$P = \frac{EV}{X}\sin\delta \quad , \quad Q = \frac{V^2 - EV\cos\delta}{X}, \tag{5.8}$$

where, $E\angle\delta$ and $V\angle 0$ are the voltage phasors of the converter and AC grid, respectively and X is the filter reactance. In rectifier mode, $e(t)$ is leading $v(t)$ and active power flows from AC- to DC-side while in inverter mode, $e(t)$ is lagging $v(t)$. Also,

Figure 5.7. *PQ* chart of the converter considering VSC limitation.

the converter can support the AC system with reactive power injection/consumption by regulating its voltage amplitude and phase angle (E, δ). The PQ chart of the proposed converter considering its limitation is sketched in Fig. 5.7.

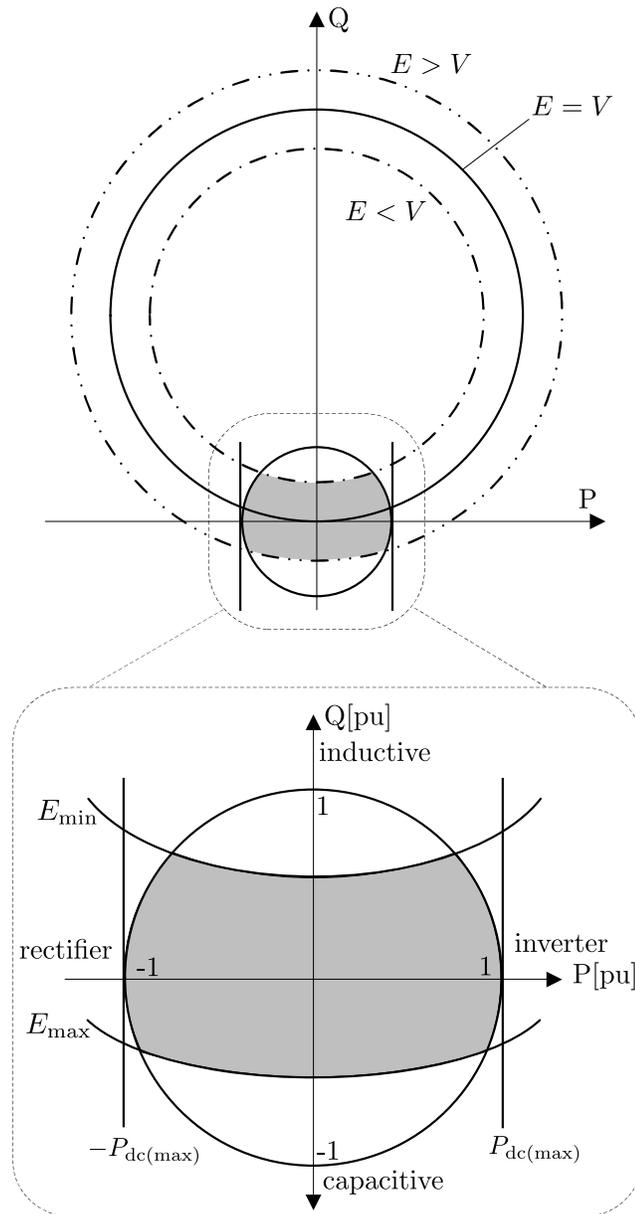The first one is maximum allowable IGBT's current which can be interpreted as

maximum MVA circle in the power plane with the radius of 1 pu. The minimum/maximum output voltage magnitude $(E_{\min}, E_{\max})$ determines the reactive-power capability of the converter as shown in Fig. 5.7 which depends on the DC-link voltage and modulation index limitation. In the proposed converter, the filter reactance is designed to be $X = 0.06$ pu. In this case, to assure the power capability of the converter is only limited by its maximum allowable IGBT's current, the output voltage magnitude must be adjustable as 0.94 pu $\leqslant E \leqslant 1.06$ pu as shown in Fig. 5.8 for inverter mode. From the previous section, it can be shown that this voltage range can be provided by the third harmonic injection in the range of $-0.12 \leqslant \gamma \leqslant 0.12$.
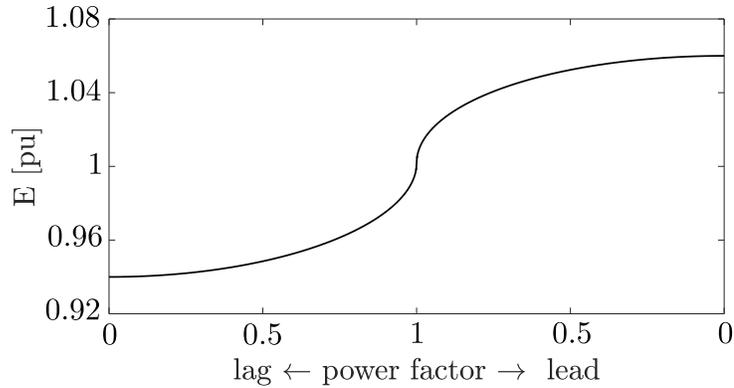
Figure 5.8. Required converter's voltage in different power factor (inverter mode).

5.4   Control Strategy

Figure 5.9 shows the schematic diagram of the control system which operates by controlling AC-side current in a *dq*-frame. This requires a synchronization mechanism that is achieved through a PLL. A reference generator is utilized to provide the reference currents $(i_{d,q})$ for the next control stage. Here, P_{ref} determines the amount and direction of transferred real power, whilst the reactive power, Q_{ref} is regulated to arbitrary value within the ratings of converter. A standard current controller in

dq-frame depicted in Fig. 5.9, which provides the expected active and reactive power exchange with the grid.

To ensure the power balance, a slow outer control loop is employed such that the total energy stored in the capacitors is effectively regulated at all time. As mentioned in the previous section, the power flow in the full-bridge arm could be controlled by injecting third harmonic voltage. Figure 5.9 illustrates the process of providing γ which is then used to generate the third harmonic component. n_{C} is the total number of capacitors in each arm which is equal to $(n-1)/4$ in an n-level converter. It is also necessary to evenly distribute the arm energy between the FBSM capacitors by selecting the proper SMs at each time. This is done according to the sorted queue of capacitor voltages and arm current direction [49].

5.5   Simulation Results

Simulation results have been obtained using MATLAB/Simulink for a 9-level 10 MVA SHMMC shown in Fig. 5.10. For simplicity, two FBSMs per phase have been used in the simulated model. However, higher number of FBSMs is suggested to be used in practice. In the nominal operating condition, the SM capacitors are set to voltage average of 2 kV. Table 5.3 lists the main parameters used for the simulation. A multi-carrier Sinusoidal Pulse-Width Modulation (SPWM) strategy obtained by the control diagram shown in Fig. 5.9 is used to regulate transferred active and reactive powers. The switching frequency of the SM-IGBTs is approximately 750 Hz, while the unfolder switches operate at AC line frequency (here 60 Hz). In practice, the number of levels is higher due to the higher grid voltage and power ratings and as a result, the switching frequency of SM-IGBTs reduces.
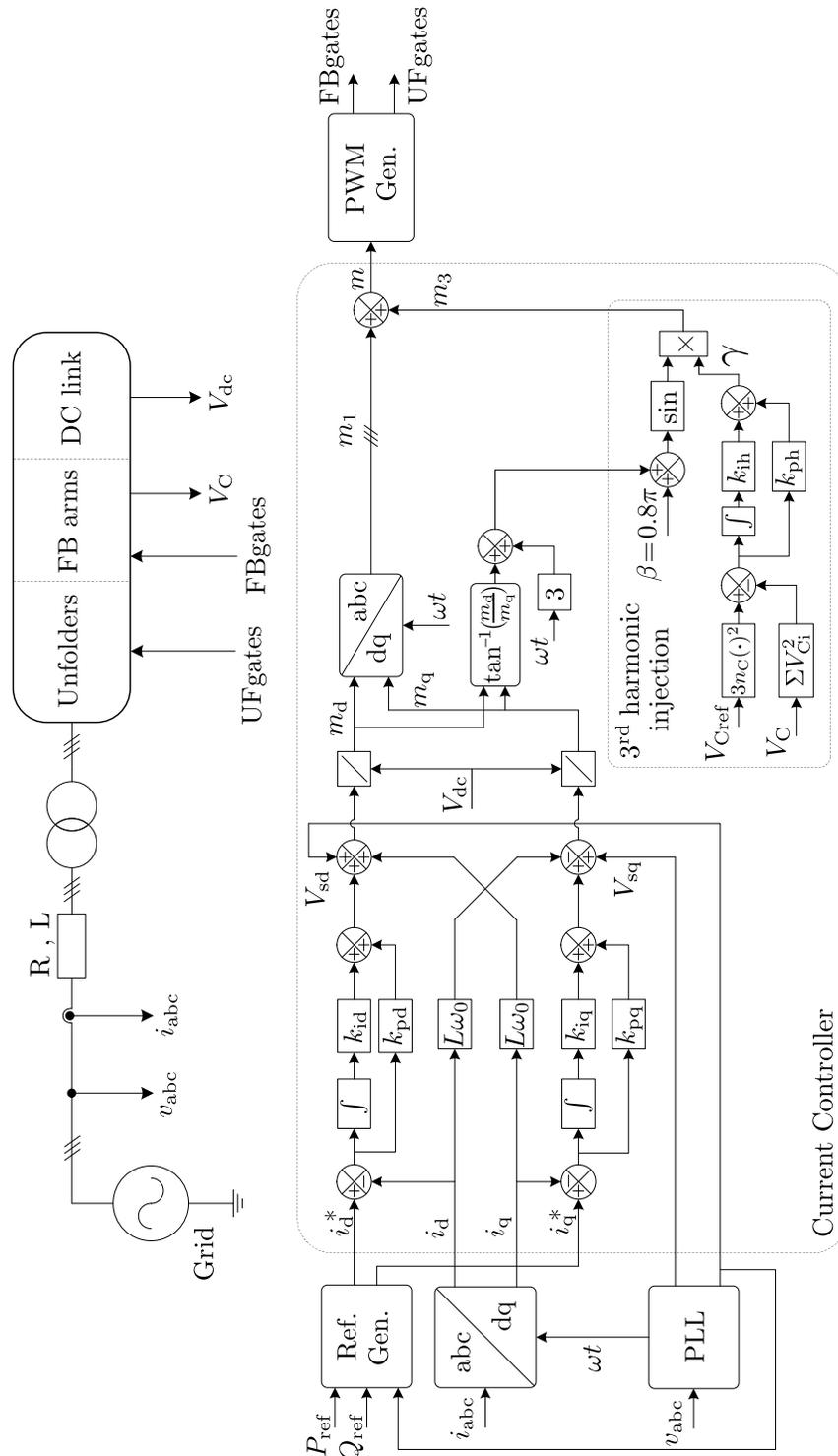
Figure 5.9. The schematic diagram of the control strategy.
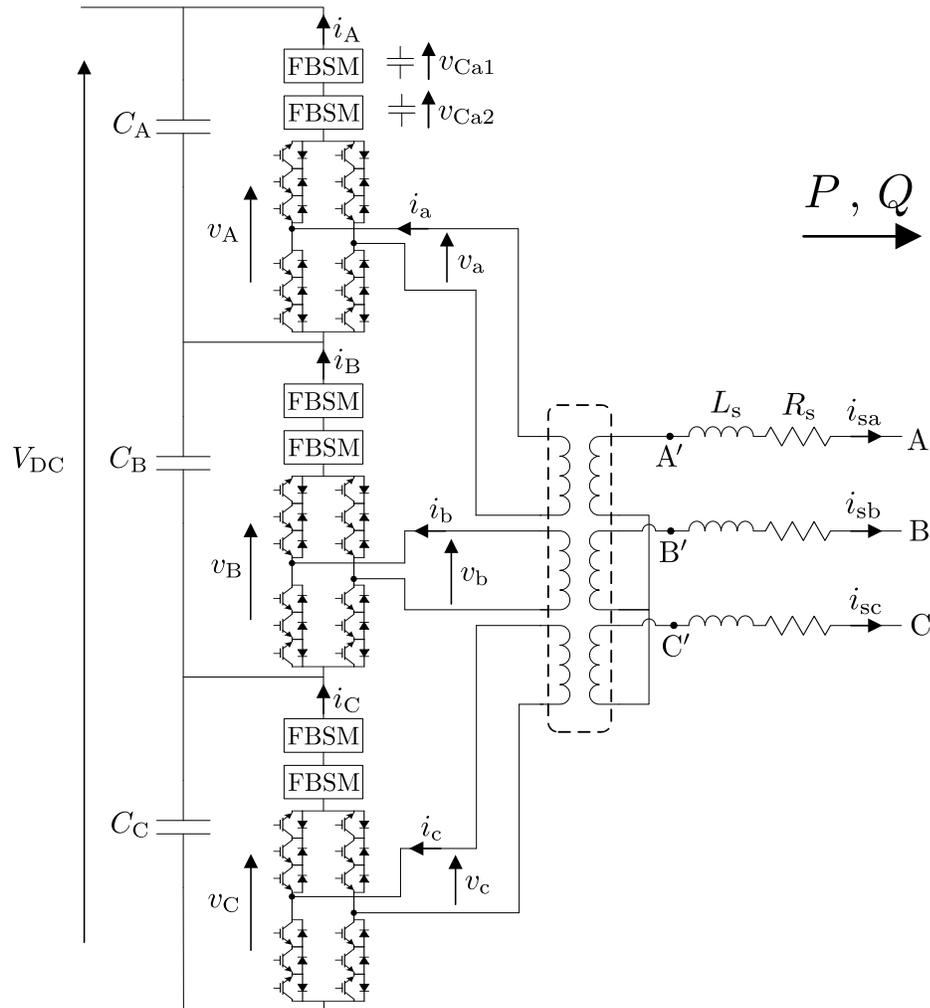
Figure 5.10. Schematic diagram of a 9-level SHMMC studied in MATLAB/Simulink.

5.5.1 Steady-State Simulation Results

Fig. 5.11 shows the steady-state simulation results for a case that $10\,\mathrm{MW}$ active power is transferred to the grid, while power factor is unity. The grid ($v_{\mathrm{A,B,C}}$), and the converter phase voltages ($v_{\mathrm{A',B',C'}}$), are presented in Figs. 5.11(a) and 5.11(b), respectively. It can be seen that the third harmonic component of the three phase voltages are cancelled out in the line-line voltages and the desired fundamental portion
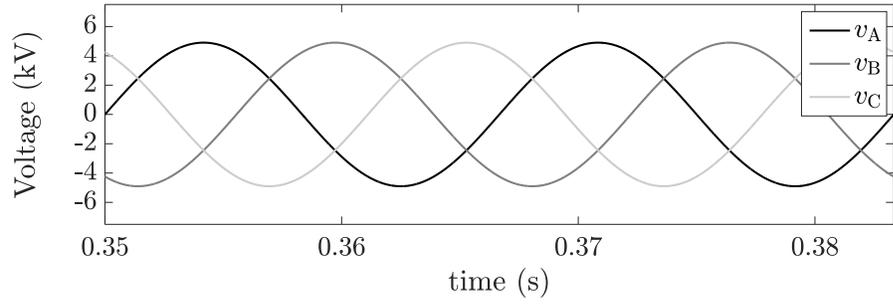
(a) Grid-side phase voltages
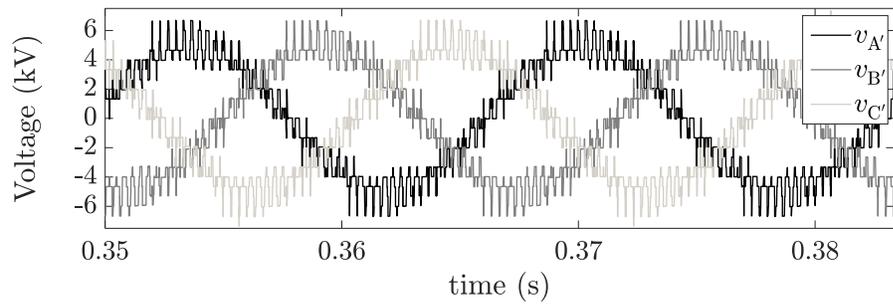
(b) Converter-side phase voltages
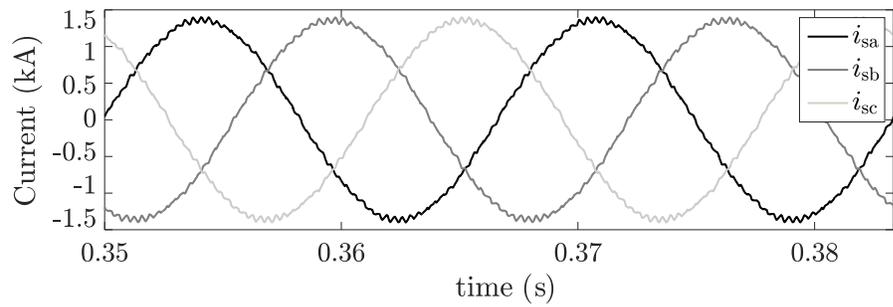
(c) Line currents
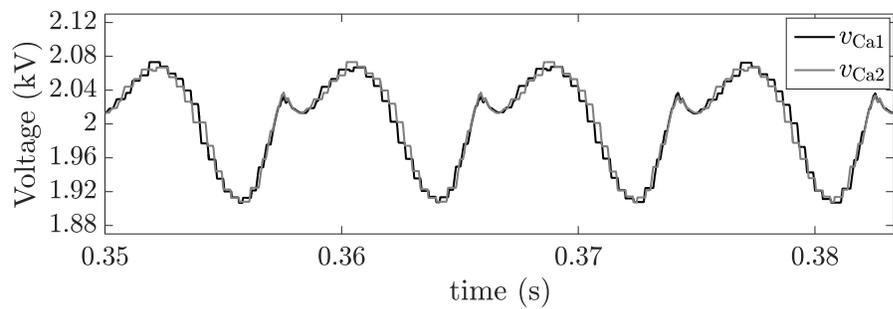
(d) SM-capacitor voltages (phase A)

Figure 5.11. Steady-state simulation results ($P = 10\,\text{MW}$, $Q = 0\,\text{MVAR}$).

Table 5.3.
SIMULATION PARAMETERS

Parameter		Rating
Power rating	$S_{\text{conv.}}$	10 MVA
Grid frequency	f	60 Hz
Grid voltage (line-line rms)	V_{s}	6.1 kV
DC-link voltage	V_{DC}	12 kV
SM capacitor	C_{SM}	4 mF
No. of SMs in FBA	n_{C}	2
Mean SM capacitor voltage	E	2 kV
Filter+Grid inductance	L_{s}	2 mH
Filter+Grid resistance	R_{s}	10 mΩ

is well synthesized. The injected line current shown in Fig. 5.11(c) is in phase with the grid voltage, showing that the power is positive and the converter operates as an inverter. The total harmonic distortion (THD) of the line current is 2.9%. In practice, by implementing higher number of SMs, the current waveform would be almost sinusoidal. The peak-to-peak ripple in phase A SM-capacitor voltages (see Fig. 5.11(d)) is approximately 9% which may vary due to the PQ operating point of the converter.

5.5.2 Transient Simulation Results

A number of active and reactive power changes (P_{ref} and Q_{ref} in Fig. 5.9), are applied to the converter. The transient response of the converter are presented for the line currents in the dq frame (i_{d}^*, i_{d}, i_{q}^* and i_{q}, in Fig. 5.9) and the total energy stored in the SM-capacitors. As shown in Fig. 5.12(a), the line currents track their references well, so the active and reactive powers are properly controlled. During each transient, a small error may occur in the total energy stored in the capacitors as shown in Fig. 5.12(b) which will be compensated in a few cycles. Thus, the implemented control

strategy is able to ensure that the converter's stored energy is properly regulated during transients.

5.6   Experimental Result

Although the simulation was performed on a 3-phase 10 MVA SHMMC, due to limited resources in our laboratory, the theoretical findings are demonstrated on a low-voltage single-phase converter shown in Fig. 5.13 with power rating of 0.5 kVA. The control system is implemented on a dSPACE-MicroLabBox unit. The DC-link is connected to a DC grid (100 V), while the AC-side feeds a resistive load operating in 90 Vrms & 60 Hz.   The parameters of the experimental setup can be found in Table 5.4. The switching frequency of SM-IGBTs is approximately 2.5 kHz, while the unfolder
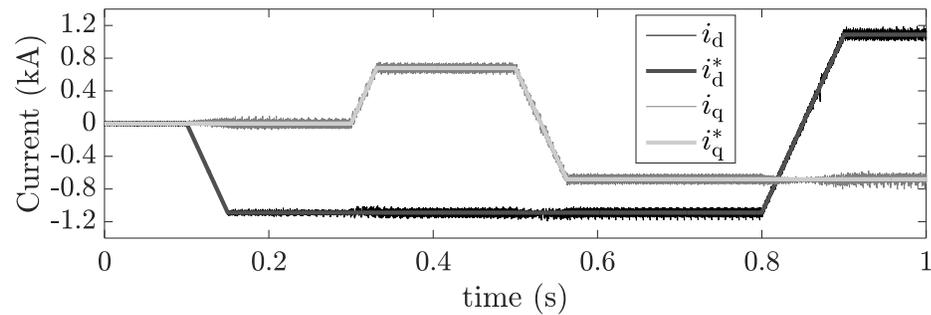
(a) *dq* frame line currents
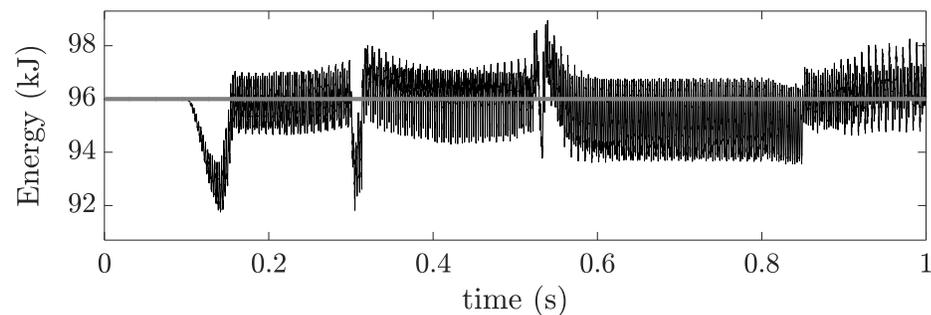
(b) Total energy stored in SM capacitors

Figure 5.12. Transient simulation results.
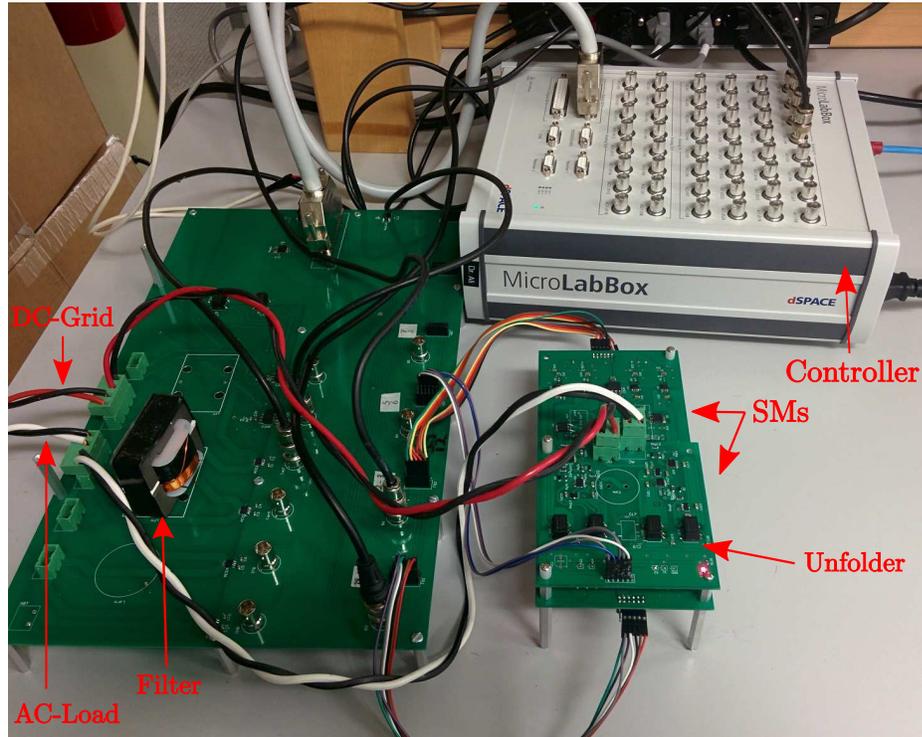
Figure 5.13. A view of the experimental setup.

switches are operating at AC line frequency (60 Hz). In practice, the number of levels

is higher which reduces the switching frequency.

Table 5.4.
EXPERIMENTAL PARAMETERS

Parameter		Rating
Power rating	$S_{\text{conv.}}$	0.5 kVA
AC-side frequency	f_{S}	60 Hz
SM capacitor	C_{SM}	820 μF
No. of SMs per arm	n_{C}	2
Filter inductance	L_{S}	5 mH

For a single-phase SHMMC without third-harmonic injection, the voltage gain is

constant and almost equals $V_{\text{DC}}/V_{\text{AC\_rms}} \approx 1.11$. The converter's AC-side waveforms

in the steady-state condition are shown in Figs. 5.14 and 5.15, respectively. It can be

seen that the inverter's output voltage is well synthesized with the expected amplitude
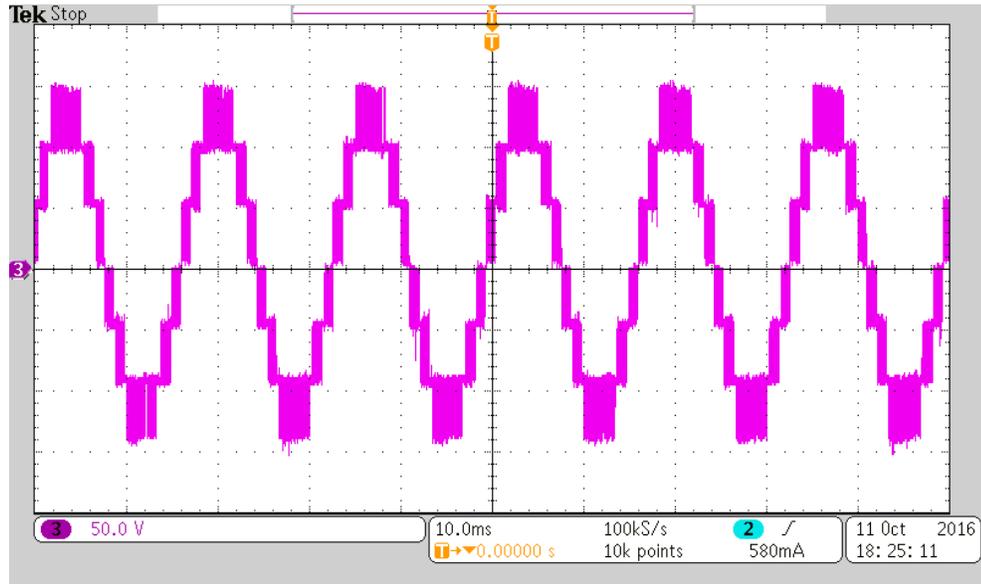
Figure 5.14. Converter's AC-side voltage in steady-state condition.
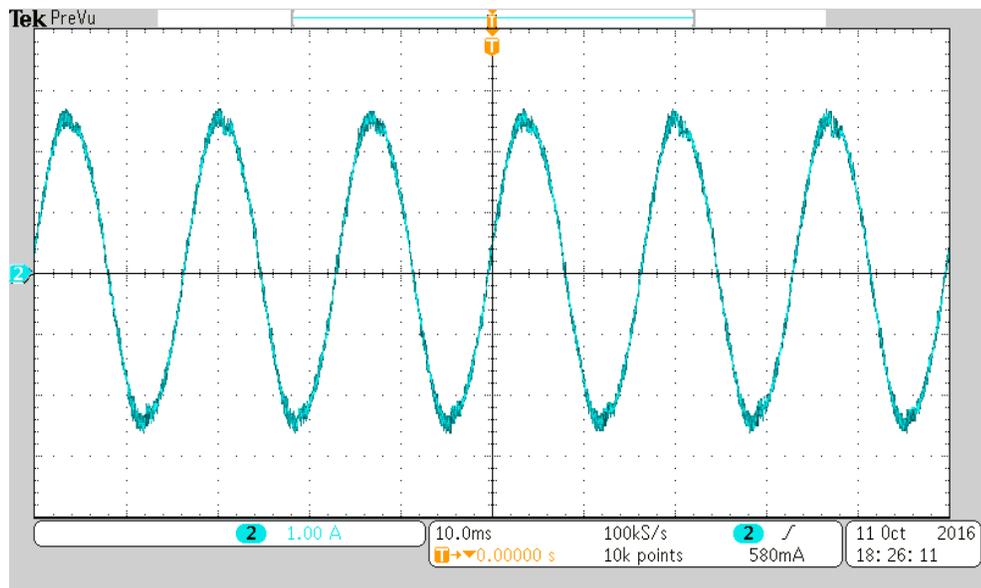
Figure 5.15. Converter's AC-side current in steady-state condition.

and frequency. In order to evaluate the dynamic response of the capacitor voltage balancing strategy, the load is suddenly increased while the SM capacitor voltages are monitored. As shown in Figs. 5.16 and 5.17, the proposed control strategy (see Fig. 5.9) is well capable of performing the capacitor voltage balancing.
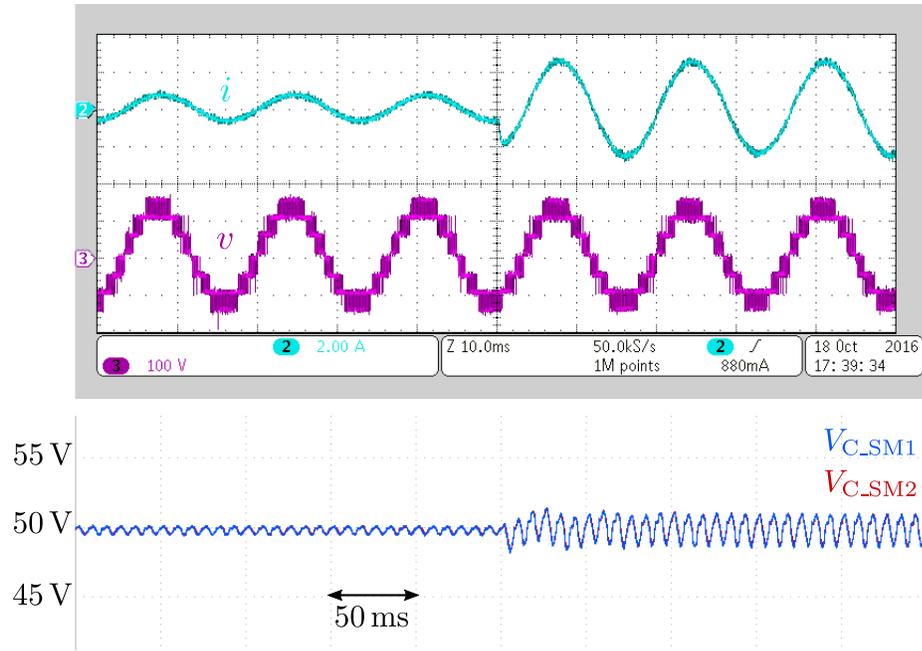
Figure 5.16. Dynamic response of the converter to the sudden load decrease.
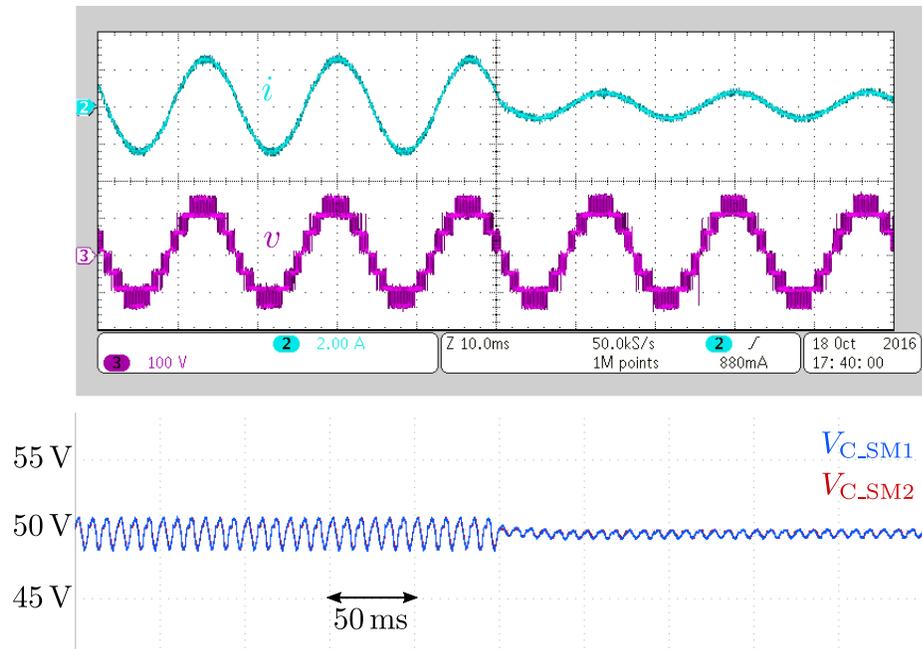
Figure 5.17. Dynamic response of the converter to the sudden load increase.

5.7   Summary

In this chapter, a novel multilevel converter called SHMMC intended for HVDC systems is proposed which has fewer components compared to conventional MMC and does not have the drawbacks of PHMMC. Also, the SHMMC provides a DC-link voltage more than three times higher than AC-side RMS voltage which makes it very desirable for HVDC applications. A control system is implemented to regulate the active power exchange and perform the capacitor voltage balancing of the converter. Both simulation and experimental results show that this topology can fulfill the requirements of a bidirectional converter intended for HVDC transmission systems.

Chapter 6

Summary and Future Works

6.1 Summary of Contributions

In this thesis, three novel multilevel converters for various type of power transmission systems are proposed. Analysis, design and experimental verification the proposed topologies have been presented. The objective of the proposed converters is to reduce the number of components in the converter and also to operate the majority of the power switches in soft-switching mode. The main contributions and conclusions of this thesis are summarized below.

(i) An AC/AC multilevel converter has been proposed for HFHW system which utilizes fewer power switches compared to conventional B2B-MMC and has switches operating in soft-switching mode;

(ii) An alternative multilevel converter for AC/AC applications in power systems has been proposed which further reduces the number of hard-switched power switches;

(iii) A high-gain multilevel inverter suitable for HVDC systems has been proposed which requires fewer power switches compared to MMC and similar to other proposed converters, the majority of its switches operate in soft-switching mode;

(iv) Separate control strategies have been implemented for the proposed topologies which regulate the AC-sides active and reactive powers and also guarantee the capacitor voltage balancing in both steady-state and transient conditions;

(v) The economical aspect of the HFHW transmission system has been studied. The use of unidirectional SMMC in the HFHW system has been compared with its alternative.

(vi) All the proposed topologies with their associated control strategies have been verified with both simulation and experimental results.

6.2   Suggested Future Work

There are a number of directions that this research could be continued; two of the most promising are outlined below.

(i) All three proposed multilevel converters are constructed by using line-frequency and soft-switched unfolders. To simplify the switch count comparison with the alternative topologies, it was assumed that the same type of IGBTs are used in the unfolders. However, the possibility of using other type of switches or IGBTs with different rating must be investigated, as the unfolder valves experience less switching stress compared to SM-IGBTs.

(ii) Different power transmission system can also benefit from employing the proposed converters. For example, an alternative transmission line design approach

shown in Fig. 6.1 is suggested to be further investigated. In this approach, third harmonic voltage is injected to the line through neutral terminal of the sending-end transformer such that the peak amplitude of phase voltages is reduced by 13.4% while the fundamental component remains intact and thus it is called Third Harmonic Injected Line (THIL) (see Fig. 6.2).
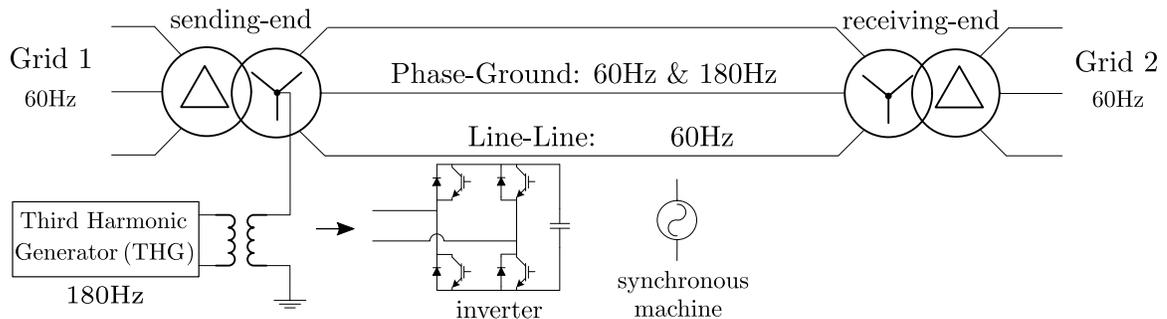
Figure 6.1. The schematic diagram of third harmonic injected line (THIL).
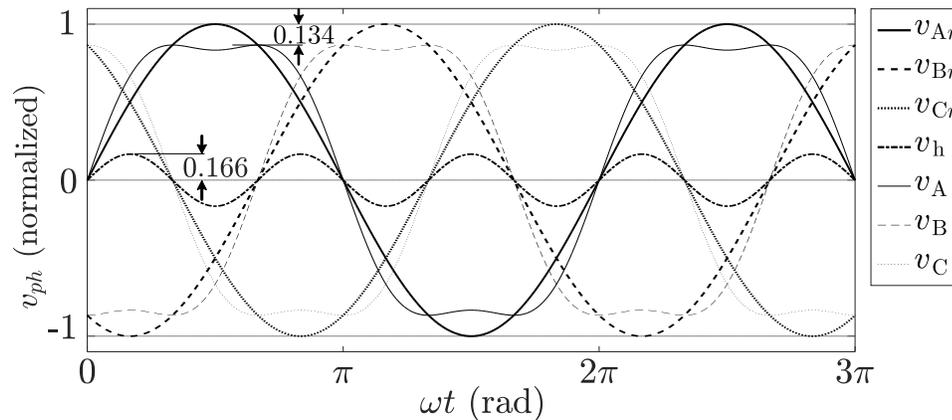
Figure 6.2. Decreasing voltage peak amplitude by third harmonic injection.

The third harmonic voltage is injected to the line by a single-phase Third Harmonic Generator (THG) and does not influence the load or generation sides. The neutral terminal of the receiving transformer is not grounded, thus the

R. Alaei and S. A. Khajehoddin, "Third harmonic injected transmission line," in *IEEE Transactions on Power Delivery*, (Early Access).

(a) neutral-fed

(b) line-fed
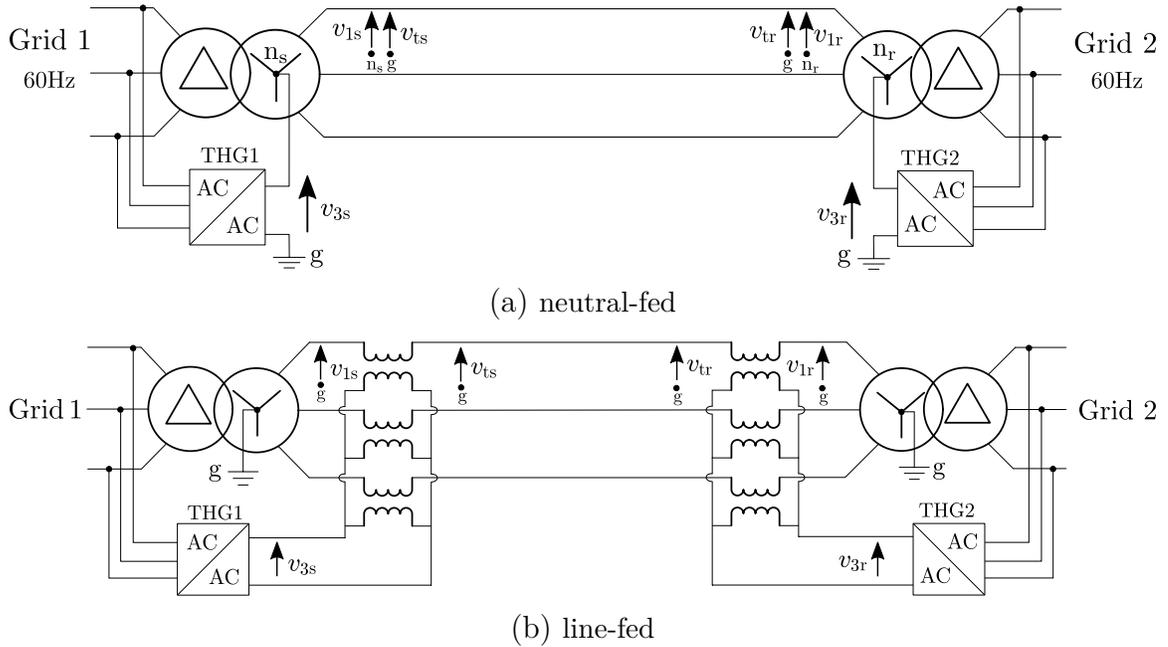
Figure 6.3. Schematic diagram of the modified THIL.

added third harmonic voltage does not create current and would not contribute to the power flow. The added harmonic voltage is cancelled out in line-to-line voltages. The objective is to utilize the insulating strength of the conductor-to-ground clearance almost continuously rather than only during the crest voltage, as opposed to conventional AC lines. With this approach, for the same fundamental voltage level, THIL requires lower conductor-to-ground clearance. This could considerably reduce the line construction capital investment by using shorter transmission towers. Furthermore, the existing AC lines could be upgraded to THIL system to increase their ground clearance, if desired. THIL system can also increase the loadability of existing AC lines, if the new phase-to-phase clearance is met.

In THIL, two voltages in 60 Hz and 180 Hz are combined at the sending-end with an adjusted phase difference between them. As a result of signal dispersion and

load angle, for longer AC lines, the arrival time difference between the two voltage components, is considerable and the variation of phase voltage peak amplitude may not be acceptable. To tackle this issue, two alternatives of THIL are proposed where third harmonic voltage is injected at both ends of the line according to each end phase voltages as shown in Fig. 6.3. Therefore, the least peak amplitude of the phase voltages are ensured along the line.

The THG could be implemented by a multilevel inverter which must be investigated.

Bibliography

[1] Y. Wang, W. Xu, Y. W. Li, and T. Hao, "High-frequency, half-wavelength power transmission scheme," *IEEE Transactions on Power Delivery (Early Access).*

[2] J. Peralta, H. Saad, S. Dennetière, J. Mahseredjian, and S. Nguefeu, "Detailed and averaged models for a 401-level MMC-HVDC system," *IEEE Transactions on Power Delivery*, vol. 27, no. 3, pp. 1501–1508, Jul. 2012.

[3] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 37–53, Jan. 2015.

[4] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 18–36, Jan. 2015.

[5] F. Hubert and M. Gent, "Half-wavelength power transmission lines," *IEEE Transactions on Power Apparatus and Systems*, vol. 10, no. 84, pp. 965–974, Oct. 1965.

[6] M. Santos, J. Jardini, M. Masuda, and G. L. C. Nicola, "A study and design of half-wavelength lines as an option for long distance power transmission," in *Proc. IEEE PowerTech Conference*, Trondheim, Norway, Jun. 2011, pp. 1–6.

[7] L. C. Ferreira Gomes, L. C. da Silva, and M. C. Tavares, "Half-wavelength transmission lines for connecting power plants in Amazon region to the Brazilian system," in *Proc. IEEE PowerTech Conference*, Grenoble, France, Jun. 2013, pp. 1–6.

[8] M. Aredes and R. Dias, "FACTS for tapping and power flow control in half-wavelength transmission lines," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 10, pp. 3669–3679, Oct. 2012.

[9] Y. Song, B. Fan, Y. Bai, X. Qin, and Z. Zhang, "Reliability and economic analysis of UHV half-wavelength AC transmission," in *Proc. IEEE International Conference Power System Technology (POWERCON)*, Auckland, New Zealand, Nov. 2012, pp. 1–6.

[10] M. Tavares and R. Torquato, "Attending small loads along a half-wavelength transmission line," in *Proc. IEEE Electrical Power and Energy Conference (EPEC)*, Winnipeg, Canada, Oct. 2011, pp. 255–259.

[11] B. Wu, *High-Power Converters and AC Drives*.   Hoboken, USA: John Wiley & Sons, 2006.

[12] G.-T. Kim and T. Lipo, "VSI-PWM rectifier/inverter system with a reduced switch count," *IEEE Transactions on Industry Applications*, vol. 32, no. 6, pp. 1331–1337, Nov./Dec. 1996.

[13] C. B. Jacobina, I. Soares de Freitas, and A. M. N. Lima, "DC-link three-phase-to-three-phase four-leg converters," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 4, pp. 1953–1961, Aug. 2007.

[14] C. Liu, B. Wu, N. R. Zargari, D. Xu, and J. Wang, "A novel three-phase three-leg AC/AC converter using nine IGBTs," *IEEE Transactions on Power Electronics*, vol. 24, no. 5, pp. 1151–1160, May 2009.

[15] J. W. Kolar, M. Baumann, F. Schafmeister, and H. Ertl, "Novel three-phase AC-DC-AC sparse matrix converter," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Dallas, USA, Mar. 2002, pp. 777–791.

[16] J. W. Kolar, F. Schafmeister, S. D. Round, and H. Ertl, "Novel three-phase AC–AC sparse matrix converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 1649–1661, Sep. 2007.

[17] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Transactions on Industry Applications*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[18] M. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, R. Critchley, W. Crookes, and F. Hassan, "The alternate arm converter: A new hybrid multi-level converter with dc-fault blocking capability," *IEEE Transactions on Power Delivery*, vol. 29, no. 1, pp. 310–317, Feb. 2014.

[19] L. Xu and V. G. Agelidis, "VSC transmission system using flying capacitor multilevel converters and hybrid PWM control," *IEEE Transactions on Power Delivery*, vol. 22, no. 1, pp. 693–702, Jan. 2007.

[20] L. Tarisciotti, P. Zanchetta, A. Watson, S. Bifaretti, and J. C. Clare, "Modulated model predictive control for a seven-level cascaded H-bridge back-to-back converter," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 10, pp. 5375–5383, Oct. 2014.

[21] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[22] S. A. Khajehoddin, A. Bakhshai, and P. K. Jain, "A voltage balancing method and its stability boundary for five-level diode-clamped multilevel converters," in *Proc. IEEE Power Electronics Specialists Conference (PESC)*, Orlando, USA, Jun. 2007, pp. 2204–2208.

[23] ——, "A simple voltage balancing scheme for m-level diode-clamped multilevel converters based on a generalized current flow model," *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2248–2259, Sep. 2008.

[24] M. Marchesoni and P. Tenca, "Diode-clamped multilevel converters: A practicable way to balance DC-link voltages," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 752–765, Aug. 2002.

[25] F. Z. Peng, J.-S. Lai, J. W. McKeever, and J. VanCoevering, "A multilevel voltage-source inverter with separate DC sources for static var generation," *IEEE*

Transactions on Industry Applications, vol. 32, no. 5, pp. 1130–1138, Sep./Oct. 1996.

[26] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE PowerTech Conference*, Bologna, Italy, Jun. 2003, pp. 272–277.

[27] J. Dorn, H. Gambach, J. Strauss, T. Westerweller, and J. Alligan, "Trans bay cable-A breakthrough of VSC multilevel converters in HVDC transmission," in *Proc. Cigré Colloquium on HVDC and Power Electronics Systems*, San Francisco, USA, Mar. 2012, pp. 1–6.

[28] M. Sztykiel, R. Da Silva, R. Teodorescu, L. Zeni, L. Helle, and P. C. Kjaer, "Modular multilevel converter modelling, control and analysis under grid frequency deviations," in *Proc. European Conference on Power Electronics and Applications (EPE)*, Lille, France, Sep. 2013, pp. 1–11.

[29] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proceedings of the IEEE*, vol. 97, no. 11, pp. 1786–1817, 2009.

[30] M. Pérez, J. Rodriguez, J. Pontt, and S. Kouro, "Power distribution in hybrid multi-cell converter with nearest level modulation," in *Proc. IEEE International Symposium on Industrial Electronics (ISIE)*, Vigo, Spain, Jun. 2007, pp. 736–741.

[31] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 662–669, Jun. 2005.

[32] X. Wang and X. Wang, "Feasibility study of fractional frequency transmission system," *IEEE Transactions on Power Systems*, vol. 11, no. 2, pp. 962–967, May 1996.

[33] W. Xifan, C. Chengjun, and Z. Zhichao, "Experiment on fractional frequency transmission system," *IEEE Transactions on Power Systems*, vol. 21, no. 1, pp. 372–377, Feb. 2006.

[34] A. Rufer, N. Schibli, C. Chabert, and C. Zimmermann, "Configurable front-end converters for multicurrent locomotives operated on 16 2/3 Hz AC and 3 kV DC systems," *IEEE Transactions on Power Electronics*, vol. 18, no. 5, pp. 1186–1193, Sep. 2003.

[35] P. Drabek, M. Pittermann, and M. Cedl, "Novel primary high voltage traction converter topology for multi-system locomotives," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, San Jose, USA, Sep. 2009, pp. 422–429.

[36] A. Gomez-Exposito, J. M. Mauricio, and J. M. Maza-Ortega, "VSC-based MVDC railway electrification system," *IEEE Transactions onPower Delivery*, vol. 29, no. 1, pp. 422–431, Feb. 2014.

[37] J. Hao and W. Xu, "Extended transmission line loadability curve by including voltage stability constrains," in *Proc. IEEE Electrical Power & Energy Conference (EPEC)*, Vancouver, Canada, Oct. 2008, pp. 1–5.

[38] H. P. S. Clair, "Practical concepts in capability and performance of transmission lines," *AIEE Transactions*, vol. 72, no. 2, pp. 1152–1157, Jan. 1953.

[39] P. Kundur, N. J. Balu, and M. G. Lauby, *Power system stability and control*. New York, USA: McGraw-Hill, 1994.

[40] H. P. Bloch and M. Singh, *Steam Turbines: Design, Application, and Re-Rating*, 2nd ed.   McGraw Hill Professional, 2008.

[41] J. C. Olivares-Galvan, "Transformer design for high frequency half-wavelngth transmission line," University of Alberta, Edmonton, Canada, Tech. Rep., Jun. 2014.

[42] CIGRE Working Group 14.20, "Economic assessment of HVDC links (Technical Brochure 388)," Tech. Rep., Jun. 2001.

[43] R. Kehlhofer, F. Hannemann, B. Rukes, and F. Stirnimann, *Combined-cycle gas & steam turbine power plants*.   Tulsa, USA: PennWell Corporation, 2009.

[44] B. Stoeber and J. Schumacher, "Gear efficiency – key to lower drive cost," *Available: http://machinedesign.com/mechanical-drives/gear-efficiency-key-lower-drive-cost. [Accessed: June 4, 2016]*, 2000.

[45] M. Lima dos Santos, J. A. Jardini, R. P. Casolari, R. L. Vasquez-Arnez, G. Y. Saiki, T. Sousa, C. Nicola, and G. Luiz, "Power transmission over long distances: economic comparison between HVDC and half-wavelength line," *IEEE Transactions on Power Delivery*, vol. 29, no. 2, pp. 502–509, Apr. 2014.

[46] M. Bahrman, "HVDC transmission: An economical complement to AC transmission," in *WECC Transmission Planning Seminar*, Feb. 2009.

[47] R. Feldman, M. Tomasini, E. Amankwah, J. C. Clare, P. W. Wheeler, D. R. Trainer, and R. S. Whitehouse, "A hybrid modular multilevel voltage source converter for HVDC power transmission," *IEEE Transactions on Industry Applications*, vol. 49, no. 4, pp. 1577–1588, Jul./Aug. 2013.

[48] J. Qin and M. Saeedifard, "A zero-sequence voltage injection-based control strategy for a parallel hybrid modular multilevel HVDC converter system," *IEEE Transactions on Power Delivery*, vol. 30, no. 2, pp. 728–736, Apr. 2015.

[49] P. M. Meshram and V. B. Borghate, "A simplified nearest level control (NLC) voltage balancing method for modular multilevel converter (MMC)," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 450–462, Jan. 2015.

[50] B. W. Williams, *Power Electronics: Devices, Drivers, Applications, and Passive Components.* Glasgow, UK: University of Strathclyde.

Appendix A

Voltage Sharing in Series-connected Semiconductors

A.1 Introduction

Due to the limited power rating of semiconductors, using a single device is insufficient in high power applications. Therefore, to increase the power capability, a number of semiconductors are paralleled to increase the current capability or series-connected to increase the voltage ratings. Using series connection of thyristors or IGBTs as a valve is common in HVDC applications. When power semiconductors are connected in series for high-voltage operation, both steady-state and transient voltages must be shared equally by each individual series device. Similarly, if they are connected in parallel to obtain higher current capability, the current sharing during both transient and steady states must be guaranteed.

A.2 Steady State Voltage Sharing

Figure A.1 shows the forward off-state I-V characteristics of two power switching devices. They both conduct the same leakage current but, they have different voltage

drops across them. If the peak-rated voltage of each device is V_{m}, it is hoped that the maximum permissible value of V can approach $2V_{\mathrm{m}}$. However, since the two devices are in series they must share the same leakage current I_{leakage}, so that if they had blocking characteristics as in Fig. A.1, device D_2 will be operating very close to its rated voltage, while device D_1 only blocks a fraction of this voltage. Therefore, the total blocked voltage $(V_1 + V_2)$ can be significantly less than the sum of the individual voltage capabilities [50].
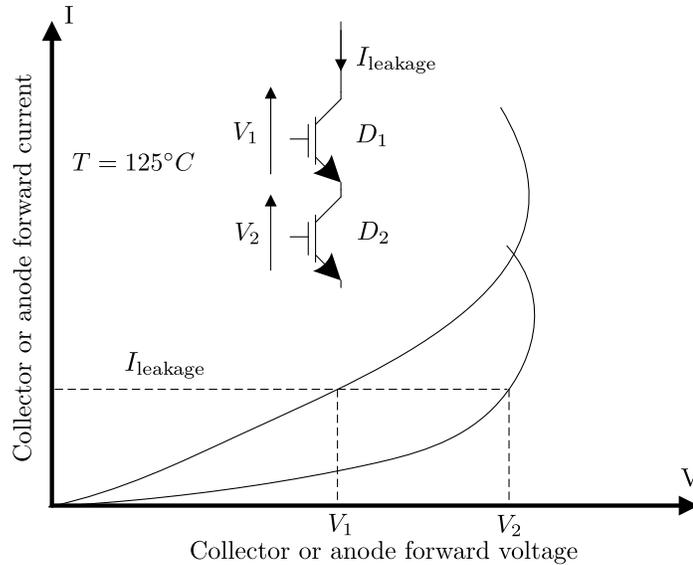

Figure A.1. Collector forward blocking I-V characteristics of two series devices.

Steady-state voltage sharing can be simply forced by connecting a large resistor in parallel with each series device as shown in Fig. A.2.

R denotes the maximum value of this resistance. The current through these resistors must be large enough to compensate the inequality in the thyristor leakage currents. The worst case of unequal sharing occurs when one device, say D_1, has negligible leakage current, I_{bmin}, whereas the remaining have maximum leakage current, I_{bmax}. If the range of maximum rated leakage or blocking currents is from I_{bmax} to I_{bmin}, then the maximum imbalance occurs when D_1 has a leakage current of I_{bmin},
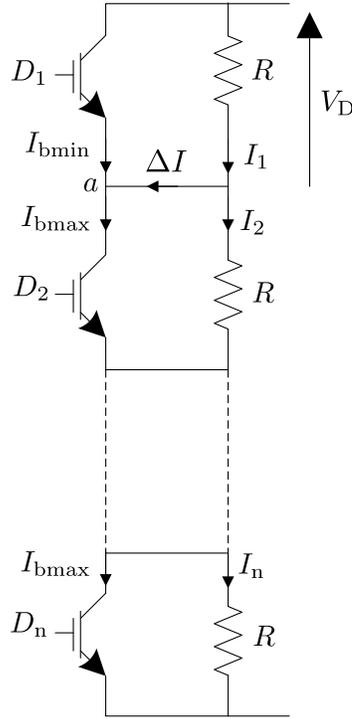
Figure A.2. Shunt resistors for voltage equalization in off-state.

while all the remainder conduct I_{bmax}. From Fig. A.2, Kirchhoff's current law at node a, gives:

$$I_{\mathrm{bmin}} \approx 0 \Rightarrow \Delta I = I_1 - I_2 \approx I_{\mathrm{bmax}}, \tag{A.1}$$

where, $I_1 > I_2$. The voltage across cell D_1 equals to $V_{\mathrm{D}} = I_1 R$. By symmetry and Kirchhoff's voltage law, the total string voltage V_{s}, is given by:

$$V_{\mathrm{s}} = (n-1)I_2 R + V_{\mathrm{D}}. \tag{A.2}$$

Eliminating ΔI, I_1, and I_2 from Eqs. (A.1) and (A.2) yields:

$$R \leq \frac{nV_{\mathrm{D}} - V_{\mathrm{s}}}{(n-1)I_{\mathrm{bmax}}} \quad , \quad n \geq 2. \tag{A.3}$$

Using the value of the resistor not larger that given by above equation, the voltage will be effectively shared among the series semiconductors, in their steady-state.

A.3 Transient Voltage Sharing

Although steady-state voltage sharing can be ensured by parallel resistors, when the devices are turned on or off, sharing resistors cannot guarantee the equal voltages across them during transients. For instance, the IGBTs which recover their blocking state fastest, or turn on last, will experience the full voltage of the series string which can destroy them. Figure A.3 shows the I-V characteristics of two unmatched thyristors or diodes during reverse recovery [50].
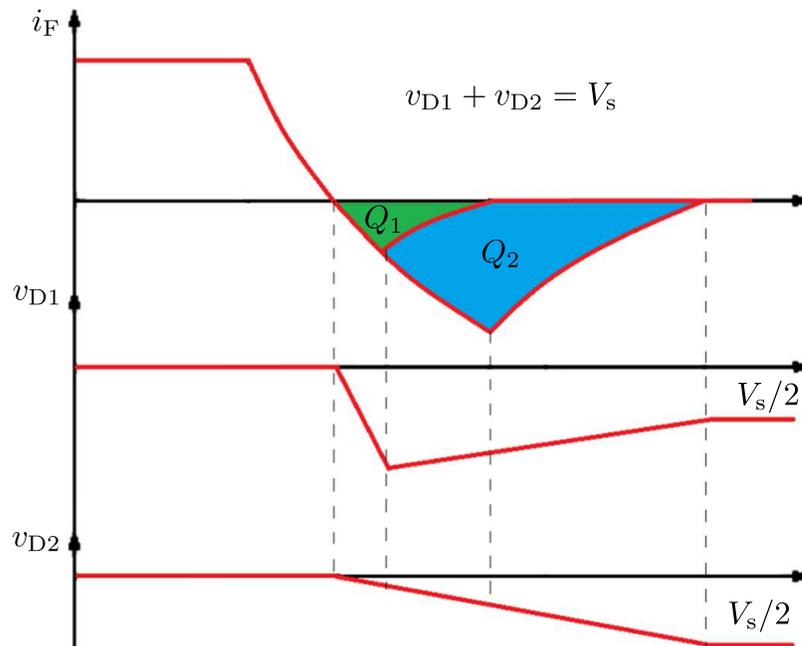

Figure A.3. Reverse recovery current and voltage for two mismatched series devices.

Since, this transient voltage distribution is inversely proportional to the device capacitance, using a capacitor of a value greater than the device capacitance across each device can solve the problem, as in Fig. A.4. In other words, the capacitor action

is to provide a transient current path bypassing a recovered device to allow a slower device to recover and to support volts. A low value resistance is connected in series with each capacitor to avoid high capacitor discharge through the device at turn-on.
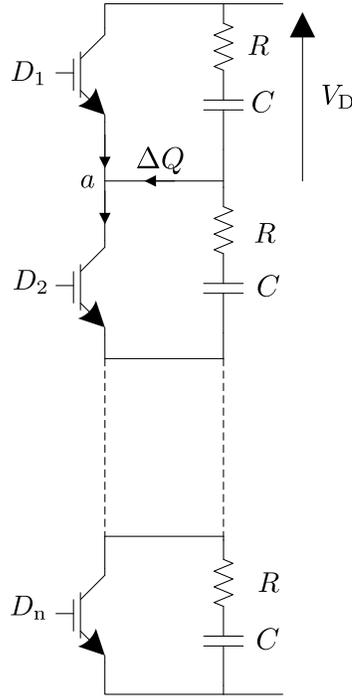

Figure A.4. Shunt capacitors for transient reverse blocking voltage.

In order to analyze the worst condition, it is assumed that D_1 has a minimum stored charge Q_{min}, which is negligible, while other devices have the maximum stored charge of Q_{max}. Therefore,

$$\Delta Q = Q_{max} - Q_{min} \approx Q_{max}. \tag{A.4}$$

The total branch voltage V_s, is the summation of the voltage across the fast-recovery device (V_D) and all of the $n-1$ slow devices voltages (V_b):

$$V_s = V_D + (n-1)V_b, \tag{A.5}$$

$$V_b = \frac{1}{n}(V_b - \Delta V) \quad \text{where} \quad \Delta V = V_D - V_b = \frac{\Delta Q}{C_{\min}}. \tag{A.6}$$

Substituting Eq. (A.6) in Eq. (A.5) leads to:

$$C \geq C_{\min} = \frac{(n-1)\Delta Q}{nV_D - V_s}. \tag{A.7}$$

Therefore, by installing a capacitor larger than $C_{\min}$ in parallel which each semiconductor, the transient voltage sharing would be insured.