Molding Flow Modeling and Experimental Study on Void Control for Flip Chip Package Panel Molding with Molded Underfill Technology

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Abstract

Increasing challenges are faced to ensure moldability with rapid advances in flip chip technology such as decreasing bump pitch and stand-off height, especially when commercial Moldable Underfill (MUF) is used and in particular, during panel level molding. One key challenge faced is severe void entrapment under the die. Experiments involving a large DOE matrix, which require significant time and process resources, are typically used to solve this issue. 3D flow simulation can be used to optimize the process to reduce defects without doing actual runs. Mold flow simulation can effectively reduce the design-to-implementation cycle time, identifying key problems before actual fabrication. In this paper, 3D mold flow simulation using Moldex3D™ V10 is applied to transfer molding to optimize design and process parameters.

This paper proposes and verifies a systematic method that can save computational resources by using 2 steps analysis: simplified panel simulation and single package simulation. The initial step, simplified panel level simulation, is to optimize the process parameters to obtain balanced melt front. The second step is to study on the package level the effect of various package-scale parameters. This analysis provides a prediction of the void location and an insight on the appropriate parameters to minimize void problem. The actual voids location and size from the experiment was captured by SAT machine and short shots were obtained. For final validation, a complete panel-level flow model is built, where the process and design parameters adopted in the actual molding were implemented. The mold filling simulation showed good correlation with the experimental short shots and actual void location. With optimized parameters from the simulation used as guidelines, experimental tests were conducted and the study showed that the simulation is a useful tool to optimize the molding process.

1. Introduction

Flip-chip packages have gained significant use in production over the years because of its high inputs/outputs (I/O), enhanced performance and small form factors[1]. Though the flip-chip technology has various advantages over the other high-density electronic packaging approaches, there are rising challenges to ensure moldability and mimimize defects with rapid advances in flip chip technology such as decreasing bump pitch, stand-off height, thinner package profiles and moldable underfill (MUF) materials. The complexity was further exacerbated by the possible interactions between these factors and their impact on package yield, reliability and performance.

Transfer molding process using MUF for flip-chip devices was developed due to reduction of process steps, cycle time and cost compared with the conventional capillary underfill process. But void entrapment[2] challenges are faced with increasingly small gap at the bumps area under the die, resulting in significant melt front imbalance and flow resistance. Experiments involving a large DOE matrix are typically used to solve this issue. However, applying the conventional trial-and-error method to optimize this process is time consuming and difficult because of the complex interactions between fluid flow, heat transfer and polymerization of MUF. Hence computer-aided-engineering (CAE) is an effective tool for analyzing the complicated physical phenomena inherent in the process of encapsulation of flip chip packages. Simulation can be used to provide further insights of the underlying physics to help address the defect concerns.

In this paper, 3D mold flow modeling of the transfer molding process with MUF using Moldex3D V10 is applied to optimize design and process parameters that can reduce device defects and enhance yield. The Cross Castro-Macosko model is used to define the MUF epoxy viscosity behaviors, where its rheological parameters were acquired using parallel plate rheometer and DSC(Differential Scanning Caloriemeter). The test vehicle selected is a flip chip package with bump height of 100um.

A systematic approach is developed to address the complex flow issues. As the full panel bumped array of flip chip devices would require high computational resources and time, an initial simplified chip level simulation is used to study the effect of various parameters. This analysis provides a prediction of the void location and an insight on the appropriate parameters to minimize void problem. With the insights provided by the preliminary study, the full panel level study is conducted next to evaluate the impact of process and design parameters with the aim of obtaining a balanced melt front and minimize voids.

The actual voids location and size from the experiment was captured by SAT machine and short shots were obtained. The mold filling simulation showed good correlation of the mold fronts obtained by process short shots and actual void locations. With the successful validation of the simulation, the simulation matrix as shown in Fig.1 was designed for a comprehensive assessment of the process, design and material impact on the molding performance.

Geometry	Process	Material
• Bump pitch • Bump height • Bump diameter • Package size • Die size • Die thickness • Bump population	• Mold temperature • Transfer profile • Filling time • Preheat time • Transfer pressure	• Reactive viscosity • Curing kinetics • Gel time

Fig.1: Rheokinetic Flow Modeling Matrix

From the rheokinetic flow modeling of MUF process, we identified the key factors and minor factors on void trapping simulation results from the extensive list of process, design and material parameters. This paper presents the valuable insights of various factors on flip chip device moldability based on process and materials used for the device. The insights can be used as upfront guidelines to predict and reduce potential product defects and failures.

With consideration of process, materials and design, this study has demonstrated that mold flow simulation is an effective tool to reduce the design-to-implementation cycle time with identification of potential void and melt front imbalance issues before actual fabrication. The simulation tool is used actively to-fro in conjunction with materials, process and design inputs and considerations, to predict the trend of various factors on moldability upfront to reduce the yield, cost and cycle time as shown in Fig.2. With our increasing range of flip chip products provided, we provide a comprehensive closed-loop solution including moldflow, thermal, mechanical and electrical studies[3] to the rising challenges faced with greater consumer demands for smaller and thinner flip-chip packages with better performance and greater functionalities.

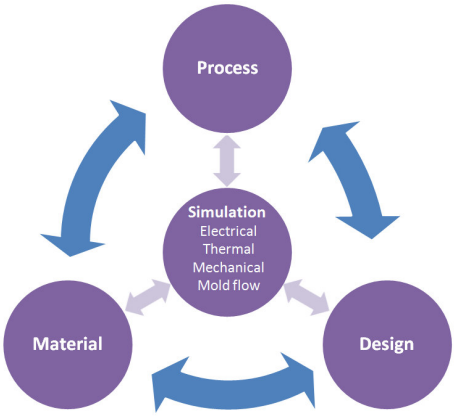


Fig.2: Closed-Loop Material, Process, Design and Simulation to Enhance Flip Chip Product Yield and Reduce Cycle Time

2. Rheokinetic Characterization of Moldable Underfill

In the transfer molding process, flow and heat transfer is dynamically coupled with the curing reaction[4]. The kinetics of the curing reaction not only affects the degree of conversion of the molding compound but also has strong effort on the mold flow with increase in viscosity due to curing reaction. Viscosity is influenced also primarily by temperature and shear rate. Therefore the rheological behavior of molding compounds is of fundamental importance for modeling of the molding process.

The MUF rheokinetic behaviors and other material properties were characterized for the flow modeling, including viscosity with varying shear rates and temperatures, curing kinetics, thermal conductivity, heat capacity and mechanical properties etc. The curing kinetics were measured using DSC with at different temperature ramp-up rates (5, 10, 20, 40°C/min). The experimental data of cure conversions were fitted by numerical parameters using the Kamal's relation [5][6] and the fitting parameters are summarized in Table I for MUF sample A. The experimental data and the numerical fitting line show good agreement, as shown in Figure 3.

$$\frac{d\alpha}{dt} = \left(k_1 + k_2\alpha^m\right)(1-\alpha)^n$$

$$k_1 = A_1 \exp\left(-\frac{E_1}{RT}\right)$$

$$k_2 = A_2 \exp\left(-\frac{E_2}{RT}\right)$$

Parameter of Kinetics	Unit	Value
M	**N/A**	**5.0467 e-1**
N	**N/A**	**1.0207**
A	**1/sec**	**1.7751 e+3**
B	**1/sec**	**1.7746 e+5**
T_a	**K**	**7.0369 e+3**
T_b	**K**	**7.0372 e+3**

Table 1. Numerical parameters using the Kamal's relation and the fitting parameters for MUF sample A

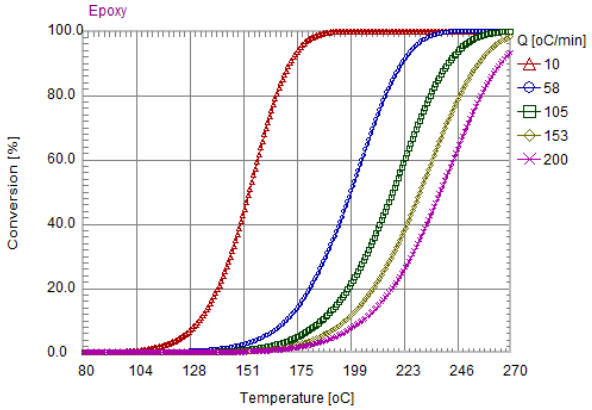


Fig 3. Curing Kinetics Curves:
Conversion (%) vs Temperature

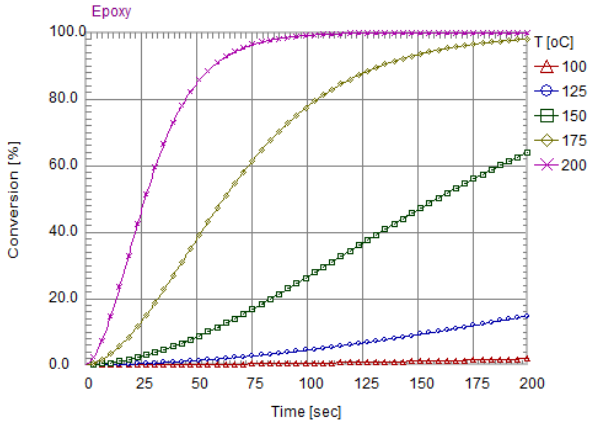


Fig 4. Curing Kinetics Curves:
Conversion (%) vs Time

The viscosity is measured by the parallel plates rheometer at different temperatures ramping rates (10, 20, 40, 60 ^{o}C/min) and different shear rates (1, 2.5, 5, 10 1/s), where the viscosity changes with time. The measured viscosity is fitted by the following Cross Castro Macosko's model [7]. The experimental data set and numerical fitting results with good agreement is shown in Fig 4 and 5.

$$\eta = \frac{\eta_0}{1+\left(\frac{\eta_0 \gamma}{\tau^*}\right)^{1-n}} \left(\frac{\alpha_g}{\alpha_g - \alpha}\right)^{c_1 + c_2 \alpha}$$

$$\eta_0 = Be^{\frac{T_b}{T}}$$

	Unit	Value
n		9.683 e-2
Tau*	Dyne/cm^2	2.000 e+3
B	g/cm.sec	6.263 e-43
T_b	K	4.937 e+4
C_1		1.818
C_2		-5.521
α_g		0.25

Table 2. Numerical parameters for Cross Castro Macosko model

Where γ is shear rate, α is conversion, n is the power law index, η_0 the zero shear viscosity, τ^* is the parameter that describes the transition region between zero shear rate and the power law region of the viscosity curve.

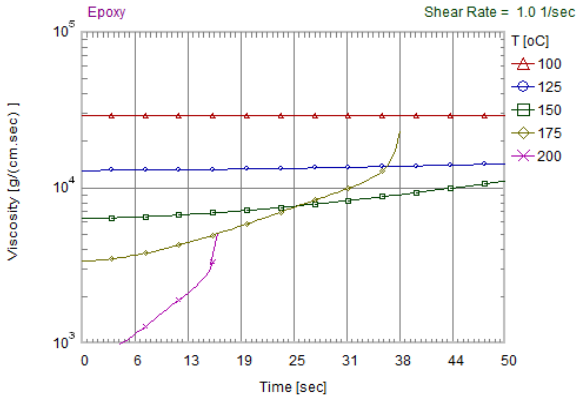


Fig 5. Viscosity Curves:
Viscosity vs Time

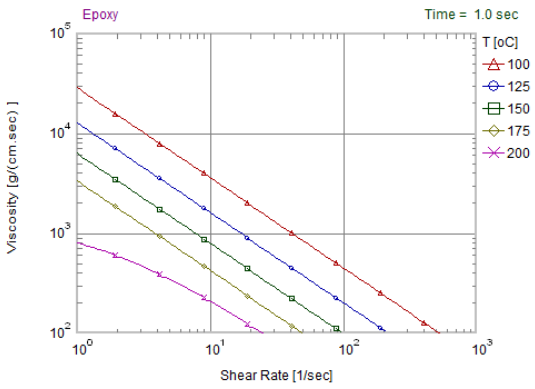


Fig 5. Viscosity Curves:
Viscosity vs shear rate

3. MUF Flow Modeling and Experimental Benchmarking

Results for Flip-chip Test Vehicle

An illustration of the transfer molding of the selected flip chip device for our current study is shown in Fig.6. The die thickness (Dt) is 0.15mm, underfill gap between substrate and die (Bh) is only 0.1mm and total mold height (Mt) is 0.53mm. There are minimum 3 mesh elements between the smallest gaps in the model. The transfer time with optimum ram speed profile control was obtained from the mold process DOE. The transfer molding process simulation is conducted using Moldex3D module for IC molding process. Actual experimental data are used in order to benchmark with our MUF flip chip transfer molding modeling.

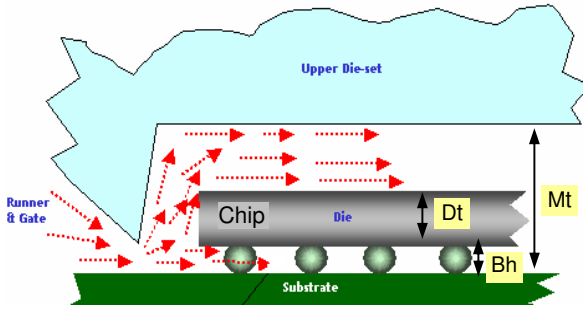


Fig. 6 Transfer molding of the selected flip chip device

The experimental short shots and simulation results are compared to assess the melt front predictions. Table 2 shows the short shots of the mold process results captured during the mold process. The comparison showed good correlation of the melt fronts obtained by process short shots with the mold filling simulation, where the melt front advancement patterns are similar to the simulated melt front contours. The melt front as observed from both short shots and simulations is generally balanced, except for slight flow retardation observed on the die areas due to flow resistance from the narrow flow channels created by the narrow gaps in these areas above the under the dies.

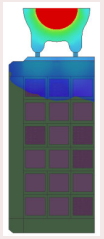
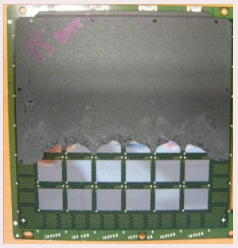
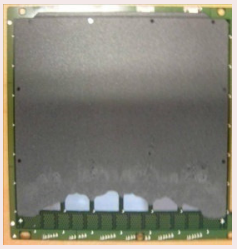
Short Shot Pictures	Moldflow Simulation
Transfer Time: T1	
	
T2	
	
T3	
	

Table 2: Short Shots and
Melt Front Simulations Correlation

The actual voids location and size from the experiment was captured by scanning acoustic microscope (SAT) imaging machine. We can observe the entrapped voids in the underfill areas in selected packages on the different rows in the panel as shown in Table 3. The locations of the simulated and experimental void entraps are nearly identical. Thus the simulation showed good correlation of the actual void locations.

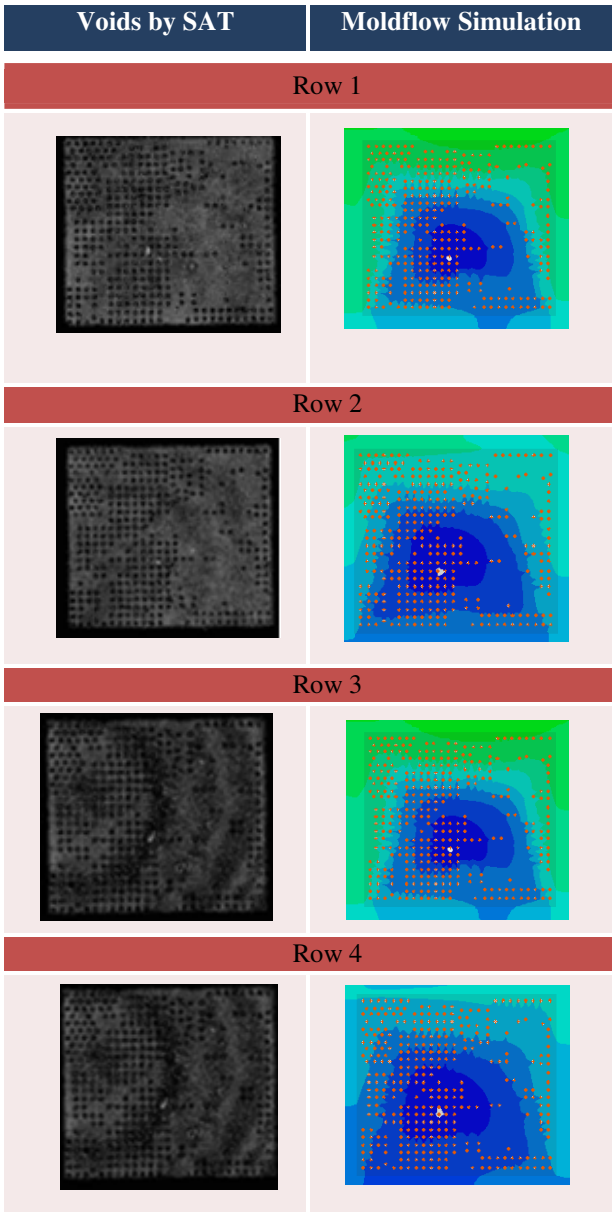


Table 2: Short Shots and
Melt Front Simulations Correlation

Fig.7 shows the simulated melt front advancement contour results for both above and under the die with the flip chip bumps. Initially, the melt front of the mold top side and bottom side are similar, but due to the presence of bumps, the melt fronts above and underneath the die are separated. The melt front near the top side of mold cavity is much faster than that of the bump area of near the substrate side where the 100µm gap is much narrower than the 280µm For this test vehicle, it is observed that the void trapping phenomena is more severe under the more densely bumped area which are next to the much less densely bumped area. The flow imbalances due to the above factors are observed to be key factors of void trapping where the two separated melt fronts are merged again.

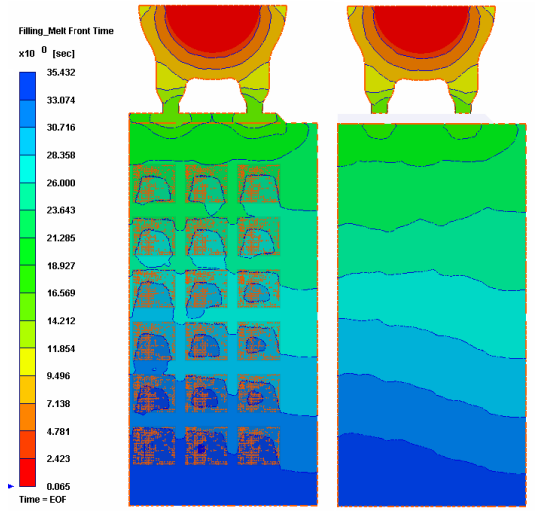


Fig. 7 Panel Level Melt Front Advancement Contours
(a) Below Die (b) Above Die

With the successful validation of the simulation, the simulation matrix as shown in Fig.1 was then studied for a comprehensive assessment of the process, design and material to enhance molding performance.

3. Systematic Evaluation of the Impact of Process and Design Parameters on Molding for a More Balanced Melt Front and Minimizing Void Issues

We have developed a systematic approach to address the complex flow issues. As the full panel bumped array of flip chip devices would require high computational resources (~7million meshes) compared to chip level study (~500,000 meshes), an initial simplified chip level simulation is used to study the effect of various package-scale parameters. This analysis provides a prediction of the void location and an insight on the key parameters to minimize the voiding problems, and overall minimize the cycle time required to obtain the results.

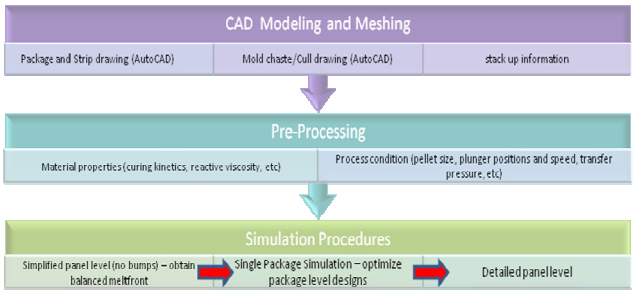
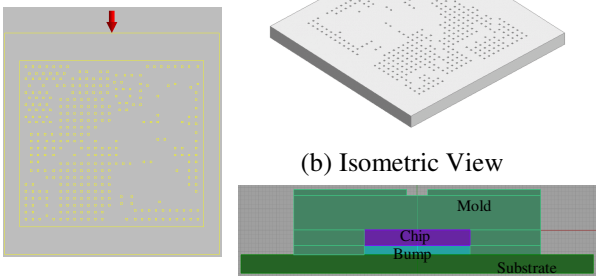


Fig. 8 Flow Chart Illustrating the Systematic Evaluation of the Impact of Process and Design Parameters on Moldability using Molding Simulation Tool Moldex3D

A. Chip Level Simulation

A simplified package 3D model with bumps is first created for an initial analysis as shown in Fig.9, with the mold filling direction as indicated by the red arrow.



(b) Isometric View

(a) Top WireframeView (c) Side View

Fig. 9 Chip Level Simulation Model

The process parameters such as filling time and mold cavity temperature are first varied to analyze the impact of process parameter change on the molding performance using the molding simulation tool. The filling time was varied in the following two key ranges; 0.5s, 1s, 2s (much below gel time) and 10s, 20s, 30s (near gel time). The results as shown in Fig. 10 show that when the filling time is varied in the range much lower than the MUF gel time, the change from 0.5-2s results in minor impact on the void location. This may be due to the minor change in viscosity during this time range (Fig.5) and hence the minor impact on void locations. When the filling time is varied in the range near the MUF gel time, the voiding location varies, for this case shifting closer to the gate side. This could be due to the sharp change in viscosity near the gel time (Fig.5) and with the rapid change in viscosity, a more significant impact on void locations is observed. The results will vary based on the molding material used.

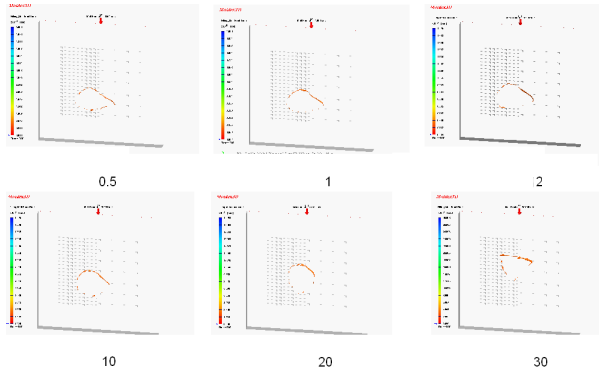
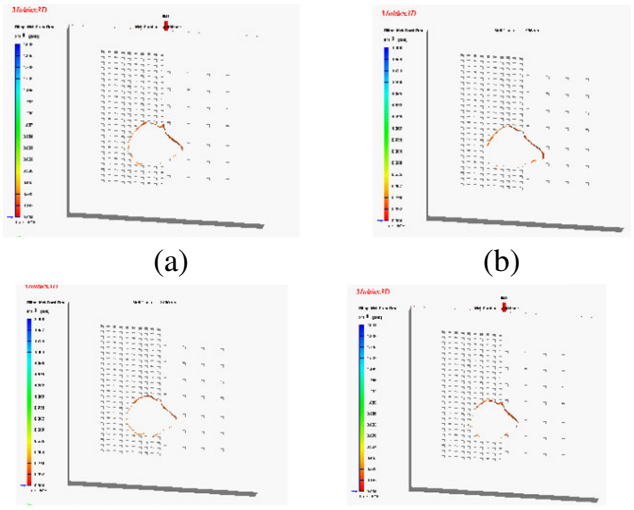


Fig. 10 Impact of Filling Time (s) on Void Location

The mold temperature was varied in the following range: 130°C, 150°C, 170°C, 190°C, 210°C. For this analysis, the filling time is 2s. The results as shown in Fig. 11 show that when filling time is in the range much lower than the MUF gel time, the change from 130°C - 210°C results in minor impact on the void location. This may be due to the minor change in viscosity during this time range, even as the temperature changes from 130°C - 210°C. The results may vary with different material and filling time used.



(a) (b)

(c) (d)

Fig. 11 Impact of Mold Temperature on Void Location, a) 130°C, b) 150°C, c)170°C, and d)190°C

Next, the impact of different die thickness keeping the bumps and total package height constant to conducted to study the impact of different gap sizes above and under the die on melt front. As shown earlier in Fig.7, initially, the melt front of the mold top side and bottom side are similar, but due to the presence of bumps, the layout and different in gap sizes between the die top to the mold cavity and bump height, the melt fronts above and underneath the die are separated. The melt front near the top side of mold cavity is much faster than that of the bump area of near the substrate side. The preliminary results indicate that the flow imbalances are potential key factors of void trapping where the two separated melt fronts are merged again. Due to the clearance difference above and under the die, larger flow lag is observed under the die, and we will like to investigate if voids issues reduced by creating better flow balance. Hence, two different die thicknesses as shown in Fig. 12 and Fig. 13 are studies to analyze the impact of similar gap sizes above and under the die on melt front.

Fig 12: Chip Thickness of 0.15mm

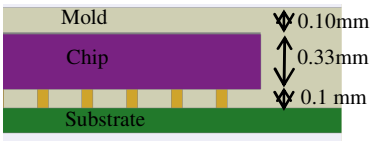


Fig 13: Chip Thickness of 0.33mm

The cross section planar cut is shown in Fig. 14 and the results of the cross sectional melt front advancements for both the thin and thick dies are shown in Fig 15 and Fig 16. The results show that the balancing the flow resistance by decreasing the gap from die top to mold cavity resulted in a more balanced melt front above and underneath the dies, reducing the voiding issues caused where the two separated melt fronts are merged again.

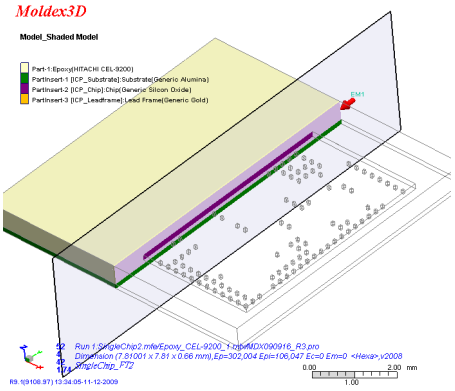


Fig 14: Cross Sectional Planar Cut for Analysis

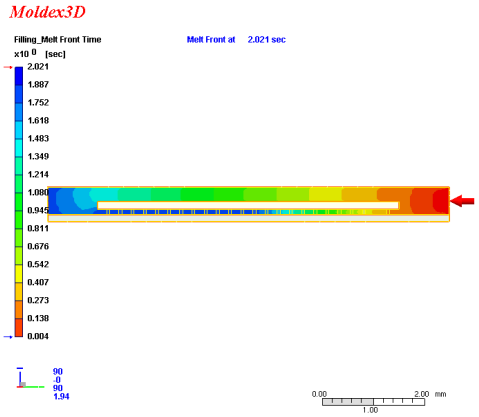


Fig 15: Melt Front Profile for Chip Thickness of 0.15mm

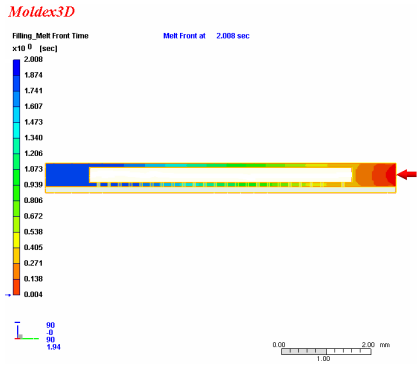
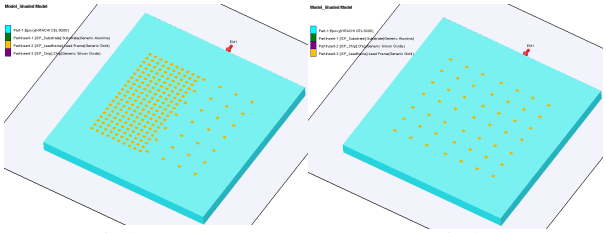


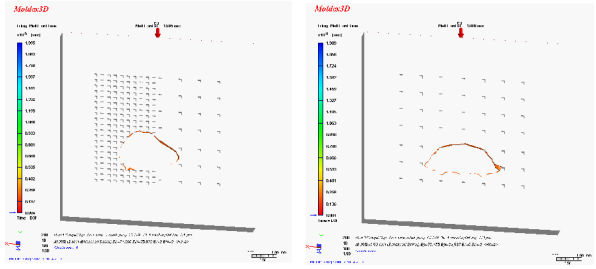
Fig 16: Melt Front Profile for Chip Thickness of 0.33mm

We also varied the bump layout to analyze the impact of different bump pitch and layout on the void locations, keeping the die thickness, bump height and total package height constant. In Fig 17, Pitch Array A has the denser bump area with pitch of approximately 0.1mm and the less dense bump area with pitch of approximately 0.6m. The results as shown in Fig 18 indicate that the different bump layout influences the location of the voids trapping. With the denser bumps area located next to the less dense bumps areas, the flow resistance caused by the denser bumps resulted in the shifting of void locations to the area with the denser bump layout. In comparison, when the bumps are evenly distributed, the void location is more centralized, though neared to the vent side with higher viscosity towards the end of filling affecting the void process.



(a) Pitch Array A (b) Pitch Array B

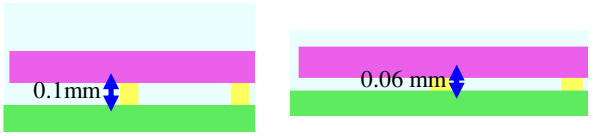
Fig 17: Different Bump Layout Simulation Models



(a) Pitch Array A (b) Pitch Array B

Fig 18: Void Locations for Different Pitch Arrays

The bump height is also varied to analyze the impact of different bump height on the void locations, keeping the die and mold thickness constant. As shown in Fig 19, two different bump heights were evaluated; 0.1mm and 0.06mm, shown in Fig 19(a) and Fig 19(b) respectively. The bump layout used is Pitch Array A as shown in Fig 17(a). The results as shown in Fig 20 and Fig 21 indicate that the bump height has an impact on the location of the voids trapping. With the smaller bump height of 60µm while keeping the other factors constant, the flow resistance of the bump area near the substrate side is increased compared to the larger smaller bump height of 100µm. Hence the melt front separation for the device with smaller bump height of 60µm above and underneath the die is more pronounced. The melt front near the top side of mold cavity is much faster than that of the bump area of near the substrate side when bump height is smaller, resulting in voids trapped nearer to the gate side where the two separated melt fronts are merged again.



(a) Bump Height 1 (b) Bump Height 2

Fig 19: Void Locations for Different Bump Height

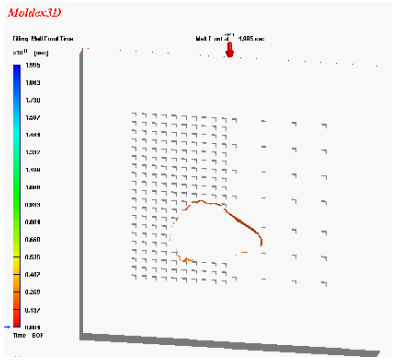


Fig 20: Void Locations for Bump Height 1 (0.1mm)

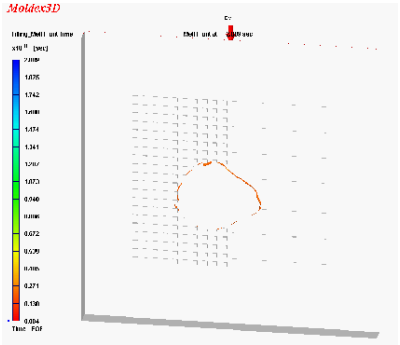
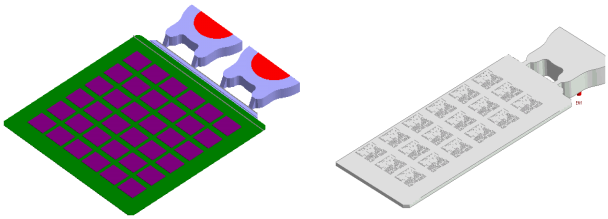


Fig 21: Void Locations for Bump Height (0.06 mm)

With the insights provided by the preliminary study, the full panel level study is conducted next with the aim of obtaining a balanced melt front and minimizes voids in the most efficient way.

B. Panel Level Simulation

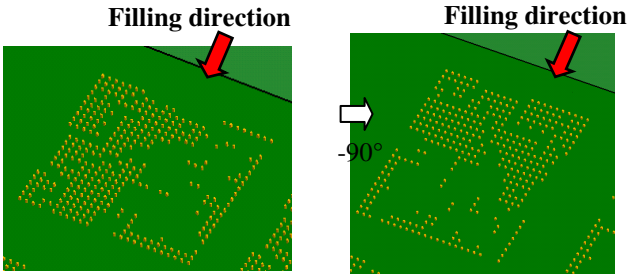
The panel level simulation model is shown in Fig. 23. The total number of finite element meshes used for full panel 3D model for the current study is about 7 million, compared to 500,000 meshes for the chip level study. Analysis was also conducted to ensure that the trends for the single chip are representative of panel level studies for this selected test vehicle and conditions. From our findings, the identified trends of the single chip analysis are representative and insights useful for the subsequent full panel analysis for this test vehicle under the investigated conditions.



(a) Panel Solid Model (b) Panel Wire Frame Model

Fig. 22 Panel Level Simulation Model Isometric View

For the panel level analysis, we varied the chip orientation and study its impact on the void location for this test vehicle. Two different chip orientations were analyzed as shown in Fig. 24 (a) and (b).

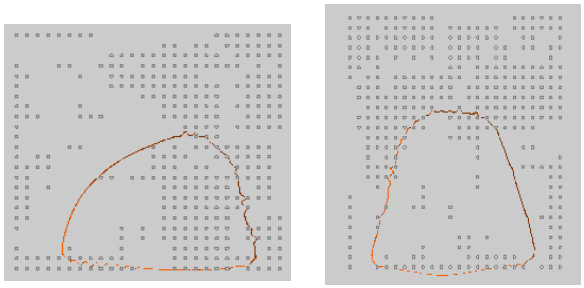


(a) Chip Orientation A (b) Chip Orientation B

Fig. 23: Panel Level Simulation Model for Different Chip Orientation

The results of the two different chip orientations on the melt front advancements and potential void locations are shown below in Fig 23, Fig 24 and Fig 25. From the results, we observed that different chip orientation resulted in different mold filling trends. For chip orientation A, the denser bump area on the right resulted higher flow resistance, where the melt fronts merged at the area of the denser bumps area, and the potential

voids location shifting towards the denser bump area. For chip orientation B, the denser bump area on top towards the gate side resulted in flow retardation at that area and melt fronts merging nearer to the center of the chip compared to the chip orientation A where the voids are located nearer to the vent side. The results are also shown both for the panel view for both chip orientations as shown in Fig 24 and Fig 25.



(a) Chip Orientation A (b) Chip Orientation B

Fig. 23: Melt Front on a Package on the Panel for Different Chip Orientation

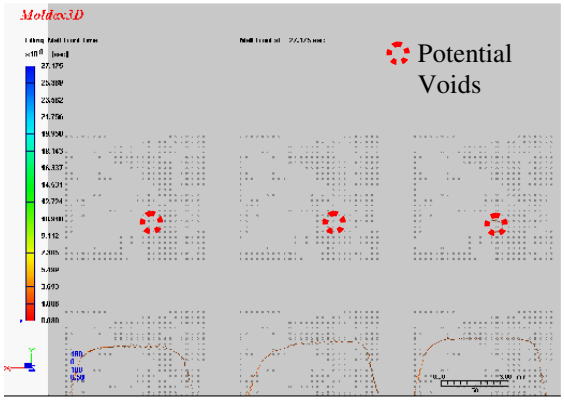


Fig. 24: Melt Front on First Two Rows on the Panel for Chip Orientation A

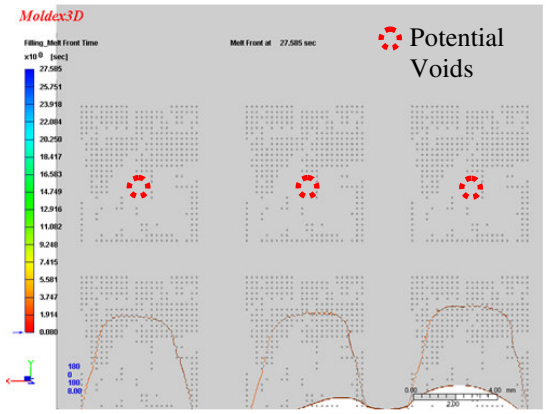


Fig. 25: Melt Front on First Two Rows on the Panel for Chip Orientation B

4. Conclusions

This paper has demonstrated our 3D mold flow modeling capability of the transfer molding process for flip chip devices with MUF using Moldex3D V10. The full MUF rheokinetic behaviors and other material properties were characterized for the flow modeling. The full panel molding simulation was conducted and compared with actual voids locations captured by SAT machine and short shots. The mold filling simulation showed good correlation of the mold fronts obtained by process short shots and actual void locations. With the successful validation of the simulation capability, the tool is then applied to optimize design and process parameters to enhance flow balance, reduce voiding problems and device defects.

To address the complex flow issues with multiple interactive factors, we designed a systematic approach to tackle the problems. An initial simplified chip level simulation is used to provide insights on the key parameters to minimize void problem. With the insights provided by the preliminary study, the full panel level study is conducted next to evaluate the impact of process and design parameters with the aim of obtaining a balanced melt front and minimize voids. Such an approach will reduce the computational resources and total cycle time required to provide mold flow solutions.

From the rheokinetic flow modeling of MUF process, we identified the key factors and minor factors on void trapping simulation results from the extensive list of process and design parameters for this study; including filling time, mold temperature, different gap sizes above and under the die, bump pitch, bump layout, bump height and chip orientation. These insights can be used as upfront guidelines to predict and reduce potential product defects and failures.

With consideration of process, materials and design, we have demonstrated that mold flow simulation is an effective tool to reduce the design-to-implementation cycle time with identification of potential void and melt front imbalance issues. With our increasing range of flip chip products provided, we provide a comprehensive closed-loop solution including moldflow, materials, process, thermal, mechanical and electrical studies [3] to address the rising challenges faced with greater consumer demands for better performance and greater functionalities.

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