Name: **AYTHA RAMESHKUMAR**
Designation:Associate Professor
Department:Electronics and Communication Engineering
Mail ID:rameshkumar_a@vnrvjiet.in
Experience (inyears):Teaching:19 yrs Research:00 Others (Industry):4yrs

1.Educational / Technical qualifications:

S.No	Level (UG / PG / Ph.D)	Year of passing	Specialization
1	B.E.	1991	Electronics
2	M. Tech.	2006	VLSI Design
3	Ph.D.	Pursuing	VLSI Design

2.Teaching and Learning:

2.1 TeachingInterests:

- VLSI Design,IOT, Micro controllers and its Applications, Microprocessors, CPLD &FPGA Architectures & Applications, Wireless communication and embeddedsystems.

2.2 Novel Teaching & Learning Techniquesadopted: PPTs, Videos, Group Discussions, POGIL, Chalk and Talk, WIT &WILetc.

2.3 Involvement in curriculum updating /Design:

- Academic Committee Member for Dept. of ECE for Curriculum design. VNRlab protocol for Microprocessor& Microcontrollers Lab, Embedded SystemsLab.

3. Co-curricular and Extra-CurricularActivities

3.1. Interests and Hobbies: Sports, ListeningMusic

3.2. CCA/ECA Organized: Convergence-2k17, Convergence-2k16, Convergence-2k15, Scintillaschunz

3.3. CCA/ECAparticipated:

- Project Evaluation committee member for M.Tech (EmbeddedSystems).
- Department Entrepreneurship cell in-charge.
- Student IETE Societyin-charge

3.4. Counseling and MentoringActivity:

- Counselor and mentor for B.TechStudents.

Committees involvedin: Departmentlevel:

- Academic CommitteeMember
- Project Evaluation CommitteeMember
- Technical Seminar Evaluation Member Institute Level:
- In-Charge for Telecom forcollege
- Student IETE societyin-charge
- Department Entrepreneurship cellin-charge

4.Conference / Workshop / Seminar / Guest Lectures:

4.1 Conducted:16

- National conference VelaSiEm-2k7 at VNRVJIET in2007
- Short term intensive course on Embedded Architecture & Applicationsat
- VNRVJIET, Hyderabad on 12-14, February2009
- Workshop on IOTs & Its Applications at VNRVJIET in 2016 on 12-14, February2016.
- Member of the Reception, Decoration, Stage Management committee andHospitality
- Organized 7th IEEE International Advance Computing Conference(IACC2017) at VNRVJIET,Hyderabad on 5th -07th January2017.

4.2 Attended: ICEEOT- 2016, IACC – 2017,E&ICT IITG, NITW,NITP, IITB,KU

- A week FDP on “LaTeX & Technical Report Writing” from 25th to 30th May 2020.

- A Five Day FDP on "Establishing Research Beyond Horizon" from 26th to 30th May 2020.
- Webinar on "Relax, Refresh, Rejuvenate" on 30th April 2020.
- Webinar on "Latex – A Scientific Documenting Tool" on 21st May 2020.
- One week NIT & JNTUH " 5G Technologies" by JNTUH , Hyderabad ,18th Dec-24th Dec 2017.
- One week FDP on "Integrated circuit and System Design Using CAD Tools" by VNRVJIET, Hyderabad from 12th -17th June 2017.
- Two-week ISTE STTP "CMOS Mixed Signal and RF VLSI Design" by IIT Kharagpur at VNRVJIET, Hyderabad,30th January 2017 to 04th February2017.
- IEEE International Conference on Electrical, Electronics and Optimization Techniques, at DMI College of Engineering, Chennai, 3-5th, March2016.
- FDP on "Trends in wireless Technologies and Evolution of Simulation tools, at VNRVJIET, 11- 23, May2015.
- TEQIP- II sponsored training program on "VLSI Design Flow Using CAD Tools and Hardware Implementation" at VNRVJIET, Hyderabad, 27thJuly-07th August 2015.
- 7th IEEE International Conference on Technology for Education at NIT, Warangal,10-12, December 2015.
- " Three Day Workshop on Outcome Based Accreditation" by NBA Nodal Centre, JNTU Hyderabad, 15th-17th February2014.
- Workshop on ASIC Design Flow Using Industry Standard EDA Tools organized by VNRVJIET on 21st-27th June 2013.
- Workshop on Wireless Sensor Nodes by VNRVJIET on 19 th-20th June2013.
- Seminar on Research Publications and Documentation by VNRVJIET, Hyderabad on 04th May2013.
- Three day International conference on REIMAGINE STEM at VNRVJIET Hyderabad.
- Workshop on "Low Power VLSI Design Methodologies" by SYNOPSYS at CVED JNTUH, Hyderabad, INDIA.
- Work shop on "VLSI Design Methodologies" by SYNOPSYS at Padmasree B.V.Raju Institute of Technology, Narsapur, INDIA, 6th -7th March2009.

5.Academic Contribution and Research &Consultancy:

5.1.Invited Lectures:

- Delivered Guest lecture on overview of Internet of things in VNRVJIET
- Delivered Guest Lecture on VLSI Design at Lords Institute of Engineering & Technology, Hyderabad –November 2014
- Delivered Lecture in FDP on Recent trends in Embedded Systems design in VNRVJIET in November2013.

5.2. Articles/Chapters published in Books:Nil

5.3. Books published as single author or as editor:Nil

5.4. ProjectsGuided:

a)UG:18 b)PG:18

5.5. Research Interests: VLSI design, Data Transmission Protocols and ProcessorArchitectures and EmbeddedSystems

5.6. Ph.D students:Nil

a)Enrolled:Nil b)Submitted:Nil c) Awarded:Nil

5.7. Papers published in reviewedJournals:

S.No	Title of the Paper	ournal Name Vol.No.PP	ISBN/ISSN No.	Impact Factor/ Citation Index	National/ International
1	Hierarchical Matched Filter Implementation on FPGA for WCDMA Systems	Journal of Communication and Computer, USA.August 2011, Vol8, PP 686-692.	ISSN No.1548-7709	2.69	International
2	Emotion Recognition from Speech Using Embedded Board OMAP 3530	IJARET, India, October 2013, vol.1, issue ix, page no.38-44.	ISSN 2320-6802	2.375	International
3	Implementation of Primary Synchronization signal Detection in LTE	International journal of Advance Engineering and Research Development , Volume 5, Issue 04, April 2018	ISSN : 2348-6406	5.71	International
4	Implementation of Secondary Synchronization in LTE	IJCRT, 2018	ISSN: 2320-2882	5.97	International
5	Implementation of synchronization for 5G NR system	Advanced Science Letters,Vol.26, No. 06,129-135pp.	E-ISSN: 1936-7317	6.224	International
6.	Implementation of 5G NR Primary and Secondary Synchronization	Turkish Journal of Computer and Mathematics Education, Vol.12, No.8, 2021,3153-3161P.P.	E-ISSN: 1309-4653	0.32	International SCOPUS

5.8. Papers presented at National / International conferences:

S.No	Title of the Paper	f the Conference/ Seminars	National/ International	Period
1	Performance Evaluation For Digital Matched Filters	National conference on VLSI & Embedded Systems	National	June 2009
2	Hybrid Form Hierarchical Matched Filter on Field Programmable Gate Arrays based on WCDMA	International Conference on Systemics, Cybernetics, and Informatics (ICSCI-2010)	International	January 2010.
3	Implementation of Hierarchical Matched Filter on FPGA for WCDMA Systems	International Conference on Advances in Information, Communication Technology and VLSI Design (ICAICV-2010)	International	August 2010

4	Implementation of Secondary Synchronization Detector for WCDMA Systems	IEEE International Conference on Electrical, Electronics and Optimization Techniques,	International	March 2016.
5	The Fastest Possible Solution to the Weighted Water – Filling Problems	7th IEEE International Advanced Computing Conference (IACC 2017)	International	January 2017

5.9. Sponsored research Projects:Nil

5.10 Consultancy Projects: Nil

6.Awards / Honors received:

Best paper award in International Conference on Systemics, Cybernetics, and Informatics (ICSCI-2010), Pentagram Research Centre, Hyderabad, January 2010.

7. Motto: Work is Worship & Efficiency is Divine Vision, Work & Efficiency SecureLife