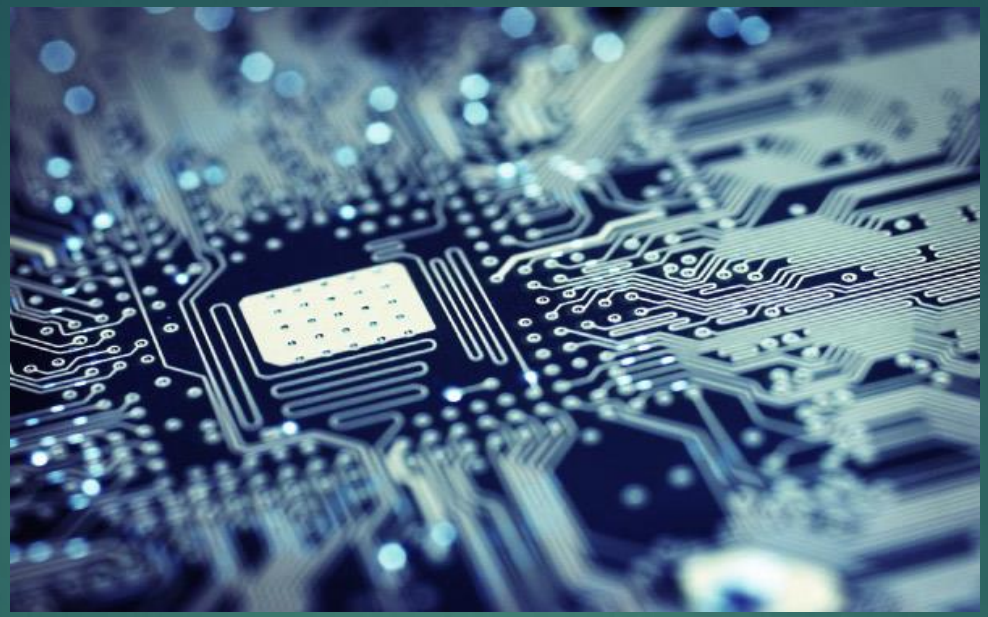


NETWORK ON CHIP

-PRESENTED BY KARTIK PATEL AND KARISHMA REDDY

AGENDA

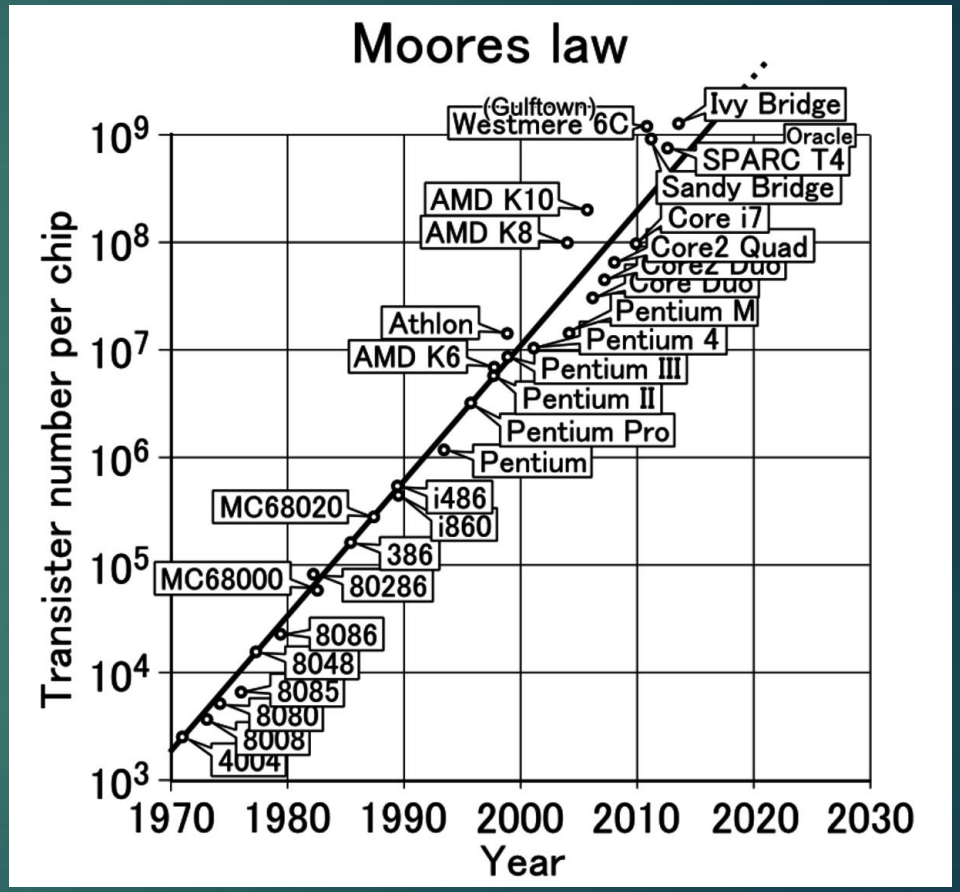
- Defining NoC and its need
- NoC topologies
- Switching Mechanisms
- NoC Switch/Router architecture
- Different types of interconnections
- Challenges associated with the novel interconnections
- Current trends in NoC
- References

End of Moore's Law?

- The number of transistor doubles in a chip every one and a half years.
- Frequency scaling does not help since it increases power dissipation.

Possible Solution

- Increase in the number of cores-parallelism.

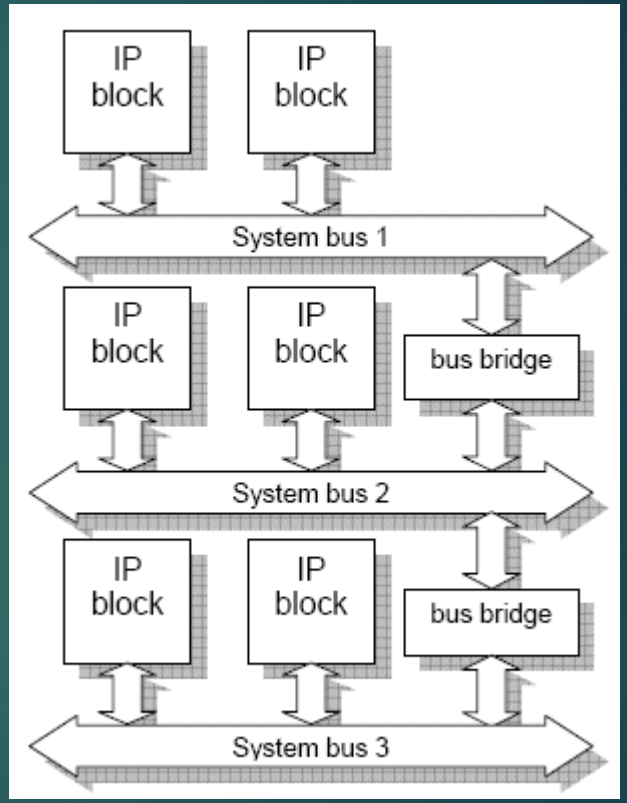


Traditional interconnection of Cores

- Traditional on chip interconnect architectures uses shared medium arbitrated bus.

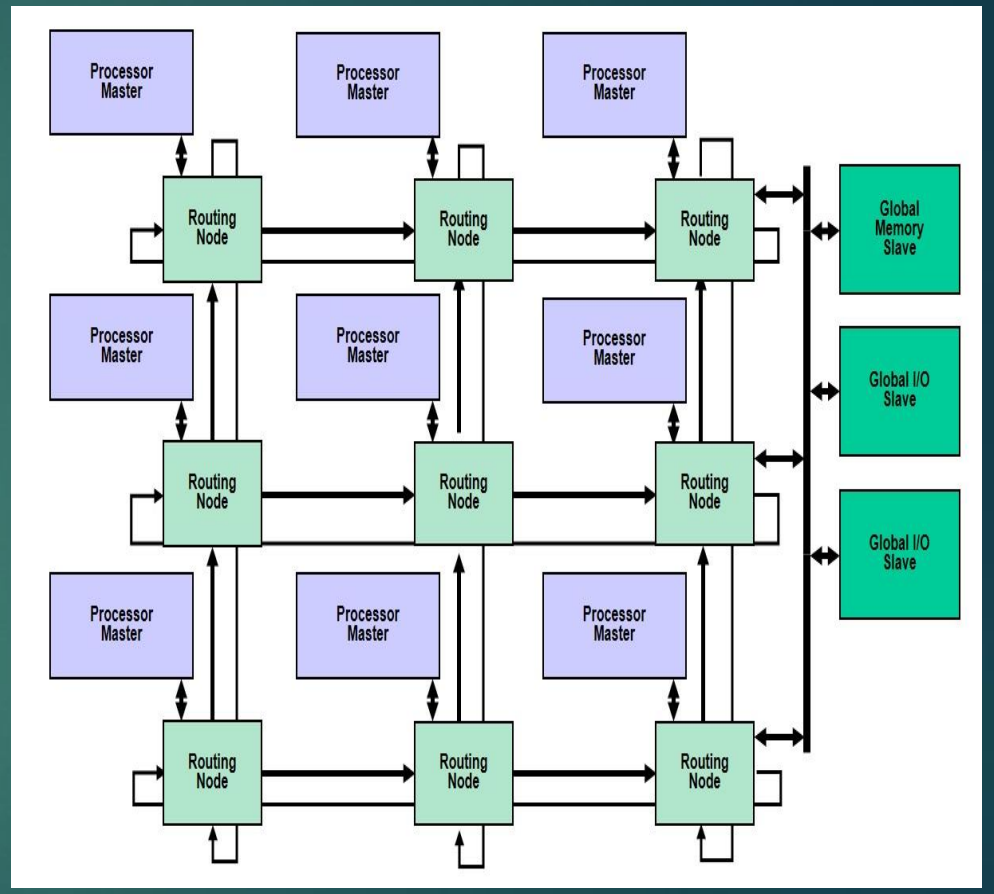
Why move to network on Chip?

- Every unit attached will add additional parasitic.
- Bandwidth is limited and shared among all the IP Blocks.
- Difficult to test.



How about a Network on Chip?

- The ever increasing demands in terms of computational intensity and low power has lead to the development of faster chips.
- Faster chips lead to increased power dissipation.
- In order to tackle the above mentioned issue, we have turned to increasing the computing resources on the chip
- Interconnection of all these processing elements using a simple shared bus architecture is not a feasible option.



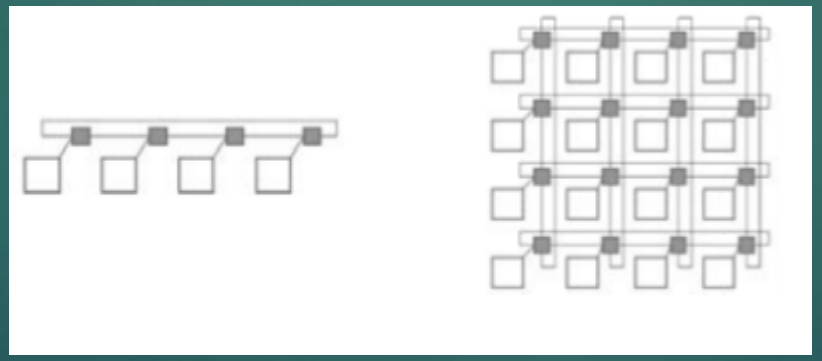
How about a Network on Chip?

- As a solution to the scalability and the bandwidth problem, we use the Network On Chip architecture.
- Network On Chip is an on-chip packet switched micro-network of interconnects. It applies data networking concepts to inter-node communication.
- Inserting routers in between communicating objects reduces the required wiring. The different IPs within the chip can be considered as nodes and a specific topology can be chosen to be implemented as an SOC design.
- It provides us with freedom from the problem of scalability and complex wiring. Since all links can operate on different signals simultaneously, parallelism is achieved .

NoC Topologies

- Direct Topology:

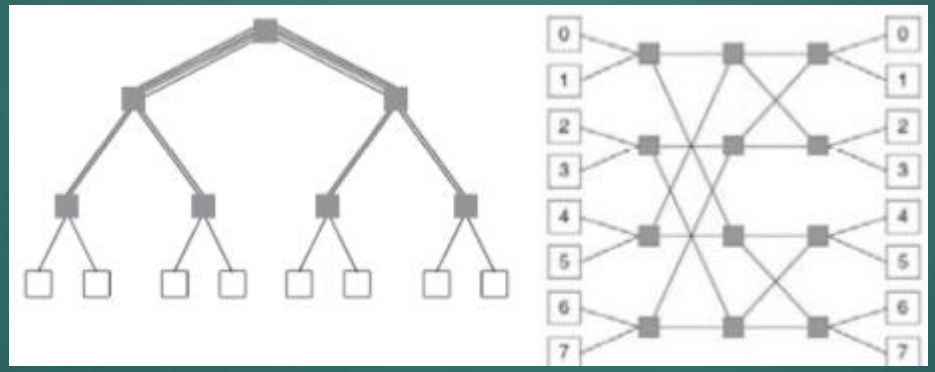
  Each node (processing element) is connected using a point-to-point direct link to its neighbors. A fundamental drawback is the increase in connectivity and cost with increase in the number of nodes.



NoC Topologies

- Indirect topology:

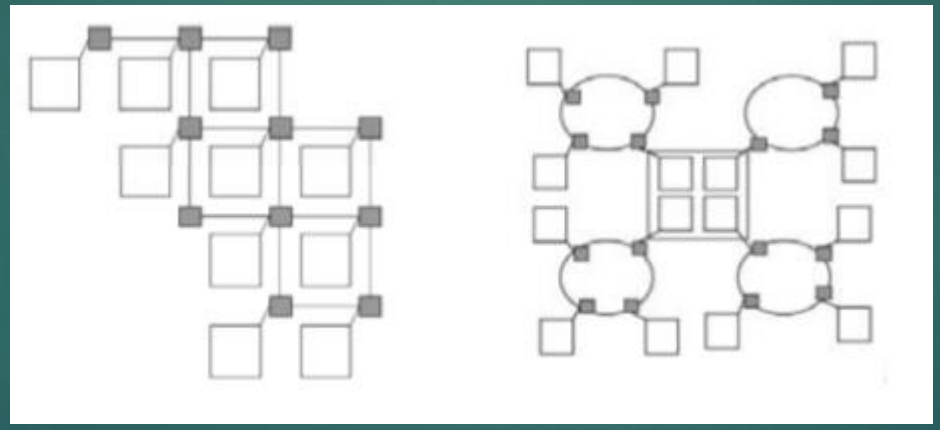
  Each node is connected to an external switch which in turn has point-to-point links to other switches.



NoC Topologies

- Irregular Topology:

  This type of topology is something that has been customized for a specific application.



How does data route?

- Switching Techniques
  - Circuit Switching
  - Packet Switching
    - Wormhole
    - Store and Forward
    - Cut-through

Packet switching

- Store and Forward

Message is split into fixed sized packets which consists of flits, starting with the header flit and the router decides after it has the entire message in its buffer.

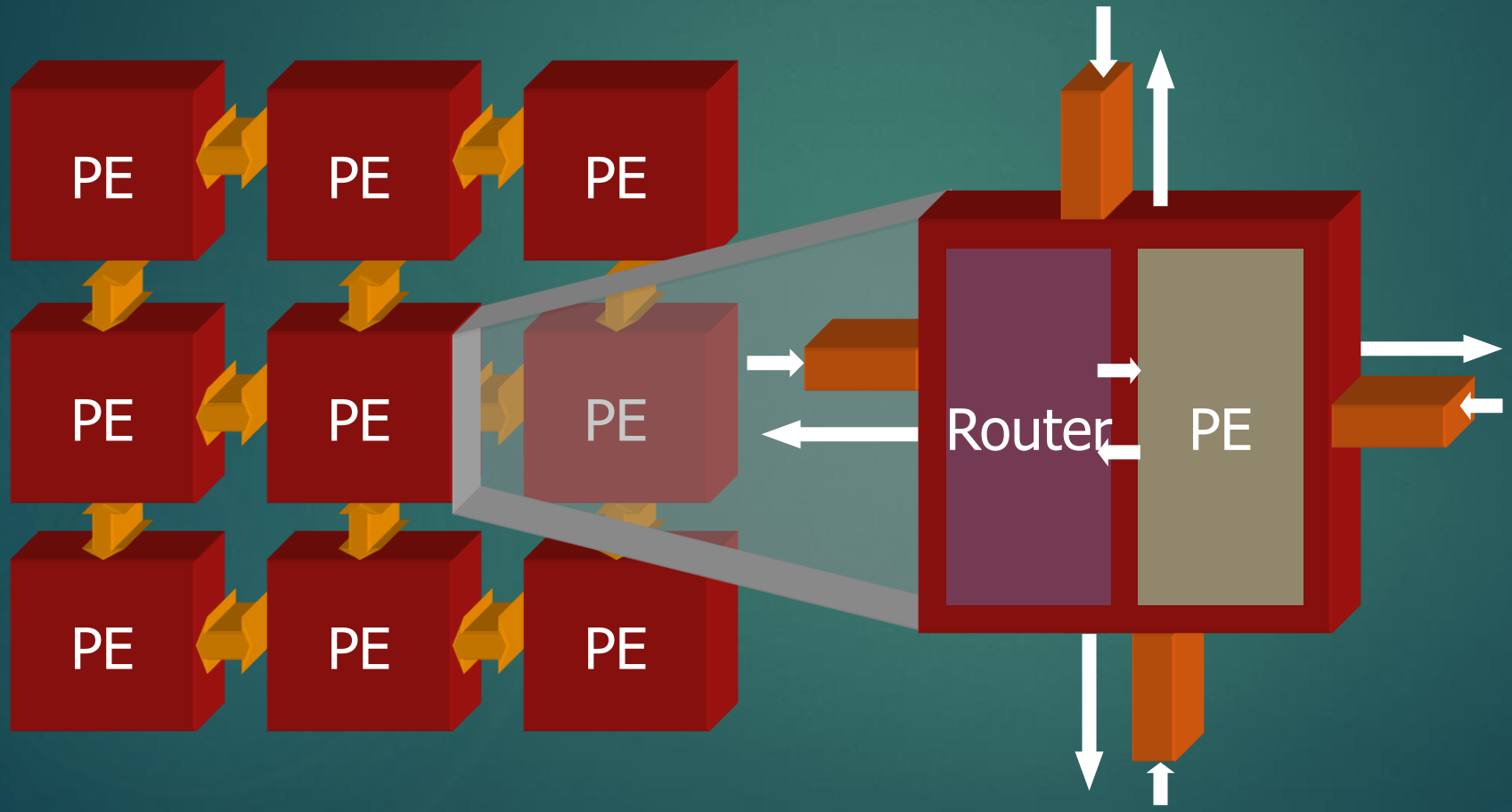
- Cut through

Same as Store and Forward but the header flit is cut through to the next router as soon as the decision is made.

- Wormhole

Same as cut through but each router has small buffers the size of one flit instead of an entire packet.

A look inside the NoC



Switch/Router architecture

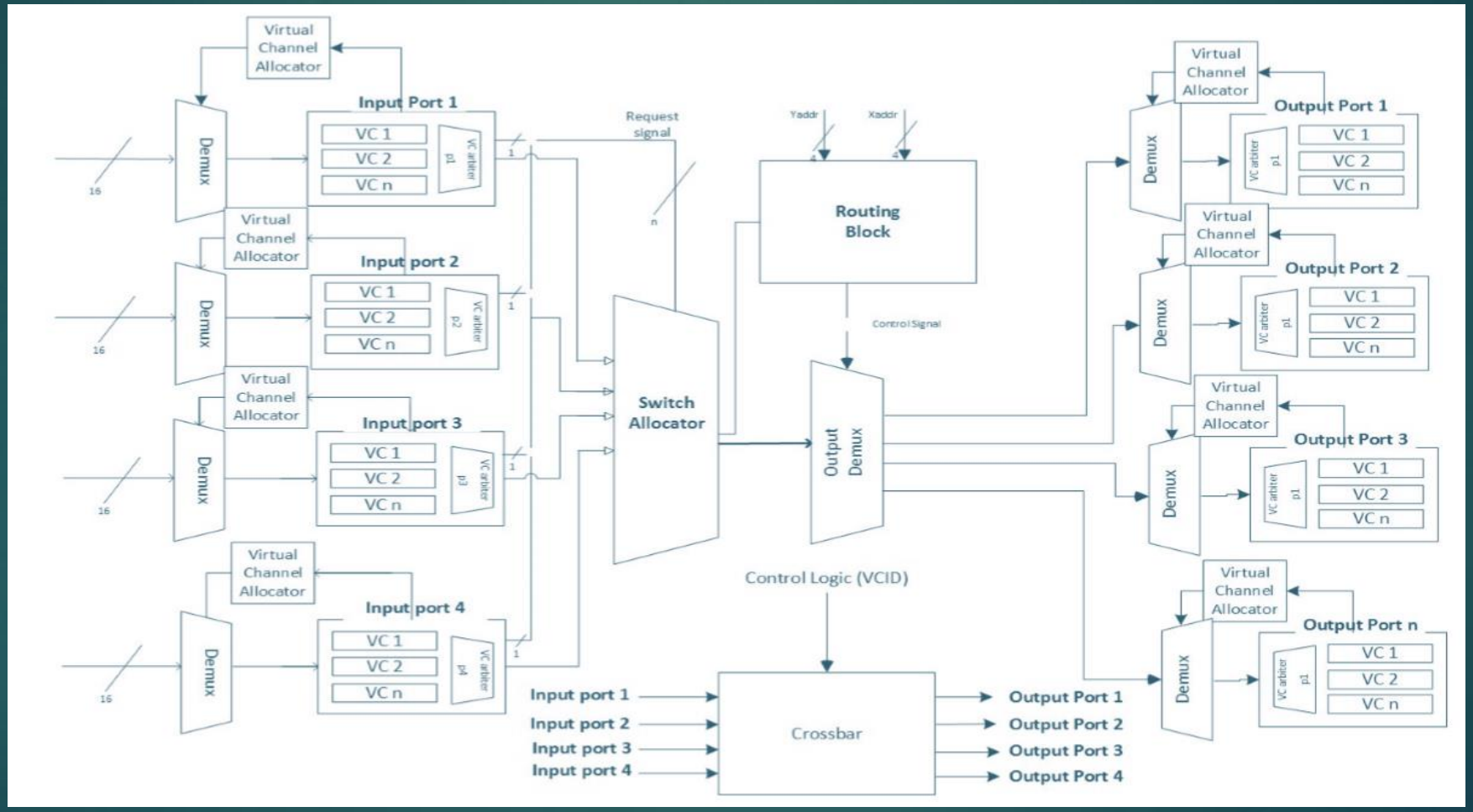


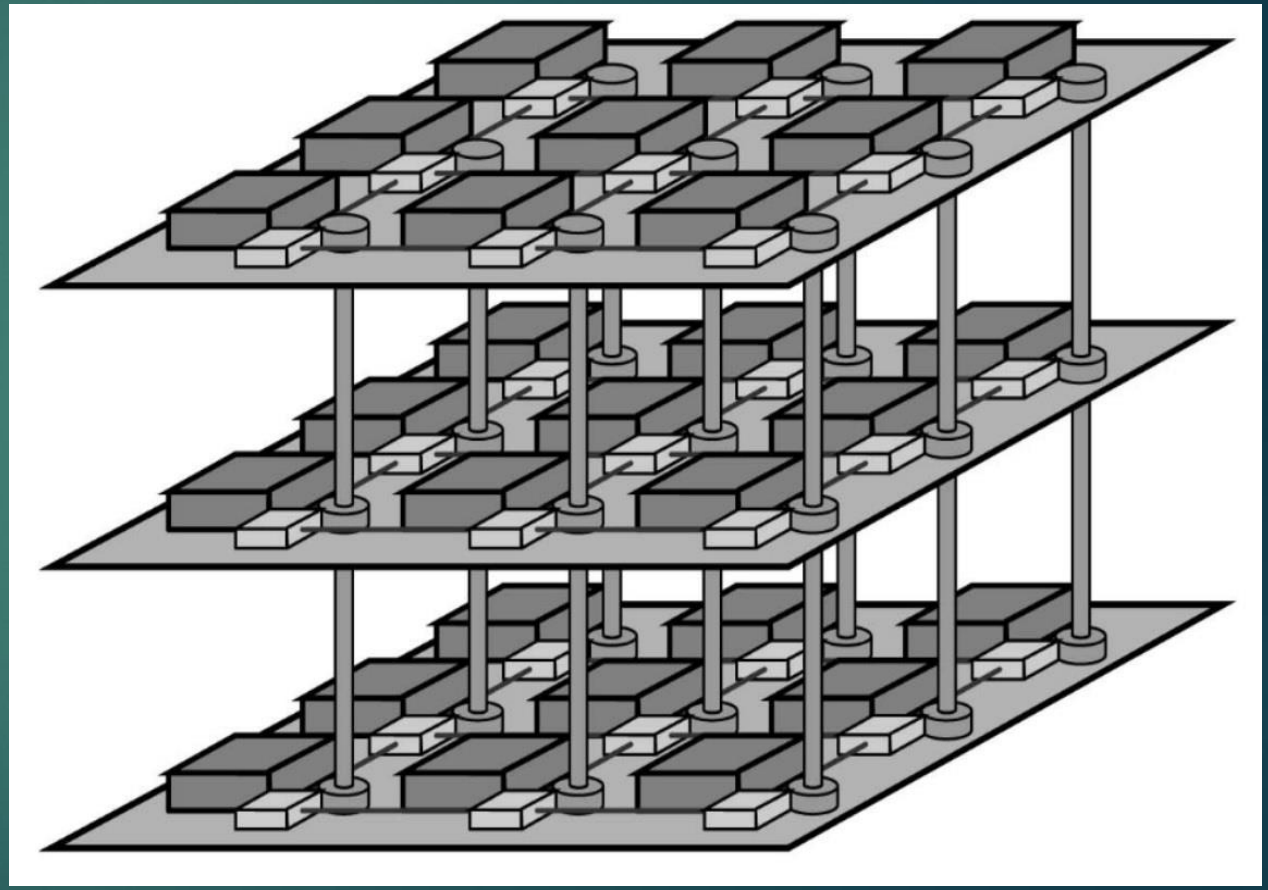
Fig. NOC router architecture.

Different interconnection techniques

- 3D Noc
- Photonic interconnects
- Wireless interconnects

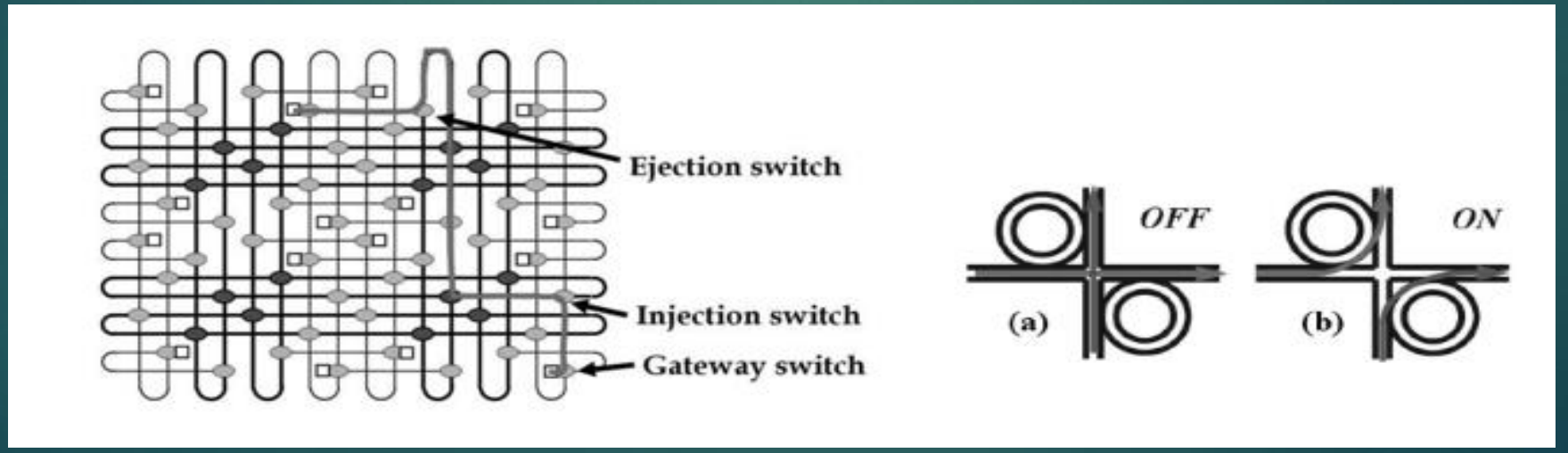
3D NoC

- Multiple active layers are stacked together
- In a given layer, interconnects are wireless and between the layers, the interconnects used are TSVs.



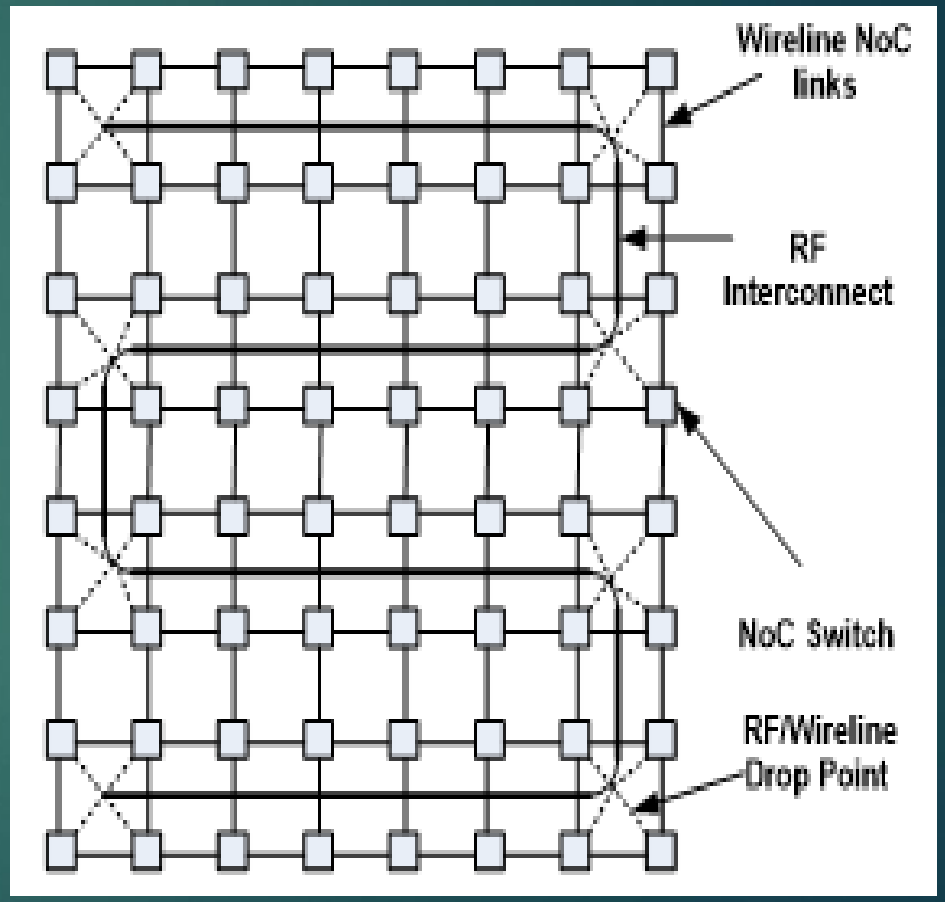
Photonic Interconnections

- These interconnects route data in the optical form from the source node to the destination node.
- The conversion from electrical to optical and optical to electrical is achieved using modulators and demodulators.



Wireless Interconnections

- Eliminates the use of physical connections by replacing them with wireless links.
- Each IP contains its own transmitter and receiver in the form of antennas in order to facilitate communication.

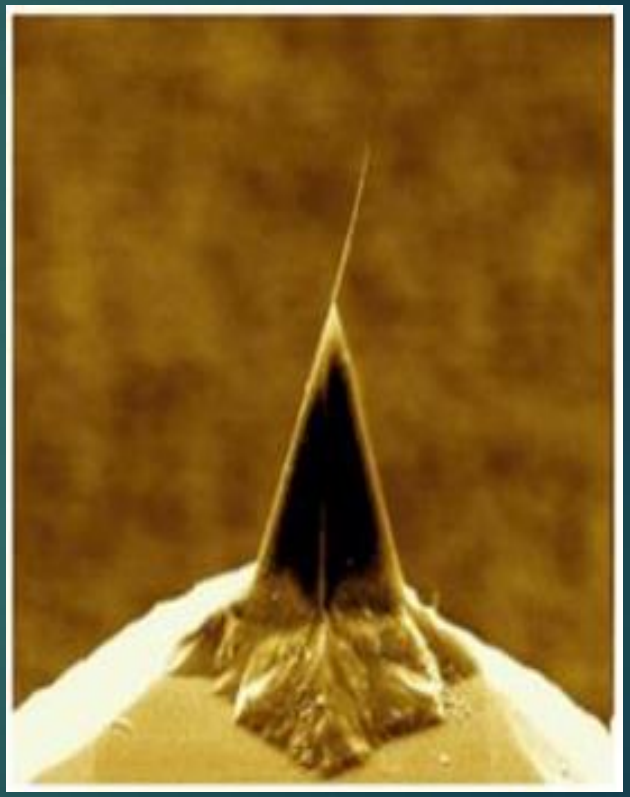


Challenges with them

- 3D NoC faces the challenge of high power dissipation resulting due to the increase in area density and smaller footprint.
- Photonic interconnects face the challenge of the practical realization of the concept due to the complexity of the integration of the photonic components.
- Wireless NoC faces the challenge of precision of the high frequency oscillators and filters.

Current trends in NoC

- The current research going on in this field involves the search for antennas that will provide efficient transmission and reception.
- An alternative being studied to replace the metal antenna is the carbon nanotube antenna.
- These antennas will be able to provide high frequency while occupying lesser area but their practical implementation is still a topic of research.



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