International Journal of Management, IT & Engineering
Vol. 8 Issue 10, October 2018,
ISSN: 2249-0558 Impact Factor: 7.119
Journal Homepage: http://www.ijmra.us, Email: editorijmie@gmail.com
Double-Blind Peer Reviewed Refereed Open Access International Journal - Included in the International Serial Directories Indexed & Listed at: Ulrich's Periodicals Directory ©, U.S.A., Open J-Gage as well as in Cabell's Directories of Publishing Opportunities, U.S.A

NEW HIGH PERFORMANCE LOW POWER CARRY LOOK AHEAD ADDER BASED ON FINFET USING MTCMOS TECHNIQUE

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Abstract

In this paper we have designed a carry look adder circuit using CMOS technique, the low power and reduce Ground Bounce noise Carry look Ahead Adder based on FinFET has been proposed. A carry look ahead adder improves the speed by reducing the time required to solve carry bits. Carry-look ahead adder is a major functional block in arithmetic logic unit due to its high speed operation. The arithmetic logic unit has been widely used in microprocessor systems and mostly in processing modules of embedded systems. As the speed of the circuit increases the most important unwanted parameter exhibited by the circuits is ground bounce noise. In this chapter, we have proposed a modified Carry look Ahead Adder based on based on FinFET using multi-threshold CMOS technique .Here we use MTCMOS technique to evaluate standby leakage current, power and ground bounce noise. All the simulation in this paper has been carried out using Empyrean Aether" tool at 22nm technology at various voltage and temperatures.

Keywords:

FINFET technology;

Leakage current;

Leakage power;

Full adder;

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1. Introduction

In the past major challenges for VLSI designer to reduce the area of chip. One of the most important issues in VLSI design is standby leakage current with continuous down scaling in advanced CMOS technology. The leakage current contributes 49-64% in active power [12] [13] of digital circuit. It affects active power; standby power and performance of digital circuits because leakage strongly depends on process variations, increase in number of transistor and technology scaling. In this chapter, we have proposed new Carry look Ahead Adder with low power and reduce ground bounce noise based on conventional Carry look ahead adder. Carry look ahead adder .In recent years, various logic styles have been proposed to implement low power adder with reduced ground bounce noise. The aim of paper is to implement the full adder to reduce power and to increase speed [13] [14]. The main idea behind this chapter aims at design, analysis and improvement of power efficiency and ground bounce noise reduction of the Carry look Ahead adder at 180nm technology. The power reduction in any logic circuit cannot be achieved with trading off performance because it can make harder to reduce leakage during run time operation. We have seen several techniques proposed to reduce leakage power [15].

One of the most important technique Multithreshold (MTCMOS) also known as power gating technique is used for reducing the leakage current and standby leakage power when device is in idle mode and to improve the performance of device in active mode. The main idea behind this technique is to turnoff device in sleep mode and cut off leakage path provides a reduced leakage with improved power performance and reduction in ground bounce noise with proposed novel technique with improved stacking and power gating.

2. Carry Look Ahead Adder

A carry-Look ahead adder is a fast parallel adder as it reduces the propagation delay by more complex hardware; there are faster ways to add two binary numbers by using carry look ahead adders. They work by creating two signals P and G known to be **Carry Propagator and Carry Generator.** The carry propagator is propagated to the next level whereas the carry generator is used to generate the output carry, regardless of input carry. The block diagram of a Carry Look ahead Adder is shown here below the number of gate levels for the carry propagation can be found from the circuit of full adder.

The signal from input carry C_{in} to output carry Cout requires an AND gate and an OR gate.

Carry Look Ahead Adder Generate Two Signals P (Carry Propagator) and other G (Carry Generate)

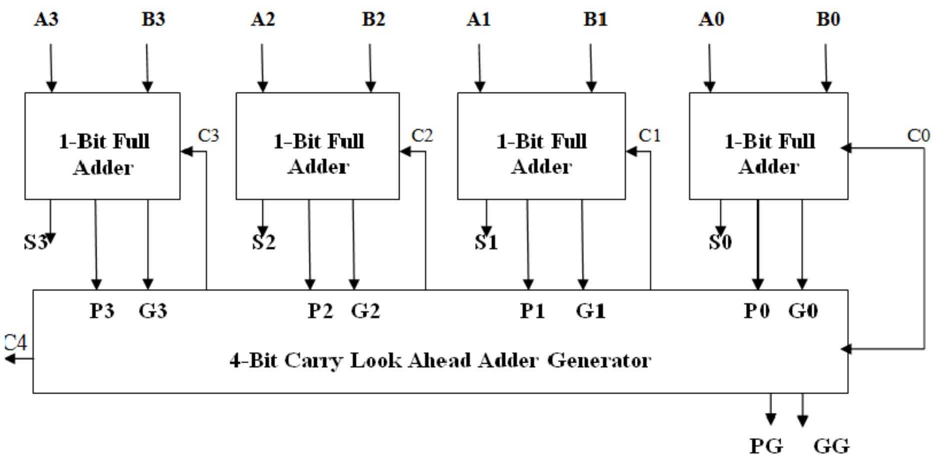


Figure 1 Carry Look Ahead Adder

The corresponding Boolean expressions are given here to construct a carry look ahead adder. In the carry-look ahead circuit we need to generate the two signals carry propagator (P) and carry generator (G).

$P_i = A_i \oplus B_i$……………………………………(1.1)

$G_i = A_i \cdot B_i$……………………………………….(1.2)

The output sum and carry can be expressed as

$Sum_i = P_i \oplus C_i$………………………………….(1.3)

$C_{i+1} = G_i + (P_i \cdot C_i)$……………………..............(1.4)

Having these we could design the circuit. We can now write the Boolean function for the carry output of each stage and substitute for each Ci its value from the previous equations:

$C_1 = G_0 + P_0 \cdot C_0$……………………………….(1.5)

$C_2 = G_1 + P_1 \cdot C_1 = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_0$…(1.6)

$C_3 = G_2 + P_2 \cdot C_2 = G_2\ P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_0$…………………(1.7)

$C_4 = G_3 + P_3 \cdot C_3 = G_3\ P_3 \cdot G_2\ P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 + P_3 \cdot P_2 \cdot P_1 \cdot P_0 \cdot C_0$..(1.8)

3. Component of Carry Look Ahead Adder

A. 28 T Full Adder Based on FinFET

One way to implement the full adder circuit is to take the logic equation (1.9) and equation (3.10) and translate them directly into complementary CMOS circuit. Some logic manipulations can help to reduce the transistor count. For instance, it is advantageous to share some logic between the sum and carry –generation sub circuits, as long as this does not slow down the carry generation, which is the most critical part as stated previously

The following is an example of such as reorganized equation set:

CARRY= A.B + B.Cin+ A.Cin……………………… (1.9)

SUM= A.B.Cin+ CARRY (A + B + Cin)……………. (1.10)

The equivalence with the original equations is easily verified. The corresponding adder design, using FinFET, is shown in figure 3.2 and the gate level implementation is shown in figure 2. It requires 28 transistors. In addition to consuming a large area, this circuit is slow.

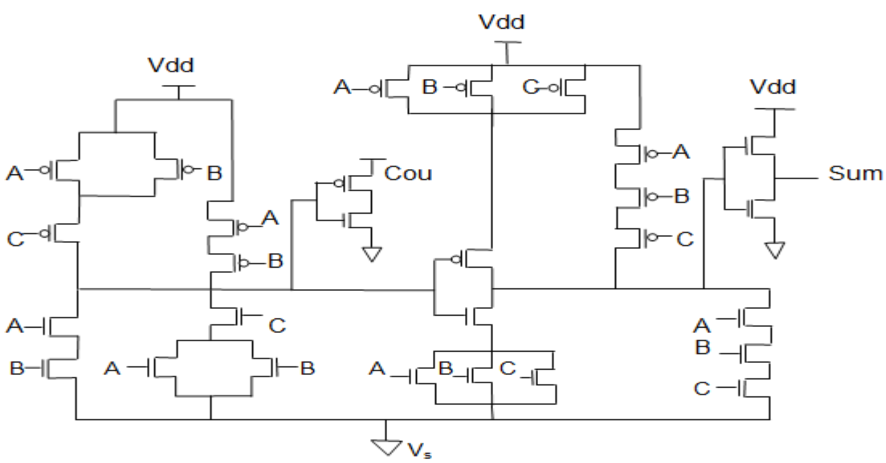


Figure 2 T Full Adder using FinFET

B. AND Gate:

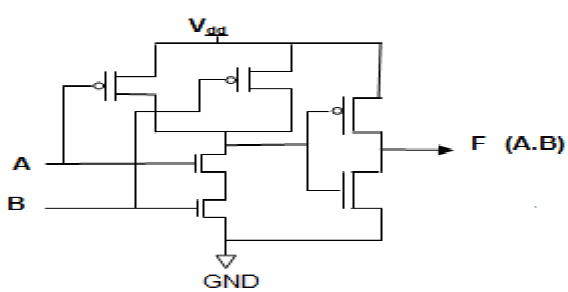


Figure.3 Conventional AND Gate

Conventional AND Gate is the combination of PMOS and NMOS. The circuit shows the realization of FinFET AND gate.

- When both a and b high, output is high.
- When either a or b is low, output, is low.

C. OR Gate:

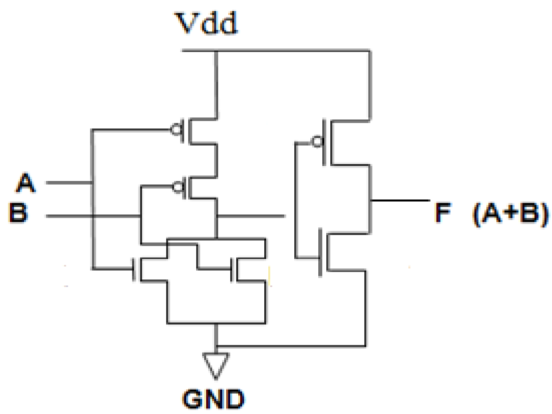


Figure.4Conventional OR Gate using FinFET

Conventional OR Gate is the combination of PMOS and NMOS. The circuit shows the realization of FinFET OR gate.

- When both A and B are Low, Output is Low.
- When either A or B high, Output is High

4. FinFET Technology

The following subsections include an introduction to the FinFET technology used in this research. A key benefit of using FinFETs is the ability to configure the back gates of the devices to provide greater speed or greater leakage control. The FINFET based transistors offers good tradeoff for power as well offering interesting delay. Fig 3.5,3.6 shows a simple structure of FinFET, it is a 4 terminal device comprising of source and drain connected by a channel, the channel is wrapped around by multiple gates, in this case we consider 2 gates namely forward and backward gates or front and back gates. A FinFET is like a FET, but the channel has been “turned on its edge” and made to stand up hence structure gave the name for the device as FinFET. FinFETs may be substituted into a former bulk-CMOS design by merely shorting the front- and back-gates together during device fabrication to allow only one gate connection per FinFET. The device parameters considerations are one of the important steps in developing a spice model and then simulating it. Commonly used FinFET simulation models available to the research community are the Predictive Technology Model (PTM) and BSIM-CMG/BSIM-IMG.[33-34]

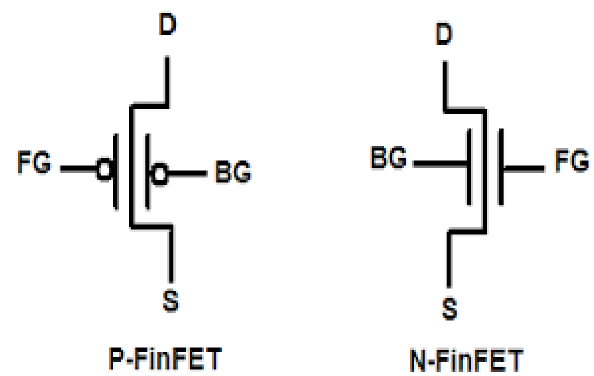


Figure .5 FinFET Symbol

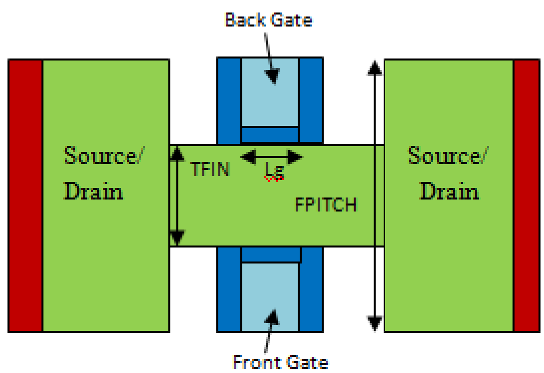


Figure 6 FinFET Structure

6. Modified Carry look Ahead Adder

We have proposed Carry look ahead adder cell based on FinFET with MTCMOS technique is implemented where a sleep transistor is added between actual ground rail and circuit ground. The device is turned off during sleep mode to cut-off the leakage path. [16] The comparison of active power, standby leakage power is done and it's observed that power is greatly reduced as we move from FinFET Carry look ahead adder cell to Modified Carry Look Ahead Adder.

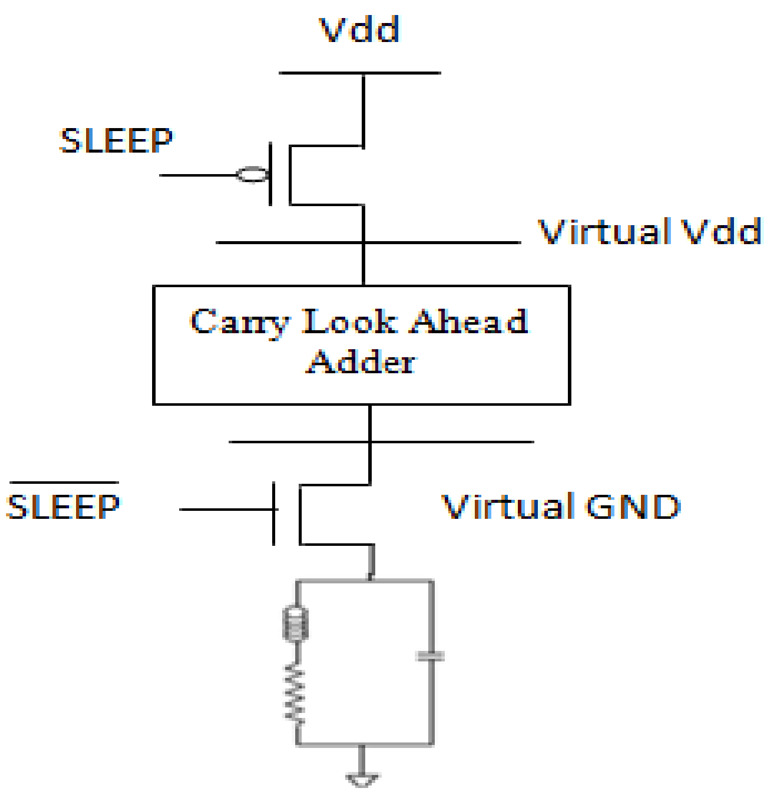


Figure 7 Modifed Carry look Ahead Adder using FinFET

7. Performance Analysis and Simulation Result

In this section, we have performed simulation of our conventional carry look ahead adder (FinFET) on Empyrean Aether Tool .

A. Active Power

At the time of operating the power is dissipated by the circuit is known as active power. Active power includes both static power and dynamic power of the circuit. Here we have calculated the active power of the circuit at various voltage and temperature. The Active power consumption of CMOS circuit [16] [17] is consumed by the following equation.

$P_{active} = P_{dynamic} + P_{static}$……………………………………(11)

$P_{avg} = P_{switching} + P_{short\text{-}circuit} + P_{leakag}$……………………….(12)

$P= (\alpha_{0\text{->}1}C_L\cdot V^2_{dd} \cdot f_{clk}) + (I_{sc}\cdot V_{dd}) + (I_{leakage}\cdot V_{dd}$………. (13)

The first term represents the switching component of power, where C_L is the load capacitance, f_{clk} is the clock frequency and $\alpha_{0\text{->}1}$is the probability that a power consuming transition occurs (the activity factor). The second term is due to the direct-path short circuit current, I_{sc}, which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground, finally, leakage current, $I_{leakage}$. As shown the table 3.6 in the case of modified Carry look ahead adder with stacking power gating active power is reduced compared to conventional Carry look ahead adder. 64 % at voltage 0.3 V and temperature 27 ^{o}C .

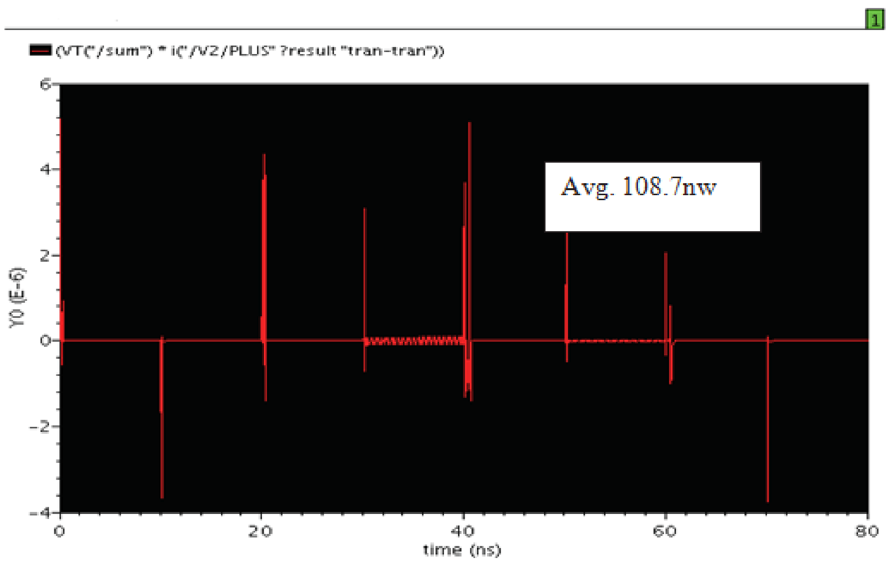


Figure .8(a) Active power of FinFET Carry Look Ahead Adder

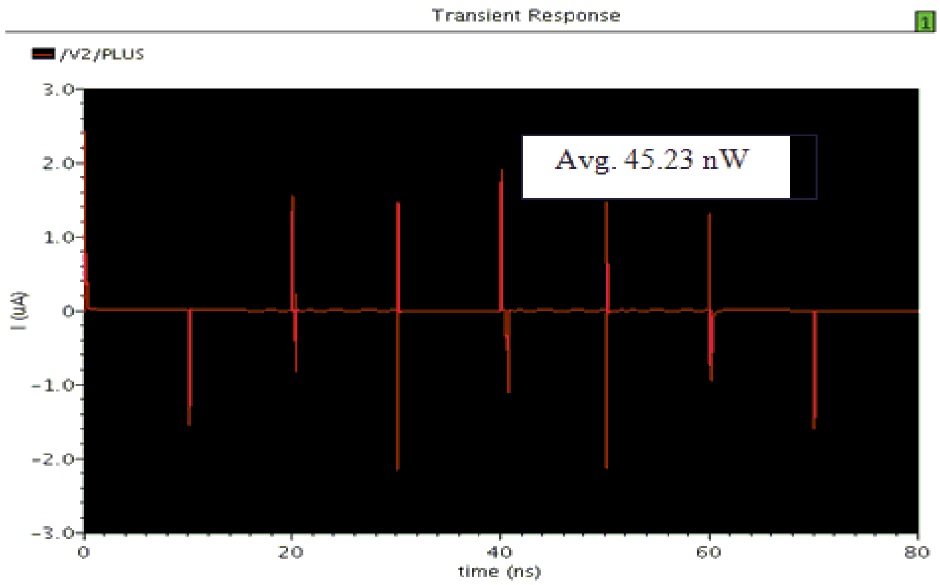


Figure8. (b) Active power of modified Carry Look Ahead Adder

Table 1.1: Active Power Dissipation of Carry look ahead Adder

Circuit	**Based on FinFET Carry Look Ahead Adder**		**Modified Carry Look Ahead Adder**	
Supply and Temperature	0.3 V	27 ^{o}C	0.3V	27 ^{o}C
Active power (nW)	108.7	108.7	45.23	45.23

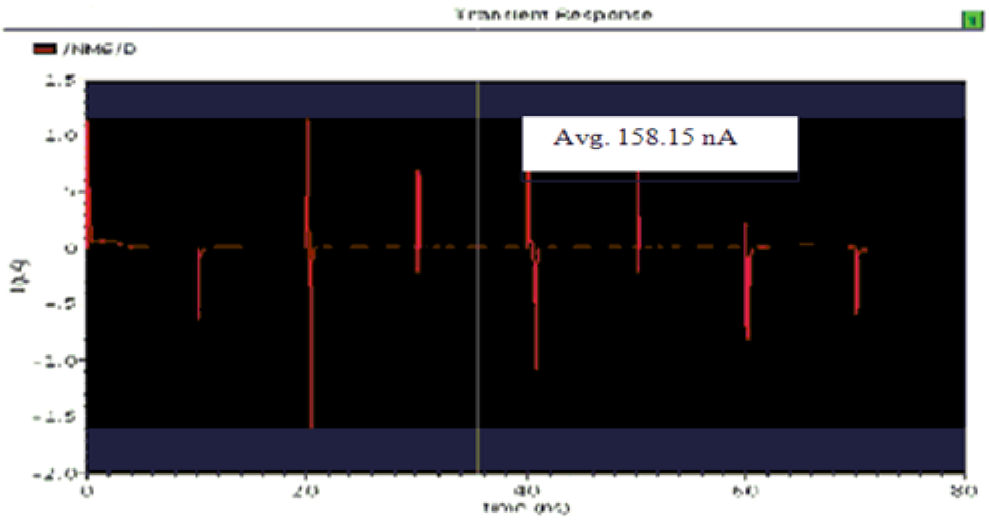
B.Standby Leakage Current

The stand by leakage is obtained when the circuit in idle mode. Here we connect the sleep transistor to the pull down network of Carry look ahead adder circuit and ground of the circuit. When we measuring the leakage current in MTCMOS Power gating then the both transistors are off [18]. The basic equation of stand by leakage is

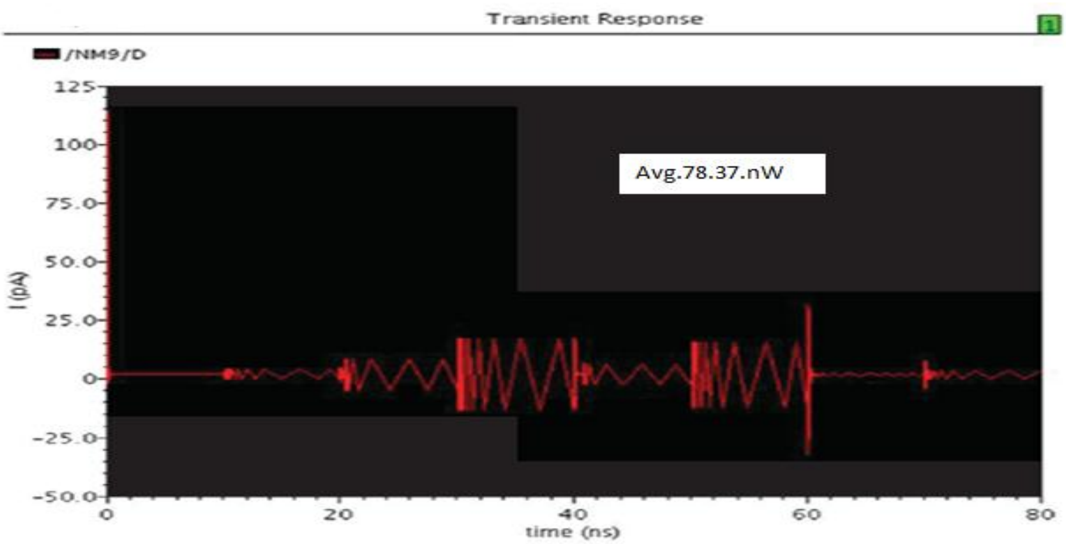
$L_{eak} = I_{sub} + I_{ox}$………………………. (13)

Where, I_{sub} = Sub threshold leakage current, I_{ox} = Gate oxide current.

Stand by leakage current is measured by at 0.3V and 27^{o}C. It is greatly reduced almost 49 % in modified Carry look ahead adder with MTCMOS power gating. The table 3.3 shows the leakage current at various voltages and various temperatures.



Figur.9 (a) Leakage current of conventional Carry Look Ahead Adder



Figuer.9 (b) Leakage current of modified Carry Look Ahead Adder

Table .2: (a) Standby Leakage current and leakage power due to various voltages

Volt. (V)	Leakage current		Leakage power	
	Based on FinFET Carry Look Ahead Adder ahead (nA)	**Modified Carry look ahead (pA)**	**Based on FinFET Carry Look Ahead Adder (mW)**	**Modified Carry look ahead (nW)**
0.3	91.80	46.53	29.23	100.89
0.4	158.15	78.37	72.76	113.15
0.5	230.50	156.20	143.59	133.23
0.6	281.70	218.48	290.89	143.69
0.7	343.50	399.18	345.50	223.50

Table .2 (B) Standby Leakage current and leakage power due to Various Temperatures

Temp. ^{0}C	Leakage current		Leakage power	
	Based on FinFET Carry Look Ahead Adder (nA)	**Modified Carry look ahead adder (pA)**	**Based on FinFET Carry Look Ahead Adder (m W)**	**Modified Carry look ahead adder (n W)**
27	157.18	78.36	70.76	113.19
47	160.70	139.20	76.80	253.69
67	162.70	248.50	79.68	387.70
87	165.80	317.30	80.55	455.36
107	193.50	423.80	90.70	573.43

C.Leakage Power

The stand by leakage power is measured at the time of idle mode. Here measured the leakage power when the sleep transistor is off. Basically the stand by leakage power is the product of the leakage current and supply voltage [8]. The basic equation of leakage power is

$P_{leak} = I_{leak} .V_{dd}$…………………………….(14)

The Table 2 (A) and Table 2 (B) shows leakage power is reduced in various voltages and temperatures after applying stacking power gating.

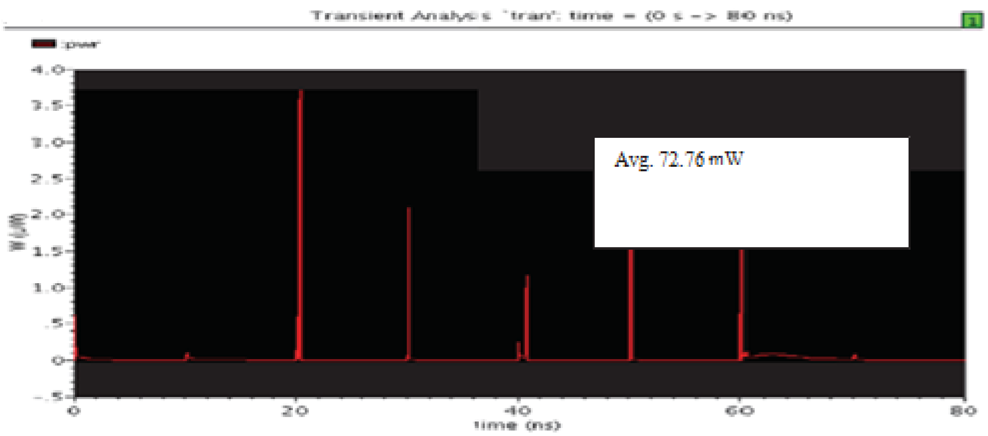


Figure . 10(a). Leakage power wave of conventional Carry look ahead adder

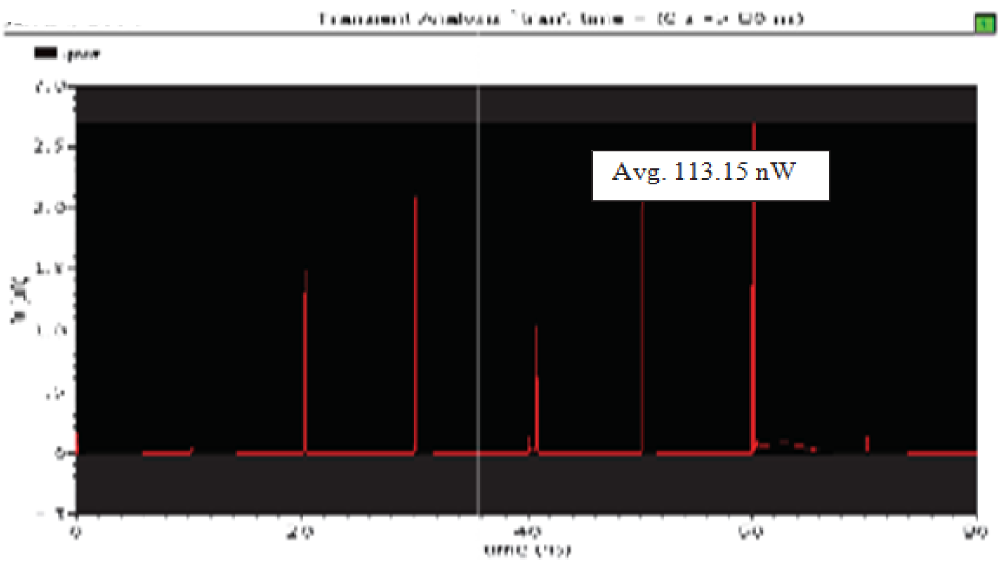


Figure 3.10(b). Leakage power wave form of modified carry look ahead adder

D.Ground Bounce Noise

During the active mode of the circuit an instant current pass from sleep transistor, which is saturation region and causes a sudden rush of the current. Elsewhere , because of self inductance of the off- chip bonding wires and parasitic inductance on chip power rails , result voltage function in the circuit depends on input/ output buffers and internal circuitry . The noise depends on the voltage. The ground bounce noise mode is in Fig (3.10). [17][18].

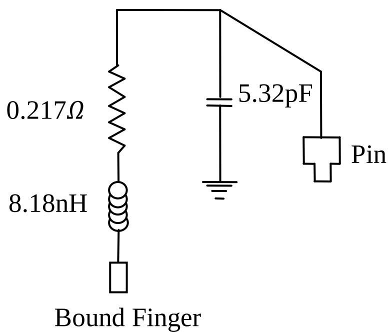


Figure 10: DIP-40 Package Pin Ground Bounce Noise mode

• Inductance L = 8.18 nH

• Resistance R = 0.217 Ω

• Capacitance C = 5.32 pF

The following wave form is showing ground bounce noise of conventional Carry look ahead Adder and modified Carry look ahead Adder.

Table 4: Ground Bounce Noise for Carry look ahead Adder

Voltage (V)	**Ground Bounce Noise (nV)**		**Temp. ^{0}C**	**Ground Bounce Noise (nV)**	
	Conv.	**Modified**		**Conv.**	**Modified**
0.3	65.30	18.34	27	63.63	41.85
0.4	63.80	40.75	47	66.42	33.26
0.5	96.40	64.41	67	69.33	44.31
0.6	125.90	89.23	87	74.66	53.32
0.7	157.14	115.90	107	80.40	63.92

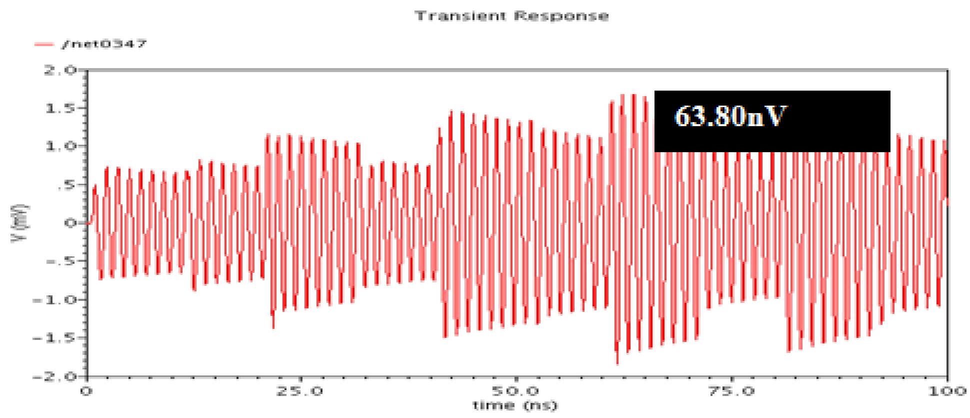


Figure 11 (a) Ground Bounce Noise of based on FinFETCarry look ahead Adder

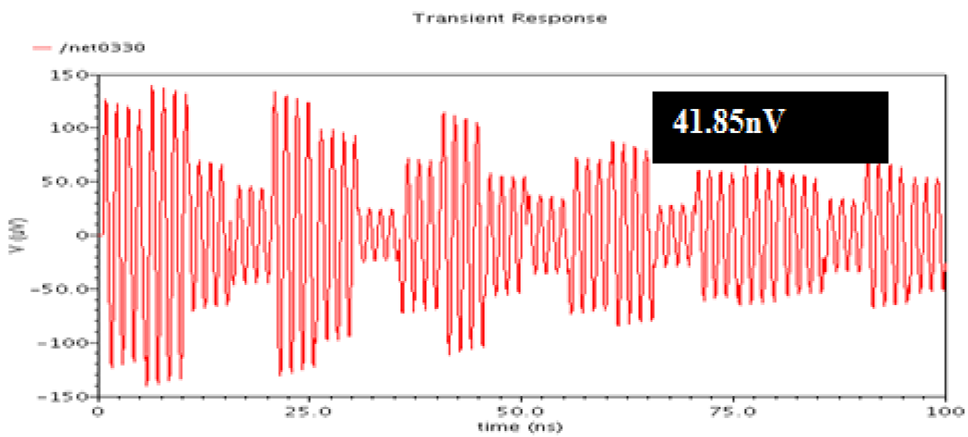


Figure 11(b) Ground Bounce Noise of modified Carry look ahead Adder

E. Ground Bounce Noise

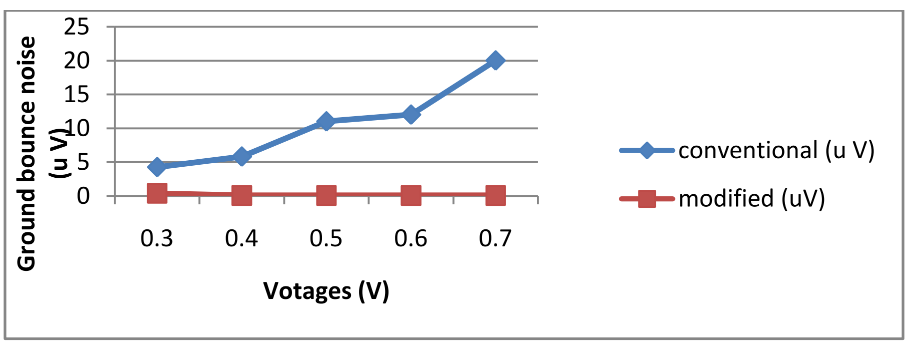


Figure 12 (a): Ground Bounce Noise graph of Carry look ahead Adder at various voltages

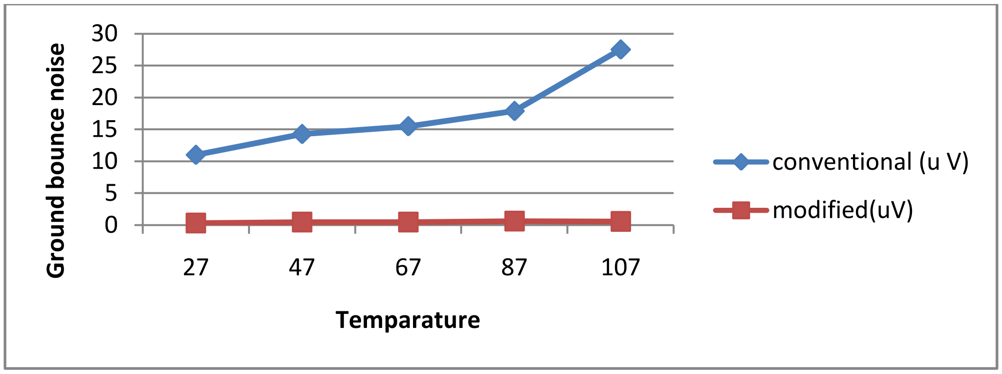


Figure 12 (b): Ground Bounce Noise graph of Carry look ahead Adder at various Temperatures

As shown in the table, the ground bounce noise is reduced up to 65 % in to various voltage and temperature

8. Conclusion

In this paper Carry look ahead adder cell based on FinFET with MTCMOS technique is implemented where a sleep transistor is added between actual ground rail and circuit ground. The device is turned off during sleep mode to cut-off the leakage path. The comparison of active power, standby leakage power is done and it's observed that power is greatly reduced as we move from based on FinFET Carry look ahead adder cell to Modified Carry Look Ahead Adder

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