New Results on Opto-Electronics

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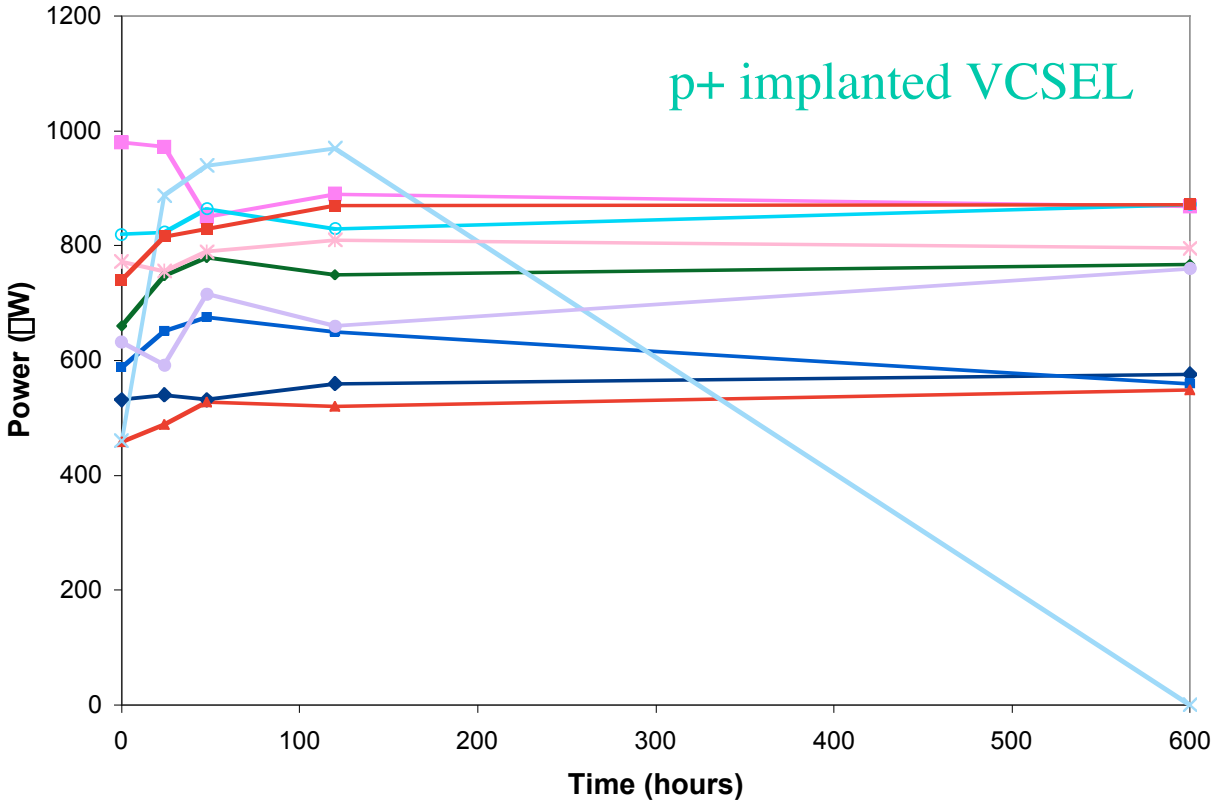
Outline

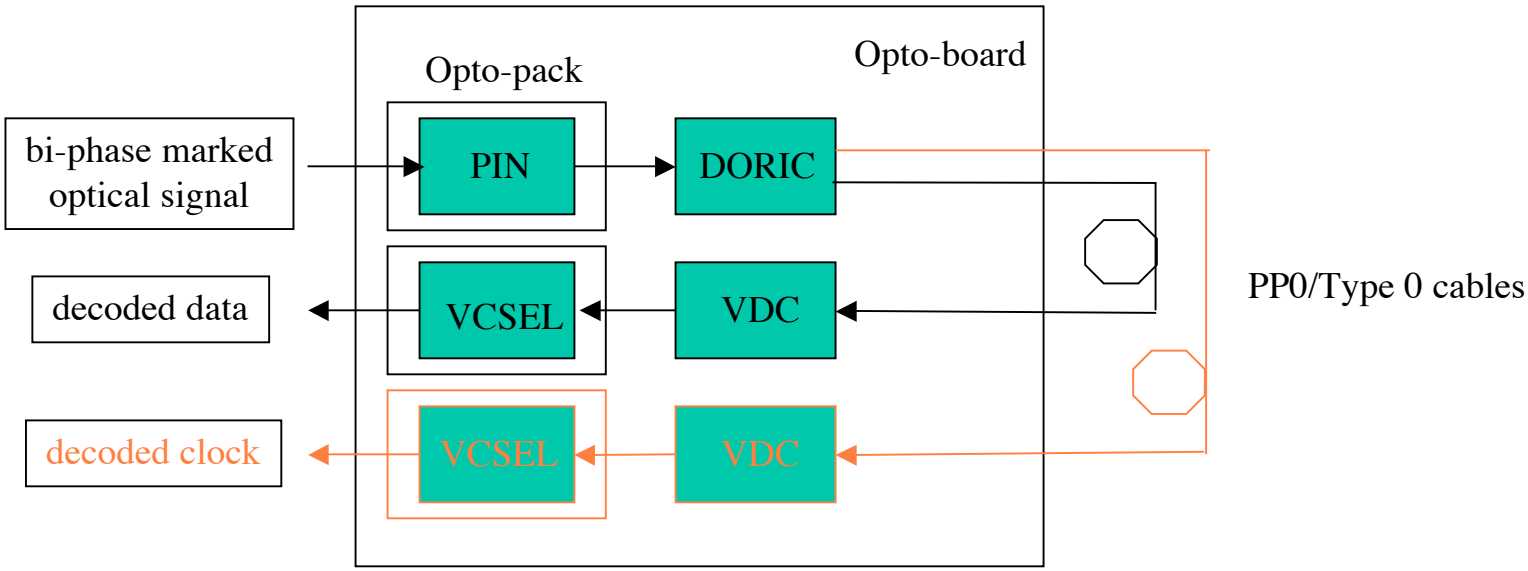
- Result on VCSEL Annealing
- Test with Type 0 cable
- Test with RX/TX
- Summary

Optical Power of Irradiated Opto-boards after Annealing



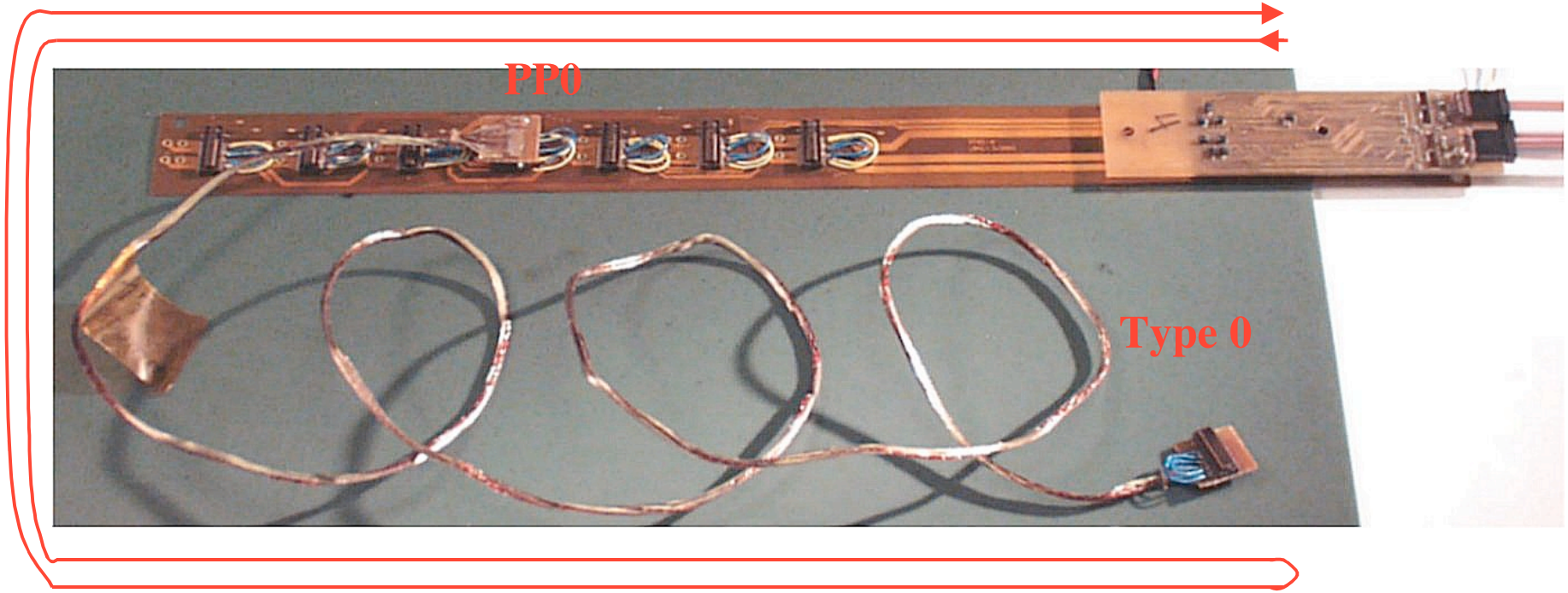
- limited annealing during irradiation partially recovers optical power lost
  - ⇨ all links have good optical power before annealing
- one VCSEL has large radiation damage
  - ⇨ large improvement with annealing
  - ⇨ dead after > 100 hours of annealing

Bit Error Testing with PP0/Type 0 Cables



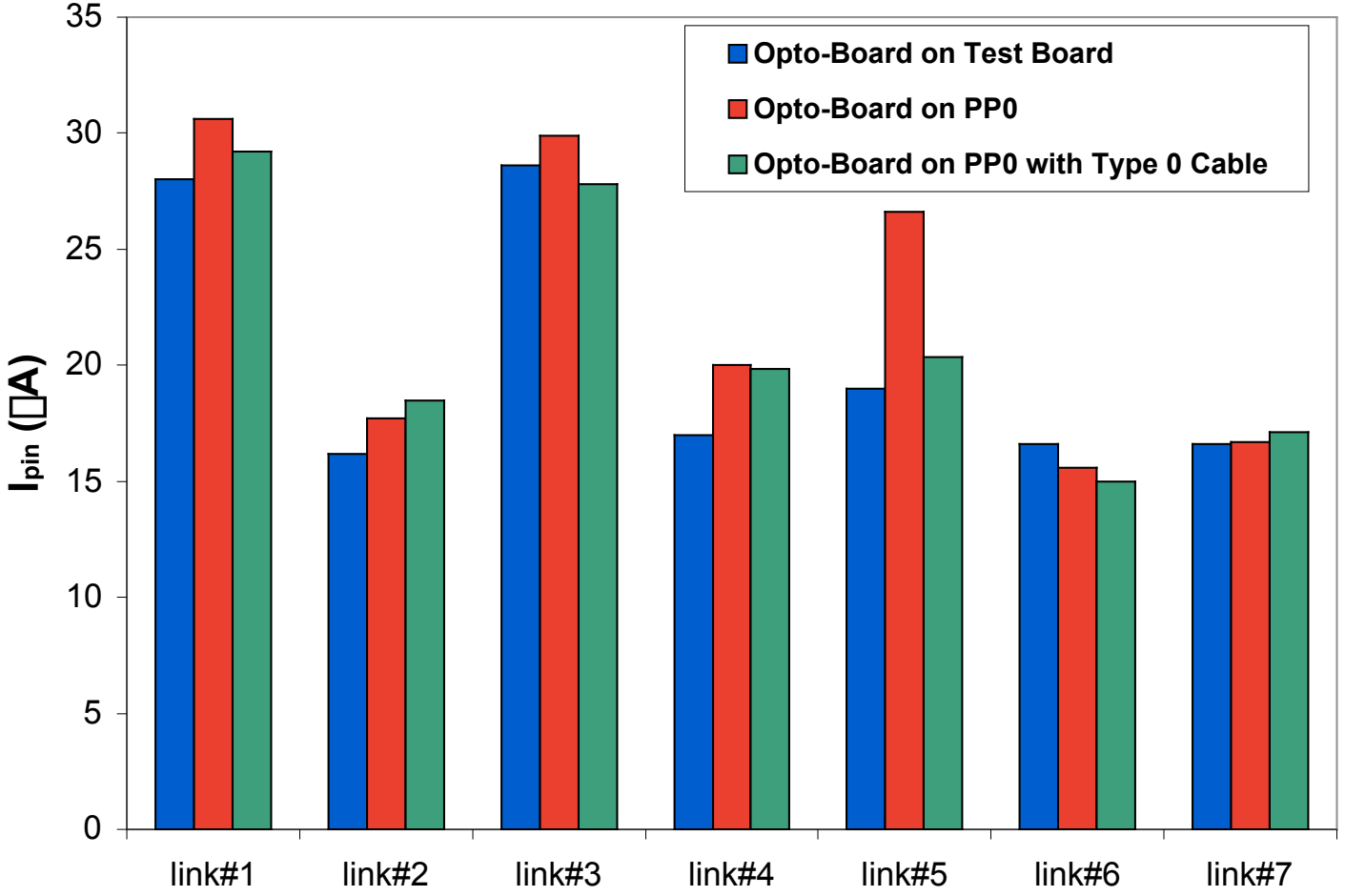
- compare original and decoded data
  - ⇨ measure minimum PIN current for no bit errors

Opto-Board with PP0 + Type 0 Cables



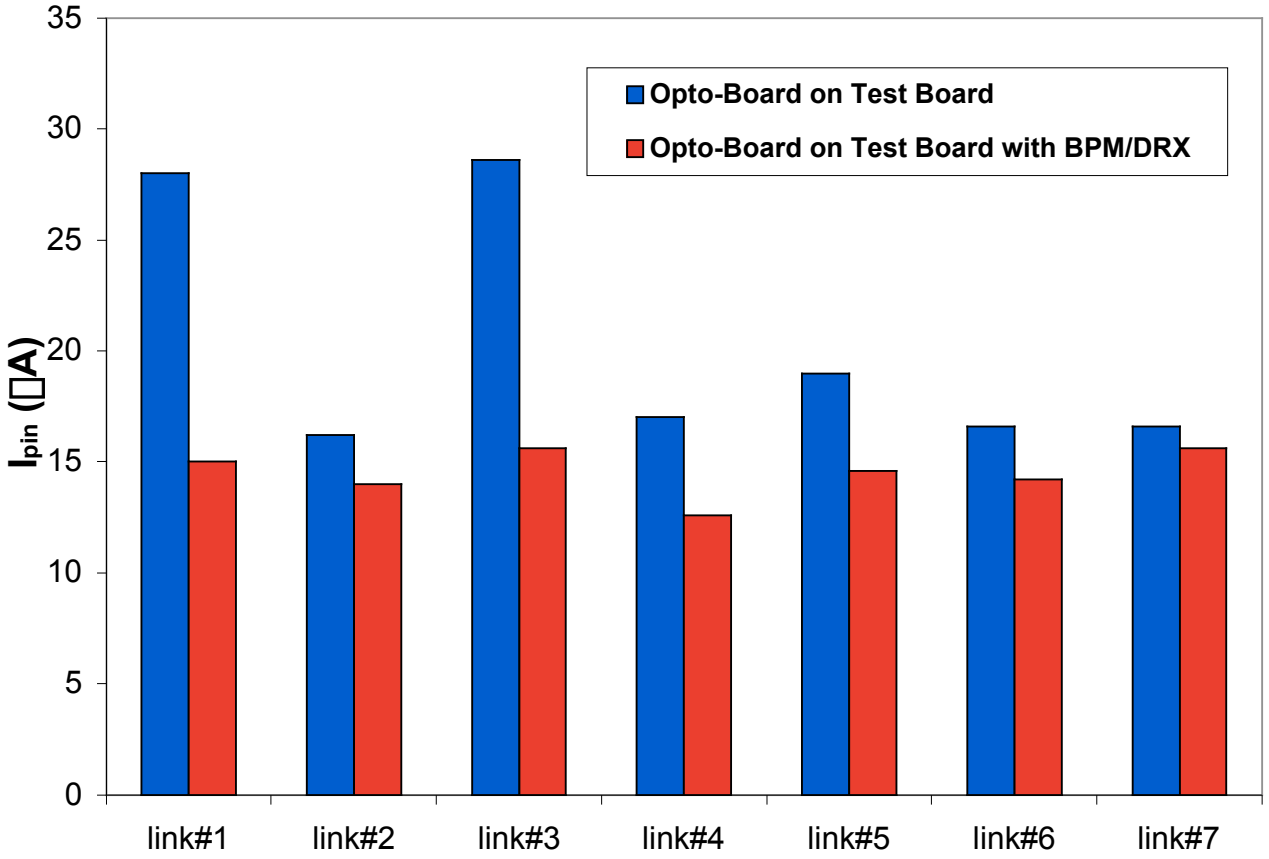
- data/clock from DORIC to VDC rerouted via PP0/Type 0 cables

PIN Current Thresholds with PP0/Type 0 Cables



- PIN current thresholds measured with other links running at 40 □A
- no increase in thresholds with PP0/Type 0 cables

PIN Current Thresholds with BPM/DRX



- thresholds for no bit error measured with other links running at 40 □A
- opto-board operates with lower thresholds with BPM/DRX

⇨ opto-board design is compatible with BPM/DRX

Summary

- one irradiated VCSEL failed during annealing
- no change in PIN current thresholds for no bit errors with PP0/Type 0 cable
- lower PIN current thresholds with BPM/DRX

⇨ opto-board is compatible with BPM/DRX

DORIC-I5e: Engineering Run

Presentation by Mike Zeoller

- **DORIC-I5e: March 2003, with MCC run**

3 metal layers (MPW runs), MZ top metal → 5 metals, LM top metal

⇨ improved power routing:
extra metals
LM sheet resistance is 61% that of MZ

⇨ reduced strays in input stage:
top metal shielding layer further separated from m1, m2

Minor improvements:

double # contacts in one preamp FET
⇨ max. $\langle I_{PIN} \rangle$: 2mA → 4mA
reduce area of input FET
⇨ reduce strays in input stage

Add power bypass capacitors (mimcaps?)