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***Abstract*—EV chargers with output power levels in the range of tens of kW are typically employing a front-end three-phase boost-type PFC rectifier stage for sinusoidal input current and DC-link voltage control, and a series-connected isolated DC/DC converter controlling the actual output/charging current or voltage. This paper explores a new synergetic control of both converter stages, which utilizes the DC/DC converter also for varying the DC-link voltage with six times the mains frequency, such that the currents of two mains phases are shaped sinusoidally. Accordingly, two bridge legs of the rectifier stage can remain clamped in 60 °-wide intervals of the mains cycle and the pulse width modulation (PWM) can be restricted to the phase carrying the lowest current, i.e., only one of the three bridge legs is operated with PWM, designated as 1/3-PWM. Furthermore, the DC-link voltage that is switched by the operating rectifier phase is kept to the minimum and the system features high efficiency and low EMI, but still maintains boost capability, i.e., the option of conventional PWM of all three rectifier bridge legs (thus denominated as 3/3-PWM), which is advantageous in case a wide input or output voltage range needs to be covered. The new control concept is derived starting from a conventional approach with constant DC-link voltage, and is verified by simulations for a three-level Vienna Rectifier front-end and two cascaded DC/DC modules supplied from the halves of the symmetrically partitioned DC-link voltage. First, the operating behavior of the system utilizing the proposed control is described analytically. Next, the performance improvement achievable with the proposed control scheme is comparatively evaluated for a 20 kW system designed for operation in a wide mains voltage range (260-530 V_{rms} line-to-line) and an extremely wide DC output / battery voltage range (150-750 V_{dc}), according to EV charging equipment supplier requirements of the State Grid Corp. of China. Finally, simulation results are presented which validate the operating principle of the proposed modulation and control scheme.**

I. INTRODUCTION

High-power EV battery chargers are supplied from the three-phase mains (e.g., 400 V_{rms} or 480 V_{rms} line-to-line) and are typically built using a boost-type PFC rectifier input stage ensuring sinusoidal mains current control and delivering a constant DC-link voltage 650-800 V_{dc} to a series-connected isolated DC/DC converter stage, which finally generates the required output voltage and/or battery charging current. In this way the operation and control of both converter stages is largely decoupled and both stages can be commissioned separately.

A well-known and widely used realization of the aforementioned concept is depicted in **Fig. 1(a)** [1]. The system employs a three-level Vienna Rectifier (VR) input stage, which features low magnetics volume and provides a symmetrically partitioned (constant) DC-link voltage (cf., **Fig. 2(a)**), such that the DC/DC converter stage can be split into two cascaded converter modules M_{xy} and M_{yz}. This approach allows to benefit from 600 V semiconductor and converter technologies known, e.g., from high-power datacenter power supply modules. Furthermore, a series/parallel rearrangement of the outputs of M_{xy} and M_{yz} could be used to cover the extremely wide output voltage range required for future EV chargers (150-750 V_{dc}, cf., **Fig. 1(b)** [2]).

However, considering that the voltage control function is implemented twice, i.e., for the output of the PFC rectifier stage and for the output of the DC/DC converter supplying the charging current, the question arises if a synergy of the

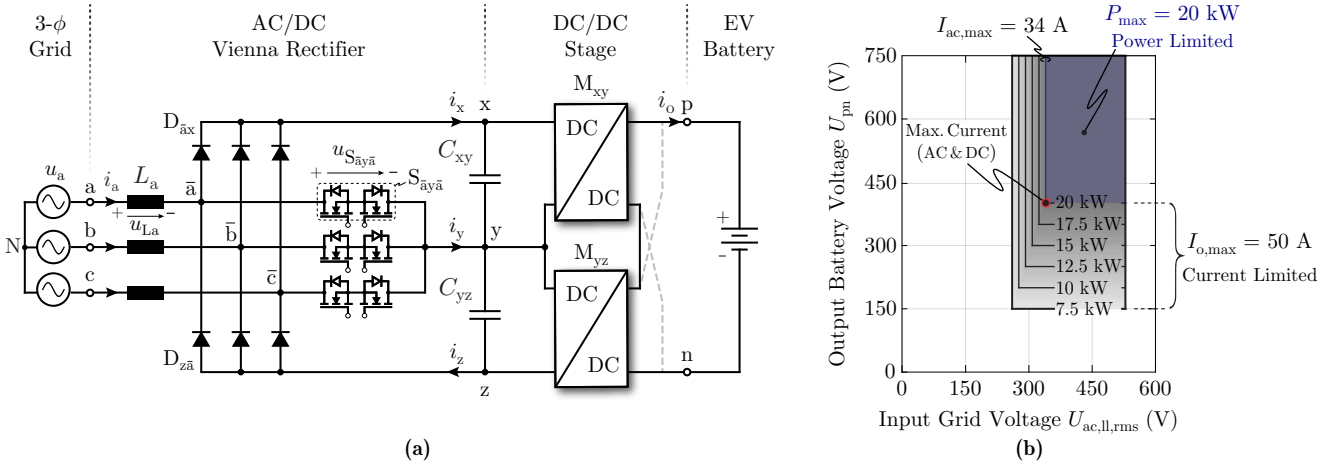

Fig. 1. **(a)** Circuit diagram of a typical three-phase/level PFC rectifier mains interface (VIENNA Rectifier) with an isolated DC/DC output stage, comprising individual converter modules, which can either be connected in series- or parallel-configuration at the output. Optionally, an additional active series/parallel rearrangement of the DC/DC converter modules can be implemented to optimally adapt the conversion ratio between DC-link and output voltage, i.e., mitigating the requirements on voltage and current capabilities of the DC/DC converter modules. **(b)** Wide-input and wide-output voltage range specification for the 20 kW EV charger at hand, where for a nominal line-to-line voltage of $U_{ac,ll,rms}$ = 400 V, the converter has to be able to provide full output current (I_o = 50 A) for output DC voltages below U_{pn} = 400 V, and thereafter has to be capable of delivering full power (P_o = 20 kW) until reaching the maximum output DC voltage U_{pn} = 750 V.

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control of both stages could be found, which would allow to reduce the overall realization effort and costs.

An according approach, which limits the functionality of the input stage to pure rectifier and/or mains frequency commutated three-phase unfolder operation and generates two cascaded time varying DC-link voltages which are supplying two cascaded DC/DC converters responsible for input current shaping and output voltage control, has been analyzed in [3,4] (based on [5,6]). Characteristic waveforms are shown in **Fig. 2(b)**. However, the cascaded voltages u_{xy} and u_{yz} are widely varying and differing, which results in relatively high voltage stresses on the DC/DC converter and unfolder power semiconductors. E.g., for a 480 V_{rms} + 10 % line-to-line three-phase mains the maximum blocking voltage reaches $\frac{\sqrt{3}}{2} \cdot \hat{U}_{ac,ll} = 647$ V, i.e., 600 V semiconductors cannot be employed any more. Furthermore, the boost functionality of the rectifier stage is not any more available, as the boost inductors at the input side are omitted for this concept [3,4]. Accordingly, DC/DC converter modules with extremely wide voltage transfer ratio range are required, which results in overdesign and impairs efficiency and power density. Furthermore, each DC/DC converter module has to be designed to temporarily operate at full power, and a limited input current quality has to be accepted, as no direct mains current control is performed.

Therefore, this paper proposes an alternative concept of synergetic control of the rectifier and DC/DC converter stage, where the basic power circuit structure of **Fig. 1(a)** is fully kept, and cascaded DC-link voltages of equal value are generated. Furthermore, the current control of one mains phase, i.e., of the phase carrying the lowest current is maintained by pulse width modulation (PWM) of the corresponding bridge leg within 60 °-intervals around the current zero crossings [2,7]–[11]. The currents of the two other phases, which are clamped to the positive and negative DC bus through the rectifier diodes (the associated bidirectional switches remain in the off-state), are controlled by the DC/DC converter modules M_{xy} and M_{yz} resulting in a six-pulse (six times mains frequency) DC-link voltage shape (cf., **Fig. 2(c)**). Consequently, this synergetic control scheme is designated as 1/3-PWM, since only one bridge leg of the three-phase VR front-end is pulse width modulated. In addition, the DC/DC converter modules are ensuring an equal splitting of the total DC-link voltage such that the maximum voltage on the semiconductors (for a 480 V_{rms} + 10 % mains) is only $0.5 \cdot \hat{U}_{ac,ll} = 374$ V, allowing the use of 600 V semiconductor technology which can be implemented by an anti-series configuration of two discrete switches, or by recently introduced monolithic bidirectional GaN HEMTs [12,13].

As the boost inductors remain on the AC-side, the above-described mode of operation, which directly connects always the highest AC-side line-to-line voltage (and/or sum of the two lower value line-to-line voltages) in 60 °-wide intervals to the DC-link, can also be changed into a partial-boost mode or a full-boost mode, where all three rectifier bridge legs are operated with PWM, thus denominated as 3/3-PWM, in case a high output voltage needs to be generated or a low mains voltage is present. This allows to reduce the voltage conversion ratio requirement of the

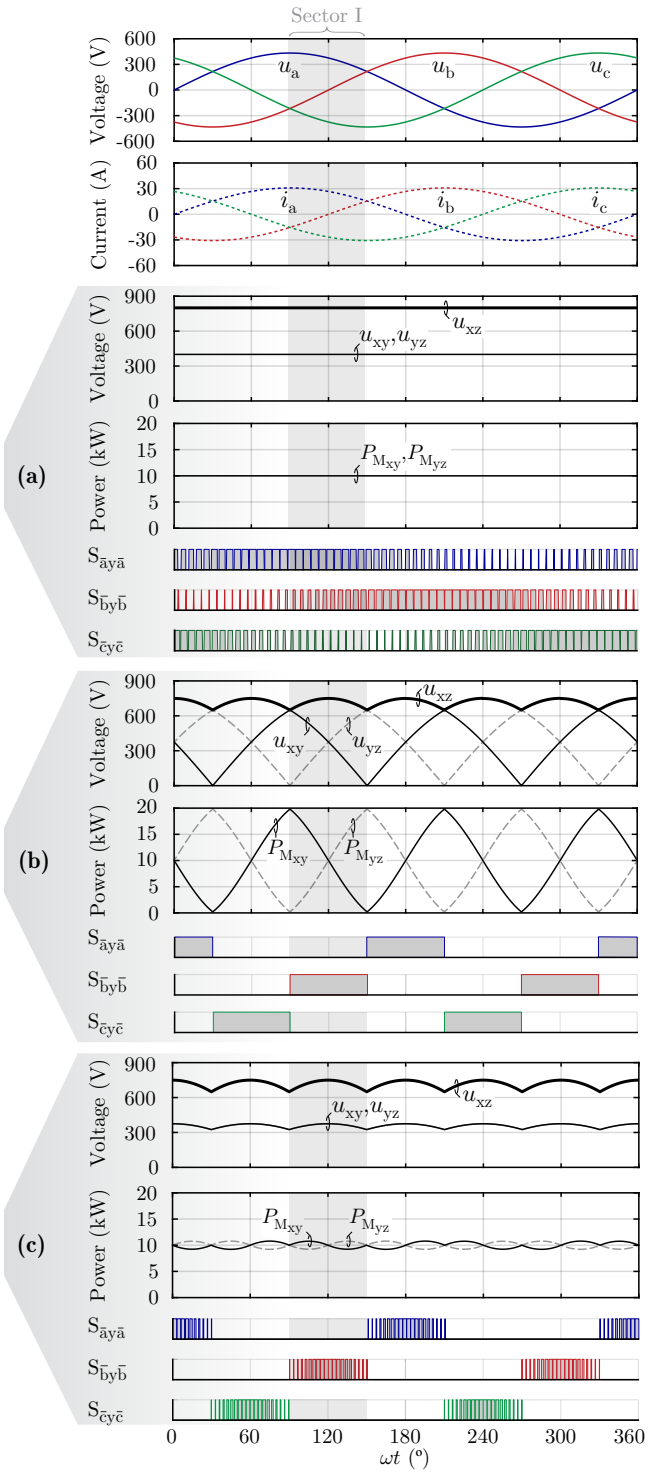

Fig. 2. Characteristic waveforms of the three-phase/level PFC rectifier and isolated DC/DC output stage (cf., **Fig. 1(a)**) presented for the highest specified input voltage ($U_{ac,ll,max} = 530$ V) and operation at 20 kW for the following control and modulation schemes: **(a)** conventional approach of boosting the input mains voltage to a DC-link voltage of 800 V, by pulse width modulating all three rectifier stage bridge legs (3/3-PWM) and subsequent decoupled equal-power operation of the DC/DC modules, **(b)** approach presented in [3]–[6] where the three-phase/level front-end is operated as a three-phase unfolder and the isolated DC/DC modules are controlled to behave as current sources generating piecewise sinusoidal currents that are defining the mains current, and **(c)** proposed synergetic control scheme that combines 1/3-PWM (pulse width modulation of one of the phases [2,7]–[11]) with six-pulse control of the DC-link voltages through the DC/DC modules, ensuring sinusoidal input currents and equal voltage sharing of the DC-link capacitors, besides a controlled DC output voltage.

DC/DC converter modules and/or results in higher efficiency and power density. Further details of the operation of the system, which is denominated as *SynC-VR-i* (*Synergetically Controlled Vienna Rectifier* with *i*solated DC/DC converter output stage), are given in the following Sections.

The paper is organized as follows: **Section II** discusses the operation principle of the SynC-VR-i, and **Section III** describes the corresponding control structure. **Section IV** shows simulation results of the new control method proving its correct functionality, while **Section V** presents an analytic and quantitative comparison of the semiconductor stresses. Finally, the main conclusions are presented in **Section VI**.

II. Operation Principle of the SynC-VR-i

Due to the three line supply of the three-phase PFC rectifier stage (cf., **Fig. 1(a)**), it is sufficient to independently control only two phase currents, e.g., i_a and i_c for the following considerations, as the third current (e.g., i_b) is directly defined by Kirchhoff's Current Law (KCL), i.e., $i_b = -(i_a + i_c)$. For controlling two phase currents two degrees of freedom are required, i.e., two line-to-line voltages of the rectifier stage, $u_{\overline{ab}}$ and $u_{\overline{bc}}$, have to be generated accordingly at any point in time, as this, together with the given mains voltage (u_{ab} and u_{bc}) and the KCL, fully determines the voltages u_{L_a}, u_{L_b} and u_{L_c} applied across the input inductors L_a, L_b and L_c, which finally determine the input currents.

Given that the mains frequency components of the inductor voltages u_{L_a}, u_{L_b} and u_{L_c} are small (operation at high switching frequency resulting in a low inductance value), the local average values $\overline{u}_{\overline{a}}$, $\overline{u}_{\overline{b}}$ and $\overline{u}_{\overline{c}}$ of $u_{\overline{a}}$, $u_{\overline{b}}$ and $u_{\overline{c}}$, are almost equal to the grid voltages u_a, u_b and u_c. Consequently, assuming input currents which are in phase with the mains phase voltages, the conduction state of the diode bridge legs of phases *a* and *c* only depends on the sign of the actual mains phase voltages u_a and u_c. Therefore, considering, e.g., *Sector I* in **Fig. 2**, the upper diode of phase *a*, showing the most positive phase voltage (u_a) and the lower diode of phase *c*, showing the most negative phase voltage (u_c), are always conducting. Accordingly, the total DC-link voltage $u_{xz} = \overline{u}_{\overline{ab}} + \overline{u}_{\overline{bc}}$ always follows the largest line-to-line voltage, i.e., $u_{xz} = \overline{u}_{\overline{ac}} \approx u_{ac}$, and exhibits a six-pulse shape as shown in **Fig. 2(c)**.

All in all, the DC-link voltage u_{xz} ($= u_{\overline{ac}}$ in *Sector I*) has to be adjusted with respect to the actual maximum line-to-line voltage u_{ac}. For the proposed synergetic control method, the DC-link voltage is controlled by properly defining the power consumption of the subsequent DC/DC converter modules M_{xy} and M_{yz}.

However, only controlling the DC-link voltage would mean that only in the most positive and most negative phase equal currents with opposite sign would be flowing and, the current in phase *b* (*Sector I*) would be zero, i.e., no sinusoidal set of three phase currents would result. Hence, a current has to be impressed in the middle phase, which in each sector is proportional to the middle phase voltage, in order to obtain three sinusoidal phase currents. As shown in **Fig. 3(b)**, this current always equals the minimum absolute phase current, which is symmetric around zero, and features a quasi triangular shape for PFC operation, i.e., within one 60 °-wide voltage sector the current is positive for 30 ° and negative for the other 30 °. Depending on the momentary voltage sector, this current can be controlled by always pulse width modulating the bidirectional switch $S_{\overline{a}y\overline{a}}$, $S_{\overline{b}y\overline{b}}$ or $S_{\overline{c}y\overline{c}}$ corresponding to the middle phase voltage, i.e., $S_{\overline{b}y\overline{b}}$ for *Sector I*.

During the turn-on phase of the pulse width modulated bidirectional switch, the switch node of the corresponding rectifier stage bridge leg is directly connected to the DC-link midpoint *y*, regardless of the current direction in the middle phase. However, during the turn-off phase, the resulting bridge leg voltage actually depends on the current direction, hence the possible voltage levels of the bridge leg of the middle phase, $u_{\overline{b}}$ for *Sector I*, are limited by the current direction in the inductor L_b. For $i_b > 0$, the switch node $\overline{b}$ can only be actively connected to the DC-link midpoint by closing $S_{\overline{b}y\overline{b}}$, and when $S_{\overline{b}y\overline{b}}$ is opened, the current commutates to the upper diode $D_{\overline{b}x}$. Consequently, since $\overline{c}$ is connected to the negative DC-link rail *z*, the voltage $u_{\overline{bc}}$ equals $u_{xz}/2$ when $S_{\overline{b}y\overline{b}}$ is closed and u_{xz} when $S_{\overline{b}y\overline{b}}$ is open, assuming that the DC-link voltage is equally split, i.e., $u_{xy} = u_{yz} = u_{xz}/2$. Accordingly, since the duty cycle of $S_{\overline{b}y\overline{b}}$ is limited between 0 and 1, the local average of the line-to-line voltage $u_{\overline{bc}}$ that can be generated for positive i_b is constrained between $u_{xz}/2$ ($= u_{\overline{ac}}/2$) and u_{xz} ($= u_{\overline{ac}}$). Hence, in order to be able to control the phase current in the middle phase (i_b) to a positive value, the local average of the line-to-line voltage u_{bc} must be larger or equal to $u_{\overline{ac}}/2$.

In analogy, for negative currents in phase *b* in *Sector I*, $\overline{b}$ can either be actively connected to the DC-link midpoint, or assumes the voltage of the negative rail *z* of the DC-link through the diode $D_{z\overline{b}}$. Given again the limitation of the duty cycle of $S_{\overline{b}y\overline{b}}$ between 0 and 1, the local average of the line-to-line voltage $u_{\overline{bc}}$ that can be generated for negative currents in this case is constrained between $u_{xz}/2$ ($= u_{\overline{ac}}/2$) and 0, and hence, the local average of u_{bc} must be smaller or equal than $u_{\overline{ac}}/2$. Consequently, for the described modulation scheme, the control is limited to pure PFC rectifier operation where u_{bc} actually equals $u_{\overline{ac}}/2$.

Based on these considerations, now the duty cycle of $S_{\overline{b}y\overline{b}}$ can be easily calculated for steady-state operation, which means that within one switching period in average no voltage is applied to the inductors, i.e., $u_{bc} = u_{\overline{bc}}$ for *Sector I*. Assuming a local averaging, the voltage $u_{\overline{bc}}$ can be written for positive currents i_b as $u_{\overline{bc}} = d_{S_{\overline{b}y\overline{b}}} \cdot u_{xz}/2 + (1 - d_{S_{\overline{b}y\overline{b}}}) \cdot u_{xz}$, while for negative currents it is just given as $u_{\overline{bc}} = d_{S_{\overline{b}y\overline{b}}} \cdot u_{xz}/2$. Furthermore, considering that in *Sector I* the DC-link voltage u_{xz} equals the line-to-line voltage u_{ac}, yields that the duty cycles of $S_{\overline{b}y\overline{b}}$ are

$$\begin{cases} d_{S_{\overline{b}y\overline{b}}} = 2 \cdot \dfrac{u_{\overline{bc}}}{u_{\overline{ac}}} & \text{for} \quad i_b < 0 \\ d_{S_{\overline{b}y\overline{b}}} = 2 \cdot \left(1 - \dfrac{u_{\overline{bc}}}{u_{\overline{ac}}}\right) & \text{for} \quad i_b > 0 \ . \end{cases} \tag{1}$$

In a next step, the low frequency current component that flows through the bidirectional switches to the DC-link midpoint i_y can be determined by multiplying the phase

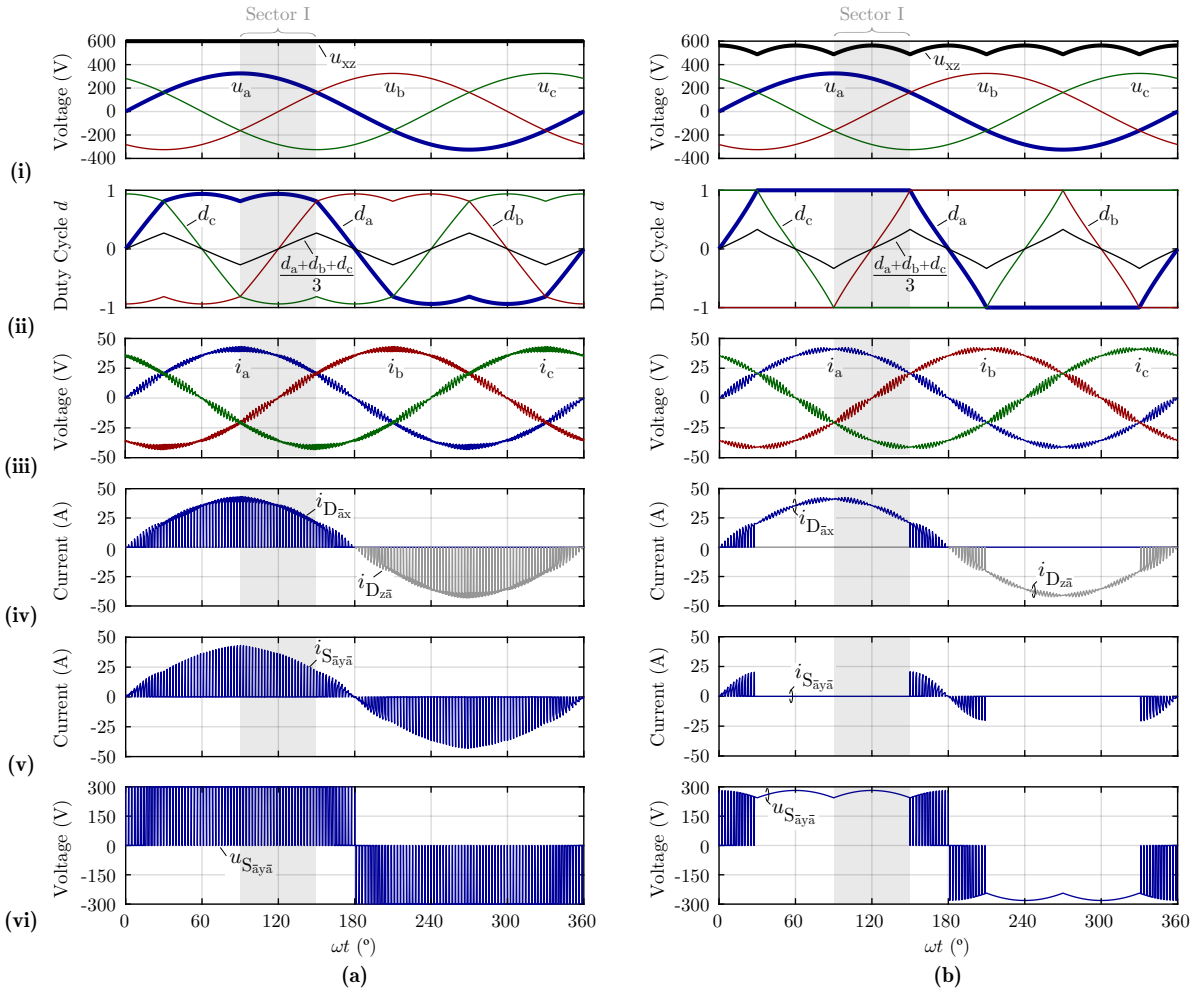

Fig. 3. Characteristic waveforms for **(a)** full-boost mode with 3/3-PWM, where all three bridge legs are pulse width modulated, and **(b)** 1/3-PWM. From top to bottom: **(i)** input grid voltages u_i for $i = \{\text{a,b,c}\}$ together with the DC-link voltage u_{xz}, **(ii)** phase-leg duty cycles d_i and common mode (zero sequence) duty cycle (where d_i = 1 implies that the diode $D_{\bar{i}\text{x}}$ is clamping the phase-leg to the positive rail x of the DC-link, and d_i = -1 implies that the diode $D_{z\bar{i}}$ is clamping the phase-leg i to the negative rail z of the DC-link), **(iii)** mains (input) phase currents $i_{\{\text{a,b,c}\}}$, **(iv)** currents of the VR diodes for phase a, $i_{\text{D}\bar{\text{a}}\text{x}}$ and $i_{\text{D}z\bar{\text{a}}}$, **(v)** current through the switch $\text{S}_{\bar{\text{a}}\text{y}\bar{\text{a}}}$, and **(vi)** voltage $u_{\text{S}_{\bar{\text{a}}\text{y}\bar{\text{a}}}}$ across the switch $\text{S}_{\bar{\text{a}}\text{y}\bar{\text{a}}}$. For illustration purpose, the waveforms are calculated for a low switching frequency of 7.5 kHz and an input inductance of $L_{\{\text{a,b,c}\}} = 700\,\mu\text{H}$.

current in the middle phase (i_b) with the duty cycle of the bidirectional switches, e.g., $i_\text{y} = d_{\text{S}_{\bar{\text{b}}\text{y}\bar{\text{b}}}} \cdot i_\text{b}$ in the case of *Sector I*. Since the duty cycle is always smaller than one, and the current in the middle phase is already low, the product of these two values leads to an even smaller current i_y, especially since when i_b is maximum, the duty cycle $d_{\text{S}_{\bar{\text{b}}\text{y}\bar{\text{b}}}}$ is zero (cf., **Fig. 3(b)**). This current i_y multiplied by half the DC-link voltage actually determines the power mismatch drawn by the two series-connected DC/DC modules, which due to the small value of i_y, is very low (a maximum of $\pm$800 W occurs for each converter module for 20 kW operation). Therefore both DC/DC converter modules are processing half the power $\pm$8 % and can be designed accordingly, as opposed to [3,4], where the DC/DC converter modules have to alternatingly process the full output power.

III. Control Strategy of the SynC-VR-I

A detailed schematic of the cascaded control consisting of three essential functional blocks is shown in **Fig. 4**. The first main block is the output current controller, which shows the lowest bandwidth of all controllers, and sets the output current reference I_o^*. By measuring the output voltage U_pn, the required power to be drawn from the mains is calculated. From this, the converter's input conductance G^* is determined, which together with the measured input voltages defines the reference phase currents that are compared with the measured phase currents. The input current control errors are then fed to the input current controller, which outputs the needed voltages across the input inductors, $u_{\text{L}_\text{a}}^*$, $u_{\text{L}_\text{b}}^*$ and $u_{\text{L}_\text{c}}^*$ (note that these are locally averaged values), and together with the mains phase voltages sets a reference for each AC terminal voltage $u_{\bar{\text{a}}}^*$, $u_{\bar{\text{b}}}^*$ and $u_{\bar{\text{c}}}^*$ of the rectifier stage. Based on these reference values, on the one hand, the actual voltage sector, and on the other hand, the line-to-line voltages in between the rectifier bridge AC terminals, $u_{\bar{\text{a}}\bar{\text{b}}}^*$, $u_{\bar{\text{b}}\bar{\text{c}}}^*$ and $u_{\bar{\text{c}}\bar{\text{a}}}^*$, are derived in order to calculate the duty cycles of the bidirectional switches (cf., (1)). In addition, the maximum line-to-line voltage, $u_{\text{ll,max}}^* = u_{\text{max}}^* - u_{\text{min}}^*$, directly determines the DC-link voltage reference for 1/3-PWM operation. This reference voltage, however, first has to be compared with the minimum DC-link voltage setpoint $U_{\text{xz,min}}^*$, which has to be larger than the required output

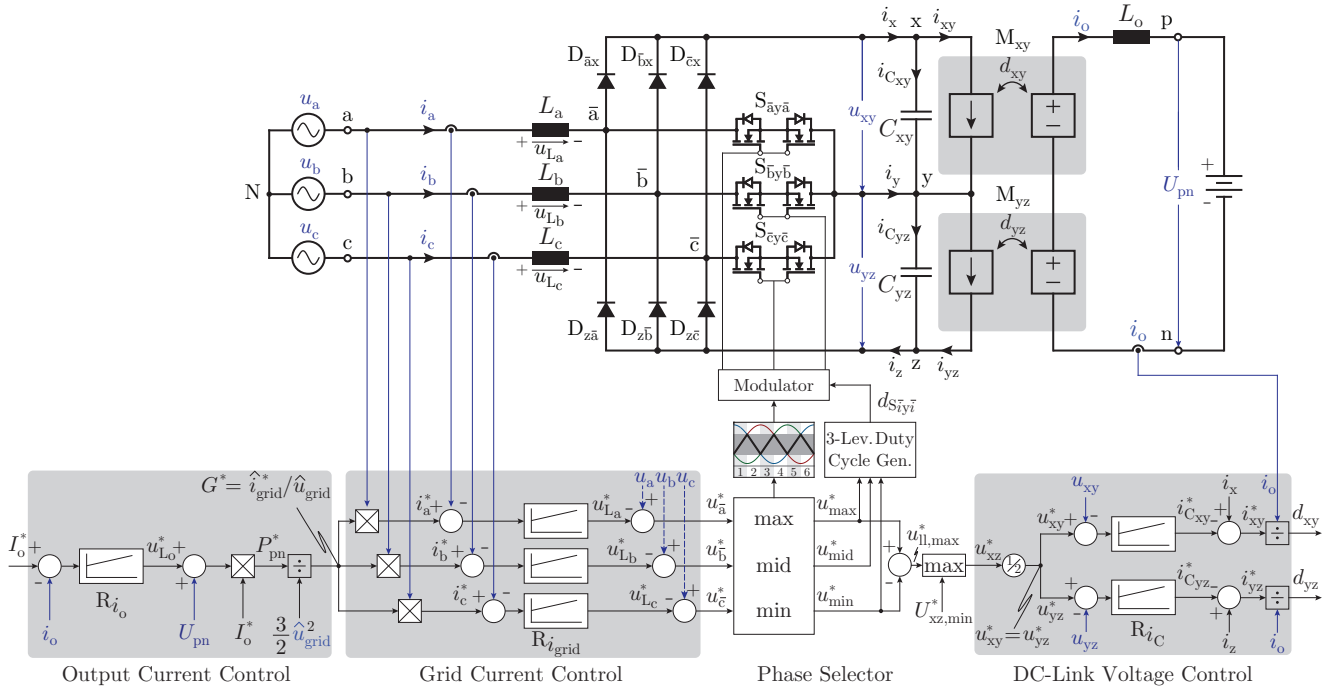

Fig. 4. Cascaded battery/output current control structure of the SynC-VR-i, where measurement values are displayed in blue, and the isolated DC/DC converter modules are replaced by equivalent dependent current and voltage sources. Note that the voltage transfer ratio of the DC/DC converter modules is considered to be 1:1 for simplicity.

voltage of the DC/DC converter stage, $U_{\mathrm{pn}} + u^*_{\mathrm{L_o}}$, in order to be able to control the load current I_{o}, and can be arbitrarily increased in order to utilize the DC/DC converter modules in a more favorable operating point concerning overall system efficiency.

As long as this voltage setpoint is below the actual maximum of the line-to-line voltage, i.e., $U^*_{\mathrm{xz,min}} < u^*_{\mathrm{ll,max}}$, the VR front-end can be operated with 1/3-PWM; on the other hand, if $U^*_{\mathrm{xz,min}} > u^*_{\mathrm{ll,max}}$, the VR front-end has to boost the input voltages to $U^*_{\mathrm{xz,min}}$ by simultaneously switching all three bridge legs, i.e., 3/3-PWM operation. Consequently, the DC-link voltage reference value u^*_{xz} provided to the DC-link voltage controller always equals the maximum of two references $U^*_{\mathrm{xz,min}}$ and $u^*_{\mathrm{ll,max}}$. This voltage is then multiplied with $1/2$ and serves as reference value for the two DC-link capacitor voltage controllers, which finally control the transferred power of each DC/DC converter module. Hence, the two DC-link voltage controllers translate the DC-link voltage control error into a charging/discharging current $i_{\mathrm{C_{xy}}}$ and $i_{\mathrm{C_{yz}}}$ of the DC-link capacitors C_{xy} and C_{yz} in order to track the DC-link voltage reference. Finally, the currents $i_{\mathrm{C_{xy}}}$ and $i_{\mathrm{C_{yz}}}$, where optionally the load state, i.e., i_{x} and i_{z} can be fed forward, are divided by the measured output current i_{o}, resulting in the duty cycles d_{xy} and d_{yz} of the two DC/DC converter modules.

IV. Simulation Results

The presented operation principle and proposed synergetic control strategy are verified with a closed-loop circuit simulation. The waveforms of the converter operating at 20 kW output power and $U_{\mathrm{ac,ll,rms}}$ = 400 V input voltage are shown in **Fig. 5(a)** for an output voltage of U_{pn} = 400 V and a controlled output current of i_{o} = 50 A. Starting with 1/3-PWM operating mode, the minimum DC-link voltage setpoint $U^*_{\mathrm{xz,min}}$ is gradually increased until 600 V, which means that the controller has to transition from 1/3-PWM operation to partial-boost mode, and finally to full-boost mode, i.e., 3/3-PWM operation.

- *1/3-PWM Mode:* As already mentioned, as long as the DC-link voltage setpoint $U^*_{\mathrm{xz,min}}$ is lower than the minimum of the six-pulse reference voltage $u^*_{\mathrm{ll,max}}$, the VR front-end is operated in 1/3-PWM mode. The cascaded controller structure is able to draw sinusoidal currents from the grid by always only switching the phase carrying the lowest current and by controlling the remaining two currents through proper shaping of the DC-link voltage $u_{\mathrm{xz}} (= u_{\mathrm{xy}} + u_{\mathrm{yz}})$, where $u_{\mathrm{xy}} = u_{\mathrm{yz}}$ is always kept.

- *Partial-Boost Mode:* As soon as the DC-link voltage setpoint $U^*_{\mathrm{xz,min}}$ increases to a value between the minimum and maximum of the six-pulse reference voltage $u^*_{\mathrm{ll,max}}$, the VR front-end operates in partial-boost mode, which means that there are intervals where the DC-link voltage reference u^*_{xz} is either defined by $u^*_{\mathrm{ll,max}}$ or the minimum DC-link voltage setpoint $U^*_{\mathrm{xz,min}}$. Consequently, within one sixth of a mains period, the controller has to alternate between 1/3-PWM and 3/3-PWM operation.

- *Full-Boost Mode:* When the DC-link voltage setpoint $U^*_{\mathrm{xz,min}}$ is higher than the maximum of the six-pulse reference voltage $u^*_{\mathrm{ll,max}}$, the VR front-end has to continuously operate in boost mode, where all three phase-legs are pulse width modulated (3/3-PWM).

It should be noted that for all above mentioned operating modes, the controller is able to symmetrically partition the total DC-link voltage, i.e., to ensure $u_{\mathrm{xy}} = u_{\mathrm{yz}}$ for the two DC/DC converter modules, and hence the blocking voltage requirement defined by half the DC-link voltage is not exceeded for the midpoint connected switches, which

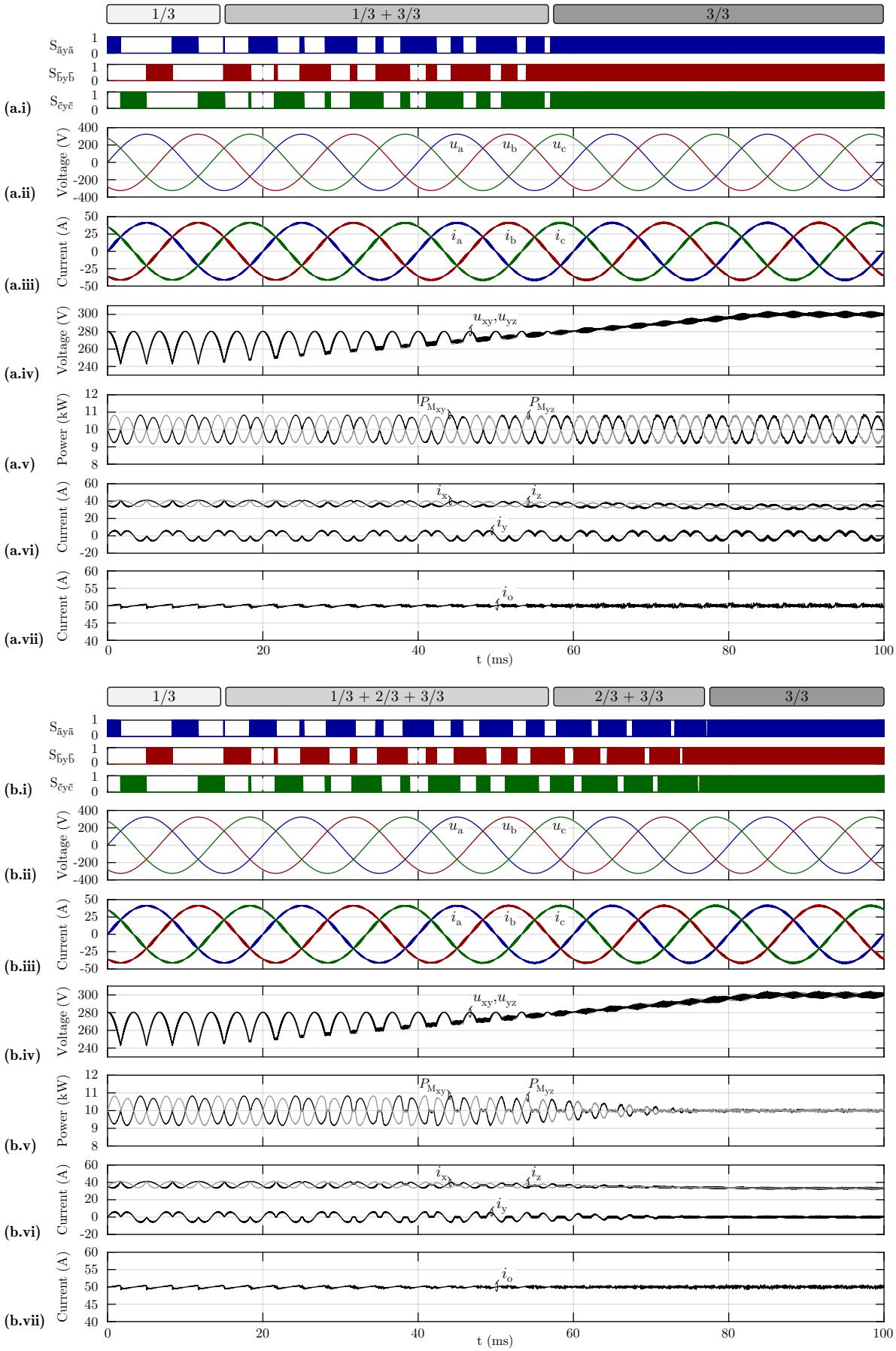

Fig. 5. Simulation waveforms of the SynC-VR-i, for **(a)** a transition between 1/3-PWM and full-boost mode with intermediate (1/3 + 3/3)-PWM operation, and **(b)** the same transition with intermediate (1/3 + 2/3 + 3/3)-PWM and (2/3 + 3/3)-PWM operation: **(i)** modulation strategy and gate signals, **(ii)** grid (AC input) voltages $u_{\{a,b,c\}}$, **(iii)** input phase currents $i_{\{a,b,c\}}$, **(iv)** DC-link voltages, where $u_{xy} = u_{yz}$ is ensured at all times, **(v)** currents of the positive (i_x), mid (i_y) and negative (i_z) DC-link rail (filtered with a first-order low-pass filter with a corner frequency of 5 kHz in order to extract the local average values), **(vi)** power transferred by the two isolated DC/DC converter modules $P_{M_{xy}}$ and $P_{M_{yz}}$, and **(vii)** battery charging, i.e., output current i_o closely adhering to the set reference value $I_o^* = 50$ A. Simulation parameters are: $f_{sw} = 100$ kHz, $L_{\{a,b,c\}} = 100$ µH, $C_{xy} = C_{yz} = 10$ µF, and $L_o = 100$ µH.

enables the use of 600 V semiconductor technology.

For sake of completeness, it has to be mentioned, that there is a possibility to modulate the VR front-end in such a way that the midpoint current i_y is minimized during partial-boost and full-boost mode, as shown in **Fig. 5(b)** for the same operating conditions as considered for **Fig. 5(a)**. This is actually explained for full-boost mode in [14]–[16], leading to a reduction of the power mismatch of the DC/DC converter modules.

Furthermore, besides minimizing the midpoint current, there is a certain voltage range in partial-boost and full-boost mode, where the transition from 1/3-PWM to 3/3-PWM can be smoothed out by only pulse width modulating two of the three rectifier stage phases, i.e., by 2/3-PWM operation as shown in **Fig. 5(b)**. The optimal implementation of this improved transition between the three modulation schemes 1/3-PWM, 2/3-PWM, and 3/3-PWM is subject of current research, which also considers the optimal use of 2/3-PWM for other types of midpoint-connected converters, including all possible VR configurations [17], the Hybrid Active Neutral Point Clamped (HANPC) [18], or the Stacked Multicell Converter (SMC) [19].

V. Semiconductor Stress Analysis

In order to quantify the performance gain achieved by the 1/3-PWM for the VR front-end at hand in terms of semiconductor losses, the switching and conduction losses of the VR front-end semiconductors are analytically derived and compared for both the 3/3-PWM and 1/3-PWM operation.

1) Switching Losses: To model the switching losses, the following two assumptions are made. Firstly, the input currents $i_{\{a,b,c\}}$ are assumed purely sinusoidal, i.e., the switching frequency current ripple of the input currents is considered to be small, such that only hard-switching transitions are occurring. And secondly, a linear dependency of the hard-switching losses on the switched current is considered. This last assumption is a valid first step approximation, particularly for Wide Bandgap (WBG) devices, as shown in [20] for 650 V GaN devices and in [21] for 900 V SiC devices. Therefore, the switching losses are modeled as

$$E_{sw}(t) = k_{sw,0} + k_{sw,1} \cdot i(t) \ , \tag{2}$$

where $k_{sw,0}$ is the current independent switching loss component (which is equal to the switching losses at zero current) and $k_{sw,1}$ characterizes the linear dependency of the switching losses on the switched current $i(t)$. By averaging the switching losses $E_{sw}(t)$ over a fundamental grid period, the following expressions for the switching losses are obtained:

$$P_{sw,3/3} = \left(k_{sw,0} + k_{sw,1} \cdot I_{avg}\right) f_{sw} \tag{3}$$

$$P_{sw,1/3} = \Big(\underbrace{\frac{k_{sw,0}}{3}}_{-66\,\%} + \underbrace{\left(1 - \frac{\sqrt{3}}{2}\right) k_{sw,1} \cdot I_{avg}}_{-86\,\%}\Big) f_{sw} \ ; \tag{4}$$

$P_{sw,3/3}$ and $P_{sw,1/3}$ are the switching losses for the 3/3-PWM and 1/3-PWM operation, f_{sw} denominates the switching frequency, and I_{avg} is the average value of the rectified sinusoidal input current $i_{\{a,b,c\}}$, resulting as $I_{avg} = {}^{2\cdot\hat{I}}/_{\pi}$, with $\hat{I}$ being the peak value of $i_{\{a,b,c\}}$.

In addition to a 66 % saving of current independent switching losses, and a 86 % saving of linearly current dependent losses, it has to be noted that in practice some further switching loss savings will occur due to the dependency of the switching losses on the switched voltage (e.g., $k_{sw,0}$ actually is proportional to u_{xy}^2 and u_{yz}^2 [22]). For the sake of clarity, the voltage dependency of the switching losses has been omitted in this analysis, but still more than two-thirds of the switching losses of the front-end VR are saved.

2) Conduction Losses: In the following, the RMS currents of the switches, and the RMS and average (avg) currents of the diodes of the VR front-end are derived for the the 3/3-PWM and 1/3-PWM schemes, in order to quantitatively compare the conduction loss difference between both modulation schemes.

- *Switch RMS Current:*

$$I_{S,rms,3/3} = \frac{\hat{I}}{\sqrt{\pi}} \sqrt{\frac{\pi}{2} + \frac{5\sqrt{3} - 16M - 8}{12}} \ , \tag{5}$$

$$I_{S,rms,1/3} = \frac{\hat{I}}{\sqrt{\pi}} \sqrt{\frac{\pi}{6} + 2\sqrt{3} \ln\left(\frac{\sqrt{3}}{2}\right)} \ . \tag{6}$$

- *Diode RMS Current:*

$$I_{D,rms,3/3} = \frac{\hat{I}}{\sqrt{\pi}} \sqrt{\left(\frac{1}{3} - \frac{3\sqrt{3}}{16}\right)(2M+1) + \frac{18M-1}{16\sqrt{3}}} \ , \tag{7}$$

$$I_{D,rms,1/3} = \frac{\hat{I}}{\sqrt{\pi}} \sqrt{\frac{\pi}{6} + \frac{\sqrt{3}}{8} \ln\left(\frac{256}{81}\right)} \ . \tag{8}$$

- *Diode AVG Current:*

$$I_{D,avg,3/3} = \hat{I} \frac{M}{\sqrt{4}} \ , \tag{9}$$

$$I_{D,avg,1/3} = \hat{I} \frac{\sqrt{3} \ln(3)}{2\pi} \ . \tag{10}$$

All currents are given in dependency of the modulation index M, which is defined as

$$M = \frac{\hat{U}}{(u_{xz}/2)} \ , \tag{11}$$

where $\hat{U}$ is the peak value of the grid (input) phase voltages $u_{\{a,b,c\}}$.

A quantitative comparison of the current stresses of 3/3-PWM vs. 1/3-PWM operation is shown in **Table I**, where for the 3/3-PWM mode a DC-link voltage of $u_{xz} = 600$ V is chosen, as also considered for the representation in **Fig. 3(a)**. The main advantage of 1/3-PWM operation regarding conduction losses is that the switches of the VR front-end only conduct the current in two 60 °-wide intervals, which are moreover centered around the zero crossing of the grid current. This translates into a very large reduction of the RMS current stress on the switches (-63.4 %), leading to 86.7 % lower conduction losses of the switches, at the cost of a small RMS and average current

TABLE I

SIMULATED AND CALCULATED SEMICOND. CURRENTS. 3/3-PWM CASE IS FOR $u_{XZ} = 600$ V, CF., **FIG. 3**.

		3/3-PWM		1/3-PWM		Difference
		Sim.	Theor.	Sim.	Theor.	
Switch	rms	10.15 A	9.85 A	3.71 A	3.68 A	-63.4 %
Diode	rms	19.28 A	19.28 A	20.40 A	20.33 A	+5.5 %
	avg	11.08 A	11.10 A	12.44 A	12.41 A	+12.3 %

increase in the diodes, +5.5 % and +12.3 % respectively (cf., **Fig. 3(iv-v)**).

Remark: If the VR front-end would always be operated with 1/3-PWM without transitioning into partial-boost or full-boost mode, a smaller die area (or number of parallel switches) could be selected for realizing the switches $S_{\bar{i}y\bar{i}}$ without large influence on the losses, since conduction losses would increase for a smaller die area, but the capacitive hard-switching losses due to the parasitic output capacitance of the switches (C_{oss}) would reduce inversely proportional to the die area [23], finally enabling a more cost effective realization of the EV-charger VR front-end for a similar performance.

VI. CONCLUSIONS

In this paper, a novel synergetic control scheme of a three-phase/level PFC rectifier and a series-connected isolated DC/DC stage for high power EV chargers is introduced. By only always pulse width modulating the phase with the smallest current (1/3-PWM), and by shaping the DC-link voltage close to the six-pulse maximum line-to-line grid voltage, a sinusoidal current consumption of all phases can be ensured, while the switching losses of the PFC stage can be reduced by more than two thirds for the given example, and the conduction losses even decrease by around -86 %. Furthermore, by symmetrically partitioning the total DC-link voltage, 600 V semiconductor technology can be used throughout the whole converter, further decreasing the losses by allowing the use of latest GaN devices. Finally, it has been shown that the converter can seamlessly transition from 1/3-PWM to partial-boost and full-boost operation mode, i.e., 2/3-PWM or 3/3-PWM operation, thus obtaining a widely controllable DC-link voltage value which reduces the output voltage range requirement of the DC/DC converter modules.

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