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Large Panel Fan Out Technology Overview and Development

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NCAP CHINA

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半导体封装技术研究所

广东省半导体智能装备与系统集成创新中心

TestConX中国 China

Suzhou ▪ October 23, 2018
Shenzhen ▪ October 25, 2018

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Personal Introduction

More than 25-year experiences in design, process, assembly, reliability and business management in electronics IC packaging, semiconductor, consumer electronics, mobile phone assembly, PCBA, thermal and aerospace industry. Motorola certified Six Sigma Black Belt. Holding position of board member of CSR (chip scale review), have filed more than 40 international patents and 150 international Journal and conference papers; working in NCAP 5 years, and prepare to move Guangdong province for LPFO integrated equipment and process development and commercialization

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NCAP Introduction

Wuxi Headquarters

- 3000m^2 Cleanroom
- Class 10/100/1,000/10,000
- 8″/12″ wafer

Beijing Center

- 1000m^2 Cleanroom
- Class 1,000/10,000

- **R&D & Engineering with 9000m²**
- **engineering assembly &metrology equipment with ￥160 million，fixed total equipment value ￥345 million。**

- **Established in Wuxi in 2012**
- **10 investors** Including the Institute of Microelectronics and the largest OSATs and substrate companies in China (JCAP, NT Fujitsu, WLCSP, ANJILI, WULIWANG, SCC, NDB, IME, Hua Tian, XIN Sheng Kuai Jie)
- **Independent business entity**

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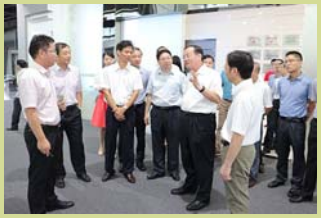
CNC Equipment Innovation Institute Introduction

Foshan Nanhai Guangdong Technology University CNC Equipment Cooperation Innovation Institute is jointly set up by Guangdong Provincial Department of Science and Technology, The People's Government of Foshan Municipality, Nanhai People's Government of Foshan and Guangdong University of Technology.

- **Honor and Qualifications**
  - National High-tech Business Incubator
  - National Group Innovation Space
  - New R&D institution in Guangdong
  - Joint-postgraduates Demonstration Base
  - College Students Practical Teaching Base in Guangdong

- **Leadership Concern**






Chinese Premier Li Keqiang inspect our work

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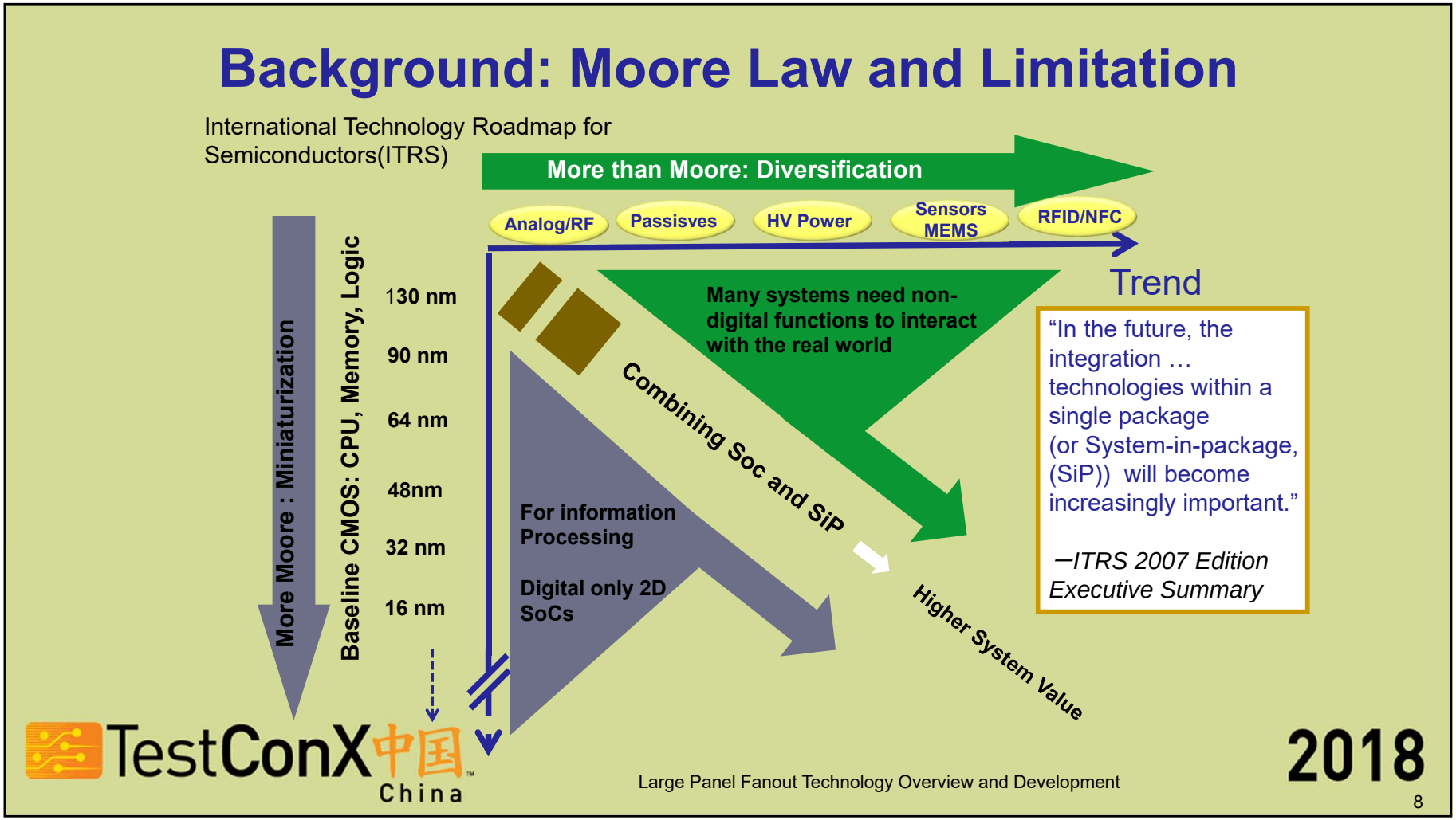
Background: Moore Law and Limitation
International Technology Roadmap for Semiconductors(ITRS)
More than Moore: Diversification
Analog/RF
Passisves
HV Power
Sensors MEMS
RFID/NFC
Trend
More Moore : Miniaturization
Baseline CMOS: CPU, Memory, Logic
130 nm
90 nm
64 nm
48nm
32 nm
16 nm
Many systems need non-digital functions to interact with the real world
Combining Soc and SiP
For information Processing
Digital only 2D SoCs
Higher System Value
"In the future, the integration … technologies within a single package (or System-in-package, (SiP)) will become increasingly important."
—ITRS 2007 Edition Executive Summary
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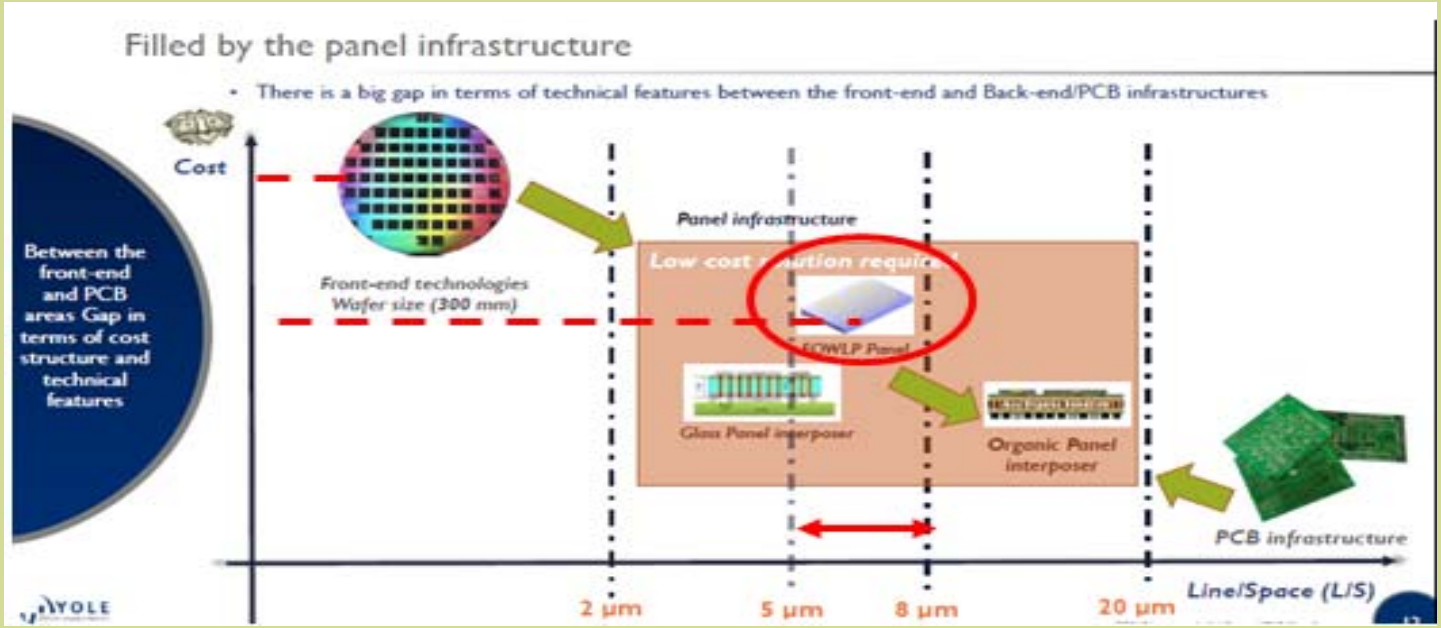
Background: Development Trend



- **The extension of Moore's law is subjected to multiple pressures such as physical limits, huge investment and so on.**
- **The urgent need to develop a new style technology progress "More Than Moore"**

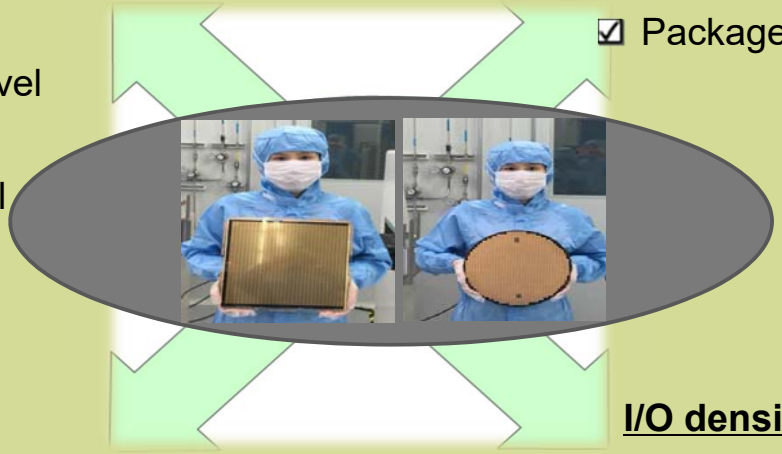
Background: Why Fanout ?

Performance

- ☑ Shorter interconnect length, high speed application;
- ☑ Superior package level reliability，
- ☑ Excellent board level reliability

Form Factor

- ☑ Thinner package，
- ☑ Package size Scalability



Cost Advantage

- ☑ Substrate /gold free，
- ☑ Scalable to the large panel (600mm above)

I/O density

- ☑ Small pitch，
- ☑ High pin counts

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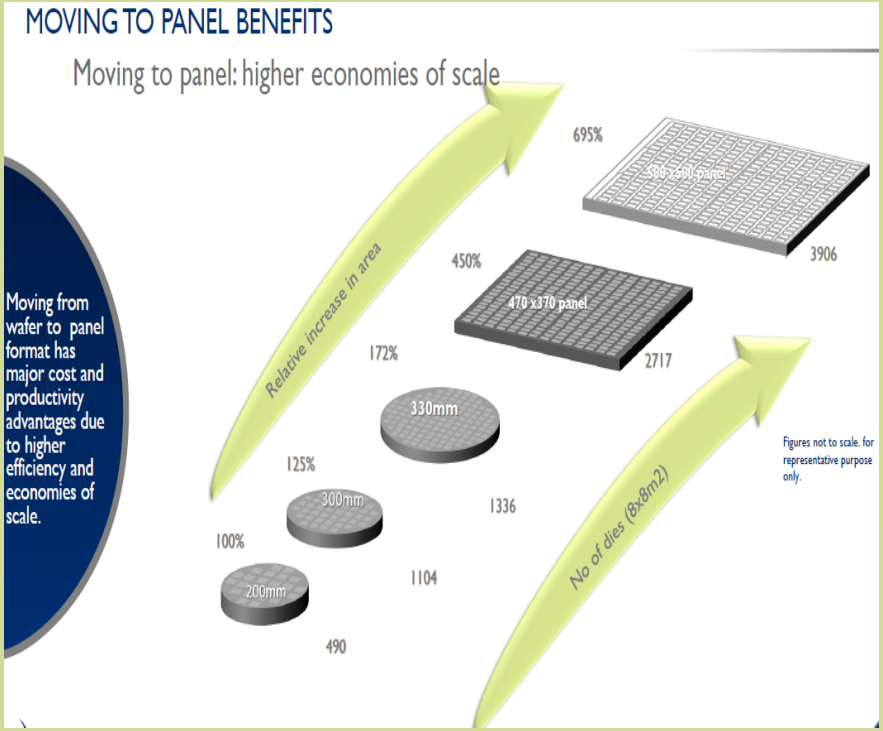
Background: Advantages of LPFO

Through LPFO integration advanced packaging technology, to achieve high-density integration, volume miniaturization and lower cost.

- **The advantages of LPFO**
  - Higher integration and wider application;
  - More flexible design and higher density wiring;
  - Better electro-thermal performance, smaller and thinner volume;
  - High efficiency and low cost



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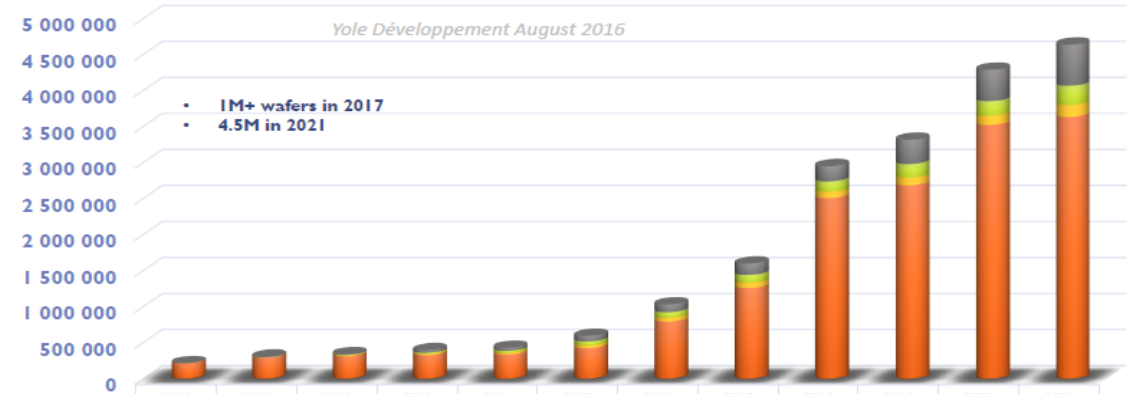
Background: Fanout Market Forecast

FAN-OUT ACTIVITY - MARKET FORECAST

Executive Summary

Fan-out activity forecast (300mm eq wafers) breakdown per end-market

Apple's example will show competitors the way



	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021
Industrial	0	6 623	10 432	33 343	42 560	75 210	103 123	155 315	211 931	335 930	435 063	570 487
Consumer	1 258	4 964	7 767	16 458	28 963	55 212	76 918	111 427	143 455	188 426	201 933	264 789
Medical	0	0	0	116	301	568	991	1 487	2 230	2 997	3 401	4 460
Automotive	0	0	7 420	17 615	21 506	38 269	56 930	71 023	85 120	105 302	125 842	165 013
Mobile - Wireless	214 123	292 016	314 053	325 654	335 120	423 691	790 923	1 257 867	2 508 956	2 683 417	3 521 846	3 632 789

Mobile - Wireless Automotive Medical Consumer Industrial

YOLE Développement

©2017 | www.yole.fr | Equipment and Materials for Fan-Out Packaging | Report

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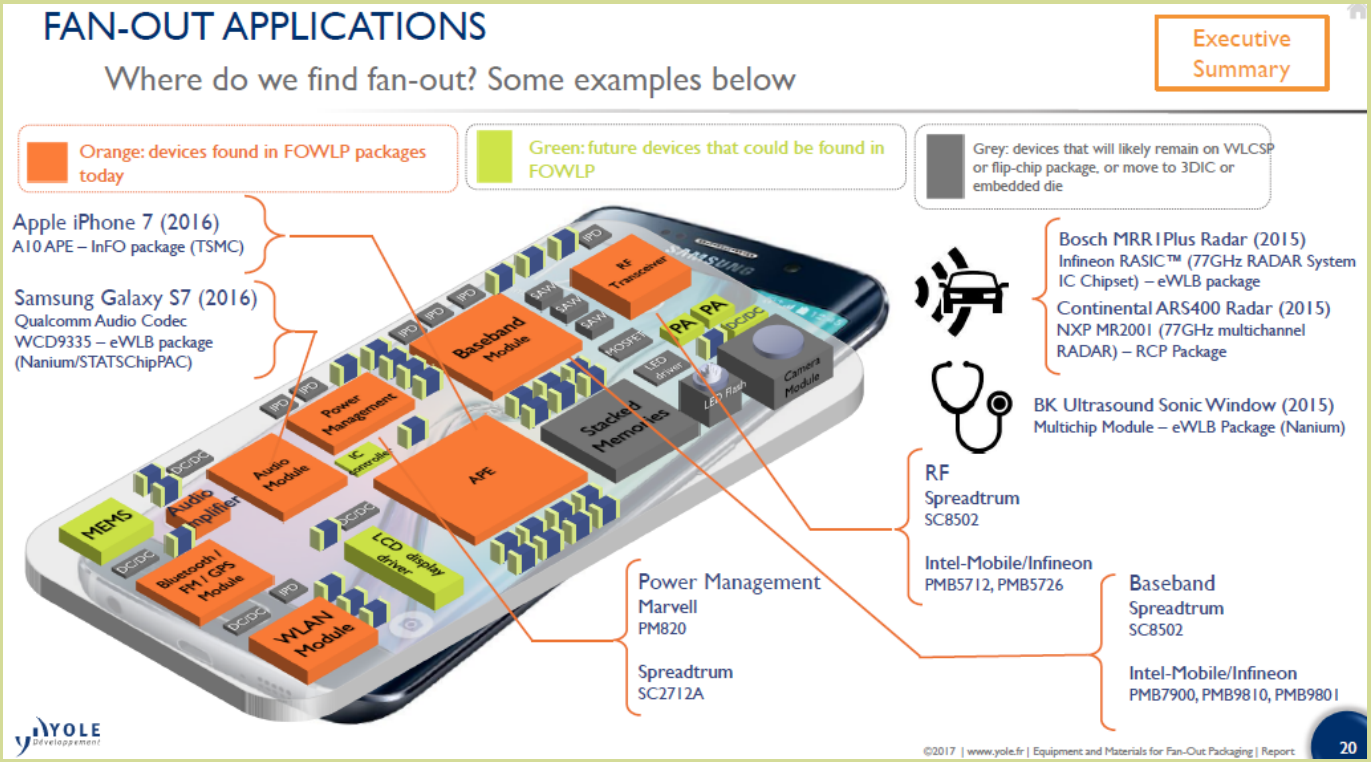
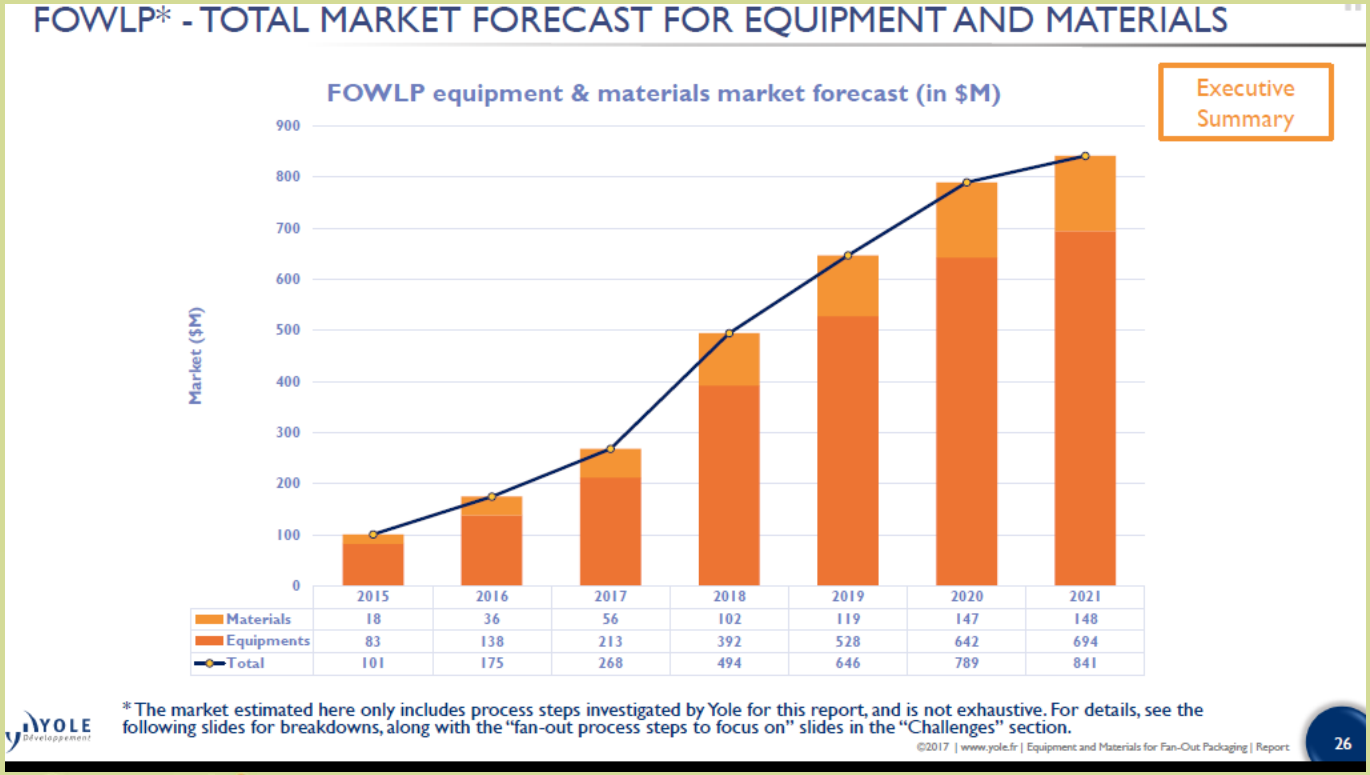
Background: Fanout Applications



Background: Fanout Materials and Equipments



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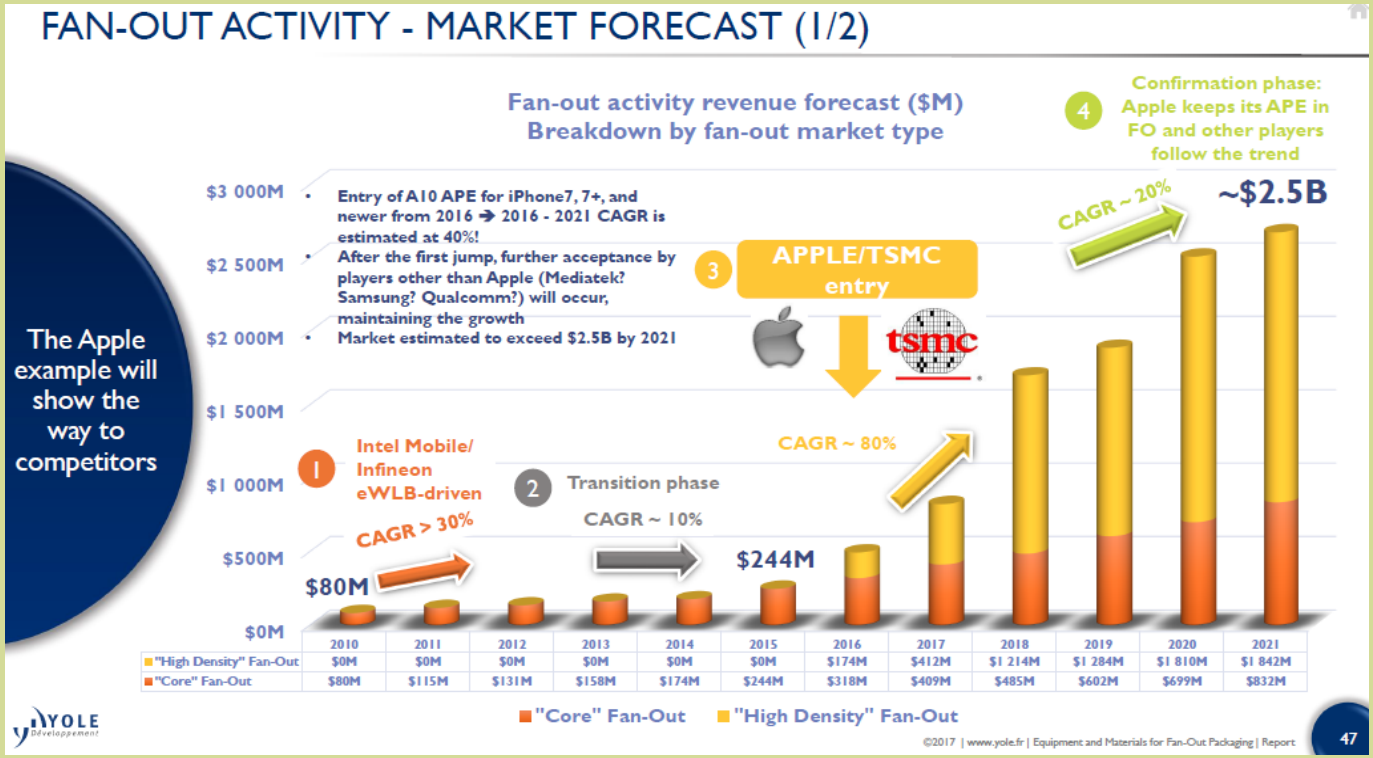
Background: Fanout Market Driver



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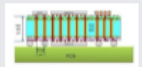
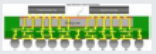
Background: Fanout Market Players

Key players pushing the panel manufacturing platform

		Fabless	OSATs	Substrate makers	IDMs
FOWLP on panel		QUALCOMM, MEDIATEK	J DEVICES, BPIL, STATSChipPAC, ASE GROUP, Powertech Technology Inc.		
Embedded die		QUALCOMM	ASE GROUP, J DEVICES	AT&S, TDK, TAIYO YUDEN, Unimicron, SHINKO	EPCOS, NXP, SCHWEIZER, Infineon, BOSCH
Glass interposer			triton	Unimicron, IBIDEN, SCHOTT, CORNING, AGC	
Organic interposer		QUALCOMM	Amkor, BPIL	SHINKO, Unimicron, SAMSUNG ELECTRO-MECHANICS	intel
Hybrid interposer		ALTERA, XILINX, Microsemi		Unimicron, KYOCERA	intel

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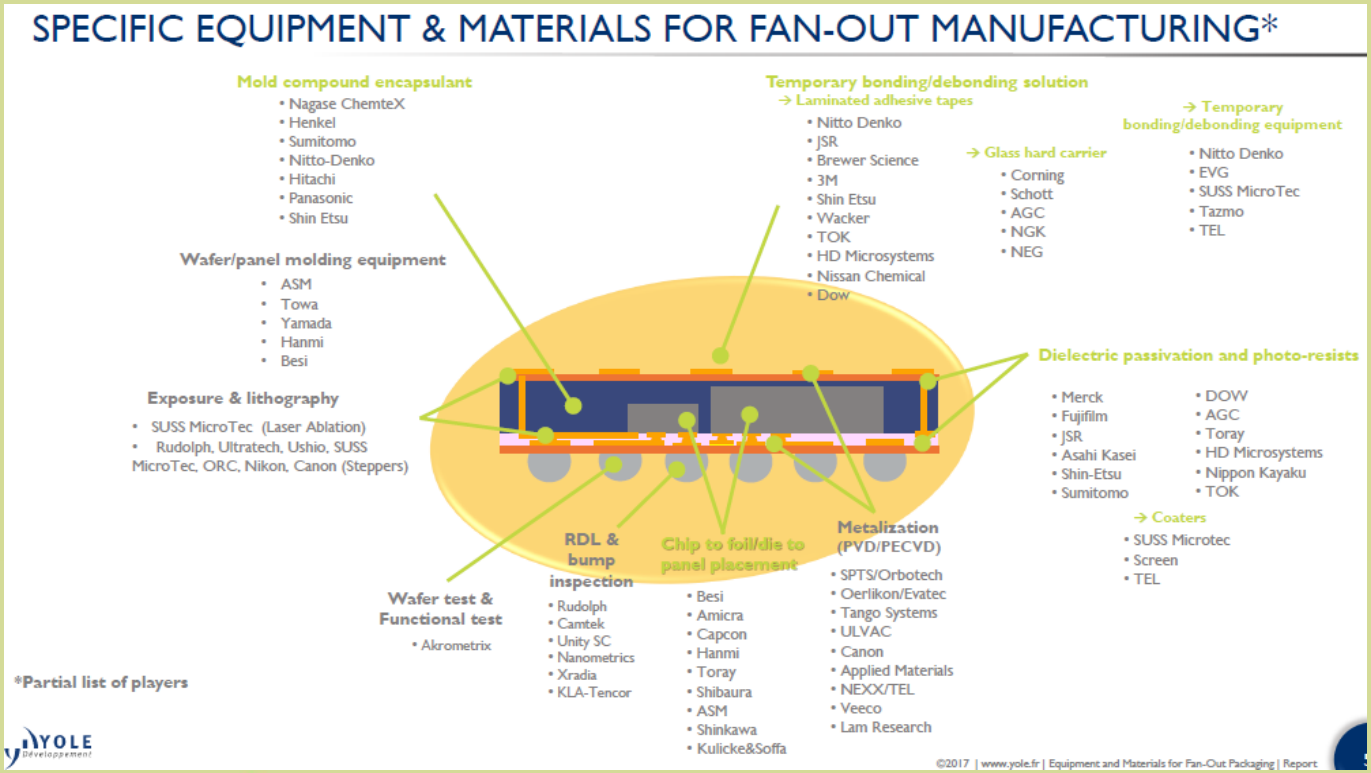
Background: Fanout Supply Chain



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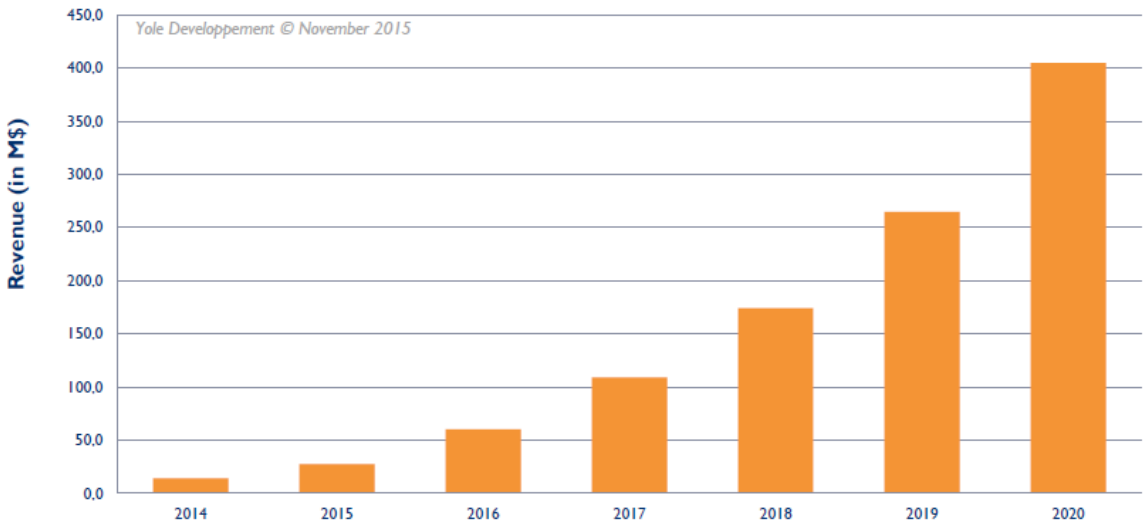
Background: Revenue from PLP

In M$

he panel
ackaging
dustry will
each $109M
y 2017



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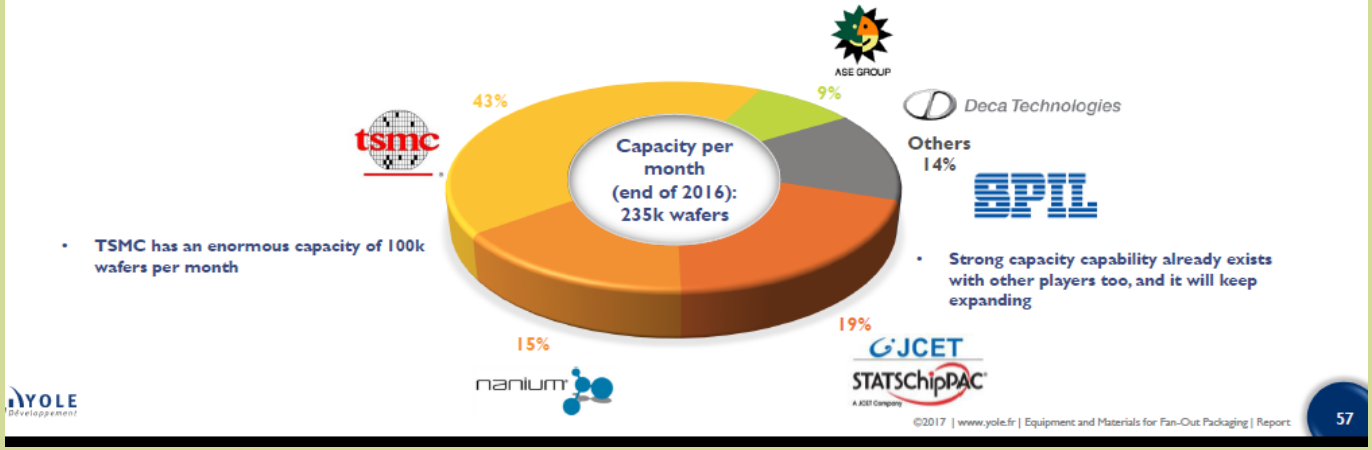
Background: Fanout Market Capacity

FOWLP - ALREADY-INSTALLED CAPACITY

- At the end of 2016, fan-out investments were already very important, and consequently so is capacity
  - With a capacity of 100,000 wafers/month, TSMC's InFO product has the largest capacity
  - Other main manufacturers are established eWLB providers: Nanium and STATS ChipPAC. Each can produce around 10,000 wafers per week.
  - STATSChipPAC is enlarging its capacity to raise production
  - Since TSMC's action was quite formidable, investment in equipment for 2017 will not be as high - but it will still be decent:
  - Led by newcomers willing to have a FOWLP offer
  - As well as major players willing to enlarge their capacity (STATSChipPAC and potentially ASE together with Deca)
- With 4.5M wafers to be produced in 2021, capacity must be increased by TSMC and/or other actors. Therefore, a second wave of investment will occur later on; otherwise, capacity be insufficient for addressing the FOWLP market if it keeps growing (see the following slides).



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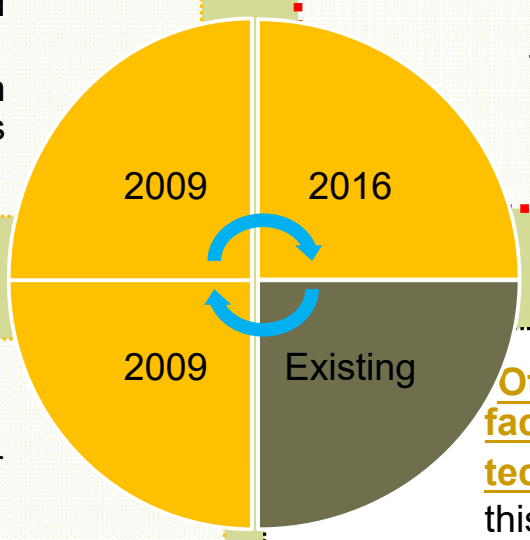
Major Fanout Technologies

- **eWLB (wafer level)**
- First fanout patent filed at 2001
- Shipped out 1billion units since mass production in 2009

- **TSMC InFO (wafer level)**: Apple used this technology in iPhone 7 (A10 processor)



- **RCP** technology (wafer level), from frees, and licensed NEPES,
- Low volume shipment

Others (e.g., DECA (chip face up panel level) technology; ASE licensed this technology (panel level, and ship out 100 million units)

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Major Fanout IPs

US006727576B2

(12) **United States Patent**
Hedler et al.

(10) **Patent No.: US 6,727,576 B2**
(45) **Date of Patent: Apr. 27, 2004**

(54) **TRANSFER WAFER LEVEL PACKAGING**

(75) Inventors: **Harry Hedler**, Germering (DE); **Thorsten Meyer**, Erlangen (DE); **Barbara Vasquez**, Munich (DE)

(73) Assignee: **Infineon Technologies AG**, Munich (DE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 10/044,000

(22) Filed: **Oct. 31, 2001**

(56) **References Cited**

U.S. PATENT DOCUMENTS

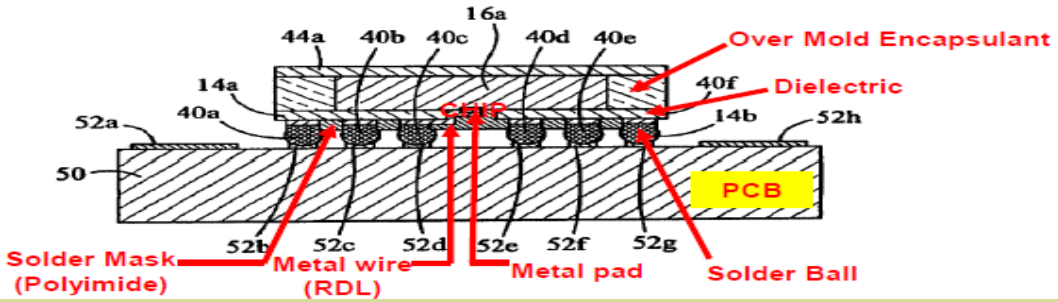
6,537,848 B2 * 3/2003 Camenforte et al. 438/106

* cited by examiner

Primary Examiner—David Nelms
Assistant Examiner—Mai-Huong Tran
(74) *Attorney, Agent, or Firm*—Fish & Richardson

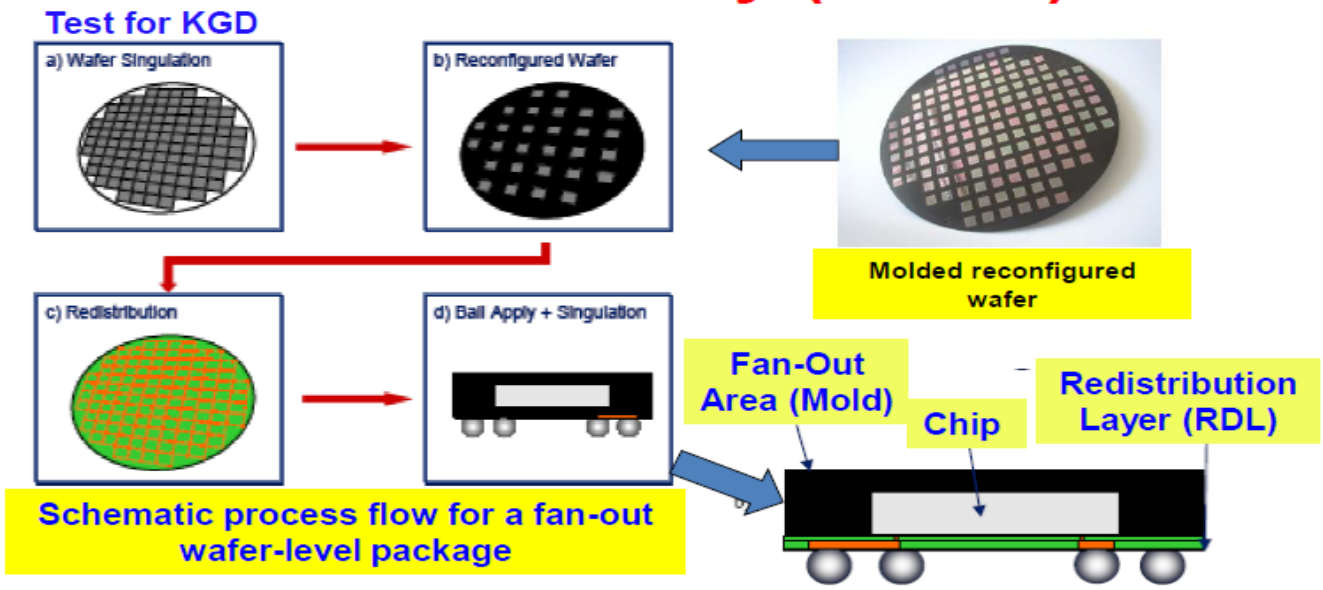
(57) **ABSTRACT**

A semiconductor structure and a method for forming the semiconductor structure, including a semiconductor chip



Typical eWLB Process Characterization

Infineon's Embedded Wafer-Level Ball Grid Array (eWLB)



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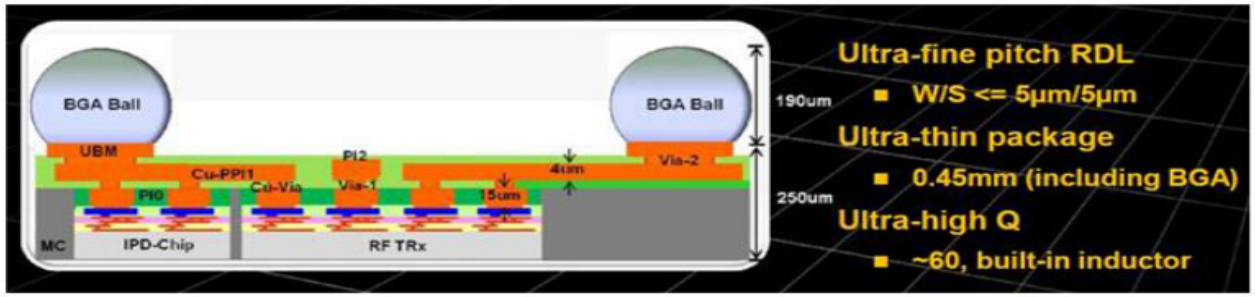
Typical InFO-WLP Process Characterization

TSMC InFO-WLP
(Integrated Fan-Out WLP)



At the TSMC Technology Symposium in San Jose, CA in April 2014, TSMC announced the latest InFO-WLP platforms:

- 8mm x 8mm is targeted at RF and WiFi chips
- 15mm x 15mm is targeted at application processor and baseband chips
- 25mm x 25mm could be applied to GPU and networking chips

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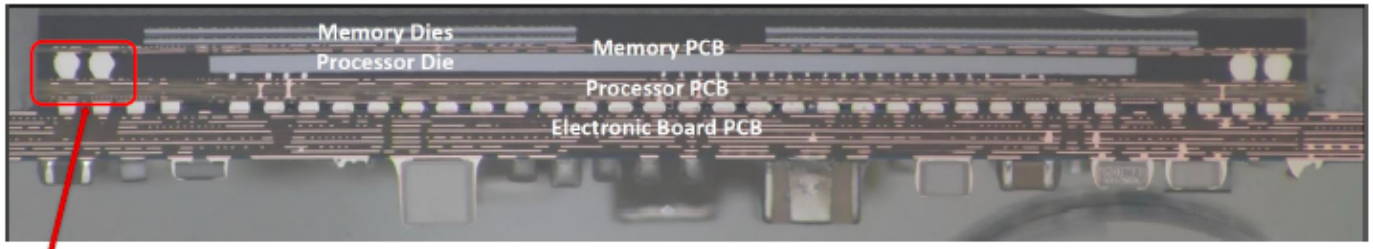
Typical InFO-PoP



Samsung Exynos 8 in typical PoP structure

(flip chip on laminate, laser drilled via with solder fill)

3D Interconnect for PoP

Apple A10 (iPhone 7) in TSMC InFO PoP

(chips first fan-out with ECD Cu posts)

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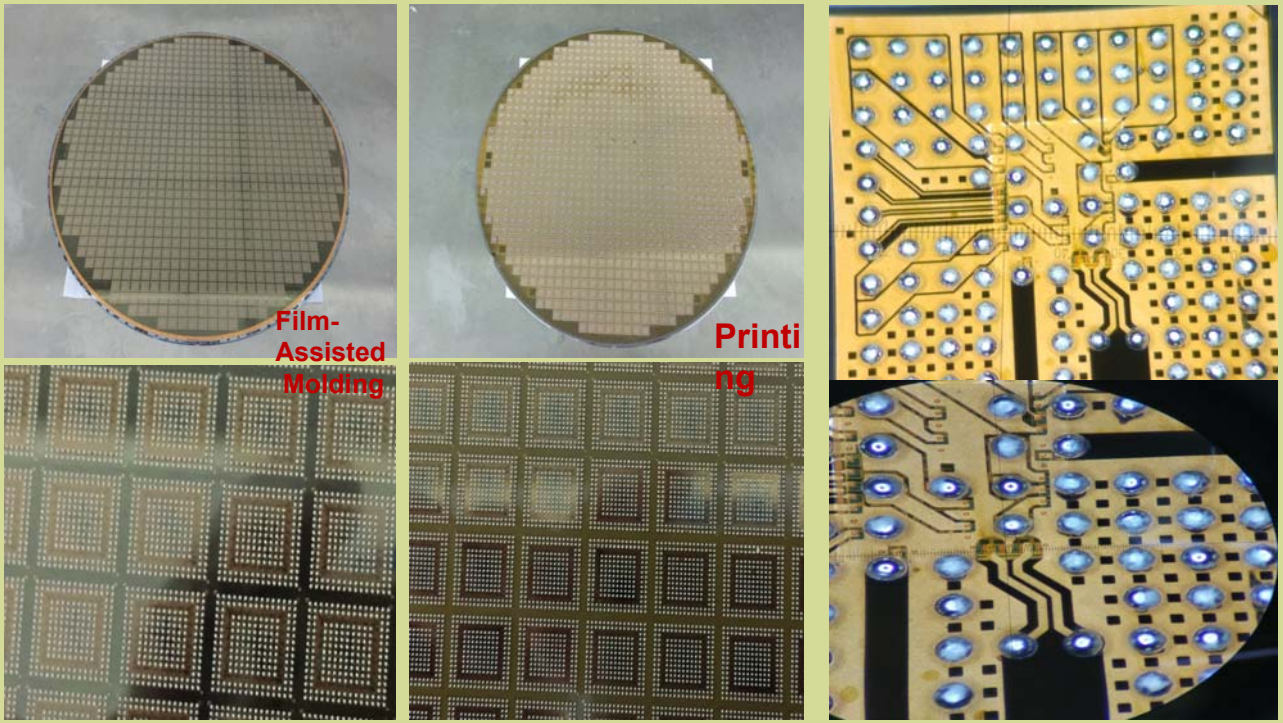
OSAT Distribution for Fan out

OSAT in China	Packaging Fan out Technologies available	status
Hua Tian Scientific Co., Ltd	eSIFO ™	Qualified and engineering samples are ready; and ready for ramping in the production
JCET	MIS technology based	Ready for mass production
NT Fujitsu	Panel level fan out	In development
National Centre for Advanced Packaging (China), mass production OSAT	eWLP, PLP, etc.	Factory built up in Jiangsu province

Typical NCAP eWLB Samples



77G eWLB sample

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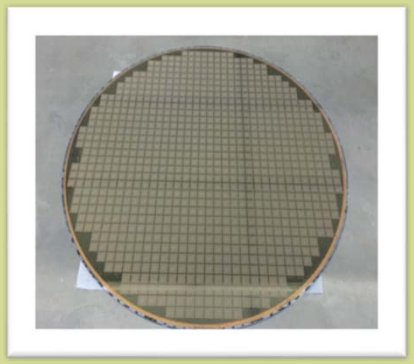
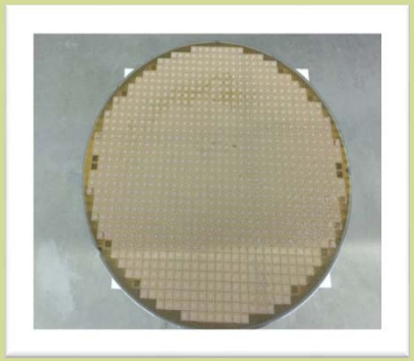
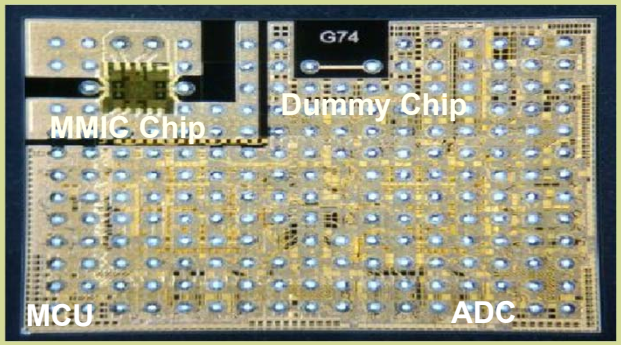
Typical NCAP eWLB Samples

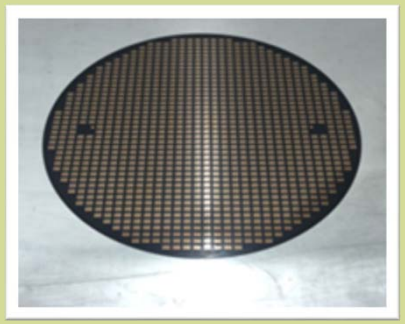


Film-assisted molding



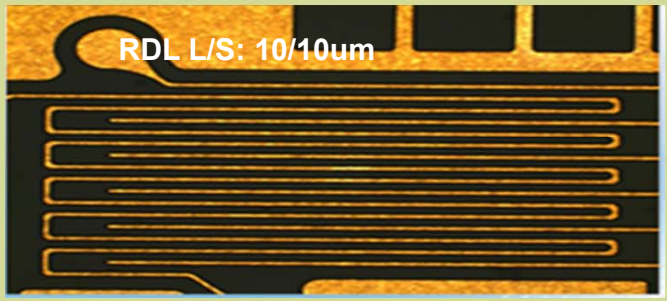
Printing





WLFO-12″

PLFO-320mm×320mm



4-chip SiP module with 204 solder balls

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Key Observations from Reliability & FA

1. During reliability test, we found solder ball drop off and big voids are observed after HTS-1008 hrs and TC-750 cycles, it is confirmed that reflow profile needs to be optimized.
2. After pre-conditioning. There are delamination found between PI materials, it is confirmed process of PI curing needs to be optimized.
3. For TC test, it is found that delamination occurred between PI and die, process and material are needed to be evaluated and optimized.
4. For uHAST-144h，it is found that delamination happened between UBM and solder ball, plating and reflow process must be evaluated and optimized.

1st Run Reliability Test

Based on eWLB fan out packaging, daisychain dies are used for packaging, and reliability assessment is done for Pre-con, Thermal Cycles (TC), HTS and uHAST according to JEDEC requirements. The major results are shown below.

Types of tests	JEDEC standard	conditions	Test points	failures	Failure modes	Root causes
Pre-con test	JESD22-A113	120℃, 24hrs; 30℃/60%RH, 96hrs; 260℃, 3x reflows;	/	29/248	Delamination between PI	Process and materials
Thermal cycles	JESD22-A104	-40℃~125℃,10℃/min	320cycles	5/77	-	
			750cycles	59/77	Delamination between PI and dies	Materials
High temperature storage (HTS)	JESD22-A103	150℃,1008hrs	1008hrs	4/45	EMC filling in and delamination between PI	Process
uHAST	JESD22-A110	130℃,85%RH, 96hrs	96hrs	5/77	-	
			144hrs	22/77	Voids and delamination between solder ball and UBM	Process

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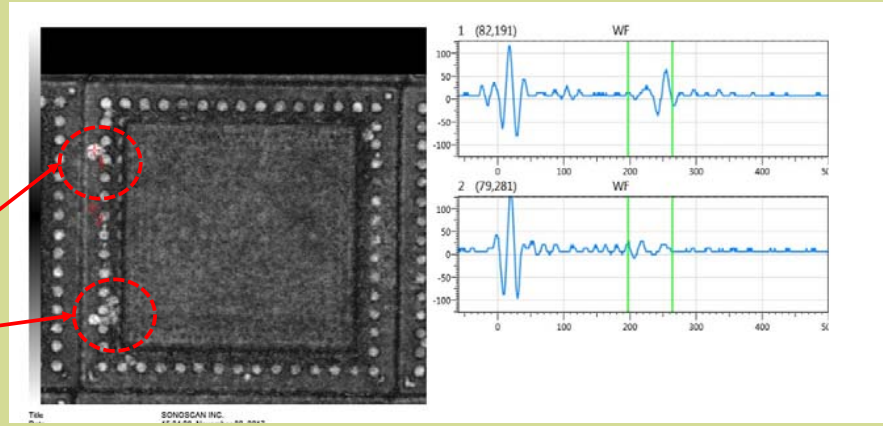
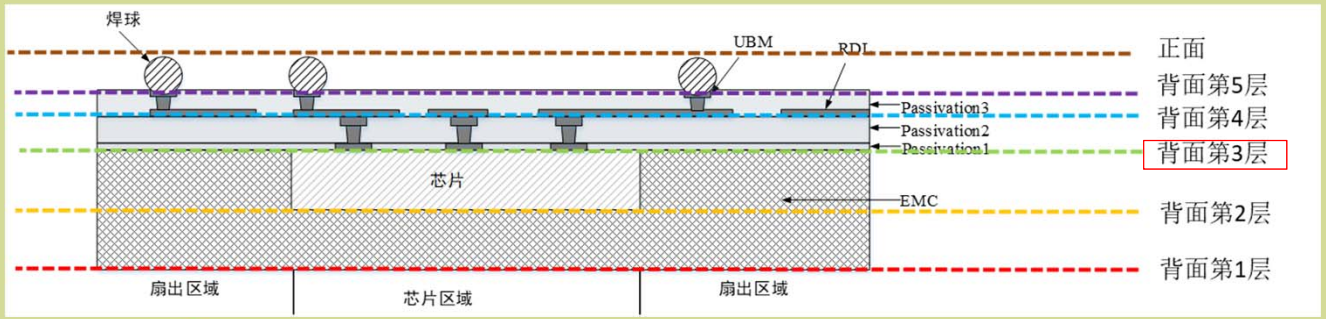
Pre-con Reliability Test



The fourth layer of chip 135， Delamination appears at the edge of PI opening.



Package Cross Section

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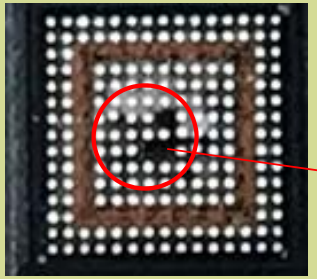
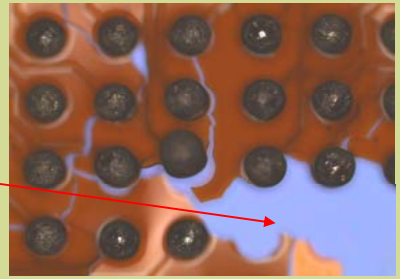
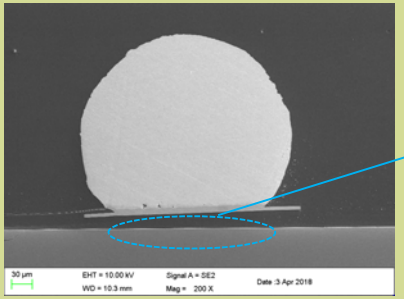
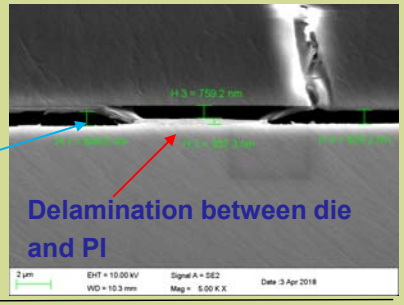
TC 750 Reliability Test





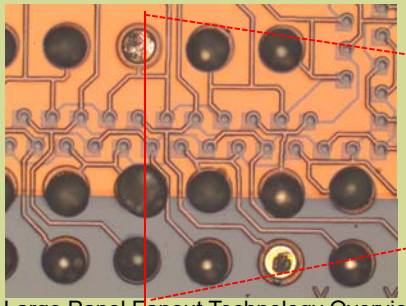
Microscopes showed surface materials drop off from die surface

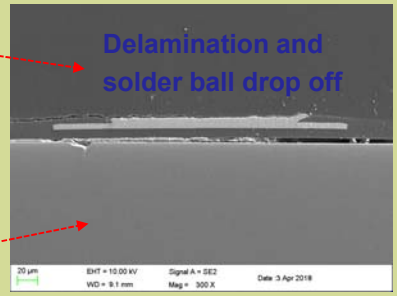




Cross-section showed delamination occurred between PI and die

Solder ball drop off





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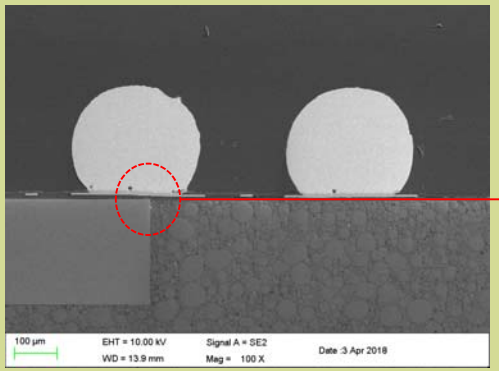
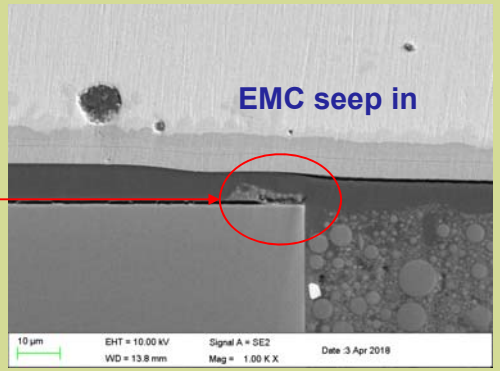
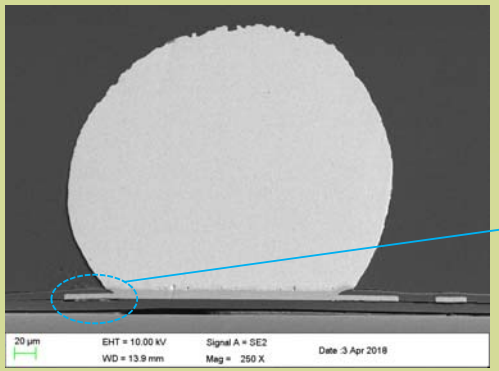
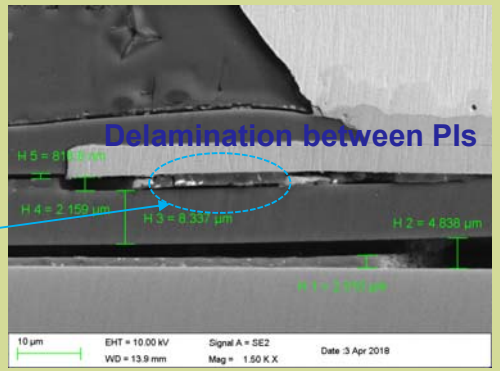
HTS (1000 hrs) Reliability Test

EMC seep into between die and PI interface









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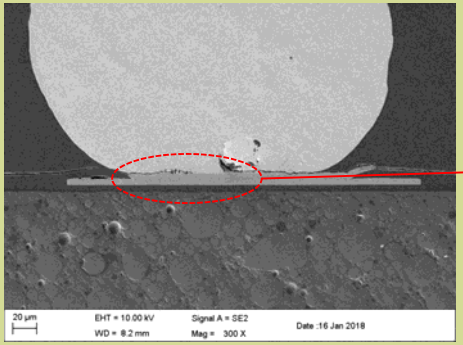
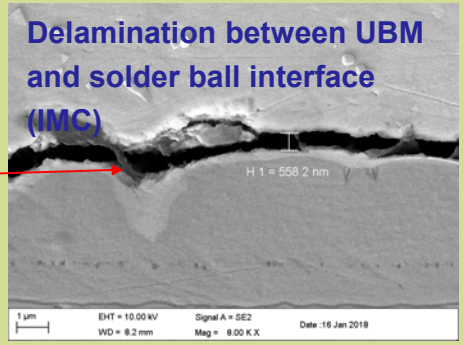
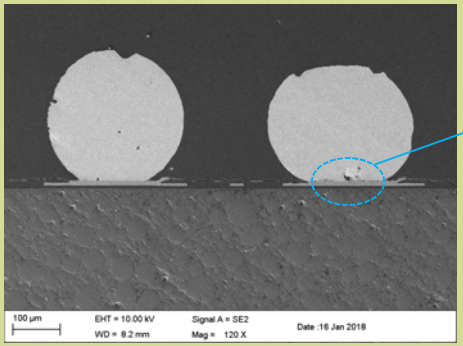
uHAST (144 hrs) Reliability Test

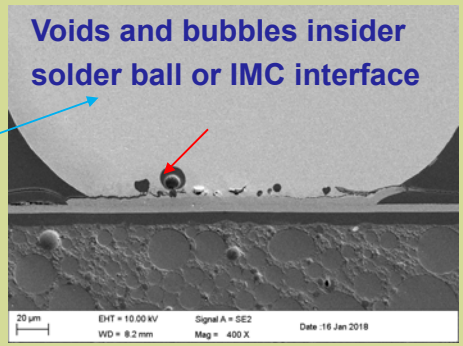
Delamination between UBM and solder ball interface





Voids and bubbles occurred at IMC interface





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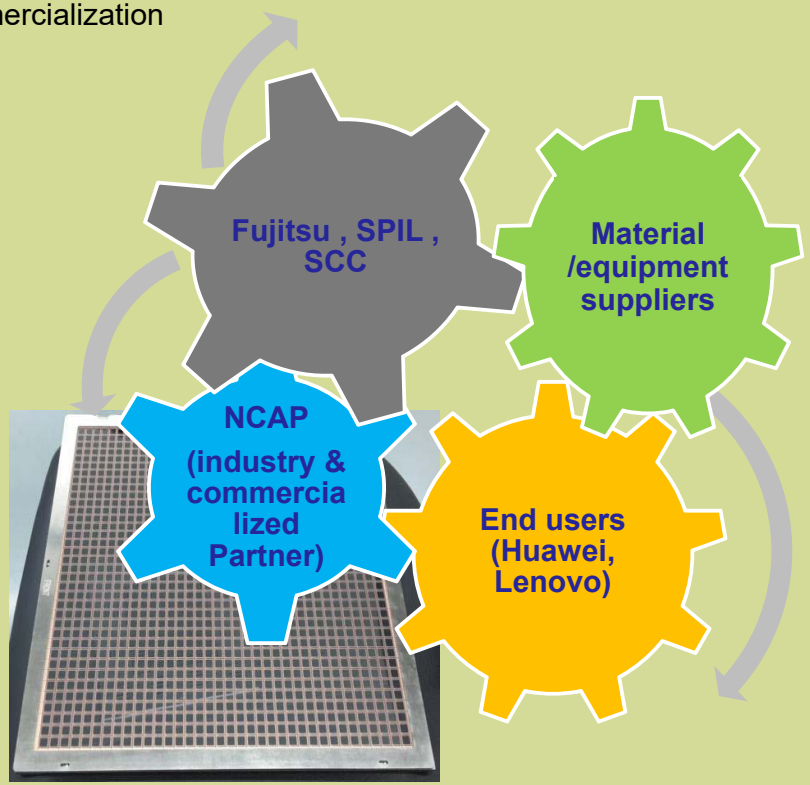
NCAP LPFO Consortium

No.	Key members
1	NCAP
2	SCC (深南)
3	SPIL (Taiwan)
4	Sinopaco（中鹏）
5	AMC（Taiwan)
6	Delphilaser（德龙）
7	Fujitsu
8	TOWA
9	Bee-semi(中电科)
10	JSR
11	Screen
12	KohYoung (高永)
13	Savansys
14	Huawei
15	Mascem（技美）
16	Sumitomo
17	Shin-Etsu(信越)
18	DNP（大日本印刷）
19	ASM
20	Ingenic(君正)
21	ORC
22	SCHOTT
23	Atotech
24	See ray
25	Lenovo

- **Objective:** Development and characterization of large panel fan out design, process and reliability in 2015, provide supply chain analysis and justification for commercialization



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Consortium Updates and Complimentary

NCAP has won the "Twelfth (2017) China Semiconductor Innovative Products and Technology" for "Integrated Large Panel Fan-out Advanced Packaging Technology".

Thanks to the supports of all the members of NCAP LPFO Consortium!

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Consortium Summary

Consortium
on Low Cost Panel Level Fan-out Technology Development

- 25 International Companies joined the Consortium
- Target single die fan-out (one layer RDL) development & demonstration (Phase 1)
- Establish design, simulation, process capability and panel level fan-out supply chain build up
- Complete single die fan-out lesson learnt and preliminary process & reliability qualification
- Drive low cost solutions & commercialization
- Establish panel level fan-out technology Industry chain embryonic in China

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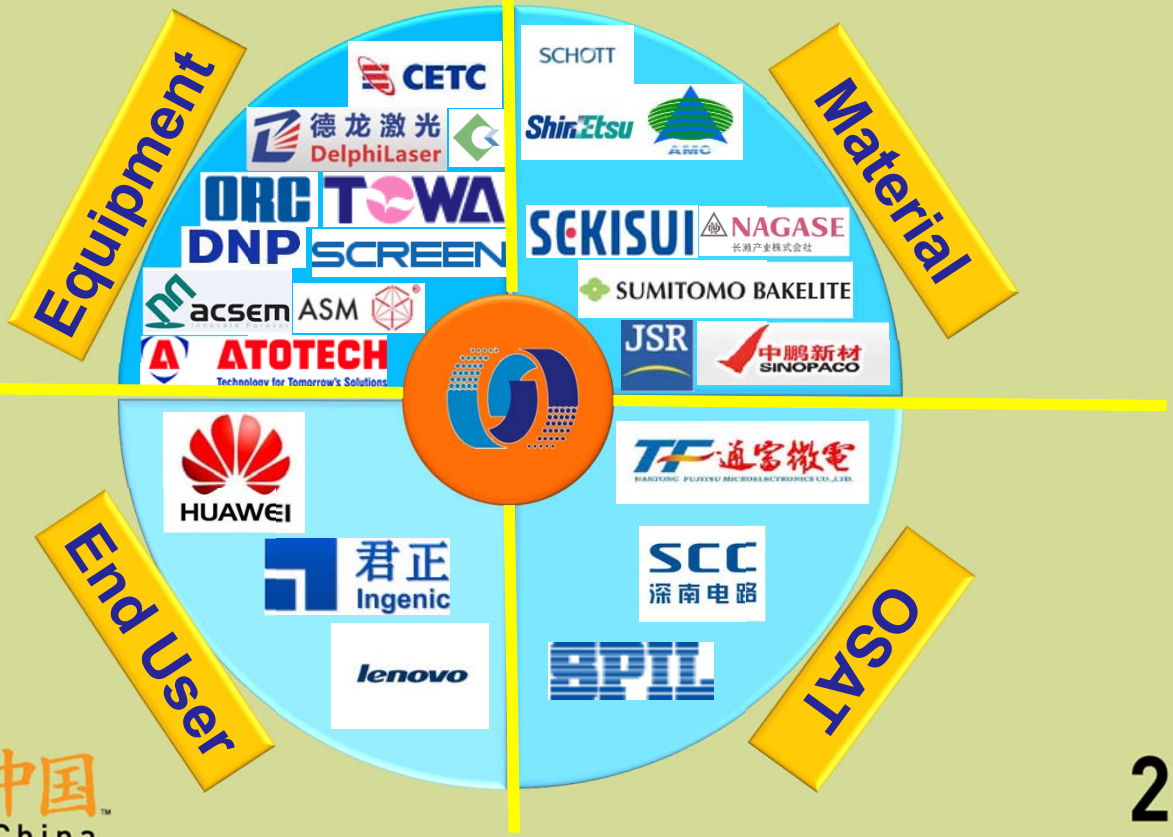
Consortium Structure

Membership fee: US$20K
Paying members :15 companies
Supporting members: 10 companies



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Die First Process Characterization

Die First Process

Lamination

Die Attach

Molding

2nd Bonding

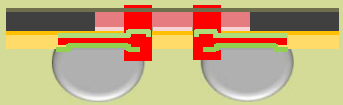
RDL

UBM

Ball Drop

Testing

Package structure



Package size: 8.9 x 7.7 mm RDL: 1 layer RDL Line/Space: 20/20μm Ball Pad Size: 250 μm Ball Pad PI Open: 230 μm Die sizes: 5.24 x 4.835mm Die pad pitch: 96 μm Die thickness: 200 μm Die Pad PIO: 65x65 μm Die Pad Qty.: 207	**Key Benefits** • Have advantage of easier process • Thinner than flip chip package (no substrate) • Support increased I/O density • Excellent electrical and thermal performance • Excellent high temperature warpage performance • Fine line & space • Panel level molding process • Establishing panel level fan out industrial base

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Die Last Process Characterization

- Die Last Process
- Substrate Pattern
- Substrate Surface Finishing
- Temporary Bonding
- Flip Chip
- Panel Molding
- Singulation
- Ball Drop
- Testing

Package structure

Package size: 8 x 8 mm
Package ball Qty : 185
Substrate Line: 1 layer
Line/Space: 30/30um

Die sizes: 6 x 6 mm
Die pad pitch: 200 µm
Die Thickness: 150 µm
Cu pillar height : 70um
Copper pillar Qty.: 203

Key Benefits

- Utilizes a Low Cost FC Coreless Substrate
- Panel processing (low cost)
- No FO Wafer Fab Investment needed, can use existing Flip Chip Packaging manufacturing lines
- Fan-Out Packages with low thickness
- Design based on flip chip die
- Test as module as usual
- Establishing panel level fan out industrial base

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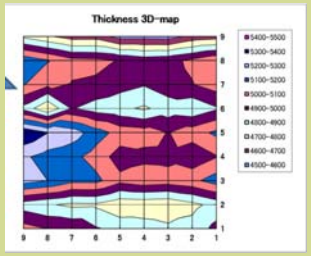
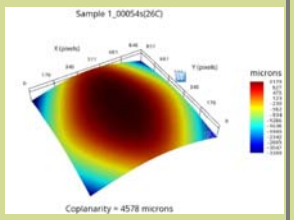
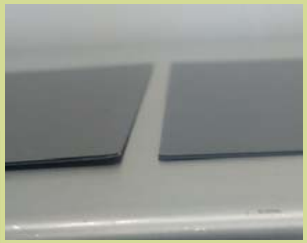
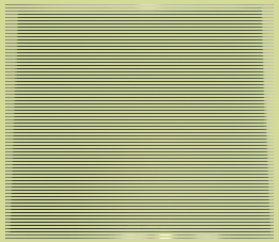
Major Results Sharing

Die First Process

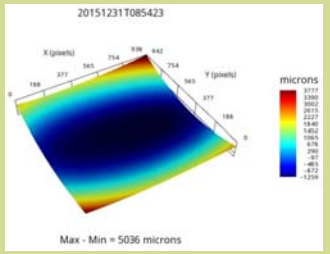


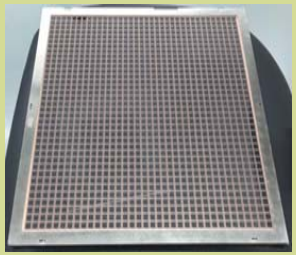


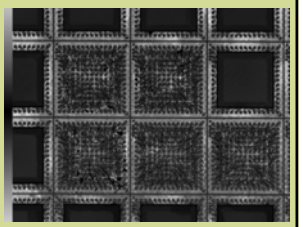


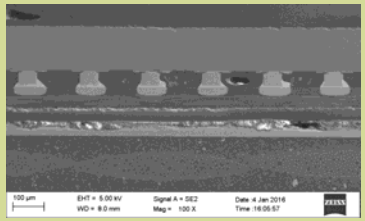


Die Last Process









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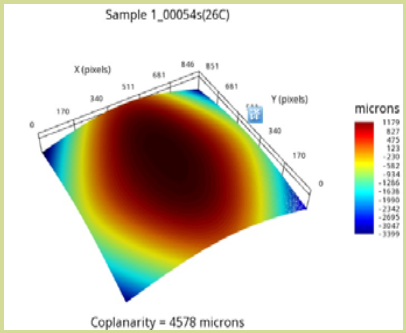
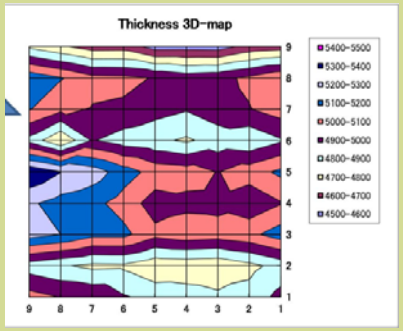
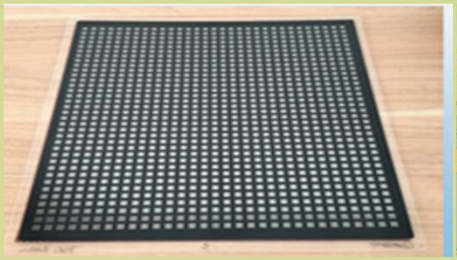
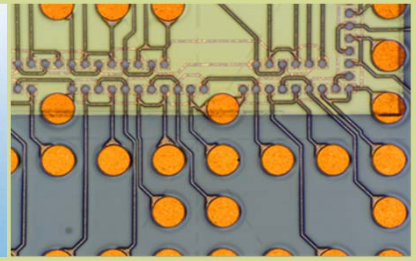
Major Results Sharing

Die First Process

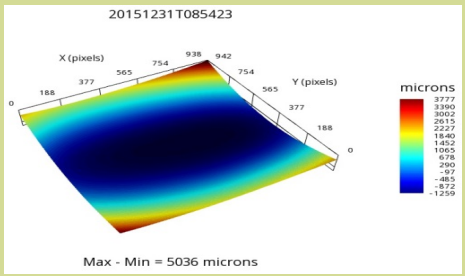


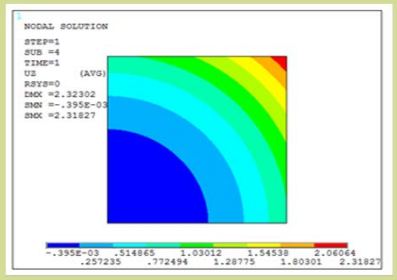


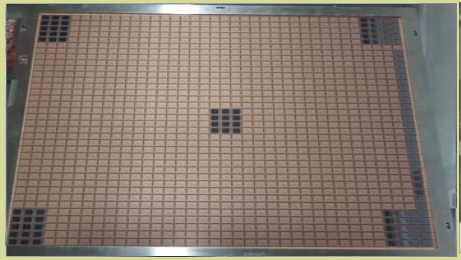


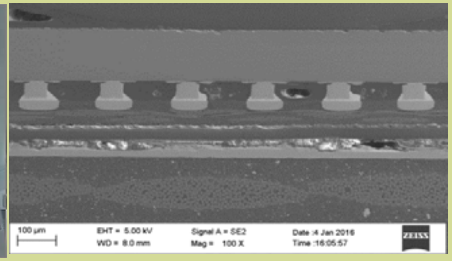


Die Last Process









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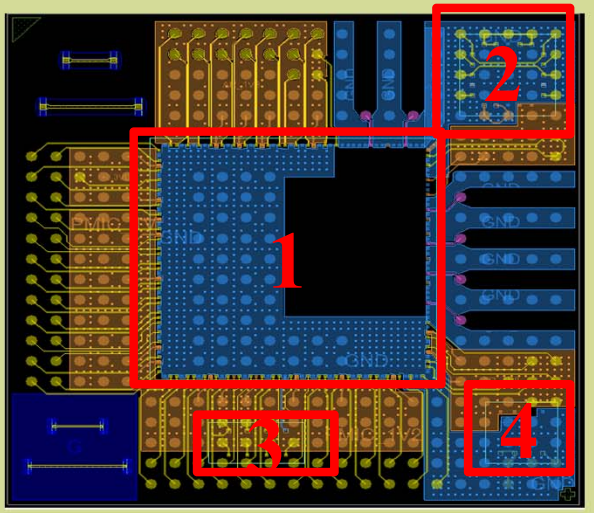
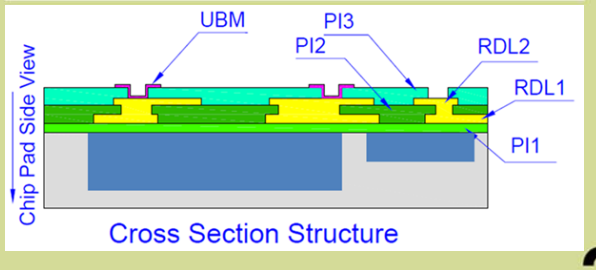
The Design Of NCAP Phase Ⅱ FOPLP Consortium

No.	1	2	3	4
Chip Type	MMIC	LDO 02	Flash	LDO 01
Size (mm)	6*6	2*2	2*1	1.5*1.5

- Panel Size: 600mmX600mm
- Package Size:12mmX12mm
- Min. Line Width/Space:10um/10um
- Min Chip to Chip Space: 200um
- Integrated Chips Count: 4
- Solder Ball Counts: >300
- RDL Layers: 2 Layers





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Future Major Works to Be Done in GD

1. Establishing large panel fan out engineering line and promote domestic equipment capability build up

In the next one year, large panel fan out line will be built up; some critical equipment will be built up, like die bonding, plating, PVD, de-bonding equipment;

2. Equipment and Material Evaluation and Verification

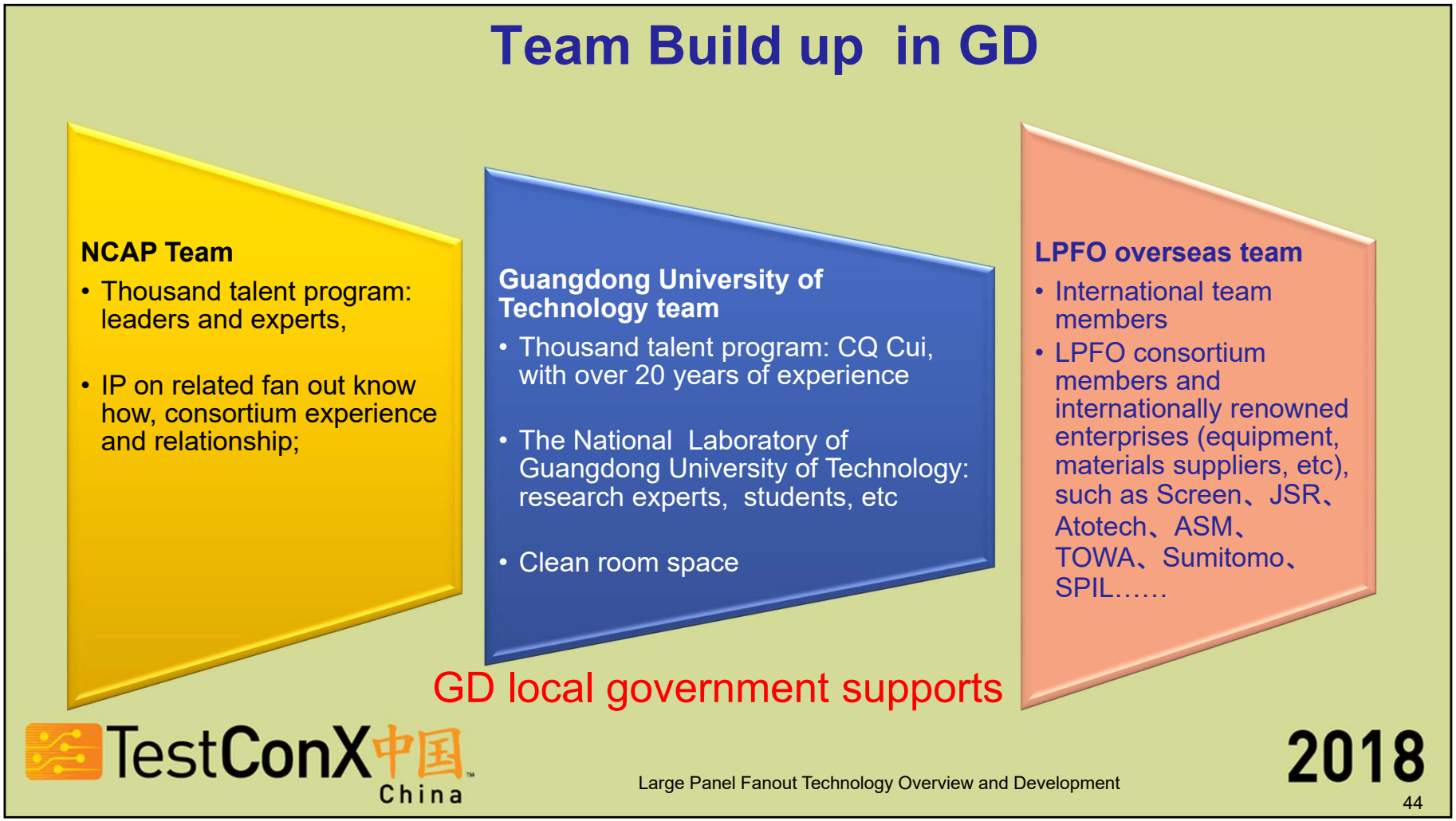
Critical panel level fan out equipment and material will be evaluated and verified;

3. Become partnership with GD semiconductor packaging equipment

a. Work together and develop new equipment together;

b. Provide engineering service to important customers;

c. Provide training centre for universities and institute.


Team Build up in GD
NCAP Team
• Thousand talent program: leaders and experts,
• IP on related fan out know how, consortium experience and relationship;
Guangdong University of Technology team
• Thousand talent program: CQ Cui, with over 20 years of experience
• The National Laboratory of Guangdong University of Technology: research experts, students, etc
• Clean room space
LPFO overseas team
• International team members
• LPFO consortium members and internationally renowned enterprises (equipment, materials suppliers, etc), such as Screen、JSR、Atotech、ASM、TOWA、Sumitomo、SPIL……
GD local government supports
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Conclusions

1. Fan out technologies are commercialized in the major forms of eWLB, RCP, InFO, and other mixed technologies.
2. The market will be booming for fan out especially after Apple iPhone 7 was using InFO technologies. LPFO will be commercialized soon.
3. NCAP has established WLP Fan out and LPFO capability and pass relevant reliability test. LPFO engineering lines will be in GD province.
4. FoZhixin microelectronics Pte Ltd will be a critical window in GD province to show LPFO equipment capability and becoming solution providers.

Acknowledgements

1. Thanks to NCAP 02 National Project supports, which support basic research and commercialized packaging environment build up.
2. Thanks to NCAP LPFO Consortium and provide huge process and reliability assessment, especially thanks to contributions of 25 key members of consortium .
3. Appreciate NCAP senior leadership team and their vision on LPFO.
4. Appreciate GDUT leaders to supports the LPFO engineering lines build up in GD.