Optimizing HV Capacitor Bank Design, Protection, and Testing

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Abstract - This paper will discuss in detail a capacitor bank protection and control scheme for >100kV systems that are in successful operation today. Including its implementation and testing on a configurable and scalable substation IED that incorporates all the necessary advanced protection and logic control functions.

Index Terms— Protection, capacitor bank, testing, relay

1. Introduction

Many utilities use shunt capacitor banks to regulate HV substation bus voltages over a range of light to heavy load and load switching conditions. For flexible VAR control, the substation capacitor bank configuration may consist of up to 6 separately switched capacitor stacks. The entire substation bank is typically switched with a circuit breaker. The voltage level is monitored and used to switch in and out three-phase capacitor stacks as required for correct VAR compensation so the bus voltage is regulated within a defined bandwidth around the targeted nominal bus voltage. Optimally there are two operating band widths that are used depending on load conditions, narrow band (NB) and wide band (WB). The number of capacitor bank stacks and bandwidths would be determined by System Operations and Planning. Capacitor stack switching is either done manually or automatically. Automatic control however must address several issues. Some of these are: 1) hunting – trying to find a stable voltage within an operating bandwidth, 2) bandwidth operation transfer 3) automatic to manual transfer, and 4) balanced switching operations of up to six capacitor bank circuit switchers over the life of the bank.

In addition to control, a number of protection functions are also required. Each three phase stack is protected with sensitive phase voltage unbalance (60) functions, which allows isolation of the faulted stack by operating the respective circuit switcher. Phase and ground overcurrent functions are provided that operate the circuit breaker for overall capacitor bus and bank faults.

Testing of this type of system requires identifying the key functions of the protection and control design where each function can be proven using test cases that can be accomplished through IED scheme testing, commissioning, and routine testing.

2. General Considerations

Although many capacitor banks are single stack design, and therefore only employ a single switch control like the main circuit breaker (PCB), due to evolving operational requirements of today's modern grid, utilities will in future require multi-switched stacks for flexible VAR control. For either design, the protection requirements are basically the same with the variable being the bank configuration and the number of capacitor stacks used. The following cap bank protection and control functions are typically found and would require testing:

- Primary voltage unbalance protection for each capacitor stack. (60)
- Adaptive phase (50/51) overcurrent protection for the capacitor bus and capacitor bank, including negative sequence overcurrent (51Q) protection.
- Earth-fault (50/51N) overcurrent protection for the capacitor bus and bank.
- Sensitive ground time overcurrent protection (64) supervised by a 3V0 (59N) element measuring the bus voltage which provides backup protection for each stack.
- Breaker failure protection of the main disconnect device. (50BF/62BF)
- Local manual trip and close control of the circuit breaker and capacitor switches when operators are on site.
- Remote manual trip and close control of the circuit breaker and capacitor switches.
- Local automatic control consisting of WB and NB voltage control. (27/59) This would also allow the local operator to select WB or NB control for manual operations.

- Remote automatic control consisting of WB and NB voltage control. This would also allow the dispatcher to select WB or NB control.
- Operation equalization between the capacitor switches over the life of the bank. (Counter)
- Detect and control capacitor bank hunting when the control is in the automatic mode.
- Engineered safety features consistent with the utilities' operating philosophy including man-machine interface standards, lockout / tag out, and maintenance requirements.

An example of a full implementation of all these features are illustrated in Figure 1.

3. IED Testing Procedures

To establish the testing procedures for this application each function's role and typical set point will be described along with a common test procedure. To simplify the process, we will assume a single stack is used (CS1 closed) and all others are open and not used. However for a complete commissioning of Figure 1 the adapted 50/51 phase settings would also require testing for each stack being in service.

Safety is top priority, always follow the site safety rules, all lockout/tag out procedures, and recommendations from the manufacturers. Isolate the IED to be tested paying close attention to the Trip, DC control, and CT/VT circuits. Read the IED label for its power supply requirements and use the correct source to power it in the panel or on the bench.

The beginning of any IED test procedure should start with a meter check of the IED's signal processing. For this case, we want to validate the currents and voltages being monitored for accuracy. We also want to verify magnitude, phase angle, correct phase connections to the IED, and used CT/VT ratios.

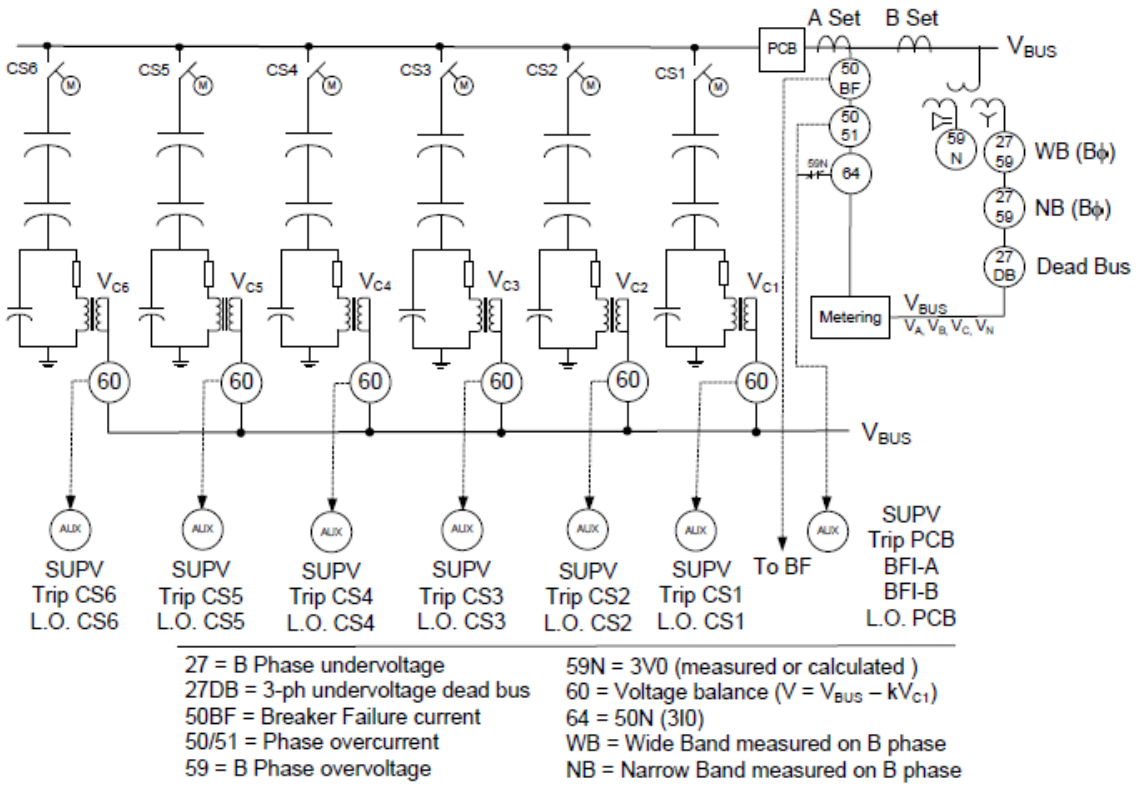

Figure 1 - Six Stack Capacitor Bank Protection and Control Scheme

Table 1 - System Settings

System Bus Voltage	164kV Ph-Ph
VT Ratio	1400:1 (94.69kV Ph-G / 67.63V Ph-G)
CT Ratio	120:1 (600:5)
Grounded Wye Bank (27MVAR)	3 parallel strings x 5 units / 9 groups per can (19.92kV, 600kVAR /can)
Low Voltage Capacitor (VC1)	0.83kV, 167kVAR

*Calculations for the protection elements are given in Appendix A.

For the purpose of this example we will use the following parameters* in Table 1:

4. Protection Elements

Two main areas of redundant protection are provided for in the IED. The first area is the protection of the individual capacitor stacks in Figure 1. This consists of using the capacitor stack neutral voltage per phase measured across a low voltage capacitor (VC1 - VC6) and comparing it on a phase-by-phase basis to the nominal 164kV bus voltage (VA, VB, VC) in a voltage balance function, device 60V. This method provides a very sensitive element that can be adjusted when commissioned to detect individual capacitor element failures per system operations requirements. A second device 60V high set element with a very short time delay will detect and trip for gross unbalances such as rack-to-rack faults in the associated stack.

The second area of protection is the capacitor bus and capacitor bank, including breaker failure protection for the PCB, and backup protection for stack failures. The capacitor bus and bank are protected by phase 50/51 elements to detect phase faults. Earth fault protection is provided by an instantaneous element, device 50N, and a sensitive ground element, device 64N (51N+59N).

5. Procedure for Testing Protection Elements

Unbalance protection: The type of the capacitor unit composing the bank and the bank configuration itself affects the sensitivity requirements set on the unbalance protection. The unbalance protection should be coordinated with the individual capacitor unit or unit fuses (internal or external) so that the fuses operate to isolate the faulty capacitor unit before the protection trips the whole bank. In our case it will selectively alarm and trip the capacitor stack based on the number of failed element groups. (CS1-CS6)

The alarm level (~105% rated voltage) is selected ideally with the first blown fuse (or open/shorted element) giving an early warning of a potential stack failure. The delayed trip level is based on the loss of additional capacitor elements that cause a group overvoltage in excess of 110% of the capacitor unit rated voltage in accordance with IEEE Std. 18 [3]. In case of cascading failure or an arcing fault within the bank, the application of an additional high-set stage operating in minimum time is recommended to minimize damage to the overall bank. (see Appendix A for details)

Testing the 60V function is executed with a balanced 3-phase source for Vbus applied and then compared phase to phase to the cap bank voltage Vc1. The Vdiff is calculated each cycle and can be tested by a fine ramp of Vc1 to the target setpoint (Source 2 with time delay) for each element. The ramp is just over 1V for the Vdiff target in the 60V elements used. Operations can be observed in the live target monitor, via GOOSE if used, or by direct output if mapped.

Phase Overcurrent (Overload) Protection (50/51): The SCB may be subjected to overvoltage resulting from combined fundamental and harmonic content. This overvoltage increases the load current drawn by the SCB and stresses the layers of film that compose the individual capacitor elements. This kind of capacitor element is sensitive to the peak voltage across it, so the peak voltage measurement principle is preferred over RMS measurement when implementing the protection.

Table 2 - Unbalance Protection Settings

Element	Setpoint Vdiff	Source 1	Source 2	Error	VT Ratio
60 Alarm	2.3% Vbase (0.2s)	3Ph 67.7V	3Ph 69.2V (~6V diff)	+/- 0.05%	1400:1
60 Timed Trip	2.5% Vbase (1.0s)	3Ph 67.7V	3Ph 69.35V (~12V diff)	+/- 0.05%	1400:1
60 Inst	5% Vbase (0.05s)	3Ph 67.7V	3Ph (~20V)	+/- 0.05%	1400:1

If the stress exceeds the SCB capability [2, 3], the bank should be removed from service. Protection based on sensitive direct differential voltage measurement is best, but a current-based overload protection with suitable current input filtering can be used as well. This is an advantage, since current based protection can be implemented economically and/or provide complementary backup protection to the SCB with voltage differential protection.

Testing is typical current injection and time measurement for these elements. These can be definite time or may use inverse curves that coordinate with the SCB capability. (see Figure 4 Appendix A) For this example the Ipu is 86A primary current for the CS1 bank, using the 120:1 CT ratio the secondary pickup targets would be 0.86A, 0.97A, and 2.2A respectively in the table.

Negative Sequence Overcurrent (51Q): If the phases of the bank are constructed in distinct separate structures, a flashover within the capacitor bank will begin as a short circuit fault over of a single-series group. Such a fault produces very little phase overcurrent. For this type of fault, fast protection is provided by the unbalance protection. However, depending on the applied scheme and the fault type, the unbalance current may be out of the normal reliable operating range of the unbalance protection. (60V or 51/50P) For example, if a flashover occurs across the entire limb, the current in the neutral connection can be very high. Also for certain capacitor bank configurations, some faults within the bank will not cause an unbalance signal and will remain undetected, for example rack-to-rack faults for banks with two-series groups connected phase-over-phase and using neutral voltage or current for unbalance protection, and rack-to-rack faults for certain H-bridge connections. Therefore, if the unbalance protection fails to operate, the initial fault may spread until it becomes severe enough to operate the short circuit protection resulting in considerable damage. For these reasons, a backup protection for the unbalance protection is recommended. The negative-sequence overcurrent protection can be used for this purpose to complement the scheme and provide tripping in the above cases.

Table 3 - Overload Protection Settings (1 stack CS1)

Element	Setpoint (Sec)	Time Delay	Source (I)	Error	CT Ratio
51Phase Alarm	1.2xIpu	50-100s	3Ph	+/- 3%	120:1
51Phase Trip	1.35xIpu	1.0-3.0s	3Ph	+/- 3%	120:1
50Phase Trip	3xIpu	0.01s	3Ph	+/- 5%	120:1

If used per IEEE Std. 18, this setting would be 10% of the primary SCB current. For this example, it would be 8.6A primary and in secondary current that would be 72mA. Depending on the natural unbalance of the bank, (measured at time of commissioning) this may not be feasible to implement with only the CS1 bank in service. It is recommended that this element not be enabled until the set point would exceed 2A secondary or the external system unbalance calculation – whichever is greater.

Testing the 51Q element can be performed in two ways: the recommended method is to begin the injection with a balanced 3-Ph current system, then ramp the system to an unbalanced state with no zero sequence until the target is reached. The least recommended method is to swap the A & C phase currents to the relay creating a pure negative sequence system and ramp it to the target setting. The reason this method is not recommended for modern IEDs: dependent elements and logic will be defeated and the 51Q will need to be isolated for testing. (Unless a test GOOSE is utilized, which is the recommendation for all complex systems.)

Earth Fault Overcurrent (50N): An earth-fault within the cap bank manifests itself in the unbalance current of the bank. In this sense, the unbalance protection provides a backup protection for the earth-fault event. In effectively earthed systems with earthed wye SCBs, the unbalanced bank load current caused by an external system earth fault may be sufficient to cause the protection to start and trip the cap bank if the non-directional low-set stage is set too low. To prevent possible false tripping, the 50N current setting is typically selected above the capacitor phase current. However, using the 59N element to supervise the 50N provides a means to set the 50N much more sensitive as a 64N protection.

The 50N can be typically tested by injecting a single phase current and monitoring its output with respect to the time delay. The 64N is tested by adding 3Ph balanced voltage to the 50N injection, the result should be an accelerated trip based on the 3V0 permissive.

Breaker Failure Protection (50BF): Breaker failure protection (50BF) is initiated from the protection trip command, either from internal protection functions or from external protection devices via binary input. This signal will initiate the 50BF back-up trip timer. If the opening of the breaker is successful by detection of low RMS current (with a special adapted current algorithm) or by 52a open contact indication or both, the timer is reset and no breaker failure trip is issued. If the current and/or contact detection has not detected breaker opening before the back-up timer has expired a back-up trip is initiated.

To test the 50BF inject a current greater than the pickup setting, and observe the element output, and/or initiate an overcurrent trip by injecting a suitable current and do not remove the current or change the 52a status for a time greater than the BF timer, a re-trip should occur.

Undervoltage or Undercurrent protection (27DB or 37): Once disconnected from the system, the SCB cannot be reconnected immediately due to the trapped charge within the capacitor units. Otherwise, catastrophic damage to the circuit breaker may occur. To discharge the bank, each individual capacitor unit has a resistor to discharge the trapped charge within 5 minutes. Undervoltage or undercurrent protection function with a time delay is used to detect the bank going out of service and prevent closing the breaker until the set time has elapsed. This delay prevents tripping of the bank for system faults external to the bank. The undervoltage or undercurrent function should be set so that it will not operate for voltages when the capacitor bank should remain in service. This application will only use the 27DB undervoltage (often called Dead Bus) function. Its use in the overall control scheme will be covered in the next section where the testing is defined.

This ends the description for testing the core protection functions, most of them are commonly used on cap bank protection schemes but will vary depending on the cap bank physical and electrical design. For typical cap banks this would be all required, but modern power grids require increasing levels of stability and control.

The remainder of this paper covers a specialized application where multi-stack cap banks can be switched and configured automatically based on the power system's changing requirements. The elements are used in the multi-stack control scheme for implementing the variable VAR application (Figure 1) which is covered in detail and includes the basic test cases for its implementation.

Table 4 - Other Current Protection Settings (1 stack CS1)

Element	Setpoint (Sec)	Time Delay	Source (I)	Error	CT Ratio
50N	50% of 51P Setpoint	100s	1Ph	+/- 3%	120:1
64N	50N + 59N	2s	1Ph (+3PhV)	+/- 3%	120:1
50BF	10% x Ibase	0.0s / 0.3s	1Ph or 3Ph	+/- 5%	120:1

6. Variable VAR Application

Voltage measuring elements are connected phase-to-ground and have an accuracy of better than 0.05%. Outputs of the voltage measuring elements assert or de-assert to provide the automatic control for the WB (wide band) raise and lower (27WB, 59WB) and NB (narrow band) raise and lower (27NB, 59NB) operating actions. During a forced outage such as a storm, we do not want the automatic control to mistake a “dead” bus as a “low” bus voltage condition and to stage all the capacitors ON. Upon reenergizing, the bus voltage might become quite high, therefore, dead bus detection (27DB) is provided. The 27DB undervoltage dead bus detection specifically disables stack switching (CS) operations when the circuit breaker (PCB) is opened or the bus voltage is below 70% on all phases for a sustained period.

(Application Note: It is important to note that voltage element measuring accuracy is very important in high voltage applications such as these. (Taking Vpri=164kV ph-ph) When the raise and lower voltage settings are only a few kV apart, for example 163kV for raise and 165kV for lower, and the voltage transformer ratio is 1400:1, this leaves us measuring secondary voltages of 67.22V and 68.04V, respectively; a difference of less than 1.0 volt. (The relay must be able to accurately and reliably discriminate between two secondary voltages that may be less than a volt difference.)

The elements/set points to be tested are:

Table 5 - Voltage Elements Settings

Element	Setpoint (Vpri L-L)	Source	Error	VT Ratio	Vsec L-N
27DB (Dead Bus)	<70% Vpri (115kV)	3-Ph	+/- 0.1%	1400	47.43
27WB	<2% Vpri (161kV)	B-Ph only	+/- 0.05%	1400	66.40
27NB	<0.75% VPri (163kV)	B-Ph only	+/- 0.05%	1400	67.22
59NB	>0.75% Vpri (165kV)	B-Ph only	+/- 0.05%	1400	68.02
59WB	>2% Vpri (168kV)	B-Ph only	+/- 0.05%	1400	69.28

Since these voltage elements are used for close/open control of the circuit switchers of the capacitor stacks, the control timers for each function would require testing. The control timer settings are:

Table 6 - Voltage Elements Control Timers

Function	Seconds / (Default)
59WB Time	15 – 30 / (15.0)
27WB Time*2	15 – 30 / (15.0)
NB to WB Transfer Timer*1	15 - 30/ (15.0)
WB Hunting Timer O-C-O / C-O-C	Minimum of 2.25 x 59WB Timer / (34)

Function	Seconds / (Default)
59NB Time	60 – 120 / (60.0)
27NB Time	60 – 120 / (60.0)
NB Hunting Timer O-C-O / C-O-C	Minimum of 2.25 x 59NB Timer / (135)
Capacitor Switch # Just Opened Block Close Time	100-300 / (300.0)

As a working example, the following Band Control definition will be used. The nominal primary bus voltage will be 164kV with a narrow band (NB) of 163kV to 165kV and a wide band (WB) of 161kV to 168kV as shown in Figure 2.

NB operation is set when expected load switching will be small and insertion or removal of capacitor stacks will regulate the voltage back into the NB region with stable operation (Figure 3) until the next load change. If automatic operation is set to NB, no regulation (bank switching) is attempted while operating within the NB region. If there is a voltage excursion below the 27NB setting for a set time, NB Time (typically 60 to 120 seconds), then the next [in sequence] capacitor stack CS is closed and the NB timer is reset.

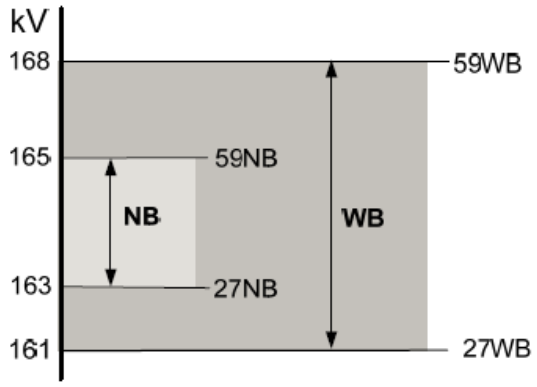

Figure 2 - Example NB and WB voltage level band control

If 27NB is still asserted for another period of NB time then the next CS is closed. This process is repeated until the voltage stabilizes within the NB region as expected or all the banks are closed.

Similarly, the opposite control occurs if the voltage exceeds the NB region and the next in sequence capacitor stack CS is opened. The sequence continues until all are open or the voltage stabilizes.

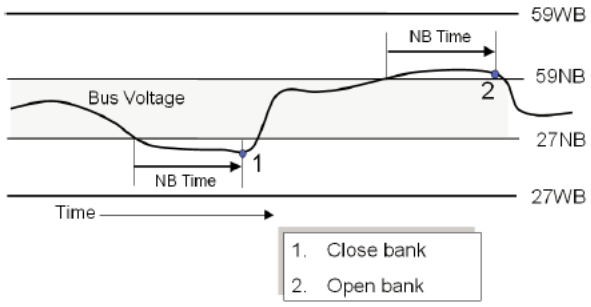

Figure 3 - Normal NB Operation

If, while set to NB operation, the voltage drops below the 27WB setting for a period equal to the NB to WB Transfer Time, then the band operation is automatically switched to WB (Figure 4) and uses the WB timer settings. The NB to WB Transfer feature was provided to allow the control to quickly respond to major system voltage excursions by switching to WB and using the shorter WB time delays.

Wide band (WB) operation is identical to the NB operation only using the shorter delays to normalize the voltage quicker. A condition known as hunting can occur when the voltage cannot stabilize within the band it is operating.

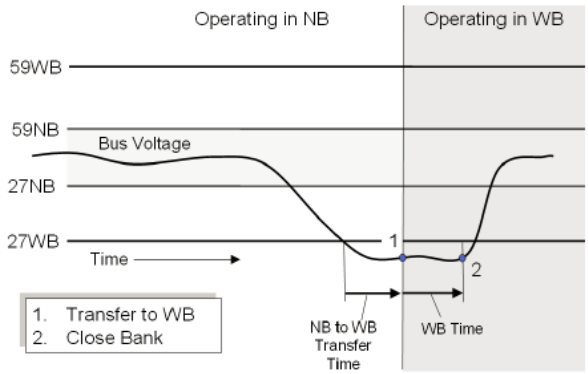

Figure 4 - NB to WB Transfer Operation

So hunting logic is designed to detect the O-C-O or C-O-C sequences within a certain time period. Depending on the operating band in use, different responses are employed.

For NB hunting detected the control is switched to WB, if already in WB and hunting is detected then it is switched from Auto to Manual control. (Figure 5)

Procedure for Testing NB and WB Voltage Levels

1. Set Auto/Manual control to MAN.
2. Using Table 1 as a reference set the primary NB and WB voltage 27 and 59 limits.
3. Apply a balanced three-phase secondary voltage level of nominal voltage, 67.6 V secondary and check primary value on front panel LCD.
4. Increment the 3-Ph voltage level up in 0.1 V steps until 59NB operates.
5. Increase further until 59WB operation is indicated
6. Increment the voltage level down and observe dropout of 59WB and 59NB.
7. Reset the secondary voltage level to nominal voltage, 67.6 V.
8. Increment the 3-Ph voltage level down in 0.1 V step until 27NB operates.
9. Decrease the voltage further until 27WB operation is indicated
10. Increment the voltage level up and observe dropout of 27WB and 27NB.
11. Record and compare to the values of Table 1

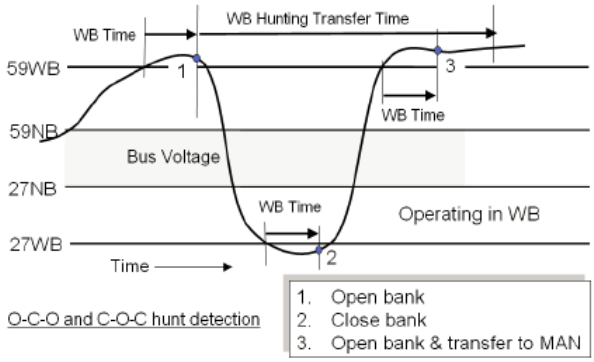

Figure 5 - WB Hunting and Transfer to Manual Operation

Set Auto/Manual operation to AUTO and 43 Band to NB. Using the following sequence (Table 7) the NB operation was tested and operations observed. There was no NB to WB transferring – 43B Band was still in NB. There were two CS open and one CS close operations.

The observed virtual switch positions were Auto/Manual operation on AUTO and 43 Band on NB. Using the following sequence (Table 8) the NB to WB transfer was tested. NB to WB transfer could be observed on the 43 Band virtual switch icon, the setting label will change from NB to WB. There was a NB to WB transfer followed by a close CS operation. The 43 Band switch was left in WB.

The observed virtual switch positions were Auto/Manual operation on AUTO and 43 Band on WB. The 43Band switch was then reset to NB. Using the following test sequence (Table 9) NB hunting and transfer to WB operation were tested. There was a NB to WB transfer – 43B Band was changed from NB to WB. There were two CS close and one CS open operations. The close-open-close operation within the NB Hunt Time established the hunting condition.

Similar sequences can be used to test and verify all permutations of the control scheme operations for NB and WB control. A suitable test plan for acceptance testing of a new IED should be prepared and used as a baseline. A subset of this test plan would be appropriate for a routine/maintenance test. A commissioning test should contain relevant test cases to prove all in service and used settings.

Table 7 - Example of NB Operation Testing

	State 1	State 2	State 3	State 4
Sec. Voltage	Nominal	59NB level + 0.5	Nominal	27NB level – 0.5
Duration – Sec.	5	59NB Time + 0.5	1.1 X NB Hunt Time	27NB Time + 0.5
Operation		CS opened		CS Closed
	State 5	**State 6**	**State 7**	
Sec. Voltage	Nominal	59NB level + 0.5	Nominal	
Duration - Sec.	1.1 X NB Hunt Time	59NB Time + 0.5	5	
Operation		CS opened		

Table 8 - Example of NB to WB Transfer Testing

	State 1	State 2	State 3	State 4
Sec. Voltage	Nominal	27WB level - 0.5	27WB level - 0.5	Nominal
Duration – Sec.	5	NB-WB Transfer Time + 0.2	27WB Time + 0.5	5
Operation		NB to WB transfer	CS closed	

Table 9 - Example of NB Hunting and Transfer to WB Testing

	State 1	State 2	State 3	State 4
Sec. Voltage	Nominal	27NB level - 0.5	Nominal	59NB level + 0.5
Duration – Sec.	5	27NB Time + 0.5	0.5	59NB Time + 0.5
Operation		CS closed		CS opened
	State 5	**State 6**	**State 7**	
Sec. Voltage	Nominal	27NB level - 0.5	Nominal	
Duration - Sec.	0.5	27NB Time + 0.5	5	
Operation		CS closed		

7. When the Cap Bank Trips

Once commissioned the cap bank protection should perform correctly, providing secure operations during switching, restraint for external faults, and a high sensitively for internal faults. Having a good protection scheme is only half the solution though, the IED should be setup to record all switching events and protection operations. This is necessary to evaluate the cause of any future event, especially if it is an internal fault. When an operation does occur, the ability to know which phase of which stack had the failure is very valuable to trouble-shooting the problem in the field. A custom event report or log can also be provided for that purpose from the disturbance and event recorder.

To find the failed capacitor can(s) in the bank a method of direct injection [4] has been shown to be the easiest and quickest method. With the bank properly isolated and depending on the bank configuration and rating, injecting a voltage of 500-1000V across the suspect stack allows one to measure with a voltmeter the voltage and with a clamp on meter the current in each capacitor can. The injected voltage will be divided by the number of cans in the injected string equally. The cans with failed elements will measure a different current value than the good can(s). More information on the capacitor's health can be determined from these measurements and is a recommended practice for routine maintenance of cap banks.

8. Conclusions

This scheme is easily scalable from 2-6 stacks by simply installing the required capacitor stacks and associated protection equipment. If, for example, a capacitor bank required only four stacks, then only the equipment and wiring for stacks 1 through 4 would be installed. This method seems obvious, however, one fact that is not so obvious is that contained in the standard six bank configuration logic are six logic gates whose outputs can be easily controlled by a setting of "Disable" to remove the banks from the control scheme. In this example we would de-assert banks 5 & 6 logic gates such that the control would ignore them since they are not installed. This makes the application scalable with a standardized control interface and HMI implementation.

This paper covers the fundamental protection elements used in typical capacitor bank applications, although there are many possible cap bank configurations, the principles for cap bank protection are the same. Specifically, a grounded wye fuse less bank configuration was used to demonstrate the protection functions and general test procedures. Calculations were provided to show the process of arriving at each protection setting, however this is an example only, and not all issues can be covered. It is recommended that both IEEE Std. 18 and IEEE C37.99 be thoroughly read and understood when looking at any specific cap bank protection scheme. Further, each IED manufacturer incorporates different levels of integrated protection functions and require a good understanding of their specific use. Testing is always recommended for a deeper understanding.

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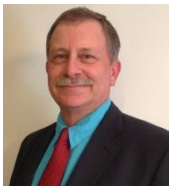
BIOGRAPHY



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APPENDIX A

[Example Calculations]

Example: A grounded Wye capacitor bank (could be fuse less or internally fused) connected to a 164kV bus. The bank consists of three parallel strings of five 19.92kV, 600kVAR units per phase with 9 groups per can for a total CS1 stack size of 27MVAR. NOTE: If all six stacks were in use, the total bank size would be 162MVAR. (CT ratio 120:1; VT ratio 1400:1)

Calculate the unbalance Alarm and Trip values for the 60 element. (| Vbus – K * Vc1 |)

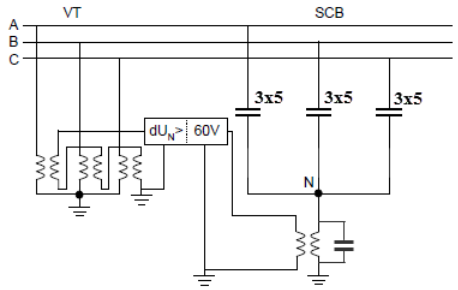

Figure 1

Cap Bank Unbalance Protection

For nominal operation

Calculate Vc1:	Zbank = $(19.92kV)^2$ / 600kVAR = 661.3 Ω	Eq 1
	Zvc1 = $(0.83kV)^2$ / 167kVAR = 4.13 Ω	Eq 2
	Iscb = Vbus/Zscb = (164kV/√3) / ((5 x 661.3) /3) + 4.13)Ω	Eq 3
	Iscb = 85.6A	
	Vc1 = 85.6A x 4.13Ω = 353V	
Calculate K:	K = Vbus L-N / Vc1 = (164kV/√3) / 353V = 268.2	

Vcan = voltage per group element: 19.92kV / 9 = 2096.3V

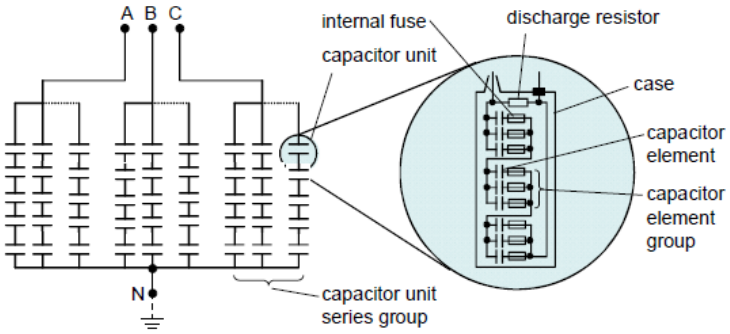

Figure 2

Capacitor Can Detail

Given an ideal system, the normal voltage differential (60) operate quantity would be zero. In order to determine proper alarm and trip points the individual element failure effects must be calculated. Using IEEE Std 18-2000 those recommended values would be 105% overvoltage for alarm and 110% overvoltage for trip.

The Alarm point would be: 1.05 x Vcan = 1.05 x 2096.3V = 2201.1V

The Trip point would be: 1.10 x Vcan = 1.10 x 2096.3V = 2305.9V

A simple calculation of # failed elements will give the respective change in Vc1.

Capacitor stack ZT(-1 group) $1 / Z_{T(-1)} = 1 / (5 \times 661.3) + 1 / (5 \times 661.3) + 1 / (4 \times 661.3)+(9-1)*(661.3/9)$

$Z_{T(-1)} = 1094\Omega$

New Z total $Zscb = Z_{T(-1)} + Zvc1 = 1094 + 4.13 = 1098.13\Omega$

New Vc1 $Vc1(-1) = ((164kV/\sqrt{3}) / 1098.13) \times 4.13 = 355.7V$

Using a spreadsheet the following table is easily produced.

Table 1

# failed elements	Vc1	Vcan
0	353.0	2096.3
1	355.7	2143.9
2	358.5	2193.7
3	361.4	2245.8
4	364.5	2300.5
5	367.7	2357.9
6	371.1	2418.3
7	374.6	2481.9
8	378.4	2548.8

Using the calculated alarm and trip levels for Vcan, we can find the closest match to Vc1 and the number of failed elements.

The Vc1 Alarm point would be: 358.5V (the 60 alarm would be set to 358.5 – 353.0 = 5.5V)

The Vc1 Trip point would be: 364.5V (the 60 trip would be set to 364.5 – 353.0 = 11.5V)

If a fast trip 60 element was desired, then an instantaneous trip using the 6th failed element value would give 371.1 – 353.0 = 18.1V

NOTE: a more sensitive alarm point could be used – the 1st failed element – using the 2.7V difference.

Short Circuit and Earth Fault Protection

Overload element settings are also defined by IEEE Std 18-2002; for grounded banks overload protection is set to 135% of nominal current and negative sequence protection typically 10%. Both with suitable delays to coordinate with surrounding protection schemes.

For this case (CS1 only):

51 Phase Alarm is set to 102A,	(i.e. 85.6A x 1.20)	TD=100s
51 Phase is set to 115A,	(i.e. 85.6A x 1.35)	TD=1.0s
50 Phase is set to 460A	(i.e. 3x 51Phase)	TD=0.01s

The operate times should coordinate with the overload limits of the SCB (Figure 3 & 4), these are typically provided by the manufacturer of the capacitors. Figure 4 shows these SCB overload points plotted for comparison. Overload alarm is set to 120% of phase setting and the trip at 135%.

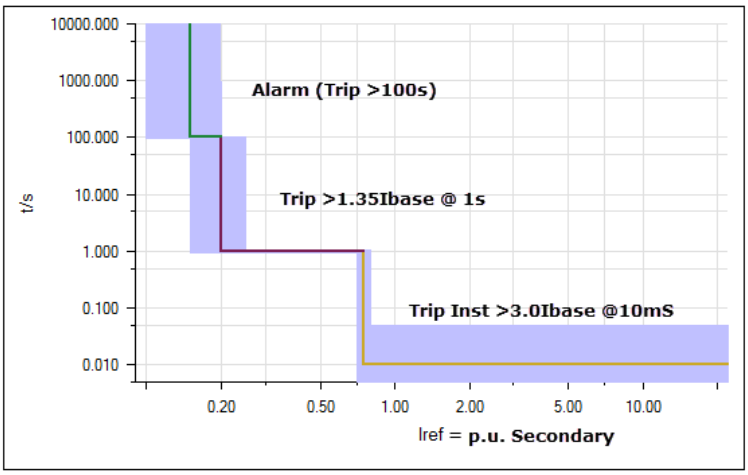

Figure 3

Coordinate definite time elements to SCB overload capability

High-set stages, if applied, should be set high enough to override inrush or outrush transient currents. Successful operation may be obtained by setting the high-set overcurrent stages at three to four times the capacitor rated current to override back-to-back bank switching. An earth-fault within the bank manifests itself also in the unbalance current of the bank. In this sense, the unbalance protection provides backup protection for the earth-fault protection. In effectively earthed systems with earthed wye SCBs, the unbalanced bank load current caused by an external earth fault may be sufficient to cause the protection to start and trip the bank if the non-directional low-set stage is set too low. To prevent a possible false tripping, the current setting is typically selected above the capacitor phase current.

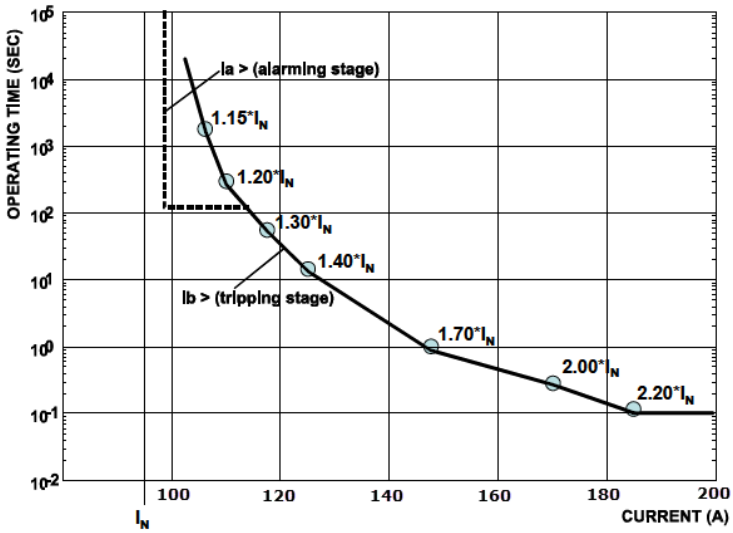

Figure 4

Overload capability characteristic of the SCB

The Negative Sequence Overcurrent protection can be typically set at 10% [3] of the nominal phase current of the SCB.

If used – the 51Q in our case would be set to 8.5A Primary (i.e. 85.6 x 0.1)

The sensitive ground time overcurrent element, 64 (50N), is unique in that it is supervised by a normally closed 59N element that measures the 3V0 on the supply bus which for balanced conditions would be zero voltage. The 50N+59N combination is looking for minor unbalances in the whole capacitor bank. Such unbalances produce little or no 3V0. This combination allows the 50N element to be quite sensitive and it can be set to pick up just above the standing unbalance of the bank. (NOTE: 59N however should be set to assert for external faults and unbalances.)

The 59N element can be set at 3-5% system voltage unbalance unless wider fluctuations are expected due to local switching. At the VT secondary this would be 2V to 3.3V. Typical settings are 10-50%.

The 50N element can be set at the bank's measured standing unbalance, this is worst case about 50% of the unbalance alarm setting. For our example this would be about 4A which equates to 2 group failures from the 60 function calculation. However it is recommended to confirm this calculation by using the "measured" natural unbalance compensation found during commissioning rather than just the calculation.

Natural Unbalance Compensation

In practice, the unbalance current or voltage measured by the unbalance protection in case of a healthy SCB does not equal zero. Also loss of individual capacitor units or elements will result to somewhat different magnitudes of unbalance current or voltage as theoretically calculated based on the SCB design.

The reason for this is the primary and secondary unbalance, which exists more or less on all SCB installations. The primary unbalance is due to system voltage unbalance and capacitor manufacturing tolerance. Secondary unbalance errors are due to possible measurement inaccuracies of the measuring transformers and due to changes in capacitance resulting from temperature variation in the bank. The total natural unbalance error will be a vectorial sum of the primary and secondary unbalance.

The error may be in a direction to make the protection more insensitive or to cause a false operation. According to general recommendations, if the natural unbalance error approaches 50% of the required alarm setting, compensation should be provided in order to correctly alarm for the failure of one unit or

element group as specified. Figure 5 shows one implementation principle of the natural unbalance compensation. The phase current *IA* is used as a synchronizing input for the compensation function, which means that the natural unbalance currents can be compensated for both amplitude and phase angle. The natural unbalance phasor(s) are recorded during commissioning of the SCB by the IED including the unbalance protection function and then used for compensating the natural unbalance currents to zero level.

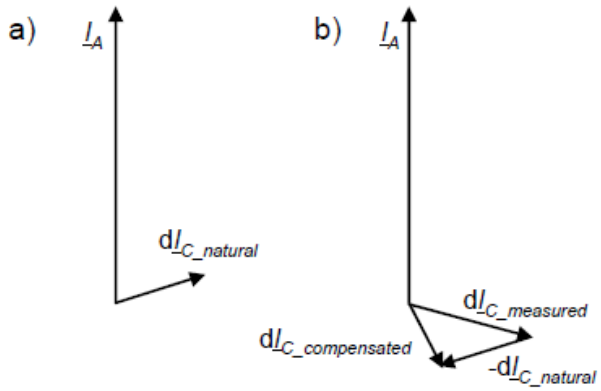

Figure 5

Principle of natural unbalance compensation for current based protection

When commissioning measures the compensation and those values used in the compensation settings, make sure the affected elements properly use them to avoid any misoperations of the sensitive protection functions.