Overlay control for nanoimprint lithography

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ABSTRACT

Nanoimprint lithography (NIL) is a promising technique for fine-patterning with a lower cost than other lithography techniques such as EUV or immersion with multi-patterning. NIL has the potential of "single" patterning for both line patterns and hole patterns with a half-pitch of less than 20nm. NIL tools for semiconductor manufacturing employ die-by-die alignment system with moiré fringe detection which gives alignment measurement accuracy of below 1nm.

In this paper we describe the evaluation results of NIL the overlay performance using an up-to-date NIL tool for 300mm wafer. We show the progress of both “NIL-to-NIL” and “NIL-to-optical tool” distortion matching techniques. From these analyses based on actual NIL overlay data, we discuss the possibility of NIL overlay evolution to realize an on-product overlay accuracy to 3nm and beyond.

Keywords: Nanoimprint lithography, Overlay, Alignment, Process control

1. INTRODUCTION

We develop nanoimprint lithography (NIL) as a low-cost patterning technology for semiconductor device manufacturing. NIL is a technique for fine pattern transfer from master plate (template) on Si wafers [1, 2]. Figure 1 shows an example of UV-NIL patterning flow and some SEM images of resist patterns obtained by UV-NIL. At first, resist drops are formed on the area to be imprinted on a Si wafer surface. Second, NIL template contacts the resist and the resist spread into grooves on the template surface. The alignment of the template and the wafer progresses just after the resist spreading. Third, the resist is exposed to UV light and cured. Fourth, the template is separated from the resist on the wafer and then the resist pattern is formed on the wafer. The same flow is repeated on another fields of the wafer.

NIL tools for 300mm Si wafer have a relatively simple structure, and do not have large components such as lasers, projection optics, or vacuum chambers. However, NIL has the potential of "single" patterning for both line patterns and hole patterns with a half-pitch of less than 20nm.

It has been pointed out that there are four issues for applying NIL into mass-production [3]. They are defectivity [4], overlay [5], throughput [6], and template infrastructure [7]. As for overlay, NIL employs die-by-die alignment with moiré fringe detection and an alignment measurement accuracy of below 1nm. An overlay accuracy of below 5nm has been reported.

Overlay accuracy of less than 3nm will be expected for chip manufacturing in around 2020. In order to qualify for the requirements from the semiconductor industry, more and more enhancements of NIL technology, such as an improvement in the overlay control accuracy for NIL-tool, image placement accuracy improvement for NIL templates and mix & match technique of NIL and other lithography tools such as an optical exposure tool, are needed. Figure 2 shows a roadmap for NIL overlay improvement toward 2020.

In this paper, the current NIL overlay status is described, and the development for mass-production of semiconductor device is discussed.

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Emerging Patterning Technologies, edited by Christopher Bencher, Proc. of SPIE Vol. 10144, 1014409 · © 2017 SPIE · CCC code: 0277-786X/17/$18 · doi: 10.1117/12.2256715

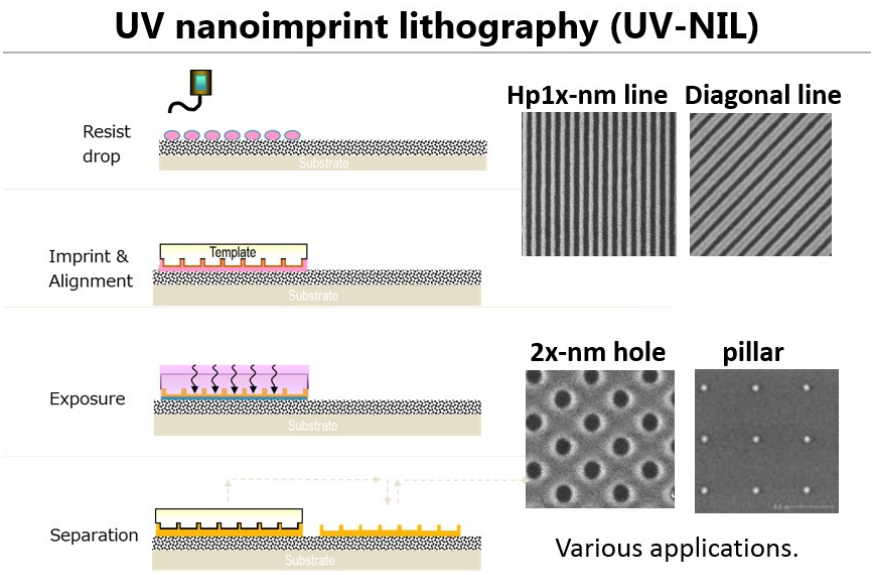

Figure 1. Left: Process flow of UV nanoimprint lithography. Right: SEM image of resist patterns obtained by UV-NIL.

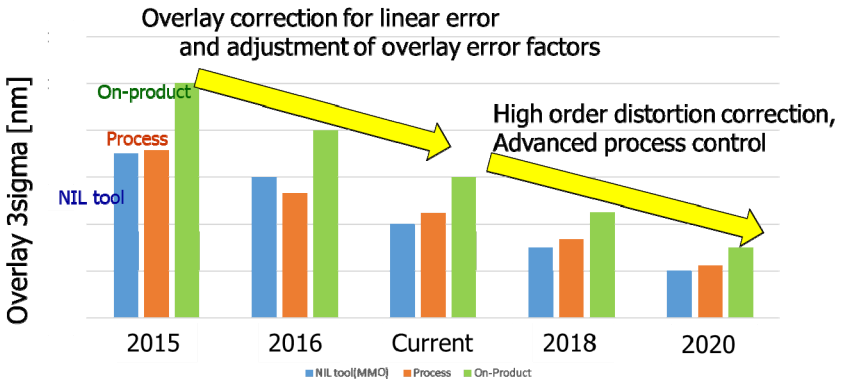

Figure 2. Roadmap for NIL overlay development.

2. NIL ALIGNMENT AND OVERLAY

NIL consists of the contact process, and then NIL tool structure completely differs from that for optical lithography tool. In the NIL tools, the template and the wafer are contacted through the resist. The alignment progresses while the template contacts the resist on the wafer. Through The Mask (TTM) alignment system is employed [8], in which the overlap image of template mark and the wafer mark are directly observed, and then the template and the wafer are aligned for each exposure field. Figure 3 illustrates a cross-sectional view of the alignment system of the current NIL tools. Four alignment marks exist in the exposure field and the NIL tool has four alignment scopes. During the alignment process, the four alignment scopes detect the relative shift of the four template marks with respect to the four wafer marks. Then the wafer stage is controlled to the target position.

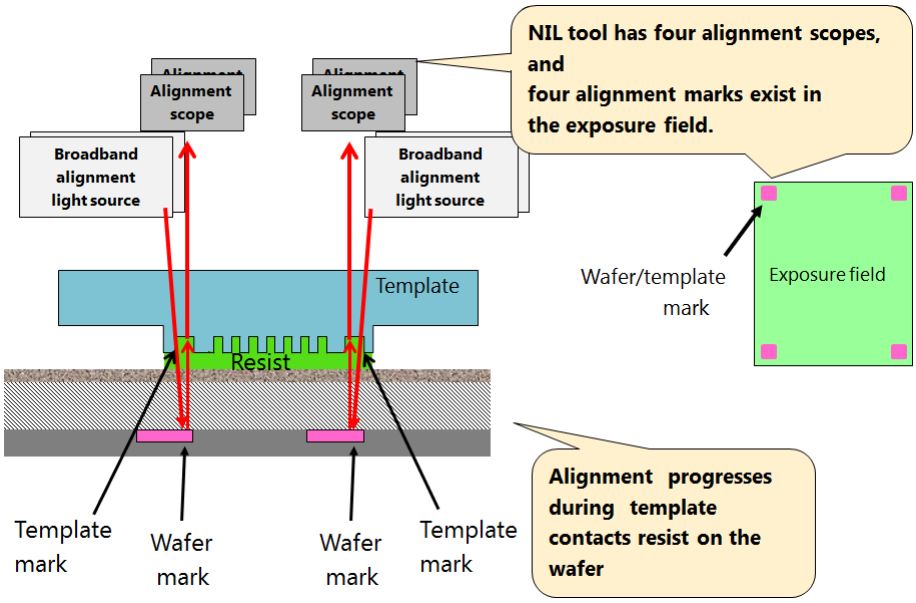

Figure 3. NIL alignment system.

Figure 4 illustrates four error sources in NIL process. They are NIL tool, template, wafer and contact process-related issue. The NIL tool has die-by-die alignment with the distortion correction function. NIL is a 1:1 patterning with no reduction and hence, the template pattern placement accuracy is more sensitive than that for photomask [7]. As for wafer, distortion control of the underlayer wafer through the process such as stack formation and/or etching, and alignment mark deformation by CMP are important [8, 9]. The residual layer thickness (RLT) is one of the NIL-specific error factors and has strong relations to the overlay [10].

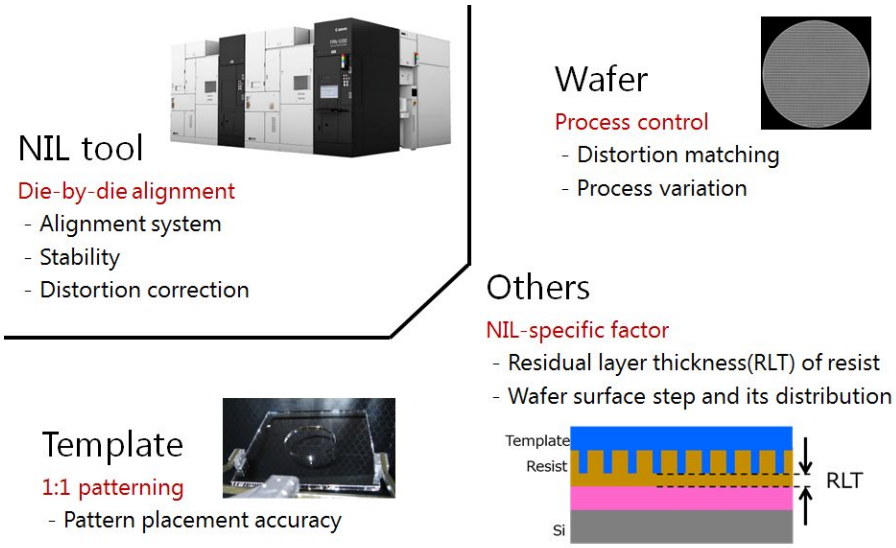

Figure 4. Error sources of NIL overlay.

Figure 5 shows results of overlay error analysis for both thinner RLT case and thicker RLT case. In the thinner RLT case, resist flow is inhibited at the narrow gap, and then the alignment movement needs strong force. The large force to align causes local distortion to the pattern. We control resist drop volume for each template with different field size and

different pattern layout density, and then find the better RLT condition with respect to overlay accuracy. In the case of wafers with surface topography, more resist drop is needed to fill the valley and to keep sufficient RLT at the peak.

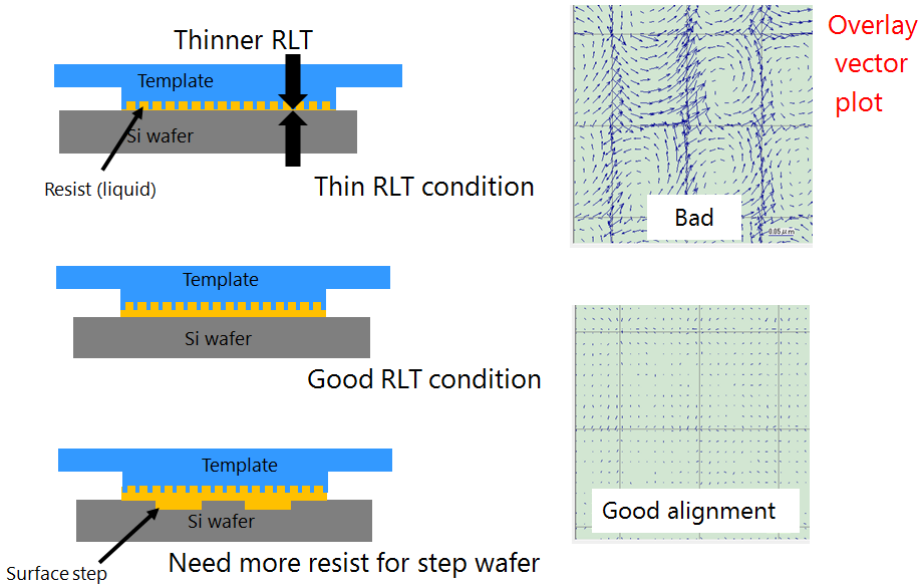

Figure 5. Impact of RLT on overlay.

3. NIL OVERLAY PERFORMANCES AND CHALLENGES

In this section we describe overlay measurement results and then discuss the potential of NIL overlay accuracy. Figure 6 shows the overlay evaluation flow in our work. At first, underlayer patterning was performed using an optical exposure tool or a NIL tool. Next, the wafer was etched to create alignment marks and overlay marks on the wafer. Then the second patterning, by the NIL tool, is applied on the wafer with alignment to the first (underlayer) pattern. Overlay error is obtained by the measurement of the bar-in-bar mark on the wafer using a commercially available overlay inspection tool.

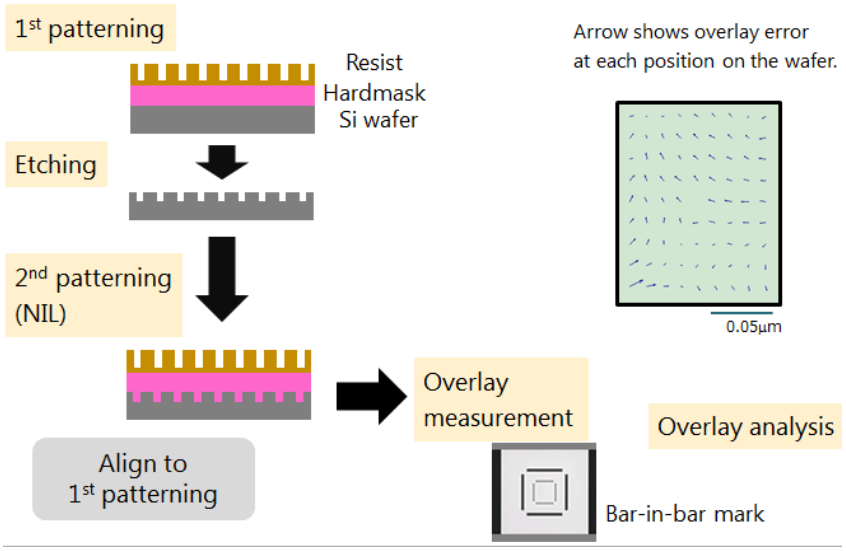

Figure 6. Evaluation flow of NIL overlay

3.1 NIL-to-NIL overlay

Figure 7 shows the overlay measurement result for the NIL tool on a 300mm wafer. In this experiment, both the first layer and second layer are patterned using a NIL tool. Overlay error |mean|+3sigma X and Y are 3.8nm and 4.5 nm, respectively.

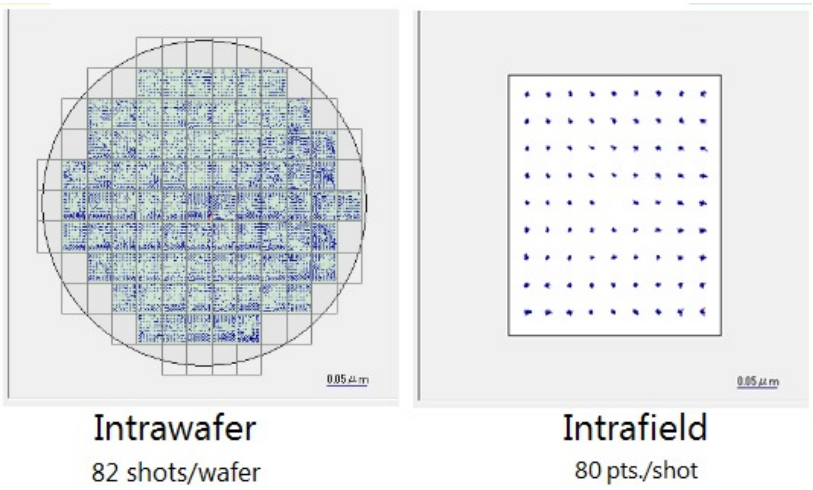

Figure 7. NIL overlay result for NIL-to-NIL process.

3.2. NIL-to-optical overlay

Figure 8 shows the overlay measurement result for "NIL-to-optical" case. In this experiment, the first layer is made by optical exposure tool and the second layer is made by NIL. For 11 wafers, overlay mean value across the wafer is less than 0.2nm. Overlay variation is 6.2nm in 3sigma for the champion wafer, but there are wafer-to-wafer variation and lot-to-lot variation. Current performance |mean|+3sigma is less than 7.5nm.

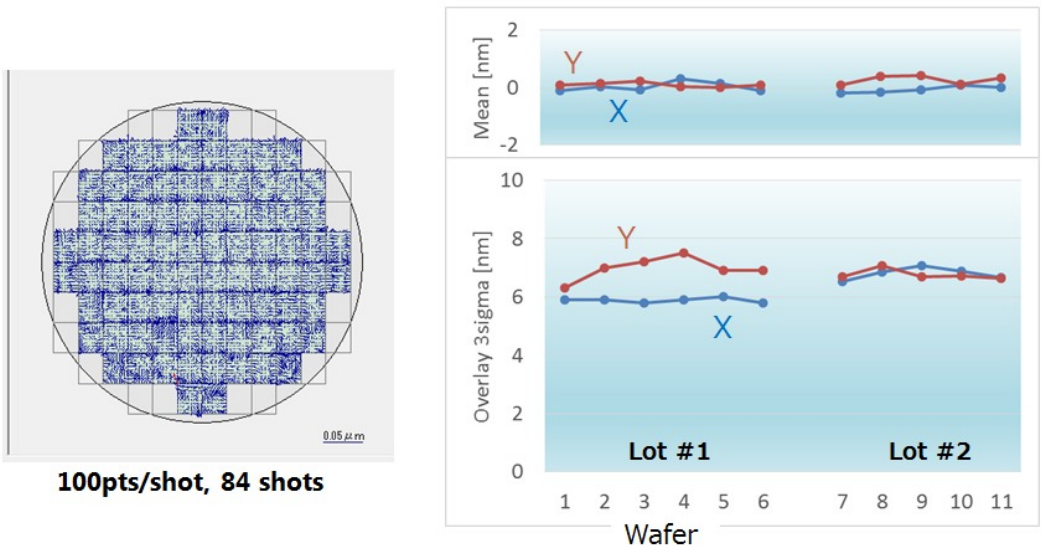

Figure 8. NIL overlay result for NIL-to-Optical process.

3.3 Potential of NIL overlay: current and future

Next, we will discuss the potential of NIL overlay accuracy. Figure 9 is a classification of intrafield overlay error by the possibility of correction. The current NIL tool has a distortion correction function, which can control shot magnification, rotation and trapezoid, by deformation of template shape [8]. The function deforms the template shape by an actuator to control these terms as the intended amount. The residual error shows the potential limit of NIL overlay accuracy.

Figure 10 shows the overlay residual error for the NIL-to-NIL process. For 6 wafers, overlay residual 3sigma is 2.5nm or less.

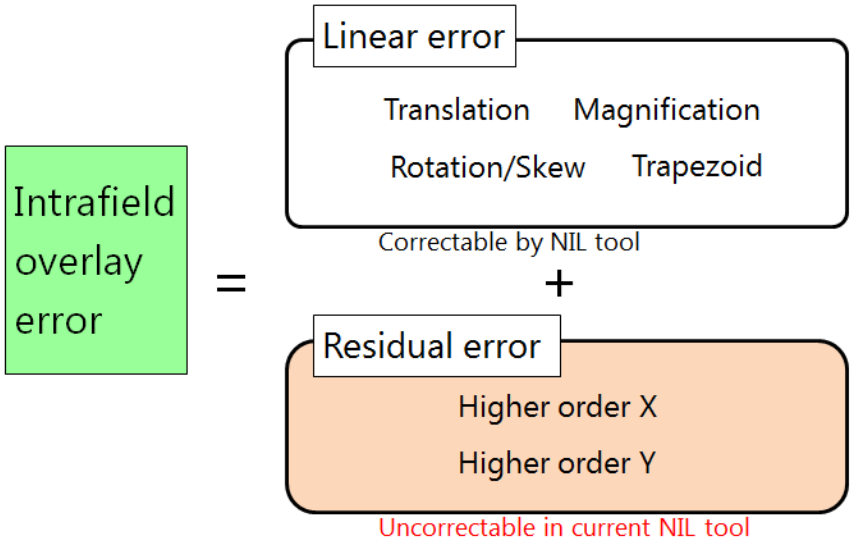

Figure 9. Decomposition of NIL overlay into correctable part and uncollectable part.

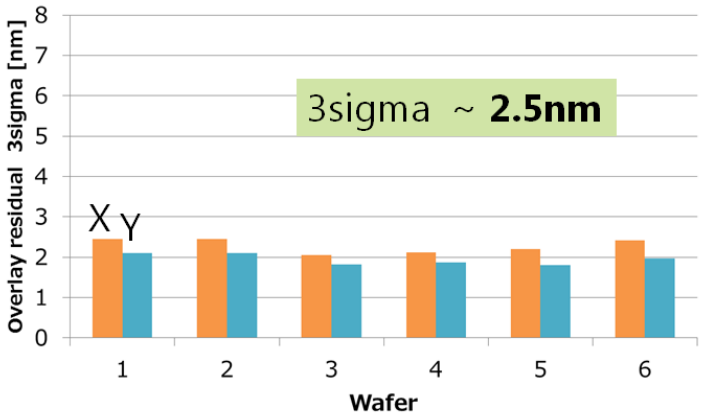

Figure 10. Overlay residual for "NIL-to-NIL"

Figure 11 explains the overlay residual error for the NIL-to-optical process. The left chart is the data obtained last year [5]. The right chart shows recent data. To improve the overlay accuracy, we adjusted some kinds of controllable factors of the NIL tools, that is, imprint force, template tilting at contact to wafer, and resist volume and distribution (RLT). Inappropriate imprint force or template attitude induces higher order distortion. And bad RLT also creates bad overlay as shown in Figure 5. After optimization, overlay residual error 3sigma decreased 35 % of initial amount. We successfully demonstrated distortion matching of the NIL tool to optical lithography tool.

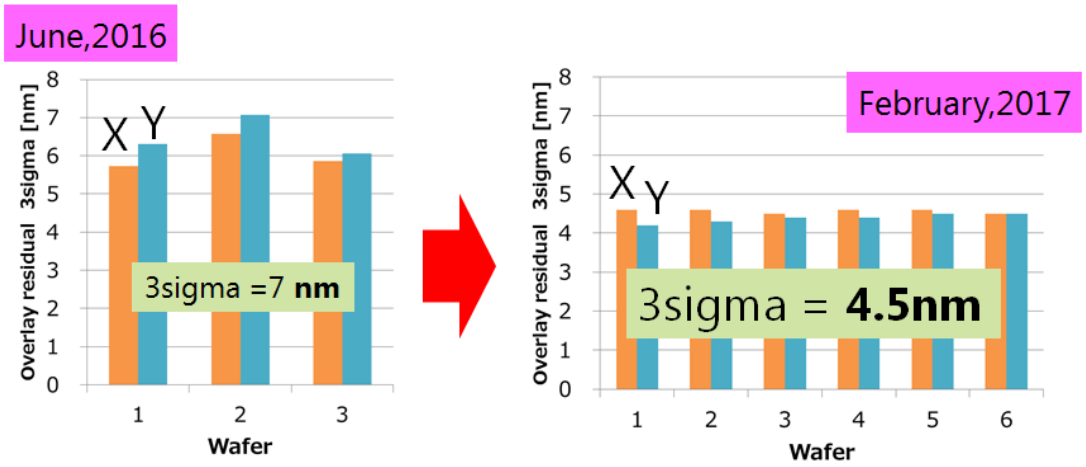

Figure 11. Overlay residual for "NIL to Optical". The left chart is the data obtained last year [5]. The right chart shows recent data.

Still we recognize a gap between NIL-to-NIL process and NIL-to-optical process in potential of overlay accuracy. To reduce the gap, we consider higher-order correction of intrafield error. Figure 12 shows estimation result of overlay error after correction of second-order, third order, and forth-order intrafield error in addition to linear correction. By applying up to third order correction, overlay error will be less than 4nm in 3sigma. Using fourth-order correction, NIL overlay performance will approach to 3nm.

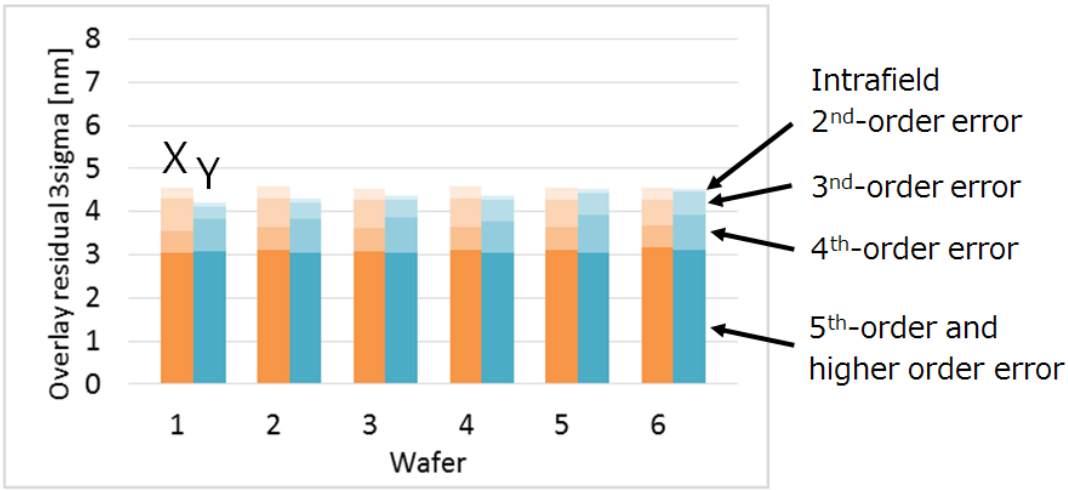

Figure 12. Estimation of overlay performance after applying higher-order intrafield correction. The n-th order error stands for intrafield overlay distribution expressed with a linear combination of $x^a y^{n-a}$, in that a=0..n [12].

To realize such correction of non-linear error, the NIL tool maker is developing a new distortion correction function. Recently, the development of higher order distortion correction was introduced [8]. The new function applies local heating to the wafer to reduce higher-order intrafield overlay error up to fourth-order. To achieve 3nm overlay on the mix-and-match overlay scheme for NIL and other lithography tools, development of higher order correction up to fourth order is necessary for NIL tools.

CONCLUSION

In the current NIL tool, we confirmed an overlay |mean|+3sigma of 4.5nm and 7.5 nm for the NIL-to-NIL process and NIL-to-optical process, respectively. The overlay residual 3sigma for NIL-to-NIL and NIL-to-optical are 2.5nm and 4.5nm, respectively. Distortion matching of NIL to optical lithography was demonstrated using NIL-specific control factors.

Further improvement is progressing to satisfy the request of tighter overlay requirement of the future semiconductor device manufacturing. Reduction in intrafield higher-order error is needed. For this purpose, a new distortion correction function is being developed. For NIL-to-optical process, 3nm overlay will be achieved by applying up to fourth-order distortion correction.

ACKNOWLEDGMENTS

The authors would like to thank Toshiba/SK hynix coworkers in the NIL Joint-development program and the NIL engineers in Canon and Canon Nanotechnologies Inc.

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