Packaging of High Temperature SiC Based Electronics

Liang-Yu Chen*, Robert S. Okojie[+], Philip G. Neudeck[+], Gary W. Hunter[+], Shun-Tien T. Lin[#]
*Ohio Aerospace Institute, Cleveland, Ohio 44142
[+]NASA Glenn Research Center, Cleveland, Ohio 44135
[#] United Technologies Research Center, East Hartford, Connecticut 06108

Abstract

In order to establish a material system for packaging 500°C SiC microsystems, aluminum nitride (AlN) and aluminum oxide (Al_2O_3) were selected as packaging substrates, and gold (Au) thick-film materials were selected as substrate metallization material for electrical interconnection system (thick-film printed wires and thick-film metallization based wire-bond) and conductive die-attach interlayer. During a 1500-hour test in atmospheric oxygen with and without electrical bias, the electrical resistance of Au thick-film based interconnection system demonstrated low and stable electrical resistance at 500°C. The electrical interconnection system was also tested in extreme dynamic thermal environment. A silicon carbide (SiC) Schottky diode was attached to ceramic substrate using Au thick-film material as the conductive bonding layer and was successfully tested at 500°C in air for more than 1000 hours. In addition to the electrical test of die-attach in static thermal environments, nonlinear finite element analysis (FEA) was used for thermal mechanical evaluation and optimization of the die-attach in a wide temperature range.

1. Introduction

NASA is interested in using high temperature operable microsystems, including micro-electro-mechanical-systems (MEMS) and on-chip electronics, to characterize *in-situ* combustion environments of aerospace engines and the atmosphere of inner solar planets such as Venus. As an example, high temperature pressure sensor is one of NASA and aerospace industry's 'most wanted' high temperature sensors for application in development of new generation of aerospace engines. The sensor and on-chip electronics must operate at temperatures up to 500°C, and the devices are always directly exposed to combustion species including oxygen in air, hydrocarbon/hydrogen in fuel, and catalytically poisoning species such as NO_x and SO_x in combustion exhaust. The temperature in the atmospheric environment of Venus is also as high as 500°C, and its gas ambience is corrosive. These operation environments can be summarized as high temperature, high dynamic pressure, and chemically corrosive. Various SiC semiconductor devices have been demonstrated to be operable at temperatures as high as 600°C [1,2], but only in a probe-station test environment partially because chip level packaging technology for high temperature (500°C and beyond) devices is still being developed. Core technologies needed for successful high temperature device packaging include high temperature operable electrical interconnection system and a conductive die-attach scheme.

MEMS devices, as they are identified, are both electrical and mechanical devices. Through micro-level mechanical operation, MEMS devices, as sensors, may transform mechanical, chemical, optical, magnetic, and other non-electrical parameters to electrical/electronic signals. As actuators, MEMS devices transform electrical/electronic signal into non-electrical/electronic operation. Therefore, compared to conventional integrated circuit (IC) packaging, the most distinct issue of high temperature MEMS packaging is to meet the thermal mechanical requirements imposed by the mechanical operability and reliability of

MEMS devices in a wide temperature range. High temperature SiC piezoresistive pressure sensors is a good example to illustrate the thermal mechanical requirements for packaging high temperature MEMS: the sensing mechanism of this device depends on the mechanical deformation of the semiconductor resistors residing on a diaphragm fabricated by micro-machining. Therefore, this device is very sensitive to the thermal mechanical stress from the die-attach due to mismatches of coefficients of thermal expansion (CTEs) in the die material (such as SiC), the substrate material, and in the die-attaching material.

Since MEMS devices have very specific structure requirements with respect to their immediate packaging environment [3], it is expected that the design of MEMS packaging will be very device dependent. This is in contradiction to the conventional IC packaging practice in which a universal package design can accommodate many different ICs. In order to address the common needs of high temperature microsystem packaging, we first discuss the basic requirements for packaging materials. Based on the discussions on the material requirements, a gold thick-film metallization based 500^{o}C operable electrical interconnection system and a thick-film material based conductive die-attach scheme are introduced. Following that the thermal mechanical evaluation and optimization of the die-attach are addressed by nonlinear finite element analysis (FEA).

2. Material Requirements

A summary of basic requirements of the major materials needed for packaging high temperature microsystems may help to establish guidelines for material selections:

Substrates: Ceramics meet the basic requirements for substrate material to be operable at high temperatures since ceramic materials have excellent and stable chemical and electrical properties at high temperatures, especially, in corrosive gas ambience. After a substrate material is selected, a high temperature operable metallization scheme (both materials and processing) matching the substrate material must be identified or developed to provide electrical interconnection. In order to reduce the thermal mechanical stress of the die-attach structure, the CTE of substrate material must match that of the device material (such as SiC). The properties of substrate surface and the interfaces formed at high temperature with other packaging materials, such as the die-attach material, also become very important. At high temperatures, the surfaces of some ceramics gradually react with gas ambience, such as oxygen and water vapor, therefore, would exhibit changes in properties such as surface resistivity and surface adhesiveness to other materials.

Al_2O_3 has excellent electrical properties and chemical/electrical stability at high temperatures so it is a candidate substrate material for high temperature operation. In comparison with Al_2O_3, AlN has a higher thermal conductivity and a lower CTE which is close to that of SiC, so it is a good substrate material for packaging SiC high temperature and high power devices. The CTEs of α and β polycrystalline SiC are very close to that of single crystal SiC, so thermal-mechanically they are ideal substrates for packaging large SiC die for operating in a wide temperature range. However, both the dielectric constants and the dissipation factors of these materials are relatively high [4]. In order to be used as a packaging substrate, the surface properties of polycrystalline SiC must be modified. After appropriate surface modification these materials might still be suitable only for low frequency application because of their high dissipation factors. Based on these discussions, AlN and 96% Al_2O_3 were selected as

high temperature substrate materials.

Metallization/Electrical Interconnection System: Most metals and alloys oxidize at temperatures near 500^{o}C in air. So the metals and alloys commonly used in conventional IC packaging such as copper, aluminum, and gold/nickel coated Kovar are excluded from packaging applications at temperatures of 500^{o}C and above unless a perfectly hermetically sealed inert/vacuum environment is available. At temperatures above 200^{o}C, intermetallic phases form at the interface of metals, such as Al and Cu. An intermetallic phase very often reduces the mechanical strength of the interconnection system. Thus, achieving material consistency in an interconnection system becomes extremely important in order to avoid thermal mechanical failure at high temperatures.

Precious metals are naturally considered for substrate metallization and electrical interconnection materials because of their chemical stability and good electrical conductivity. But some precious metals, such as platinum (Pt) and palladium (Pd) react with atomic hydrogen (H) to form H rich alloy at elevated temperatures. Though this is desirable for gas sensing devices [5], it is not so for electrical interconnection applications, because the phase transition may cause significant changes in the physical and electrical properties of these metals. Gold (Au) is extensively used for both substrate metallization and thin wire-bond in packaging and hybridizing conventional ICs. Besides the high conductivities and superior chemical stability at high temperatures, Au also has a low Young's modulus and a narrow elastic region. As it will be discussed in the Conductive Die-attach section, these features of Au are helpful to reduce thermal stress generated at the Au/die and the Au/substrate interfaces due to CTE mismatches if Au thick-film material is used as die-attaching interlayer. These features of Au are especially important to packaging high temperature MEMS because a wide range of operation temperature is of concern and the thermal mechanical stress is critical to the reliability of the packaged device. It has been reported that Au thin film/wire with small grain size suffered from electro-migration of Au atoms at grain boundaries at high temperature under extreme current density (~10^{6} A/cm^{2}) operation [6]. Surface modification and coating were suggested for Au conductor in order to be able to operate at high temperature and high current density [6].

Conductive Die-attach: Generally, die-attach materials are expected to be electrically and thermally conductive and physically/chemically stable at high temperatures, and to permit a die attaching process at a temperature within the temperature range of device operation. For applications in high temperature MEMS packaging, the thermal mechanical properties of die-attach material such as CTE, Young's modulus, fatigue/creep properties, and their temperature dependencies are very much of concern since the die attaching material is in intimate contact, both electrically and mechanically, with the die and the substrate. The die attaching material is, therefore, also expected to thermo-mechanically compensate for any possible CTE mismatch between the die and the substrate materials. Another major concern of die-attaching materials for high temperature application is long-term chemical and mechanical stabilities of its interfaces formed with the die and substrate materials at high temperatures. If the die-attach is expected to be electrically conductive, the electronic properties of its interface with the die would also become critically important. Combining all these mechanical, chemical, and electrical requirements, it is apparent that a material system for die-attach with a suitable attaching process is critical to the success in packaging high temperature MEMS device.

The thermal mechanical stress of the die-attach due to the mismatches of CTEs of the die, the attaching material, and the substrate may cause degradation and failure of packaged devices. The extreme case of die-attach failure caused by thermal mechanical stress is cracking of the die or the attaching material. For high temperature MEMS devices, besides the failure due to fatigue and creep in the die and attaching materials, thermal stress can also cause undesired device thermal response, irreproducibility of device operation, and output signal drift. Therefore, the thermal mechanical failures of the die-attach due to material CTE mismatches are expected to be common and important thermal mechanical issues which need to be addressed in packaging MEMS devices, especially high temperature MEMS devices.

3. High Temperature Electrical Interconnection System

As discussed in the last section, 96% Al_2O_3 and AlN are selected for substrate materials because of their high temperature chemical and electrical stabilities. Au thick-films provide basic chemical and electrical stabilities at high temperatures [7,8], therefore are selected for metallization and wirebond. In this section we discuss an Au thick-film based 500^{o}C operable electrical interconnection system for packaging low power high temperature microsystems.

Au thick-film was screen-printed on a ceramic substrate (AlN or 96% Al_2O_3) and cured at 850^{o}C in air using the recommended curing process [9], to form printed wire and metallization pads for wire-bond. In order to examine the high temperature stability of the printed thick-film circuit, the test circuit was electrically tested at 500^{o}C in air for a total of ~1500 hours using four probe resistance measurement. The electrical resistance of the thick-film wire/circuit was first measured at room temperature, then the temperature was ramped up to 500^{o}C for ~1000 hours without electrical current flow and the resistance of the wire was measured periodically. The resistance fluctuated slightly within 0.1% during the first 1000 hours test, as shown in Figure 1. After testing for 1000 hours without electrical bias, the circuit was biased with 50 mA DC current and the resistance was continuously monitored. The resistance fluctuated slightly within 0.1% for 500 hours with electrical bias. This very small change in resistance is acceptable for almost all envisioned high temperature device packaging applications.

Figure 1: Normalized resistance of thick-film wire at various temperatures with and without DC

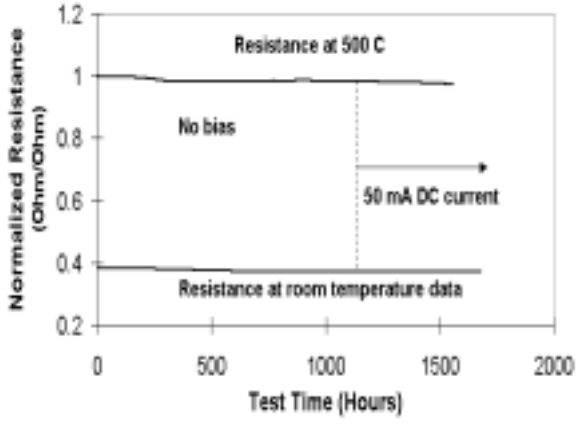
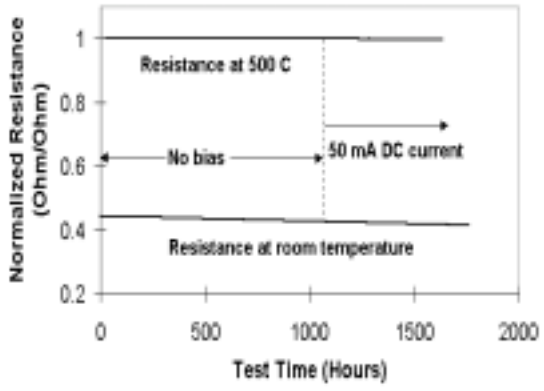
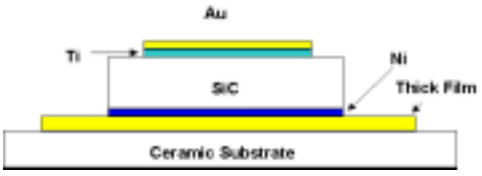


Figure 2: Normalized resistances of wire-bond test circuit measured at room temperature and 500°C vs. test time at 500 °C with and without DC bias.



In addition to the high temperature electrical validation discussed above, the Au thick-film metallization system needs to be mechanically evaluated at high temperatures in order to be reliably applicable at elevated temperatures. The tensile strength of Au thick-film metallization on 96% Al_2O_3 substrate has been tested at room temperature after extended storage at 500°C [7,10]. In order to examine the mechanical strength and the thermal dynamic stability of the binding system of Au thick-films at high temperature, the shear strength of Au thick-film metallization on 96% Al_2O_3 substrate was tested at temperatures up to 500°C. The shear strength (breaking point) at 500°C reduced by a factor of ~ 0.80 with respect to that at 350°C while the shear strength (breaking point) at 350°C was close to that at room temperature. The shear strength of Au thick-film designed for AlN were not as high as those for Al_2O_3, but it was sufficient for application in microsystem packaging operable at 500°C.

Figure 3: Schematic diagram of as - fabricated SiC device and die-attach structure.



After the electrical and mechanical qualifications of Au thick-film metallization on Al_2O_3 and AlN substrates, the electrical stability of thick-film metallization based wire-bond test circuit [9] including thick-film conductive wire/pads, bonded thin Au wires, and the interfaces between them were extensively tested at high temperature with and without electrical bias in oxidizing air. The test sample is composed of 22 units of 1 mil Au wire-bond (44 bonds) in series. The resistance of the wire-bond sample was measured at room temperature and 500°C at various testing times at 500°C. The resistance was first measured at room temperature, followed by

ramping the temperature up to 500°C and the resistance was monitored in air without electrical bias for 670 hours. As shown in Figure 2, the temperature was then lowered back to room temperature and the resistance was recorded again. After this thermal cycle, the circuit resistance was continuously monitored for a total of 1200 hours at 500°C in air without electrical bias (current flow), followed by another 500 hours at 500°C with 50 mA (DC) current. The resistances under all these conditions were desirably low (less than 0.5 Ω per unit) and decreased slowly and slightly at an average rate of 2.7% over the 1500 hour testing period. The rate of resistance decrease under the DC bias is close to that without electrical bias.

An identical wire-bond circuit of that tested in static thermal environments was electrically tested in dynamic thermal environment. The wire-bond circuit was tested under thermal cycles between room temperature and 500°C with an initial temperature rate of 32°C/min for 123 cycles first, then at the temperature rate of 53°C/min (higher than thermal shock rate) for additional 100 cycles with 50 mA electrical bias. The maximum change in electrical resistance during the thermal cycles is 1.5% at room temperature, and 2.6% at 500°C [11].

4. Conductive Die-attach

An Au/Ti/SiC Schottky diode with a Ni ohmic contact on the backside was used as a device to test the die-attach scheme developed for high temperature operation [12]. After dicing, the 1 mm x 1 mm SiC diode chip was attached to a ceramic substrate (either AlN or 96% Al_2O_3) using Au thick-film material as shown in Figure 3. This Au thick-film die-attaching scheme resulted in a low resistance die-attach which is necessary for packaging many devices with vertical topologies.

The optimum process for attaching SiC dies (with Ni contact) to the ceramic substrate was investigated. The thick-film uniformity issue needs to be addressed first. As discussed elsewhere [12], the organic vehicle of "raw" thick-film materials evaporates during the initial drying process. Since the thick-film material is sandwiched by the ceramic substrate and the SiC die, the escaping organic vehicle molecules have a relatively long way to migrate to escape from the sides. During rapid drying this may distort somewhat the thick-film distribution, therefore, cause non-uniform thick-film distribution between the die and the substrate. A slower drying process (120°C – 150°C) was critical to keep the thick-film bonding layer uniform and the die parallel to the substrate after the curing process. It was also necessary to consider reducing the amount of organic vehicle evaporated during die-attach processing. A two-step die-attach process was used. A thick-film layer was first screen-printed on the substrate and cured at 850°C, the SiC die was then attached to the cured thick-film pattern with minimal amount of subsequent thick-film.

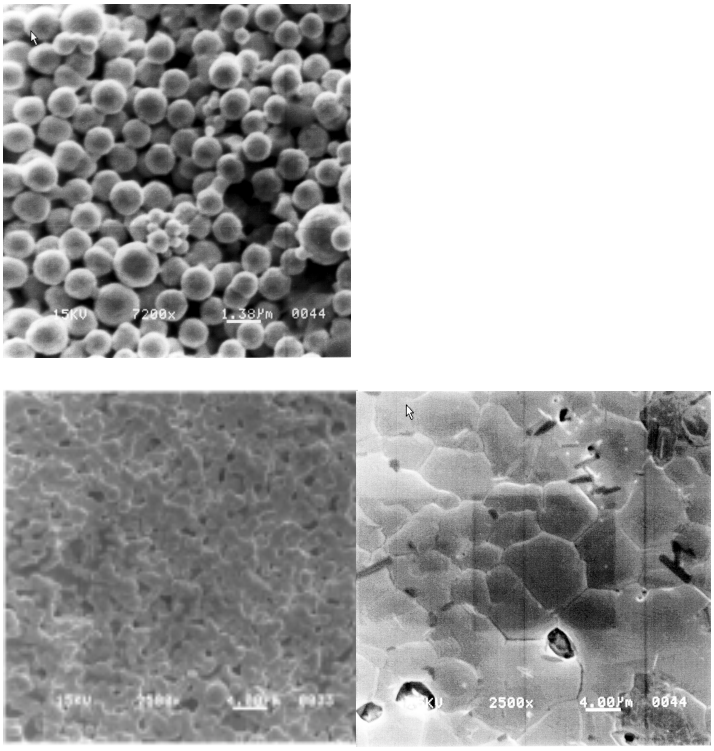


Figure 4, Scanning Electron Microscope (SEM) micrograph of thick film surfaces cured at (a) 500°C for 25 min, (b) 600°C for 20 min, and (c) 850°C for 15 min. (a) Micro powder structure indicating insufficient boundary diffusion. (b) Chain structure replaces powder structure indicating a critical curing condition. (c) A large and smooth grain structure indicating solid film formation.

The second processing parameter to be optimized is the final curing temperature. A lower final curing temperature (with respect to standard curing temperature of 850°C) was desired in order to minimize the curing effects on the interfacial properties of Au/Ti/SiC device. To determine an optimized final curing temperature for the die-attach process, micro-structures and surface compositions of the thick-film cured at various temperatures were investigated. As shown in Figure 4a, the surface of thick-film cured at 500°C showed very sharp Au micro powder structures indicating that there was insufficient diffusion to form a solid film at this temperature. The thick-film surface cured at 850°C (Figure 4c) showed large grain sizes and a relatively smooth surface indicating thick-film formation. The thick-film surface cured at 600°C (Figure 4b) showed that micro powder structure has been replaced by net and chain structures indicating a critical curing condition necessary for formation of a coherent thick-film. Based on this result, 600°C was selected as the preferred final die-attach processing temperature. Auger Electron Spectroscopy was used to characterize the surface compositions of the thick-film surfaces cured at 500, 600, and 850°C. In addition to expected normal levels of carbon and oxygen surface contaminations, copper and lead (oxides as binders) were found on the surfaces of all three samples. Compared to the sample surfaces cured at 500 and 600°C, binder concentrations on the sample surface cured at 850°C were relatively lower indicating high curing

temperature is preferred for binder molecules migration to the interface with ceramic substrate. So the first layer of thick-film screen-printed on the substrate was cured at 850^{o}C for best adhesion. Since the thick-film material used as die-attach binding materials 'sees' metals on both sides (Au thick-film on the substrate and the Ni thin film on the backside of the SiC die), it seems less likely that the binders should significantly segregate to the interfaces. A 0.001" diameter Au wire was bonded on the top Au thin-film metallization pad with a thick-film overlayer by thermal-compression bonding technique. Thick-film material was also used to reinforce the top Au thin film for better wire bonding. The Au thin-film metallization area was coated with thick-film on the top then dried at 150^{o}C for 10 minutes. The thick-film on the device top was cured during the final die-attach process (at 600^{o}C).

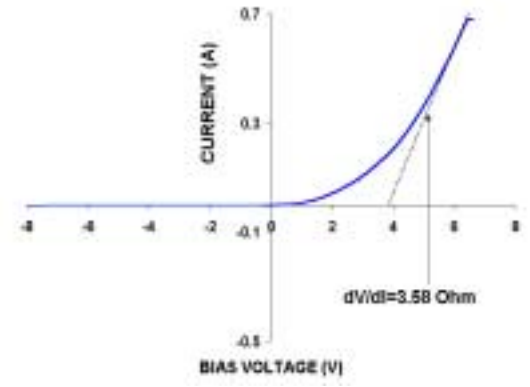


Figure 5: I-V curve of attached SiC test-diode characterized at 500 ^{o}C after being tested for 1000 hours at 500 ^{o}C oxidizing air.

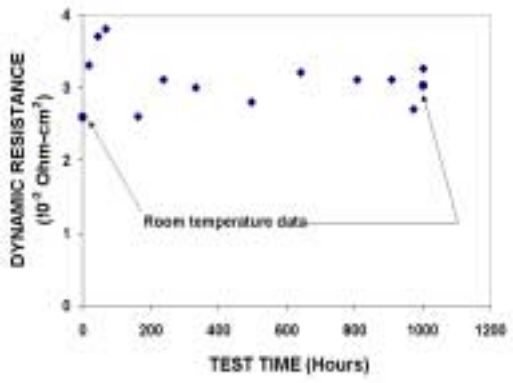


Figure 6: Minimum specific dynamic resistance (normalized to device area) calculated from I-V data vs. heating time at 500 ^{o}C. This resistance includes resistances contributed from the Au(Ti)/ SiC rectifying interface, SiC wafer, the die-attach materials/ interfaces. Resistances of the bonded wire and the test leads have been subtracted.

The attached SiC test diode (Figure 3) was characterized by current - voltage (I-V) measurements at both room temperature and 500°C for various heating times. A minimum dynamic resistance (dV/dI) in a high current (forward biased) region of the I-V curve was used to estimate both the stability and the upper limit of resistance of the die-attach structure (both interfaces and materials), as shown in Figure 5. This dynamic resistance includes forward dynamic resistance of Au/Ti/SiC interface, SiC wafer bulk resistance, the die-attach materials/ interfaces resistance, bonded wire resistance, and the test leads resistance in series. The resistance contributed from test leads and bonded wire were measured independently and subtracted. The attached device was first characterized by I-V measurements at room temperature. The device exhibited rectifying behavior and the minimum dynamic resistance after subtracting test-leads/bond-wire resistance (applies to all the following discussion) measured under forward bias was ~ 2.6 Ω, as shown in Figure 7. The temperature was then ramped up to 500°C (in air) and the diode was *in situ* characterized periodically by I-V measurement for ~1000 hours. During the first 70 hours at 500°C the (lowest) dynamic resistance under forward bias increased slightly from 3.3 Ω to 3.8 Ω. After that the dynamic resistance decreased slightly and remained at an average of 3.1 Ω. The diode was then cooled down to room temperature and characterized again. The minimum forward dynamic resistance measured at room temperature was 3.3 Ω. It is worth noting that the device's I-V curve changed somewhat with time during heat treatment at 500°C. However, the dynamic resistance of attached diode remained comparatively low over the entire duration of the test and temperature range, indicating a low and relatively stable die-attach resistance.

AlN material properties			
Temp (deg C)	CTE (xE-6/C)	E (xE6 psi)	ν
-15	3.14	50.00	0.25
20	3.90	50.00	0.25
105	5.36	50.00	0.25
205	6.51	50.00	0.25
305	7.25	50.00	0.25
405	7.76	50.00	0.25
505	8.25	50.00	0.25
605	8.72	50.00	0.25
705	9.09	50.00	0.25

96% Alumina properties			
Temp (deg C)	CTE (xE-6/C)	E (xE6 psi)	ν
-15	5.34	44.00	0.21
20	6.20	44.00	0.21
105	7.83	43.58	0.21
205	8.48	43.06	0.21
305	8.89	42.51	0.21
405	9.28	41.93	0.21
505	9.65	41.34	0.21
605	10.00	40.74	0.21
705	10.33	40.13	0.21

SiC material properties			
Temp (deg C)	CTE (xE-6/°C)	E (xE6 psi)	ν
-15	2.93	66.72	0.3
20	3.35	66.72	0.3
105	3.97	66.42	0.3
205	4.23	66.08	0.3
305	4.46	65.74	0.3
405	4.68	65.39	0.3
505	4.89	65.05	0.3
605	5.10	64.71	0.3
705	5.29	64.36	0.3

Au material properties			
Temp (deg C)	CTE (xE-6/C)	E (xE6 psi)	ν
-15	14.04	11.09	0.44
20	14.24	10.99	0.44
105	14.71	10.83	0.44
205	15.23	10.59	0.44
305	15.75	10.28	0.44
405	16.29	9.92	0.44
505	16.89	9.51	0.44
605	17.58	9.03	0.44
705	18.38	8.50	0.44

Table 1: Basic material properties of SiC, Au, 96% alumina, and AlN used for FEA simulation for die-attach structure.

5. Thermal Mechanical Properties of Die-attach

As it was discussed in Material Requirements section, the mechanical issues of most concern for high temperature MEMS packaging are the die-attach thermal stress problem and the general guidelines for material selection, structure design, and optimization of attaching process to minimize overall thermal stress of the die-attach structure. Assuming that a conventional die-attach structure, in which the die-backside is attached to a substrate using an attaching material layer, is adopted, the typical die-attach structure is illustrated in Figure 3. The die-attach using Au thick-film material discussed in last section is a typical example of this structure.

For high temperature microsystem packaging, thermal mechanical properties of the die-attach structure need to be addressed at two levels: 1) Mechanical damage of the die-attach structure resulting from thermal mechanical stress. 2) Thermal stress/strain effects on the mechanical operation of devices. The failures at both levels are rooted in thermal mechanical stress of the die-attach. The thermal mechanical governing equations [13] of the die-attach are complicated, but analytically solvable in some cases [14,15]. References 14-15 have investigated the design of the die attach assembly using closed analytical solution assuming linear elastic material properties. Nonlinear effects were also considered in a simplified model in reference 15. Considering the wide temperature range and low yield strength of gold thick-film, a non-linear elastic-plastic finite element analysis (FEA) was used to simulate Au thick-film based SiC die-attach as an example of die-attach optimization for packaging high temperature MEMS.

The basic mechanical properties of SiC, Au, AlN, and 96% Al_2O_3 and their temperature dependence used for FEA simulation are listed in Table 1 [11]. The temperature dependence of Young's modulus of AlN in a wide temperature range has not been reported, so it was extrapolated as a constant from the data at room temperature. Poisson's ratios of both single crystal 4H-SiC and AlN are not published, so they were estimated according to those of other carbides and nitrides. The thermal and mechanical properties of 4H SiC were assumed isotropic. Since the yield strength of Au thick-film material has not been published, the simulation was conducted in a range of yield strength from 650 to 3000 psi. The numerical calculation using the yield strength at the low end diverged.

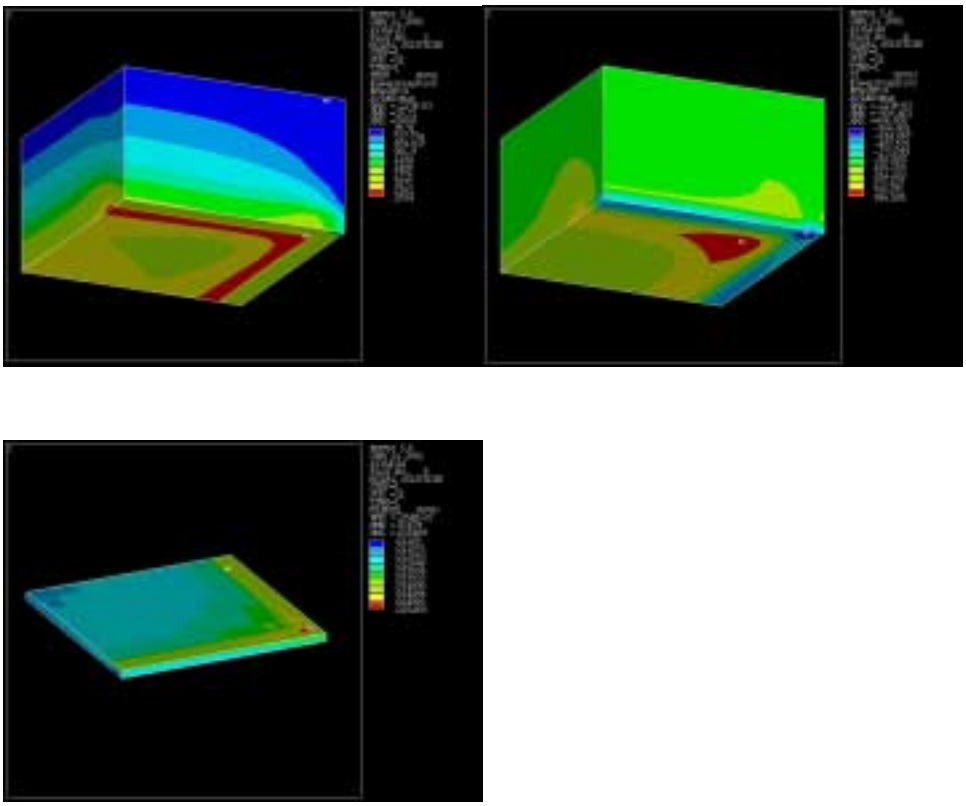


Figure 7: Thermal stress and strain distribution in SiC die and Au thick-film layer at room temperature, the relaxing temperature is 600^{o}C. (a) Von-Mises stress distribution in SiC die. (b) Maximum Principal Stress distribution in SiC die. (c) Equivalent Plastic Strain in Au thick-film layer.

Figure 7(a) and (b) show Von-Mises stress and Maximum Principal Stress contours of a quarter of SiC/Au/AlN die-attach structure at room temperature with relaxing temperature of 600^{o}C. Horizontally, at the interface with a Au thick-film layer, the stress in the die basically increases with the distance from the center of the die attach interface, the stress reaches a maximum at the area close to the die edges, especially, at the corner. This is understandable. The source of thermal stress of the die-attach structure is CTE mismatch at bonding interfaces. At the area far from the neutral point (larger distance from neutral point, DNP) the trends of relative displacement with respect to Au thick-film, driven by the CTE mismatch, would be larger. From this it can be predicted that the maximum thermal stress would increase tremendously with increase of the die-size, or attaching area. Vertically, the stress attenuates rapidly with the distance from the interface. At the die center region the stress near die surface attenuates by a factor of 1/80 with respect to the stress at the interface. With this picture of thermal stress distribution one can conclude that flip-chip bonding would not be recommended for high temperature MEMS devices if the CTE mismatch is not well controlled, and a thicker die (or a stress buffer layer of the same material) can significantly reduce the thermal stress at die surface region.

Figure 7(c) shows Equivalent Plastic Strain (EPS) in the Au thick-film layer. Because of the same physical mechanism as that for SiC die, the highest EPS in Au layer are located at the area close to the corner, where the DNP is larger. This indicates that smaller die-size/attaching-area may provide relatively better thermal mechanical reliability with respect to larger dies.

In comparison with AlN substrate, 96% Al_2O_3 substrates have relatively higher CTEs (~6.2×10^{-6} / ^oC compare with ~3.9×10^{-6} / ^oC of AlN). The FEA results indicate that using AlN substrate would result in an improvement of maximum Von-Mises stress in SiC die by a factor of 0.29, an improvement of Von-Mises stress in the substrate by a factor of 0.33, and an improvement of MPS in Au thick-film layer by a factor of 0.42. This improvement of thermal stress/strain corresponds to an improvement of fatigue lifetime of Au thick-film layer by a factor of 4.3 – 9.0 (assuming the power law exponent in Coffin-Mason model, C, is -0.4 and -0.6, respectively). So in terms of thermal mechanical reliability of die-attach, AlN is suggested for packaging SiC high temperature MEMS devices compared to 96% Al_2O_3 owing to the fact that the CTE of AlN is close to that of SiC.

Figure 8 shows maximum Von-Mises Stress in substrate and SiC and the EPS of the thick-film layer vs. the thickness of Au attach layer. The maximum stress in the SiC die decreases by a factor of 0.75 with respect to the thickness change from 20 μm to 50 μm, for AlN substrate, while the maximum stress in the SiC die decreases by a factor of 0.5 with respect to the thickness change from 20 μm to 50 μm, for 96% Al_2O_3 substrate. The increase of Au layer thickness also significantly improves the stress in AlN substrate, as shown in Figure 8(b). Figure 8(c) shows the maximum EPS in Au layer vs. thickness of Au attaching layer. The increase of the thickness from 20 μm to 50 μm significantly reduces the EPS in the Au thick-film layer in both AlN and Al_2O_3 cases.

Besides the dependence of thermal mechanical configuration of the die-attach on material properties of the die, the attaching layer, and the substrate, the thermal mechanical stress in a die-attach structure also depends on the temperature deviation from the relaxing temperature, T_R, at which the structure is thermal-mechanically relaxed [13,16]. In order to assess the relaxing temperature effects on the thermal stress of the die-attach structure, the stress distribution of the die-attach at room temperature is simulated by FEA assuming that the structure is relaxed at various temperatures (from 300 - 600^{o}C). Figure 9 shows the maximum Von-Mises stress in the die and EPS in Au thick-film layer vs. the relaxing temperature. If the relaxing temperature could be lowered from 600^{o}C to 300^{o}C, the maximum Von-Mises Stress in the die can be reduced by a factor of 0.8. And the maximum EPS in Au thick-film layer can be reduced by a factor of 0.5. The fatigue lifetime corresponding to the stress reduction is improved by a factor of 3 (assuming the exponent in Coffin-Mason model of fatigue, C, is -0.6). Ideally, the thermal mechanical property of the die-attach structure is optimized if the relaxing temperature could be set at the middle of the operation temperature range.

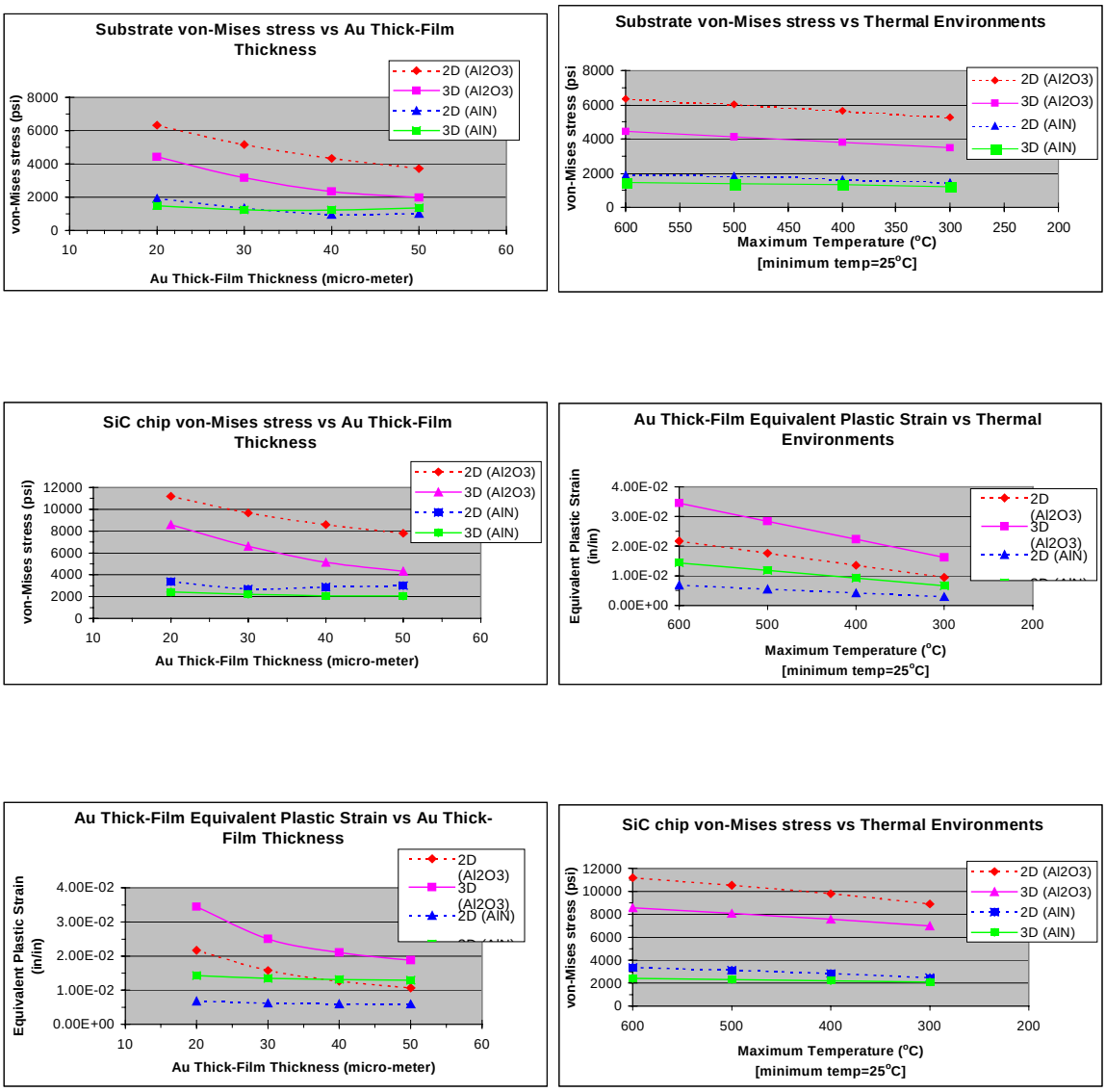


Figure 8: Maximum stress and strain of die-attach vs. the thickness of Au thick-film interlayer, at room temperature. (a) von-Mises stress in AlN substrate, (b) von-Mises stress in SiC die, and (c) EPS in Au thick-film

Figure 9: Relaxing temperature dependence of maximum stress and strain in SiC chip, substrate, and Au attaching layer.

6. Summary and Discussion

Ceramic substrates, Al_2O_3 and AlN, and Au thick-film metallization based material system were discussed for low power high temperature chip level packaging. The electrical interconnection system of this packaging system has been extensively tested in a temperature range from room temperature to 500°C with and without electrical bias in oxidizing environments. The mechanical strengths of Au thick-film metallization on both Al_2O_3 and AlN substrates have been preliminary tested at 500°C. Following electrical and mechanical tests in

static thermal environments, the Au thick-film wire-bonds were evaluated in extremely dynamic thermal environments from room temperature to 500^{o}C. The test sample including 44 Au wire-bonds, survived 120 thermal cycles at temperature rate of 32^{o}C/min and 100 additional cycles at 53^{o}C/min in oxidizing environment with 50 mA DC current which is sufficient for many low power devices. An attached SiC diode using this technology was successfully tested at 500^{o}C in an oxidizing environment for more than 1000 hours setting lifetime records for high temperature electronic packaging.

In order to optimize the thermal mechanical properties of Au thick-film material based SiC die-attach, nonlinear FEA was used to simulate and compare the thermal mechanical stress/strain distributions against material, structure, and processing parameters to establish basic guidelines of material selection, structure design, and processing parameters determination.

The combination of versatile functions of MEMS devices and survivability/operability at high temperature introduces a new generation of micro-devices, high temperature MEMS, with revolutionary capabilities for many aerospace applications. Packaging these revolutionary devices, however, presents new challenges and research in device packaging. In meeting these challenges, innovative packaging materials possessing superior physical/chemical properties suitable for high temperature operation, innovative structure/design meeting these specific device and operation requirements, and innovative packaging processes able to accommodate both the new materials and the new structures are expected.

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