Pass-Transistor Logic

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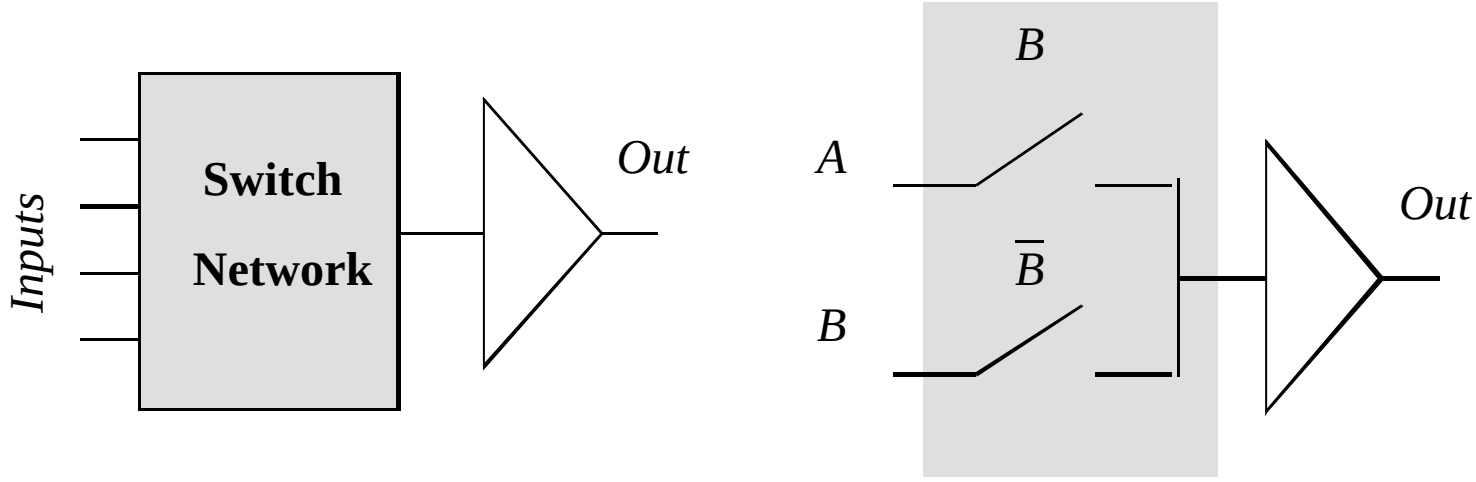


- **N transistors**
- **No static consumption**

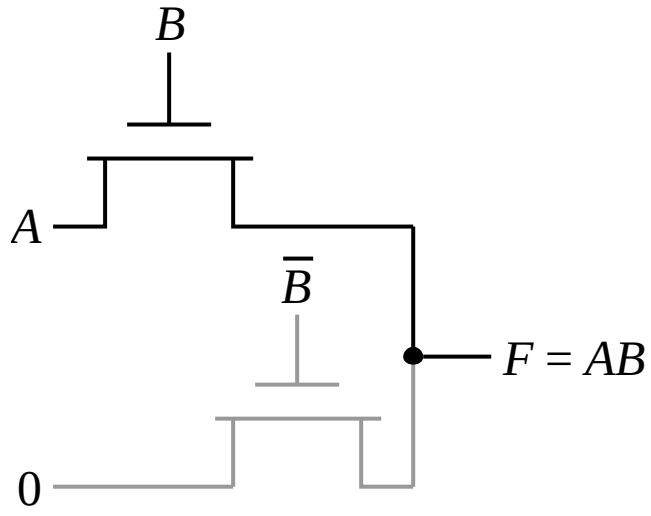
Primary inputs drive the gate terminals + source-drain terminals. In contrast to static CMOS – primary inputs drive gate terminals.

Example: AND Gate

When B is “1”, top device turns on and copies the input A to output F. When B is low, bottom device turns on and passes a “0”.

The presence of the switch driven by $\overline{B}$ is essential to ensure that the gate is static – a low-impedance path must exist to supply rails.

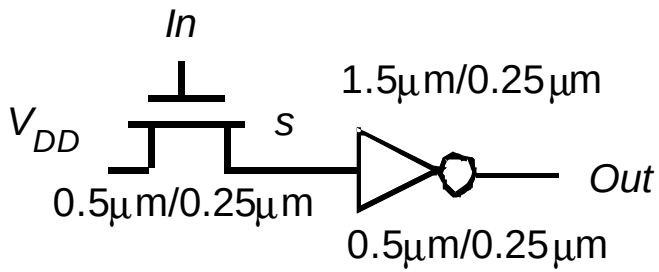
Adv.: Fewer devices to implement some functions. Example: AND2 requires 4 devices (including inverter to invert B) vs. 6 for complementary CMOS (lower total capacitance).

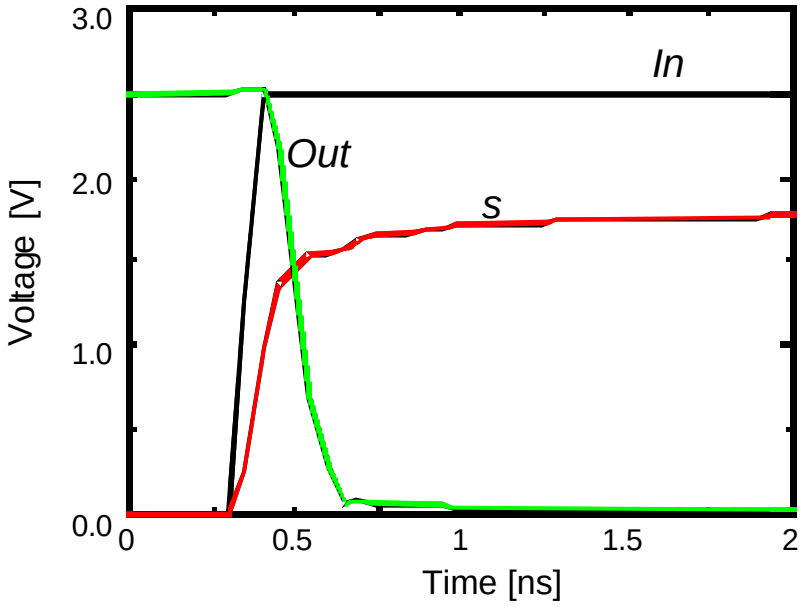


NMOS is effective at passing a 0, but poor at pulling a node to Vdd. When the pass transistor a node high, the output only charges up to V_{dd}-V_{tn}. This becomes worse due to the body effect. The node will be charged up to $V_{dd} - V_{tn}$ (V_s)

$$V_s = V_{dd} - (V_{tn0} + g(\sqrt{|2\Phi_f| + V_s} - \sqrt{|2\Phi_f|}))$$

NMOS-Only Logic

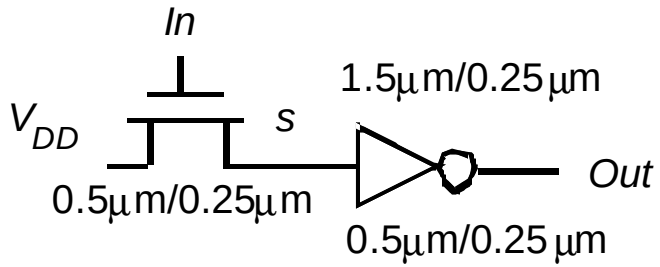




V_s is initially 0. V_s will initially charge up quickly, but the tail end of the transient is slow. The current drive of the transistor (gate-to-source voltage) is reduce significantly as V_s approaches V_{dd}-V_{tn} (the current available to charge up node "s" is reduced drastically.

For cascading, the output of a pass transistor (#1) should not drive the gate of another MOS device (#2). This will produce an output = V_{dd}-V_{tn1}-V_{tn2}

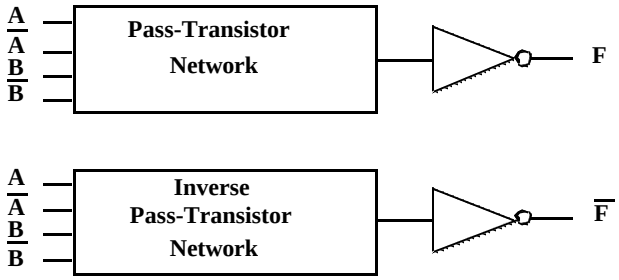
Energy Consumption



Pass transistors require lower switching energy to charge up a node, due to the reduces voltage swing. The output node charges from 0 -> V_{dd}-V_{tn}, and the energy drawn from the power supply for charging the output of a pass transistor is given by $C_L.V_{dd}(V_{dd}-V_{tn})$

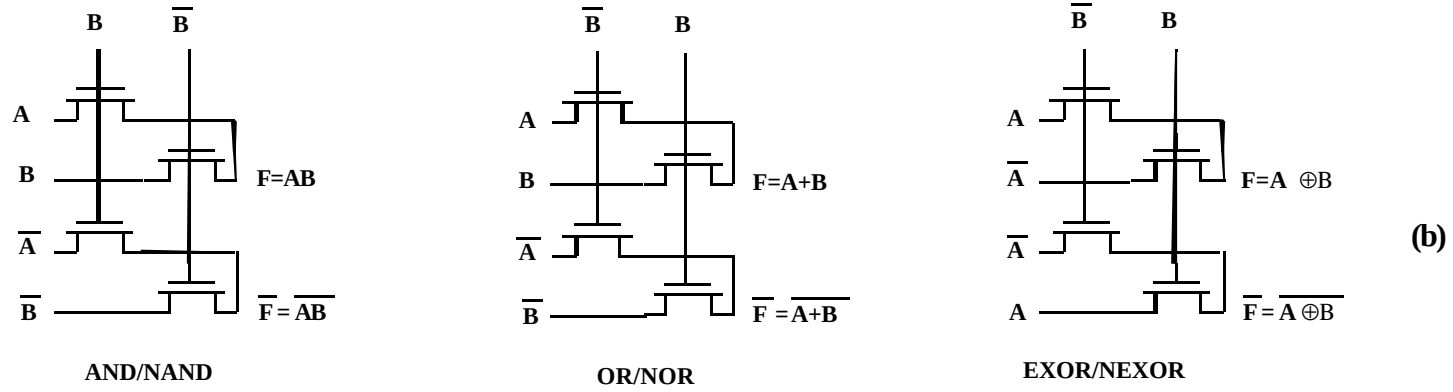
While lower switching power is consumed, it may consume **static power** when output is high – the reduced voltage level may be insufficient to turn off the PMOS transistor of the subsequent CMOS inverter.

Complementary Pass Transistor Logic



(a)

To accept and produce true and complementary inputs and outputs.



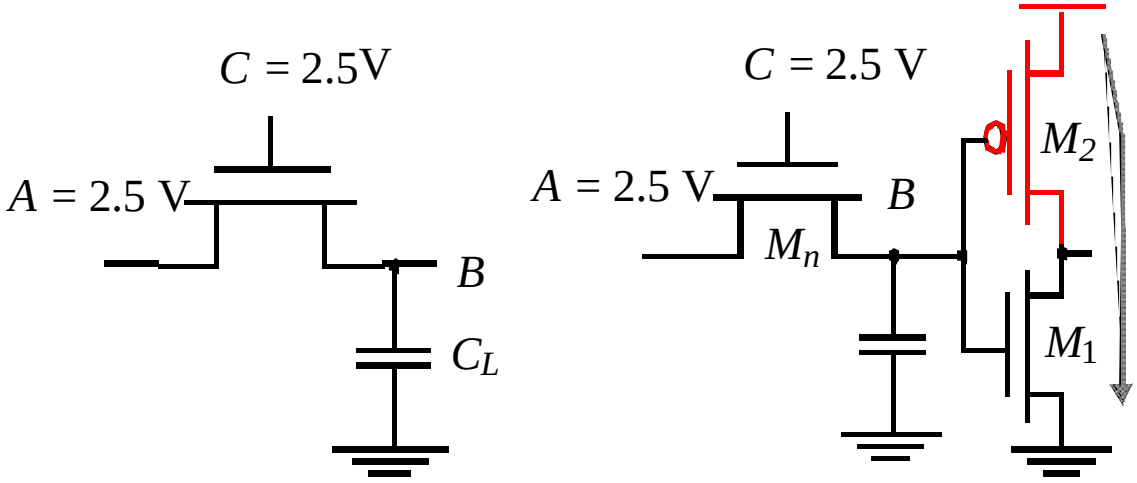
(b)

• Since circuit is differential, complimentary inputs and outputs are available. Although generating differential signals require extra circuitry, complex gates such as XORs, MUXs and adders can be realized efficiently.

• CPL is a static gate, because outputs are connected to Vdd or GND through a low-resistance path (high noise resilience).

• Design is modular – all gates use same topology; only inputs are permuted. This facilitates the design of a library of gates.

Main Problems of NMOS-only Switch

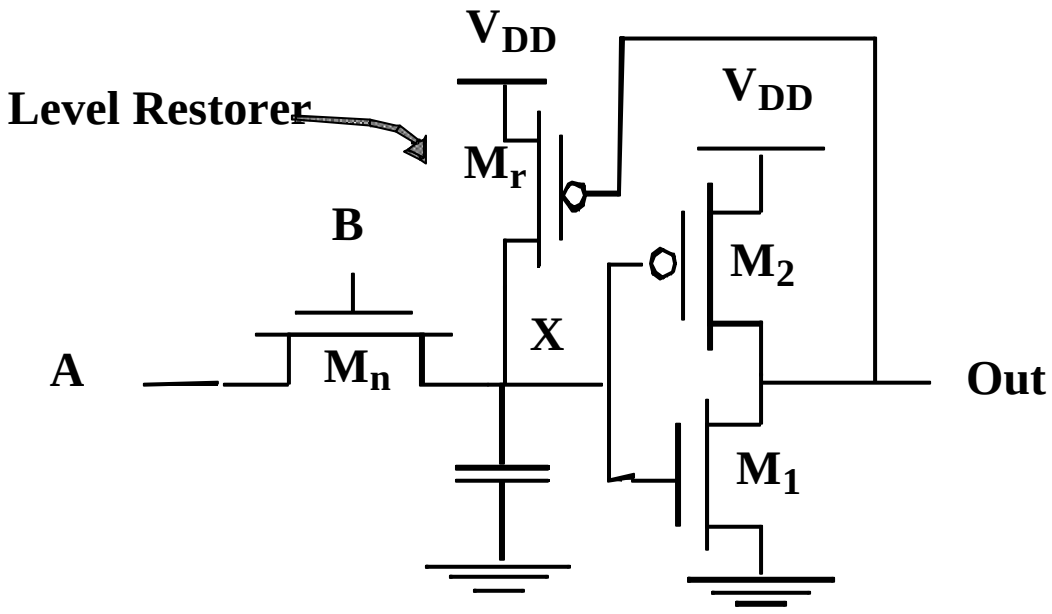


V_B does not pull up to 2.5V, but 2.5V - V_{TN}

Threshold voltage loss causes

static power consumption + slower transition

NMOS Only Logic: Level Restoring Transistor



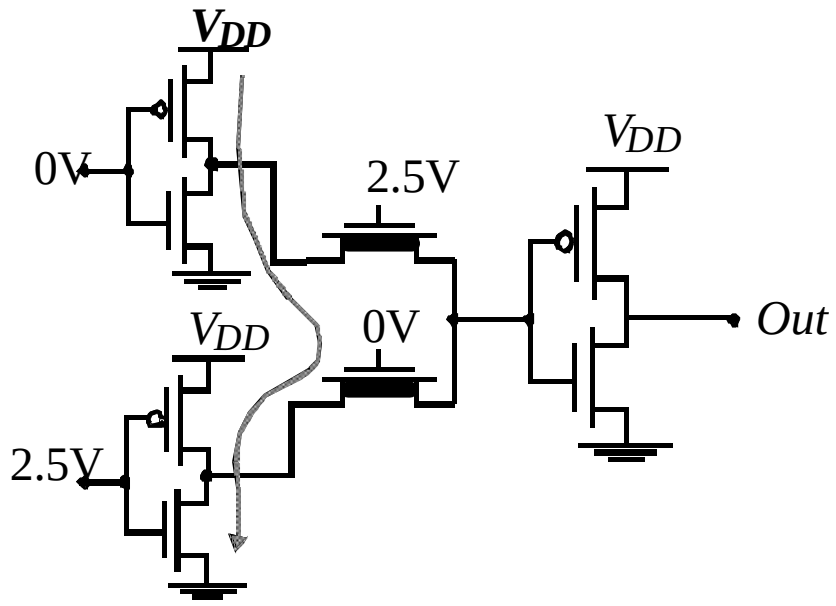
• Advantage: Full Swing. Eliminates static power in inverter + static power through level restorer and pass transistor, since restorer is only active when A is high.

• Restorer adds capacitance, takes away pull down current at X – contention between M_n and M_r (slower switching). Hence M_r must be sized small. M_n and M_r must be sized such that the voltage at node X drops below the threshold of the inverter V_M, which is a function in the sizes of M_1 and M_2.

Solution 2: Single Transistor Pass Gate with V_T~0

Use very low threshold values for NMOS pass transistors, and standard high-threshold devices for inverters.

Note: Body effect will still cause an increase in the threshold voltage.

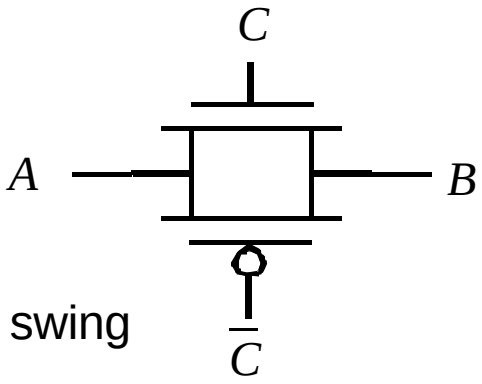


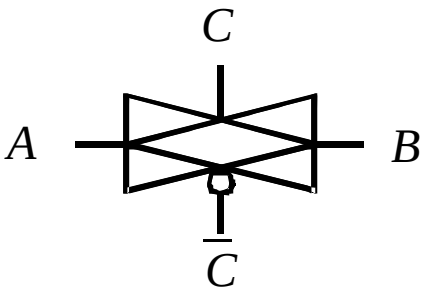
WATCH OUT FOR LEAKAGE CURRENTS (DC Sneak path)

While these leakage paths are not critical when the device is switching constantly, they do pose a large energy overhead when the circuit is in the ideal state.

Solution 3: Transmission Gate

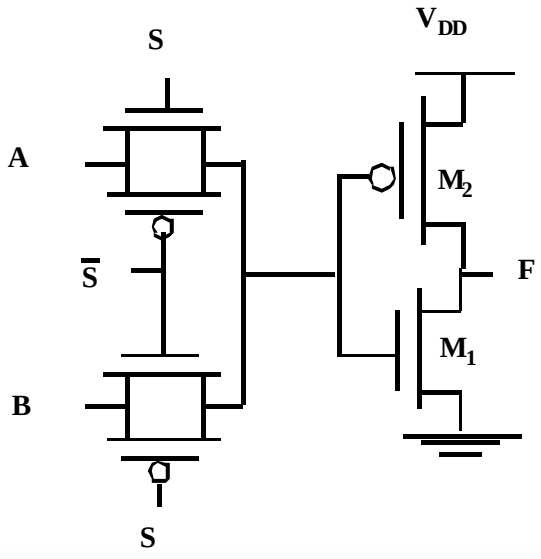
NMOS passes a strong “0”
PMOS passes a strong “1”



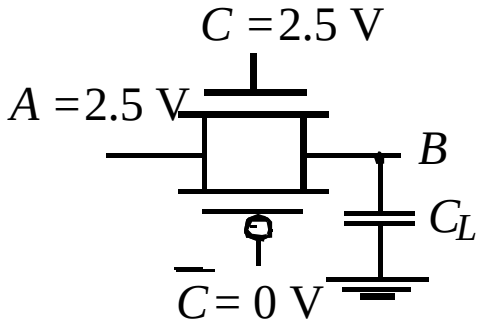


Transmission gates enable rail-to-rail swing

These gates are particularly efficient in implementing MUXs



$\overline{F}=(AS+B\overline{S})$



6 devices vs. 8 for complementary CMOS

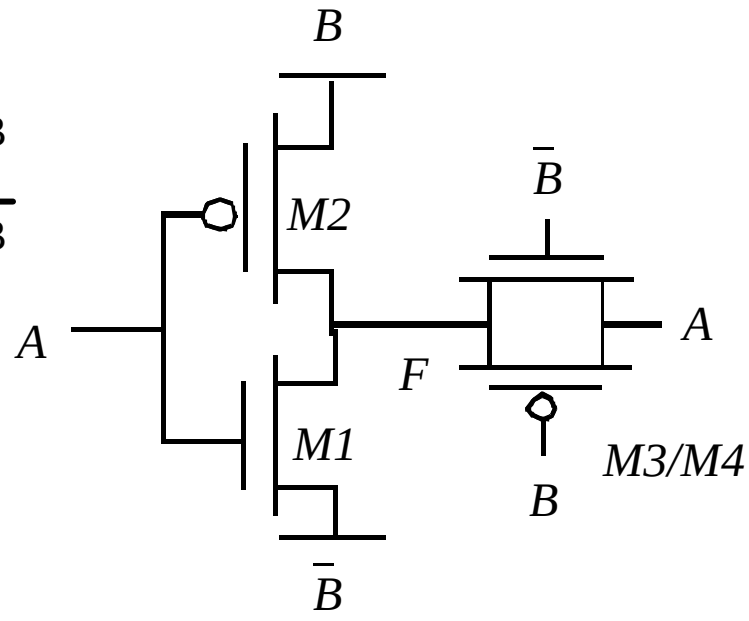
Another Example: Transmission Gate XOR

6 devices (including inverter for B) vs. 12 for complementary CMOS

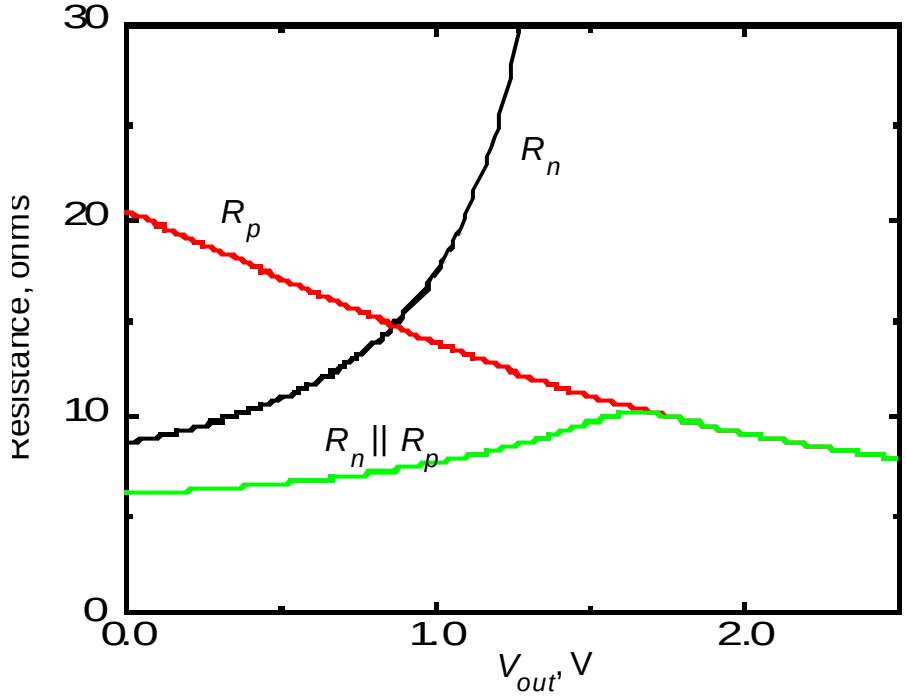
For B=1, M3 & M4 are off, M1 & M2 are on. F = $\overline{A}B$

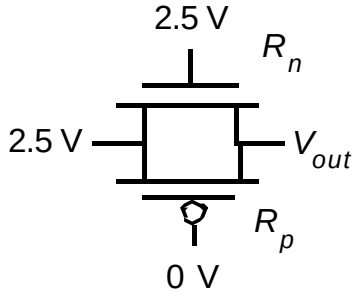
For B=0, M1 & M2 are off. M3 & M4 are on. F = $A\overline{B}$

Regardless of the value of A & B, node F is connected to V_{dd} or GND (static gate)



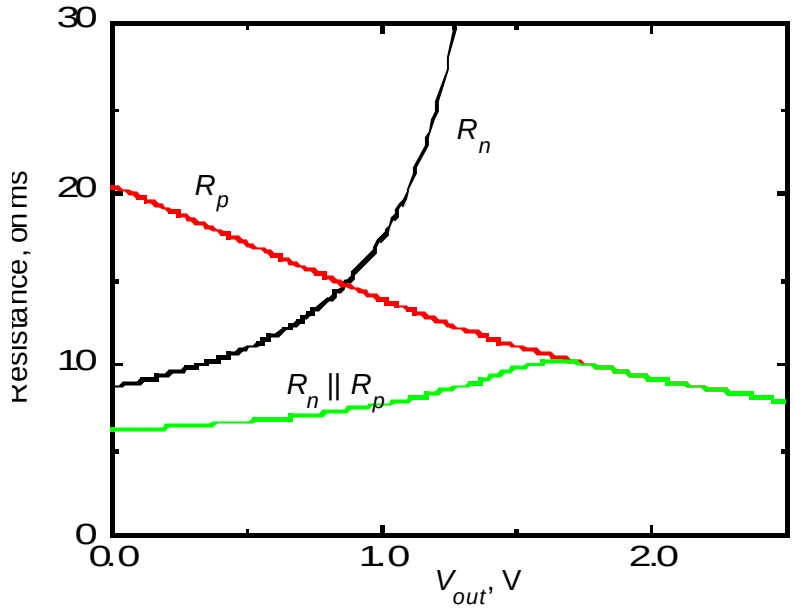
Resistance of Transmission Gate

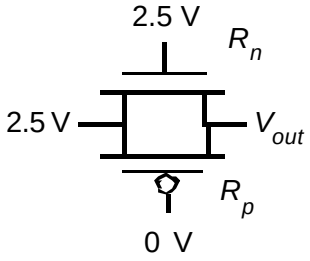




R_n {(V_{dd}-V_{out})/I_n} & R_p {(V_{dd}-V_{out})/I_p} are in parallel. The currents through devices are dependent on value of V_{out} and hence the operating mode of the transistors. During the low-to-high transition, the pass transistors traverse through a number of operation modes.

Since V_d and $V_g = V_{dd}$, the NMOS is either in saturation or off. The PMOS changes from saturation to linear during the transient.





- $V_{out} < |V_{tp}|$: NMOS and PMOS saturated
- $|V_{tp}| < V_{out} < V_{dd} - V_{tn}$: NMOS saturated, PMOS linear
- $V_{dd}-V_{tn} < V_{out}$: NMOS cutoff, PMOS linear

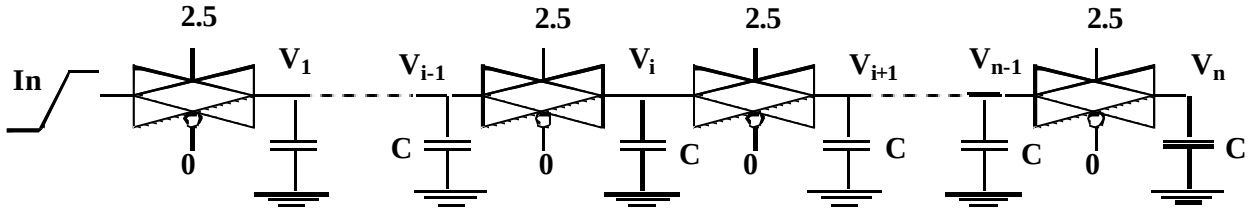
R_{eq} is relatively constant. Thus when analyzing transmission-gate networks, the simplifying assumption that the switch has a constant resistive value is acceptable.

$$R_n = \frac{V_{dd} - V_{out}}{I_n} = \frac{V_{dd} - V_{out}}{k_n\left[(V_{dd} - V_{tn})(V_{dd} - V_{out}) - \frac{(V_{dd} - V_{out})^2}{2}\right]} \approx \frac{1}{k_n(V_{dd} - V_{tn})}$$

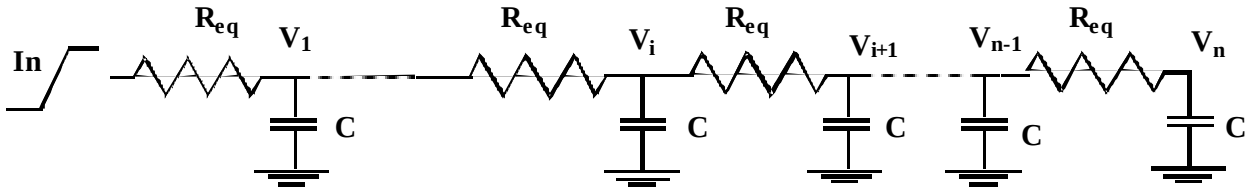
Similarly,

$$R_p = \frac{V_{dd} - V_{out}}{I_p} \approx \frac{1}{k_p(V_{dd} - |V_{tp}|)}$$

Delay in Transmission Gate Networks



(a)



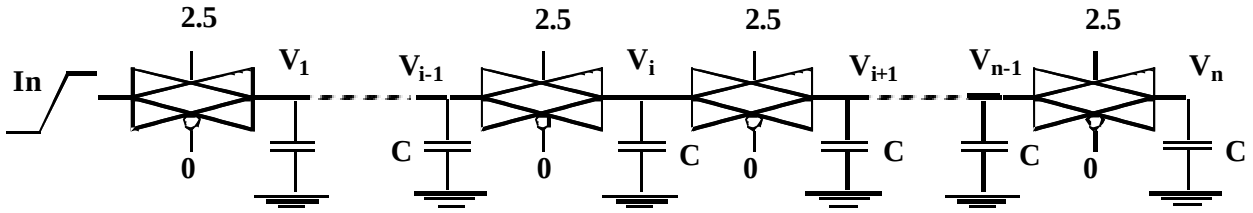
(b)

$$t_p = 0.69\sum_{k=0}^{n} CR_{eq}k = 0.69CR_{eq}\frac{n(n+1)}{2}$$

t_p is proportional to n^2 and increases rapidly with the number of switches in the chain.

Solution: Insert buffers.

Delay Optimization



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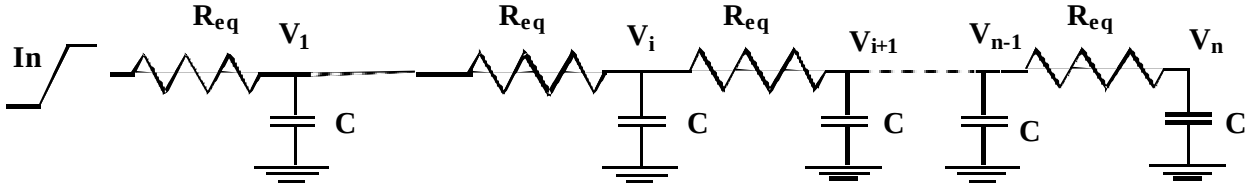
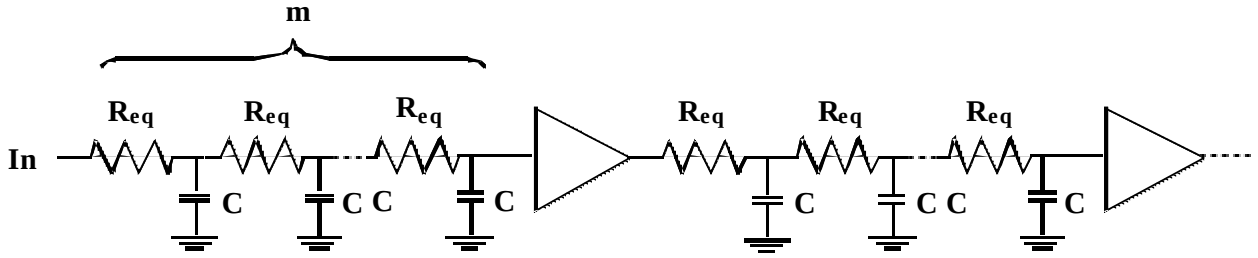


(b)



(c)

$$t_p = 0.69\left[\frac{n}{m} CR_{eq} \frac{m(m+1)}{2}\right] + \left(\frac{n}{m} - 1\right) t_{buf}$$

Linear dependence on n instead of n^2

To find m_{opt}, then $\frac{\partial t_p}{\partial m} = 0$ yielding $m_{opt} = 1.7\sqrt{\frac{t_{buf}}{CR_{eq}}}$