PCB Thermal Design Guide for GaN Enhancement Mode Power Transistors

Contents

1. Embedded GaN*PX*™ Package

The GaN*PX* package, shown in Figure 1, is the first implementation of a discrete GaN power device to be embedded within a laminate construction.
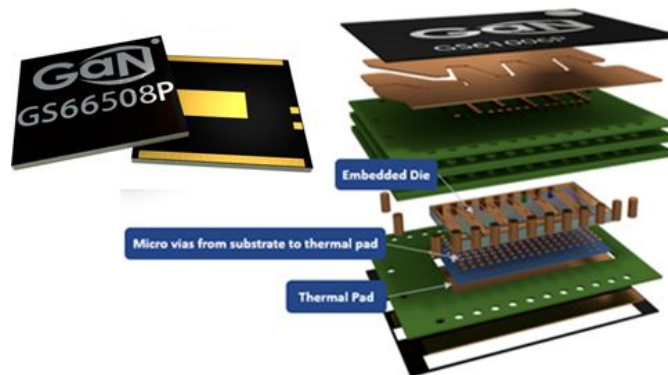

Figure 1 GaN*PX* Embedded Packaging

Conventional packaging techniques such as clip or wire bonding, and molding compounds, are replaced using a series of galvanic processes. The GaN die is protected within the laminate construction. Figure 1 provides a cross sectional view showing a series of printed circuit board plating to form source and drain bus bars that significantly augment the current carrying capacity of the conventional die metallization. This greatly reduces the critical loop inductance and hence the difficulties of driving the high speed, high current switch. The new embedded packaging technique provides a solution for GaN power devices with small volume, low resistance and low inductance.

The embedding technique has been implemented in various package sizes. GS66508P (650 V/30 A) was selected for this thermal analysis.

1.1. Substrate/Thermal Pad Connection

The GaN*PX* package with GaN Systems Enhancement mode HEMTs (E-HEMTs) (GS6650xP and GS6100xP) has a thermal pad on the bottom side. It is electrically connected to the die substrate through the high density micro vias filled with copper to provide low thermal resistance path for optimum cooling. The substrate is electrically isolated from Drain and Source pads on the package.

The substrate or thermal pad must always be connected to Source on the PCB for optimum device performance (Figure 2). Any other substrate connections or connecting substrate to voltage potential other than Source affect the device parameters and reduce device performance. **DO NOT** connect thermal pad to Drain, keep floating or connect to ground (unless the source is also tied to ground).
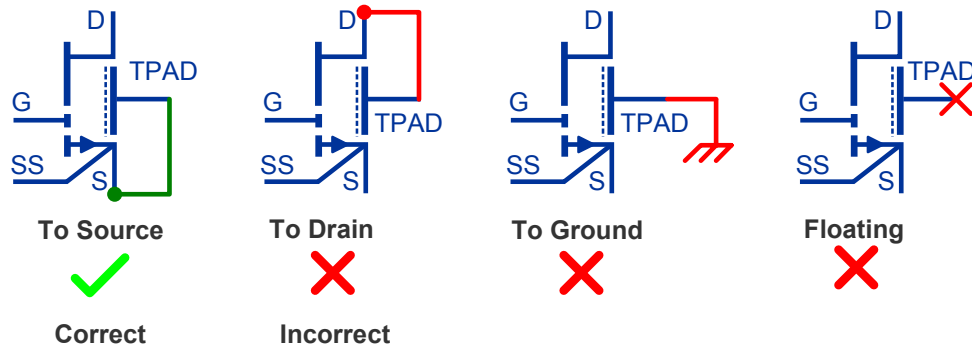

Figure 2 Substrate/Thermal Pad Connection

1.2. Thermal dissipation path

The bottom side cooling with a heat sink via PCB is the most effective cooling method for GaN*PX*. The primary heat dissipation paths of the GaN*PX* package, mounted on the PCB, are illustrated in Figure 3. The majority of heat, generated in the die, flows down to the thermal pad and then transfers to the PCB. The copper planes on the PCB are playing the roles as the heat spreaders and thermal vias provide a low thermal resistance path from the top copper to the bottom side of PCB. A heatsink is attached to the bottom copper plane via a Thermal Interface Material (TIM) and dissipates the heat to the ambient.
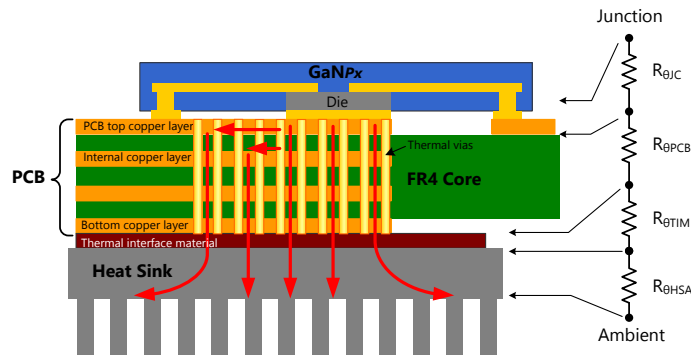

Figure 3 Cross section view of GaN*PX* package and thermal dissipation path

The top side of the package thermal resistance is several times larger than the junction-to-case thermal resistance, for example for GS66508P : $R_{\theta JTop}$=7 °C/W vs. $R_{\theta JC}$=0.5 °C/W. In spite of this, additional cooling can be achieved by using heatsink on both, the top and bottom, sides of the package. The effect of the double-sided cooling will be briefly discussed in the section A4 of this document.

The top side cooling should only be used as additional to the bottom side cooling if needed.

2. PCB design considerations

PCB design is essential for the thermal management of the GaN*PX* package and PCB thermal resistance is the primary consideration for overall system thermal performance. There are several key factors that impact the PCB thermal performance, such as a heat spreading copper pad and thermal vias.

2.1. Heat spreading copper pad

The top copper pad plays important role to conduct the heat from the small area under the device to larger area on the PCB. As such, the top copper layer must have sufficient thickness and area to provide enough heat spreading. It is recommended to always use 2 oz or thicker copper on all layers. The internal and bottom layers also improve the heat spreading. The bottom copper pad serves as the contact surface to the heatsink or Thermal Interface Material (TIM) and it should have sufficient coverage to allow optimum heat transfer to the heatsink.

2.2. Thermal vias

The most effective way to improve vertical heat transfer for FR-4 PCB is to add plated through-hole thermal vias between conductive layers. Since FR-4 material has very low thermal conductivity, thermal vias design is one of the dominating factors for total PCB thermal resistance.

Below are some considerations for thermal vias design:
- Adding open plated through vias to the SMT pad ("Via In Pad") is generally not a common practice as it may create the solder-wicking issue: the solder tends to be drained down into the vias during the reflow process and generates solder voids on the pad. Following steps can be taken to limit this problem:

- o Use small via diameter. The surface tension of solder limits the amount of solder wicking on smaller vias. With 0.3 mm or smaller via diameter, the solder wicking can be reduced.
    - o Fill the vias with thermally conductive materials. It eliminates the solder wicking but adds cost and extra manufacturing step.
- 8 mil (0.2 mm) is typical minimum mechanical drilling size. 12 mil (0.3 mm) is more common and lower cost.
- IPC-6012 specifies minimum 0.8 mil (20 μm) copper plating thickness for Class 2 PCB and 1 mil (25 μm) is standard via plating thickness and will be used for this analysis.

3. PCB Thermal Analysis

A simplified junction-to-ambient compact thermal model for the GaNPX package mounted on PCB can be found in Figure 3, where:
- $R_{\theta JC}$ - junction-to-case (package) thermal resistance;
- $R_{\theta PCB}$ - PCB thermal resistance;
- $R_{\theta TIM}$ - TIM thermal resistance, and
- $R_{\theta HSA}$ - heatsink-to-ambient thermal resistance.

$R_{\theta JC}$ is fixed value that can be obtained from datasheet. PCB and TIM thermal resistance are largely dependent on the PCB layout design so $R_{\theta PCB}$ and $R_{\theta TIM}$ are of interest for this thermal analysis.

$R_{\theta JHS}$ is the total thermal resistance from junction to heatsink surface and is defined as:

$$R_{\theta JHS} = R_{\theta JC} + R_{\theta PCB} + R_{\theta TIM} \qquad \textbf{(Eq.1)}$$

ElectroFlo® thermal analysis software was used for the thermal simulation. All simulations were conducted at a power dissipation of 10 W. An assumption was made that the surface temperature of the heatsink was constant and equal to 25 °C. Thermal interface material GAP3000S30R from Bergquist™ [1] was selected for this analysis with 0.25 mm thickness and thermal conductivity of 3 W/m·K.

3.1. PCB Setup and thermal via pattern

This thermal analysis was based on the following PCB setup:
- Single GS66508P 650 V enhancement mode HEMT.
- Device is placed at standard FR-4 PCB with 1.0 mm and 1.6 mm thicknesses
- 2 oz copper on 2, 4 or 6 layers
- Assume all copper layers are evenly distributed.

Thermal vias:
- 12 mil (0.3 mm) diameter placed on 25 mil (0.64 mm) grid spacing.
- Standard 1 mil (25 μm) copper plating thickness
- No via filling.

3.2. Impact of copper pad area and thermal vias

To create the PCB layout with optimum thermal performance, the first step is to determine the right size for the heat spreading copper pad and how many vias are needed under the thermal pad. To investigate the impact of copper area or number of the vias on the PCB thermal performance, eight PCB layouts were chosen for the thermal analysis (Figure 4):

- Copper pads on all layers are same size.
- The layout starts with the minimal copper area (Layout #1), which is the same size as the package thermal pad. 30 vias (10x3) can be fitted under the thermal pad.
- For each layout additional vias are placed and copper area is increased accordingly.
- The design constraint rule is that no vias are added towards the drain side in order to maintain the same clearance between thermal and Drain pads. Also the left edge of the copper pad keeps minimum 0.5 mm distance from Gate and Source-sense pads. There will be no vias added on the left side the package as that area is typically used for gate driver circuit.
- Starting at layout #5, the copper pad covers both thermal and Source pads. Layout #1 through layout #4 have the thermal pad separated from the Source and these layouts are only for the thermal analysis. In the actual circuit the thermal pad must always be electrically connected to the Source.
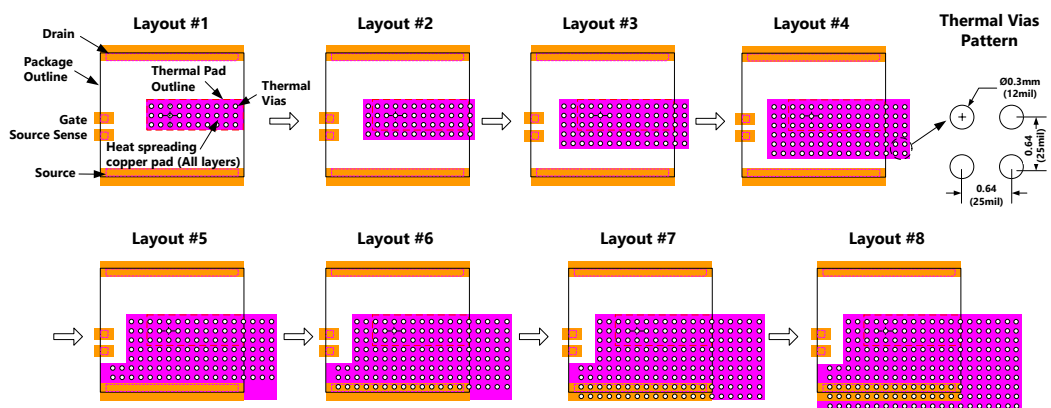

Figure 4 PCB Layouts for copper area optimization

All 8 PCB layouts were analyzed on standard 1.6 mm PCB with 2 copper layers (2 oz copper thickness). Figure 5 shows the example of the thermal analysis results.
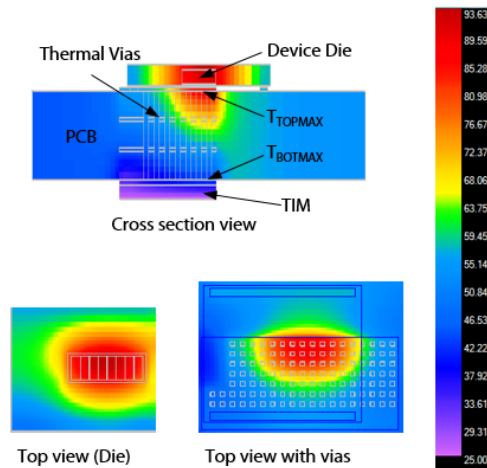
Figure 5 Example of thermal simulation results (Layout #5)

The PCB thermal resistance R$_{\theta PCB}$ is defined by:

$$\mathbf{R_{\theta PCB}} = \frac{T_{TOPMAX} - T_{BOTMAX}}{P_{DISS}} \qquad \textbf{(Eq.2)}$$

where T$_{TOPMAX}$ and T$_{BOTMAX}$ are the maximum temperatures on the top and bottom copper layers, which are approximately located at the center of the die; P$_{DISS}$ is power dissipation (P$_{DISS}$ = 10 W).

The thermal analysis results are listed in Table 1 and Figure 6 show the correlation between the number of vias, copper area and thermal resistance. Layout #1 has the highest thermal resistance as expected. Both PCB and TIM thermal resistances decrease with the increasing of via numbers and copper area. When number of thermal vias increase from 30 to 210 (Layout #1 to #8), the PCB thermal resistance R$_{\theta PCB}$ drops almost 2.4 times from 11.5 °C/W to 4.8 °C/W. The TIM thermal resistance R$_{\theta TIM}$ also reduces about 3 times as the contact area increases.

Table 1 Thermal resistance breakdown for 8 PCB layouts

PCB Layout	Number of vias	R$_{\theta PCB}$ (°C/W)	R$_{\theta TIM}$ (°C/W)	R$_{\theta JHS}$ (°C/W)
#1	30	11.54	5.25	17.29
#2	48	7.97	3.98	12.45
#3	70	6.46	2.83	9.79
#4	96	5.65	2.13	8.46

#5	123	5.13	1.95	7.58
#6	150	5.05	1.92	7.47
#7	179	4.91	1.85	7.29
#8	210	4.87	1.80	7.18

We can see that layout #5 with 123 vias achieves about 95 % of total reduction of the thermal resistance. After that adding more vias (or increasing copper pad size accordingly) starts to become a matter of diminishing return. By increasing number of vias from 123 to 210 the PCB thermal resistance reduces only by 5 %. This is due to the limited heat spreading in horizontal direction as can be seen in Figure 6. The copper pad and thermal vias become less effective when they are located further away from the heat source.
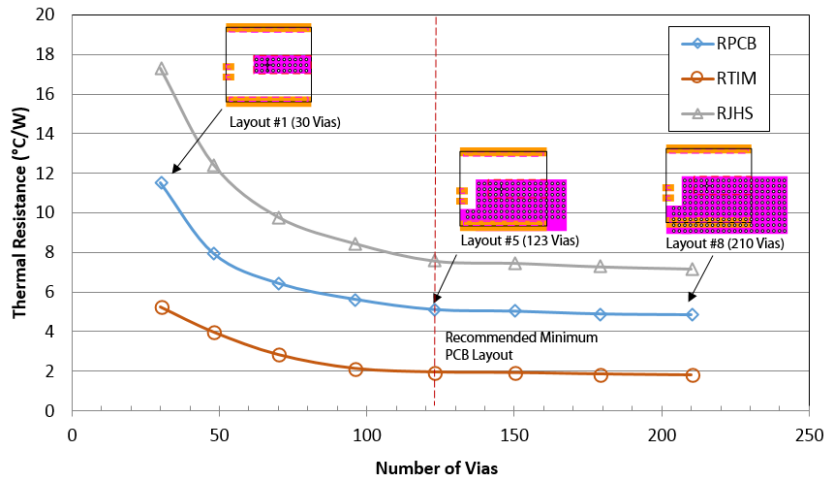

Figure 6 PCB thermal resistance for 8 PCB layouts

Based on the thermal analysis above, layout #5 was chosen as the recommended minimum PCB layout design. For optimum PCB thermal performance, it is recommended that the copper pad and thermal vias should cover at least 10x 5 mm area (50 mm^2) under the thermal pad (or approximately 120 thermal vias), as shown in Figure 7.
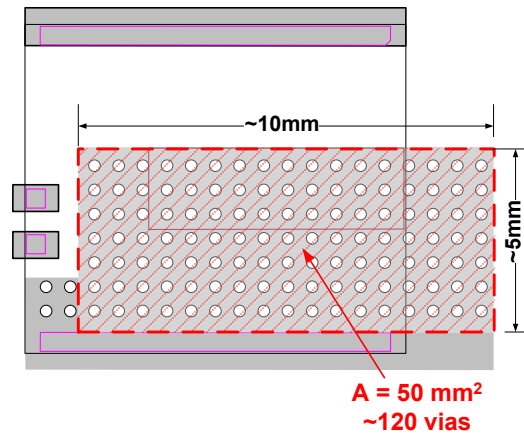
Figure 7 Recommended minimum copper area under thermal pad

3.3. Impact of copper layers and PCB thickness

Adding more internal copper layers on the PCB structure improves the PCB thermal performance. It is known that 2, 4 or 6 layers PCB are typical for power application. If design allows it is recommended to use at least 4 layer PCB design. While 1.6mm is standard thickness for FR-4 PCB, 1.0mm PCB is also common and can be used to further improve the PCB thermal resistance. Using recommended minimum PCB layout Figure 8 and Table 2 show the thermal resistance results for 2, 4, and 6 layers PCB with 1.6 mm and 1.0 mm thickness. Both PCB and TIM thermal resistances reduce with more PCB layers because adding internal layers not only improve vertical

heat transfer through the PCB, but also increase the horizontal heat spreading resulting in more even heat distribution on the TIM surface.
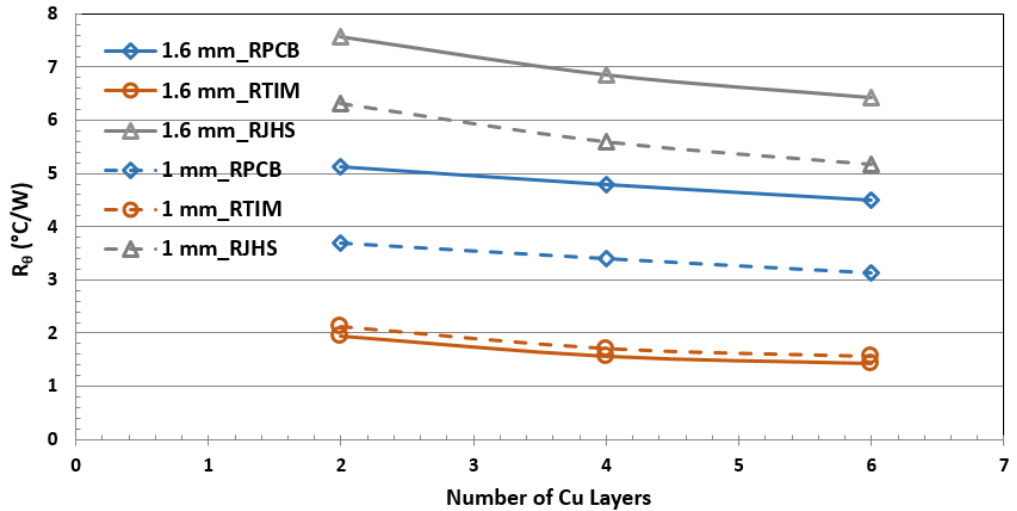

Figure 8 Impact of copper layers and PCB thickness on thermal resistance

Table 2 Thermal resistance with different number of copper layers and PCB thickness

Layers	1.6 mm PCB			1.0 mm PCB		
	$R_{\theta PCB}$ (°C/W)	$R_{\theta TIM}$ (°C/W)	$R_{\theta JHS}$ (°C/W)	$R_{\theta PCB}$ (°C/W)	$R_{\theta TIM}$ (°C/W)	$R_{\theta JHS}$ (°C/W)
2	5.13	1.95	7.58	3.69	2.12	6.31
4	4.8	1.56	6.86	3.39	1.71	5.6
6	4.51	1.42	6.43	3.12	1.56	5.18

For 1.6 mm PCB, the total junction-to-heatsink thermal resistance decrease about 10 % for each 2 layers. Reducing PCB thickness from 1.6 mm to 1.0 mm provides about 30 % improvement on PCB thermal resistance. PCB thickness has less effect on TIM thermal performance and actually increases TIM thermal resistance by about 10 %. It can be seen, that using 1.0 mm PCB is more effective than adding more copper layers for the standard PCB of 1.6 mm thickness. For example, 2 layer 1 mm PCB has lower thermal resistance than 6-layer 1.6 mm PCB. So it is recommended to use 1.0 mm PCB, if design allows.

Note, that not all PCB manufacturers can reliably produce 6-layer 1.0 mm PCB with 2 oz copper. It is recommended to always confirm with your PCB manufacturer before using any PCB design discussed in this application note.

3.4. Thermal Interface Material

The TIM thermal resistance $R_{\theta TIM}$ is critical for the overall device thermal performance as it accounts for about 20-30 % of the total junction to heatsink thermal resistance. As shown in the thermal analysis before, $R_{\theta TIM}$ is complicated to calculate numerically as it varies with different PCB layouts and number of copper layers. So far all thermal analysis results above are based on one type of TIM (GAP3000S30R, 0.25 mm thick with thermal conductivity of 3 W/m·K).

Figure 9 shows the breakdown of thermal resistances with 4 different types of TIMs from Bergquist®.
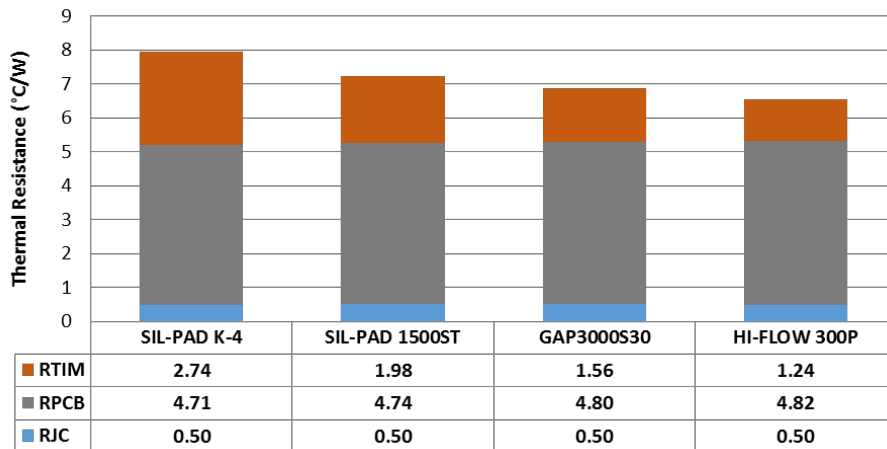

	SIL-PAD K-4	SIL-PAD 1500ST	GAP3000S30	HI-FLOW 300P
■ RTIM	2.74	1.98	1.56	1.24
■ RPCB	4.71	4.74	4.80	4.82
■ RJC	0.50	0.50	0.50	0.50

Figure 9 Thermal resistance breakdown (4-layer 1.6 mm PCB with recommended footprint) using 4 different TIMs

In absent of the detailed thermal simulation or measurement, TIM thermal resistance $R_{\theta TIM}$ can be also estimated by using the following equation:

$$R_{\theta TIM} = L/(A \cdot k) \qquad \text{(Eq. 3)}$$

where L is the TIM thickness (m); A is the effective contact area (m²) and k is the thermal conductivity of TIM (W/m·K), which can be obtained from TIM datasheet.

Note that A in the Eq. 3 is not necessarily the total contact copper area at the bottom layer. Instead it is defined as "effective" contact area depending on the PCB heat spreading. The effective contact area increases when thicker or more layers of copper are used.

For recommended PCB footprint, A = 56 mm^2 can be used to provide reasonable estimation for standard 1.6 mm PCB with typical error < 10 % compared to detailed thermal simulation results.

4. Maximum power capability

4.1. Junction-to-Ambient Thermal Resistance

The total junction-to-ambient thermal resistance $R_{\theta JA}$ is essential for designer to estimate the maximum power capacity of the system and can be calculated by following equation:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta PCB} + R_{\theta TIM} + R_{\theta HSA} \qquad \textbf{(Eq.4)}$$

where $R_{\theta PCB}$ and $R_{\theta TIM}$ have been discussed in the previous section and $R_{\theta JC}$ is a fixed value that can be obtained from the device datasheet (0.5 °C/W for GS66508P). The heatsink to ambient $R_{\theta HSA}$ thermal resistance is largely dependent on the heatsink design and airflow.

4.2. Power calculation

Once the junction-to-ambient thermal resistance is determined, the maximum allowed power dissipation can be calculated using the following equation:

$$P_{DMAX} = \Delta T_{MAX}/R_{\theta JA} \qquad \textbf{(Eq.5)}$$

where ΔT_{MAX} is the maximum allowed temperature rising above ambient. Figure 10 shows the calculated maximum power dissipation vs. heatsink-to-ambient thermal resistance (4-layer 1.6 mm PCB, ΔT_{MAX} = 50 °C, 75 °C and 100 °C), which can be used to evaluate system thermal performance. For example, if a system design has heatsink-to-ambient thermal resistance estimated about 3 °C/W and ΔT_{MAX} = 100 °C, the maximum allowed power loss will be about 10 W per single device using the recommended PCB footprint on 4-layer 1.6 mm PCB.
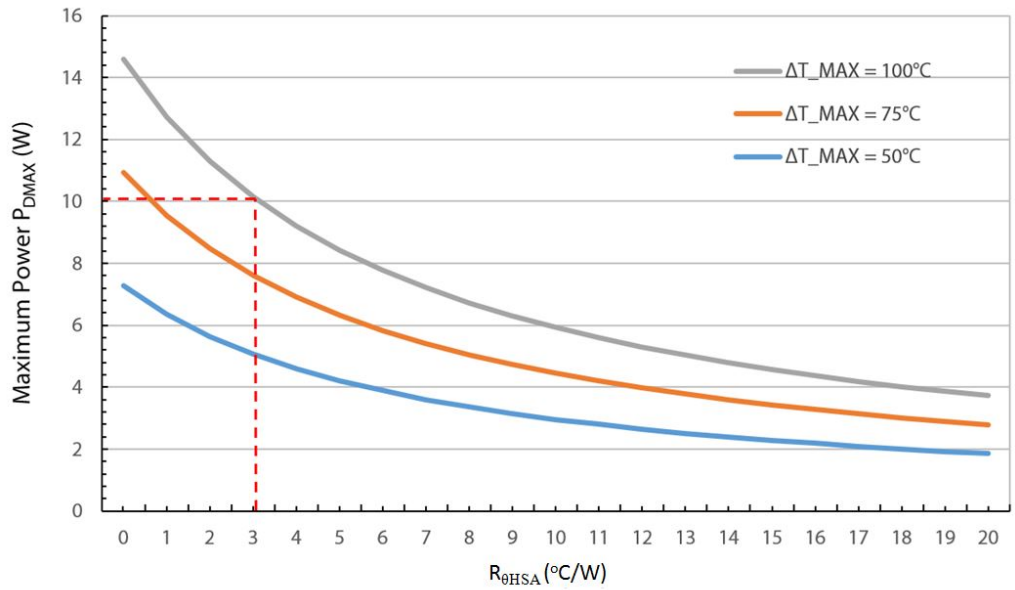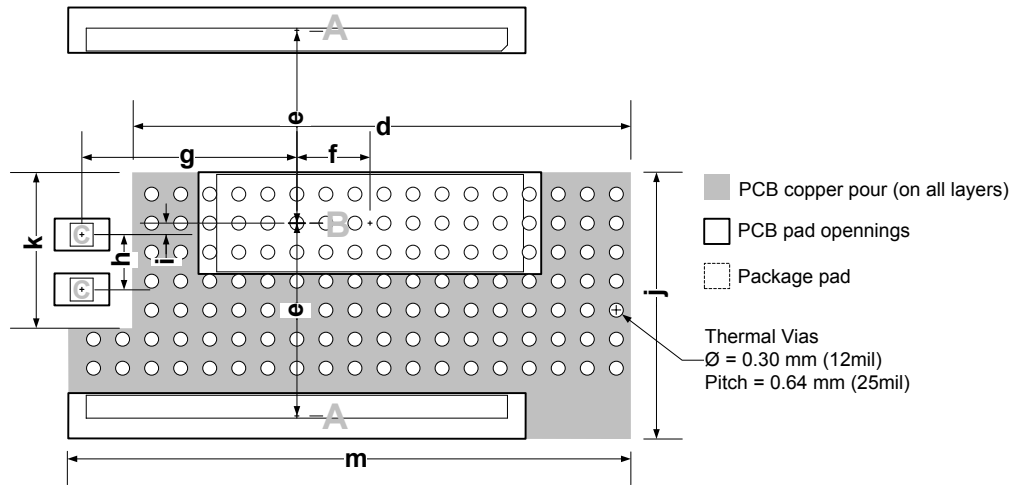
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Figure 10 Maximum power dissipation for GS66508P (4-layer 1.6 mm PCB, ΔT$_{MAX}$ = 50 °C, 75 °C and 100 °C)

Appendix

A.1. Recommended PCB footprint for GS66508P

Pad Dimension

Pad	X-size		Y-size	
	mm	inch	mm	inch
A	10	0.39	1	0.039
B	7.5	0.3	2.2	0.087
C	1.2	0.05	0.7	0.028

All Dimensions are typical

	mm	inch		mm	inch
d	10.9	0.429	i	0.25	0.010
e	4.22	0.166	j	5.84	0.230
f	1.6	0.063	k	3.42	0.135
g	4.7	0.185	m	12.3	0.484
h	1.2	0.047			

Figure 11 Recommended PCB footprint for GS66508P

A.2. PCB clearance

The recommended PCB footprint for GS66508P has 2.6 mm clearance between Drain and thermal pads. According to IPC 2221 [2] table 6-1, 2.6 mm meets the minimum spacing requirement for 520 V DC operation on uncoated bare board (B2 type, sea level up to 3050 m), which is sufficient for most AC/DC converter with rectified DC bus voltage up to 400 V DC. However, if the assembly is to be encapsulated or operated at lower voltage, this clearance can be reduced. For example, if conformal coating is applied, the PCB clearance can be reduced to 1.6 mm for 520 V DC.

This provides an opportunity to further improve the PCB thermal resistance. As shown in Figure 5, the heat source (die) is located at the edge of the copper pad, which is not the best case for heat spreading. Ideally the heat source should be located at the center of the copper pad. The junction-to-heatsink thermal resistance can be reduced by about 20 % if two rows of thermal vias are added (PCB clearance reduces from 2.6 mm to 1.33 mm) on standard 4-layer 1.6 mm PCB , as shown in Figure 12.
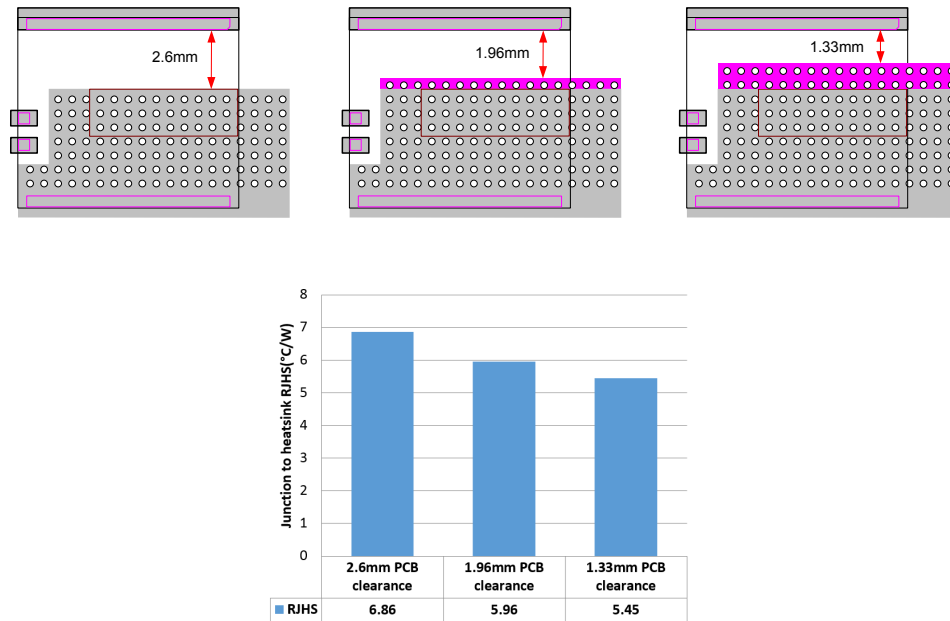
Figure 12 Thermal resistance improvement with smaller PCB clearance (4-layer 1.6 mm PCB)

A.3. Thermal simulation and temperature measurement comparison

4-layer 1.6 mm PCB with 123 thermal vias was manufactured and GS66508P was mounted on it. During this process the thermal vias were filled with solder. The temperature was measured using the FLIR T420 Series thermal camera. Power dissipation was 10 W. TIM was not used during this comparison. Figure 12 shows the temperature measurement and the thermal simulation results.
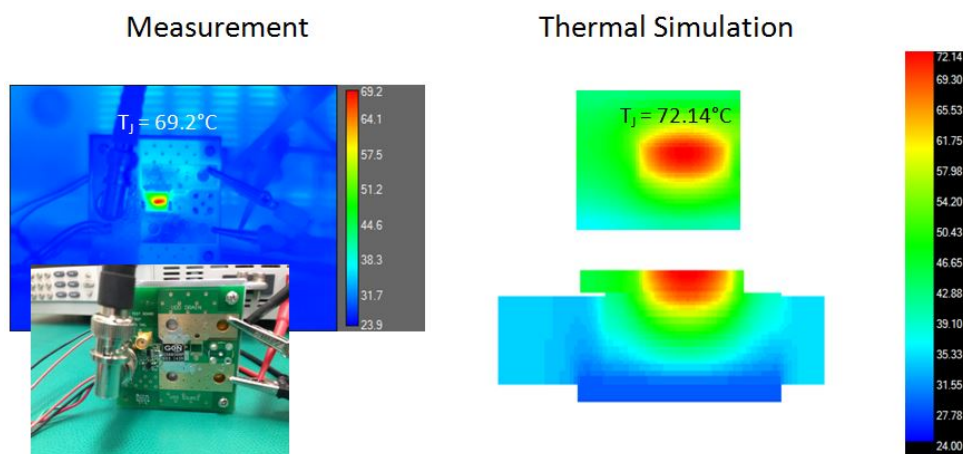

Figure 13 Temperature measurement and thermal simulation results comparison

As can be seen, a good agreement between measurement and thermal simulation was obtained (with accuracy~5 %).

A.4. GS66508P double-sided cooling

As mention in Section 1.2, during traditional cooling of GaN*PX* , the heat transferred from the die through the PCB to heatsink. GaN*PX* is very thin package: the thickness is 0.45 mm. The additional heat pass removal can be created by using extra heatsink on top of the package, which is covered by a layer of soldermask and silkscreen. It has uneven surface and is not designed to withstand high voltage or provide safety insulation. If a heatsink is attached on the top of the package, a layer of interface material with High Voltage (HV) insulation must be added between heatsink and device top surface to fill the gap and provide safety insulation.

The thermal simulation set-up for double-sided cooling is shown in Figure 14. Device GS66508P was mounted on 4-layer 1.6 mm PCB with 123 thermal vias. GAP3000S30R, 0.25 mm thick with thermal conductivity of 3 W/m·K TIM layer was used on the top of the package. Assumption was made that the infinite heatsinks were used on the top of the package and the bottom side of TIM layer under the PCB and they provided the TIM layers temperature of 25 °C.
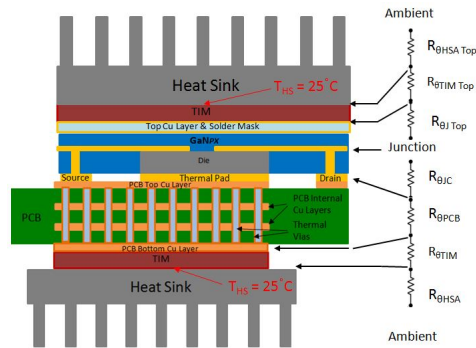

Figure 14 Double-sided cooling thermal simulation set-up

In this case the thermal resistance R$_{\theta JHS}$ can be calculated using a one dimensional model. As heat is transferred via the top and bottom side of the package, the thermal resistances to the top and bottom side have to be considered. The junction-to-heatsink thermal resistance can be calculated using the equation for parallel connection of thermal resistances:

$$\mathbf{R_{\theta JHS}} = \frac{R_{\theta JHSBottom} \cdot R_{\theta JHSTop}}{R_{\theta JHSBottom} + R_{\theta JHStop}} \qquad \textbf{(Eq.6)}$$

where: $R_{\theta JHSBottom}$ - bottom junction-to-heatsink thermal resistance (see Eq. 1); $R_{\theta JHSTop}$ - top junction-to-heatsink thermal resistance is defined as:

$$R_{\theta JHSTop} = R_{\theta JTop} + R_{\theta TIMTop} \qquad \textbf{(Eq.7)}$$

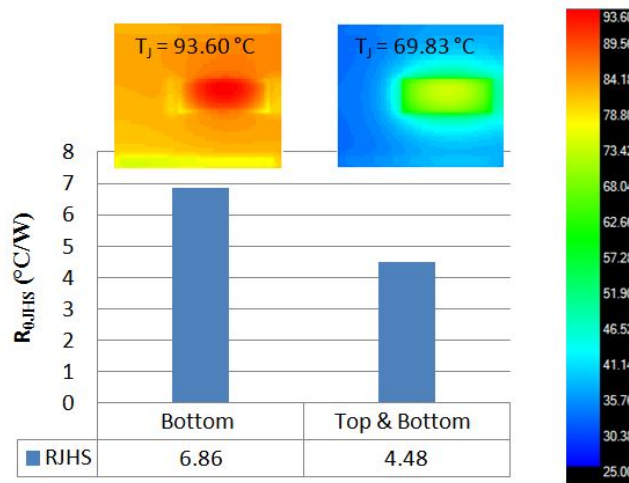Figure 15 shows the impact of the double-sided cooling on GaN$_{PX}$ thermal performance.

Figure 15 GaN$_{PX}$ thermal performance using the double-sided cooling

Double-sided cooling improves the package thermal performance by 35 %. This result is valid only when the bottom and top heatsinks are able to cool the TIM layers up to 25 °C. When the temperature boundary conditions are changed, the effect of double-sided cooling will be different and more thermal simulations will be needed to predict the device junction temperature.

The top side cooling should only be used as additional to the bottom side cooling.

Summary

This note has outlined PCB thermal design and layout considerations for using GaN*PX* devices (GS66508P) in real applications.

References

1. http://www.bergquistcompany.com/thermal_materials/gap-pad.htm
2. IPC-2221B Generic Standard on Printed Board Design

www.gansystems.com   North America・Europe・Asia