PCIe® Compliance Updates

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Synopsys

Disclaimer

The information in this presentation refers to specifications still in the development process. This presentation reflects the current thinking of various PCI-SIG® workgroups, but all material is subject to change before the specifications are released.

PCIe 4.0 Compliance Program Status

PCI Express 4.0 Time Frame

Test Specifications

- Config Test Specification – Rev 0.3 Work Group Approved
- Link/Transaction Test Specification – Rev 0.3 Work Group Approved
- System Firmware (BIOS) Test Specification – Rev 0.3 Work Group Approved
- Electrical Test Specification – Rev 0.3 Work Group Approved
- Retimer Test Specification – 0.3 Work Group Approved

Integrator's List

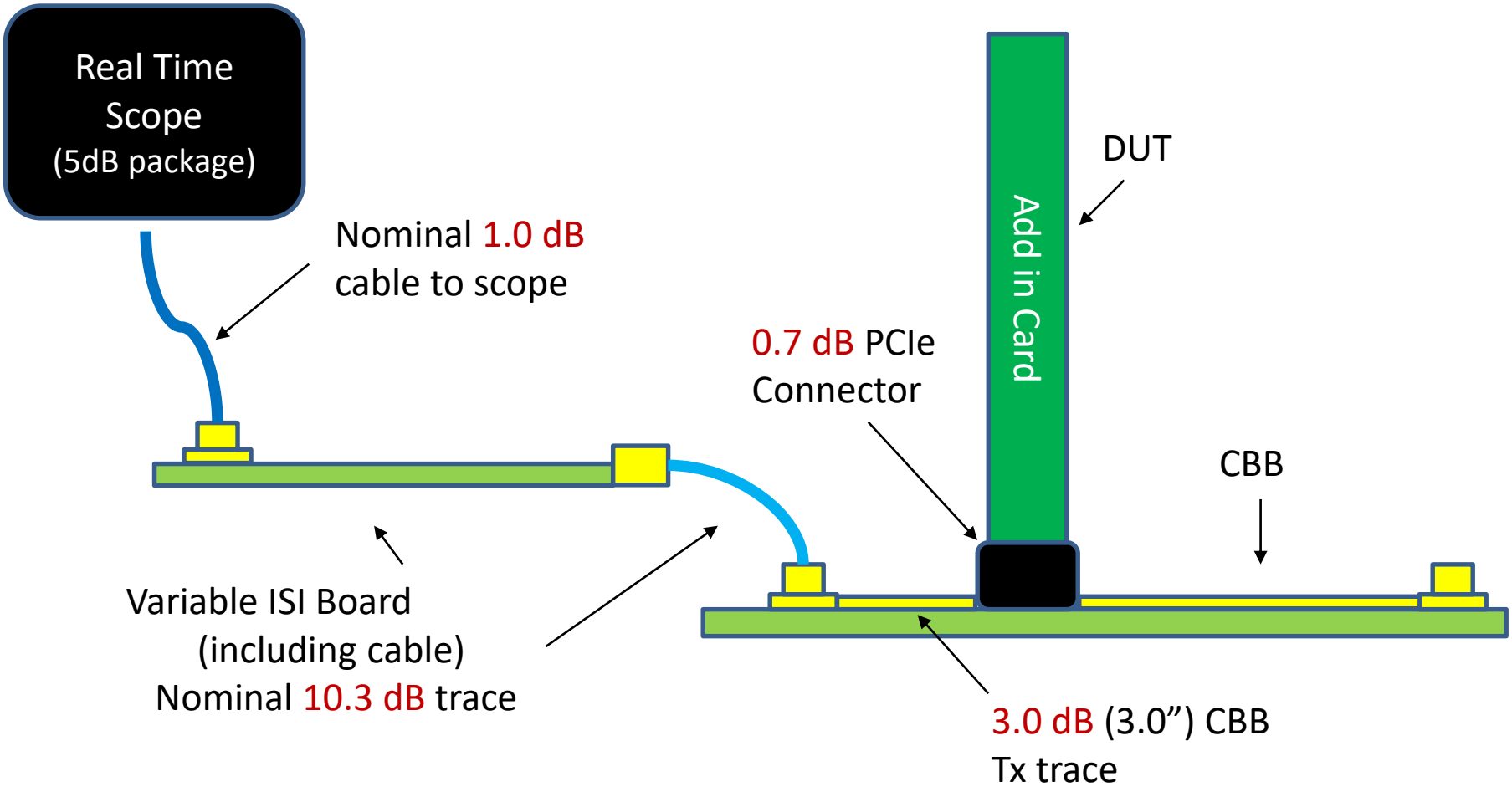
- Pre-FYI testing was done in April and will continue until official FYI status is reached
- FYI testing targeting late 2017
- Official testing targeting middle 2018

PCIe 4.0 Electrical Tests Under Development

PCIe 4.0
Electrical Tests Under Development

- **Tx signal quality test at 16GT/s**
  - End of channel eye diagram
- **Tx preset equalization test at 16GT/s**
  - Preset 0 – Preset 10
- **16.0GT/s receiver test**
  - Stressed eye receiver loopback test
- **Link equalization handshaking at 16GT/s**
  - Tx starts with correct preset requested through protocol
  - Tx responds to protocol changes and adjusts
  - Rx correctly adjusts the link Tx and operates with a stressed eye
- **All 2.5/5.0/8.0GT/s Testing Still Required for 4.0 Integrators List for a 16GT/s Capable Device**

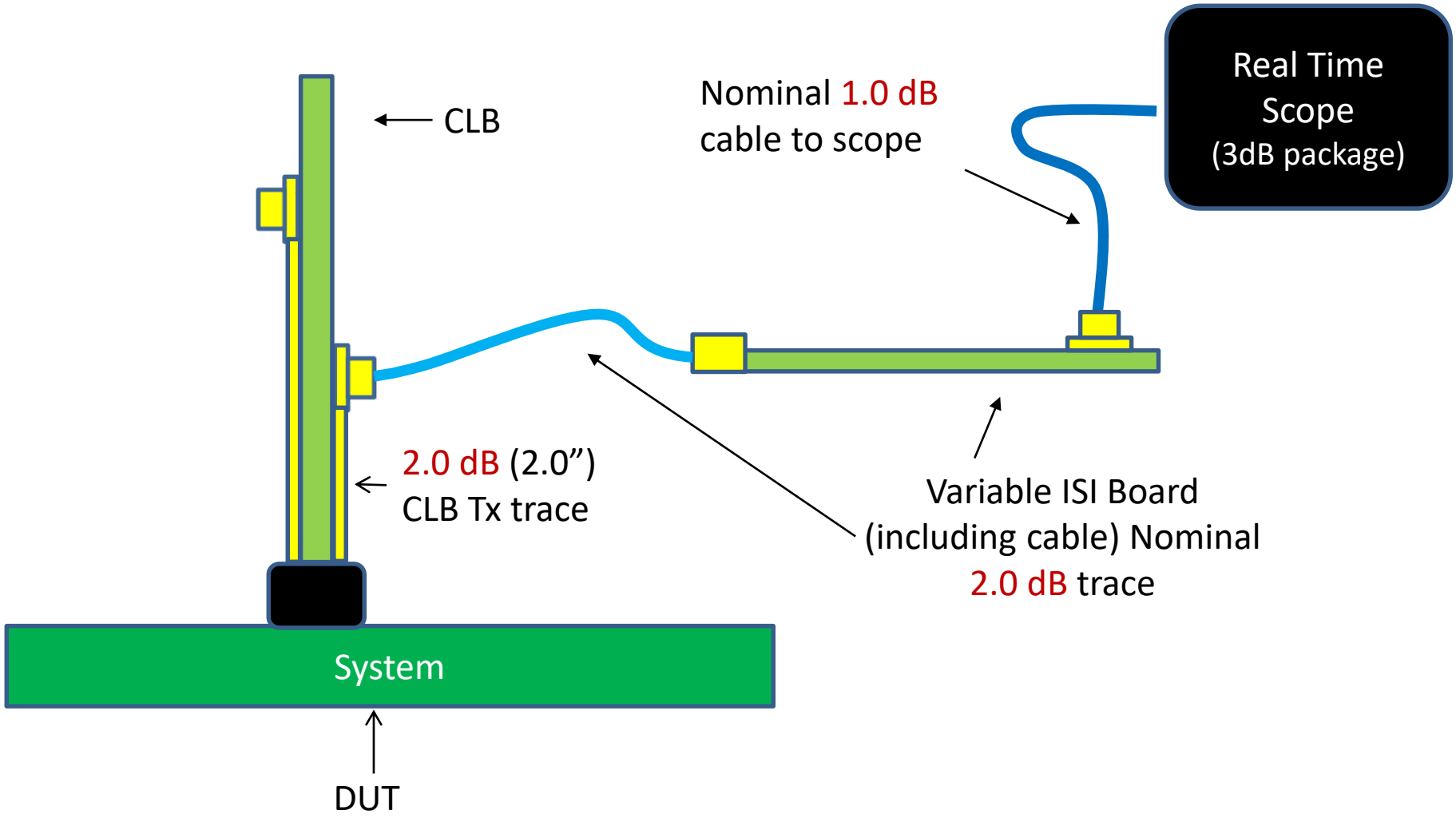
PCIe 4.0 (Add-in Card)
Tx Signal Quality Test at 16 GT/s



PCIe 4.0 (Add-in Card)
Tx Signal Quality Test at 16 GT/s

- **Channel Setup**
  - Add-in Card plugs into CBB -> Variable ISI Board -> Scope
  - 20dB at 8GHz of additional loss (including package embedding)
- **Power on CBB**
- **Scope bandwidth is 25GHz**
- **5dB package model embedded on scope**
- **Toggle DUT to transmit 16GT/s Compliance Pattern**
  - 1ms pulse of 100MHz clock signal into Rx Lane0
- **Capture 2.0M UI waveform for every Tx EQ Preset**
- **Waveforms post processed using SigTest**
  - Time Domain CDR algorithm used to recover clock
  - Behavioral Rx Equalization applied
  - Eye width & Eye height @ E-12
  - Each lane must pass SigTest analysis for at least one Tx EQ Preset
    - EW > 0.3UI (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)
    - EH > 15mV (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)

PCIe 4.0 (System)
Tx Signal Quality Test at 16 GT/s



PCIe 4.0 (System)
Tx Signal Quality Test at 16 GT/s

- **Channel Setup**
  - CLB plugs into system -> Variable ISI Board -> Scope
  - 8dB at 8GHz of additional loss (including package embedding)
- **Power on System**
- **Scope bandwidth = 25GHz**
- **3dB package model embedded on scope**
- **Toggle DUT to transmit 16GT/s Compliance Pattern**
  - 1ms pulse of 100MHz clock signal into Rx Lane0
- **Capture 2.0M UI waveform for every Tx EQ Preset**
- **Waveforms post processed using SigTest**
  - Ref clock captured with data waveform and used for clock recovery
  - Behavioral Rx Equalization applied
  - Eye width & Eye height @ E-12
  - Each lane must pass SigTest analysis for at least one Tx EQ Preset
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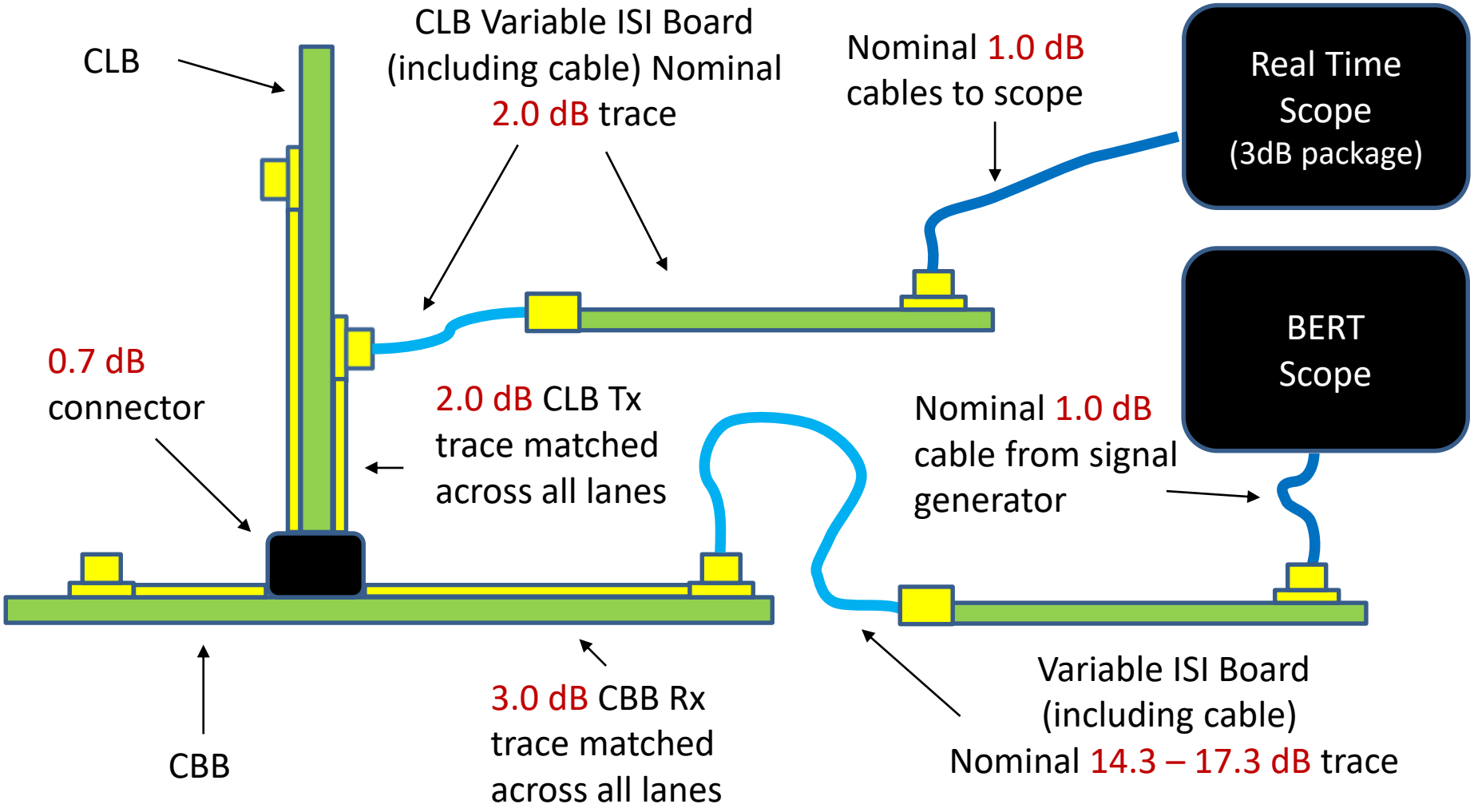
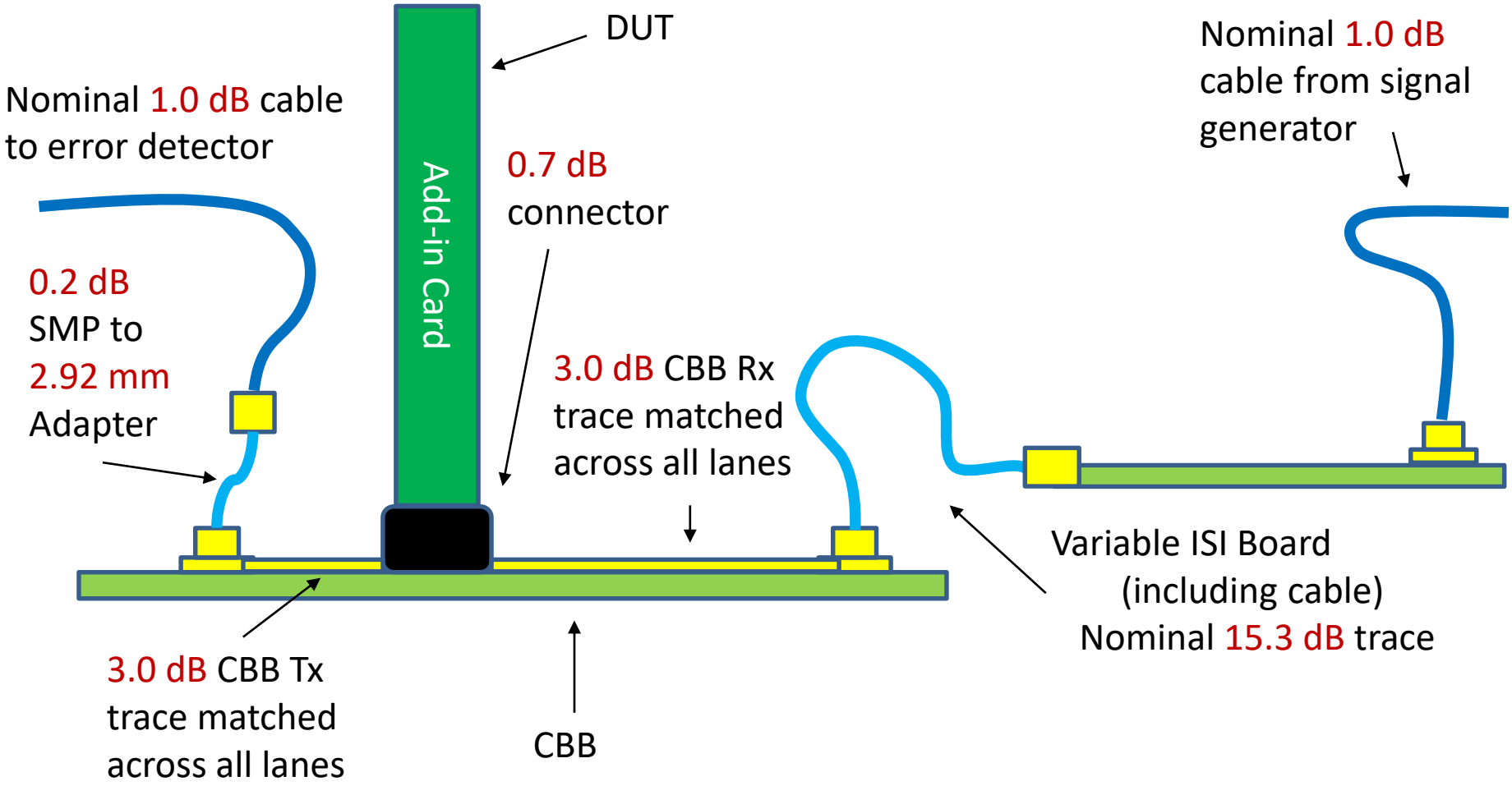
PCIe 4.0 (Add-in Card)
Rx Stressed Eye Calibration at 16GT/s



PCIe 4.0 (Add-in Card)
Rx Stressed Eye Calibration at 16GT/s

- **Calibrate Swing & Tx EQ Presets**
  - Setup - SMA cable from BERT to Scope
  - Swing calibrated to 800mV differential
  - Calibrate voltage levels for Preset 0 - 9
- **Calibrate Rj & Sj**
  - Setup - SMA cable from BERT to Scope
  - Rj – 1ps RMS (clock pattern used)
  - Sj – 0.1UI (16GT/s compliance pattern used)
- **Channel Setup**
  - BERT -> Variable ISI -> CBB -> CLB -> Variable ISI -> Scope
  - 27 – 30dB at 8GHz of additional loss (including 3dB package embedding)
- **Calibrate DMI & CMI**
  - DMI – 14mV (End of 27dB Channel)
  - CMI – 150mV (End of 27dB Channel)
- **Channel Selection**
  - Increase channel loss from 27 to 30dB
  - Find channel where the eye width/height is closest to target without dropping below
    - Must use Optimal Tx EQ Preset which is the Preset which gives the largest eye area
- **Eye Width & Eye Height Calibration**
  - Optimal Tx EQ Preset is used with final channel
  - Adjust Sj, DMI, & Swing until eye width/height (measured with SigTest) targets are achieved
  - EW = 18.75 +/- 0.5ps EH = 15mV +/-1.5mV

PCIe 4.0 (Add-in Card)
Rx Stressed Eye Test at 16GT/s



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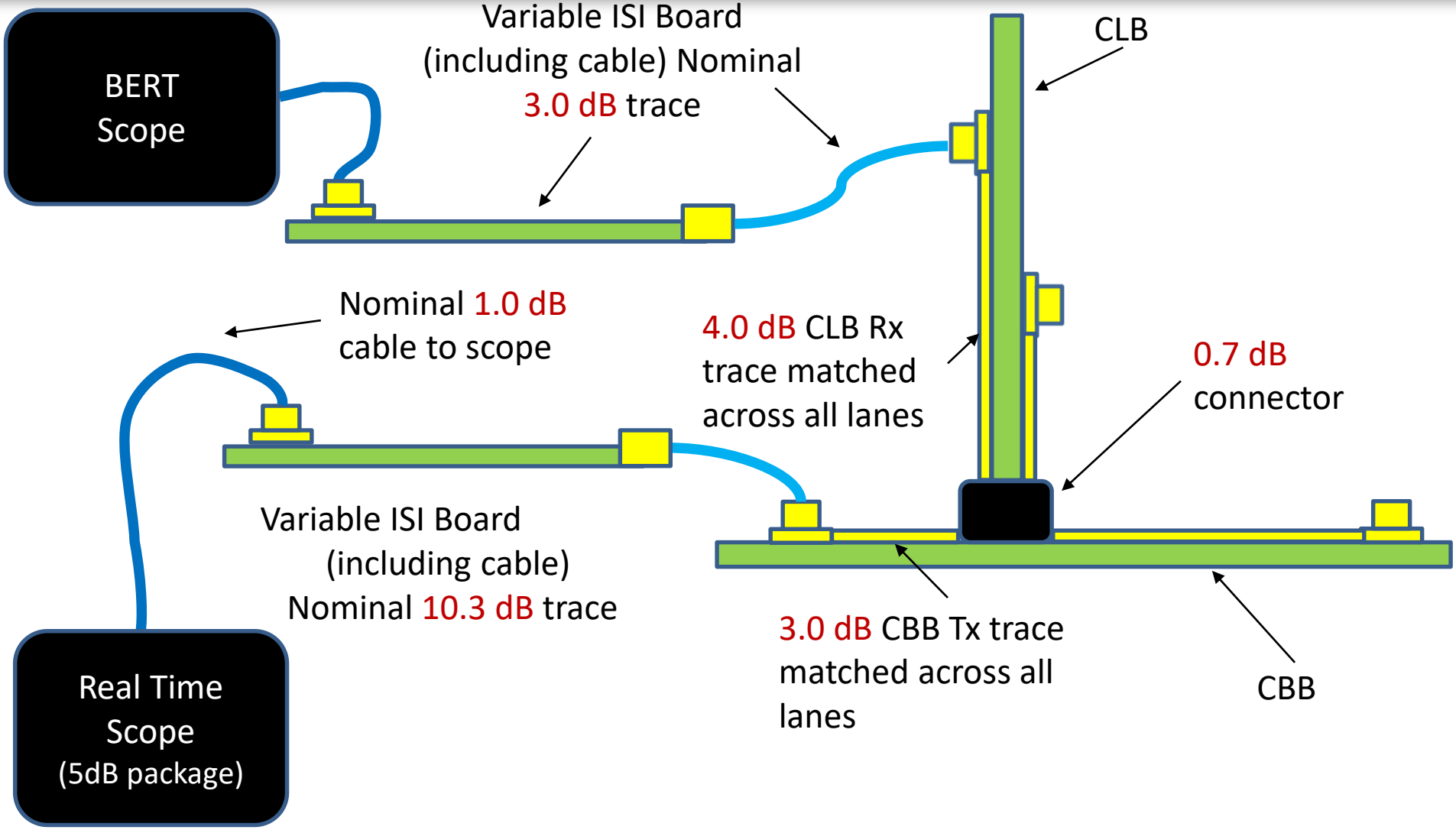

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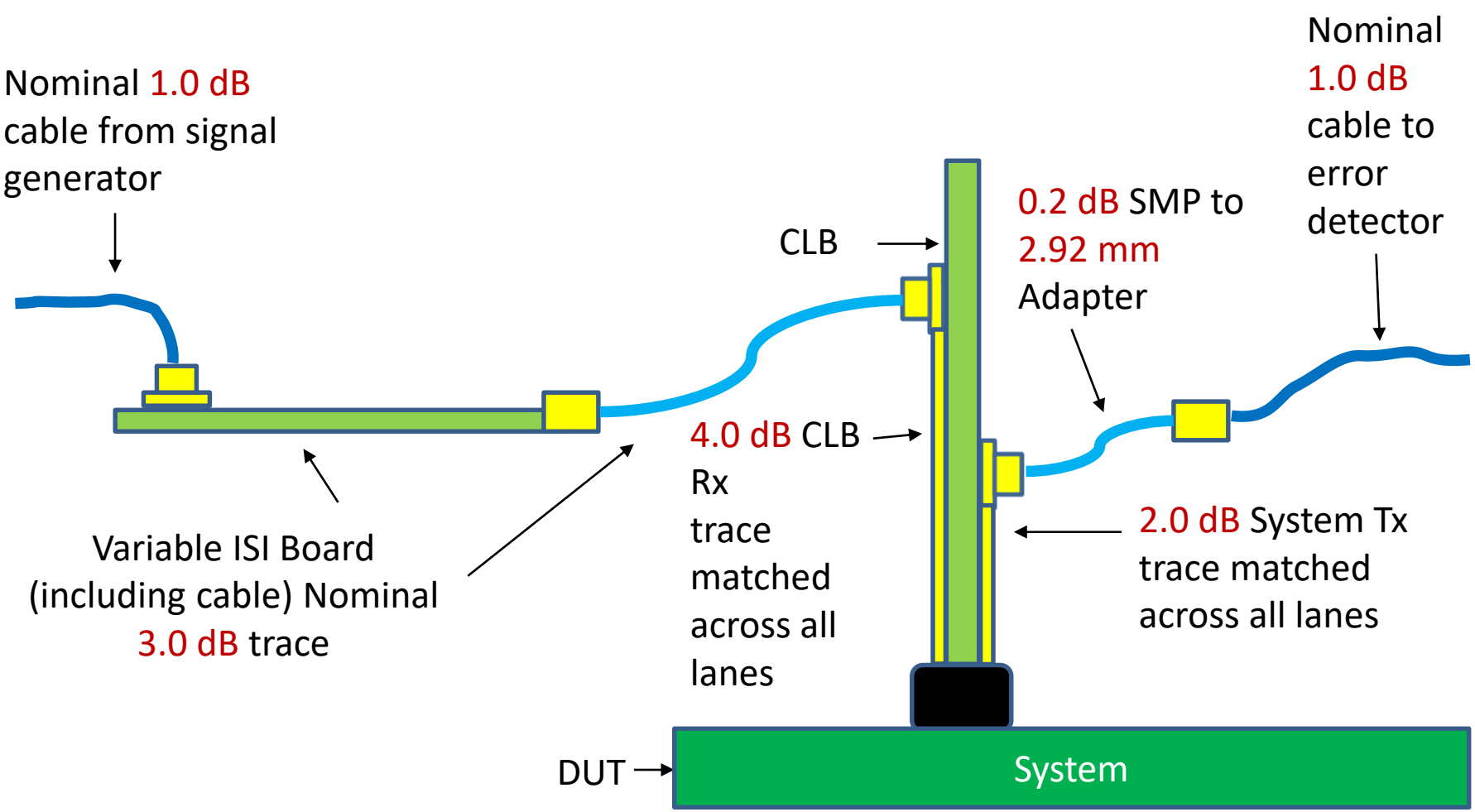


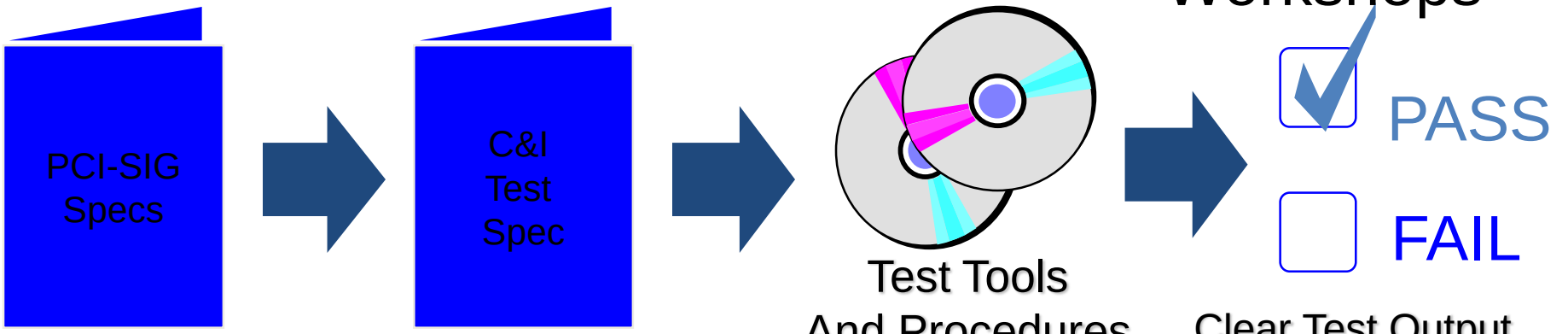
Link Equalization Tests

- **Tests Required for 8GT/s & 16GT/s**
- **Requires protocol-aware test equipment**
  - LeCroy PERT used
  - Keysight BERT recently approved through SEG
- **Tx link equalization response test**
  - Use protocol-aware test equipment to request a Tx equalization change
  - Check that the DUT responds and sets its Tx to the correct preset within required time period
  - Measurement of DUT Tx done by going to loopback and sending compliance pattern
  - Do this check for all presets
- **Rx link equalization**
  - Calibration the same as standard Rx test
  - Start with a non-optimal Tx equalization setting (P7 or P8)
  - Allow DUT to request for equalization adjustments
  - Place DUT into loopback
  - Monitor bit stream for errors

Compliance Program Overview

- **PCIe® 4.0 Test Program Under Development**
- **PCIe 3.0 Integrators List testing (started April 2013)**
  - Tests for 2.5, 5, 8 GT/s maximum data rates
- **Card Electromechanical (CEM) form factor only**
  - FYI testing underway for SFF-8639/U.2
    - Devices can get on Integrator's List if tested separately as CEM w/adapter
  - M.2 (Socket 3) under development
- **PCI™, PCI-X™, PCIe 1.x retired as of Jan 1, 2013**
  - PCIe 2.0 testing continues until 4.0 officially commences
  - 2.5 and 5 GT/s testing will continue as part of 3.0/4.0 process

PCIe 3.0 Compliance Process



PCI-SIG Specs
Describes
Device Requirements
• 3.0 Base and CEM specs

C&I Test Specs
Define
Test Criteria based on spec requirements
- •Test Definitions
- • Pass/Fail Criteria

Test H/W & S/W
Validates
Test Criteria
- •Compliance
- •Interoperability

Clear Test Output
Maps
Directly to Test Spec

Predictable path to design compliance

Same process as 1.x, 2.x

PCIe 3.0 Compliance Test Overview

- **Physical Layer**
  - 3.0 CLB and CBB fixtures
  - Add receiver and link equalization testing
  - New Sigtest
    - Reference CTLE+DFE
    - Test Channel Embedding
  - New Clock Tool
    - Provides clock phase jitter test to 3.0 base specification
  - PLL Bandwidth
- **Configuration Space**
  - Updated PCIeCV for new fields and capabilities
- **Link & Transaction Layer**
  - Run existing 2.0 tests at 8GT/s for 3.0 8GT/s capable devices
  - New tests covering link equalization and other new features
- **Platform Configuration**
  - Run existing tests at 8GT/s
  - New tests for 3.0

1.0 Test Specs Available

Compliance Workshop: Overview

- **Usually announced 2 months in advance**
  - Registration closes 3 weeks prior for domestic, and 4 weeks prior for international
  - No on-site registration!!!!
- **Testing is done using the standard CEM form factor**
  - Others under development
- **Passing at a workshop is the only way to be listed on the PCI-SIG Integrators List**
  - Pass all gold suite tests
  - Pass interoperability testing

Compliance Workshop: Interoperability Testing

- **Systems get rooms**
- **Add-in cards travel room to room**
- **Switches run both paths**
- **Goal: demonstrate interoperability between products**
- **80% passing rate required for eligibility for PCI-SIG Integrators List**
- **Demonstrate that the link can train and operate at the highest common link speed supported**

Electrical Tests

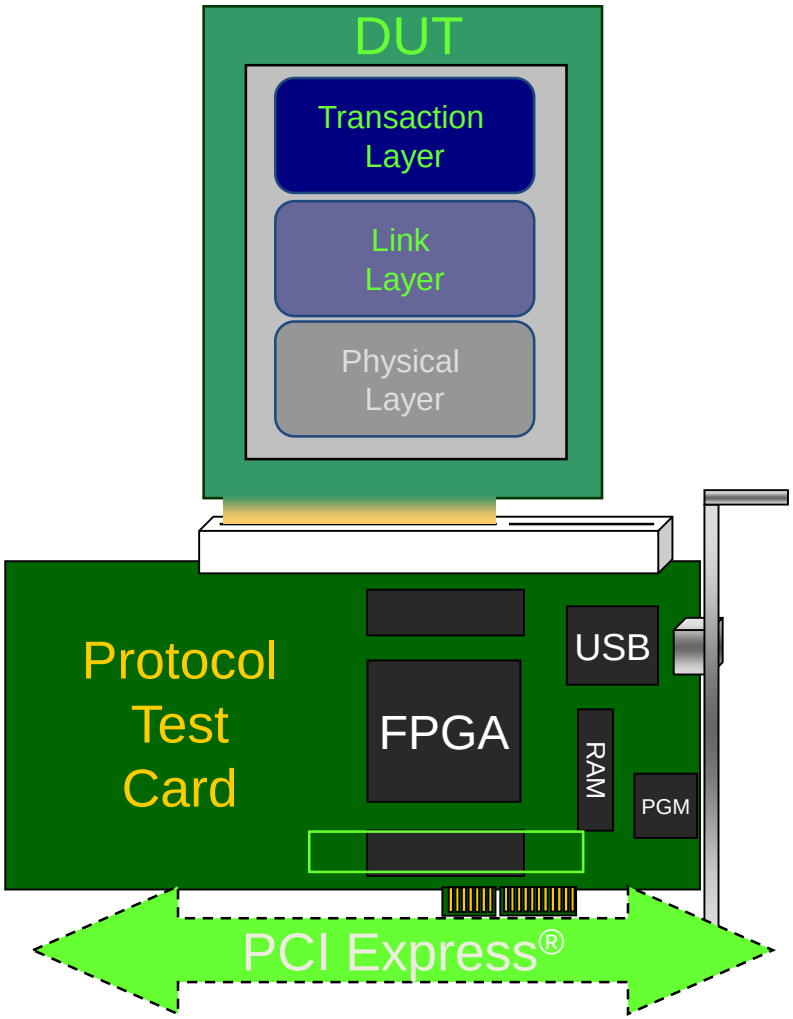
PCIe 3.0 Required Electrical Tests

- **Tx signal quality test at all supported link speeds (similar to 2.0 procedure)**
- **PLL bandwidth**
- **5.0GT/s selectable de-emphasis test**
- **Tx preset equalization test**
- **8.0GT/s receiver test**
- **Link equalization handshaking**
  - Required Tx adjustments
  - Requesting link partner to adjust if needed

Detailed test equipment specific test procedures for Tx and Rx testing available at PCI-SIG website

Protocol Testing

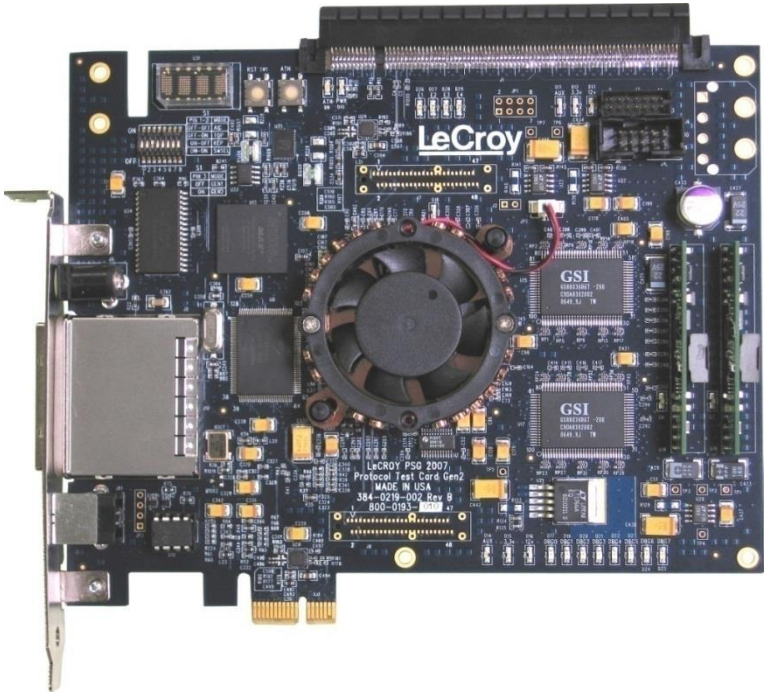
PCIe Protocol Testing



- **Test Control software running on platform or Device Under Test (DUT) initiates test traffic**
- **PTC monitors and acts on that traffic**
  - Checking protocol
  - Injecting errors

PCI Express® PTCs

- **x16 mechanically, x1 electrically**
- **2.0 - Agilent or LeCroy 2.0 PTC used**
- **3.0 - Agilent 3.0 PTC or LeCroy 3.0 PTC used**



PCIe Link / Transaction Compliance Tests

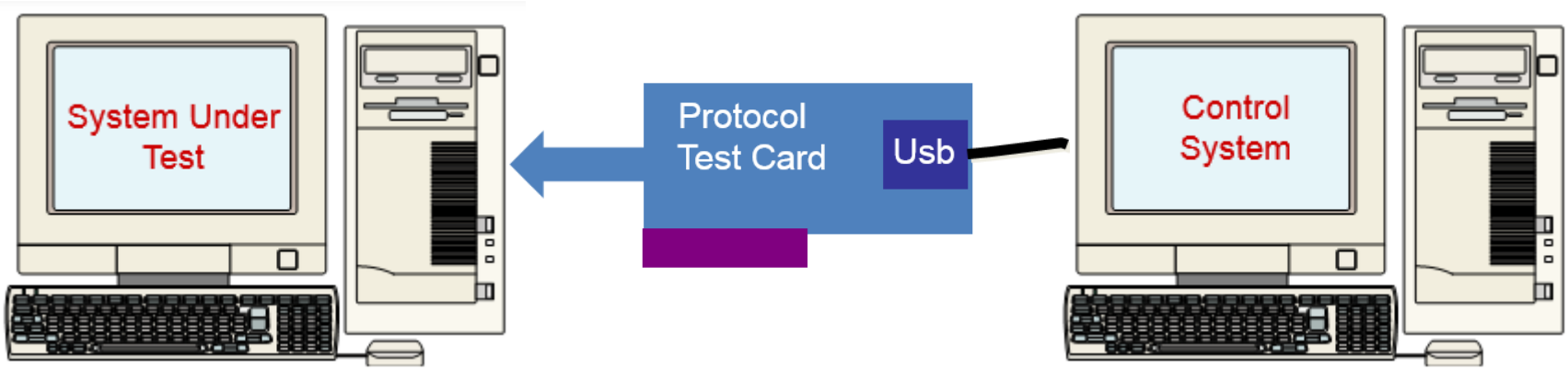
- **Described in Link Layer Test Spec and Transaction Layer Test Spec**
  - Merged test spec for 3.0
- **Speed requirement**
  - Must be run at highest supported link speed
- **Tests (from 1.x)**
  - Reserved fields – Device ignores them
  - NAK response – Device will resend after receiving NAK
  - Replay Timers – Device will resend packet if no response
  - Replay Count – Device will resend multiple times when no response
  - Link Retrain – Device will retrain if continued no response
  - Replay TLP order – Device replays TLPs in proper order
  - Bad CRC – Device detects, drops, and logs (DLLPs & TLPs)
  - Undefined packet – Device ignores
  - Bad Sequence Number – Device detects, drops, and logs
  - Duplicate TLP – Device returns data once
  - Request Completion – Issue UR for config requests not supported

PCIe 3.0 Protocol Tests

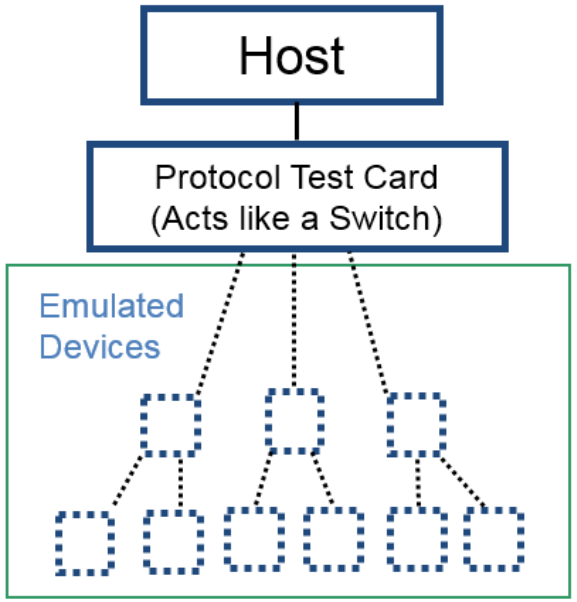
Test Name	Description
5GT/s selectable de-emphasis testing	FYI for 2.0, required for 3.0
Link Equalization Protocol	Verifies DUT responds to Tx EQ adjustment requests
Loopback (informative, implemented)	Enables receiver electrical testing
Function Level Reset	Only for endpoints that support FLR
Latency Tolerance Requests	Check that upstream port sends properly formed LTR requests
Link Partner Enters/Exists Compliance Mode (informative)	Verify the DUT attempts link training
SKP Processing (informative)	Verify DUT can process a variety of SKPs
L1 for D3 state	Verifies DUT requests L1 entry when it goes to D3
ECRC	Generates correct ECRC
Reserved Bit Test	Extension of 2.0 test for 3.0, add reserved bit monitoring

Platform BIOS Testing

Platform BIOS Testing



- **Protocol Test Card Can Represent Any Hierarchical Multi-Device Topology**
- **Device Decodes All Type 0 and Type 1 Configuration Cycles**



All BIOS testing run using 3.0 PTC at workshops

PCIe BIOS Test

- **Multiple Functions per device**
- **Different BAR combinations**
  - I/O, Mem, 64bit
  - Various size requests
  - Prefetchable, non-prefetchable
- **Bridges With Resource Requests**
- **ASPM Configurations**
- **Option ROMs**
  - Varying sizes
  - Different for each device function
  - Shrinkable, removable
- **Complex Multiple Switch and Bridge Topologies**
- **2.0 updates:**
  - Use 3.0 PTC
  - No functional changes since 1.1
  - Run at 5.0GT/s as FYI

3.0 BIOS Tests

- **New capabilities present in devices (ACS, IOV, etc…)**
- **Max payload size**
  - All functions of a multi-function device are set to the same max payload size
- **Common clock test**
  - Common clock config bit should be set to the same on both sides of the link
- **Slot Power Test**
  - Configure x16 slots with >25W
- **ASPM optionality (new for 3.0)**
  - Only enable ASPM (L0s or L1) if both sides support it
- **VC mapping**
  - TC mapped to only one VC
- **Clock power management**
  - Should not be enabled on CEM form factor

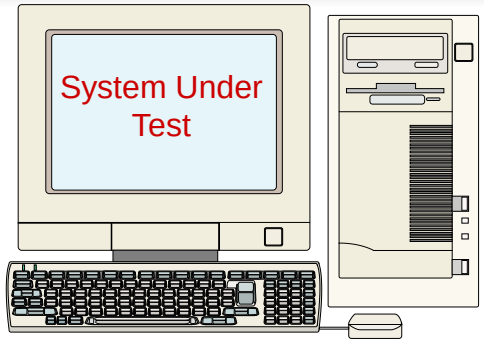
Review the test spec for details!

Full PCIe 3.0 Bios Tests Available at Workshops

Configuration Tests

Configuration Tests – Diagram

System Test (YI only)



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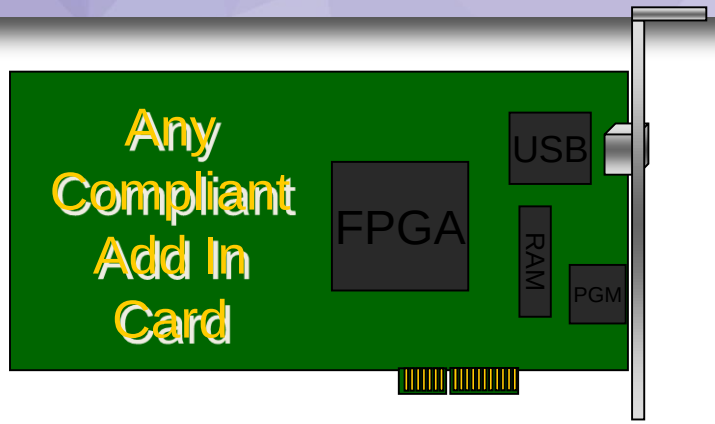
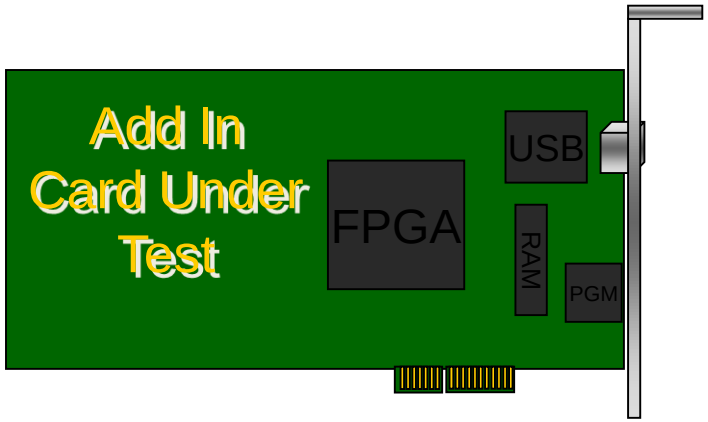


Add in Card Test



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Commercially available gold system used for 2.0 and 3.0 testing

PCIECV – 2.0 Link Speed Test

- **Gold System**
  - 5GT/s capable, 2.0 spec compliant system used for testing add-in cards

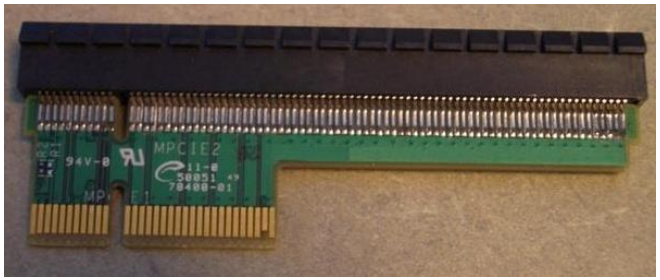
- **Set target link speed to limit maximum link speed and then write retrain link bit. Disable autonomous width or bandwidth changes on both components**
  - Upstream 2.5 Downstream 5.0 Result 2.5
  - Upstream 5.0 Downstream 5.0 Result 5.0

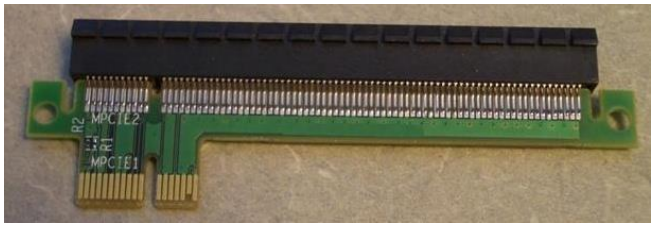
- **Test criteria**
  - Autonomous Bandwidth Status must never be set
  - Config registers must never be reset
  - Actual link speed matches expected link speed

PCIECV – 2.0 Link Width Test

- **CEM 2.0 spec requires x4 and x8 to be supported as intermediate widths**
- **Specified in 2.0 Config test spec**
- **Testing only static link width support**
- **Use low cost mechanical adaptors to do all testing with standard x16 slot**
- **Insert in riser card, and check that the link comes up in the correct link width**

Connector / Card	x1	X4	X8	x16
x1	Required	Required	Required	Required
x4	No	Required	Required	Required
x8	No	No	Required	Required
x16	No	No	No	Required





PCI Express 3.0 Config Tests

- **PCIECV 3.0 update released**
  - 2.1 spec updates
    - E.g. ARI, DPA, Resizable BAR, Multi-cast, LTR, TPH extended capabilities
  - Run tests at 8GT/s
  - 3.0 config space updates
    - Secondary PCI Express extended capability
  - IOV Capabilities
    - E.g. ATS Extended Cap, SR-IOV extended cap
- **PCIECV 1.5.2.4 update released**

Review the test spec for details!

Full PCIECV 3.0 version available at workshops

Thank you for attending the PCI-SIG Developers Conference Israel 2017.

For more information please go to www.pcisig.com