Professional Development Course

PDC 1: Nanotechnologies for Microelectronics Packaging Applications: Current trends in IoT, Wearable, 3D, Flex Circuits, Thermal and Embedded passives

Course Leader: James E. Morris

Affiliation: Department of Electrical & Computer Engineering, Portland State University, Portland, OR 97207-0751, USA

PDC 2: 3D Integrated Circuits Failure Analysis

Course Leader: Ingrid De Wolf, Prof.

Affiliation: IMEC, Belgium & KULeuven, Belgium

PDC 3: Fan-In and Fan-Out in Wafer Level Packaging

Course Leader: Albert Lan

Affiliation: Senior Director, Engineering Center, SPIL, Taiwan

PDC 4: Energy Efficient Thermal Management of Data Centers

Course Leader: Yogendra Joshi

Affiliation: G.W. Woodruff School of Mechanical Engineering Georgia Institute of Technology, Atlanta, GA 30332

PDC 5: Internet of Things (IoT) focusing on Wireless Sensors Network and Active RFID

Course Leader: Holden Li

Affiliation: Tamasek Laboratory at Nanyang Technological University

PDC 6: 2.5D- and 3D-Stacked Integrated Circuits

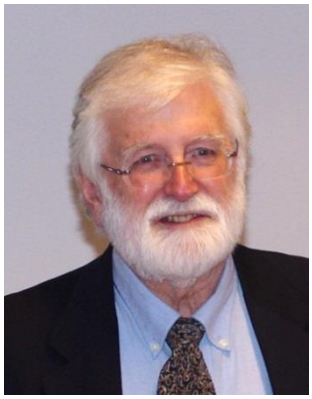
Course Leader: Paul Franzon,

Affiliation: NCSU

Enquiries :

PDC Chair
Riko I Made
riko.imade@smart.mit.edu
www.eptc-ieee.net

General Chair
Ranjan Rajoo
ranjan.rajoo@globalfoundries.com



PDC 1: Nanotechnologies for Microelectronics Packaging Applications: Current trends in IoT, Wearable, 3D, Flex Circuits, Thermal and Embedded passives

Course Leader: James E. Morris

Affiliation: Department of Electrical & Computer Engineering, Portland State University, Portland, OR 97207-0751, USA

Course Description: The course begins with an introduction to electronics packaging for context, which includes the current trends in IoT, wearable, 3D, flex circuits, thermal and embedded passives. It then focuses on the application of nanoparticle and CNT properties to the enhancement of packaging materials for reliability, e.g. by melting-point depression, sintering, Coulomb blocks, enhanced chemical activities, high mechanical strength, low ballistic resistance, etc. At the same time it will discuss applications of nanowires and other nanoscale structures.

Course Outline:

(1) Introduction to Electronics Packaging and current trends: IoT, flex circuits, wearables, 3D thermal, embedded passives, etc.
(2) Introduction to Nanotechnologies in Electronics Packaging
(3) Nanoparticle properties: melting point depression, coulomb block, sintering, optical, etc
(4) Nanoparticle fabrication
(5) Nanoparticles for high-k dielectric capacitors and resistors for embedded passives
(6) Nanogranular magnetic core inductors for embedded passives
(7) Nanoparticles in electrically conductive adhesives,
(8) Nanoparticles in microvias and conductive inks for SMT interconnect
(9) Nanoparticles added to lead-free solders and flip-chip underfills
(10) CNTs: fabrication, characterization (chirality, etc), and properties
(11) CNT effects in solders
(12) CNTs for thermal management and electromagnetic shielding
(13) Graphene for thermal management
(14) Nanowires and nanoscale spring interconnects
(15) Current commercial applications of nanopackaging
(16) Nanoscale modeling and simulation
(17) Summary

The course will be beneficial to electrical, mechanical, and materials engineers alike, or anyone with an interest in electronic device design, fabrication, assembly, or application. The level will be introductory, and accessible to students and graduates in any of these areas or the physical sciences.

Biography

Jim is a Professor Emeritus of Electrical & Computer Engineering at Portland State University, Oregon, and at the State University of New York at Binghamton. His B.Sc. and 1st Class Honors M.Sc. degrees in Physics are from the University of Auckland, New Zealand, and his Ph.D. in Electrical Engineering is from the University of Saskatchewan, Canada. He has served as Department Chair at both Binghamton and Portland, and was the founding Director of Binghamton's Institute for Research in Electronics Packaging. Jim has also held faculty positions at Saskatchewan, Victoria University of Wellington (NZ), and South Dakota School of Mines & Technology, with visiting/sabbatical positions at

Loughborough University (UK) as a Royal Academy of Engineering Distinguished Visiting Fellow, Chemnitz University of Technology (Germany), University of Maryland (USA), University of Bordeaux (France), University of Greenwich (London), Chalmers University of Technology (Sweden), Dresden University of Technology, University of Canterbury (NZ) as an Erskine Fellow, and Helsinki University of Technology as a Nokia-Fulbright Fellow, with honorary appointments at Shanghai University and Shanghai Jiao Tong University. Other positions have included Senior Technician and Post-Doctoral Fellow at the U of S, brief periods with Delphi Engineering (NZ) and IBM-Endicott (New York), and industrial consulting. He was recognized in 2015 with an honorary doctorate from the POLITEHNICA University of Bucharest.

Jim is an IEEE Fellow and an IEEE Components, Packaging, & Manufacturing (CPMT) Society Distinguished Lecturer. He has served as CPMT Treasurer (1991-1997) and Vice-President for Conferences (1998-2003), and currently sits on the CPMT Board of Governors (1996-1998, 2011-2016) and on the joint Oregon CAS/CPMT Chapter executive committee, and chairs the CPMT Nanotechnology technical committee. He was awarded the IEEE Millennium Medal and won the CPMT David Feldman Outstanding Contribution Award in 2005. He is an Associate-Editor of the IEEE CPMT Transactions and has been General Chair of three CPMT-sponsored conferences, Treasurer or Technical Chair of others, and serves on several CPMT conference committees. As the CPMT Society representative on the IEEE Nanotechnology Council (NTC), he instituted a regular Nanopackaging series of articles in the IEEE Nanotechnology Magazine, established the NTC Nanopackaging technical committee, (which also acts as a program committee for annual IEEE NANO conferences,) served as the 2010-2012 NTC Awards Chair, chaired the IEEE NANO 2011 conference in Portland, and served as NTC Vice-President for Conferences (2013-2014) and currently as Vice-President for Finance. He also co-founded the Oregon Chapter of the IEEE Education Society in 2005 and sits on its executive committee, and was Program Chair for the 1st and 2nd IEEE Conferences on Technology for Sustainability (2013/14).

His research activities are focused on electrically conductive adhesives, the electrical conduction mechanisms in discontinuous nanoparticle thin metal films, with applications to nanopackaging and single-electron transistor nanoelectronics, and on an NSF-funded project in undergraduate nanotechnology education. He has edited or co-authored five books on electronics packaging and two on nanodevices, and lectures internationally on nanopackaging and electrically conductive adhesives. He is currently putting together the expanded second edition of his book: “Nanopackaging: Nanotechnologies and Electronics packaging” (Springer, 2016.).

PDC 2: 3D Failure Analysis

Course Leader: Ingrid De Wolf, Prof.

Affiliation: IMEC, Belgium & KULeuven, Belgium

Course description: In 3D stacked-IC technology, thinned Si wafers/dies are vertically interconnected offering faster and more compact electronic circuits with heterogeneous integration capabilities. The stacked wafers/dies are electrically interconnected using µ-bumps and Cu TSVs (Through Silicon Vias). However, the introduction of these new materials and new fabrication schemes is associated with new failure mechanisms requiring new failure analysis (FA) techniques. In addition, even for well-known failures in 2D-chips, pin-pointing the failure location becomes increasingly challenging because of a combination of inaccessibility of the devices (part of a 2.5D or 3D stack) with small dimensions and high density of the devices.

In this course, after a short introduction to 3D technology and failure analysis, various failure analysis techniques that can be used for FA of 3D technology are discussed in detail. Their principle is explained, the advantages and limitations for 3D technology-FA are discussed, and typical case studies are presented. The course will cover well known classical techniques, such as for example X-ray, scanning acoustic microscopy (SAM) and magnetic field imaging, but also new developments of these techniques. In addition, less conventional techniques (ex. lock-in thermography, polariscopy, EOTPR and some recent new electrical test-based techniques) will be covered.

Course Outline:

(1) Introduction
(2) 3D technology
- short introduction to the technology (aim, TSV, micro-bumps, thinning and stacking, Cu pillars,...)
- overview of expected failure mechanisms in 3D technology

(2) Failure analysis
- what, why, 2D versus 3D
- failure analysis sequence
- challenges

(3) Overview of 3D FA techniques (+ case studies)
- Infra-red microscopy
- X-ray based techniques
- Acoustic techniques (SAM, GHz SAM, acoustic signals)
- Magnetic field/current imaging methods
- TDR and EOTPR
- Polariscopy
- Photon emission microscopy

- Lock-in thermography
- New e-test based techniques

(4) Conclusions

Biography: Ingrid De Wolf received the PhD in Physics from the KU Leuven university, Belgium, in 1989. In the same year she joined imec in Belgium, where she worked in the field of microelectronics reliability, with special attention for gate oxide reliability, mechanical stress analysis using micro-Raman spectroscopy and failure analysis using emission microscopy. From 1999 to 2014, she headed the group REMO, where research is focused on reliability, test and modelling of 3D technology, interconnect, MEMS and packaging. She managed to grow this group from a small team of 3 members to a highly recognized group of about 40 people which is involved in several programs within imec (3D, interconnect, Optical IO, GaN, Litho, PV, MEMS, STT-MRAM...). She authored or co-authored 14 book chapters and more than 350 publications of which ~30 invited, and won several best paper awards at conferences focusing on reliability and failure analysis (ESSDERC, ESREF, ISTFA, EOS/ESD symposium, IEDM). She was often involved as session chair or technical committee member of these conferences, and is member of the steering committee of ESREF. She is chief scientist at imec, IEEE senior member and professor at the department of Metallurgy and Materials Engineering of the KU Leuven where she teaches courses on non-destructive testing, MEMS reliability and failure analysis, characterization techniques and FMEA.

PDC 3: Fan-In and Fan-Out in Wafer Level Packaging

Course Leader: Albert Lan

Affiliation: Senior Director, Engineering Center, SPIL, Taiwan

Course description:

The Wafer Level Package (WLP) continues to see strong growth driven by mobile phones, tablets, portable players, wearable and IoT devices with its benefits of small form factor and low profile packages.

In this course, we will introduce the innovative solutions of WLP include mold type WLCSP (mWLCSP), Fan-out Wafer Level Package (FOWLP). Also, the future trend will be covered Panel Level FO technology.

Course Outline:

(1) Introduction
(2) What is Wafer Level Package
(3) Market Trend of Wafer Level Package
(4) Innovative Package Solutions Introduction and Challenge
(5) Molded WLP (mWLCSP)
(6) Fan-Out WLP (FOWLP)
(7) Future Package Solutions Introduction and Challenge
(8) Panel Level Fan-Out (PLFO)
(9) Summary

Biography

Education:

- Master of industrial & mechanical engineering department, Univ. of Wisconsin, Madison

- Job Experience:
  - Over 20 years of job experience on semiconductor industry, especially focus on bumping and flip chip advanced assembly technology.
  - Vice Chairman of Semiconductor Equipment and Materials International Taiwan Association.
  - Chairman of TILA (Taiwan Intelligent Leader Association)
- Now :
  - Senior Director of Engineering Center of SPIL (Siliconware, Taiwan), which is 3rd biggest assembly house in the world now

PDC 4: Energy Efficient Thermal Management of Data Centers

Course Leader: Yogendra Joshi

Affiliation: G.W. Woodruff School of Mechanical Engineering
Georgia Institute of Technology, Atlanta, GA 30332

Course Description: While a number of energy efficiency initiatives have recently resulted in slowing the growth rate of energy consumption by data centers, currently about 3% of the electrical energy produced in the world is consumed by data centers. As much as 20%-50% of this is associated with the operation of the cooling hardware. In this course, I will focus on energy efficient thermal management of data centers. Starting from the trends in energy consumption by cabinets and data centers, I will discuss the currently used metrics to quantify their energy efficiency and sustainability. I will discuss the evolution of the environmental guidelines for data centers, prescribed by the American Society of Heating refrigeration and Air Conditioning (ASHRAE). I will then focus on approaches to improve energy efficiency of air-cooled data centers. Emerging trends such as improved air delivery, aisle containment, and "free cooling" will be discussed. Concepts of model based robust and sustainable design of data center facilities of the future will be addressed. A growing segment of data centers are high performance computing (HPC) installations. The growth towards exa-scale computing imposes some of the most serious thermal management and energy efficiency challenges for such facilities. Advanced thermal management approaches including hybrid liquid/air cooling, and liquid immersion cooling to handle the projected sharp increases in server heat loads in HPC will be discussed.

Course Outline: The course will present the following topics:

(1) Energy consumption trends by servers, cabinets, and data centers
(2) Energy efficiency metrics
(3) Environmental control guidelines evolution
(4) Current state-of-the-art of data center thermal management
(5) Emerging trends for energy efficiency improvement
    - Improved tile air delivery
    - Aisle containment
    - "Free cooling"
(6) Energy efficiency enhancements in air cooled data centers through cooling advances
    - Metrology
    - Modeling and sustainable design
(7) Thermal management for High performance computing
    - Hybrid, and indirect liquid cooling
    - Direct liquid cooling
(8) Future thermal management trends

References:

- *Energy Efficient Thermal Management of Data Centers*, Yogendra Joshi and Pramod Kumar, Editors, Springer, 2012.
- *Air Flow Management in Raised Floor Data Centers*, Vaibhav K. Arghode, and Yogendra Joshi, Springer, 2016.

Biography: *Yogendra Joshi* is Professor and John M. McKenney and Warren D. Shiver Distinguished Chair at the G.W. Woodruff School of Mechanical Engineering at the Georgia Institute of Technology. His research interests are in multi-scale thermal management. He received a Ph.D. in Mechanical Engineering and Applied Mechanics, from the University of Pennsylvania in 1984. He is the author or co-author of over 320 archival journal and conference publications, and is an elected Fellow of the ASME, the American Association for the Advancement of Science, and IEEE. He was a co-recipient of ASME Curriculum Innovation Award (1999), Inventor Recognition Award from the Semiconductor Research Corporation (2001), the ASME Electronic and Photonic Packaging Division Outstanding Contribution Award in Thermal Management (2006), ASME J. of Electronics Packaging Best Paper of the Year Award (2008), IBM Faculty Award (2008), IEEE Semitherm Significant Contributor Award (2009), IIT Kanpur Distinguished Alumnus Award (2011), ASME InterPack Achievement Award (2011), ITherm Achievement Award (2012), and ASME Heat Transfer Memorial Award (2013).

PDC 5: Internet of Things (IoT) focusing on Wireless Sensors Network and Active RFID

Course Leader: Holden Li

Affiliation: Tamasek Laboratory at Nanyang Technological University

Course Outline

This short course focuses on the technology and markets enabling the Internet of Things (IoT), especially related technologies such as Wireless Sensor Network and Active RFID. The class will discuss in detail generic IoT sensors, especially MEMS based one, that are commonly used and also upcoming ones; technologies progression over the past ten years and looking beyond; reality versus the hype, etc.

It will also specifically address issues like the hardware advantages and disadvantages for each choice. Participants will have a better understanding of what IoT is and which part does wireless sensing and RFID play. Other interesting topics include the architecture of IoT from the ground up; traditional Active RFID, RFID enabled cellphones, smart active labels/ battery assisted passive tags, and Wireless/Ubiquitous Sensor Networks (USN). Lastly, a brief introduction on the various energy harvesting mechanisms will also be discussed.

Course outline:

(1) Introduction and background of IoT
(2) RFID System Basics
(3) Various RFID related technologies used in IoT
(4) RFID related application in Singapore
(5) Wireless Sensor Networks (WSN)
(6) WSN in Singapore context
(7) Enablers of IoT – Energy Harvesting
(8) Real Time Location Systems
(9) Tradeoff studies of various technologies
(10) Related Opportunities in Singapore and South East Asia

Biography

Dr Holden Li graduated in NUS with a Bachelor of Engineering (Honors) in 1997. In 2000 Holden enrolled in Stanford University for his graduate studies under Professor Thomas Kenny. During his PhD studies, Dr Holden Li was actively involved in MEMS process development in finding suitable packaging solutions to MEMS and BioMEMS devices. Besides, he worked closely with several industrial partners who benefited from the on-going research activities in Kenny's group at that time. He was awarded his MSc and PhD in Mechanical Engineering in 2001 and 2005 respectively. Back in Singapore in September 2005, he started to lead a research team in MEMS sensors research effort in the area of MEMS R&D and reliability study. Beyond this, his passion for R & D in microelectronics, and his strong academic interest in the area of micro and nanotechnology propelled him to seek for funding opportunity in this area. He is currently working closely with several senior faculties in the area of microelectronics, MEMS research and Internet of Things (IoT) applications both in NTU and Temasek Laboratories at NTU. He is serving on the National Committee of Semiconductor Devices

PDC 6: 2.5D- and 3D-Stacked ICs

Course Leader: Paul Franzon,

Affiliation: NCSU

COURSE OUTLINE

Three dimensional chips stacked using Through Silicon Via (TSV) technology has been under consideration and the subject of intensive research for several years now. This tutorial covers the technology, applications, design and CAD for 3DIC. The technology will be introduced, including TSVs, face to face technologies, integration options and interposers. Applications will be discussed as driven by cost, performance and power efficiency needs. Examples will be given from the commercial world and the author's own research. CAD and CAD-driven design will be covered including verification, test, and thermal evaluation

Outline

(1) 3DIC Motivation
   a. Power Efficiency
   b. Memory Bandwidth
   c. Bandwidth density
   d. Heterogeneous Integration
   e. Cost reduction

(2) 3DIC Manufacturing
   a. Bulk TSV formation
   b. SOI TSV formation
   c. Wafer and chip assembly flows
   d. Interposers

(3) 3DIC Design and Test
   a. Power and power efficiency
   b. Memories and memory interfaces
   c. The potential for logic partitioning
   d. CAD flows
   e. Thermal design
   f. Power delivery

(4) Test
   a. Test issues
   b. Potential Test Flows
   c. Test standards
   d. Cost issues

(5) Conclusions and Future perspectives.

Biography

Paul D. Franzon is currently a Distinguished Professor of Electrical and Computer Engineering at North Carolina State University. He earned his Ph.D. from the University of Adelaide, Adelaide, Australia. He has also worked at AT&T Bell Laboratories, DSTO Australia, Australia Telecom and three companies he cofounded, Communica, LightSpin Technologies and PBI Inc. His current interests center on the technology and design of complex microsystems incorporating VLSI, MEMS, advanced packaging and nano-electronics. He has lead several major efforts and published over 200 papers in these areas. In 1993 he received an NSF Young Investigators Award, in 2001 was selected to join the NCSU Academy of Outstanding Teachers, in 2003, selected as a Distinguished Alumni Professor, and received the Alcoa Research Award in 2005. He served with the Australian Army Reserve for 13 years as an Infantry Solider and Officer. He is a Fellow of the IEEE.